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Optical receiver design and optimisation for multi-gigahertz applications

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Optical Receiver Design and Optimisation for Multi-Gigahertz Applications

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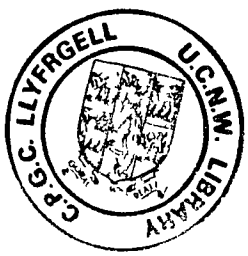

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Summary

This thesis is concerned with structures and design techniques appropriate for the realisation of integrated optical receivers operating at multi-gigahertz frequencies. The development and practical proving of novel signal designs tailored specifically to very high bit-rate optical communication systems is reported. Timing imperfections and signal dependent noise - a result of the optical amplification deployed in all high-performance systems - are two major impairments that must be accommodated if optimum system performance is to be achieved. Here, a signal design that accommodates these impairments is developed and compared to established designs. The new signal designs are shown to provide improved performance, in particular, they exhibit tolerance to uncertainty in the exact level of the impairment.

Following the derivation of the signal designs a range of practical realisations are described. A receiver amplifier GaAs MMIC for 4.8 Gbit/s operation with embedded signal shaping is described followed by the design and test of integrated post-detection filters for 10 and 15 Gbit/s systems. The susceptibility of the embedded signal shaping receiver to variations in photodiode capacitance leads to the development and test of a low input-impedance common-gate 5 Gbit/s GaAs MMIC receiver. To effect signal shaping at very high data-rates a modified distributed amplifier structure is proposed which better utilises the capabilities of the available foundry processes. Two distributed amplifier based optical receivers with embedded signal shaping are devised and simulation results for 10 Gbit/s show the efficacy of this design approach. The implications of noise matching are investigated and a 2 GHz SCM receiver is used as a vehicle to illustrate the methods developed.

The long term goal of receiver design is to fully integrate both optical and electrical components onto a single chip. A preliminary investigation of the feasibility of this goal is carried out on an experimental InP-based process. Two receiver designs for 10 Gbit/s were prepared as a precursor to a detailed design of an OEIC with embedded signal shaping that incorporates the novel topologies developed during this work.

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List of Symbols

A_v	Voltage gain
$A_z(0)$	Midband closed loop transimpedance
$A_z(s)$	Closed loop transimpedance
A_{zo}	Midband open loop transimpedance
APD	Avalanche photodiode
b_o	Optical power $b_o \in \{b_{min}, b_{max}\}$
b_{max}	Optical power for a signal '1'
b_{min}	Optical power for a signal '0'
B	Bit rate
B_o	Optical bandwidth
BER	Bit error rate
BW	Bandwidth
c_{11}, c_{12}, c_{21}, c_{22}	Two-port chain matrix elements
C	Gate and drain noise correlation coefficient
$\mathbf{C}$	Two-port chain matrix
C_d	Photodiode capacitance
C_{dg}	Drain-gate capacitance
C_{ds}	Drain-source capacitance
C_f	Feedback capacitance
C_{gs}	Gate-source capacitance
CAD	Computer aided design
CB	Common-base
$\mathbf{C}_C$	Correlation matrix, chain representation
CD	Common-drain
CG	Common-gate
CS	Common-source
C_T	Total input capacitance
$\mathbf{C}_Y$	Correlation matrix, admittance representation
$\mathbf{C}_Z$	Correlation matrix, impedance representation
d	Decision threshold
$\frac{d}{dt}\langle i_d i_d^* \rangle$	Drain noise current power spectral density
$\frac{d}{dt}\langle i_g i_d^* \rangle$	Gate and drain noise currents cross-correlation spectral density
$\frac{d}{dt}\langle i_g i_g^* \rangle$	Gate noise current power spectral density
d_{opt}	Optimum decision threshold

DA	Distributed amplifier
e, e_1 and e_2	Noise voltage sources
E	Cost function
E_{isi}	Total ISI squared error
E_{td}	Total TD squared error
E_{zs}	Total ISI slope squared error
EDFA	Erbium doped fibre amplifier
f	Frequency
f_{cd}	Drain line cut-off frequency
f_{cg}	Drain line cut-off frequency
f_T	Current gain cut-off frequency
F_e	APD excess noise factor
F_{min}	Minimum noise factor
FA	Fibre amplifier
FET	Field effect transistor
FWHM	Full width at half maximum
g_{ds}	Drain-source conductance
g_m	Transconductance
g_{mo}	Absolute value of g_m
G	Optical gain
G_k	Gain coefficient; Stage gain
G_o	Real part of Y_{out}
$h_{0,n/2}$	ZFE output at intervals $T/2$
$h_{m,n/2}$	Matched filter output at intervals $T/2$
$h_o(t)$	Output pulse shape
$h'_o(t)$	Time derivative of $h_o(t)$
$h_p(t)$	Input pulse shape
$h_T(t)$	Linear receiver impulse response
$H_o(f)$	Fourier transform of output pulse
$H_p(f)$	Fourier transform of input pulse
$H_{DA}(f)$	Distribute amplifier transfer function
HFET	Heterojunction MESFET
$H_{FT}(f)$	Transversal filter transfer function
$H_M(f)$	Whitened matched filter transfer function
$H_T(f)$	Linear receiver frequency response
$H_\lambda(f)$	Zero forcing filter transfer function
i, i_1 and i_2	Noise current sources
$i_{eq}(t)$	Equivalent input noise current
i_d	Gate noise current
i_g	Drain noise current
I_1, I_2 and I_3	Noise integrals
I_{dss}	Saturated drain current
I_g	Gate leakage current
$\mathrm{Im}(\cdot)$	Imaginary part
I_p	Photodiode current

IFFT	Inverse fast Fourier transform
ISI	Intersymbol interference
k	Boltzmann's constant
l_d	Drain line inductance per unit length
l_g	Gate line inductance per unit length
L_d	Drain inductance
L_g	Gate inductance
L_s	Source inductance
m_t	Transverse mode number
M	APD gain
M1, M2, M3	Metal levels 1, 2 and 3
$M_n(s, h_T(t))$	MGF of the additive Gaussian noise
MCB	Modified Chernoff bound
MESFET	Metallic Schottky barrier FET
MFPP	Marked and filtered Poisson process
MGF	Moment generating function
MIM	Metal-Insulator-Metal
MMIC	Microwave Monolithic Integrated Circuit
$M_{Y_0}(s, h_T(t))$	Symbol conditioned MGF for symbol '0'
$M_{Y_1}(s, h_T(t))$	Symbol conditioned MGF for symbol '1'
n_{sp}	Population inversion parameter
N	Network order
NF_{min}	Minimum noise figure
NRZ	Non return to zero
NSD	New signal design
OA	Optical amplifier
OEIC	Optoelectronic integrated circuit
OTDM	Optical-time division multiplexing
$p(y \mid 0)$	Conditional PDF for a symbol '0'
$p(y \mid 1)$	Conditional PDF for a symbol '1'
p_n	n^{th} pole
P	Drain noise coefficient
$\overline{P}$	Sensitivity
$P(\tau)$	Power penalty
P_0	Probability of a symbol '0'
P_1	Probability of a symbol '1'
$P_{dB}(\tau)$	Power penalty in dB
P_{err}	Error probability
PDF	probability density function
PIN	p-i-n photodiode
PRBS	Pseudo random bit sequence
q	Electronic charge
$Q(\cdot)$	Gaussian Q-function
r	Jitter range
r_n	n^{th} residue

R	Gate noise coefficient
R_{co}	Electrode contact resistance
R_d	Drain resistance
R_{ds}	Drain-source resistance
$\mathrm{Re}(\cdot)$	Real part
R_f	Feedback resistance
R_g	Gate resistance
R_i	Gate charging resistance
R_{in}	Resistive portion of the input impedance
R'_{in}	Parallel combination of R_{in} and R_f
R_n	Noise resistance
R_s	Source resistance
$\mathcal{R}_s$	Responsivity
RC	Raised cosine
R_L	Load resistance
RZ	Return to zero
s	MCB adjustable parameter
$s(t)$	Pulse sequence at the input of the decision device
$s_{in}(t)$	Input signal
$s_{out}(t)$	Output signal
$S_{eq}(f)$	Spectral density of equivalent input noise current
$S_{in}(f)$	Input signal spectrum
$S_{out}(f)$	Output signal spectrum
S_{ser}	Series noise generator power spectral density
S_{shn}	Shunt noise generator power spectral density
SI	semi-insulating
SLA	Semiconductor laser amplifier
SNR	Signal to noise ratio
t	Time
t_s	Sampling instant
T	Bit period
$\mathbf{T}$	Transformation matrix
T_{gk}	k-th stage artificial gate line delay
T_{dk}	k-th stage artificial drain line delay
T_s	Pulse width (FWHM)
TD	Telegraph distortion
V_{DD}	Drain bias voltage
V_{GG}	Gate bias voltage
V_{SS}	Source bias voltage
$VSWR$	Voltage standing wave ratio
W_{isi}	ISI weight
W_{td}	TD weight
W_{zs}	ISI slope weight
WC_{isi}	Worst case ISI
y_{11}, y_{12}, y_{21}, y_{22}	Two-port admittance matrix elements

$\mathbf{Y}$	Two-port admittance matrix
Y_{opt}	Optimum noise admittance
Y_{out}	Output admittance
$Y_N(f)$	Equivalent noise admittance
z_{11}, z_{12}, z_{21}, z_{22}	Two-port impedance matrix elements
$\mathbf{Z}$	Two-port impedance matrix
Z_0	Line characteristic impedance
Z_{od}	Drain line characteristic impedance
Z_{og}	Gate line characteristic impedance
ZFE	Zero forcing equaliser
α	Spectrum roll-off factor
Γ	Excess channel-noise factor
$\delta(\cdot)$	Dirac impulse
Δ_k	matched line delay
ΔF_1	Equivalent noise bandwidth for σ^2_{sp}
ΔF_2	Equivalent noise bandwidth for σ^2_{sp-sp}
η	Quantum efficiency
θ	Absolute temperature
θ_0	Standard reference temperature
σ^2	Proportionality factor for OAs signal dependent noise
σ^2_0	Total mean square noise associated with a binary '0'
σ^2_1	Total mean square noise associated with a binary '1'
σ^2_c	electronic receiver mean square noise
σ^2_d	Mean square signal dependent noise
σ^2_t	Mean square signal independent noise
σ_{isi}	Intersymbol interference standard deviation
σ_o	Output noise standard deviation
σ^2_s	OA signal shot noise
σ^2_{sp}	OA spontaneous emission shot noise
σ^2_{sp-sp}	OA beat noise between spontaneous emission components
σ^2_{s-sp}	OA beat noise between signal and spontaneous emission
Σ_1	Noise summation
τ	Normalised timing offset; Tap delay
τ_g	Gate line interstage delay
τ_d	Drain line interstage delay
τ_k	k-th stage equivalent tap delay
τ_o	Carriers travel delay
τ_s	Soliton width parameter
$*$	Convolution
*	Complex conjugate
†	Hermitian conjugation

Chapter 1

Introduction

The very large bandwidth potential of optical fibre based systems and their low cost makes the optical fibre the preferred carrier for the long-haul telecommunication traffic. In fact, optical fibre communication systems cover 50% of the required capacity of all long-haul traffic world-wide and 70% in the UK [1]. Supporting new services such as tele-conferencing, high speed computer data networks, high definition cable TV and integrated services to the home necessitates research in the telecommunications industry directed towards the development of higher data rate systems in the interest of minimising the bit transport costs to the customer. Indeed, demonstrations of 10 Gbit/s optical systems are already common in laboratories worldwide [2, 3, 4, 5] and soliton, optical time division multiplexed and polarisation division multiplexed based system experiments demonstrating optical transmission out to 100 Gbit/s have been reported [6, 7, 8, 9]. As the bit rates increase lightwave systems employing optical amplifiers clea''y out-perform the more traditional regenerative systems [10]. As the systems evolve towards the use of optical amplifiers and higher bit rates, transmission impairments such as intersymbol interference, signal and timing jitter and signal dependent noise assume greater importance and must be considered in the system design process. In particular these impairments must be taken into consideration and included in the design and optimisation of optical receivers. Accordingly, in this thesis the development of rigorous design strategies for high performance optical receivers and their proof via practical realisation is considered for the next generation of optical systems.

1.1 Receivers and signal processing for direct detection optical communication systems

In direct detection optical communication systems the optical signal incident on the photodiode is converted into an electrical current, which is then amplified and further processed before the information carried by the optical signal can be extracted. The role of signal processing is to condition and reshape the electrical signal at the input of the decision device so that recovery of the information is facilitated and made with minimum ambiguity. Signal processing at the receiver must then take account of the transmitted signal format, shaping the wave form appropriately whilst at the same time minimising noise so as to enable clear decisions to be made [11]. The goal of signal shaping in digital optical receivers is thus the minimisation of the amount of optical power needed to achieve a given probability of error — the maximisation of the receiver sensitivity — in the presence of transmission impairments [12]. The move towards high speeds increases the importance of timing considerations. The signal must be filtered to achieve an eye pattern which is open vertically (low intersymbol interference) and horizontally (providing good jitter tolerance), whilst simultaneous maximisation of the receiver sensitivity requires its equivalent noise bandwidth be kept as small as possible within the above constraints. Since all high performance systems that are currently envisaged employ optical amplifiers, any signal design strategy proposed must account for the signal dependent nature of noise in optically amplified systems [10].

In parallel with the above developments in core network optical fibre transmission there is marked growth in mobile telecommunications [13] and in the use of subcarrier multiplexed optical fibre systems [14] to support mobility, as well as for other applications. This makes it appropriate to consider analogue optical receivers with rather different requirements, addressing specifically these applications. Analogue optical receivers should generate low noise across the band to maximise the signal to noise ratio of all the received channels and have good gain flatness across the band of each of the received channels to preserve the channel spectral content.

Various general receiver structures have been identified in the literature both for analogue and digital transmission with different performances and benefits. Among these the high impedance and the transimpedance [11] remain the more popular for wide band applications with the high impedance approach achieving the highest values of sensitivity and

the transimpedance approach obviating the need for bandwidth equalisation. For analogue applications, due to the usually narrow band requirements, the high impedance structure with some form of signal and noise tuning network is the favoured solution [15].

Receiver performance ultimately depends on the technology used and the best reported results for multi-Gbit/s optical receivers have been obtained using high electron mobility transistors and hybrid technology [16, 17]. However, there is a move towards integration to reduce production costs, improve repeatability and reliability, and ultimately achieve high performance. Accordingly, this study concentrates on integrated receivers intimately incorporating signal shaping/processing functions. The main focus is on GaAs MESFET technology exploring readily available foundry facilities, but preliminary consideration is given to the potential of InP-based technology for future requirements.

1.2 Thesis organisation

Following this introductory chapter, signal processing techniques for digital optical receivers will be considered in chapter 2. In the case of PIN receivers different signal shaping solutions are reviewed and their performance compared with that of a raised cosine receiver which is shown to provide nearly ideal noise filtering and time domain performance. The raised cosine solution is then investigated for receivers where the signal dependence of the noise cannot be ignored, i.e. APD or optically preamplified receivers. It is shown that optimised sensitivity can be only achieved at the expense of poor tolerance to timing imp irments such as sampling and signalling jitter; conversely, timing robustness can be only achieved at the expense of sensitivity. To overcome this limitation a new family of waveforms for digital optical communication systems is derived that allows both optimised sensitivity and jitter tolerant operation to be obtained in optical receivers dominated by signal dependent noise. System implications for optical preamplified receivers are examined. Finally, an assessment of the realisability of the equalisation functions necessary to implement the new signal designs is effected.

Practical demonstration of the signal shaping strategies discussed in chapter 2 require the choice of an appropriate technology. GaAs microwave monolithic integrated circuit technology is now mature, achieving operating frequencies compatible with todays multi-Gbit/s optical communication system requirements. Also, custom fabrication facilities are readily available from the GaAs process manufacturers. Chapter 3 describes briefly

the GaAs technology and the models used in the practical implementation of the circuits discussed in subsequent chapters in this thesis. Noise modelling of the GaAs foundry active devices is considered in detail and a noise de-embedding technique is developed and applied to the determination of the noise coefficients that characterise the noise model chosen to represent the noise behaviour of the foundry MESFETs. The noise modelling and the de-embedding technique are then validated.

Chapter 4 discusses the practical implementation of the signal processing strategies proposed in chapter 2 for the realisation of jitter tolerant optical receivers. The discussed designs are implemented as GaAs MMICs. Two signal shaping designs are considered. The first is an optical receiver that incorporates the signal shaping necessary to secure optimum noise filtering and jitter tolerant operation according to the modified Chernoff bound criterion, while the second explores the possibility of using passive GaAs MMIC networks to effect signal shaping at very high bit rates and two practical post-detection filters are demonstrated for operation at 10 and 15 Gbit/s. In connection with the post-detection filter designs a novel direct time domain optimisation technique is developed that allows accurate design of GaAs MMIC passive filters. In this chapter, the realisation of optical receivers tolerant to the input circuit parasitics is also considered and a transimpedance configuration with a common-gate front-end stage is proposed as a means to achieve the desired robustness. The common-gate concept applied to optical receivers is demonstrated in this chapter through the implementation of a 5 Gbit/s optical receiver.

In chapter 5 the use of distributed amplifiers in optical communication systems is considered. The basic principles of operation of the distributed amplifier are reviewed and its use as an optical receiver discussed. A design example suggesting that standard GaAs MESFET technology can be used to implement distributed optical receivers operating at bit rates well over 10 Gbit/s is given. A novel technique is presented for using the distributed amplifier as an active pulse shaping/filtering network by effectively constructing the amplifier as a transversal filter. To illustrate the use and potential of the distributed amplifier as a pulse shaping network two 10 Gbit/s optical receiver designs with embedded signal shaping are presented. The first is designed to have a 100% raised cosine roll-off while the second implements a particular case of the new signal designs and its time domain performance is compared with its equivalent passive realisation.

Chapter 6 discusses electronic noise minimisation for optical receivers. Some well known noise reduction design solutions are discussed in an unified manner by considering the gen-

eral case of an optical receiver that uses a generic noise matching network between the photodiode and the front-end amplifying stage. From this general treatment the criteria for optimum noise matching in optical receivers are established. The design and optimisation of a noise tuned optical receiver for subcarrier multiplexed systems integrated as a GaAs MMIC is considered. A critical study of tuning networks suitable for integration is undertaken and the details of the design and optimisation strategy are given.

Chapter 7 is a first exploration of the potential of a still experimental InP-based process for the construction of 10 Gbit/s OEIC optical receivers. The InP-based process is briefly described and two optical receiver designs are proposed that satisfy the basic design requirements established in this chapter and demonstrate the potential of the technology for the realisation of 10 Gbit/s optical receivers.

Finally, chapter 8 concludes the thesis, summarising the main findings and identifying areas where further research may be appropriate.

1.3 Summary of main contributions

The main contributions of this thesis may be summarised as follows:

- A new class of signal designs (NSD) is derived for optical communication systems that allow for the optimisation of the optical receiver sensitivity while maintaining jitter tolerant operation in systems dominated by signal dependent noise.

- An assessment of the realisability of the necessary equalisation functions to implement the NSD is made and it is shown that optimised all-pole networks can provide close to optimum performance. As a step in the simplification of the design and optimisation process it is shown that a bandwidth optimised Thomson filter can be used as a near optimum equaliser.

- A computationally simple noise de-embedding procedure is developed and applied to the noise modelling of the GaAs foundry MESFETs that are used in the active circuit implementations discussed in this thesis.

- Design and fabrication of a GaAs MMIC optical receiver with embedded signal shaping based on the modified Chernoff bound optimisation technique.

- Demonstration of the first common-gate transimpedance optical receiver. The receiver operates at 5 Gbit/s and is desensitised with respect to the input parasitic capacitances.

- Development and implementation of a novel direct time domain optimisation technique suitable for the design of very high speed GaAs MMIC signal shaping passive structures.

- Demonstration of GaAs MMIC post-detection signal shaping filters designed to satisfy the new signal design requirements and for operation at 10 and 15 Gbit/s. The optimisation of the impulse response of these filters is made using the optimisation technique mentioned above.

- The equivalence between the transversal filter and the distributed amplifier is demonstrated. It is thus proposed that a modified distributed amplifier — due to its very high frequency capabilities — can be used as a signal shaping/filtering network for multi-Gbit/s optical systems. In particular, two 10 Gbit/s design examples are given that demonstrate the possibility of implementing optical receivers with embedded pulse shaping using distributed amplifiers structures. Additionally alternative structures are proposed that can overcome some limitations of the originally proposed technique.

- The optimum noise matching criteria for optical receivers is established.

- Design, optimisation and fabrication of the first GaAs receiver with an integrated noise tuning network for subcarrier multiplexed applications.

- Demonstration of the capability of an experimental InP-based process for the realisation of 10 Gbit/s optical receivers.

The contributions made during the course of this research have led to the following publications:

1. I. Darwazeh, P. Lane, W. Marnane, P. Moreira, L. Watkins and M. Capstick. A high bit-rate GaAs MMIC optical receiver with optimum signal shaping. *Digest of 3rd. Bangor Communications Symposium*, pages 321–324, Bangor Wales, May 1991.

2. P. Moreira, P. Lane, I. Darwazeh and J. O'Reilly. Time domain optimisation of GaAs signal shaping filters for very high bit rate optical communications. *Digest of IEE-11th Saraga Colloquium on Digital and Analogue Filters and Filtering Systems*, pages 11/1–11/4, London UK, December 1991.

3. J. J. O'Reilly and P. M. R. S. Moreira. Signal design for multi-Gbit/s optical receivers. *Proc. Conference on Information Science and Systems, Vol. 1*, pages 101–105, Princeton USA, March 1992.

4. I. Darwazeh, P. Lane, W. Marnane, P. Moreira, L. Watkins, M. Capstick and J. O'Reilly. GaAs MMIC optical receiver with embedded signal processing. *IEE Proc.-G*, 139(2):241-243, April 1992.

5. P. Moreira, I. Darwazeh and J. O'Reilly. Design of an integrated tuned front-end GaAs receiver for SCM applications. *Digest of 4th. Bangor Communications Symposium*, pages 180–183, Bangor Wales, May 1992.

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8. I. Darwazeh, P. Moreira, P. Lane and J. O'Reilly. GaAs integrated common gate optical receiver. *Workshop on Integrated Circuits for Optical Communications, Conference of Optical Fibre Communications-OFC'93*, San Jose USA, February 1993.

9. J. O'Reilly, P. Lane, P. Moreira and I. Darwazeh. A GaAs based approach to signal shaping for optical communications. *Workshop on Integrated Circuits for Optical Communications, Conference of Optical Fibre Communications-OFC'93*, San Jose USA, February 1993.

10. P. Moreira, I. Darwazeh and J. O'Reilly. Distributed amplifier signal shaping strategy for multigigabit digital optical transmission. *Electron. Lett.*, 29(8):655–657, April 1993.

11. P. Moreira, I. Darwazeh and J. O'Reilly. Noise optimisation of tuned integrated GaAs receiver. *Proc. International Symposium on Fibre Optic Networks and Video Communications SPIE Vol. 1974: Transport Technologies for Broadband Optical Access Networks*, pages 20–25, Berlin Germany, April 1993. in Press.

12. P. Lane, I. Darwazeh, P. Moreira and J. O'Reilly. GaAs MMIC technology applied to signal shaping for high bit-rate optical communications. *Proc. International Symposium on Fibre Optic Networks and Video Communications SPIE Vol. 1974: Transport Technologies for Broadband Optical Access Networks*, pages 57–67, Berlin Germany, April 1993, In Press.

13. I. Darwazeh, P. Moreira, P. Lane and J. O'Reilly. 5 Gbit/s GaAs optical receiver MMIC. *Digest of 5th. Bangor Communications Symposium*, pages 163–166, Bangor Wales, June 1993.

14. P. M. R. S. Moreira, P. M. Lane, I. Darwazeh and J. O'Reilly. Time domain optimisation of high bit rate optical receivers. *Proc. Sixth Annual IEEE International ASIC Conference*, pages 494–497, Rochester USA, September 1993.

15. P. Moreira, I. Darwazeh and J. O'Reilly. Novel optical receiver design using distributed amplifier pulse shaping network. *Digest of IEE-Colloquium on Optical Detectors and Receivers*, pages 8/1–8/4, London UK, October 1993.

16. P. Moreira, I. Darwazeh and J. O'Reilly. Design and optimisation of a fully integrated GaAs tuned receiver preamplifier MMIC for optical SCM applications. *IEE Proc.-J Special Issue on Analogue Optical Fibre Communications*, 1993, In Press.

In the next chapter signal processing techniques for digital optical receivers will be considered.

Chapter 2

Signal shaping and noise filtering for optical communications

In this chapter, the relations between noise filtering, control of intersymbol interference and sensitivity relating to optical receivers will be further explored in the context of optimising the receiver performance by tailoring its impulse response. Signal designs for receivers dominated by Gaussian noise (PIN-receivers) will be reviewed. For systems where signal-dependent noise is dominant, depressed threshold signals will be examined and a new class of signals with optimum time domain characteristics will be derived. These signals offer advantages over more conventional ones, when system impairments such as signaling or timing jitter are important considerations [18]. Equalisers that use these targets will be compared with those obtained by a rigorous optimisation method based on the modified Chernoff bound. Finally, the possibility of using realisable networks to implement the required signal shaping will be investigated.

2.1 Signal shaping for PIN-receivers

The system model of an optical receiver is represented in figure 2.1. In this figure all the functions of the linear receiver are combined in the single transfer function $H_T(f)$ and $S_{eq}(f)$ is the spectral density of the effective input noise current. The general optimisation problem for binary optical receivers is to find the optimum transfer function $H_T(f)$ that will minimise the bit error rate (BER) in the presence of noise. In PIN-receivers the signal-dependent noise contribution can be neglected and the total receiver noise can be considered Gaussian and entirely due to circuit noise [11]. The role of the decision circuit

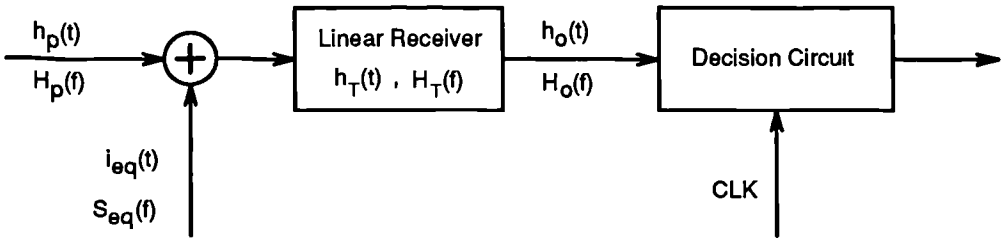

Figure 2.1: Optical receiver system model

is to detect the presence or absence of the pulse $h_p(t)$ at the sampling instant t_s. In this case, the optimum solution is the whitened matched filter whose transfer function can be written as (see for instance [19] or [20]):

$$H_T(f) = \frac{H_p^*(f)}{S_{eq}(f)} e^{-j2\pi f t_s} \tag{2.1}$$

were $H_p^*(f)$ is the complex conjugate of the input signal spectrum. A receiver with such transfer function will act by enhancing the signal plus noise spectrum at frequencies were the signal spectrum is high and the noise spectrum is low and, reciprocally, reducing it at frequencies where the noise spectrum is high and the signal spectrum is low. However, an optical receiver should be capable of detection of a stream of pulses and not only a single isolated pulse. The matched filter solution can, in the presence of coloured noise, exhibit strong intersymbol interference (ISI) and, consequently, fail to optimise the BER at the decision circuit. To obviate this problem other solutions are necessary. O'Mahony [21] proposes a solution to this problem by minimising simultaneously the noise power and intersymbol interference at the equaliser output. Variational calculus techniques were used to maximise the ratio:

$$\frac{h_o^2(t_s)}{\sigma_o^2 + \sigma_{isi}^2} \tag{2.2}$$

were $h_o(t_s)$ is the value of the output variable at the sampling instant t_s. σ_o^2 and σ_{isi}^2 are the average noise power and the ISI variance respectively, at the output of the equaliser and are defined by:

$$\sigma_o^2 = \int_{-\infty}^{\infty} S_{eq}(f) |\, H_T(f) \,|^2 df \tag{2.3}$$

$$\sigma_{isi}^2 = \frac{1}{4} \sum_{\substack{k=-\infty \\ k \neq 0}}^{\infty} h_o^2(t_s - kT) \tag{2.4}$$

The maximisation of equation (2.2) is effected under the constraint that the signal spectrum at the output $H_o(f)$ must occupy a maximum bandwidth of $\pm 1/T$ where T is the bit

period. This is justified by the fact that the spectral density of the effective input noise current $S_{eq}(f)$ is approximately proportional to the square of frequency and, consequently, it might be advantageous to reduce the contribution to σ_o^2 from the higher frequency part of the spectral density $S_{eq}(f)$. However, by doing this, there is the possibility of increasing the ISI and so there has to be a compromise between reducing the noise contribution and minimising ISI under the indicated bandwidth constraint.

It is worthwhile noticing that the solution obtained by O'Mahony can be written as the product of two functions, one of them having the form of a whitened matched filter. Theoretically an optical sensitivity improvement of 0.8 dB was expected, when comparing with the raised cosine target (RC), and experimentally a 0.5 dB improvement was obtained for a PIN-FET receiver operating at 160 Mbit/s [21].

Hooper [22] also addresses the problem of simultaneous minimisation of noise and ISI. In his approach the SNR defined by:

$$\left.\frac{S}{N}\right|_{t=ts} = \frac{h_o^2(t_s)}{\sigma_o^2} \tag{2.5}$$

is maximised under the constraints of zero ISI and zero telegraph distortion (TD). The solution obtained has the form:

$$H_T(f) = H_M(f) \cdot H_\lambda(f) \tag{2.6}$$

were $H_M(f)$ is the whitened matched filter defined by equation (2.1) and $H_\lambda(f)$ is the transfer function of a transversal filter (zero forcing equalizer (ZFE)) that is given by:

$$H_\lambda(f) = \sum_{n=-\infty}^{\infty} \lambda_n e^{j2\pi nT} \tag{2.7}$$

whose coefficients λ_n are given by the solution of the linear equation:

$$\left[h_{m,n/2}\right]\left[\lambda_n\right] = \left[h_{0,n/2}\right] \tag{2.8}$$

were $h_{m,n/2}$ is the output of the matched filter at intervals of time $T/2$ and $h_{0,n/2}$ is the output of the ZFE at intervals of $T/2$. In this case the output spectrum is not band limited. The performance of such optimum equalisers was evaluated in the case of a noise spectrum proportional to the square of frequency ($S_{eq}(f) \propto 1+(af)^2$) and compared with the raised cosine equaliser performance. A SNR improvement between $0.1-0.4$ dB was obtained and only half this improvement is expected for the optical sensitivity.

Integrate and dump receivers [23, 24] have also been used as a means to realise matched receivers avoiding the problems of intersymbol interference. However, also in this case only a moderate increase in sensitivity ($< 1\,\mathrm{dB}$) is obtained when comparing with a simple lowpass filter [24] or with the unclocked mode of operation [23].

The above considerations seem to suggest that the raised cosine target is close to the optimum solution for signal shaping in systems dominated by Gaussian noise, although its derivation is based only on time domain considerations without considering the input signal or noise characteristics.

2.1.1 Timing performance

Scanlan [25] derives the condition that has to be met by a class of signals band limited to less than $\pm 1/T$, if the first Nyquist criterion (zero ISI) [26] is to be satisfied and shows that among this class there are signals with improved sensitivity to small timing errors. However, the second Nyquist criterion (zero TD) [26] is neither included in Scanlan's formulation nor is it demonstrated that it is possible to obtain such band limited signals that both obey the second criterion and still offer improved sensitivity to small timing errors. The second Nyquist criterion is an important consideration when moderate to large timing errors are involved in the detection process. To obtain tolerance to timing errors it is important for the eye-diagram to be maximally opened horizontally around the decision threshold level, which for PIN-receivers should be situated at 50% of the vertical eye opening [11]. This condition is satisfied by the RC target. Also, the tails of the RC pulse decay at a rate of $1/t^3$ which guarantees moderate tolerance to timing jitter.

In the next section it will be shown that although the raised cosine target presents both good frequency and time domain characteristics and offers near optimum performance for systems dominated by additive Gaussian noise, in systems dominated by signal dependent noise it is possible to obtain pulse targets that perform better than the raised cosine, especially in the presence of timing errors.

2.2 Signal shaping for receivers dominated by signal dependent noise

Semiconductor laser amplifier (SLA) or fibre amplifier (FA) can be used in long haul transmission systems to increase the span length without the use of electronic regeneration

or to increase the optical receiver sensitivity (preamplified receivers) [27, 28]. In such systems the noise at the output of the FA or SLA is dominated by the signal-spontaneous and spontaneous-spontaneous beat noise components [29, 30, 31]. However, optimised operation of an optically amplified system requires an optical filter to be placed after the optical amplifier (OA) either to contain the build-up of the spontaneous-spontaneous contribution to noise in an amplifier chain or to optimise the preamplifier performance. In such conditions the noise environment at the receiver is dominated by signal-spontaneous beat noise contributions exhibiting strong signal dependence [29, 30, 31]. Accordingly, the receiver decision threshold should be set at a low level in the vertical eye opening. Specifically, the Gaussian approximation [11, 32] predicts that to optimise the receiver sensitivity a decision threshold given by

$$d_{opt} = \frac{\sigma_0}{\sigma_1 + \sigma_0} \tag{2.9}$$

should be used. Here d_{opt} is the optimum value of the normalised threshold and σ_0 and σ_1 are the root mean square value of the total noise power associated with a binary '0' and a binary '1', respectively. In these circumstances it is appropriate to evaluate the performance of the raised-cosine pulse target in the presence of jitter since the optimum decision threshold level no longer coincides with maximum horizontal opening of the eye-diagram.

An upper bound on the system power penalty in the presence of timing jitter can be obtained by considering a systematic timing offset in the sampling instant which, for symmetrical pulses, correspond to the adoption of the so called worst case jitter probability density function (PDF) described in [33]. In such an assessment the effects of intersymbol interference can be easily allowed for if the eye-closure description is adopted [34, 35]. The error probability of incorrectly identifying a received '0' or '1' is given by

$$P_{err} = 0.5\left\{Q\left(\frac{P(\tau)(s_u(\tau) - d_{opt})}{\sigma_1(\tau)}\right) + Q\left(\frac{P(\tau)(d_{opt} - s_l(\tau))}{\sigma_0}\right)\right\} \tag{2.10}$$

where

$$Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^\infty e^{-u^2/2}\, du \tag{2.11}$$

$P(\tau)$ is the optical power penalty expressed as a function of the normalised time offset τ ($\tau = t/T$). $P(\tau)$ is defined as the increase in signal power required to maintain a given P_{err} with $P(0) = 1$ when the decision threshold is set at the optimum value. In equation

(2.10) σ_1 was written as $\sigma_1(\tau)$ to stress the fact that in systems involving OAs the noise power associated with a signal '1' is dependent on $P(\tau)$ as is true for avalanche photodiode (APD) receivers [36]. Optical amplifiers noise can be expressed as a signal-independent noise term σ_i^2 ($\sigma_i^2 = \sigma_0^2$) and a signal-dependent noise term σ_d^2 which is proportional to the input optical power [29, 31]. Consequently $\sigma_1(\tau)$ can be expressed as

$$\sigma_1(\tau) = \sqrt{\sigma^2 P(\tau) + \sigma_0^2} \tag{2.12}$$

where σ^2 is the constant of proportionality (the possible signal dependence of σ_0 will be considered later in this chapter). For a given error probability and optimum decision threshold, σ_0 and σ should be selected according to

$$\sigma_0 = \frac{d_{opt}}{\mathrm{SNR}} \tag{2.13}$$

$$\sigma^2 = \left(\frac{1 - d_{opt}}{\mathrm{SNR}}\right)^2 - \sigma_0^2 \tag{2.14}$$

(with SNR = 6 for an error probability equal to 10^{-9}). Finally $s_l(\tau)$ and $s_u(\tau)$ are the lower and upper envelope of the inner-eye, respectively. They can be numerically estimated for a pseudo random bit sequence (PRBS) from:

$$s_l(\tau) = \max\{s(kT + \tau)\}, \qquad \forall k : m_k = 0 \tag{2.15}$$

$$s_u(\tau) = \min\{s(kT + \tau)\}, \qquad \forall k : m_k = 1 \tag{2.16}$$

with $\tau \in (-0.5, 0.5)$ and

$$s(t) = \sum_{k=-\infty}^{\infty} m_k \, h_o(t), \qquad m_k \in \{0, 1\} \tag{2.17}$$

The power penalty (in decibel) as a function of the timing offset τ is then given by:

$$P_{dB}(\tau) = 10 \log[P(\tau)] \tag{2.18}$$

This power penalty for optical receivers using the raised cosine design is represented in figure 2.2 for different values of the optimum decision threshold d_{opt}. From this figure it can be obs rved that $P_{dB}(\tau)$ depends strongly on the value of the optimum decision threshold and specifically for systems where low threshold values should be used ($d_{opt} < 0.3$) the raised cosine signal design becomes unduly intolerant to timing offsets and jitter. To achieve reasonable robustness the decision threshold is usually set closer to the centre of

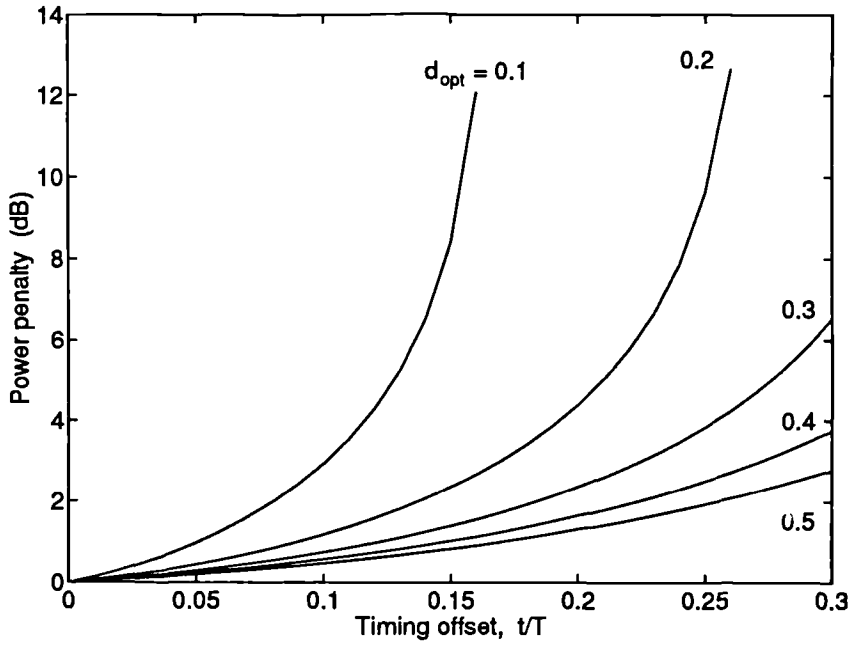

Figure 2.2: RC power penalty versus timing offset for different values of d_{opt}

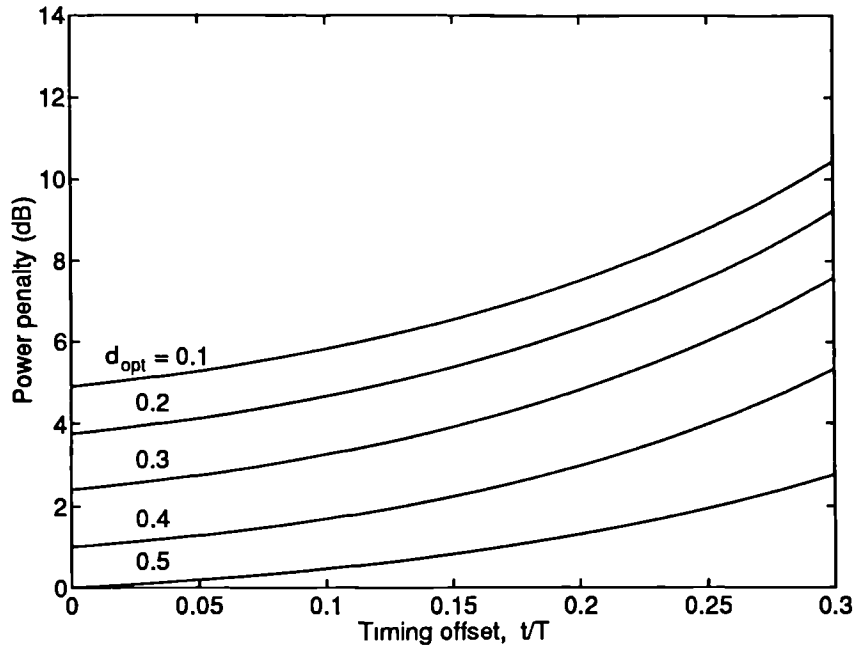

Figure 2.3: RC power penalty versus timing offset for different values of d_{opt} when the decision level is set at 50%

the vertical eye opening. Figure 2.3 represents the power penalty of equation (2.18) when the non-optimum decision threshold $d = 0.5$ is used instead of the optimum value. The receiver can now be seen to be more tolerant to timing errors but a sensitivity penalty approaching 6 dB is incurred in the absence of timing errors. Accordingly it is appropriate to devise a signal shaping arrangement such as to allow the decision threshold to be set lower in the vertical eye opening, commensurate with the signal-spontaneous beat noise dominance, without incurring undue jitter penalty.

2.2.1 Depressed threshold designs

The problem of deriving signal targets for optical receivers that allow for the decision threshold level to be placed at its optimum value wile maintaining a jitter tolerant operation was addressed by O'Reilly and Fyath [37] for the case of APD receivers. To achieve this, two time domain constraints were imposed on the pulse shape at the input of the decision circuit:

$$h_o(t) = \begin{cases} 1, & t = 0 \\ 0, & t = nT \quad \text{and} \quad n \neq 0 \end{cases} \tag{2.19}$$

$$h_o(t) = \begin{cases} 0, & t = (n + 1/2)T \quad \text{and} \quad n \neq 0, -1 \\ d, & t = \pm T/2 \end{cases} \tag{2.20}$$

Constraint (2.19) corresponds to the first Nyquist criterion while constraint (2.20) enforces the second Nyquist criterion with respect to the optimum decision threshold level. The second constraint ensures that the eye-diagram is maximally opened horizontally at the threshold level so that jitter tolerant operation is attained. The above conditions can be easily converted to their frequency domain equivalents and the minimum bandwidth solution is found to be:

$$H_o(f) = \begin{cases} \frac{T}{2}\left[1 + 2\,d\,\cos(\pi f T)\right], & |f| < 1/T \\ 0, & \text{elsewhere} \end{cases} \tag{2.21}$$

The signal spectrum of equation (2.21) poses problems of physical realisation since for values of $d < 0.5$ the spectrum is discontinuous at $f = 1/T$. This difficulty can be overcome by recognising that $H_o(f)$ can be written as a sum of two components, one having the form of a full raised cosine spectrum and the other of a rectangular spectrum. The rectangular part of the spectrum can now be modified according to Nyquist's first criterion by adding a transmission function which has skew symmetry about the cut-off frequency $1/T$ without

perturbing the original constraints (2.19) and (2.20). The amplitude spectrum of equation (2.21) can then be made to have a gradual roll-off and in [37] the amplitude spectrum

$$H_o(f) = H_1(f) + H_2(f) \tag{2.22}$$

where

$$H_1(f) = \begin{cases} 2\,d\,[1+\cos(\pi\,f\,T)], & |f| < 1/T \\ 0, & \text{elsewhere} \end{cases} \tag{2.23}$$

$$H_2(f) = \begin{cases} 1-2\,d, & 0 < |f| < (1-\alpha)\,B \\ \frac{1-2\,d}{2}\left\{1-\sin\left[\frac{\pi\,(|f|-B)}{2\,\alpha\,B}\right]\right\}, & (1-\alpha)\,B < |f| < (1+\alpha)\,B \\ 0, & |f| > (1+\alpha)\,B \end{cases} \tag{2.24}$$

that is band limited to $(1+\alpha)\,B$ was proposed. The corresponding time domain representation is given by

$$h_o(t) = \text{sinc}(2\,t/T)\left[\frac{2\,d}{1-4\,(t/T)^2} + \frac{(1-2\,d)\,\cos(2\,\pi\,\alpha\,t/T)}{1-(4\,\alpha\,t/T)^2}\right] \tag{2.25}$$

were $B = 1/T$ is the bit rate and α the spectrum roll-off factor ($0 \leq \alpha \leq 1$). O'Reilly and Fyath have shown that when such a signal shaping strategy is used in conjunction with APD retiming receivers, these can benefit from improved tolerance to alignment jitter without incurring a noise penalty. In fact, a small improvement in sensitivity was obtained ($\approx 0.15\,\text{dB}$) in the absence of timing errors, for a design with $d = 0.3$ and $\alpha = 0.25$, while a sensitivity penalty of less than 2 dB w s predicted for timing errors up to 25% of the bit period.

Examples of signal spectrum and signal shape are given in figures 2.4 and 2.5 respectively. Figure 2.4 represents both the unmodified amplitude spectrum (equation (2.21)) and the modified amplitude spectrum (equation (2.21)) for $d = 0.3$. In the case illustrated, careful selection of the roll-off factor ($\alpha = 0.25$) produced a frequency spectrum well suited for approximation by a realisable network. In reference [37] pulse shaping networks implemented as 4-th order low pass networks were successfully used to provide equalisation for return to zero (RZ) signalling pulses. Time domain pulse shapes for $d = 0.3$ and $d = 0.2$ are shown in figure 2.5 with corresponding values of $\alpha = 0.25$ and $\alpha = 0.3$ selected to obtain good frequency domain targets.

The following remarks can now be made on the described approach:

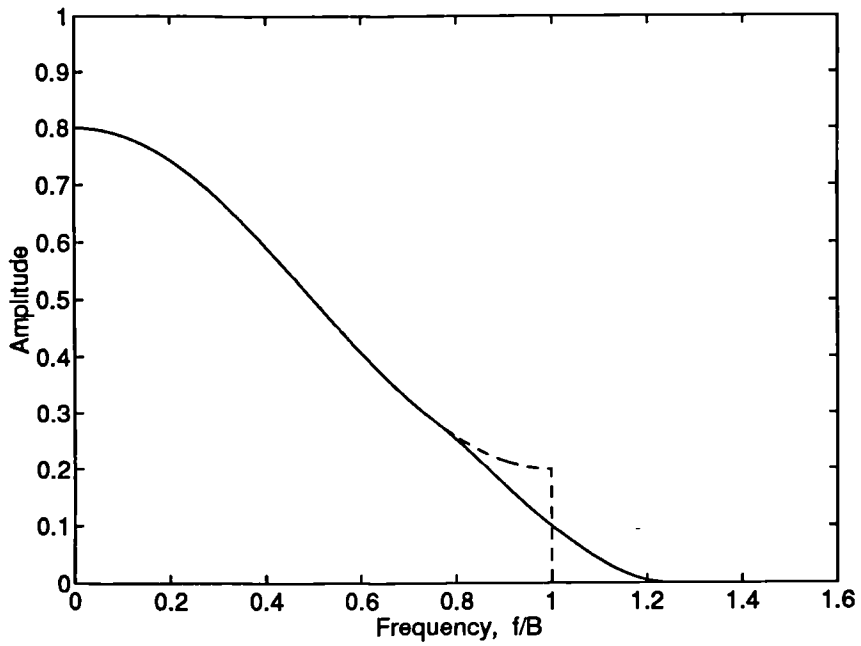

Figure 2.4: Pulse spectrum for $d = 0.3$: '– – –' $\alpha = 0$, '——' $\alpha = 0.25$

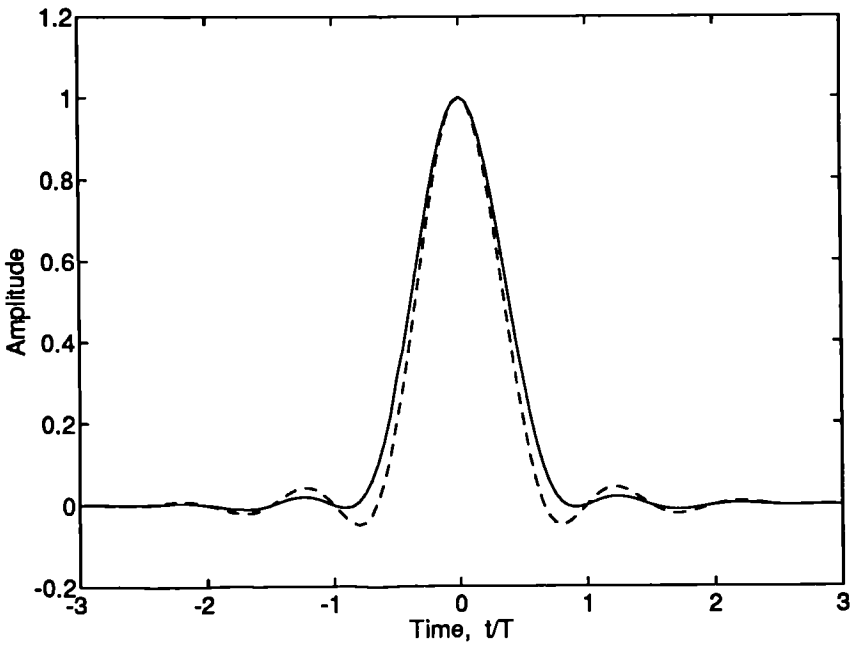

Figure 2.5: Pulse shapes: '——' $d = 0.3$ and $\alpha = 0.25$, '– – –' $d = 0.2$ and $\alpha = 0.3$

- An arbitrary modification of the signal spectrum (equation (2.21)) has to be made, for values of d less than 0.5, so that no discontinuity is present at $f = 1/T$.
- The modified spectrum roll-off factor α has to be chosen so that the frequency domain response can be approximated by a realisable network of moderate complexity.
- The roll-off factor has influence on the amount of pulse tail ripple that is obtained in the time domain. However as shown in figure 2.5 even for values of α that provide a smooth frequency roll-off, pulse tail ripple can be significant, particularly so for low values of the decision threshold.

Of these considerations the last point is of most significance since although condition (2.20) ensures that the eye diagram is maximally opened horizontally around the decision threshold level, on its own (2.20) is not sufficient to ensure low ripple in the pulse tails and consequently the discussed signal design does not guarantee optimum tolerance to small timing errors and jitter. It is thus necessary to impose an extra time domain constraint so that receiver operation tolerant to both small and large timing errors is achieved even for low values of d.

2.3 Depressed threshold designs with improved jitter tolerance

Timing errors cause the receiver performance to degrade both because the signal is sampled at a point were its amplitude is not maximum and because ISI due to other received pulses contributes to eye closure. For small timing errors the worst case ISI can be expressed as

$$WC_{isi} = \Delta t \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \left| \frac{d\, h_o(t)}{dt} \, |_{t=nT} \right| \tag{2.26}$$

where Δt is the timing error relative to the optimum sampling point. This equation shows that tolerance to small timing errors can be increased if the time derivative of $h_o(t)$ is minimised at the sampling instants $t = nT$. Consequently, a third time domain constraint can be imposed so that the time derivative of $h_o(t)$ is forced to be zero at the sampling instants nT. With this additional condition, a new class of waveforms for binary optical transmission with improved tolerance to timing and signaling jitter can be derived. The

time domain constraints for $h_o(t)$, normalised to $T = 1$, can now be written as:

$$h_o(t) = \begin{cases} 1, & t = 0 \\ 0, & t = n \quad \text{and} \quad n \neq 0 \end{cases} \tag{2.27}$$

$$h_o(t) = \begin{cases} 0, & t = (n + 1/2) \quad \text{and} \quad n \neq 0, -1 \\ d, & t = \pm 1/2 \end{cases} \tag{2.28}$$

$$\frac{d\, h_o(t)}{dt} = 0, \qquad t = n \tag{2.29}$$

(2.27) ensures zero intersymbol interference and (2.28) that decision threshold crossings, with $d < 0.5$, occur midway between signal epochs. The eye is thus appropriately disposed vertically about the decision threshold d. Conditions (2.27) and (2.28) together provide tolerance to large deviation timing errors while the additional condition (2.29) ensures tolerance for small perturbations in the signaling and sampling processes. The combined imposition of these constraints will produce signal designs especially well suited to soliton and optical-time division multiplexed (OTDM) systems. In the frequency domain, with $h_o(t) \Leftrightarrow H_o(f)$ a Fourier pair, these constraints correspond to:

$$\sum_{n=-\infty}^{\infty} H_o(f - n) = 1 \tag{2.30}$$

$$\sum_{n=-\infty}^{\infty} e^{\jmath \pi n} H_o(f) = 2\, d \cos(\pi f) \tag{2.31}$$

$$\sum_{n=-\infty}^{\infty} (f - n)\, H_o(f - n) = 0 \tag{2.32}$$

for which a minimum finite support solution exists on $|f| \leq 3/2$, this solution is given below with full derivation in appendix A:

$$H_o(f) = \begin{cases} \frac{1}{2} + d\, \cos(\pi f), & 0 \leq |f| \leq \frac{1}{2} \\ \frac{1}{2} \left[\frac{3}{2} + d\, \cos(\pi f) - |f| \right], & \frac{1}{2} < |f| \leq \frac{3}{2} \\ 0, & \text{elsewhere} \end{cases} \tag{2.33}$$

hence

$$h_o(t) = \text{sinc}(t)\, \text{sinc}(2t) + \frac{d}{2} \left[\text{sinc}\left(t + \frac{1}{2}\right) + \text{sinc}\left(t - \frac{1}{2}\right) \right] [1 - \cos(2\pi t)] \tag{2.34}$$

Illustrative frequency and time response functions are shown in figures 2.6 and 2.7 respectively. From equation (2.33) it can be seen that the obtained frequency response

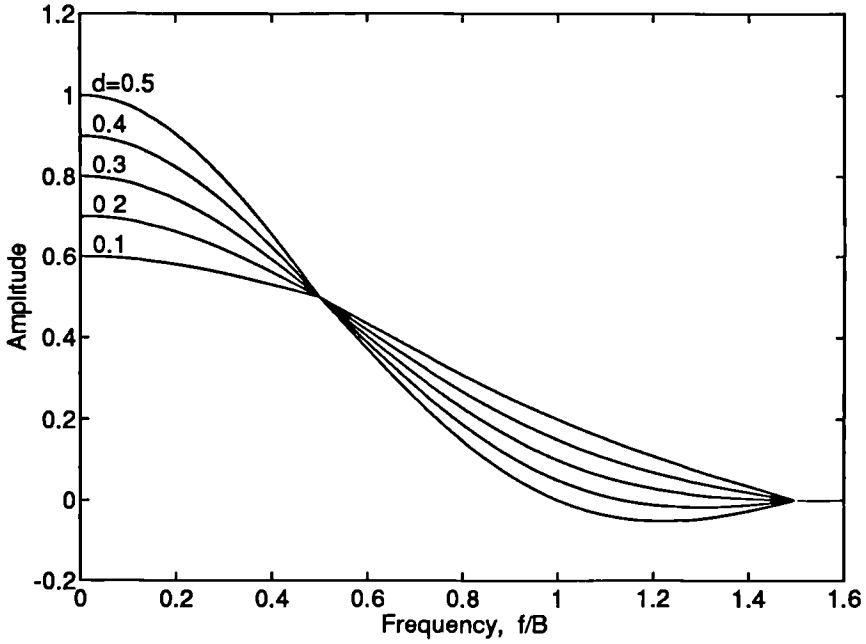

Figure 2.6: Pulse spectrum for different values of d

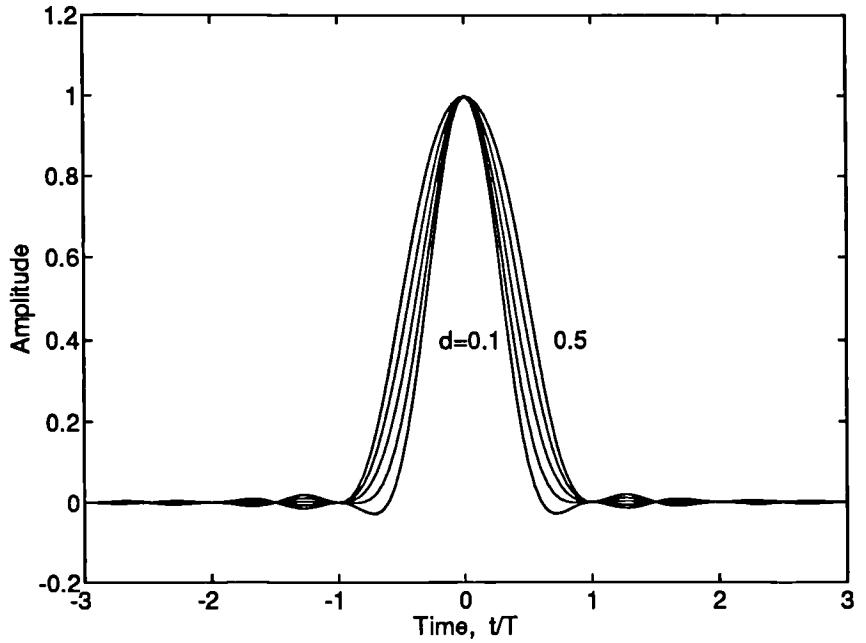

Figure 2.7: Pulse shape for different values of d

is continuous and is non-negative for $d \leq 1/\pi$. Although, the derivative of $H_o(f)$ is discontinuous at $f/B = 0.5$, it was found that $H_o(f)$ provides a suitable target for practical realisation even for the lowest values of d.

2.3.1 Timing and signaling jitter

The power penalty of equation (2.18) is represented in figure 2.8 for the new signal designs (NSD). Comparison with figures 2.2 and 2.3 reveals that such signal designs offer the possibility of optimising the receiver sensitivity by placing the decision level at its optimum value while maintaining jitter tolerant operation similar to that obtained in a raised cosine receiver with the decision level set at the non-optimum value of 0.5. Moreover, as a result of constraint (2.29) the power penalty is negligible for timing offsets up to 5% of the bit period for all values of d. For large timing errors the power penalty is significantly improved, particularly in the cases were $d < 0.3$ were the improvement can be of the order of several dBs.

The power penalty for signaling jitter was also considered and a worst case evaluation of the effects of signal jitter was adopted. Specifically, the PDF for the symbol arrival

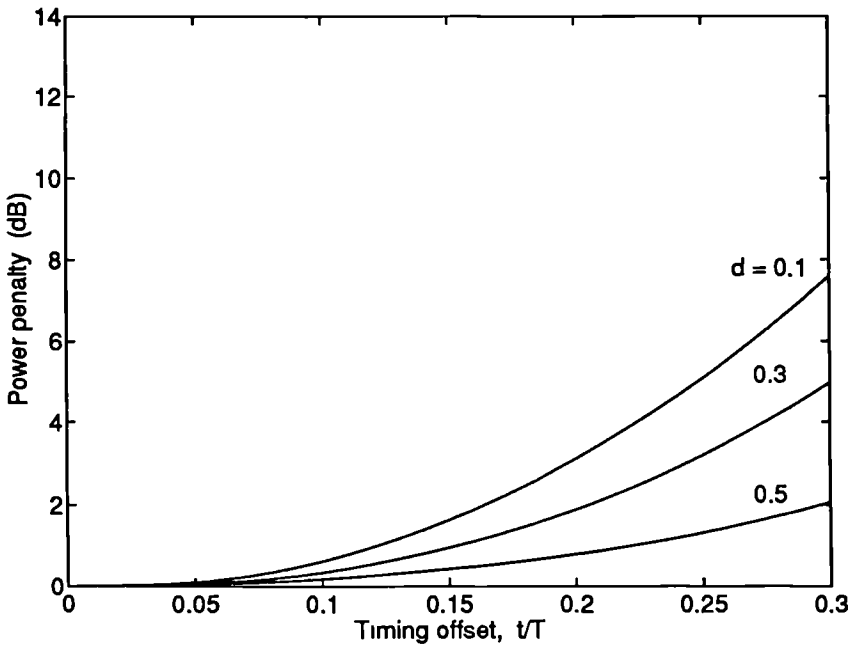

Figure 2.8: NSD power penalty versus timing offset for different values of d

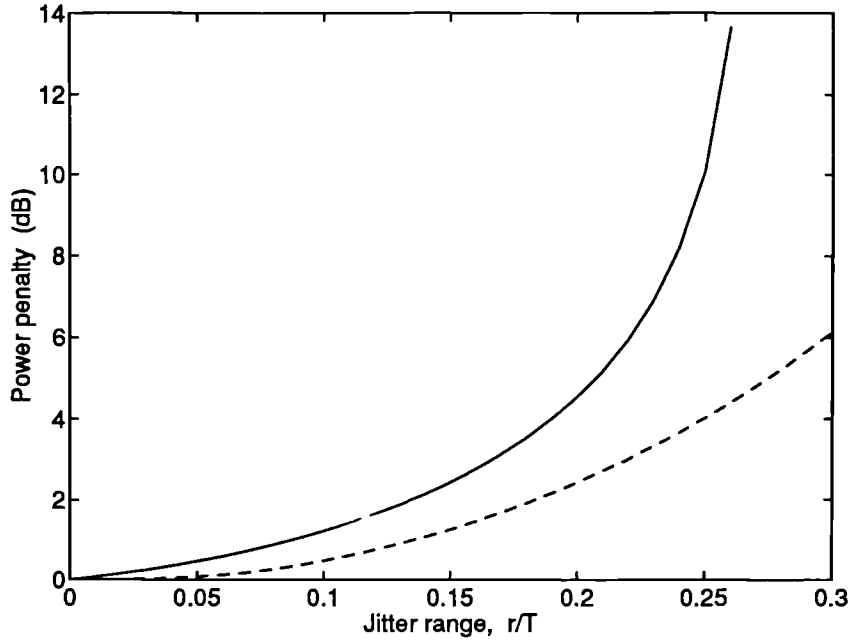

Figure 2.9: Power penalty versus r for $d_{opt} = 0.2$: '——' RC; '– –' NSD

times was considered to be

$$\frac{1}{2}[\delta(t/T + r) + \delta(t/T - r)] \tag{2.35}$$

were $\delta(\cdot)$ is the Dirac impulse and $2 \times r$ is the jitter range normalised to the bit period. In this case the behaviour of the power penalty as a function of the jitter range is very similar to that obtained previously for the power penalty as a function of timing offset for both the raised cosine and the new signal design . Figure 2.9 illustrates the case $d = 0.2$ showing improvements of 1.5 dB and 6.5 dB for $r = 15\%$ and 25% of the bit period, respectively.

This tolerance to timing and signal jitter makes the new designs particularly attractive for use in single or multi-channel soliton systems were Gordon-Haus jitter and soliton collisions are the main impairments imposing limitations on the achievable bit rate-distance product [38, 39].

2.3.2 Receiver noise and sensitivity

It is necessary to establish the noise and sensitivity implications for an optical receiver that will incorporate pulse equalisation to such signal designs. This can be done for the receiver front-end as well as for an optically preamplified receiver by evaluation of the Personick noise integrals [11, 32] for the selected equalising transfer function.

Two shapes of detected optical pulses will be considered below:

- A rectangular pulse that occupies a fraction T_s of the bit period T and has amplitude $1/T_s$.
- A soliton pulse that, after detection, has full width at half maximum (FWHM) which is a fraction T_s of the bit period and has pulse shape given by

$$h_p(t) = \frac{1}{2\tau_s \cosh^2(t/\tau_s)} \tag{2.36}$$

where the soliton width parameter τ_s is related to the FWHM by $T_s = 1.763\tau_s$ [38].

Both input pulse shapes are normalised such that

$$\int_{-\infty}^{\infty} h_p(t) = T \tag{2.37}$$

With this normalisation the pulse amplitude corresponds to the received optical power. The results of the evaluation of the noise integrals are represented in figures 2.10 and 2.11 for the rectangular and soliton pulses, respectively. In these figures values of the noise integrals are plotted as functions of the pulse width T_s with the decision threshold d as a parameter. For comparison purposes values of the noise integrals for the raised cosine case are also shown in the figures. It should be noticed that the dependence on T_s is stronger for the new signal designs than for the raised cosine, for all values of d. The reason for this is that for the NSD the frequency spectrum extends to $1.5\,B$ as opposed to B in the RC case. This also has the consequence that 't is not possible to use the NSD for signaling with rectangular pulses having normalised pulse widths greater than 0.67 since their spectrum has a null at $f = 1/T_s$. However, the zero in $H_o(f)$ for $d = 0.5$ is compatible with the special case of non return to zero signaling (NRZ). Also, $H_o(f)$ becomes negative in certain regions of the spectrum for values of d greater than $1/\pi$ which complicates equalisation if simple passive networks are to be used. However, in systems dominated by signal dependent noise the optimum decision threshold is expected to lie in the region where $d \leq 1/\pi$ which is also the range where the power penalty advantage of the NSD is most significant, as figures 2.2 and 2.8 show.

The electronic receiver noise can be expressed as [11]

$$\sigma_c^2 = \left[S_{shn} + \frac{S_{ser}}{R_{in}^2}\right] I_2\, B + (2\pi\, C_T)^2\, S_{ser}\, I_3\, B^3 \tag{2.38}$$

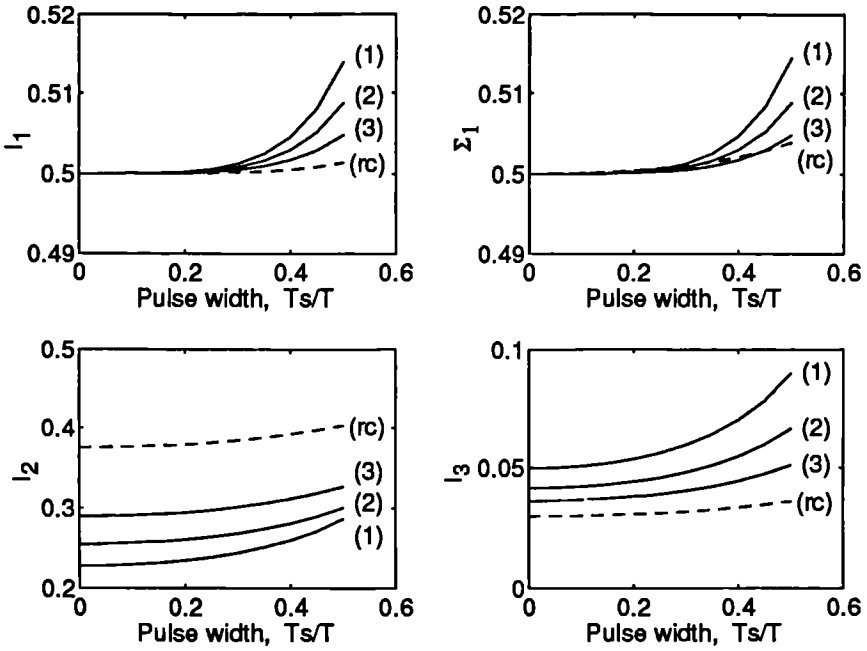

Figure 2.10: Personick noise integrals versus pulse width for rectangular input pulse: (1) $d = 0.1$; (2) $d = 0.2$; (3) $d = 0.3$

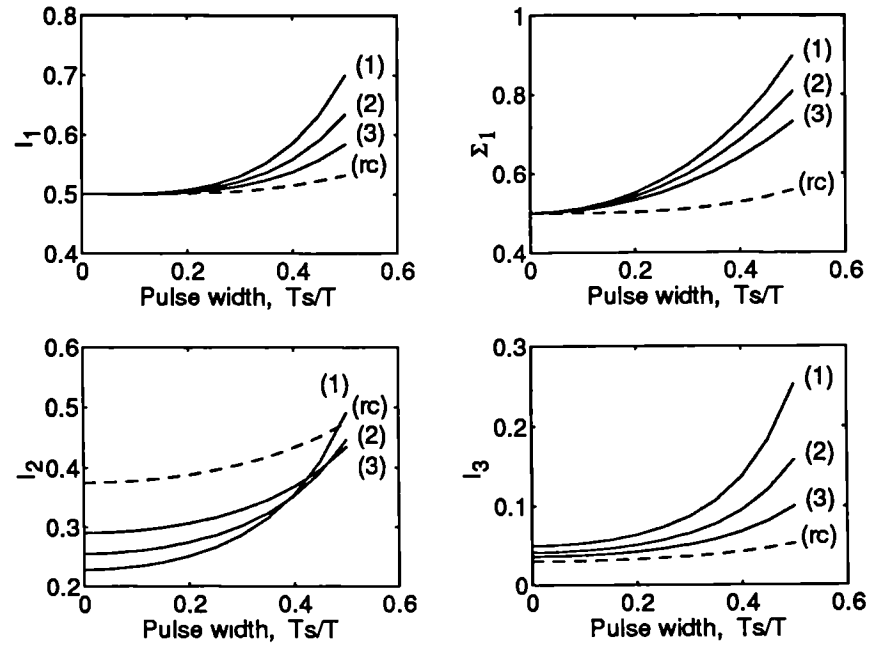

Figure 2.11: Personick noise integrals versus pulse width for soliton input pulse: (1) $d = 0.1$; (2) $d = 0.2$; (3) $d = 0.3$

where R_{in} is the resistive part of the input impedance, C_T is the total input capacitance and I_2 and I_3 are the Personick noise integrals defined by

$$I_2 = \int_0^\infty | H_T(f) |^2 \, df \tag{2.39}$$

$$I_3 = \int_0^\infty | H_T(f) |^2 \, f^2 df \tag{2.40}$$

where

$$H_T = \frac{H_o(f)}{H_p(f)} \tag{2.41}$$

when the bit period T is normalised to unity. The power spectral densities of the shunt S_{shn} and series S_{ser} equivalent noise generators for a FET receiver are given by

$$S_{shn} = \frac{4\,k\,\theta}{R_{in}} + 2\,q\,I_g \tag{2.42}$$

$$S_{ser} = \frac{4\,k\,\theta}{g_m}\Gamma \tag{2.43}$$

where k is Boltzmann's constant, θ is the temperature, q is the electronic charge, I_g is the FET gate leakage current, g_m is the device transconductance and Γ is Ogawa's excess channel-noise factor [40].

For a PIN-receiver the sensitivity is

$$\overline{P} = \frac{1}{\mathcal{R}_s} \mathrm{SNR}\,\sigma_c \tag{2.44}$$

were $\mathcal{R}_s$ is the photo-diode responsivity and SNR = 6 for a BER of 10^{-9}. The results of such a computation are represented in figure 2.12 using published data for a 10 Gbit/s optical receiver [17, 41]. Two cases are considered: a low input impedance receiver (R_{in} = 50 Ω) and a high input impedance receiver (R_{in} = 470 Ω). The low impedance receiver noise is dominated by thermal noise generated in R_{in}, consequently the NSD offers a sensitivity advantage when compared with the RC due to its lower value of I_2. In the high impedance case the noise is dominated by the FET channel noise and the RC design presents a sensitivity advantage due to its lower value of I_3. The noise integrals and the related sensitivity have a stronger dependence on the pulse width for the NSD than for the RC, particularly so for soliton pulses. This is however of no practical consequence for soliton systems were pulse widths must be kept smaller than at least 20% of the bit period to reduce interaction between adjacent pulses [42]. Also, for the high bit rates under consideration, a small inductor is frequently used at the receiver input to reduce the noise

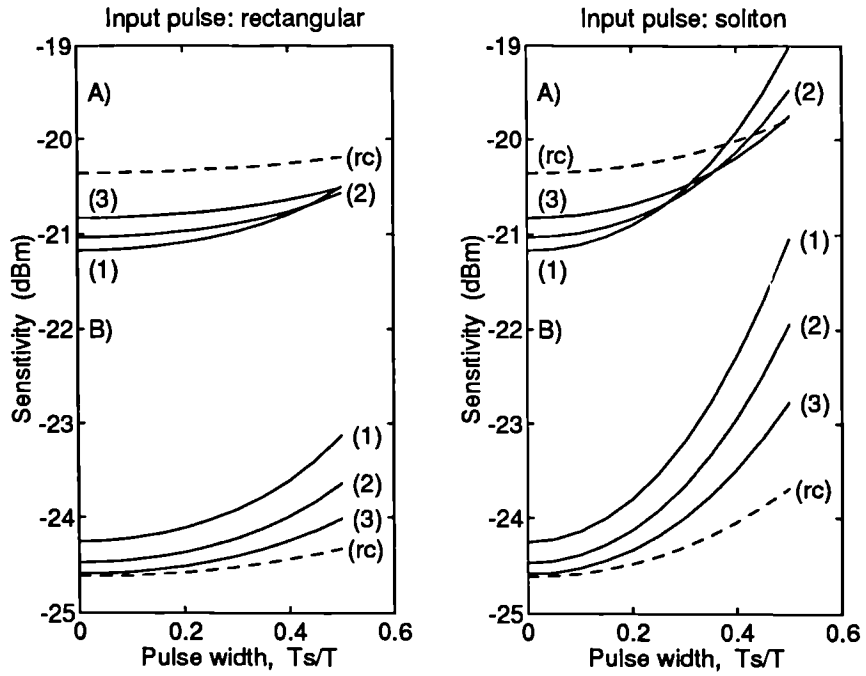

Figure 2.12: Electronic receiver sensitivity versus pulse width for A) $R_{in} = 50\,\Omega$ and B) $R_{in} = 470\,\Omega$: (1) NSD $d = 0.1$; (2) NSD $d = 0.2$; (3) NSD $d = 0.3$; (rc) RC

power spectral density at high frequencies, the value being optimised so that the influence of I_3 is minimised. This will result in comparable noise performance of electronic receivers employing both signal designs.

To assess the performance of the new signal designs in a signal dependent noise environment optically preamplified receivers will be considered and specifically the SLA preamplified receiver sensitivity will be estimated for the two cases of absence and presence of timing jitter.

For an SLA preamplified receiver the noise can be split in two components, namely a signal independent and a signal dependent noise term. The signal independent noise term can be written as a sum of three contributions

$$\sigma_i^2 = \sigma_c^2 + \sigma_{sp}^2 + \sigma_{sp-sp}^2 \tag{2.45}$$

where σ_c^2 is the value of the mean square circuit noise (defined above) and σ_{sp}^2 and σ_{sp-sp}^2 are the spontaneous emission shot noise and the beat noise between spontaneous emission components due to the OA. For the case of an APD receiver preceded by an SLA these are given by [29, 30]

$$\sigma_{sp}^2 = \eta\, q^2 M^2 F_e\, (G-1)\, n_{sp}\, m_t\, \Delta F_1\, I_2\, B \tag{2.46}$$

$$\sigma^2_{sp-sp} = \eta^2 q^2 M^2 (G-1)^2 n^2_{sp} m_t \Delta F_2 I_2 B \tag{2.47}$$

were η is the photo-detector quantum efficiency, M is the APD gain, F_e is the APD excess noise factor, G is the optical gain, n_{sp} is the population inversion parameter, m_t is the transverse mode number, ΔF_1 is the equivalent noise bandwidth for the spontaneous shot noise, ΔF_2 is the equivalent noise bandwidth for the beat noise between spontaneous emission components and the other symbols have the previously defined meanings. The optically preamplified receiver operation can be optimised by reducing the noise contributions of σ^2_{sp} and σ^2_{sp-sp}. This is achieved by placing an optical filter of bandwidth B_o between the OA and the photo-detector. However, even in these circumstances, the signal independent noise term will be dominated by beat noise between the spontaneous emission components σ^2_{sp-sp}.

The signal dependent noise term, which is entirely due to the OA, can be written as the sum of two components that in the general case depend not only on the signal power in the time slot in question but also on the signal power in the adjacent time slots

$$\sigma^2_d = \sigma^2_s + \sigma^2_{s-sp} \tag{2.48}$$

where σ^2_s is the signal shot noise and σ^2_{s-sp} is the beat noise between signal and spontaneous emission components. For a signal 'zero' or signal 'one' these are given by

$$\sigma^2_s = q \mathcal{R}_s M^2 F_e G \left[I_1 b_0 + (\Sigma_1 - I_1) b_{max} \right] B \tag{2.49}$$

$$\sigma^2_{s-sp} = 2 \eta q \mathcal{R}_s M^2 G (G-1) n_{sp} \chi \left[I_1 b_0 + (\Sigma_1 - I_1) b_{max} \right] B \tag{2.50}$$

were $b_0 \in \{b_{min}, b_{max}\}$ is the signal power in the considered time slot with b_{min} the signal power corresponding to a signal '0' and b_{max} the signal power corresponding to a signal '1', χ is the excess noise coefficient for the signal spontaneous beat noise due to facet reflectivities and I_1 and Σ_1 are the Personick noise integral and sum defined by

$$I_1 = \mathrm{Re}\left(\int_0^\infty H_p(f) \left[H_T(f) * H_T(f) \right] df \right) \tag{2.51}$$

$$\Sigma_1 = \frac{1}{2} \sum_{n=-\infty}^{\infty} H_p(n) \left[H_T(n) * H_T(n) \right] \tag{2.52}$$

with the bit period normalised to unity. With these definitions the total noise for a signal '0' and '1' can be written as

$$\sigma^2_0 = \sigma^2_t + \sigma^2_d \qquad \text{for} \qquad b_0 = b_{min} \tag{2.53}$$

$$\sigma_1^2 = \sigma_i^2 + \sigma_d^2 \qquad \text{for} \qquad b_0 = b_{max} \tag{2.54}$$

In an optimised receiver the signal dependent noise term is dominant and is almost entirely due to beat noise between signal and spontaneous emission σ_{s-sp}^2.

The noise equations described so far are for an SLA preamplified receiver but they can be easily modified to account for the noise of in an EDFA preamplified receiver if $m_t\,\Delta F_1$ and $m_t\,\Delta F_2$ are replaced by the optical filter bandwidth B_o, χ is replaced by 1 and all the noise terms multiplied by a factor of 2 to account for the two polarisation states [31, 43]

To estimate the sensitivity of the preamplified receiver a perfect extinction ratio will be assumed ($b_{min} = 0$). The noise terms involving the difference $\Sigma_1 - I_1$ will be taken into account since, as can be seen from figure 2.11, depending on the pulse width this difference can have significant values and consequently have a strong influence on the receiver sensitivity.

For SLA preamplified receivers the sensitivity can be written as

$$\overline{P} = \frac{\mathrm{SNR}}{G\mathcal{R}_s}\left\{\sqrt{K^2\,(\Sigma_1 - I_1)\,\Sigma_1 + \frac{\sigma_i^2}{M^2}} + \frac{1}{2}\,K\,(2\,\Sigma_1 - I_1)\right\} \tag{2.55}$$

with

$$K = q\,\mathrm{SNR}\,[F_e + 2\,\eta\,n_{sp}\,\chi\,(G-1)]\,B \tag{2.56}$$

When evaluating the sensitivity using equation (2.55) it is necessary to consider that the sensitivity depends on the Personick noise integrals and on Σ_1 and that these are functions of the optimum decision threshold which in turn is a function of the optical input power. For the NSD case, in order to evaluate the optimum decision threshold and sensitivity, it is necessary to solve the above equation iteratively with the two additional equations:

$$d_{opt} = \frac{\sigma_0}{\sigma_1 + \sigma_0} \tag{2.57}$$

and

$$b_{max} = 2\,\overline{P} \tag{2.58}$$

Since the values of the noise integral and Σ_1 for the RC do not depend on the decision threshold level, then such values can be used as a starting point to obtain the sensitivity and optimum threshold level for the new signal designs. The sensitivity and optimum threshold level versus the optical gain for a 10 Gbit/s preamplified PIN receiver using a 1.5 μm InGaAsP optical amplifier, are shown in figure 2.13. These results were obtained

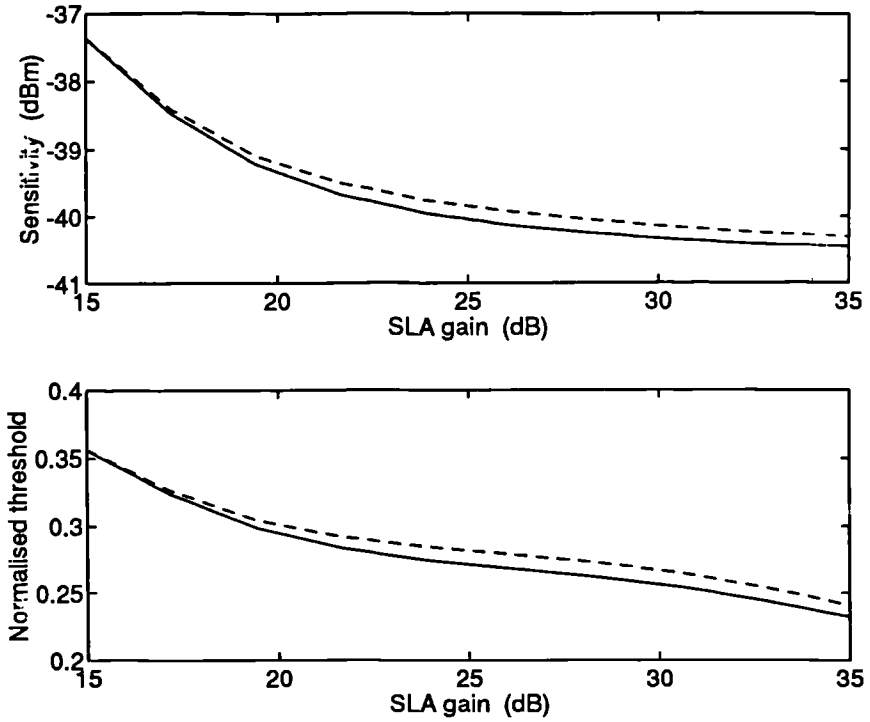

Figure 2.13: Sensitivity and optimum decision level versus optical gain:'——' NSD; '– –' RC

using data from references [44] and [30] and assuming near-traveling-wave operation (input and output facet reflectivities equal to 10^{-4}) and an optical filter bandwidth of 3 nm. Figure 2.13 shows both a small improvement in sensitivity and a slightly lower value of the optimum decision threshold for all considered values of the optical gain. This is a consequence of the smaller value of σ_t^2 for the NSD. This can be easily understood when considering that the signal independent noise is dominated by σ_{sp-sp}^2 proportional to I_2 which takes smaller values for the new signal designs. This situation can, however, be inverted when the difference $\Sigma_1 - I_1$ takes significant values. In this case, σ_0^2 will start to be dominated by σ_{s-sp}^2 due to signals in adjacent time slots resulting in both a sensitivity degradation and an increase of the optimum decision level. This is certainly not so for signaling with rectangular pulses where $\Sigma_1 - I_1 \approx 0$ for all pulse widths and also, as noted before, for soliton systems where the pulse widths must be less than $0.2T$ to avoid soliton interactions, the region where $\Sigma_1 - I_1 \approx 0$ for both signal designs.

The preamplified receiver sensitivity dependence on the timing offset is obtained by

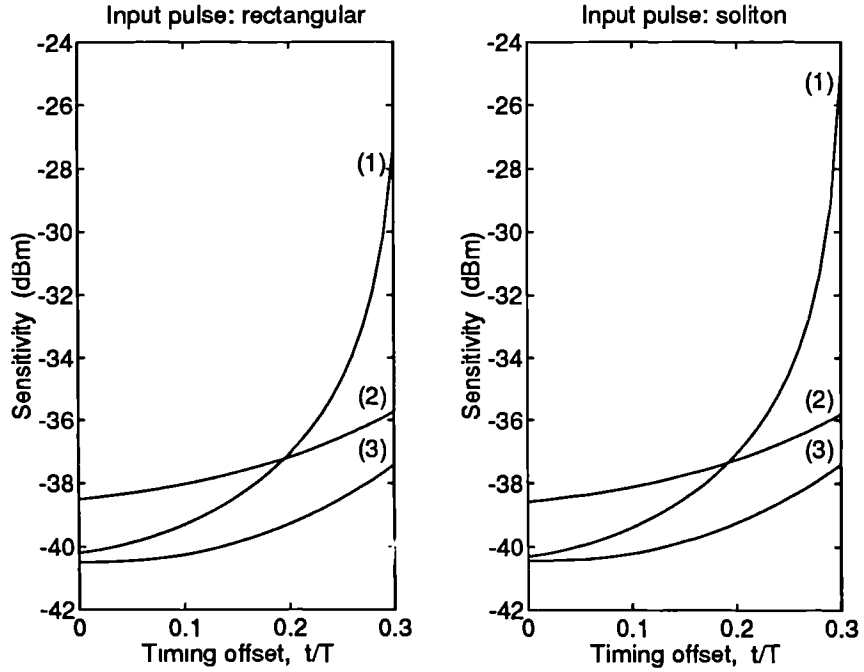

Figure 2.14: Sensitivity versus timing offset: (1) optimised RC; (2) RC with 50% decision level; (3) NSD

solving the nonlinear equation

$$P_{err} = 0.5\left\{Q\left(\frac{G\,M\,\mathcal{R}_s\,b_{max}\,[s_u(\tau)-d]}{\sigma_1}\right)+Q\left(\frac{G\,M\,\mathcal{R}_s\,b_{max}\,[d-s_l(\tau)]}{\sigma_0}\right)\right\} \qquad (2.59)$$

for b_{max} with σ_0 and σ_1 obtained from equations (2.53) and (2.54), respectively, and the value of d obtained from (2.57) for the optimised RC and NSD. Figure 2.14 shows the receiver sensitivity versus the timing offset for an optically preamplified PIN receiver ($M = 1$). The cases shown correspond to rectangular and a soliton pulses with an SLA gain of 35 dB and bit rate of 10 Gbit/s. In this figure three cases are represented: raised cosine with optimised decision level (curve (1), $d_{opt} = 0.25$ for rectangular pulse and $d_{opt} = 0.24$ for soliton pulse); raised cosine with 50% threshold level (curve (2)) and new signal design (curve (3), $d_{opt} = 0.23$ for rectangular pulse and $d_{opt} = 0.23$ for soliton pulse). The pulse widths used are $0.5T$ for the rectangular pulse and $0.15T$ for the soliton pulse. This figure clearly illustrates the advantage of the NSD — it provides a sensitivity similar to the optimised RC in the absence of timing errors and a tolerance to timing errors similar to the RC with 50% decision level, thus allowing the receiver sensitivity to be optimised without incurring undue jitter penalty.

2.4 The MCB-based approach to signal design

In section 2.3 the receiver optimisation was considered from a purely time domain viewpoint. That is, constraints (2.27), (2.28) and (2.29) were imposed on the signal at the input of the decision circuit that led to minimisation of the ISI effects in the presence of timing and signaling jitter. This approach used a very limited knowledge of the noise processes involved, namely the values of the noise variances associated with a received signal '1' and '0' and therefore of the appropriate optimum decision threshold value. In fact, noise and receiver sensitivity could only be assessed after a given transfer function had been decided upon. Also, the noise statistics at the input of the decision circuit were assumed to be Gaussian, which is not true for any optical communication system and especially for APD or optically preamplified receivers where the signal is better modeled as a marked and filtered Poisson process (MFPP) corrupted by additive Gaussian noise [45]. Here a rigorous statistical optimisation method based on the modified Chernoff bound (MCB) will be briefly reviewed. Illustrative results will be presented which show that optimal solutions obtained under the MCB criteria produce signals with the same general time domain characteristics as the signals derived in section 2.3.

The most objective criteria to evaluate optical receiver performance is the BER that can be directly linked to the bit error probability P_{err}. In a binary optical receiver the received signal, after being filtered and amplified, is sampled at a suitable instant and the sampled value y compared with the decision threshold d. If y is above the threshold d, then the received signal is identified as a symbol '1' and otherwise as a symbol '0'. The bit error probability can thus be written as

$$P_{err} = P_0 \int_d^{\infty} p(y \mid 0)dy + P_1 \int_{-\infty}^{d} p(y \mid 1)dy \tag{2.60}$$

where P_0 and P_1 are the *a priori* probabilities for the symbols '0' and '1', respectively, $p(y \mid 0)$ and $p(y \mid 1)$ are the conditional probability density functions of the compound signal and noise processes associated with the symbols '0' and '1', respectively. In principle, equation (2.60) could be minimised directly by optimising the receiver design parameters but in practice this requires detailed knowledge of the conditional PDFs of equation (2.60) which must accommodate for randomness in

- the signal process,

- the photon multiplication in the optical-preamplifier or carrier multiplication in the avalanche photodiode,
- additive Gaussian noise,
- intersymbol interference,
- signal and timing jitter.

An analytical solution for such a PDF is in general not known. As a consequence, P_{err} is not minimised directly. Instead an upper bound on P_{err} is formed and it is this upper bound that is minimised. One such bound that has been applied successfully to optical communication problems is the modified Chernoff bound (MCB). The MCB is formulated in terms of the moment generating functions (MGFs) of the signal and noise processes involved and can be written as [46, 47]

$$\text{MCB} = \frac{M_n(s, h_T(t))}{2\sqrt{2\pi}\,\sigma_c\, s}\left[M_{Y_0}(s, h_T(t))\,\exp\{-s\,d\} + M_{Y_1}(s, h_T(t))\,\exp\{s\,d\}\right] \geq P_{err} \quad (2.61)$$

assuming equal *a priori* probabilities for '0s' and '1s'. In this equation $M_n(s, h_T(t))$ is the MGF of the additive Gaussian noise, which is independent of the signal and gain processes and is given by

$$M_n(s, h_T(t)) = \exp\left\{\frac{\sigma_c^2\,(h_T(t))}{2}\,s^2\right\} \quad (2.62)$$

$M_{Y_0}(s, h_T(t))$ and $M_{Y_1}(s, h_T(t))$ are the symbol conditioned MGFs for the signal and gain processes when signals '0' or '1' are received. As written in equation (2.61), the MCB is a function of the receiver impulse response $h_T(t)$, the decision threshold d and the real parameter s ($s > 0$). Consequently, the MCB can be minimised by appropriately choosing $h_T(t)$ and the values of d and s. The optimum value of d can be readily obtained from equation (2.61) by setting

$$\frac{\partial}{\partial d}\,\text{MCB} = 0 \quad (2.63)$$

and solving for d

$$d_{opt} = \frac{1}{2\,s}\,\ln\left\{\frac{M_{Y_0}(s, h_T(t))}{M_{Y_1}(s, h_T(t))}\right\} \quad (2.64)$$

When d in equation (2.61) is replaced by the expression for d_{opt} the threshold optimised MCB is obtained and is given by

$$\text{MCB} = \frac{M_n(s, h_T(t))}{\sqrt{2\pi}\,\sigma_c\, s}\sqrt{M_{Y_0}(s, h_T(t))\,M_{Y_1}(s, h_T(t))} \geq P_{err} \quad (2.65)$$

The optimisation problem is now reduced to the search for the optimum impulse response and value of s providing the tightest possible bound. Although the optimum $h_T(t)$ can be obtained without imposing any constraints of physical realisability, it is usually assumed that a post-detection filter is used to shape the receiver impulse response. This filter, which can take the form of a lumped element network [48] or of a distributed microwave filter [49], can then be numerically optimised so that the MCB is minimised. This approach has been proven to produce near optimum solutions [48, 49] and has the advantage of avoiding realisability problems that otherwise would be encountered when trying to match the real network impulse response to the idealised optimum.

Figure 2.15 represents the eye-diagram for an APD receiver optimised using the MCB technique with the post detection filter realised as an ideal lumped element network [50]. In figure 2.16 the eye-diagram for the NSD with $d = 0.25$ is represented. These figures clearly display the time domain similarities of the two signal designs. Note that the MCB optimised design has all the time domain characteristics that were imposed when deriving the NSD without them being explicitly assumed in the MCB formalism. This is however a consequence of a jitter description of the signal process embedded in the symbol conditioned

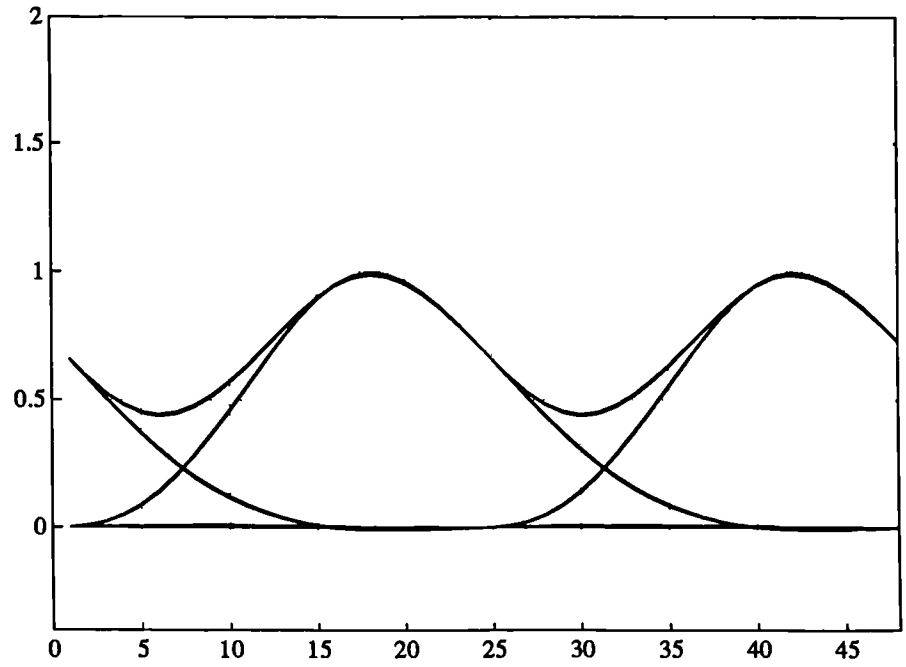

Figure 2.15: Eye-diagram for an MCB optimised APD receiver ([50], chapter 6)

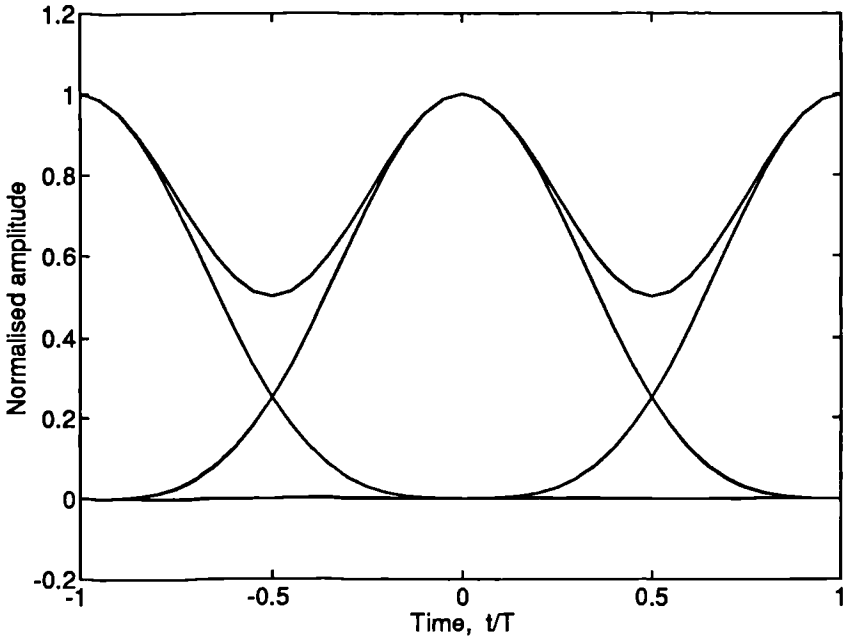

Figure 2.16: NSD eye-diagram $d = 0.25$

MGFs $M_{Y_0}(s, h_T(t))$ and $M_{Y_1}(s, h_T(t))$ which allows the receiver to be specifically optimised to show robustness over a certain range of jitter [47]

Although the MCB technique is a strictly rigorous approach that can in principle provide a full description of a system, there is nonetheless the advantage of simplicity to be gained when considering the new signal designs. More often than not, the design engineer is not in possession of the full information necessary about the system to allow a rigorous optimisation to be done or the task is too complex to be undertaken. However, in the case of the NSDs the information needed is reduced and can be easily obtained from the system experimental data.

2.5 Time domain optimisation of post-detection realisable filters

In this section, the problem of approximating the time domain constraints (2.27), (2.28) and (2.29) of section 2.3, using a realisable network will be considered. The formulation proposed by Lind and Nader [51, 52] for the design of realisable filters that minimise ISI will be adopted and extended to included constraints (2.28) and (2.29). In reference [51] a combination of variational calculus and numerical optimisation was used to determine

the set of poles that reduce the ISI to less than a pre-specified amount. Here, due to the additional complexity brought about by constraints (2.28) and (2.29), the problem will be treated from a purely numerical point of view. The case of rectangular input pulses will be considered.

2.5.1 Time domain response and cost functior

When a realisable network is used to effect pulse shaping, the constraints defined by equations (2.27), (2.28) and (2.29) are not exactly met. The total squared error for each of these constraints can serve as a measure of the network performance and consequently be used to form the cost function for numerical optimisation. This cost function can be defined as

$$E = W_{isi} E_{isi} + W_{td} E_{td} + W_{zs} E_{zs} \tag{2.66}$$

with

$$E_{isi} = \frac{1}{h_o^2(t_s)} \sum_{\substack{k=-1 \\ k\neq 0}}^{\infty} h_o^2(t_s + k) \tag{2.67}$$

$$E_{td} = \left[\frac{h_o(t_s - 0.5)}{h_o(t_s)} - d\right]^2 + \left[\frac{h_o(t_s + 0.5)}{h_o(t_s)} - d\right]^2 + \frac{1}{h_o^2(t_s)} \sum_{k=1}^{\infty} h_o^2(t_s + 0.5 + k) \tag{2.68}$$

$$E_{zs} = \sum_{k=-1}^{\infty} h_o'^2(t_s + k) \tag{2.69}$$

where $h_o'(t)$ is the time derivative of $h_o(t)$ and t_s is the sampling instant. Equations (2.67), (2.68) and (2.69) correspond to the total normalised squared error in constraints (2.27), (2.28) and (2.29), respectively, while W_{isi}, W_{td} and W_{zs} are appropriate weights. In the above equations the precursor ISI was assumed to be limited to $t_s - 1$. This is a reasonable assumption because the joint minimisation of equations (2.67) to (2.69) produces solutions with insignificant precursor ISI for times smaller than $t_s - 1$.

The success of the optimisation process is strongly dependent on the choice of the sampling instant t_s which will be based on the two following criteria:

- maximise the SNR at the filter output
- maximise the tolerance to timing errors by making the the main lobe of $h_o(t)$ as symmetrical as possible

The first criterion means that $h_o(t)$ should be sampled at its maximum amplitude point, this is

$$h_o(t_s) = \max\{h_o(t)\} \tag{2.70}$$

while the second criterion imposes the constraint that $t_s \geq 0.5$ for decision thresholds approaching 0 and $t_s \geq 1$ for $d = 0.5$. Accordingly the sampling instant will be allowed to vary freely inside the range

$$t_s \geq 0.5 \tag{2.71}$$

Note that the two conditions imposed on t_s are mutually compatible since the network delay increases with the number of elements and pulse symmetry around t_s is only achieved for high order (≥ 6) networks. Also, as discussed in [52], by letting t_s be a floating variable, peaks in the frequency response band edge are eliminated and as a result, the filter noise bandwidth is reduced.

If the pulse shaping filter is a lumped element network with pole locations p_n and residues r_n the impulse response is given by

$$h_T(t) = \begin{cases} 0, & t \leq 0 \\ \sum_{n=1}^{N} r_n \exp\{p_n t\}, & t > 0 \end{cases} \tag{2.72}$$

were N is the order of the network. For the network to be realisable, the poles p_n must be constrained to lie in the left-half of the s-plane. The network response to the input pulse $h_p(t)$ is given by $h_o(t) = h_p(t) * h_T(t)$ which for a rectangular input pulse with unity area and width T_s is

$$h_o(t) = \begin{cases} 0, & t \leq 0 \\ \sum_{n=1}^{N} \frac{r_n}{p_n T_s} \left[\exp\{p_n t\} - 1\right], & 0 < t < T_s \\ \sum_{n=1}^{N} \frac{r_n}{p_n T_s} \left[1 - \exp\{-p_n T_s\}\right] \exp\{p_n t\}, & T_s \leq t \end{cases} \tag{2.73}$$

with corresponding time derivative

$$\frac{d\,h_o(t)}{dt} = \begin{cases} 0, & t \leq 0 \\ \sum_{n=1}^{N} \frac{r_n}{T_s} \exp\{p_n t\}, & 0 < t < T_s \\ \sum_{n=1}^{N} \frac{r_n}{T_s} \left[1 - \exp\{-p_n T_s\}\right] \exp\{p_n t\}, & T_s \leq t \end{cases} \tag{2.74}$$

If the filter is restricted to be an all-pole network, then the residues r_n must satisfy the equations

$$r_n = \frac{\prod_{m=1}^{N} (-p_m)}{\prod_{\substack{m=1 \\ m \neq n}}^{N} (p_n - p_m)}, \qquad n = 1, 2, \ldots, N \tag{2.75}$$

As shown in appendix B the infinite sums of equations (2.67), (2.68) and (2.69) can be expressed in closed form and are given by

$$\sum_{\substack{k=-1 \\ k \neq 0}}^{\infty} h_o^2(t_s + k) = h_o^2(t_s - 1) + \sum_{n=1}^{N} \sum_{m=1}^{N} \frac{a_n\, a_m}{p_n\, p_m\, (x_n\, x_m - 1)} \tag{2.76}$$

$$\sum_{k=1}^{\infty} h_o^2(t_s + 0.5 + k) = \sum_{n=1}^{N} \sum_{m=1}^{N} \frac{a_n\, a_m\, b_n\, b_m}{p_n\, p_m\, (x_n\, x_m - 1)} \tag{2.77}$$

$$\sum_{k=-1}^{\infty} h_o'^2(t_s + k) = h_o'^2(t_s - 1) + h_o'^2(t_s) + \sum_{n=1}^{N} \sum_{m=1}^{N} \frac{a_n\, a_m}{x_n\, x_m - 1} \tag{2.78}$$

where

$$x_n = \exp\{-p_n\} \tag{2.79}$$

$$a_n = \frac{r_n}{T_s} [1 - \exp\{-p_n\, T_s\}] \exp\{p_n\, t_s\} \tag{2.80}$$

$$b_n = \exp\left\{\frac{p_n}{2}\right\} \tag{2.81}$$

when constraint (2.71) is satisfied. These results allow for the cost function to be evaluated exactly in the time domain. Numerical methods can now be used to find the optimum set of poles that minimise equation (2.66).

2.5.2 Optimisation process and results

Using the above results, the cost function E is a function of the decision threshold d, the pulse width T_s (that are design parameters), the pole positions p_n and the sampling instant t_s. Due to the realisability constraints that were explicitly included in the derivation of the analytical expression for the cost function, finding the optimum filter transfer function $H_T(f)$ is equivalent to obtain the pole positions p_n and the value of t_s that minimise E.

In the optimisation process, both the pole positions p_n and the sampling time t_s can be taken as optimisation variables. In such an approach, for each iteration new poles

p_n and the sampling time t_s are estimated and the value of the cost function evaluated. Alternatively, only the poles p_n are estimated and the value of t_s is obtained from equation (2.70). The latter approach being preferred, since it uses a reduced number of optimisation variables and guarantees that the signal is sampled at its maximum amplitude point.

The optimisation process was divided in two stages: generation of an initial (trial) solution followed by the refinement of this solution. In the first optimisation stage three different types of filters were used to generate the initial solution. The considered types were: Thomson (maximum flat delay), Butterworth and Parabolic filters. After selection of the order and type of filter, the filter bandwidth was optimised to minimise the cost function. In the second optimisation stage, the pole positions obtained from the bandwidth optimised filter were then optimised to obtain a further reduction in the value of the cost function. From this optimisation process it was found that the bandwidth optimised Thomson filter provides near optimum performance with improved performance for higher order networks. Of the bandwidth optimised filters, the Butterworth gave the worst results due to excessive ripple in the time domain response that resulted in large amounts of ISI. Finally, the parabolic filter provided a reasonable performance but with a skewed time domian response around the sampling instant. In figures 2.17 and 2.18 the cost function is plotted as function of the decision threshold value for a 7^{th}-order optimum filter and for the bandwidth optimised Thomson filter, respectively. For both filter types the normalised rms ISI is less than 6×10^{-3} for all values of d and T_s considered ($T_s \in \{0.1, 0.2, \ldots, 0.6\}$). From these figures it can be observed that the cost function increases sharply for values of $d > 0.35$ which corresponds, as expected, to the range of values of d where the theoretical spectrum of equation (2.33) becomes negative.

Figures 2.19, 2.20 and 2.21 show the eye-diagram for the ideal pulse shape of equation (2.7), the optimum filter and the optimised bandwidth Thomson filter. The results are for $d = 0.2$ and $T_s = 0.5$ with poles $p_1 = -5.77$, $p_{2,3} = -5.66 \pm j1.74$, $p_{4,5} = -4.26 \pm j4.28$ and $p_{6,7} = -2.67 \pm j7.30$ for the optimum filter and poles $p_1 = -6.16$, $p_{2,3} = -5.90 \pm j2.15$, $p_{4,5} = -5.04 \pm j4.36$ and $p_{6,7} = -3.32 \pm j6.72$ for the bandwidth optimised Thomson filter ($BW = 0.59$). The weight setting used in the cost function was $W_{isi} = W_{td} = W_{zs} = 1$ which was found to work well in practice. The filter transfer functions for the three case are shown in figure 2.22. This figure shows that the three magnitude responses are very similar and in particular the magnitude response of the optimum and Thomson filters are indistinguishable, although they correspond to two different set of poles. The

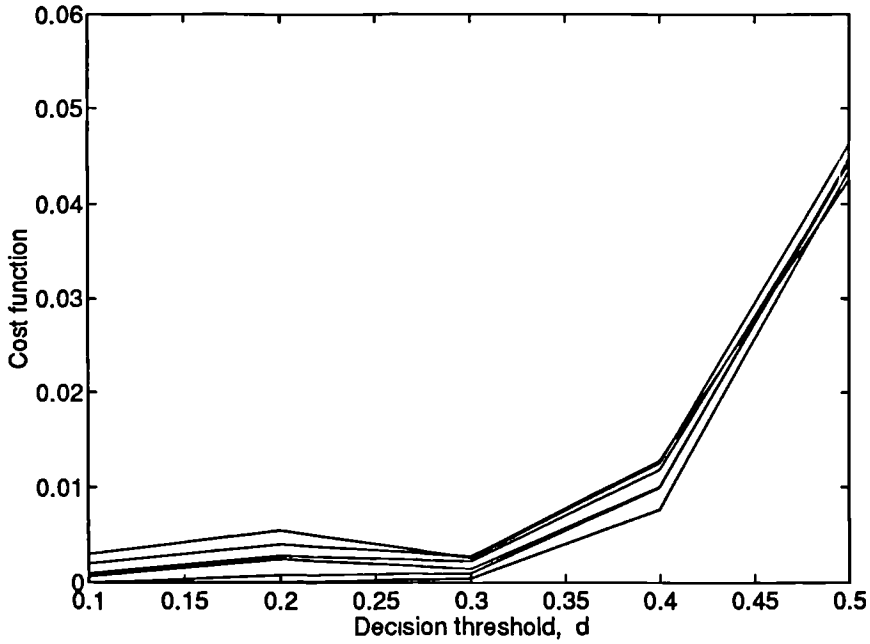

Figure 2.17: Optimum filter cost function vs d for different values of T_s and $N = 7$

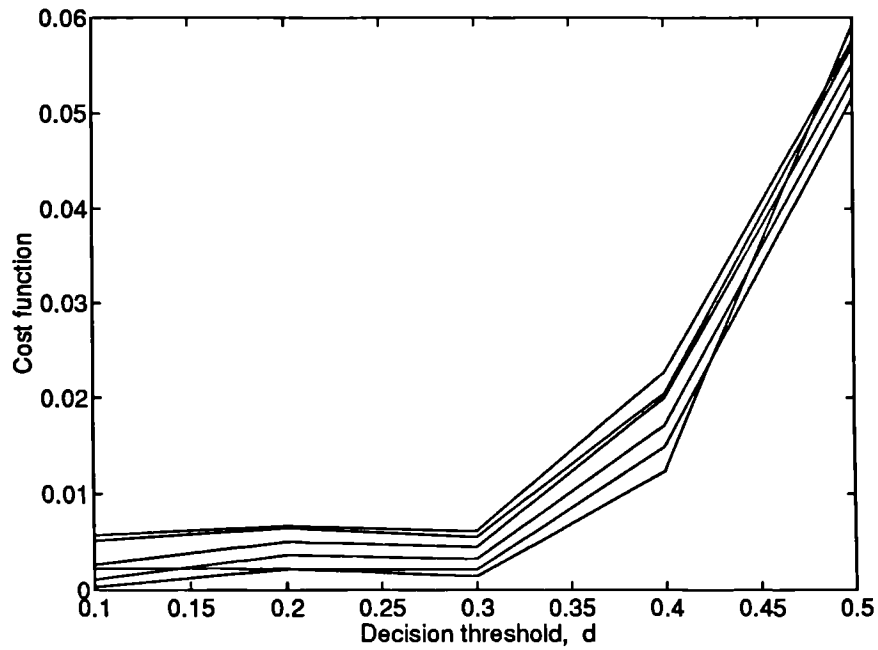

Figure 2.18: Optimised bandwidth Thomson filter cost function vs d for different values of T_s and $N = 7$

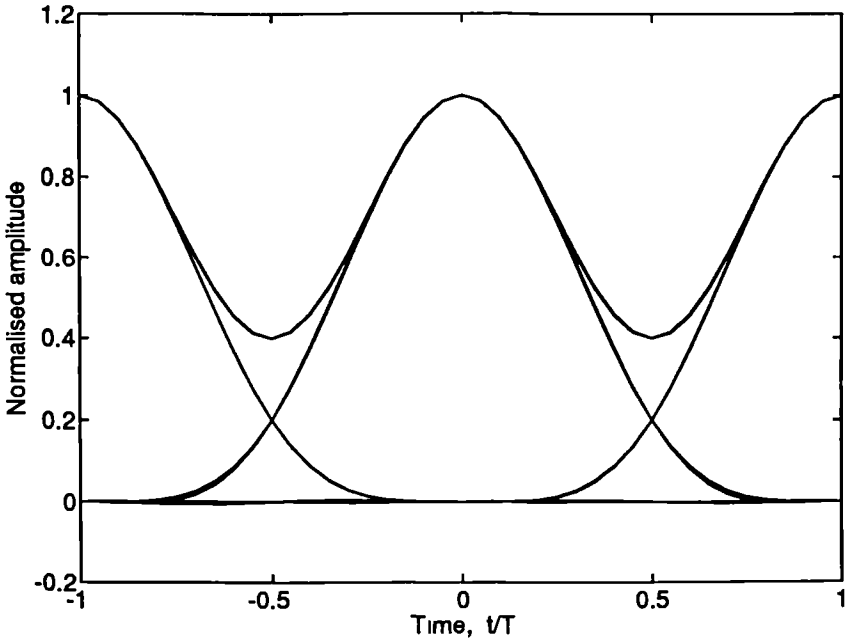

Figure 2.19: NSD eye-diagram for $d = 0.2$

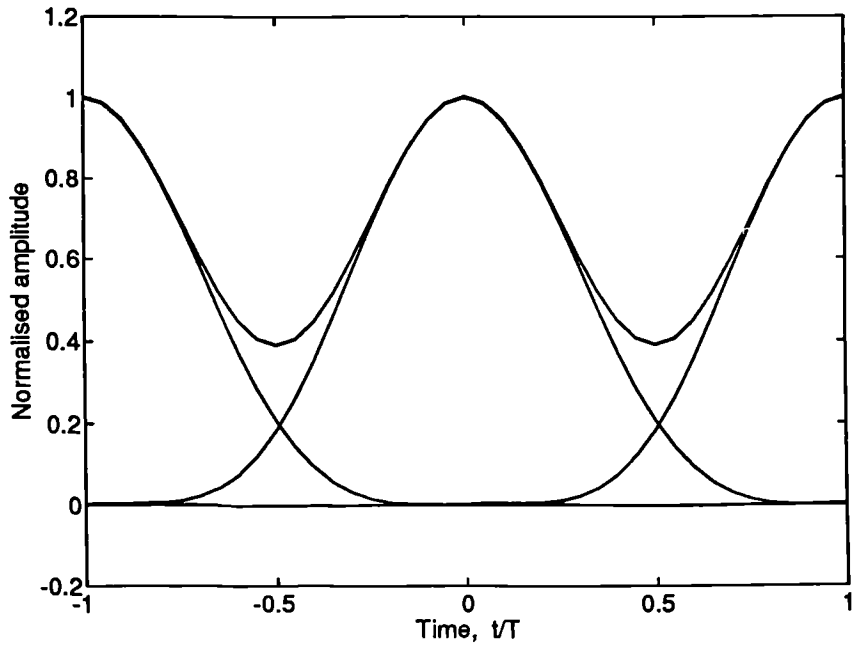

Figure 2.20: Optimum filter eye-diagram for $d = 0.2$ and $T_s = 0.5$

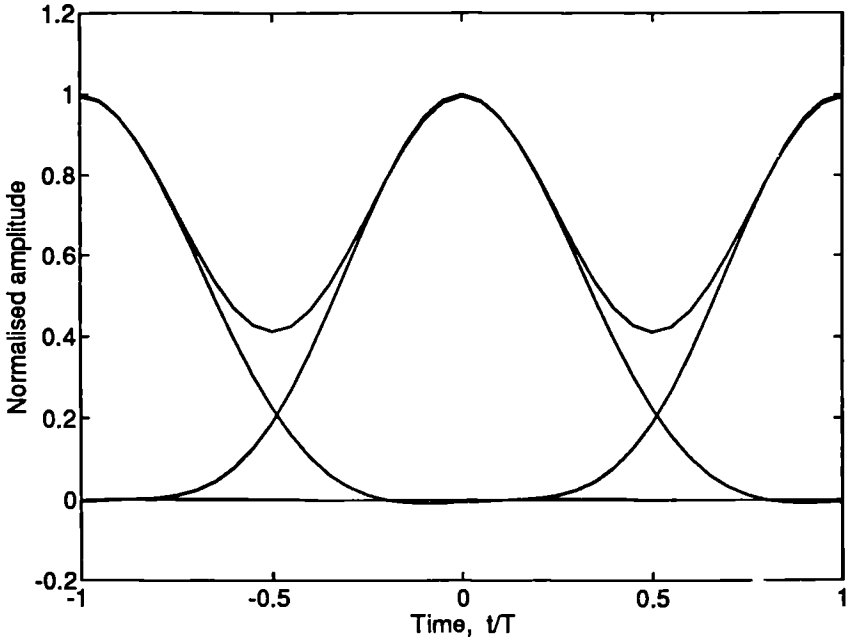

Figure 2.21: Thomson optimised filter eye-diagram for $d = 0.2$ and $T_s = 0.5$

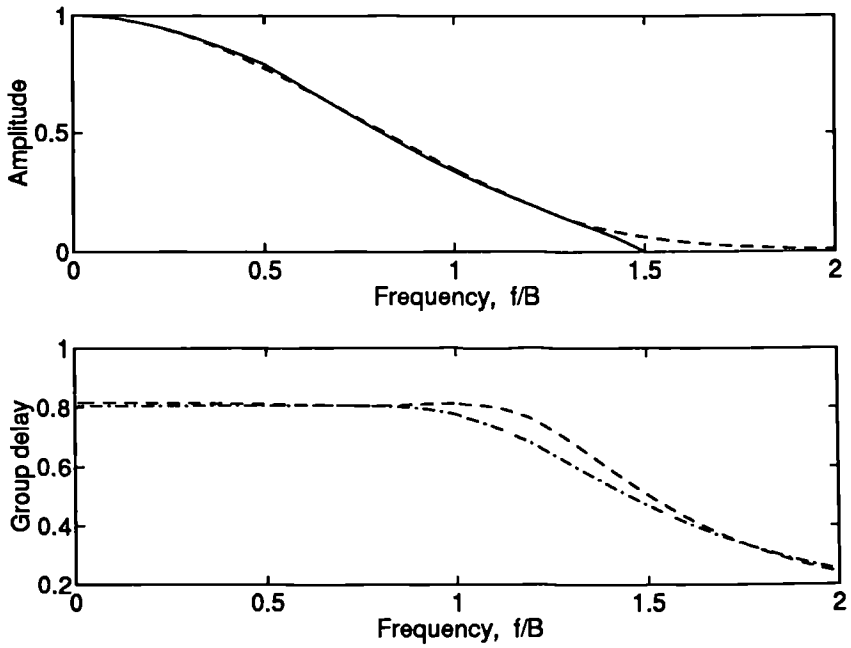

Figure 2.22: Filter transfer function for $d = 0.2$ and $T_s = 0.5$, NSD: '——'; optimum: '– –'; Thomson '– · –'

main difference between the two is in the group delay with the optimum filter showing a flatter response over a wider frequency range and thus closer to an ideal constant delay response. The approach to signal design developed in this section is especially well suited for practical implementation since realisability constraints were built into the the problem formulation. The method avoids the use of idealised target functions and allows the filter to be optimised directly in the time domain. For the higher bit-rates of interest for today's optical communications, networks have to be modeled as being composed by distributed elements rather than by lumped elements as assumed here. As a consequence, the network impulse response is no longer given by equation (2.72) and the analysis presented here would have to be reformulated to account for the filter distributed nature. Despite this, the time and frequency domain responses obtained by such an approach can be used as 'realistic' targets for truly distributed networks or networks realised using quasi-lumped elements as is the case of passive filters implemented as monolitic microwave integrated circuits (MMICs).

2.6 Summary

In this chapter signal processing for digital optical receivers was considered. Several approaches for PIN receivers, where noise is considered as signal independent and optimum solutions are known, were reviewed. In the case of receivers dominated by signal dependent noise, such as optically preamplified or APD receivers, it was shown that the commonly used raised cosine target can result in either non-optimum sensitivity or poor tolerance to timing and signaling jitter. A new family of wave forms was derived that allows both optimised sensitivity and jitter tolerant operation to be obtained. The derivation of the new signal designs was based on strict time domain constraints and on the knowledge that optimised sensitivity requires the receiver decision threshold to be set at a low level in the vertical eye opening. Sensitivity implications for optically preamplified receivers were examined indicating that the new signal designs produce receivers with sensitivities similar to the optimised raised cosine receiver but with a much improved tolerance to jitter.

An optimisation technique based on the modified Chernoff bound that allows a rigorous statistical description of all the noise processes involved in optical direct detection was described. This approach was shown to produce signals with the same time domain characteristics as the NSDs.

Finally, the problem of using realisable networks to effect the NSDs pulse shaping was addressed. It was shown that optimised all-pole networks of order ($N \geq 6$) can provide almost ideal pulse shaping and that a bandwidth optimised Thomson filter can be used as a near optimum equaliser.

Although the realisability problem was addressed in this chapter, this was only done from a formal point of view. It is thus necessary to consider the problem of practical realisation of such signal designs using currently available technologies. The next chapters will address this problem for multi-Gbit/s systems.

Chapter 3

GaAs technology and noise modelling

In this chapter, the technology used for the practical realisation and assessment of the signal shaping strategies discussed in the previous chapter is described. Microwave monolithic integrated circuit (MMIC) technology is now a mature technology and offers an attractive prospect for use in optical communication systems. Commercially available GaAs MMIC technologies allow the integration of active and passive components on the same die thus allowing the realisation of compact passive and active structures. This has the advantage of reducing production costs and, more importantly, overcomes problems of reliability and repeatability usually encountered in discrete and hybrid optical receivers designed for multi-Gbit/s operation.

The MMIC GaAs process used in the research described in this thesis was optimised and fully characterised for operation up to 20 GHz. The process and devices are briefly described in this chapter together with their circuit models. This will aid understanding of the process limitations and will provide the necessary background for the circuit optimisation methods to be developed in subsequent chapters.

No noise models are provided by the foundry for the active devices (GaAs MESFETs). Instead, measured two-port noise parameters are given at a few frequency points for the standard MESFET cells when biased for minimum noise. This information proved to be insufficient for accurate noise optimisation of optical receivers and consequently a MESFET noise model was adopted. The noise model and the method used for the de-embedding of its intrinsic noise coefficients are described in detail in this chapter. Finally, the adopted model and the noise de-embedding technique are validated for the foundry devices by comparing the predicted noise parameters with experimental data.

3.1 The GaAs foundry process

The foundry is a high performance GaAs multilayered process based on direct ion implantation into GaAs semi-insulating (SI) substrate. It has three metallisation layers, two dielectric layers, a mesa and mesa trim layer, thus allowing for the implementation of MESFETs and several types of passive and interconnecting structures. The process FETs are 0.5 μm gate length depletion mode MESFETs and have nominal cut-off frequencies of 20 GHz.

A cross-sectional view of the layer structure of a GaAs MMIC is represented in figure 3.1. A mesa layer is grown on the SI substrate which is used to form the MESFETs and the

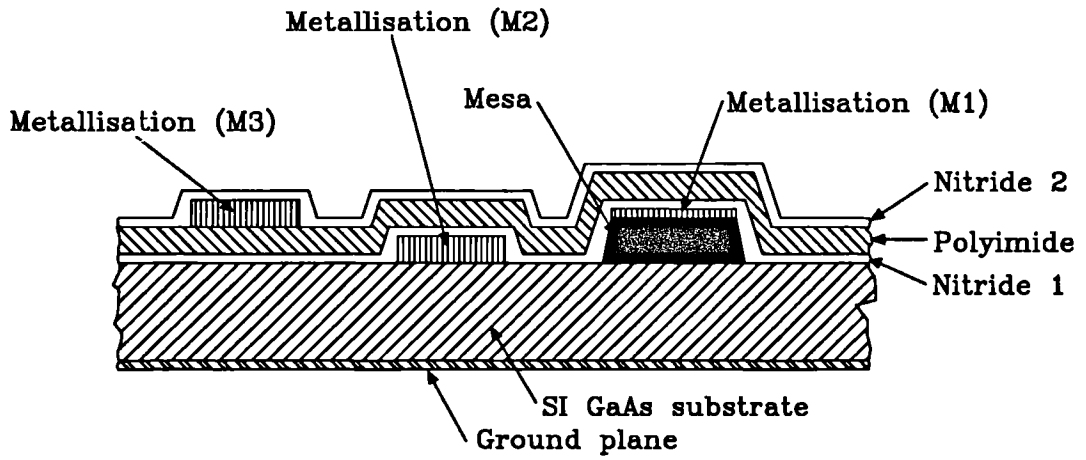

Figure 3.1: GaAs MMIC cross-sectional view

resistors. The mesa layer can be etched to allow the production of high value resistors. A metal layer (M1) is used to make the ohmic contacts with the mesa structure for production of resistors and the MESFET source and drain electrodes. The next metal level (M2) is used to form the MESFET gate Schottky contact. This metal is also used for the bottom plates of the metal-insulator-metal (MIM) capacitors, the interdigital capacitors, the underpass interconnections, the lower level transmission lines and the base metallisation for the bond pads. Interlayer dielectrics — Silicon Nitride (nitride 1) and Polyimide — are placed on the wafer to separate the metal layers, passivate the active devices and provide the dielectric for the overlay capacitors. Via holes are etched in the two dielectric layers and filled with metal at those points were connections have to be made between the various metal layers. A top metal level (M3) is added which provides for the low-loss transmission lines, planar inductors, capacitor top plates and bond pads. A final layer of silicon nitride (nitride 2) is

used to act as a protection and passivation layer covering the whole die with the exception of the bonding areas. Finally, through-GaAs vias are used to provide a low-inductance path to the back-face ground plane.

3.2 Device modelling

All the devices in the process, except transmission lines, are modelled by lumped element equivalent circuits. The models are based on measurements made on the foundry standard cells for frequencies up to 20 GHz. Closed form polynomial expressions relate the value of the prime element of the equivalent circuit to the device physical dimensions. The parasitic elements, representing the device non-ideal behaviour, are then related to the physical dimensions again using closed form polynomial expressions.

A brief description of the devices of relevance to this work is given below, together with the equivalent circuit models. For each device, the derived two-port chain-matrix (better known as the ABCD-matrix) is presented. These subsequently will be used in the thesis for the time domain simulation and optimisation of post-detection signal shaping filters.

3.2.1 Passive devices

Resistors

A typical GaAs mesa resistor layout is illustrated in figure 3.2. The resistor is manufactured on the ion implanted GaAs mesa layer that can be either etched or unetched, resulting in sheet resistivity values of 300 Ω/□ and 180 Ω/□, respectively. This allows the production of resistors of values ranging from 10 Ω to 10 kΩ. The equivalent lumped element model of

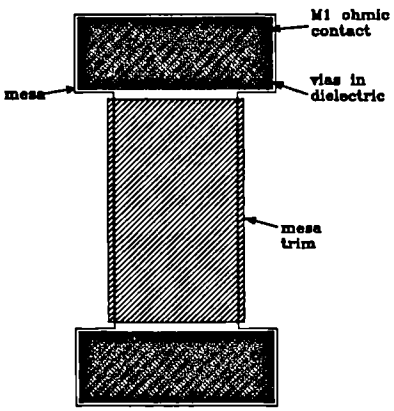

Figure 3.2: Mesa resistor layout

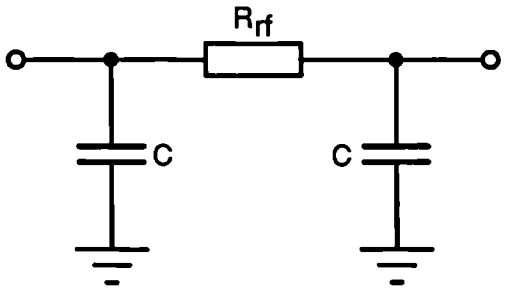

Figure 3.3: Mesa resistor model

the mesa resistor is shown in figure 3.3. The resistor model includes a series resistance of frequency dependent value to account for the skin effect. The chain matrix for the resistor equivalent circuit is given by

$$\mathbf{R} = \begin{bmatrix} 1 + s\,C\,R_{rf} & R_{rf} \\ s\,C\,(2 + s\,C\,R_{rf}) & 1 + s\,C\,R_{rf} \end{bmatrix} \tag{3.1}$$

The mesa resistors are linear at low voltages only. A resistor behaviour within 10% of the ideal linear behaviour can be achieved by using a resistor with minimum length

$$L_{min} = 4V^2 \tag{3.2}$$

were L_{min} is in μm and V is the voltage drop across the resistor in volts .

MIM capacitors

Two types of metal-insulator-metal capacitors can be constructed. These are the silicon nitride and the polyimide overlay capacitors. High value MIM capacitors can be formed with the silicon nitride as the insulating material, giving capacitances in the range 1.3 – 59 pF. Lower value MIM capacitors can be formed using as insulating material a combination of the two dielectric layers (the silicon nitride and the polyimide) giving capacitance values in the range 0.06 to 2.5 pF. Figure 3.4 shows the physical layout of a silicon nitride

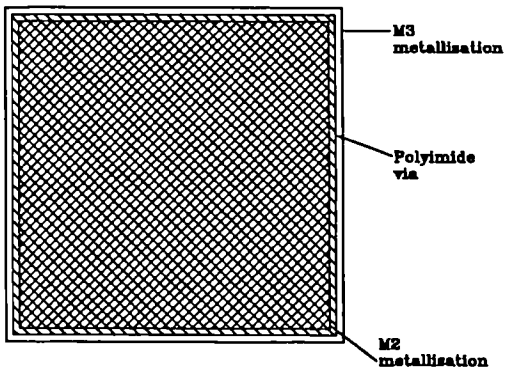

Figure 3.4: MIM capacitor layout

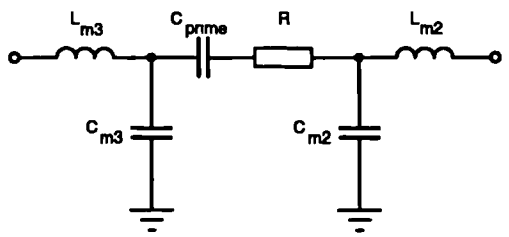

Figure 3.5: MIM capacitor model

capacitor. The polyimide capacitor has a similar layout but the polyimide via is omitted. An equivalent circuit model, valid for both types of capacitor, is shown in figure 3.5 and the corresponding chain matrix is given by

$$\mathbf{C} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \tag{3.3}$$

where

$$c_{11} = 1 + Z_3 Y_2 + Z_4 c_{21} \tag{3.4}$$

$$c_{12} = Z_3 + Z_5 (1 + Z_3 Y_2) + Z_4 c_{22} \tag{3.5}$$

$$c_{21} = Y_1 (1 + Z_3 Y_2) + Y_2 \tag{3.6}$$

$$c_{22} = 1 + Z_3 Y_1 + Z_5 c_{21} \tag{3.7}$$

with

$$Y_1 = s\,C_{m2} \tag{3.8}$$

$$Y_2 = s\,C_{m3} \tag{3.9}$$

$$Z_3 = R + \frac{1}{s\,C_{prime}} \tag{3.10}$$

$$Z_4 = s\,L_{m2} \tag{3.11}$$

$$Z_5 = s\,L_{m3} \tag{3.12}$$

Due to the low dielectric loss of silicon nitride, the resistance value in the equivalent circuit model is set to zero for silicon nitride capacitors. Also, for silicon nitride MIM capacitors the equivalent circuit is symmetric with $C_{m2} = C_{m3}$ and $L_{m2} = L_{m3}$.

Planar spiral inductors

Planar inductors are produced from a square spiral in the M3 metallisation level, as shown in figure 3.6, with values ranging from 0.35 to 13 nH. The equivalent circuit model of figure

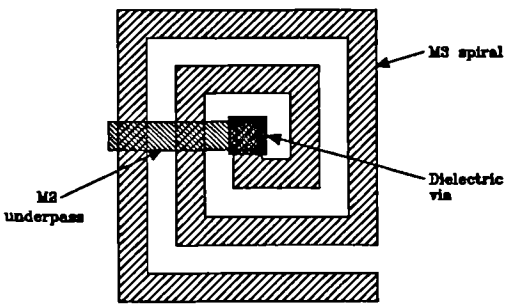

Figure 3.6: Spiral inductor layout

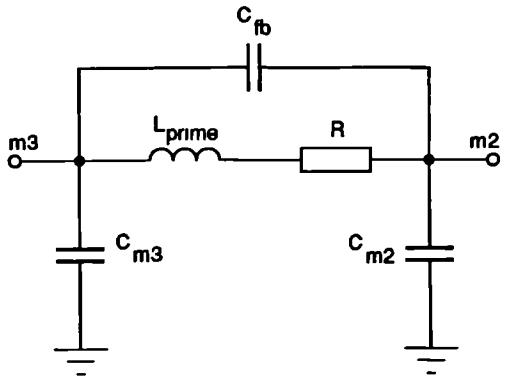

Figure 3.7: Spiral inductor model

3.7 is capable of modelling the inductor behaviour up to 80% of the s_{21} resonant frequency. Resonant frequencies can vary from 32 GHz for a three turn inductor to 8 GHz for a seven turn inductor. The inductor model is asymmetrical and its chain matrix is given by

$$\mathbf{L} = \begin{bmatrix} 1 + Z_3 Y_2 & Z_3 \\ Y_1 (1 + Z_3 Y_2) & 1 + Z_3 Y_1 \end{bmatrix} \tag{3.13}$$

where

$$Y_1 = s\, C_{m3} \tag{3.14}$$

$$Y_2 = s\, C_{m2} \tag{3.15}$$

$$Z_3 = \frac{R + s\, L}{1 + s\, C_{fb} (R + s\, L)} \tag{3.16}$$

Transmission lines

Transmission lines are implemented as microstrip lines using the M2 or M3 metal layers with metal M3 preferred due to its lower loss characteristics. Impedance values ranging from 40 Ω to 110 Ω can be obtained. A cross-sectional view of a M3 line is shown in figure 3.8. For both type of lines, the chain matrix is written as

$$\mathbf{L} = \begin{bmatrix} \cos(\varphi) & \jmath\, Z_0 \sin(\varphi) \\ \jmath\, Z_0^{-1} \sin(\varphi) & \cos(\varphi) \end{bmatrix} \tag{3.17}$$

where Z_0 is the characteristic impedance of the line and φ is the electrical length given by

$$\varphi = 2\pi\, c_0^{-1}\, f \sqrt{\varepsilon_{eff}}\, l \tag{3.18}$$

f being the frequency, c_0 the speed of the light, ε_{eff} the frequency dependent effective dielectric constant and l the physical length of the line. The foundry provides polynomial

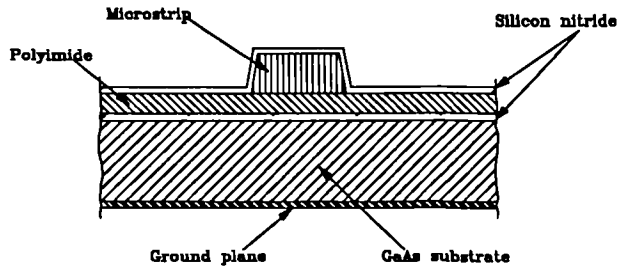

Figure 3.8: Cross-section of a M3 microstrip transmission line

expressions that relate Z_0 and ε_{eff} to the line width for both M2 and M3 lines. Due to the multi-dielectric nature of these microstrip lines, conventional microstrip simulator models cannot be used directly to predict performance. Nonetheless, isolated bend discontinuities can be accommodated by applying a length correction to the lines adjoining the bend. Data for both unchamfered and 50% chamfered bends are given by the foundry but models for microstrip T-junctions or coupled bends are not provided, although bends are assumed to be coupled when they are less than 250μm apart.

Other forms of transmission lines, such as coplanar lines, can be constructed but are not supported by the manufacturer's electrical models.

Bond pads

Bond pads are builtup from M2 and M3 metals that are connected through vias in the polyimide and nitride 1 layers. A window is opened in the nitride 2 to allow bonding to the M3 metallisation level. Bond pads are represented electrically by a capacitance to ground with a value proportional to the pad dimension.

Via Holes

Through GaAs vias are used to provide low impedance d.c. and r.f. ground paths. Ground vias are 50 μm in diameter and are etched from below the die to a standard 120 μm bond pad. They are modelled as a series inductor and resistor to ground.

Chip interface models

An electrical model is provided by the foundry for the physical transition between the GaAs MMIC and the r.f. input and output transmission lines on alumina. The physical transition is illustrated in figure 3.9 and the corresponding equivalent circuit is shown in figure 3.10. The model assumes 50 Ω microstrip alumina lines with the top of the GaAs chip at the same height as the top of the alumina substrate. Two sets of equivalent circuit element values are given, corresponding to alumina thicknesses of 635 μm and 245 μm. The model is valid up to 14 GHz for 635 μm alumina and up to 20 GHz for 245 μm alumina substrate. The elements of the chain matrix for the physical transition are

$$c_{11} = 1 + Z_3 Y_2 + Z_4 c_{21} \tag{3.19}$$

$$c_{12} = Z_3 + Z_4 c_{22} \tag{3.20}$$

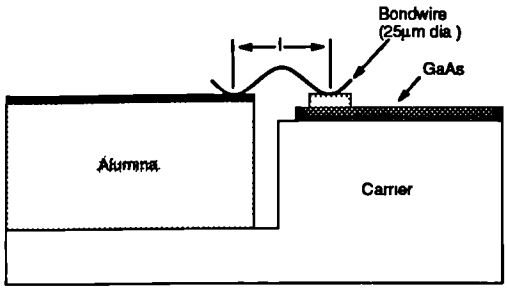

Figure 3.9: MMIC/Alumina transition

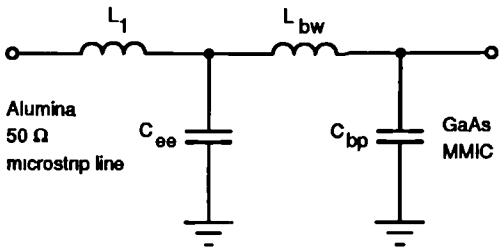

Figure 3.10: MMIC/Alumina transition model

$$c_{21} = Y_1(1 + Z_3Y_2) + Y_2 \tag{3.21}$$

$$c_{22} = 1 + Z_3Y_1 \tag{3.22}$$

where

$$Y_1 = s\,C_{ee} \tag{3.23}$$

$$Y_2 = s\,C_{bp} \tag{3.24}$$

$$Z_3 = s\,L_{bw} \tag{3.25}$$

$$Z_4 = s\,L_1 \tag{3.26}$$

3.2.2 Active devices

The foundry active devices are 0.5 μm gate length MESFETs with a II - gate geometry as shown in figure 3.11. The FET active area is defined in the mesa layer with the source and drain ohmic contacts in the M1 metallisation level. Interconnections between the ohmic contacts in the source and the drain are made using metal M3. The gate is formed in

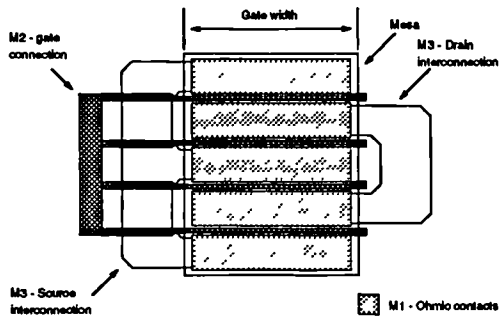

Figure 3.11: Four finger MESFET layout

the M2 metallisation level and the allowed geometries are 1, 2, 3, 4 and 6 finger FETs with individual finger widths ranging from 50 μm to 175μm. Typical figures for the FETs, as a function of the total gate width, are g_m = 148 mS/mm, g_{ds} = 11.5 mS/mm and f_T = 19 GHz at a bias current equal to 100% of I_{dss}. For low noise operation the devices should be biased at 20% of I_{dss} in which case g_m = 82 mS/mm, g_{ds} = 11 mS/mm and f_T = 16 GHz. The mean I_{dss} figure for the MESFETs is 150 mA/mm.

The foundry provides bias dependent, scalable, linear FET models. These models cover all the allowed FET geometries and are valid for bias currents within the range 10%–100% of I_{dss}. The validity of the models is, however, restricted to V_{ds} = 5 V. Alternatively, circuit values for the small-signal FET equivalent circuit model of figure 3.12 are given for some geometries at fixed bias points. This equivalent lumped element circuit is capable

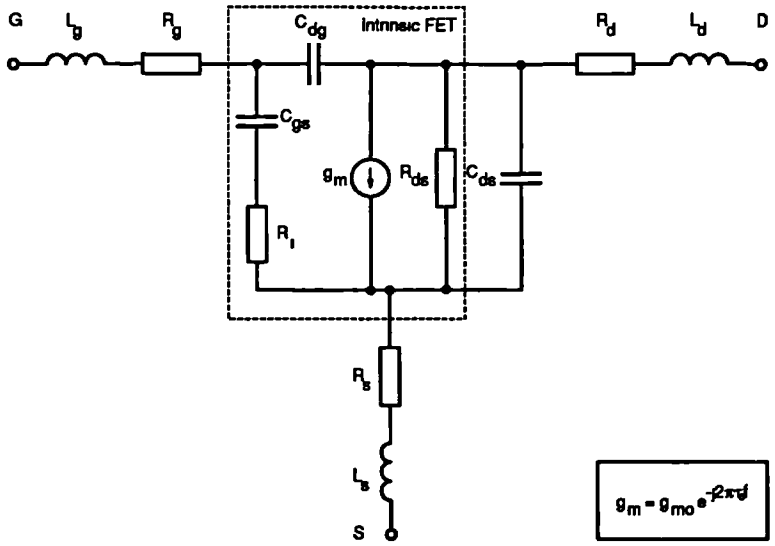

Figure 3.12: MESFET equivalent circuit

of modelling the FET behaviour to frequencies over 20 GHz. The physical origin of the various circuit elements of the model is represented in figure 3.13. The model is subdivided into two parts, the intrinsic parameters that characterize the active region under the gate and are functions of the biasing conditions and the extrinsic parameters that are bias independent. Both types of parameter depend on the device dimensions and are functions of the technological parameters. The intrinsic parameters comprise the input capacitance C_{gs}, the transconductance g_{mo}, the output conductance g_{ds} and the feedback capacitance C_{dg}. These parameters can be related to variations in the drain current and the stored charge in the active region of the device as functions of the gate and drain voltages [53].

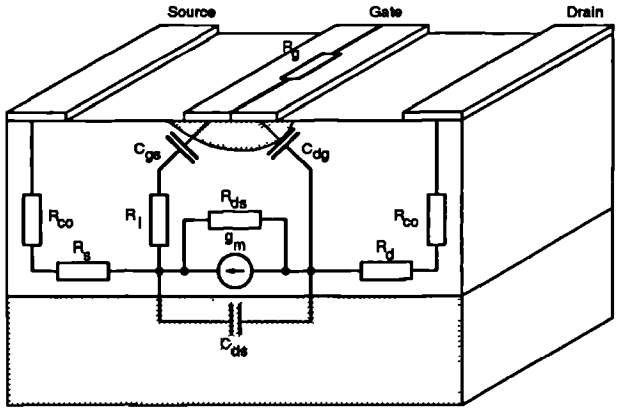

Figure 3.13: Physical origin of the MESFET equivalent circuit

Additionally, the gate charging resistance R_i and the time τ_o taken by the carriers to travel under the gate region are necessary for correct modelling of the electrical behaviour of the intrinsic device. The extrinsic circuit elements are:

- the inductances L_g, L_d and L_s associated with the size of the electrodes and interconnections;
- the series gate resistance R_g used to model the voltage drop associated with the flow of gate current in the gate metallisation;
- the source R_s and drain R_d resistances composed of the electrode contact resistance (R_{co}) and the resistance of the doped source and drain access regions, respectively;
- C_{ds} corresponding to the substrate capacitance.

The equivalent circuit element values for the foundry FETs were obtained from s-parameter measurements on devices in the common-source (CS) configuration. Since through-GaAs via holes are used for source grounding, the values of R_s and L_s actually model the FET source extrinsic elements plus the via connections. For other configurations, common-drain (CD) and common-gate (CG), this must be considered and the via effect subtracted for R_s and L_s.

3.3 Noise modelling

The noise behaviour of a passive or active device can be fully characterized at microwave frequencies by three noise parameters: the minimum noise factor F_{min}, the optimum source

admittance Y_{opt} and the equivalent noise resistance R_n, together with a set of small-signal parameters such as the s-parameters or any other equivalent set [54, 55]. Noise analysis of a microwave circuit can then be effected using the measured values of the noise and small-signal parameters of the device. There are, however, some advantages to be gained by using circuit noise models instead of measured parameters. First, noise models for the passives can be simply obtained from the equivalent circuit without the need for a separate noise characterisation. Secondly, noise measurement techniques are, at present, time consuming and susceptible to experimental error [56]. Thus, measured noise parameters are usually provided by device manufacturers at only a limited number of frequencies. In this case, a noise model must be used to either interpolate or extrapolate the device noise behaviour at those frequencies where no experimental data is available. Finally, the MMIC designer may use the active device in configurations other than the one in which the device was characterised (usually the CS configuration). This normally amounts to removing the effects of grounding impedances of the source electrode (usually via holes) to account correctly for the noise performance of the other configurations. This operation is only possible if the noise model adopted has physical significance.

For the GaAs foundry used the manufacturer provides measured values of F_{min}, Y_{opt} and R_n in the frequency range 2–20 GHz in 2 GHz steps. These parameters are given for the standard foundry FET cells biased for low noise operation. As discussed before, for these standard geometries the manufacturer also provides the element values of the FET small-signal equivalent circuit. This information on its own, due to the sparsity of the noise characterization, is not sufficient for accurate noise analysis of the broad and narrow-band optical receivers that will be discussed in the following chapters. Nonetheless, it is sufficient to obtain the parameters of a noise model that can be used to predict the noise performance of the devices over the desired frequency range. The method used to obtain such parameters is discussed in the following sections.

3.3.1 The MESFET noise model

As for the case of small-signal modelling, the noisy FET can be separated into two parts, the extrinsic and the intrinsic device. The extrinsic noisy FET, shown in figure 3.14, consists of the noiseless elements L_g, L_s, L_d and C_{dg} and the access resistances R_g, R_s and

R_d that generate thermal noise with spectral densities given by

$$\frac{d}{df}\langle i_n i_n^* \rangle = \frac{2\,k\,\theta}{R_n}, \qquad n = g, s \text{ and } d \tag{3.27}$$

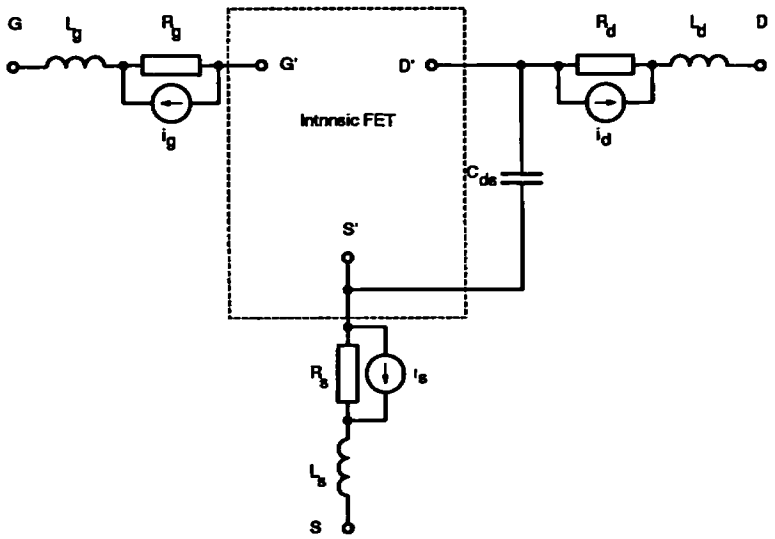

Figure 3.14: Extrinsic FET noise model

The inductances L_g, L_s, L_d and the substrate capacitance C_{ds} whilst not contributing directly to the generation of noise, introduce a frequency dependence in the noise generated by the extrinsic FET thermal noise sources and transform the noise spectrum associated with the intrinsic device. Equation (3.27) can only be used to predict the thermal noise generated by the extrinsic circuit if the values of the access resistances are 'physical' values. Since these are obtained from the small-signal model of the MESFET, which is obtained using parameter fitting techniques, this might actually not be the case. However, for the foundry FETs the values given for the extrinsic components are practically independent of the bias conditions, which tends to indicate the self-consistency of the model and consequently the physical significance of the extrinsic element values [57].

The model chosen to represent the intrinsic noisy FET is shown in figure 3.15. It has been extensively used in the literature for the noise modelling of MESFETs and was first proposed by Van der Ziel [58, 59]. The model characterizes the noise behaviour of the intrinsic FET by introducing two noise current generators; one in the gate input circuit i_g and the other in the drain output circuit i_d. The resistors R_i and R_{ds} are assumed to be noiseless, with their noise contribution totally included in i_g and i_d.

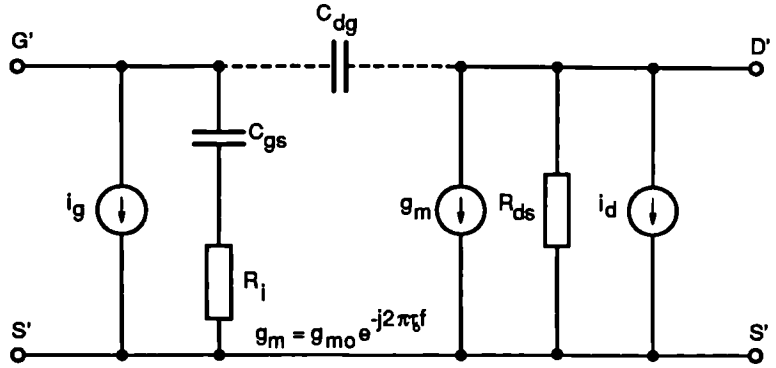

Figure 3.15: Intrinsic FET noise model

The noise current generator i_d represents the short-circuit channel noise generated in the drain-source path. This can be shown to have a white spectrum in the microwave frequency range [56] with power spectral density given by

$$\frac{d}{df}\langle i_d i_d^* \rangle = 2\,k\,\theta\,g_{mo}\,P \tag{3.28}$$

where P is a dimensionless coefficient that depends on the d.c. bias conditions, the device geometry and the technological parameters. In the absence of drain bias, this noise source represents the thermal noise generated in the drain resistance R_{ds} [60]. For positive bias, the channel noise is larger than the thermal noise generated in R_{ds} alone. The channel noise is then attributed to different phenomena such as hot-electron noise, inter-valley-scattering noise and high-field diffusion noise [56, 60]. Besides, any thermal noise generated locally in the channel modulates the conductive cross section of the channel and results in an amplified noise voltage at the drain [58, 60]. Additionally, locally generated noise voltages in the channel result in charge fluctuations in the depletion region that in turn induce a compensation charge fluctuation in the gate electrode [59, 60]. The total induced-gate charge fluctuation is described, in the intrinsic noise model, by the noise current generator i_g which has frequency dependent power spectral density given by

$$\frac{d}{df}\langle i_g i_g^* \rangle = 2\,k\,\theta\,\frac{(\omega\,C_{gs})^2}{g_{mo}}\,R \tag{3.29}$$

where $\omega = 2\,\pi\,f$ and R is a dimensionless coefficient dependent on the FET geometry, the bias conditions and the technological parameters. Since, i_g and i_d have a common origin, the two noise sources are partially correlated with cross-correlati n spectral density given by

$$\frac{d}{df}\langle i_g i_d^* \rangle = \jmath\,2\,k\,\theta\,\omega\,C_{gs}\,C\sqrt{P\,R} \tag{3.30}$$

where the correlation coefficient C is defined by:

$$C = \jmath \frac{\frac{d}{df}\langle i_g i_d^* \rangle}{\sqrt{\frac{d}{df}\langle i_g i_g^* \rangle \frac{d}{df}\langle i_d i_d^* \rangle}} \tag{3.31}$$

As is the case for the other two coefficients, P and R, C is a function of the technological parameters, the bias conditions and the device geometry. In the model the cross-correlation spectral density is purely imaginary since it results from the capacitive coupling of the gate circuit with the drain circuit noise sources.

The noise model, as it stands, can be further enhanced to account for flicker noise [56, 61], the generation-recombination noise linked to the existence of traps in the semiconductor forbidden band [56, 62] and the noise due to the gate leakage current [58, 59, 56, 62]. However, these effects become dominant at low frequencies only where no noise data is available for the foundry MESFETs. Consequently, no attempt was made to include these phenomena in the noise modelling of the devices.

Since first introduced by Van der Ziel [58, 59], the noise coefficients P, R and C have been estimated from physical device modelling and used, together with the above described model, to predict the device noise parameters F_{min}, Y_{opt} and R_n. However, only recently has the problem of obtaining the values of the noise coefficients from experimental measurements started to be considered [62, 63, 64, 65, 66, 67]. Since equations (3.28), (3.29) and (3.30) fully determine the frequency dependence of the intrinsic device noise sources, if the power and cross-correlation spectral densities of the intrinsic FET can be found from experimental data, at least at one measurement frequency f, then the values of P, R and C can be obtained from the inversion of these equations. They are given by

$$P = \frac{1}{2\,k\,\theta\,g_{mo}} \frac{d}{df}\langle i_d i_d^* \rangle \tag{3.32}$$

$$R = \frac{g_{mo}}{2\,k\,\theta\,(\omega\,C_{gs})^2} \frac{d}{df}\langle i_g i_g^* \rangle \tag{3.33}$$

$$C = \frac{1}{\jmath\,2\,k\,\theta\,\omega\,C_{gs}\sqrt{P\,R}} \frac{d}{df}\langle i_g i_d^* \rangle \tag{3.34}$$

where, in this case, the power and cross-correlation spectral densities represent measured values. The experimentally obtained values of the noise coefficients can then be used in equations (3.28), (3.29) and (3.30), to predict the intrinsic device noise behaviour over the entire frequency range where the noise phenomena accounted for in the model are

dominant. If the effects of the extrinsic device are then allowed for, a full characterisation of the FET can be obtained. The remaining problem is then to obtain the magnitude of the intrinsic noise sources at the measurement frequencies. This can be done using a de-embedding technique where the influence of the extrinsic FET is removed from the experimental data. Before the de-embedding technique and procedures are discussed the noise analysis method that will serve as its basis will be reviewed.

3.3.2 Noise analysis

The noise analysis method to be used is the correlation matrix method proposed by Hilbrand and Russer [68]. In this analysis the noisy two-port network is seen as an interconnection of more basic two-ports whose noise behaviour is known. Although more general methods are available [64, 67, 66], the types of network discussed in this thesis can be generally considered as two-ports. Also, the Hilbrand and Russer method can be simply and efficiently used for computer-aided noise analysis.

To describe a two-port network as the interconnection of more basic two-ports the following operations need to be effected [69]: series connection, parallel connection and cascade connection. If the admittance, impedance and chain matrix representations are chosen to describe the linear two-ports then, in the appropriate representation, each of these connections corresponds to a simple matrix operation. That is, if two two-port networks $\mathbf{N}_1$ and $\mathbf{N}_2$ are to be interconnected to form the two-port network $\mathbf{N}$, then the matrix describing the resulting two-port is obtained by [69]

$$\text{Parallel:} \quad \mathbf{Y} = \mathbf{Y}_1 + \mathbf{Y}_2 \tag{3.35}$$

$$\text{Series:} \quad \mathbf{Z} = \mathbf{Z}_1 + \mathbf{Z}_2 \tag{3.36}$$

$$\text{Cascade:} \quad \mathbf{C} = \mathbf{C}_1 \mathbf{C}_2 \tag{3.37}$$

where $\mathbf{Y}$, $\mathbf{Z}$ and $\mathbf{C}$ represent the two-port matrices in the admittance, impedance and chain representations respectively and the subscripts 1 and 2 refer to the two-ports to be connected[1]. The different representations can be easily converted one to another [70] so that the mathematical operation corresponding to the desired interconnection is implemented in the more convenient representation.

[1]In the chain representation $\mathbf{N}_1$ and $\mathbf{N}_2$ correspond to the input and output networks, respectively.

Additionally, any noisy linear two-port can be replaced by a noise equivalent circuit that consists of the original two-port, now assumed to be noiseless, and two additional noise sources [54, 55]. This is shown in figure 3.16 for the three representations considered. The noisy network is then represented by its linear two-port matrix (**Y**, **Z** or **C**) and its

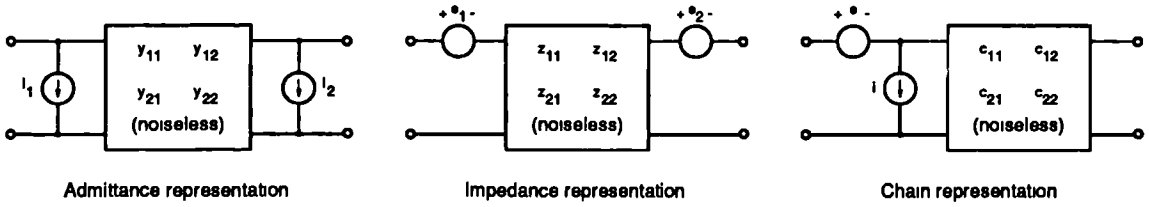

Figure 3.16: Two-port noise models

correlation matrix ($\mathbf{C}_Y$, $\mathbf{C}_Z$ or $\mathbf{C}_C$) whose elements are the power and cross-correlation spectral densities of the equivalent noise sources and are defined as:

$$\mathbf{C}_Y = \begin{bmatrix} \frac{d}{df}\langle i_1 i_1^* \rangle & \frac{d}{df}\langle i_1 i_2^* \rangle \\ \frac{d}{df}\langle i_1^* i_2 \rangle & \frac{d}{df}\langle i_2 i_2^* \rangle \end{bmatrix} \tag{3.38}$$

$$\mathbf{C}_Z = \begin{bmatrix} \frac{d}{df}\langle e_1 e_1^* \rangle & \frac{d}{df}\langle e_1 e_2^* \rangle \\ \frac{d}{df}\langle e_1^* e_2 \rangle & \frac{d}{df}\langle e_2 e_2^* \rangle \end{bmatrix} \tag{3.39}$$

$$\mathbf{C}_C = \begin{bmatrix} \frac{d}{df}\langle e\, e^* \rangle & \frac{d}{df}\langle e\, i^* \rangle \\ \frac{d}{df}\langle e^* i \rangle & \frac{d}{df}\langle i\, i^* \rangle \end{bmatrix} \tag{3.40}$$

If the noisy networks $\mathbf{N}_1$ and $\mathbf{N}_2$ are interconnected to form the two-port network **N**, their correlation matrices must be combined as [68]:

$$\text{Parallel:} \quad \mathbf{C}_Y = \mathbf{C}_{Y1} + \mathbf{C}_{Y2} \tag{3.41}$$

$$\text{Series:} \quad \mathbf{C}_Z = \mathbf{C}_{Z1} + \mathbf{C}_{Z2} \tag{3.42}$$

$$\text{Cascade:} \quad \mathbf{C}_C = \mathbf{C}_{C1} + \mathbf{C}_1\, \mathbf{C}_{C2}\, \mathbf{C}_1^\dagger \tag{3.43}$$

where † denotes Hermitian conjugation.

Finally, conversion between representations for the correlation matrices are given by the transformation

$$\mathbf{C}_R = \mathbf{T}\, \mathbf{C}_O\, \mathbf{T}^\dagger \tag{3.44}$$

where $\mathbf{C}_O$ and $\mathbf{C}_R$ denote the correlation matrix of the original and resulting representation, respectively and **T** is the transformation matrix between the two representations. This

matrix is given in table 3.1 for transformations between the admittance, impedance and chain representations [68].

resulting representation	original representation		
	Y	Z	C
Y	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$	$\begin{bmatrix} -y_{11} & 1 \\ -y_{21} & 0 \end{bmatrix}$
Z	$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$	$\begin{bmatrix} 1 & -z_{11} \\ 0 & -z_{21} \end{bmatrix}$
C	$\begin{bmatrix} 0 & c_{12} \\ 1 & c_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -c_{11} \\ 0 & c_{21} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Table 3.1: Transformation matrices

3.3.3 Noise de-embedding

The noise de-embedding problem can now be solved. It involves the determination of the correlation matrix of the embedded network $\mathbf{N}_2$ (or $\mathbf{N}_1$) when the correlation matrices of the composite network $\mathbf{N}$ and of the embedding network $\mathbf{N}_1$ (or $\mathbf{N}_2$) are known. This can be done by inverting equations (3.35), (3.36), (3.37), (3.41), (3.42) and (3.43):

$$\text{Parallel:} \quad \begin{cases} \mathbf{Y}_2 = \mathbf{Y} - \mathbf{Y}_1 \\ \mathbf{Y}_1 = \mathbf{Y} - \mathbf{Y}_2 \end{cases} \qquad \begin{cases} \mathbf{C}_{Y2} = \mathbf{C}_Y - \mathbf{C}_{Y1} \\ \mathbf{C}_{Y1} = \mathbf{C}_Y - \mathbf{C}_{Y2} \end{cases} \tag{3.45}$$

$$\text{Series:} \quad \begin{cases} \mathbf{Z}_2 = \mathbf{Z} - \mathbf{Z}_1 \\ \mathbf{Z}_1 = \mathbf{Z} - \mathbf{Z}_2 \end{cases} \qquad \begin{cases} \mathbf{C}_{Z2} = \mathbf{C}_Z - \mathbf{C}_{Z1} \\ \mathbf{C}_{Z1} = \mathbf{C}_Z - \mathbf{C}_{Z2} \end{cases} \tag{3.46}$$

$$\text{Cascade:} \quad \begin{cases} \mathbf{C}_2 = \mathbf{C}_1^{-1}\,\mathbf{C} \\ \mathbf{C}_1 = \mathbf{C}\,\mathbf{C}_2^{-1} \end{cases} \qquad \begin{cases} \mathbf{C}_{C2} = \mathbf{C}_1^{-1}\,(\mathbf{C}_C - \mathbf{C}_{C1})\,\mathbf{C}_1^{\dagger\,-1} \\ \mathbf{C}_{C1} = \mathbf{C}_C - \mathbf{C}_1\,\mathbf{C}_{Z2}\,\mathbf{C}_1^{\dagger} \end{cases} \tag{3.47}$$

The remaining problem is now to determine the correlation matrices of the composite and embedding networks. The correlation matrix of the total two-port in the chain representation can be calculated from the measured values of the noise parameters F_{min}, Y_{opt} and R_n as

$$\mathbf{C}_C = 2\,k\,\theta_0 \begin{bmatrix} R_n & \frac{(F_{min}-1)}{2} - R_n Y_{opt} \\ \frac{(F_{min}-1)}{2} - R_n Y_{opt}^* & R_n \mid Y_{opt} \mid^2 \end{bmatrix} \tag{3.48}$$

where θ_0 is the standard reference temperature of the input termination (290 K). The correlation matrix of the embedding network can, in principle, be obtained by the same process [67]. However, the embedding network is normally not accessible for direct measurement. In this case, if the equivalent circuit is known, consists only of passive elements and is reciprocal then the correlation matrix can be obtained in the admittance or impedance representations as

$$\mathbf{C}_Y = 2k\theta\,\mathrm{Re}(\mathbf{Y}) \tag{3.49}$$

$$\mathbf{C}_Z = 2k\theta\,\mathrm{Re}(\mathbf{Z}) \tag{3.50}$$

This means that for a passive network knowledge of the equivalent circuit and physical temperature is sufficient to obtain its correlation matrix.

Foundry FET noise de-embedding

At this stage, all the methodology to effect noise de-embedding has been developed. It will now be applied to obtain the values of the P, R, and C noise coefficients for the GaAs foundry standard cells. The steps involved in the de-embedding process are as follows:

1. Obtain the FET correlation matrix in the chain representation from the measured values of F_{min}, Y_{opt} and R_n using (3.48).

2. From the measured s-parameters obtain the FET Z-matrix, or alternatively evaluate it using the FET equivalent circuit.

3. Form the Y-matrix of the gate and drain extrinsic impedances and using (3.49) obtain their correlation matrix in the admittance representation. Using (3.44) transform the result into the chain representation.

4. Form the Z-matrix of the source impedance and using (3.50) obtain the correlation matrix in the impedance representation.

5. De-embed from the source extrinsic impedance using (3.46) and transform the result in the chain representation (3.44).

6. Using (3.47) de-embed from the gate impedance and then from the drain impedance.

7. Convert the last result into the admittance representation. At this stage the de-embedded network consists of the intrinsic device plus C_{ds}. Although C_{ds} and C_{dg} are not part of the intrinsic noise model (figure 3.15), de-embedding from these components is not necessary since the magnitude of the intrinsic correlation matrix in the admittance representation is not affected by the presence of C_{ds} and C_{dg}.

8. The de-embedding process is now complete. The noise coefficients P, R, and C are then calculated from equations (3.32), (3.33) and (3.34), respectively, using the experimentally determined values for the power and cross-correlation spectral densities and the measurement frequency. If the de-embedding process is done at more than one frequency, then an average of the extracted noise coefficients should be effected to reduce the effects of measurement noise and of experimental errors.

The extracted values of the noise coefficients P, R and C can now be used in the FET noise model to predict the device noise behaviour at any frequency falling within the range of validity of the model.

3.3.4 Results and method validation

Using the noise de-embedding technique described above, the values of the noise coefficients P, R and C were obtained for the foundry standard FET cells biased for low noise operation. The measured values of the noise parameters F_{min}, Y_{out} and R_n, used in the de-embedding process were obtained from data supplied by the manufacturer at 10 equally spaced frequencys points between 2 and 20 GHz. Since no set of measured s-parameters was available from the manufacturer, the device Z-matrix was evaluated from the MESFET small signal equivalent circuit. The noise coefficients were extracted for each device at the 10 measurement frequencies and the mean value of each coefficient was determined and employed. The de-embedded P, R and C values are given in table 3.2 for the foundry standard MESFET cells.

MESFET	P	σ_P	R	σ_R	C	σ_C
2×100	1.184	0.018	0.162	0.035	0.751	0.015
4×75	1.153	0.030	0.147	0.032	0.775	0.026
4×150	1.178	0.011	0.170	0.036	0.863	0.026
6×50	1.154	0.012	0.146	0.021	0.775	0.055

Table 3.2: P, R and C values and standard deviation for the foundry MESFETs

Figure 3.17 represents the frequency behaviour of the de-embedded correlation matrix for the 4 × 150 MESFET obtained at step 7 of the de-embedding process described above. From this figure it can be seen that the de-embedded device displays a noise behaviour very close to that predicted for the intrinsic device by equations (3.29), (3.30) and (3.28). The gate noise power spectral density (S_{gg} in figure 3.17) has an almost ideal parabolic frequency behaviour, while the drain noise power spectral density (S_{dd} in figure 3.17) deviates less than 2% from a white power spectrum. The imaginary part of the cross-correlation spectral density (Mag(S_{gd}) in figure 3.17) is almost perfectly linear, as predicted by equation (3.30) but, as can be seen from the figure the phase of the de-embedded cross-correlation spectral density differs from the ideal 90 degree value. However, this difference is at maximum 8% over all the frequency range.

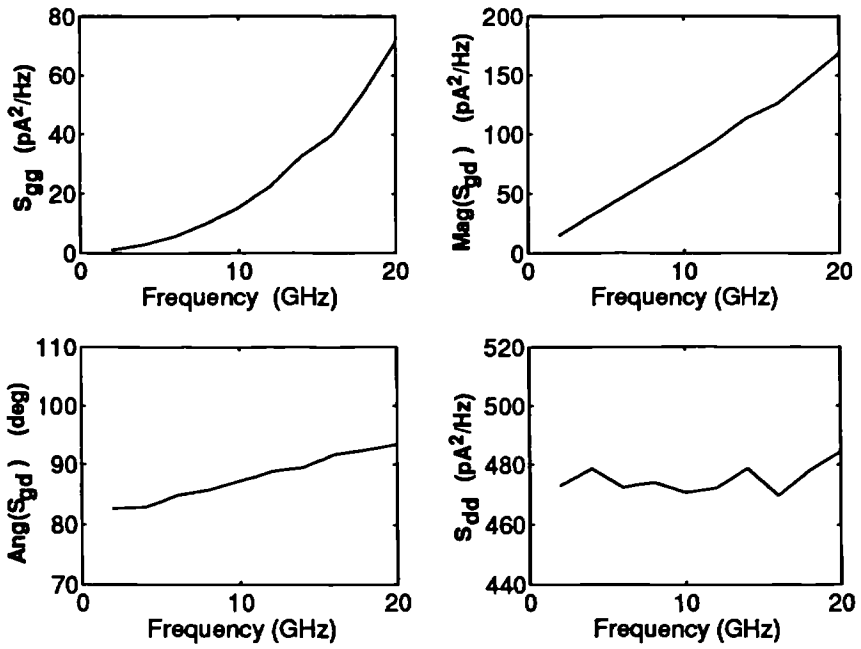

Figure 3.17: Frequency behaviour of the C_Y-matrix elements for the 4 × 150 intrinsic MESFET

For the other three devices the de-embedded correlation matrix displayed also nearly ideal frequency behaviour.

The de-embedded values of the noise coefficients are shown in figures 3.18 and 3.19 for the 4 × 150 and the 2 × 100 MESFETs, respectively. Also represented in the figures are the mean values of the three noise coefficients. From these figures the noise coefficients are seen, as expected, to be practically independent of frequency over the measurement

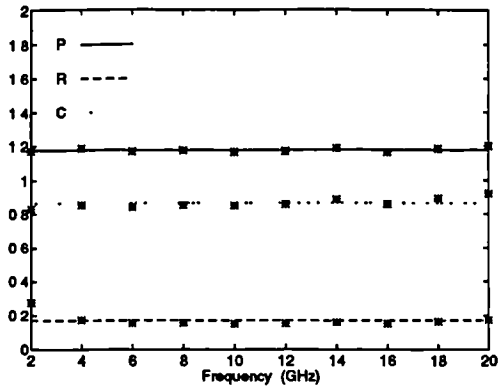

Figure 3.18: De-embedded P, R, and C values for the 4×150 MESFET

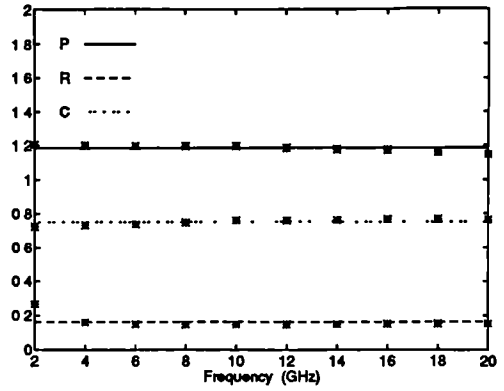

Figure 3.19: De-embedded P, R, and C values for the 2×100 MESFET

frequency range.

Finally, figures 3.20 and 3.21 compare the measured values of the noise parameters NF_{min}, $\mathrm{Re}(Y_{opt})$, $\mathrm{Im}(Y_{opt})$ and the normalised value of R_n for both MESFETs with the values obtained from simulation using the adopted noise model and the de-embedded values of P, R and C. These figures show very good agreement between the simulation and measured parameters, thus validating both the adopted MESFET noise model and the noise de-embedding technique.

3.4 MATLAB Toolbox: Circuit Analysis

A circuit analysis toolbox was written for use with the numerical analysis program MATLAB [71]. The toolbox uses the MATLAB matrix functions to provide a specialised set of circuit analysis functions. It consists of a collection of algorithms, expressed as MATLAB files, which implement all the mathematical functions necessary for the noise and frequency response numerical analysis of two-port networks of arbitrary complexity. The toolbox includes:

- signal and noise interconnection functions;
- signal and noise de-embedding functions;
- two-port ideal passive and active element models;
- two-port GaAs foundry passive and active device models;

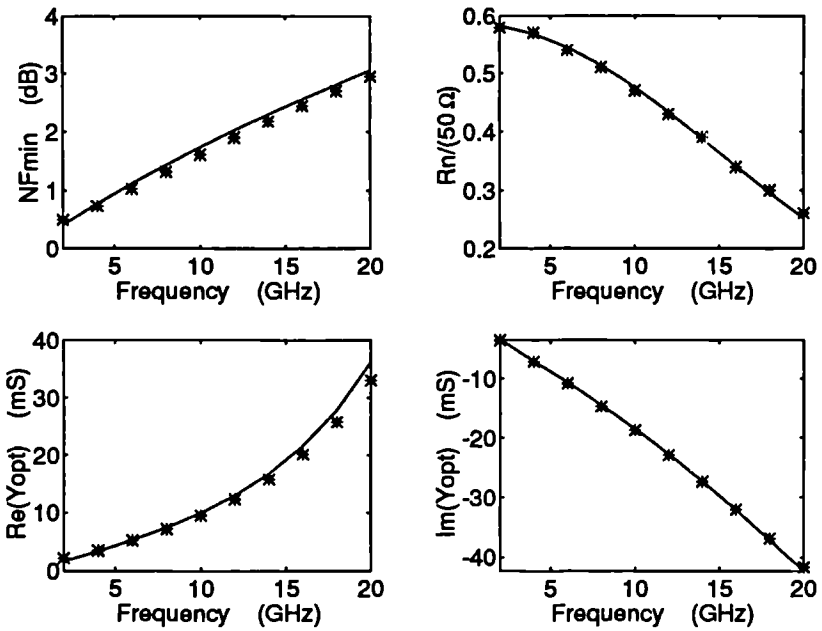

Figure 3.20: Measured ('*') and predicted ('—') noise parameters for the 4×150 MESFET

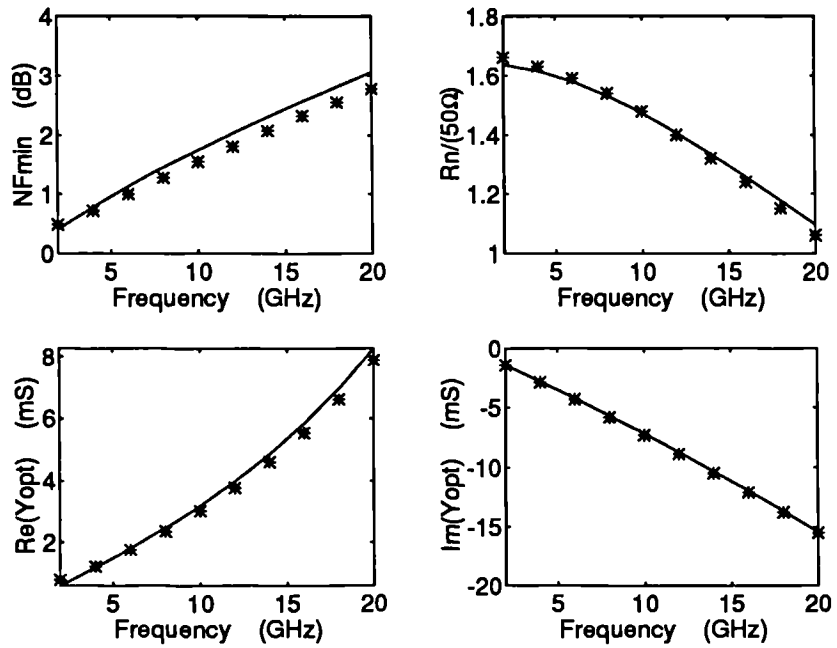

Figure 3.21: Measured ('*') and predicted ('—') noise parameters for the 2×100 MESFET

- P, R and C noise de-embedding routine;
- general utility functions.

A short description of the circuit analysis toolbox functions is given in appendix C.

The toolbox was successfully used to effect the noise de-embedding process discussed in this chapter. It was also used for the time domain optimisation of post detection pulse shaping filters as well as for the noise optimisation of an analogue noise-tuned optical receiver. These will be discussed in the following chapters.

3.5 Summary

In this chapter the GaAs MMIC process used in the practical implementations to be discussed later in this thesis was described. A brief description of the main features of the process, the physical layout of the foundry passive and active devices, their equivalent circuit models and model limitations has been provided. The derived chain matrix for each of the GaAs foundry passive components was also given.

Noise modelling of the foundry active devices (MESFETs) was considered in detail. Noise data provided by the manufacturer was used to determine three noise coefficients that, together with the small signal equivalent model, allow full characterisation of the noise behaviour of the active devices. The adopted noise model was discussed and its noise coefficients obtained for the standard foundry MESFET cells. A two-port network noise analysis technique was reviewed that served as the basis for the noise de-embedding method used in the determination of the MESFET's noise coefficients P, R and C. The de-embedding procedure used for the foundry MESFETs was detailed and the obtained values of the noise coefficients given. The adopted noise model and the de-embedding procedure were then validated by comparing the simulated noise parameters F_{min}, Y_{opt} and R_n with the experimental data provided by the manufacturer.

In the next chapter the potential of the GaAs technology for the realisation of the signal shaping strategies developed in the previous chapter will be assessed. This will be done by realising both passive and active structures that implement the pulse shaping strategies of chapter 3 and are suitable for optical communication systems operating in the Gbit/s region.

Chapter 4

Pseudo-lumped-element GaAs receivers for binary signalling

This chapter discusses the practical implementation of the signal processing strategies proposed in chapter 2 for the realisation of jitter tolerant optical receivers and also the realisation of optical receivers tolerant to input circuit parasitics. The proposed designs were implemented as MMICs using the GaAs foundry process described in the previous chapter. Three designs are presented. The first one to be discussed is an optical receiver designed to operate at 4.8 Gbit/s with 50% return-to-zero (RZ) pulses. The receiver integrates both the linear amplification and the signal shaping functions that are usually shared between the amplifier and the post-detection filter. The receiver filtering function was derived using the MCB optimisation technique described in section 2.4 and provides optimum signal shaping for use with APD photodiodes [72, 73]. This design clearly illustrates the practical viability of the signal shaping techniques proposed in chapter 2 and it will serve to assess the GaAs foundry potential and limitations for the realisation of high-speed optical receivers. The potential advantages of embedded signal shaping may, however, not be achieved in practice due to the tolerance with which a pre-specified transfer function can be achieved. For an integrated receiver this tolerance is essentially associated with the receiver input circuit and depends on factors such as photodiode capacitance, bond-wire inductance and mounting stray capacitance. The second design proposed is considered to mitigate this problem by using a low input impedance front-end stage. The receiver operates at 5 Gbit/s and was conceived as a true transimpedance design using a common-gate (CG) front-end stage to achieve a high degree of insensitivity to input parasitics [74, 75, 76].

The last design discussed explores the use of passive post-detection filters implemented as GaAs MMICs to effect the pulse shaping proposed in section 2.3. This design extends

the useful frequency range of the GaAs technology for signal shaping beyond the capability of active circuits and pulse shaping filters for 10 Gbit/s and 15 Gbit/s operation are demonstrated [77]. For the purpose of accurate design of GaAs post-detection filters, a time domain optimisation technique was developed [78, 79]. The technique allows for the inclusion of process degeneracies associated with the quasi-lumped nature of the GaAs foundry devices and overcomes some of the limitations of commercially available computer aided design (CAD) tools.

4.1 GaAs receiver with embedded signal shaping

In this section the design, optimisation and performance of a GaAs integrated optical receiver will be discussed. The objective is to design an avalanche photodiode (APD) receiver based on the MCB optimisation strategy [46, 47]. The receiver is optimised to operate at 4.8 Gbit/s with RZ pulses and incorporates the required signal shaping to secure optimal noise filtering and jitter tolerance. Of course useful signal gain and good output matching to 50 Ω is also required.

The main feature of the design is the integration of the pulse shaping function in the preamplifier itself. This has some advantages over the traditional physical splitting between linear amplification and the equalisation or filtering functions [80] since it minimises the number of system components. This, consequently reduces the number of circuit interconnections which can be translated into a reduction of production and packaging costs, improved circuit repeatability and increased system reliability.

Physically, the integration of the amplification and filtering functions in the same MMIC can be made in two fundamentally different ways. In a first approach, the preamplifier is followed by a pulse shaping filter with both functional blocks integrated on the same chip. This approach retains all the integration advantages mentioned above but adds complexity to the design. However, the traditional method of receiver design requires either the presence of an equaliser before the pulse shaping filter to correct for the preamplifier frequency response or, alternatively, the use of a preamplifier with excess-bandwidth so that the overall receiver response is virtually independent of the preamplifier response. This may result in a noise penalty. In a second approach the preamplifier response is tailored to match the response of the required filtering transfer function. This approach has the advantage of simplicity over the first one and was selected for the realisation of the

APD receiver being considered here.

4.1.1 Receiver target response

The MCB based optimisation method could, in principle, be directly used to obtain the optimum receiver. The optimisation would involve the selection of an appropriate preamplifier structure with some of the circuit parameters taken as optimisation variables. The actual receiver impulse response would then be directly used in equation (2.65) to evaluate the MCB. An iterative procedure could then arrive to the optimum solution for a given circuit topology and a given set of optimisation variables. Such an optimisation process would require the efficient evaluation of the receiver noise and impulse response as well as the capability to evaluate and use the MCB as the cost function to control the optimisation algorithm. Such a combination of factors is not provided by present day CAD tools and an alternative route had to be followed for the design and optimisation of the receiver using the MCB criteria.

In reference [48] O'Reilly *et al* showed that receiver filters realised as L-C ladder networks can be optimised using the MCB formulation to provide a receiver performance approaching the strict optimum established using variational calculus techniques. Furthermore, it is shown that in practice simple third order networks yield a performance that is close to the optimum. This suggests that an MCB optimised receiver can be obtained if its impulse response can be made to match that of an adequately optimised L-C ladder network. The third order lumped element network represented in figure 4.1 was obtained using an MCB based optimisation technique [48, 50] for the set of design parameters given in table 4.1 and it was used to define the receiver target response. The corresponding

Bit rate	4.8 Gbit/s
Input pulse	Gaussian
Jitter range	15% of T
APD gain	10
APD ionisation coefficient	0.3
Noise spectral density	$10\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$

Table 4.1: Receiver design parameters

eye-diagram is shown in figure 4.2. This network was used as the basis for the preamplifier design. It should be noted that no attempt was made to evaluate or include in the optimisation the 'true' receiver noise; instead a white noise spectrum was assumed. However,

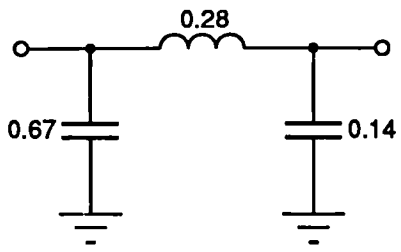

Figure 4.1: MCB optimised filter, ref. [50]

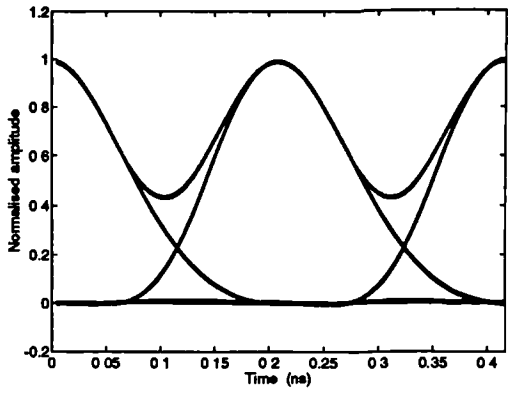

Figure 4.2: Receiver target eye-diagram

coloured noise can easily be included in the optimisation as discussed in reference [81].

4.1.2 Receiver design

The adopted circuit topology is shown in figure 4.3. The design consists of three stages where each stage is based on the $4 \times 75\,\mu$m foundry FET which, for this design, offered a good compromise between gain and bandwidth. The front-end stage is a transimpedance stage (TZ) using an FET in a common source configuration with voltage-shunt feedback.

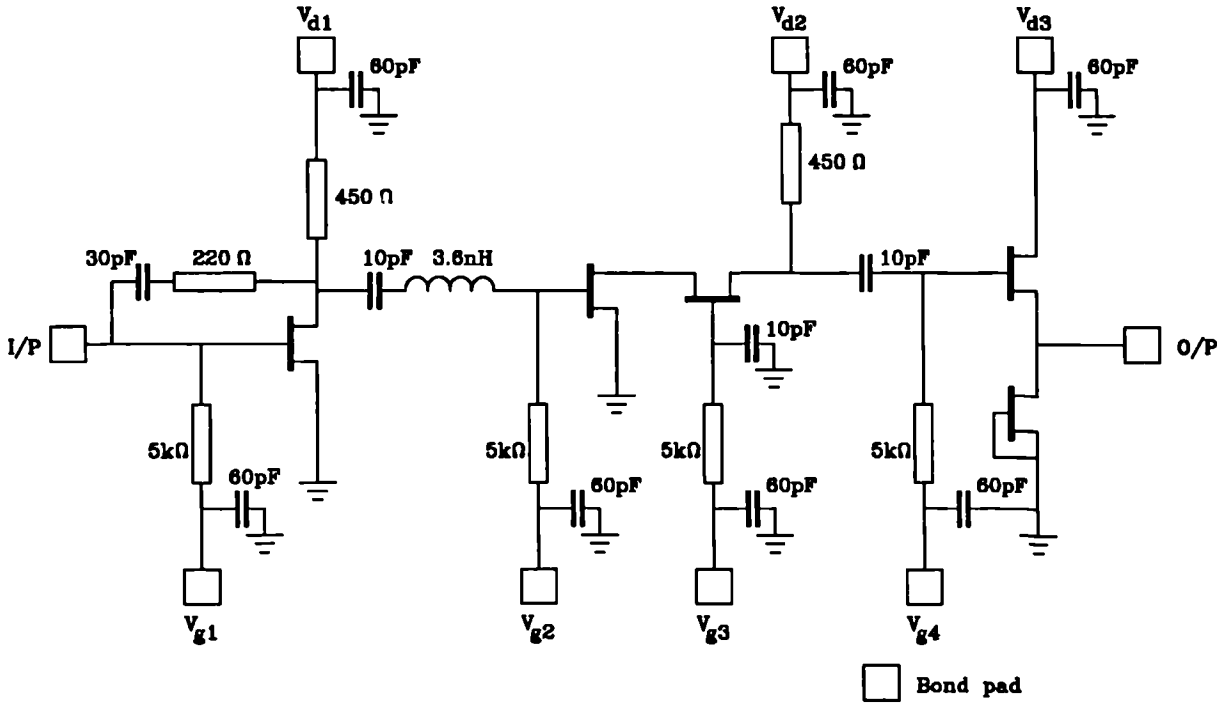

Figure 4.3: Optical receiver schematic diagram

A low value of the feedback resistor (220 Ω) was selected to achieve wideband operation of the first stage and ensure a low input impedance, securing a final optimised response that is not unduly compromised by variations in the photodiode capacitance and bond-wire inductance. The input stage is followed by a cascode gain stage that provides a voltage gain of nearly 10 and a series inductor is used between the two first stages. This inductor, together with the combined effects of shunt capacitances of the FETs and passives, on its two terminals, acts as a third order low pass filter and facilitates the matching of the receiver response with that of the target filter response. The final stage is a source follower with an active load selected to provide an output impedance close to 50 Ω, resulting in a VSWR better than 1.9:1 over the range of operation. The final stage voltage gain is ≈ 0.5 and so the total receiver transimpedance is close to 60 dBΩ. The area occupied by the receiver on GaAs is 2×3 mm and a photomicrograph of the receiver is shown in figure 4.4.

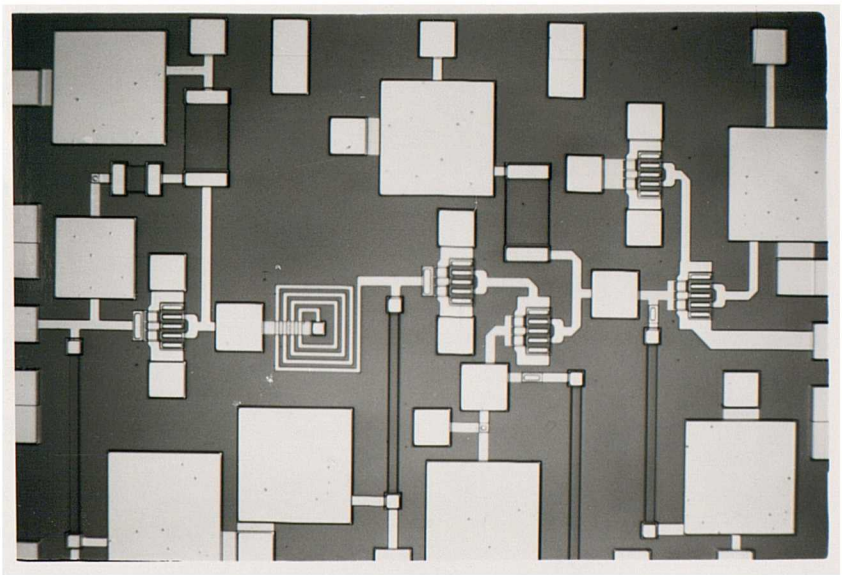

Figure 4.4: Receiver photomicrograph

4.1.3 Optimisation and simulation results

As discussed before, the design goal is to obtain an MMIC receiver circuit that emulates as closely as possible the impulse response of the MCB optimised L-C ideal filter. For the proposed design this was achieved by the optimisation of the values of the feedback resistance, the first and second stage drain resistances, the coupling inductor between the

first and second stages and the FETs bias currents.

Due to the nature of the problem, the optimisation process is best done in the time domain. However, no commercial microwave CAD tools were available to provide a time domain optimisation facility. Therefore, the MMIC design was optimised in the frequency domain[1]. From the description of the GaAs foundry components and associated circuit models, examined in the previous chapter, it is to be expected that the receiver performance will depend on the actual MMIC layout. Thus, the optimisation consists in an iterative process between optimisation of component values (dimensions) and circuit layout. The adopted optimisation procedure can be described in four distinct stages:

1. In the first stage the circuit is modelled using detailed FET models but ideal passive elements are used and no layout information is included. This allows the feasibility of the design to be assessed and gives a first estimate of the GaAs passive component values.

2. Next, complete equivalent circuits for all passive devices are used and the circuit is tuned to accommodate their affect. Transitions to external circuits are also added at this stage.

3. A detailed GaAs layout is now produced with the lengths of critical transmission lines in the circuit extracted from the MMIC layout. Their affect is included in the circuit modelling.

4. The circuit is again tuned to compensate for the affect of the layout.

Some iteration is required for the last two optimisation stages since new component values (dimensions) lead to a different layout and conversely a new layout may lead to new component values. In spite of that, the execution of the first two optimisation stages ensures that the interaction between the final two optimisation stages is small and convergence is rapidly achieved.

Figure 4.5 shows the final frequency response of the MMIC (solid line) and compares it to the response of the ideal target (broken and dotted line). Also shown in the figure is the receiver response at the first stage of the optimisation p ocess (broken line). This

[1]A time domain optimisation technique for the optimisation of post-detection GaAs filters will be considered later in this chapter.

figure clearly reveals the impact that the non-ideal behaviour of the GaAs passive components, the transmission lines and the interface components have on the receiver response. This degradation due to circuit 'non-ideal' behaviour becomes increasingly important with higher frequency operation. Thus any optimisation method, to be successful, must account for these factors as thoroughly as possible.

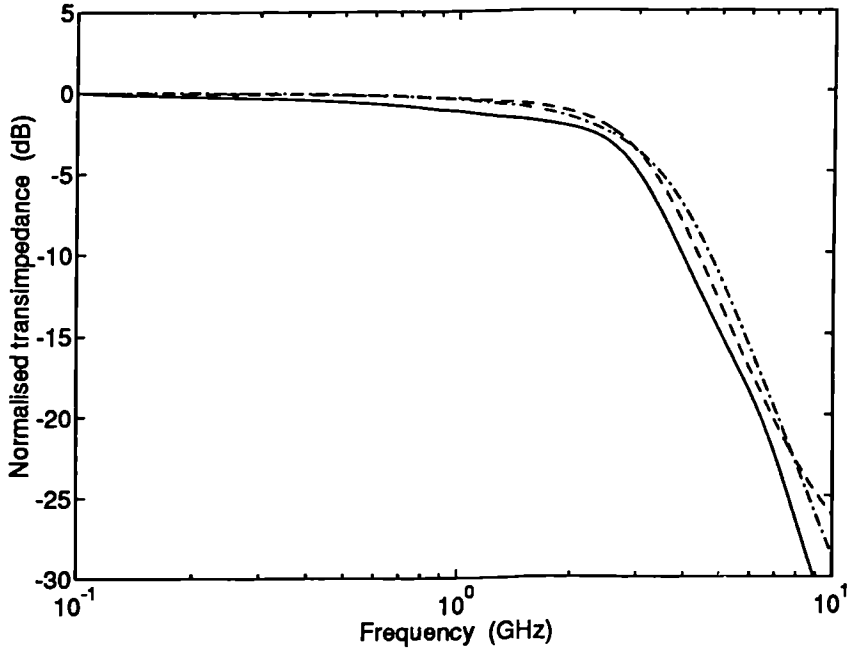

Figure 4.5: Receiver frequency response: '———' final MMIC; '– · –' with ideal passives; '– – –' target

The MMIC was optimised assuming a photodiode capacitance (C_d) of 0.3 pF and a bond-wire inductance (L_{bw}) of 1 nH. Figure 4.6 shows the simulated eye-diagram using these values. When compared with the eye-diagram of the ideal L-C filter it displays 16% of eye-closure, at the optimum sampling point, resulting in approximately 0.8 dB of optical power penalty due to intersymbol interference. In spite of that, the eye still exhibits the general features of the target (figure 4.2), namely depressed signal crossings and low slope ISI, at the optimum sampling instant, assuring tolerance to jitter and sampling errors.

Spread in component values can affect the receiver response and consequently its pulse shaping function. For the GaAs foundry components tolerance is typically less than 10%. In contrast, the photodiode capacitance and bond wire inductance can vary by as much as 100%; consequently, these will be the main factors affecting the receiver response. Figure

4.7 shows the receiver eye-diagram when the photodiode capacitance is increased to 0.5 pF maintaining the bond-wire inductance value. The eye now displays 22% of eye-closure, corresponding to about 1.1 dB in optical power penalty, this being almost entirely due to an increase in the eye diagram skew. Besides eye-closure, skew in the eye-diagram will also reduce the tolerance to timing errors and jitter and thus must be avoided. To reduce the sensitivity to photodiode capacitance and bond-wire inductance the receiver input impedance must be reduced. For a transimpedance design this is achieved using a low value of the feedback resistance which can mean the use of excessive amounts of feedback, compromising the receiver gain, stability and noise. In the next section, the use of the common-gate configuration for the front-end stage will be proposed as a way to realise receivers with intrinsic low input impedance and with a high degree of insensitivity to photodiode parasitics.

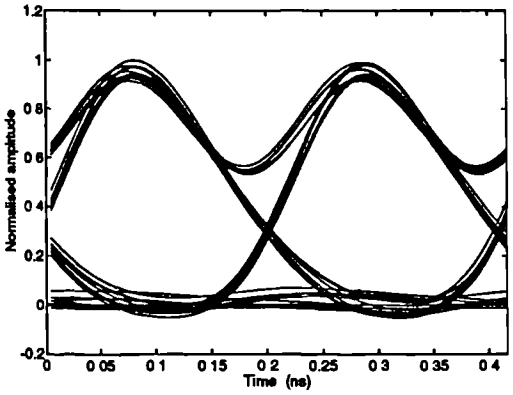

Figure 4.6: Eye-diagram $C_d = 0.3\,\text{pF}$ and $L_{bw} = 1\,\text{nH}$

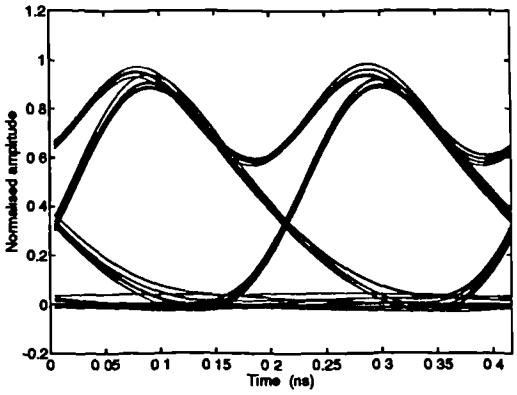

Figure 4.7: Eye-diagram $C_d = 0.5\,\text{pF}$ and $L_{bw} = 1\,\text{nH}$

4.2 Common-gate optical receivers

As shown in the previous section, signal shaping networks can be critically affected by circuit sensitivity to parameters that are difficult to control and predict. For an integrated optical receiver preamplifier such parameters are mainly associated with the receiver input circuit and are the photodiode capacitance, the bondwire inductance and the mounting parasitic capacitance. To deal with this problem two solutions can be adopted. In the first one, a preamplifier with excess bandwidth is used followed by a post-detection filter that effects the desired signal shaping function. The preamplifier bandwidth must be high

enough so that the predicted worst case −3 dB frequency is higher than the maximum frequency of interest, resulting in an overall receiver response that is virtually independent of the preamplifier response. This approach is obviously incompatible with embedding of the signal shaping in the preamplifier and is technologically difficult to implement since high bit rate receivers already operate close to the speed limits of present day semiconductor technologies. The second solution is to use a preamplifier front-end circuit configuration that renders the overall receiver tolerant to the input circuit parasitics. Circuit topologies that have an intrinsically low input impedance can be used as the first stage of an optical receiver to achieve some degree of insensitivity to photodiode and assembly parasitics. From this viewpoint the useful transistor configurations are the common-base (CB) for bipolar circuits and the common-gate (CG) for FET circuits. Optical receivers that use the CB configuration as the input stage have been proposed in the past [82, 83, 84, 85]. The proposed designs used the CB configuration either as a first stage in a transimpedance optical receiver [83] or simply as a low impedance input stage [82, 84, 85]. Here, a novel implementation of a low input impedance design realised as a GaAs MMIC employing a common-gate configuration as the first stage of a transimpedance receiver is demonstrated. The assembled receiver achieved 5 Gbit/s operation with an optical sensitivity better than −13 dBm. The low impedance front end solution — that is both compatible with the embedding of the signal shaping in the receiver or with the use of post-detection filters — will now be discussed.

4.2.1 Low input impedance receivers

The mechanism by which a low input impedance stage, like a CG stage, can provide increased tolerance to photodiode parasitics can be understood by considering the following argument: the usual CS configuration has an intrinsically high input resistance which, when combined with the photodiode capacitance, the mounting capacitance and the FET gate-to-source capacitance (G_{gs}) gives origin to a dominant pole that limits the bandwidth capability of the optical receiver. By using an input configuration with an intrinsically low input resistance this pole can be shifted up in frequency so that it is no longer dominant. In this case, variations in the input pole position, due to circuit uncertainties, will have only a moderate effect on the receiver bandwidth. Additionally, a transimpedance optical receiver can also be made to be more tolerant to photodiode and parasitic capacitances if a low input impedance first stage is used [83]. This can be understood with reference to the

simplified diagram of a transimpedance amplifier represented in figure 4.8. In this diagram the amplifier input impedance is the parallel combination of the resistance R_{in} and the capacitor C_{in} and the amplifier is assumed to have a frequency independent voltage gain A_v. The photodiode is modelled by the ideal current source I_p and the capacitance C_d.

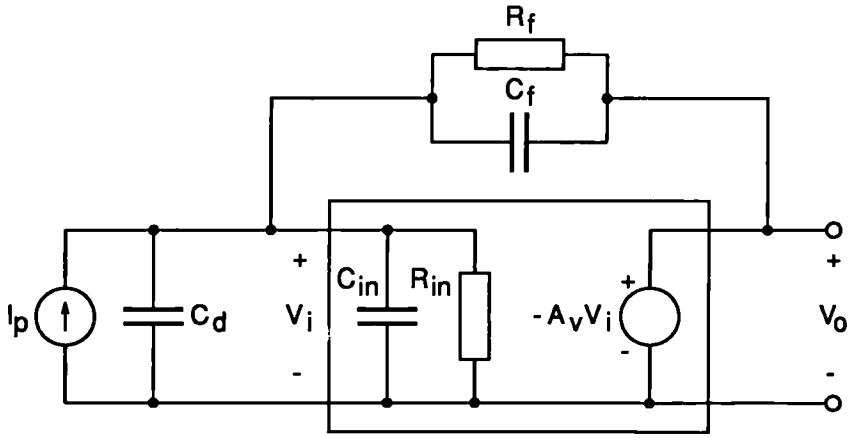

Figure 4.8: Transimpedance optical receiver model

The feedback impedance is represented as the parallel combination of the resistance R_f and the capacitance C_f. For this simplified model the close loop transimpedance $A_z(s)$ can be written as

$$A_z(s) = \frac{A_z(0)}{1 + s\left[C_f + \frac{R'_{in}}{A_{zo}}(C_d + C_f + C_{in})\right] A_z(0)} \tag{4.1}$$

where $A_z(0)$ is the midband closed loop transimpedance given by

$$A_z(0) = \frac{-A_{zo}}{1 + A_{zo}/R_f} \tag{4.2}$$

and $A_{zo} = R'_{in}\, A_v$ is the midband open loop transimpedance with R'_{in} the parallel combination of R_{in} and R_f.

In equation 4.1 the total input capacitance $C_d + C_f + C_{in}$ appears multiplied by the factor R'_{in}/A_{zo} and this shows that for two amplifiers with identical open-loop transimpedance gains, a lower input resistance — R'_{in} — will produce a frequency response that is much less sensitive to the total value of the input capacitance. Alternatively, since $R_{in}/A_{zo} = 1/A_v$ the amplifier voltage gain can be increased to desensitise the amplifier response from the total value of the input capacitance. However, this approach poses problems at microwave frequencies were the extra delay introduced by the additional gain stages required can

cause instability problems. Consequently, the low impedance approach is to be preferred at microwave frequencies.

Since a CG configuration can be made to have a low input impedance, it can be used as the first stage of a transimpedance optical receiver to reduce the circuit sensitivity to the total input capacitance. The low frequency input resistance of the common-gate configuration is given by

$$R_{in} = \frac{R_{ds} + R_L}{1 + g_{mo} R_{ds}} \tag{4.3}$$

where R_L is the load resistance of the CG stage. For the foundry MESFETs the product $g_{mo} R_{ds}$ takes values ranging from 7 to 13 depending on the type of device and on the operating conditions. For high values of $g_{mo} R_{ds}$ the input resistance can be approximated by

$$R_{in} \approx \frac{1}{g_{mo}} \left(1 + \frac{R_L}{R_{ds}}\right) \tag{4.4}$$

These equations show that it is possible to obtain a low input resistance with a CG stage when the real part of the load impedance is $< R_{ds}$. This situation contrasts with the case of bipolar transistors where the high value of the collector to emitter resistance makes the input resistance practically independent of the load and equal to $1/g_{mo}$ [86].

Finally, a noise penalty is to be expected when using a CG front-end [87]. This is due to the less than unity current gain of the CG stage resulting in the direct addition of the thermal noise of the first stage load and the second stage noise to the overall equivalent noise at the input of the preamplifier.

4.2.2 Receiver design

The schematic diagram of the GaAs MMIC common-gate receiver is shown in figure 4.9. The receiver is a three stage amplifier with two independent shunt-feedback loops. The first CG transistor is a $2 \times 100\,\mu$m MESFET biased at a drain current of 6 mA for low noise operation. The $2 \times 100\,\mu$m MESFET was selected for the CG input stage because it offers the highest values for the product $g_{mo} R_{ds}$ ($= 7.6$) of all the foundry standard cells when biased for low noise operation. For this FET it is thus possible to obtain a low input impedance even with a relatively high value of load resistance. The bias current of the first stage is supplied by V_{DD} and V_{SS} through the two $750\,\Omega$ drain and source resistors and can be adjusted by varying the gate voltage V_{GG}. The source bias resistor can also serve as a bias resistor for the photodiode. The output of the CG is AC-coupled to a

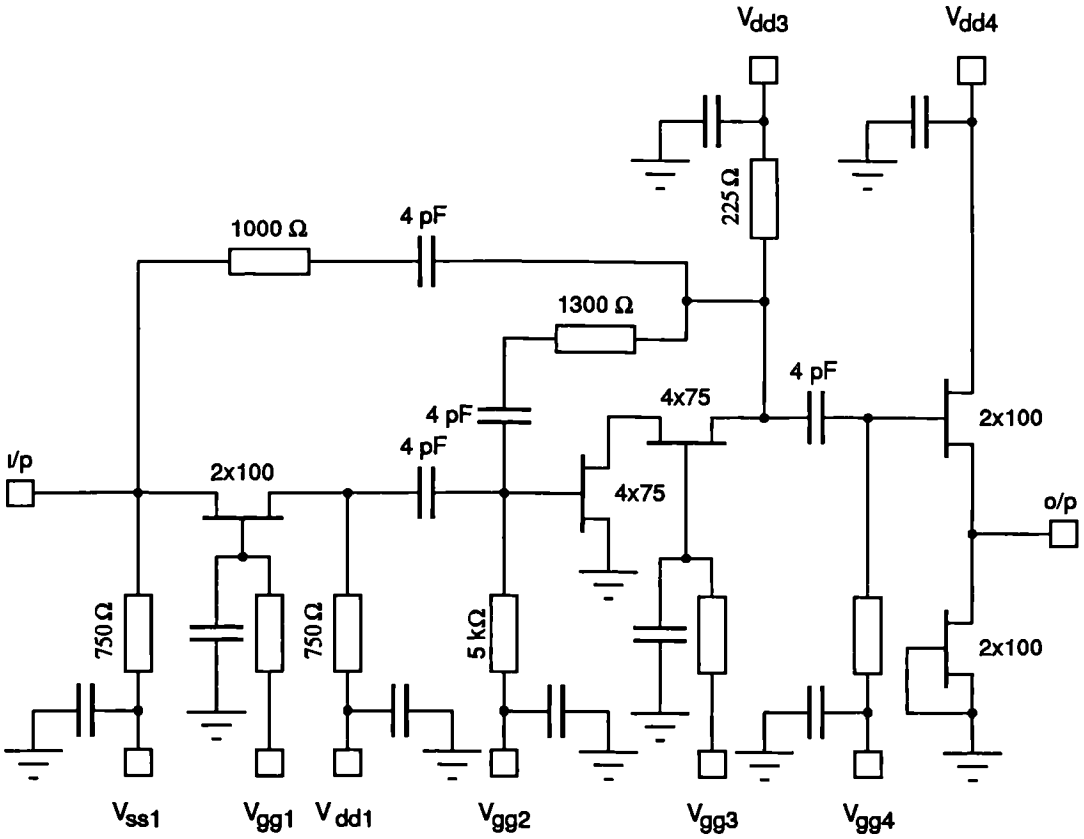

Figure 4.9: Common-gate optical receiver

cascode gain stage implemented using the higher transconductance $4 \times 75\,\mu$m MESFETs. Voltage-shunt feedback is used around this stage in order to provide a relatively low load impedance ($\leq R_{ds}$ of the first FET) for the common gate stage without incurring excessive noise penalty. The closed-loop input resistance of the cascode is $288\,\Omega$ providing the required loading of the CG stage to achieve an open-loop input resistance of $78\,\Omega$. The overall receiver feedback is voltage-shunt and is implemented using a series combination of a $1000\,\Omega$ resistor and a 4 pF capacitor, resulting in a closed-loop input resistance of $47.5\,\Omega$. Finally the output is an AC-coupled common-drain stage with an active source load. The output MESFETs are $2 \times 100\,\mu$m devices running at I_{DSS} and providing close to $50\,\Omega$ output impedance. Each of the three stages has its own independent bias arrangement to allow maximum operational flexibility.

A photomicrograph of the manufactured MMIC is shown in figure 4.10. The MMIC chip size is 2 mm×2 mm and was mounted on an alumina substrate with the associated chip decoupling capacitors. A chip InAlGaAs/InP top-entry $40\,\mu$m diameter PIN-photodiode, having external measured responsivity of 0.79 A/W and a capacitance close to 0.15 pF, was

bonded to the input of the receiver and optical power was launched into the PIN using a fibre cleaved at a 45 degrees angle. The whole receiver was then packaged and tested.

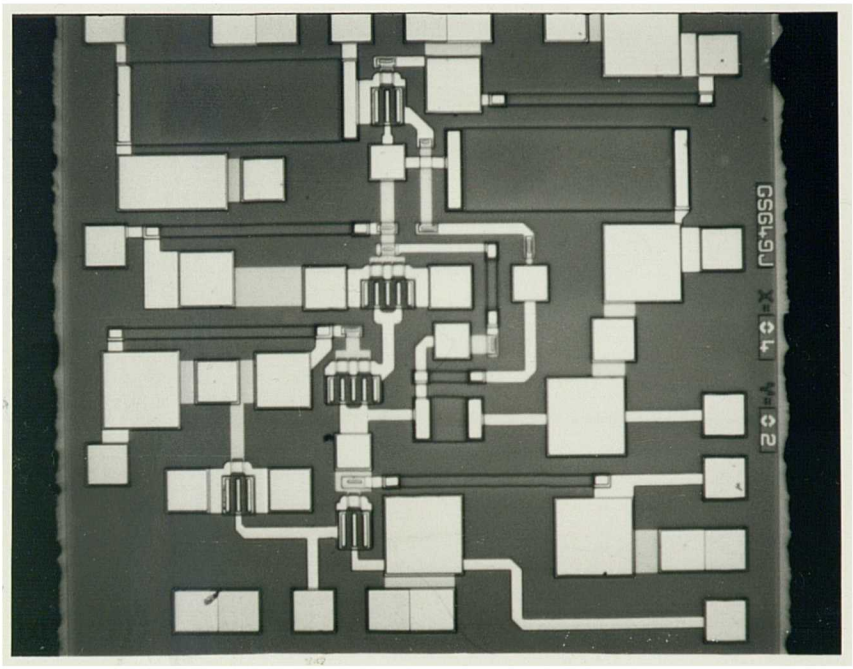

Figure 4.10: Receiver photomicrograph

4.2.3 Simulation and experimental results

The CG receiver was simulated taking into consideration the external bias circuit and the frequency behaviour obtained for different values of photodiode capacitance. The simulation results are shown in figure 4.11. The predicted response shows a transimpedance gain of 45 dBΩ and a bandwidth variation from 3.4 GHz to 2.9 GHz for a PIN capacitance variation from 0.1 pF to 0.5 pF respectively. The low −3 dB frequency (not shown in the graph) is below 10 MHz and is due to AC coupling between the stages. The measured receiver transimpedance is shown in figure 4.12. The midband transimpedance gain is 44 dBΩ but the measured −3 dB bandwidth is 1.5 GHz which is noticeably lower than that predicted by simulation. Part of this loss in bandwidth is due to the PIN response which contributes to the overall receiver response with a roll-off of 2 dB per decade from 100 MHz to 2 GHz. When this roll-off is corrected ('*' in figure 4.12) the estimated receiver

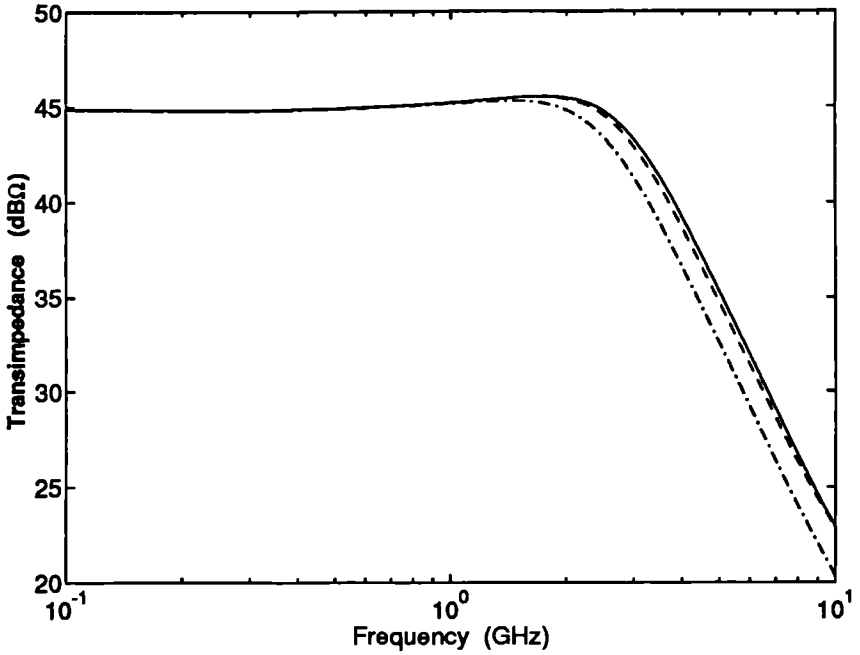

Figure 4.11: Simulated receiver response: '——' $C_d = 0.1\,\mathrm{pF}$, '– –' $C_d = 0.2\,\mathrm{pF}$ and '– · –' $C_d = 0.5\,\mathrm{pF}$

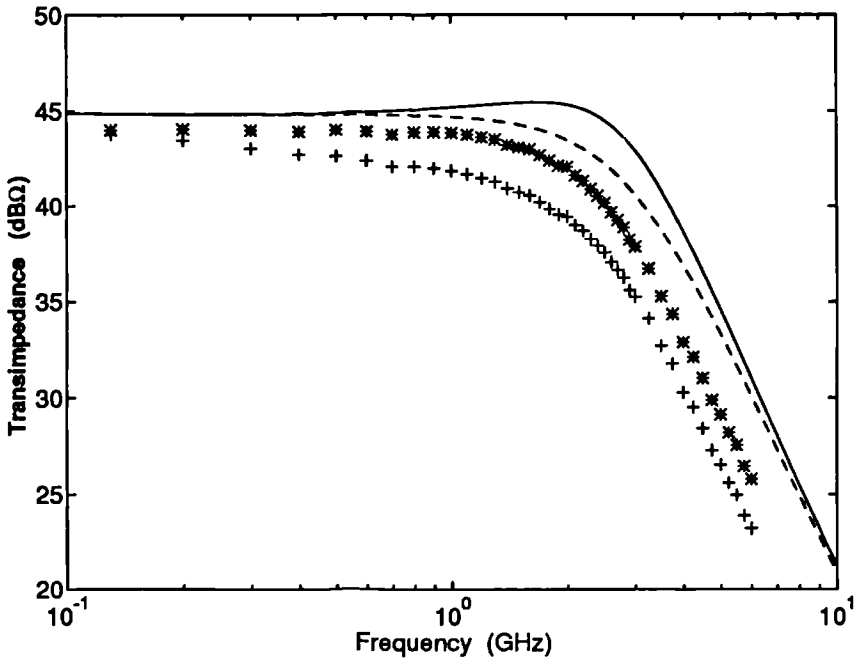

Figure 4.12: CG receiver response: '+' measured, '∗' corrected for PIN response, '——' simulated with $C_d = 0.15\,\mathrm{pF}$ and '– –' simulated with added feedback capacitances

bandwidth is 2.3 GHz[2]. However, the PIN response can not fully account for the loss in bandwidth, which was also observed on the electrical measurements of the s_{21} parameter of the preamplifier. This problem was discussed with the foundry process manufacturer. It was suggested that the discrete model provided for the resistors (discussed in the previous chapter) is inaccurate and that the foundry resistors should be modelled as thin-film resistor with distributed capacitance. To investigate this possibility the receiver was simulated adding a small capacitance across each of the feedback resistors. The value of this feedback capacitances was optimised until reasonable agreement between the corrected frequency response and the predicted response was observed. The simulated receiver response is represented in figure 4.12 (dashed line) when a value of 25 fF is used for both the feedback capacitances. As can be seen from figure 4.12 the corrected and the re-simulated receiver responses display similar frequency behaviour over the measurement range. In spite of that, the choice of values of the feedback capacitances is somewhat arbitrary and the loss in bandwidth can not be attributed with complete certainty to the existence of such parasitic feedback capacitances.

The equivalent input noise current spectral density was measured and both the measurement and the simulation results are shown in figure 4.13. Since the CG receiver gain is relatively low, a post-amplifier with 23 dB gain and 7 dB noise figure was used for the noise and the sensitivity measurements. In this case the noise introduced by the post-amplifier is significant and the measured noise and sensitivity correspond to the receiver and post-amplifier combination. In figure 4.13 the measured noise is shown ('+') together with the simulated noise for receiver alone ('——') and the simulated noise for the receiver followed by the post-amplifier ('– –'). Also shown in the figure ('*') is the measured noise when the corrected receiver response is used to estimate the equivalent input noise current spectral density.

Figure 4.14 shows the measured sensitivity for the receiver and post-amplifier combination for 5 Gbit/s operation. Two sets of measurement points are shown that correspond to a pseudo random bit sequence (PRBS) with length $2^7 - 1$ ('*') and a repetitive '0101' ('+') pattern. The measured optical sensitivity for a BER of 10^{-9} was −13.1 dBm and −14.4 dBm for the PRBS and the '0101' pattern respectively. The repetitive '0101' pat-

[2] This result is consistent with the higher bandwidth measured when using the BT&D-2022 PIN (C_d = 0.15 pF) mounted on a 50 Ω K connector and connected to the CG preamplifier using a bias 'T'. With this PIN the low frequency 2 dB per decade roll-off was not present and a 2.8 GHz −3 dB bandwidth was measured.

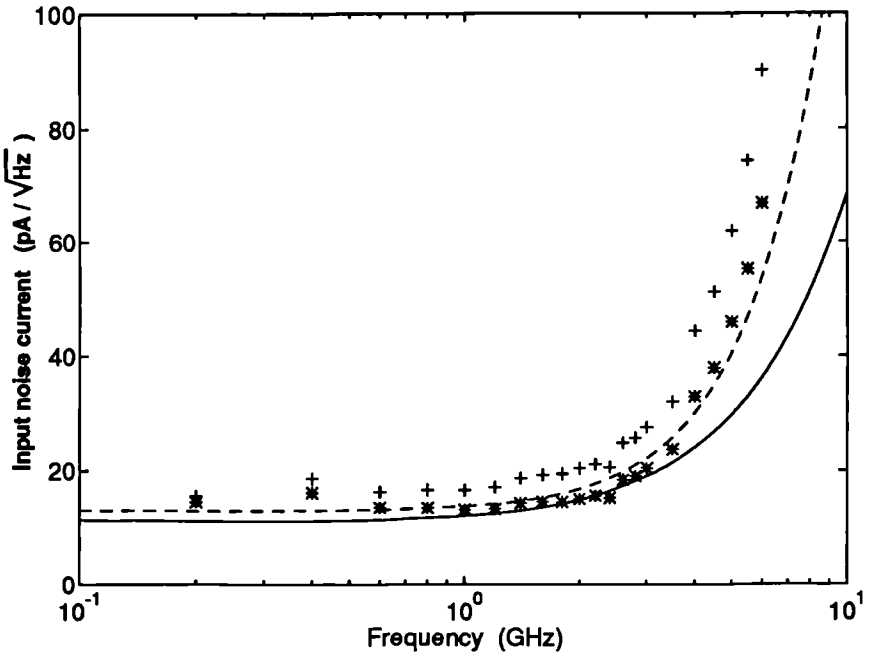

Figure 4.13: Equivalent input noise current spectral density: '+' measured for the receiver with a 7 dB NF post-amplifier, '*' corrected for PIN response, '– –' simulated and '——' simulated for the receiver only

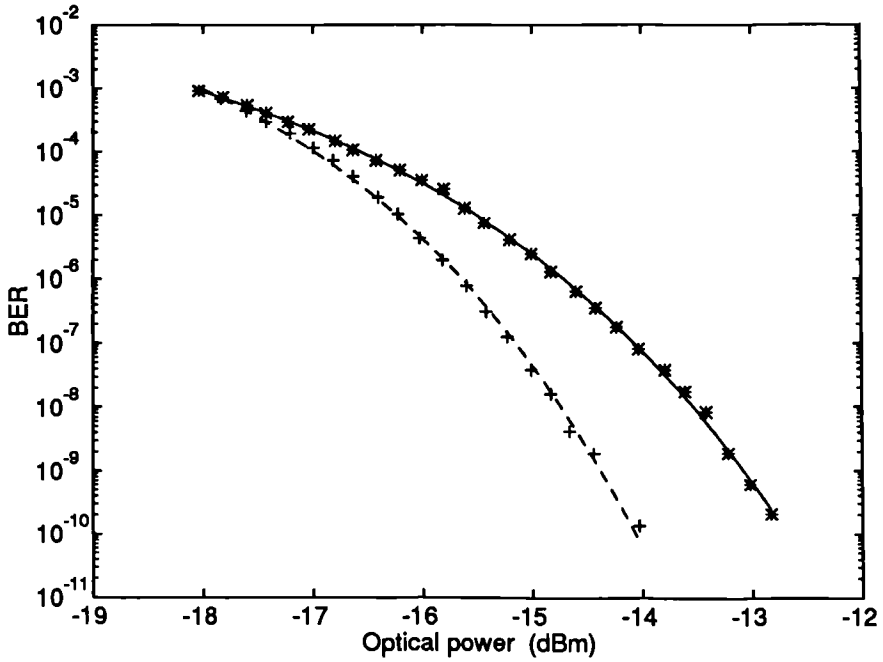

Figure 4.14: Optical sensitivity: '*' $2^7 - 1$ PBRS and '+' '0101' pattern

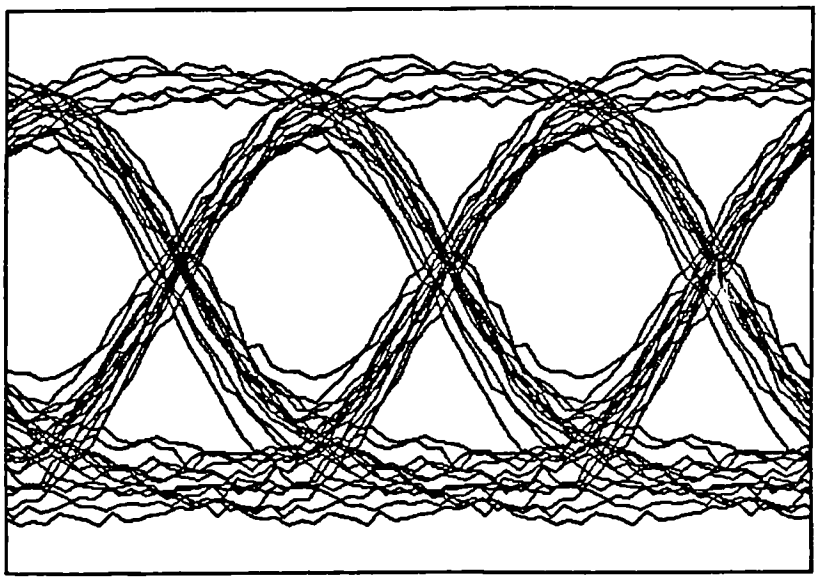

Figure 4.15: Measured eye-diagram ($B = 5\,\text{Gbit/s}$, $P = -17\,\text{dBm}$)

tern was used to assess the effects of patterning due to the receiver low $-3\,\text{dB}$ frequency. The predicted receiver sensitivity from simulation is $-21.1\,\text{dBm}$ for the receiver alone and $-20.2\,\text{dBm}$ for the preamplifier/post-amplifier combination. When the measured noise and frequency responses are used to estimate the receiver sensitivity a figure of $-21.7\,\text{dBm}$ is obtained. However, this figure degrades to $-17.6\,\text{dBm}$ when the response of the PIN diode is accounted for in the sensitivity calculation.

The mentioned sensitivity values are based on noise considerations only and the effects of ISI due to the receiver reduced bandwidth are not considered. To account for ISI the eye-closure penalty was estimated from the measured eye-diagram, shown in figure 4.15, and is $3\,\text{dB}$. Using this value the predicted sensitivity is $-17.2\,\text{dBm}$ when the simulated noise and transimpedance are used and $-14.6\,\text{dBm}$ when the corrected noise and transimpedance measurements are used. This last value is within $1.5\,\text{dB}$ of the measured sensitivity.

4.3 Separate pseudo-lumped signal shaping networks

Embedding of the signal shaping function in the receiver preamplifier was considered in section 4.1. The proposed technique is attractive due to its simplicity and because it offers the possibility of reducing the number of system components. Yet, due to the frequency limitations of the active devices provided by the GaAs foundry process, embedding of the signal shaping in the preamplifier can only be usefully done for bit rates not exceeding

5 Gbit/s when standard optical receiver circuit topologies are used[3]. However, as discussed in the previous chapter, the GaAs foundry components are characterised and accurately modelled for frequencies up to 20 GHz. This means that GaAs passive elements can be used to implement post-detection passive pulse shaping filters operating at data rates approaching 20 Gbit/s. In this section the design and optimisation of two passive post-detection filters will be considered. These filters, designed for operation at 10 and 15 Gbit/s, implement the pulse shaping functions necessary for the practical realisation of the signal designs proposed in section 2.3. The general structure of the time domain optimisation technique developed for the design of these filters will now be discussed and compared with the established optimisation procedure.

4.3.1 The direct time domain optimisation method

The receiver design of section 4.1 illustrates clearly the importance of accounting in the design and optimisation processes for all the degeneracies associated with the quasi-lumped nature of the GaAs components and it shows that circuit layout is an important part of MMIC design. Thus, any accurate design or optimisation technique must account for the process degeneracies as intimately and directly as possible. The established method of design and optimisation of GaAs MMICs that fulfils these requirements can be described by the following basic sequence of operations (figure 4.16):

1. The circuit design and optimisation process begins by the conversion of the mathematical optimum target into a suitable form. Such a form can be either the response of an ideal lumped element circuit or a set of s-parameters. These are the only forms that most commercial available CAD tools accept as targets for circuit optimisation. This first step is of fundamental importance to the whole of the optimisation process since the mathematical target might be physically unrealisable.

2. Next, a first MMIC layout is done using estimated values for the GaAs circuit elements. These can be obtained from the ideal lumped circuit that is being used as a target, when the implementation of a passive GaAs circuit is the objective. In the case of a complex active circuit, the GaAs element values can be obtained from a pre-optimisation cycle where most (or all) elements are considered ideal. This was

[3]Techniques to extend the signal shaping capacity of active circuits will be addressed in the next chapter.

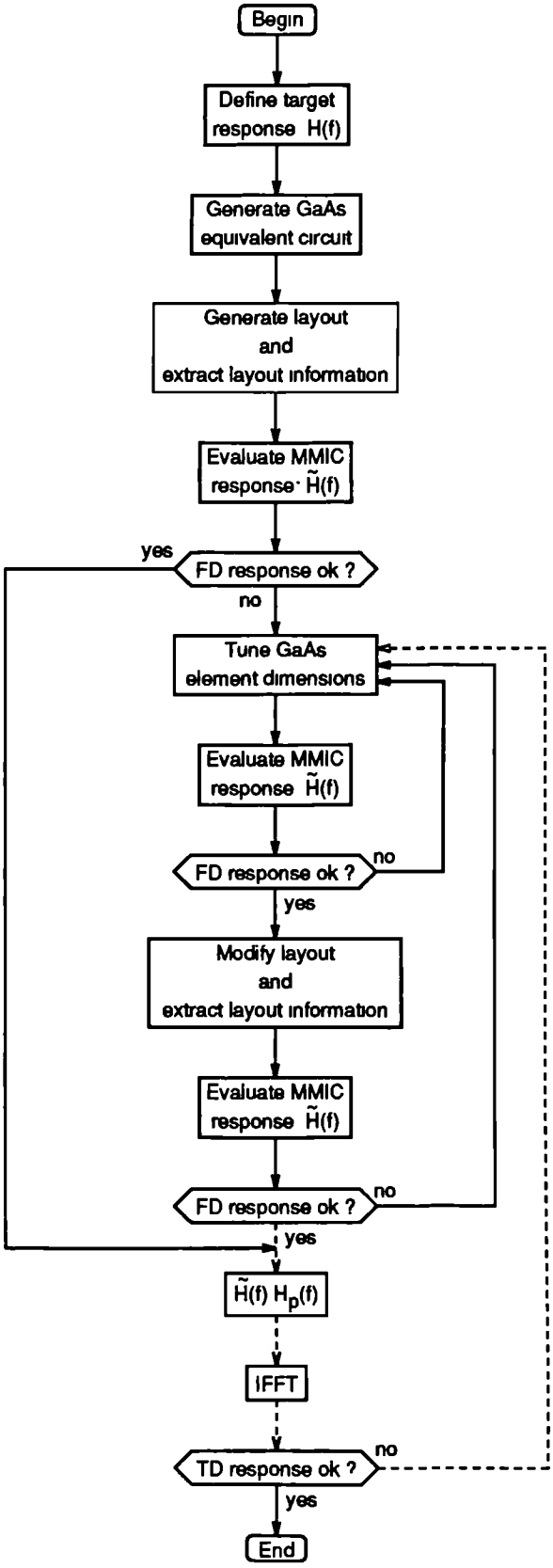

Figure 4.16: Established optimisation procedure

the approach used to obtain the initial values of the MCB based receiver described in section 4.1.

3. Using information extracted from the circuit layout the MMIC response is simulated and the cost function, that measures the discrepancy between the MMIC response and the specified target response, is evaluated. A decision is taken whether the circuit performance is satisfactory or there is room for improvement. In case the response is acceptable, a further check on the MMIC time domain response is made if required.

4. When improvement of the MMIC response is necessary, a frequency domain optimisation cycle is entered where the GaAs element dimensions are tuned until an acceptable response is obtained. The layout is then modified to accommodate the new GaAs element dimensions and the new layout information is extracted and used to simulate the MMIC response. The cost function is then evaluated and the frequency domain cycle is repeated until a satisfactory frequency response is obtained. Although the frequency domain optimisation cycle was considered here as being composed of two separate actions — optimisation of the GaAs element dimensions and layout modification — both operations can be merged in one. In spite of that, no single commercially available CAD tool offers this possibility. Therefore, sharing of the design and optimisation process among circuit optimisers and layout CAD tools forces an artificial splitting to be introduced in the optimisation procedure.

5. If the objective of the optimisation process is to achieve a pre-specified frequency response the optimisation process is complete at this stage. However, when a certain time domain response is required, the result of the frequency domain optimisation must be checked in the time domain. For this, the MMIC frequency response is multiplied by the input pulse spectrum and the result converted into the time domain by means of an inverse fast Fourier transform (IFFT). The result is then matched against the desired pulse response. If the MMIC response is acceptable then the optimisation process is concluded. Otherwise, the frequency domain optimisation cycle (phase 4) must be repeated.

Commercially available CAD tools do not provide the facilities necessary for the realisation of the last phase of the optimisation procedure (represented by the dashed path in the flowchart of figure 4.16). A supporting numerical analysis software package is necessary

to perform the frequency to time domain conversion and to evaluate the cost function in the time domain. This means that to implement the time domain optimisation using the established frequency domain procedure, constant switching between software packages is necessary. However, the main weakness associated with the procedure described above is the absence of a natural feedback path between the time domain errors and the frequency domain optimisation. Consequently, the success of the design often depends on an informed guess by the designer to direct the frequency domain optimisation to the desired solution. For all the above reasons, the procedure is inefficient when applied to the optimisation of circuits designed to realise the signal shaping strategies proposed in this thesis — which aim to replicate certain optimum time domain responses — or in general, to any digital communication problem where some aspects of the time domain circuit response are of critical importance. To overcome these limitations, a direct time domain optimisation procedure was devised. This is represented in the flowchart in figure 4.17 and follows, broadly, the same structure as the previous one. That is, it consists of an initial phase where the time domain target response and a first layout estimate are obtained, followed by an optimisation loop where the GaAs element dimensions are tuned and the layout modified until an acceptable time domain solution is reached. The sequence of operations is essentially the same as the one executed in the frequency domain optimisation cycle of the previous procedure, which is represented by the solid line path in the flowchart of figure 4.16. The main difference between the two optimisation processes lies in the cost function evaluation, now done in the time domain at each stage of the optimisation and used directly to control the optimisation outcome.

Practical implementation of the proposed procedure requires, besides MMIC frequency response evaluation, that at each iteration the MMIC response be converted into the time domain and convolved with the input pulse before the cost function can be evaluated. As mentioned before, these are mathematical processing capabilities that are not found in commercial microwave circuit simulators. Since the use of a CAD tool to obtain the MMIC response would pose implementation and efficiency problems, it was decided that both the circuit simulation and the evaluation of the cost function, and related operations, would be made using the same numerical analysis package. For this the MATLAB program [71] was used in conjunction with the purpose-developed MATLAB circuit analysis toolbox, described in the previous chapter, allowing the integration of the simulation, cost function

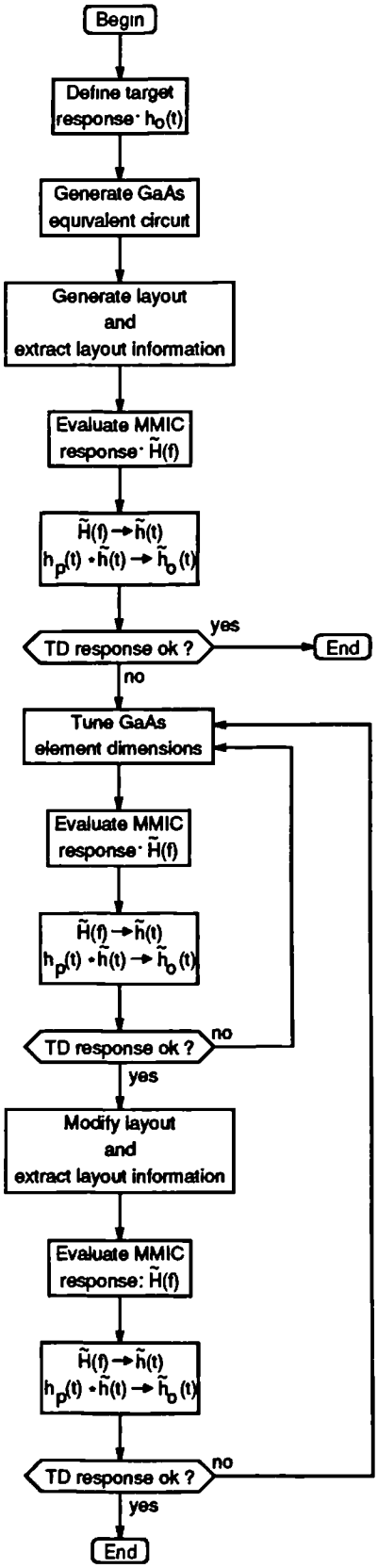

Figure 4.17: Time domain optimisation procedure

evaluation and optimiser in the same package[4].

Finally, it should be pointed out that both in the proposed and the established optimisation procedures the operations of layout generation and modification had to be made with recourse to a separate software package and through human intervention, which imposes some limitations on the efficiency of the process. Nonetheless, most of the optimisation effort is in obtaining the GaAs element dimensions and usua ., only a few layout modifications are necessary before the final solution is obtained when a good starting point GaAs circuit is selected.

4.3.2 10 and 15 Gbit/s post-detection filters

The direct time domain optimisation method described above was applied to the design and optimisation of 10 and 15 Gbit/s post-detection filters constructed on GaAs. These filters are sixth order L-C ladder networks and implement the pulse shaping function necessary for the practical realisation of the new signal designs (NSD) proposed in section 2.3. A relatively high order network was used to achieve, with an all-pole structure, the degree of eye symmetry relative to the optimum sampling instant needed to ensure maximum tolerance to jitter. The manufactured filters are appropriate for systems with an optimum decision threshold setting of $d = 0.2$ and employing 25% duty cycle rectangular pulses as the signalling elements.

Frequency and time domain targets

The frequency response (s_{21}) of an ideal sixth order ladder L-C network, figure 4.18, was chosen as the target for the frequency domain optimisation of the GaAs filters. The ideal

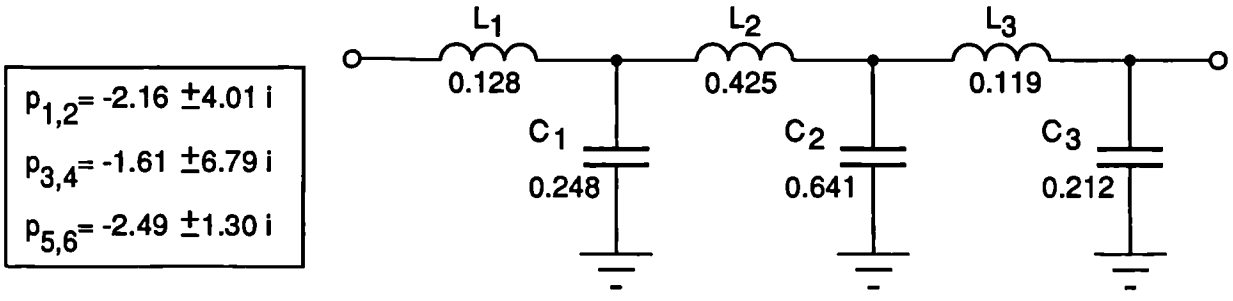

Figure 4.18: Ideal lump d element filter and normalised pole positions

[4]The effort invested in developing the circuit analysis toolbox, using MATLAB, can be justified by the added flexibility to the design-optimisation process, due to the availability of a wide range of mathematical, signal processing functions and different optimisation algorithms within MATLAB.

circuit has the same topology as the implemented GaAs filters and consequently it provides a realistic target for both the magnitude and group delay responses. Additionally, it served to obtain the first estimate of the GaAs filters element values. These were obtained by optimising the positions of a set of six poles $(p_1, p_2, \ldots, p_6)$ ir the s-plane, until the all-pole pulse response they define closely matched the mathematical target response (equation (2.34)). The optimisation of the pole positions was made in the time domain and the least square error between the mathematical target and the filter response was minimised. After an optimum set of poles were obtained, the values of the ideal filter elements were calculated from these using standard filter design techniques [88]. Both the normalised pole positions and the normalised filter element values are given in figure 4.18.

To effect the time domain optimisation of the GaAs networks the mathematical pulse response, defined by equation (2.34) with $d = 0.2$, was used as the target. Since this pulse response is not physically realisable a weighting function was introduced to ensure the success of the time domain optimisation. A rectangular function with period $0.5T$ and width $0.2T$ was used which also ensured that errors in the time domain constraints defined by equations (2.27), (2.28) and (2.29) are emphasised while the contributions to the cost function due to those time instants not corresponding directly to errors in these constraints are minimised.

Optimisation results

Figures 4.19 to 4.22 illustrate the simulation results at different stages of the optimisation process for the 15 Gbit/s filter. Figure 4.19 represents the simulated eye-diagram for the ideal lumped element filter of figure 4.18. The obtained eye-diagram is almost an exact replica of the NSD eye-diagram when d=0.2, figure 2.19, indicating that the chosen low pass structure can be successfully used to effect the desired pulse shaping function. To generate the eye-diagram of figure 4.20 the circuit elements of the ideal network were replaced by their appropriately scaled GaAs counterparts. The figure reveals the severe penalty incurred in performance due to the degeneracies associated with the GaAs elements and clearly points to the need for accounting as completely as possible for these in the optimisation process. In figure 4.21 the result of conventional frequency domain optimisation is shown. Here, a full description of the GaAs elements is used and all the critical layout components are included for circuit simulation and optimisation. The improvement in performance achieved by the frequency domain optimisation is clear. However, the

eye still exhibits a significant amount of intersymbol interference although all the other required characteristics — correct positioning of the signal trajectory crossings, low telegraph distortion and low slope ISI — can already be observed. Finally, figure 4.22 shows the simulated eye-diagram after the time domain optimisation procedure proposed in this chapter. Again, all the significant circuit and layout degeneracies are included. The sim-

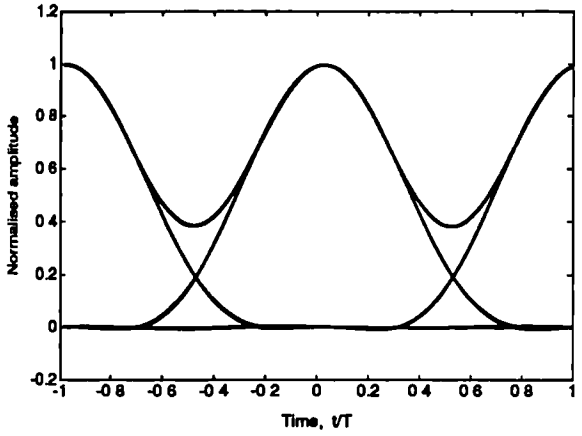

Figure 4.19: Eye-diagram of the ideal lumped element network

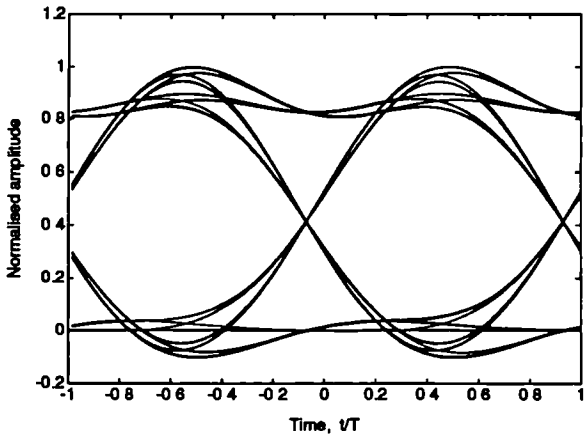

Figure 4.20: Eye-diagram of the unoptimised GaAs network

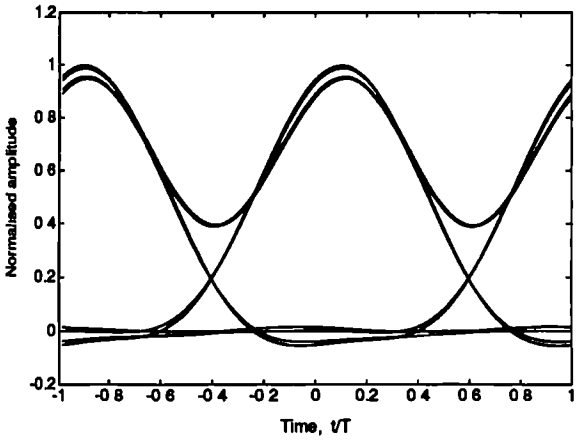

Figure 4.21: Eye-diagram after conventional frequency domain optimisation

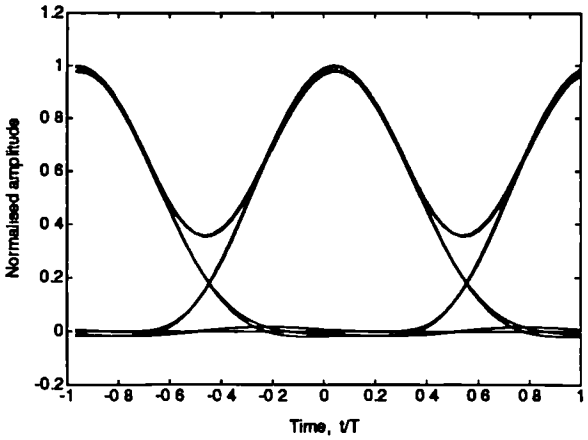

Figure 4.22: Eye-diagram after the proposed time domain optimisation

ulated eye-diagram clearly shows that a performance very close to the one obtained with an ideal lumped element network is possible with a GaAs network for the high bit rates under consideration and the excellent intersymbol interference and telegraph distortion performance of the filter is evident.

A photomicrograph of the fabricated 10 and 15 Gbit/s filters is shown in figure 4.23.

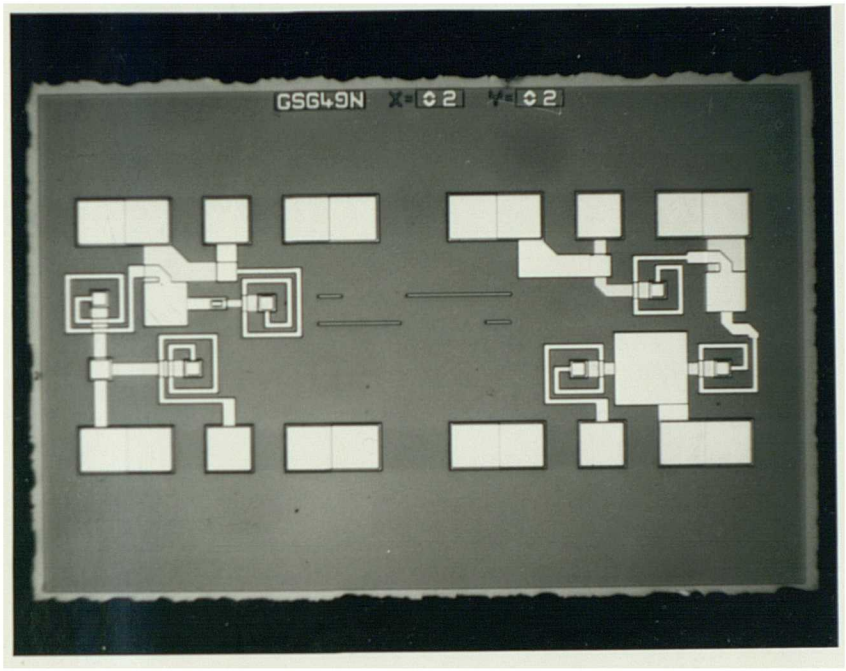

Figure 4.23: Photomicrograph of the 10 Gbit/s (left) and 15 Gbit/s (right) filters

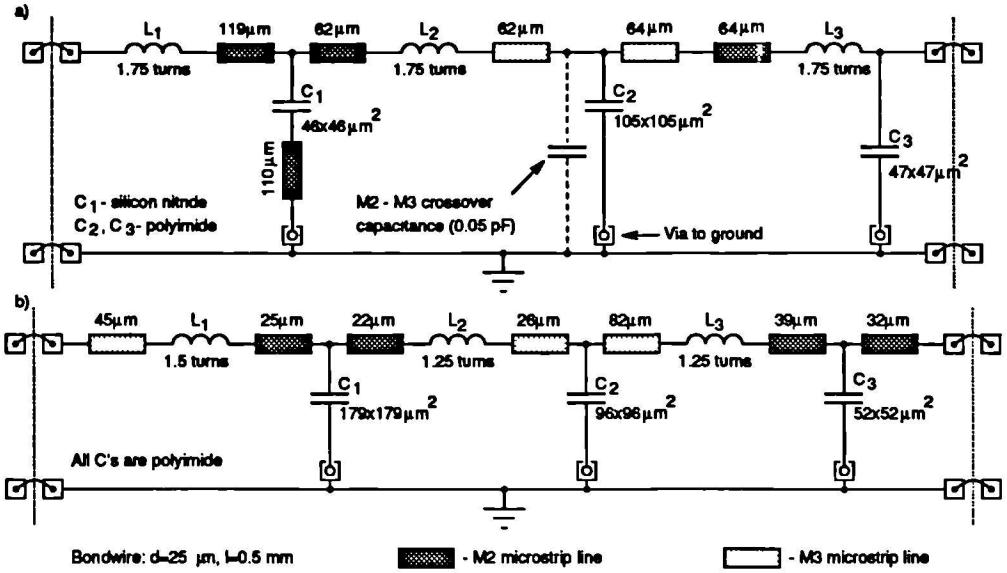

Figure 4.24: GaAs filters, extracted layout: a) 10 Gbit/s and b) 15 Gbit/s

The chip size is 2 mm×1 mm with each filter occupying an area smaller than 1 mm×1 mm. Figure 4.24 is the schematic diagram of the final GaAs filters and includes all the relevant layout information. From this, it can be seen that the layout information used to model the GaAs networks accounted for through GaAs vias, interconnecting transmission lines, alumina to GaAs transitions and estimated metal to metal crossover capacitances. Additionally the inductor and capacitor dimensions were constrained to be within the range allowed by the GaAs foundry process used.

Experimental results

The 10 and 15 Gbit/s filters were characterised experimentally by s-parameter measurements up to 25 GHz using a two-port microwave wafer probe and an automatic network analyser. Since wafer probe testing was used, the simulated effects of bondwire inductance and the alumina end effect capacitance are not present in the measured s-parameters although they were taken into account during the optimisation process. To be able to compare the experimental and simulation results and to evaluate the filters performance these effects were added to the experimental data. The predicted and the measured (corrected) magnitude and group delay of the s_{21} parameter for the 10 and the 15 Gbit/s filters are represented in figures 4.25 and 4.26, respectively. Both figures display very good agreement between the predicted and the measured responses over the entire measurement range. Using the measured frequency responses, 10 and 15 Gbit/s eye-diagrams were simulated which are shown in figures 4.27 and 4.28, respectively. The simulated eye-diagrams

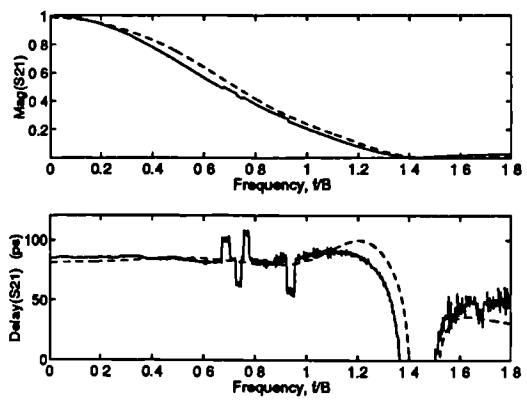

Figure 4.25: 10 Gbit/s GaAs filter frequency response: '– –' predicted, '——' measured

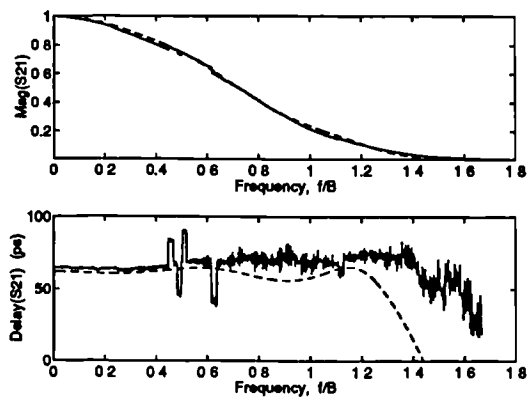

Figure 4.26: 15 Gbit/s GaAs filter frequency response: '– –' predicted, '——' measured

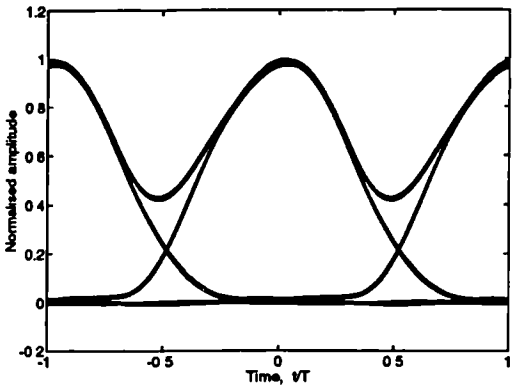

Figure 4.27: 10 Gbit/s eye-diagram

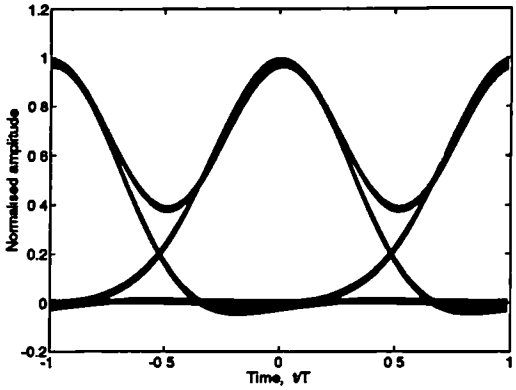

Figure 4.28: 15 Gbit/s eye-diagram

are very similar to the predicted eye for the 15 Gbit/s filter, figure 4.22, and exhibit low intersymbol interference, low telegraph distortion, low slope ISI and the signal trajectory crossings are very close to the design value $d = 0.2$. Based on the experimental data and using the eye-closure approach described in section 2.2 the power penalty versus timing offset for the two filters was estimated and is represented in figures 4.29 and 4.30 for the 10 and 15 Gbit/s filters, respectively. These graphs show that in the absence of timing errors both filters introduce less than 0.5 dB of penalty, when compared with the ideal NSD with $d = 0.2$, due to the small ISI present at the optimum sampling instant ($t = 0$). Since the eye-diagrams are not perfectly symmetrical around $t = 0$ the power penalty is different for positive and negative timing offsets, which are represented in the figures by the dotted and

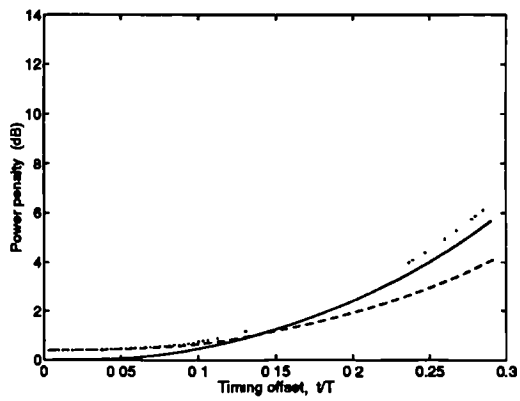

Figure 4.29: Power penalty versus timing offset for the 10 Gbit/s filter: '– –' negative and '. . . .' positive timing offsets, '——' new signal design with $d = 0.2$

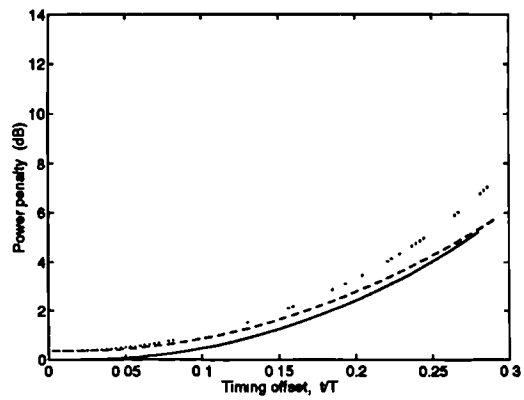

Figure 4.30: Power penalty versus timing offset for the 15 Gbit/s filter: '– –' negative and '. . . .' positive timing offsets, '——' new signal design with $d = 0.2$

the dashed lines respectively. For the 10 Gbit/s filter the estimated power penalty never exceeds by more than 0.5 dB that of the ideal signal over the plotted timing offset range, while for the 15 Gbit/s filter the figure is 0.75 dB for timing offsets less than 15% of the bit period and 1 dB for timing offsets as large as 25% of the bit period.

The results obtained show that the new signal designs proposed in section 2.3, which improve the system robustness to signalling and timing jitter, can be practically implemented and the resulting system performance can be expected to be close to that theoretically predicted without any increase in system complexity when compared with classical raised cosine equalisation. The experimental results also show that the adopted optimisation strategy allows the rigorous design and optimisation of realisable filters for high speed digital optical communication systems.

4.4 Summary

In this chapter the practical realisation of the signal shaping strategies proposed in chapter 2 and the suitability of present day GaAs technology for the realisation of such signal designs was investigated. To this end, two GaAs MMIC designs were discussed. The first design is an APD optical receiver optimised for operation at 4.8 Gbit/s with 50% RZ pulses. This receiver incorporates the signal shaping necessary to secure optimal noise filtering and jitter tolerant operation according to the MCB criterion. The second signal shaping design presented explores the possibility of using passive GaAs MMIC networks to effect signal shaping at very high bit rates. The implemented designs were studied in connection with the new signal shaping strategies discussed in section 2.3 and two practical post-detection filters were demonstrated for operation at 10 and 15 Gbit/s. A novel time domain optimisation technique was developed for the accurate design of GaAs post-detection filters and was successfully applied in the optimisation of the above mentioned filters. A third design was also discussed that makes use of a low input impedance front-end stage — the common gate configuration — to construct an optical receiver that achieves a high degree of insensitivity to photodiode parasitics. The manufactured GaAs MMIC receiver achieved 5 Gbit/s operation with a sensitivity better than −13 dBm.

In the next chapter the use of distributed amplifiers to implement optical receivers that overcome the frequency limitations of the more common receiver topologies will be considered. In particular, a new method of using the distributed amplifier as a transversal

filter will be proposed and the potential that the technique offers for the realisation of very high bit rate pulse shaping optical receivers will be illustrated.

Chapter 5

Distributed amplifier signal shaping strategy

In the previous chapter, the design of a GaAs MMIC optical receiver with embedded signal processing was considered. The proposed technique is attractive due to its simplicity but, because of the frequency limitations of the active devices and circuit topology used, its usefulness is limited to bit rates less than 5 Gbit/s. In this chapter the potential of the distributed amplifier to overcome the frequency limitations of the more commonly used circuit topologies and to provide useful gain up to frequencies close to f_T of the active devices used will be examined. The use of distributed amplifiers as optical receivers will be discussed and a design example will be presented which suggests that for the GaAs foundry process described in chapter 3 distributed optical receivers operating at bit rates well over 10 Gbit/s are a practical possibility. A novel technique is presented for using the distributed amplifier (DA) as an active pulse shaping/filtering network by effectively constructing the amplifier as a transversal filter [89, 90]. The technique can be successfully applied to the signal shaping strategies developed in this thesis and allows the implementation of post-detection active filters and optical receivers with embedded signal shaping for operation at 10 Gbit/s or higher. The potential of the distributed amplifier as a pulse shaping network will be illustrated by two optical receiver designs with embedded signal shaping. The first is a 10 Gbit/s optical receiver designed to have a 100% raised cosine frequency response while the second implements a particular case of the new signal designs derived in chapter 2 and its performance will be compared with its equivalent passive realisation described in section 4.3.

5.1 Additive amplification

Optical receivers have been, with very few exceptions, constructed as a class of amplifiers known as multiplicative amplifiers. For these amplifiers, the desired gain is obtained by cascading successive stages resulting in an overall gain proportional to the product of the gains supplied by the individual stages. In a simplified study, Ohkawa [91] concluded that such receivers can achieve 3 dB bandwidths close to 36% of the cutoff frequency (f_T) of the active devices when some form of matching network is used between the stages or close to 24% of f_T when no such networks are used. Nonetheless, in practical implementations, due to circuit degeneracies, such figures are usually not achieved. A second class of amplifiers exists — additive amplifiers — with which 3 dB bandwidths approaching f_T are obtainable in practice. Such amplifiers are formed by 'paralleling' several active devices and the overall gain is proportional to the sum of the gains contributed by the individual active devices. Such amplifiers are called distributed amplifiers and were first introduced by Percival [92] as vacuum tube amplifiers. However, the concept is extensible to either bipolar or FET amplifiers and the widest bandwidth MMIC amplifiers reported have been constructed as distributed amplifiers [93, 94]. The basic principles of operation of the distributed amplifier will now be reviewed.

5.1.1 The distributed amplifier

A distributed FET amplifier is constructed by combining the input and output capacitances of the active devices with inductors ' ı such a way that two artificial transmission lines are formed [95, 96, 97]. One of the possible topologies is shown in figure 5.1. In such a circuit the input and output capacitances of each device become the capacitance per unit

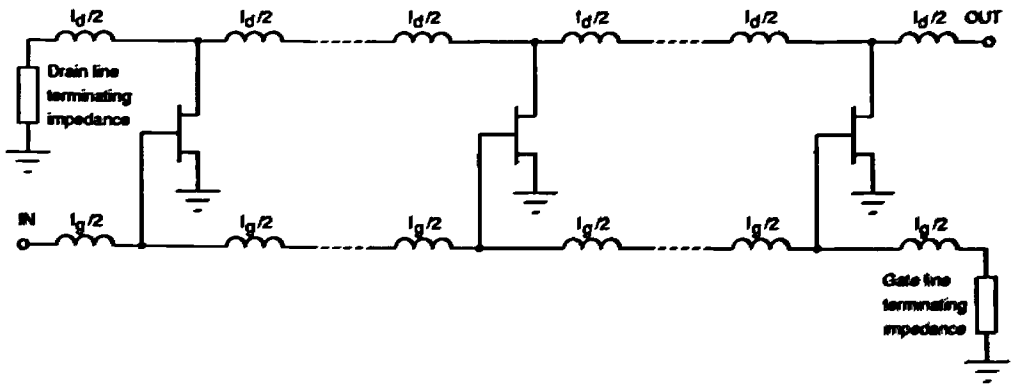

Figure 5.1: Distributed amplifier

section of the input (gate) and output (drain) lines respectively, with the output line being coupled to the input line through the transconductance of the active devices. Additionally, both the gate and the drain lines are terminated — at both ends — by their characteristic impedances. The basic principle of operation of the distributed amplifier is easily described with reference to its simplified model shown in figure 5.2. In this model, the active devices are represented as the intrinsic device only and are assumed to be unilateral ($C_{dg} = 0$). The input artificial transmission line can be seen to result from the combination of the

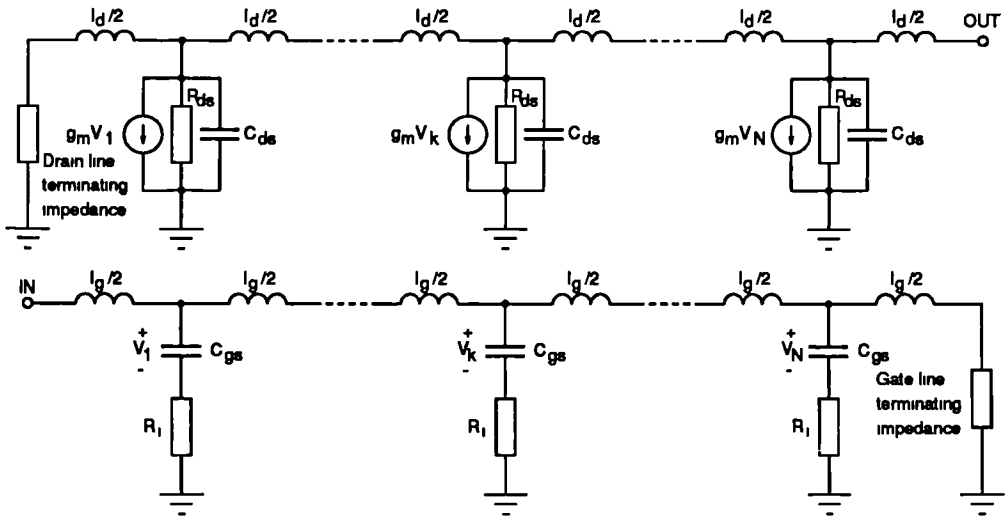

Figure 5.2: Simplified model of a distributed amplifier

inductances $l_g/2$ with C_{gs} while the output line is formed by the combination of C_{ds} with the inductances $l_d/2$. Using this model, the amplification process can be described as follows: When a signal is applied to the input port it travels down the gate line towards the termination where, ideally, it is totally absorbed. The travelling signal is sampled by the gates of the individual FETs and transferred to the drain line via the transconductance. If the phase velocities in the two transmission lines are equal, the signals travelling in the forward direction on the drain line will add in phase. Backwards propagation in the drain line will also occur but the back propagating wave will be totally absorbed by the drain line termination. If the loss in R_i and R_{ds} is ignored then the power gain of the amplifier is given by [96]

$$G = \frac{1}{4} N^2 g_m^2 Z_{og} Z_{od} \tag{5.1}$$

where N is the total number of stages and

$$Z_{og} = \sqrt{l_g/C_{gs}} \tag{5.2}$$

$$Z_{od} = \sqrt{l_d/C_{ds}} \tag{5.3}$$

are the characteristic impedances of the gate and drain lines respectively. Equation 5.1 shows that is possible to increase the amplifier gain simply by increasing the number of stages. However, due to the loss introduced by R_i and R_{ds} there is an optimum number of stages that maximises the amplifier gain for a given active device [96]. Also, as in any other type of amplifier, a tradeoff between gain and bandwidth has to be made. In theory, the gain should remain flat up to f_T if the cut-off frequency of the lines is made much higher than the f_T of the devices. The cut-off frequency of the gate and drain lines — which relate directly to the phase velocity of the lines — are given respectively, by:

$$f_{cg} = \frac{1}{\pi\sqrt{l_g C_{gs}}} \tag{5.4}$$

$$f_{cd} = \frac{1}{\pi\sqrt{l_d C_{ds}}} \tag{5.5}$$

Therefore, once the transmission line impedance is selected the line cut-off frequency cannot be chosen independently. Even when these factors are considered, distributed amplifiers still allow the highest bandwidths to be achieved with 28, 55 and 95 GHz bandwidth amplifiers being reported in the literature with corresponding s_{21} gains of 6, 10 and 5.5 dB [98, 94, 93].

Some other desirable features of distributed amplifiers include good input and output matching and low sensitivity to circuit element value variations, while its main disadvantages are relatively high noise and high power consumption when compared to other amplifier schemes.

Finally, for practical realisation the gate and drain inductors are commonly replaced by short lengths of high-impedance transmission lines which makes the distributed amplifier an ideal candidate for MMIC integration in both microstrip [99] and coplanar [100] wave guide technologies.

5.1.2 Distributed optical receivers

The use of distributed amplifiers to implement optical receivers has received very little attention in the literature. The first proposal to use the distributed amplifier as an optical receiver was made by Aitchison in 1990 [101], but since then only two experimentally demonstrated distributed receivers have been reported [102, 103, 104]. The published receivers were implemented using GaAs MESFETs. One of the designs achieved 11 GHz bandwidth with an average noise spectral density of $27\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ (transimpedance gain not reported) and was designed as a coplanar structure [102, 103]. The other displayed a transimpedance gain of $38\,\mathrm{dB}\Omega \pm 1\,\mathrm{dB}$ over the range 3–13 GHz with average noise of $18\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and was constructed as a MMIC using microstrip technology. Both receivers were designed for coherent detection applications.

Although Aitchison's analysis [101, 105] indicates that there is a noise advantage if a distributed amplifier is used to construct an optical receiver — instead of the common-source structure — his conclusions must be put in perspective. His analysis is based on early work [106, 97] on the noise behaviour of distributed amplifiers, where the gate and drain artificial transmission lines are assumed to be lossless, i.e. the presence of R_i in the gate and R_{ds} in the drain transmission line is completely neglected. Consequently, the input and output impedances of the amplifier are assumed to be purely real and thus the contribution to the receiver noise of the cross-correlation spectral density noise term of the active devices — which is imaginary [59, 60] — is negleted. Another consequence of this simplified analysis is that the signal to noise ratio degradation that starts to occur once the number of amplifying stages increases above a certain limit is not taken into account. Finally, from bandwidth considerations, the characteristic impedance of the input line must be chosen to be less than $100\,\Omega$ (typically $50\,\Omega$). Since a load termination of the same magnitude as the line impedance must be used, this corresponds to a minimum receiver noise floor close to $18\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. A distributed optical receiver is thus expected to be noisier than an optimised common-source receiver, as happens for $50\,\Omega$ microwave amplifiers. Nonetheless, the distributed amplifier is still attractive for very high speed optical communication systems since it offers the possibility of achieving the highest bandwidths and when used in coherent or optically pre-amplified systems its poorer noise performance can be tolerated.

The comments made above point to a need for a better understanding of the noise

mechanisms in distributed amplifiers so that the amplifier parameters which influence its noise performance can be identified and consequently noise optimised designs can be produced. Such work is beyond the scope of this thesis but some possible solutions to the reduction of noise in distributed optical receivers can be proposed. First, for a distributed optical receiver the photodiode is directly connected to the input artificial transmission line and the standard system requirement of 50 Ω input impedance is not present. This means that the line impedance can be made higher to increase the transimpedance gain of the amplifier, at the same time decreasing the noise contribution of the gate line terminating impedance. From bandwidth considerations it is not practical to increase the line impedance to values higher than approximately 100 Ω, yet even this slightly higher value will reduce the contribution of the termination resistor to the equivalent input noise spectral density from 18 pA/$\sqrt{\text{Hz}}$, for a 50Ω termination, to 13 pA/$\sqrt{\text{Hz}}$. Second, a further reduction in the noise due to the input line termination can be achieved if, as suggested by Niclas [107], instead of a straightforward termination the last amplification stage employs a shunt-feedback circuit to provide for the termination of the gate artificial transmission line. Finally, the use of noise matching networks between the photo-diode and the input port of the distributed amplifier can be investigated. Since in a distributed optical receiver the use of an input matching load is translated into a degradation of the receiver noise and gain performance, the absence of input matching usually results in excessive ripple in the receiver response. Such a problem can be minimised by improving the quality of the gate line termination load by using a matching circuit between the transmission line and its termination, as reported in reference [98].

5.1.3 16.4 GHz GaAs MMIC distributed optical receiver

The potential offered by the distributed amplifier for very high speed optical system applications is illustrated here by a very high bandwidth distributed optical receiver. The receiver was designed using the GaAs foundry process described in chapter 3 and consists of six identical stages, one of which is shown in figure 5.3. The stage comprises the gate and drain lines with the inductors replaced by lengths of microstrip line. The MESFETs used are $2 \times 50\,\mu$m biased at I_{dss} and a microstrip line was inserted in series with the MESFET drain to equalise the phase velocity between the input and output artificial transmission lines. The $2 \times 50\,\mu$m MESFET was chosen for the design because it offers the smallest value of C_{gs} of all the standard MESFET cells. This allowed the gate line characteristic

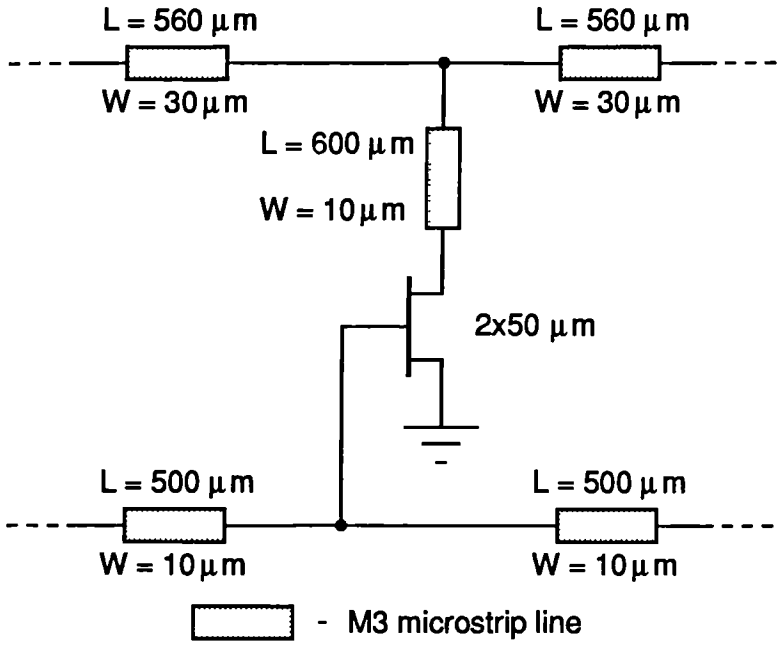

Figure 5.3: Single stage of the distributed optical receiver

impedance to be set at 75 Ω without compromising the receiver bandwidth. Also, the small loss introduced by this device permitted six devices to be cascaded to obtain a transimpedance gain of 42.3 dBΩ. The PIN and the PIN/MMIC transition were modelled by the equivalent circuit represented in figure 5.4. This model accounts for the photodiode junction capacitance (C_d), the bulk resistance (R), the bond-wire inductance (L) and the fringing effect capacitance (C) of the MMIC input transmission line [108].

The layout of the receiver sent for fabrication is represented in figure 5.5 and its dimensions are 3 μm×2 μm. In the layout design discontinuities were minimised by using curved lines instead of sharp corners and the coupling between lines was minimised by maintaining the transmission lines as far apart as possible within the layout constraints.

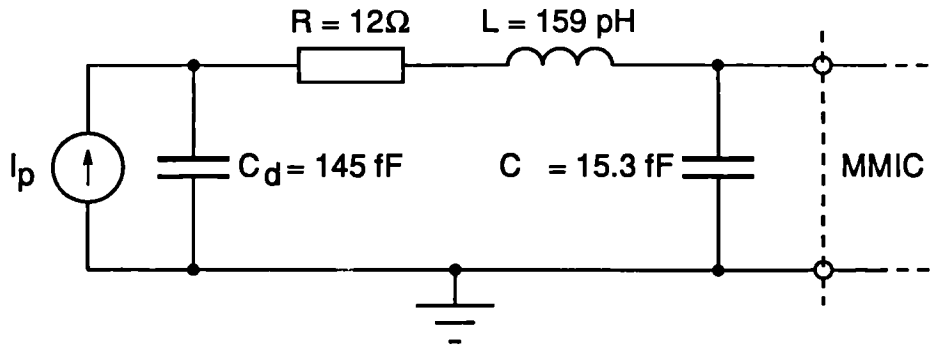

Figure 5.4: PIN and PIN/MMIC transition equivalent circuit

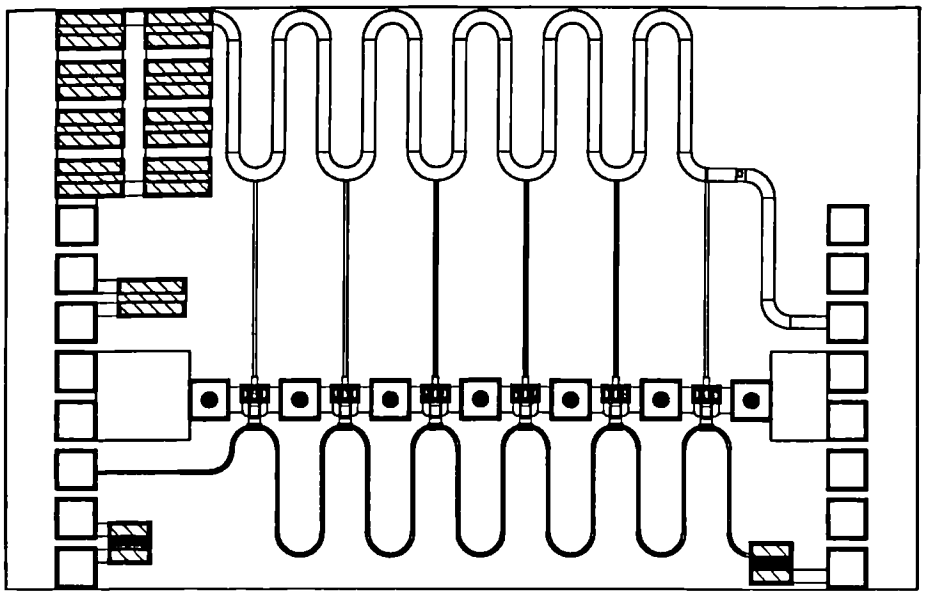

Figure 5.5: Distributed receiver layout

Also, as can be noticed from the layout, no on-chip capacitors are used for decoupling. This was done to avoid possible resonance of the bond-wire inductance with the capacitors and to allow the decoupling to be optimised off chip. Finally, the drain load (50 Ω) was split into eight 25 Ω resistors — two parallel arrangements of four resistors in series. With this arrangement it was possible to bias the receiver through the drain termination while maintaining linear behaviour of the load resistor. This scheme also permits the receiver to achieve DC operation.

The simulated transimpedance and group delay frequency behaviour of the distributed receiver is shown in figure 5.6. The receiver exhibits a 3 dB bandwidth of 16.4 GHz with a transimpedance gain of 42.2 ± 1.4 dBΩ and a group delay of 110 ± 40 ps within the pass-band. These figures when compared, for example, with the best simulation results for the common-gate receiver discussed in the previous chapter represent a decrease in gain of 75% but an increase in bandwidth of 566%. Finally, figures 5.7 and 5.8 show the simulated eye-diagrams for 10 and 20 Gbit/s operation. These results illustrate clearly the superiour high frequency performance of the distributed amplifier.

In the next section it will be shown that the distributed amplifier is fundamentally equivalent to a transversal filter and that this can be used to obtain an amplifier with a controlled frequency response. In particular, the distributed amplifier can be used to implement the signal shaping strategies proposed earlier in this thesis.

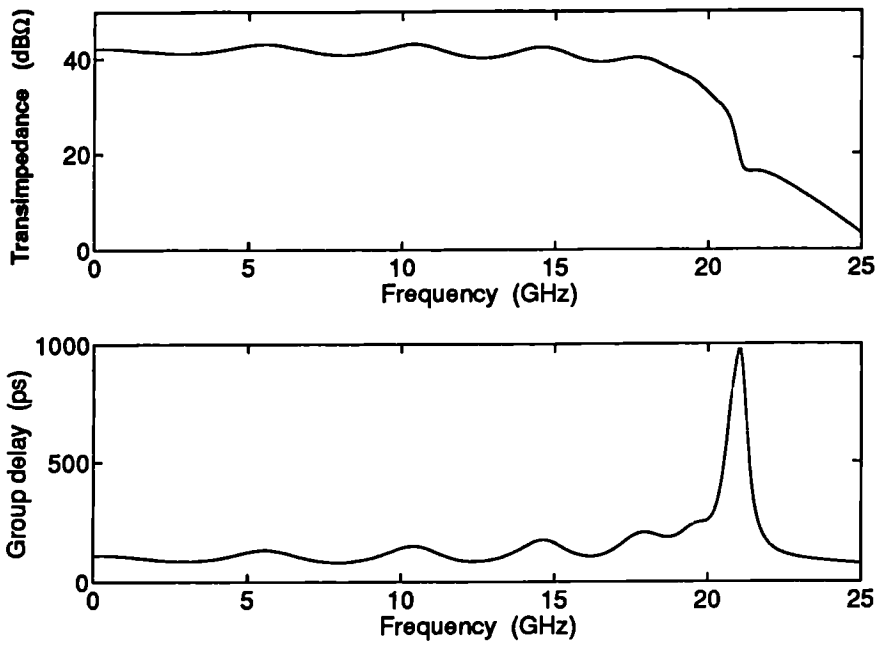

Figure 5.6: Distributed receiver transimpedance and group delay

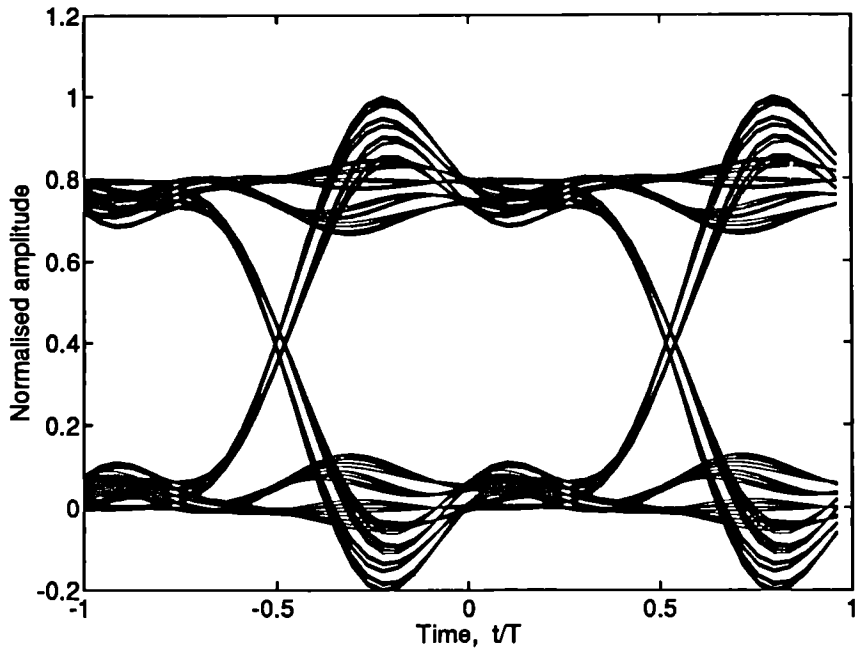

Figure 5.7: 10 Gbit/s eye-diagram

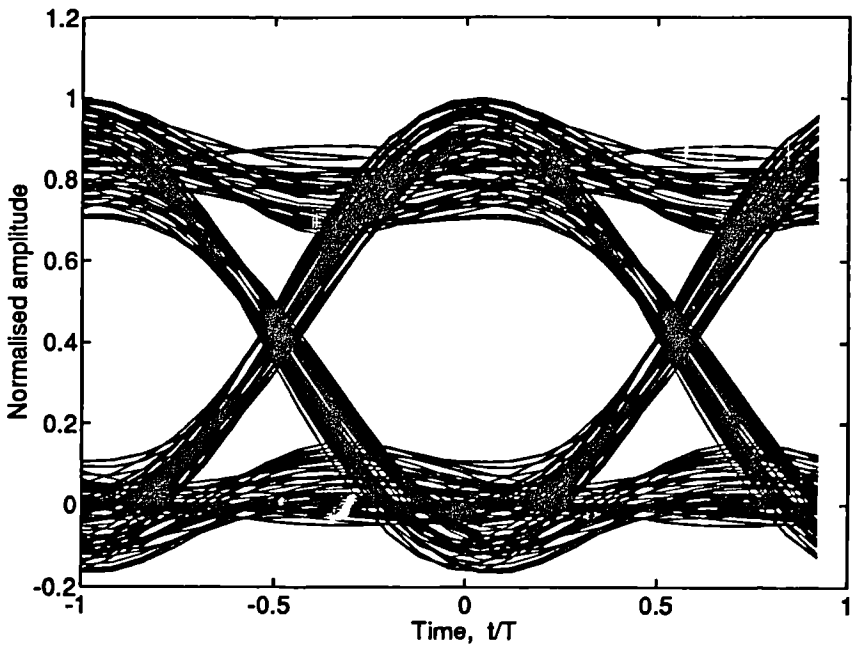

Figure 5.8: 20 Gbit/s eye-diagram

5.2 The distributed amplifier as a transversal filter

Transversal filters find wide applications in digital communication systems [109] and have been proposed as a means to reduce the effects of linear distortion impairments in digital fibre optic systems [80, 12]. Some of their possible applications include the equalisation of chromatic and polarisation dispersion in direct-detection systems that use multimode lasers [80, 12], chromatic dispersion conpensation in coherent-detection systems [110] and limited bandwidth equalisation in optical receivers [111]. A functional representation of the transversal filter is shown in figure 5.9. The filter consists of a delay line with total delay $2N\tau$ and with $2N+1$ taps, where 2N is the number of delay line sections and τ is the section delay. A signal travelling along the delay line is sampled at each tap output. The sampled outputs are multiplied by the respective gain coefficients $G_{-N}, G_{-N+1}, \ldots, G_N$ and summed to form the final output. The frequency response of such a structure is given by [19]

$$H_{TF}(f) = \left[\sum_{k=-N}^{N} G_k \, e^{-j2\pi f k\tau} \right] e^{-j2\pi f N\tau} \tag{5.6}$$

The basic operation of a distributed amplifier as a transversal filter can be understood by considering figure 5.10 showing the functional equivalent of a $2N+1$ stage distributed

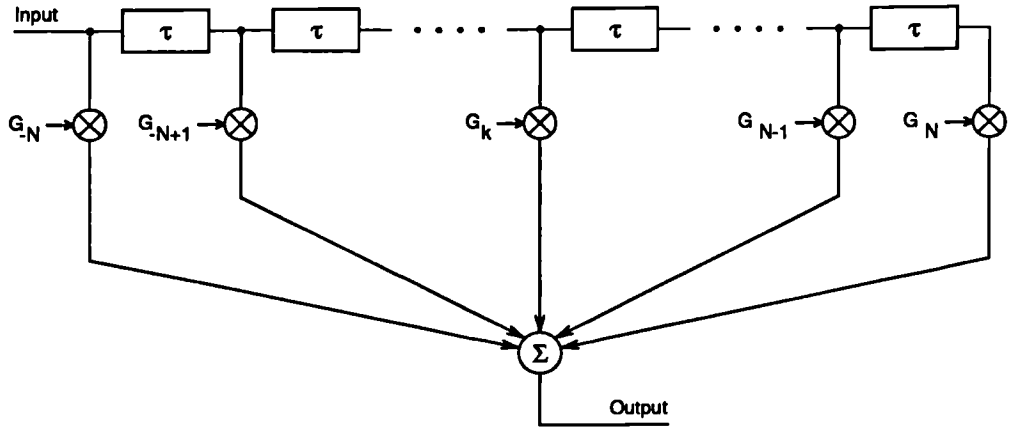

Figure 5.9: Transversal filter

amplifier. In this figure, G_k is the gain of stage k which ideally corresponds to the MESFET transconductance g_{mk}. The delays τ_g and τ_d are the respective interstage delays of the gate and drain transmission lines. They are associated with the time taken by a signal to travel between two consecutive gate electrodes in the gate artificial transmission line (τ_g) and between two consecutive drain electrodes in the drain transmission line (τ_d). The contribution to the total output due to gain stage k, for an input signal $s_{in}(t)$, can be expressed as:

$$s_{out}^{k}(t) = G_k\, s_{in}(t - (N+k)\,\tau_g - (N-k)\,\tau_d) \tag{5.7}$$

Therefore, the total output signal is

$$s_{out}(t) = \sum_{k=-N}^{N} s_{out}^{k}(t) \tag{5.8}$$

$$s_{out}(t) = \sum_{k=-N}^{N} G_k\, s_{in}(t - k\,(\tau_g - \tau_d) - N\,(\tau_g + \tau_d)) \tag{5.9}$$

with corresponding signal spectrum

$$S_{out}(f) = \sum_{k=-N}^{N} G_k\, S_{in}(f)\, e^{-\jmath 2\pi f k (\tau_g - \tau_d)}\, e^{-\jmath 2\pi f N (\tau_g + \tau_d)} \tag{5.10}$$

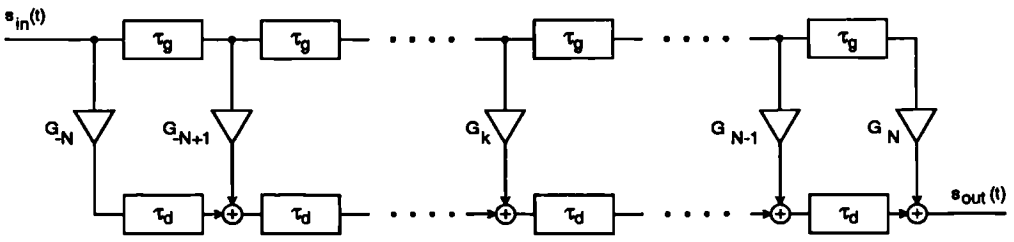

Figure 5.10: Functional equivalent of a $2N+1$ stage distributed amplifier

where $s_{in}(t) \Leftrightarrow S_{in}(f)$ and $s_{out}(t) \Leftrightarrow S_{out}(f)$ are Fourier transform pairs. From the above the transfer function is

$$H_{DA}(f) = \left[\sum_{k=-N}^{N} G_k \, e^{-j2\pi f k(\tau_g - \tau_d)} \right] e^{-j2\pi f N(\tau_g + \tau_d)} \tag{5.11}$$

Comparing equations (5.6) and (5.11) it can be seen that the transfer function of the distributed amplifier is the same as that of a transversal filter with the equivalent tap delay $\tau_g - \tau_d$ chosen to be equal to τ. A difference between the two transfer functions is in the complex exponential term outside the brackets. However, this term adds only a linear phase to the transfer function, which is different for the two structures, reflecting the inherent time delay for each structure. The transversal filter and the distributed amplifier are thus functional equivalents allowing standard time and frequency domain techniques [109] to be used to choose the gain coefficients G_k and the equivalent tap delay $\tau_g - \tau_d$ so that the distributed amplifier can be used at microwave frequencies to implement a given filtering function.

If the gain coefficients G_k and the tap delay τ are known, the distributed equivalent can be readily implemented in MMIC technology if for each amplifying stage the following equalities are observed:

$$\frac{g_{mk}}{\max[g_{mk}]} = \frac{G_k}{\max[G_k]} \tag{5.12}$$

$$\tau_k = \tau_g - \tau_d = \tau \tag{5.13}$$

where g_{mk} and τ_k are the k-th stage transconductance and equivalent tap delay, respectively. For the case of an FET based MMIC the stage gain can be set by controlling the FET area, while the delay elements can be implemented by including impedance matched transmission lines in series with the gate (or drain) line as shown in figure 5.11. The delay elements ΔT_k, shown in figure 5.11 as transmission lines, are designed to give an effective delay:

$$\Delta T_k = \frac{1}{2}\left[\tau - (T_{g_k} - T_{d_k})\right] \tag{5.14}$$

Where, T_{g_k} and T_{d_k} are the delays of the k-th stage gate and drain artificial transmission lines respectively. Since the MESFET C_{gs} is much higher than its C_{ds}, then, for a given line impedance the inherent delay in the gate artificial transmission line is higher than that of the drain line. Therefore, placing the delay lines in series with the gate inductors has the advantage of reducing circuit size and losses.

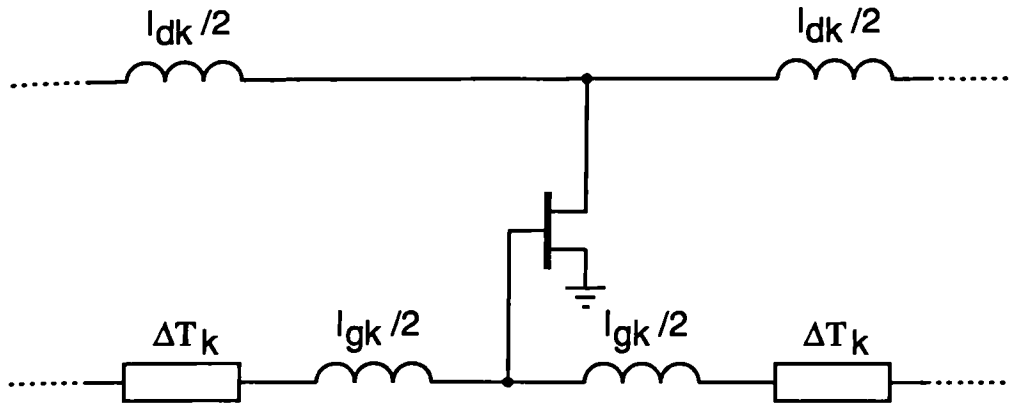

Figure 5.11: Single section of the 'distributed transversal filter'

Design procedure

The design of the distributed amplifier equaliser starts with the selection of the equivalent tap delay $\tau_g - \tau_d$. Here, the designer has some degree of freedom but the final value is a compromise between the number of stages necessary to achieve the desired gain and the maximum frequency of operation. Once the equivalent tap delay τ is fixed, the desired impulse response is sampled at intervals τ to determine the values of the gain coefficients, as shown in figure 5.12 a). This sets the relative values of the gain coefficients G_k which must be denormalised using the relation (5.12) once the maximum MESFET area is known. The choice of the highest FET area is effected in the frequency domain in such a way that the lowest transmission line cutoff frequency (f_c in figure 5.12 b)) is chosen to be higher than the highest frequency of interest but low enough to eliminate the periodicity of the frequency response, effectively providing an anti-alias filter. Finally, the delay line elements are designed as impedance matched transmission lines in series with the gate or the drain transmission line according to equation (5.14). Due to the artificial transmission line losses and circuit non-idealities the circuit must be optimised so that the desired response is obtained.

5.2.1 Alternative structures

When negative gain coefficients are needed to realise a given impulse response then a modification of the basic distributed transversal filter is necessary. A possible solution is the realisation of a distributed filter with two separate artificial gate transmission lines and a common drain line. The input signal could then be fed to the two gate lines in

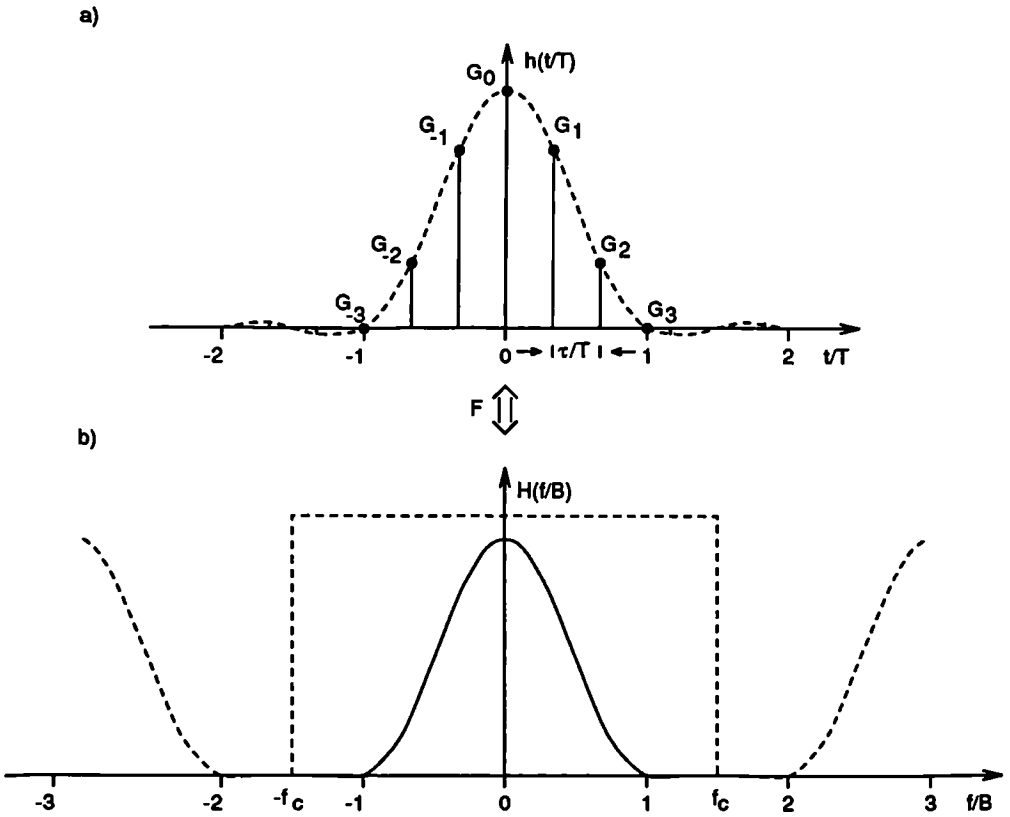

Figure 5.12: Determination of gain coefficients a), transmission line cutoff frequency b)

anti-phase by using a broadband power splitter and an inverter. An example of such a structure is represented in figure 5.13 where a transversal filter with positive ($G_{\pm 1}$, G_0) and negative ($G_{\pm 2}$) coefficients is realised. The major drawback of this structure is the need for power splitting and signal inversion of the input signal. This can introduce a noise penalty and so such a structure might not be useful for the construction of optical receivers with embedded signal shaping. Nonetheless, it can be used to implement post-detection signal shaping filters with gain where the noise requirements are not so stringent.

A second limitation of the distributed transversal filter is associated with the relative sizes of the MESFETs used to implement the different gain coefficients and results from size restrictions imposed by the foundry process used. Since the relative areas of the MESFETs are set by the impulse response that is being implemented and the foundry process sets a minimum FET area that can be used this can result in either FET areas higher than the maximum allowed by the process or in the maximum area FET setting an artificial transmission line whose cutoff frequency is less than the maximum frequency of interest. Two solutions to this problem are possible. First, the tap delay can be strategically selected

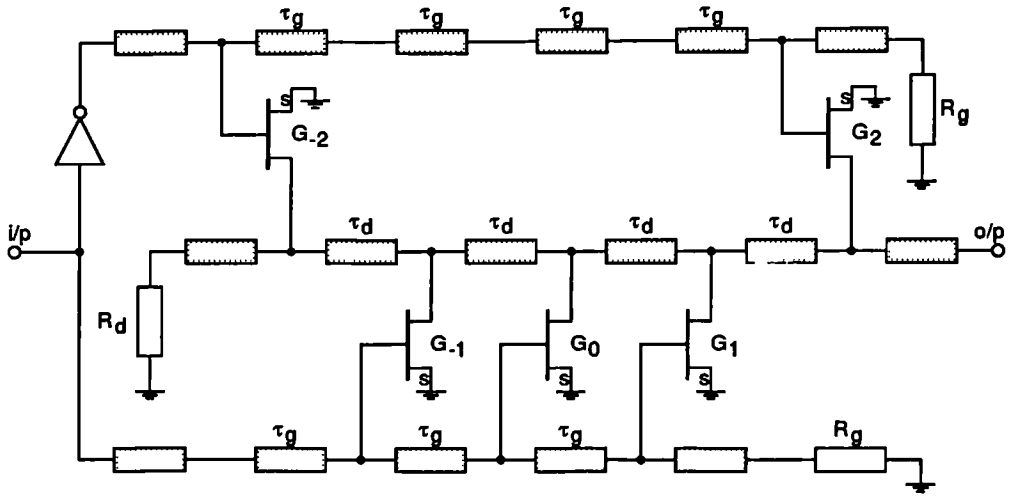

Figure 5.13: Microwave transversal filter with both positive and negative gain coefficients

to avoid very small gain coefficients but if by so doing the area ratio still falls outside the range allowed by the foundry process then the higher gain coefficients can be shared among two or more consecutive stages, whereby the added stages have zero differential delays between the gate and drain transmission lines ($\tau_g - \tau_d = 0$). This is exemplified in figure 5.14 where the gain coefficient G_k is split equally between two amplifying devices. A second possibility is to design all the MESFETs to have the same area and to then optimise the differential delays ($\tau_{g_k} - \tau_{dk}$) between each two consecutive stages so that the desired impulse response is obtained. A preliminary investigation of this method gave promising results but it was found that the design of the transmission line cutoff frequency should be carefully effected to eliminate the undesirable response at frequencies higher than the

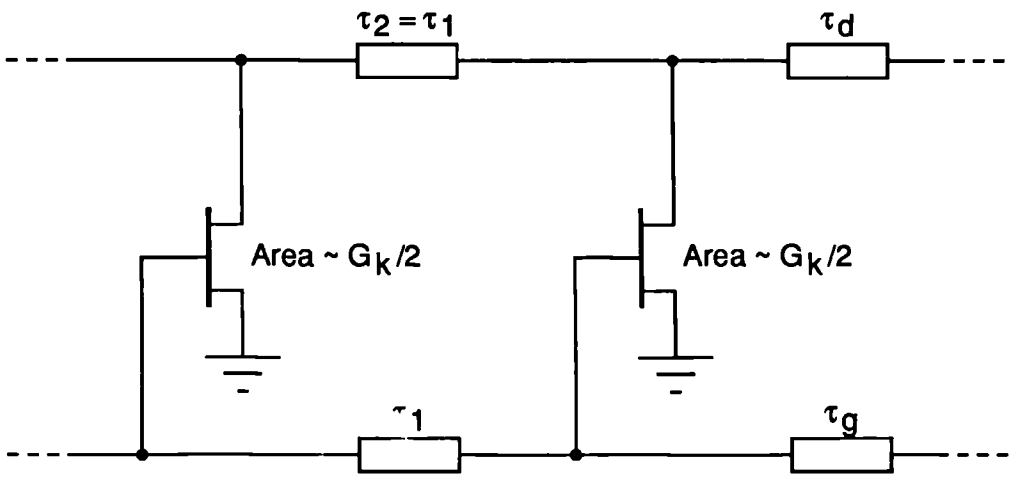

Figure 5.14: Gain sharing between two MESFETs

maximum frequency of interest.

The use of the distributed amplifier as a signal processing element, as discussed here, is based on the fundamental equivalence between the transversal filter and the distributed amplifier. Such an equivalence has been identified in the literature in different forms [112, 89, 113]. However, further insight into such use of the distributed amplifier is obtained by recognising that in the classical distributed amplifier the gate and drain artificial transmission lines are in fact constructed as low-pass filters. Based on this, standard filter theory can be used to design the artificial transmission lines and obtain the desired frequency response. This view was first proposed by Minnis in [114] where the common low-pass structure of the distributed amplifier was transformed into a band-pass one by adding shunt inductance in parallel with FET C_{gs}. In this way a well controlled band-pass response was obtained and operation close to the maximum frequency of oscillation (f_{max}) of the FETs was obtained. The same concept was used in reference [115], where a detailed procedure is given for the design of low-pass distributed amplifiers having the characteristics of a Tchebycheff filter.

5.2.2 Design examples

The practical implementation of the distributed amplifier transversal filter concept developed in this chapter will now be considered by means of two receiver designs with embedded signal shaping.

Raised cosine receiver

The first design considered is a 10 Gbit/s distributed optical receiver preamplifier having a raised cosine transfer function. Both the gate and drain transmission line characteristic impedances were chosen to be 50 Ω. Five common-source stages were used to implement the raised cosine transfer function resulting in an equivalent tap delay ($\tau = \tau_g - \tau_d$) of 33.3 ps when the gain coefficients G_3 and G_{-3} are selected as shown in figure 5.12. Using this value of τ the gain coefficients obtained from the impulse response are $G_0 = 1$, $G_{-1} = G_1 = 0.74$ and $G_{-2} = G_2 = 0.27$. Practical realisation as a GaAs MMIC was examined and the amplifier parameters were optimised to take into account line losses and the degeneracies associated with the GaAs process used. After optimisation, the transistor sizes $4 \times 94\,\mu$m, $4 \times 70\,\mu$m and $2 \times 50\,\mu$m were obtained corresponding to the gain coefficients G_0, G_1 and G_2 and corresponding to a total gate width of 1140 μm and a D.C. transimpedance of 114 Ω.

With the maximum area FET ($4 \times 94\,\mu$m) used and the $50\,\Omega$ characteristic impedance the gate line cutoff frequency is close to 10 GHz and the correct anti-aliasing function is realised. Impedance matched transmission lines of different lengths were used in each stage in series with the gate line to obtain the equivalent tap delay of $33.3\,ps$. In this investigation, standard GaAs $50\,\Omega$ transmission lines were used in the simulation as the impedance matched delay lines which, due to their dimensions, are somewhat impractical. Nonetheless, this does not constitute an impediment to the realization of the proposed designs since very compact low impedance GaAs coplanar transmission lines can be made using the technique described in reference [116]. Figure 5.15 shows the simulated gain and delay characteristics. It is clear from the graphs that a well controlled response is obtained up to the highest frequencies of interest, giving excellent agreement between the circuit response and the target. The eye diagram for this amplifier is given in Figure 5.16 showing little ISI. The PIN model used in the simulations is that shown in figure 5.4 and the final microstrip line dimensions are given in table 5.1. In this table, l_g, w_g, l_d and w_d are the microstrip line dimensions used to implement the gate and drain inductances $l_{gk}/2$ and $l_{dk}/2$ shown in figure 5.11 and Δ_l and Δ_d are the dimensions of the matched delay lines ΔT_k in the same figure.

Gain coefficient	$G_{\pm 2} = 0.27$	$G_{\pm 1} = 0.74$	$G_0 = 1$
MESFET (I_d=0.5 I_{dss})	$2 \times 58\,\mu$m	$4 \times 68\,\mu$m	$4 \times 91\,\mu$m
l_g (μm)	324	542	601
w_g (μm)	10	10	10
l_g (μm)	110	131	121
w_g (μm)	20	20	20
Δ_l (μm)	1104	996	690
Δ_w (μm)	151	151	151

Table 5.1: Raised cosine receiver element dimensions

New signal design receiver

The second design to be discussed is also a 10 Gbit/s receiver with embedded pulse shaping. The signal shaping function implemented by the receiver is the same as for the 10 Gbit/s post-detection GaAs filter discussed in section 4.3, that is, it equalises a 25% duty cycle rectangular pulse into the new signal design for an optimum decision threshold setting of $d = 0.2$. Selection of the gain coefficients in this design was effected in such a way as to avoid

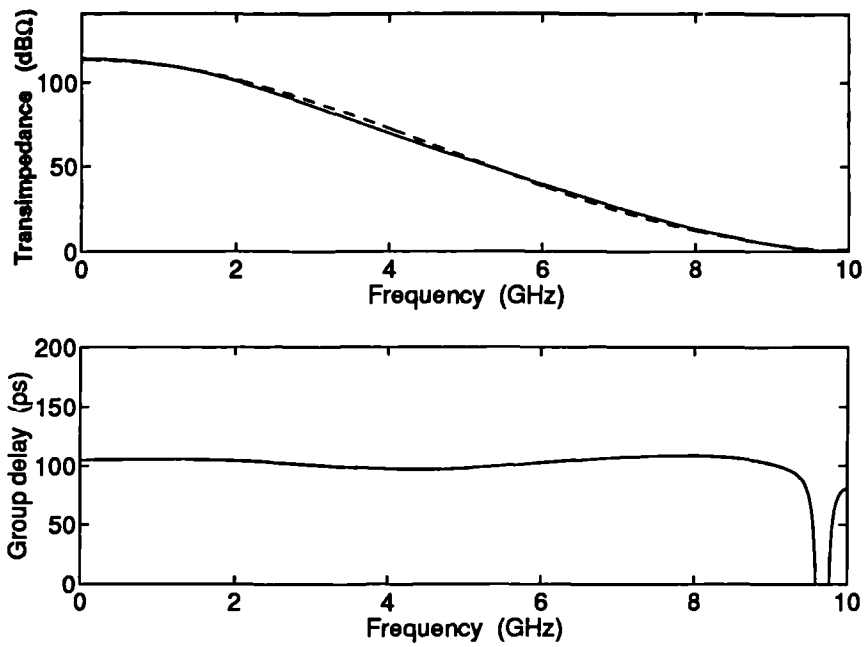

Figure 5.15: Raised cosine receiver transimpedance gain and group delay, '——' simulated response, '— · —·' target response

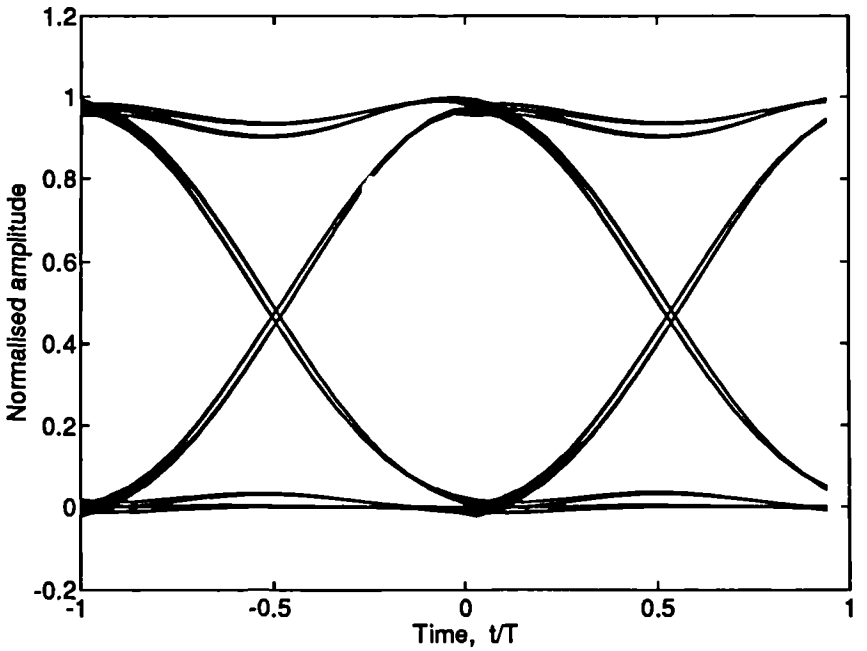

Figure 5.16: Raised cosine receiver simulated eye diagram

high ratios between the maximum and minimum coefficients. For this, the impulse response to be approximated was sampled at instants $\pm 0.5\tau$ and $\pm 1.5\tau$ — avoiding sampling the highest value at $t = 0$ — resulting in the relative gain coefficients $G_{\pm 1} = 1$ and $G_{\pm 2} = 0.27$ when τ is chosen to be 31.06 ps. After circuit optimisation these gain coefficients correspond to FET sizes of $4 \times 100\,\mu$m and $2 \times 84\,\mu$m respectively. The gain blocks were designed as cascode stages. This reduced the loss in the drain line and enabled a higher D.C. gain to be achieved (125Ω) with approximately the same total gate width (1136 μm) as the previous design. The component dimensions used in the simulations are given in table 5.2 and the PIN model is the same as that used in the previous example. Figure 5.17 shows the simulated transimpedance gain and group delay characteristics and the eye-diagram is shown in figure 5.18.

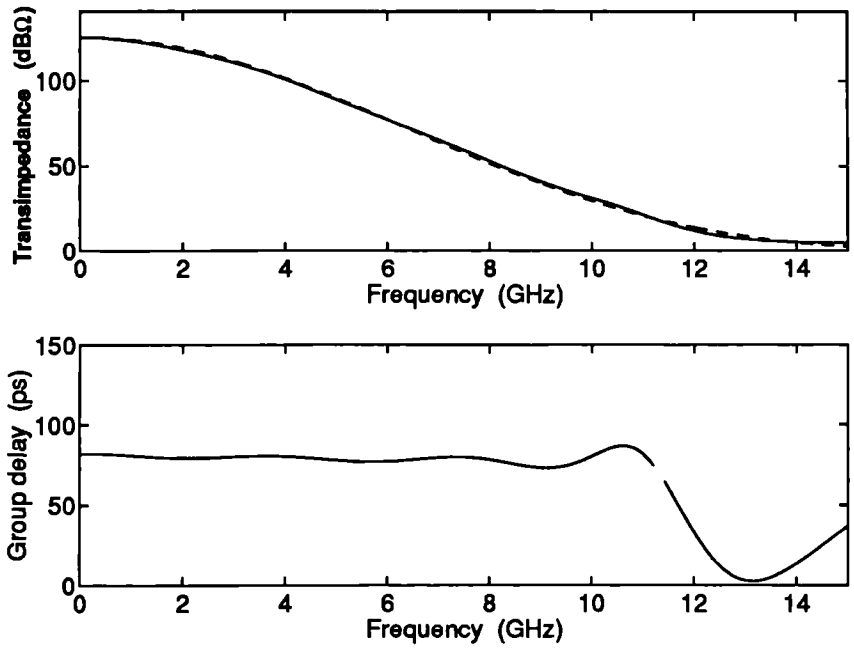

Figure 5.17: New signal design receiver transimpedance gain and group delay, '——' simulated response, '— · —·' target response

For comparison purposes the simulated eye-diagram for the 10 Gbit/s post-detection filter designed in section 4.3 is shown in figure 5.19. As can be seen from figures 5.18 and 5.19, pulse shaping performance comparable with the post-detection filters of the previous chapter is obtained with the distributed amplifier approach.

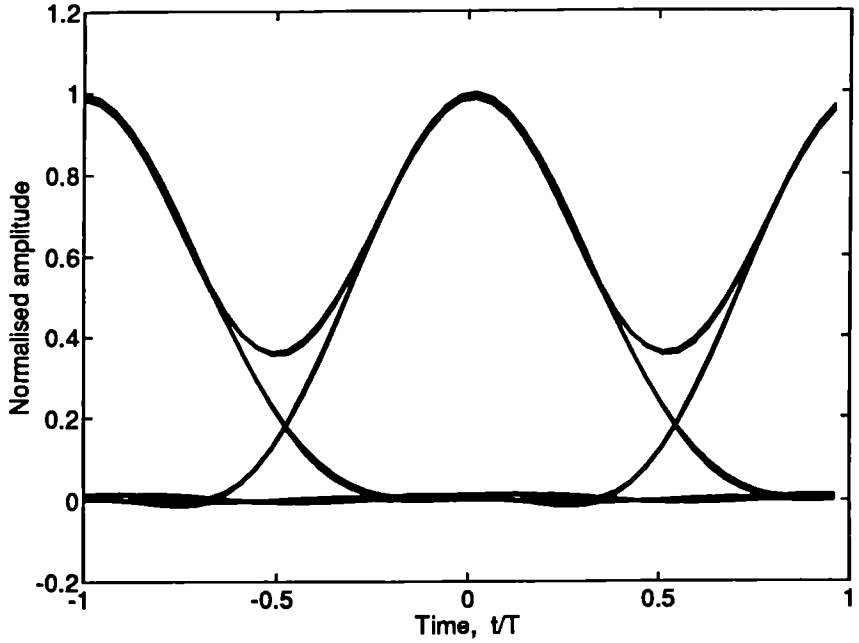

Figure 5.18: New signal design distributed receiver simulated eye diagram

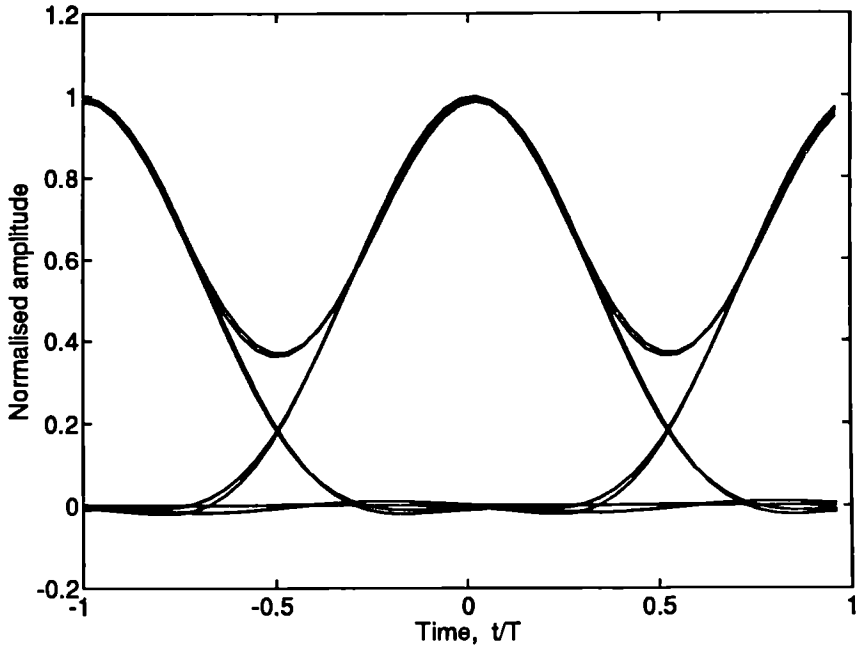

Figure 5.19: New signal design post-detection filter simulated eye diagram

Gain coefficient	$G_{\pm 2} = 0.27$	$G_{\pm 1} = 1$
MESFET (I_d=0.5 I_{dss})	$2 \times 84\,\mu$m	$4 \times 100\,\mu$m
l_g (μm)	159	556
w_g (μm)	10	10
l_g (μm)	81	126
w_g (μm)	30	30
Δ_l (μm)	545	540
Δ_w (μm)	151	151

Table 5.2: New signal design receiver element dimensions

5.3 Summary

In this chapter the possibility of using the distributed amplifier for future very high speed optical communication systems was investigated. The basic principles of operation of the distributed amplifier were reviewed and its operation as an optical receiver has been discussed. A distributed optical receiver design has been presented that achieves a bandwidth of 16.4 GHz with a transimpedance gain of 42.2 dBΩ. These figures represent a bandwidth improvement of five times over the designs presented in the previous chapter, which use the same GaAs process foundry. Operation is therefore predicted for bit rates well over 10 Gbit/s. A novel method for operating the distributed amplifier as a transversal filter with gain at microwave frequencies was presented and discussed. Some limitations of a practical nature of the proposed method were identified and possible solutions proposed. Design examples were given that show the practicability of the technique and its particular usefulness in optical systems where pulse shaping is required. The designs discussed are two 10 Gbit/s optical receivers with embedded signal shaping. The first receiver was designed to have a 100% raised cosine frequency roll-off transimpedance while the second implements the pulse shaping function necessary to equalise a rectangular input pulse into a particular case of the new signal designs proposed in chapter 4.3. The results obtained with this receiver were compared with its equivalent GaAs passive realisation, discussed in the previous chapter, showing a very similar pulse shaping performance.

In the next chapter the problem of minimisation of electronic noise generated in optical receivers will be considered.

Chapter 6

Electronic noise minimisation for optical receivers

In this chapter the problem of noise minimisation in optical receivers will be addressed. The most commonly used techniques to reduce circuit noise will be discussed by considering the case of an optical receiver that uses a generic type of noise matching network between the photodiode and the front-end amplifier. The treatment is general and two specific results are derived: First, an expression is given that relates the optical receiver equivalent input noise current spectral density with the familiar microwave description of circuit noise in terms of the parameters F_{min}, Y_{opt} and R_n. Second, the criteria for optimal noise matching in optical receivers are established. The concepts discussed are then applied to the design and optimisation of a noise tuned SCM optical receiver integrated as a GaAs MMIC. The receiver is intended for use in a particular practical system and includes an integrated noise matching network [117, 118, 119]. A critical study of tuning networks suitable for integration is undertaken and the details of the design and optimisation strategy for such networks are discussed. Simulation results predict low noise and high gain performance, and verify the validity of the design technique adopted.

6.1 Noise matched receivers

In chapter 2 receiver optimisation was couched in terms of choosing the optimum impulse response leading to the minimum BER for a given optical power. Both in the classical [11, 120] and in the MCB-based approach [46, 47] electronic receiver noise is considered to be a Gaussian random variable with variance given by

$$\sigma_c^2 = \int_{-\infty}^{\infty} S_{eq}(f) \mid H_T(f) \mid^2 df \tag{6.1}$$

that should ideally be minimised to optimise the receiver sensitivity. This variance can be minimised by the appropriate choice of $H_T(f)$. However, not only noise but also ISI, tolerance to jitter and so ultimately sensitivity depend on the receiver impulse response $h_T(t)$ and it is thus not possible to choose $H_T(f)$ based solely on noise considerations. Nonetheless, the value of σ_c^2 can be also minimised by using appropriate circuit techniques to reduce the value of the power spectral density $S_{eq}(f)$ of the equivalent input noise current. Some of the well-known design solutions that can be used to reduce the noise generated in the optical receiver include the following

- selection of the best circuit configuration;
- careful selection of the active devices;
- selection of the optimum bias conditions for the active devices;
- use of a noise matching network.

All these solutions can be discussed in a unified manner by considering the general case of an optical receiver that uses a noise matching network between the photodiode and the front-end. The concept of noise matching for optical receivers was first proposed by Hullet and Muoi [121] who showed that an inductance in series with the front-end input can improve the receiver's noise performance. The concept has been adopted for very high bit rate optical receivers [122] where more complex noise matching networks have been used to produce the lowest equivalent input noise current spectral densities reported [16, 123, 124]. The generic noise model of an optical receiver employing a noise matching network is represented in figure 6.1. Here I_p is the signal current, N is a two port network that without loss of generality represents the photodiode equivalent circuit (excluding the signal current source), the noise matching network and the photodiode bias network, e_1

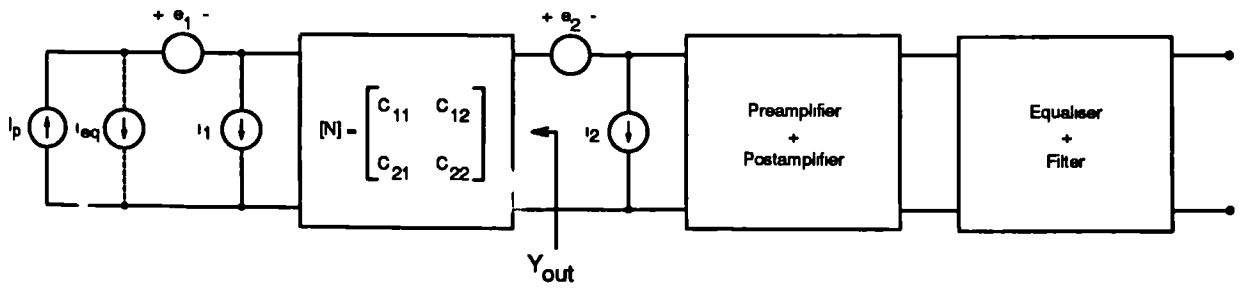

Figure 6.1: Optical receiver noise model

and i_1 are the noise sources that characterise the noise behaviour of the network N while e_2 and i_2 characterise the noise behaviour of the active part of the optical receiver. The noise sources e_2, i_2, e_1 and i_1 can be replaced by two equivalent noise sources e and i at the input of the network N. In the analysis, all the noise sources will be considered to be characterised by their correlation matrices, as discussed in chapter 3, and the chain-matrix will be the adopted representation [68] unless otherwise stated. Noise sources e_2, i_2 can be referred to the input and their effect lumped with that of noise sources e_1 and i_1 using the transformation (equation (3.43) in chapter 3)

$$\mathbf{C}_c = \mathbf{C}_{c1} + \mathbf{N}\,\mathbf{C}_{c2}\,\mathbf{N}^{\dagger} \tag{6.2}$$

with

$$\mathbf{C}_c = \begin{bmatrix} \frac{d}{df}\langle ee^* \rangle & \frac{d}{df}\langle ei^* \rangle \\ \frac{d}{df}\langle e^* i \rangle & \frac{d}{df}\langle ii^* \rangle \end{bmatrix} \tag{6.3}$$

$$\mathbf{N} = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} \tag{6.4}$$

$$\mathbf{C}_{c1} = \begin{bmatrix} \frac{d}{df}\langle e_1 e_1^* \rangle & \frac{d}{df}\langle e_1 i_1^* \rangle \\ \frac{d}{df}\langle e_1^* i_1 \rangle & \frac{d}{df}\langle i_1 i_1^* \rangle \end{bmatrix} \tag{6.5}$$

$$\mathbf{C}_{c2} = \begin{bmatrix} \frac{d}{df}\langle e_2 e_2^* \rangle & \frac{d}{df}\langle e_2 i_2^* \rangle \\ \frac{d}{df}\langle e_2^* i_2 \rangle & \frac{d}{df}\langle i_2 i_2^* \rangle \end{bmatrix} \tag{6.6}$$

where, $\mathbf{C}_c$ is the correlation matrix of the total network, $\mathbf{C}_{c1}$ and $\mathbf{N}$ are, respectively, the correlation and chain-matrix of the noise matching network and $\mathbf{C}_{c2}$ is the correlation matrix of the amplifier. Both noise source e and i can be further lumped together into the equivalent input noise current i_{eq}. However, since the signal current source I_p effectively represents an open circuit to the voltage noise source e, the equivalent input noise current i_{eq} is simply equal to i. Then, from equation (6.2) the noise spectral density of the equivalent input noise current i_{eq} is given by

$$S_{eq}(f) = \frac{d}{df}\langle i_{eq} i_{eq}^* \rangle = \frac{d}{df}\langle ii^* \rangle \tag{6.7}$$

with

$$\frac{d}{df}\langle ii^* \rangle = \frac{d}{df}\langle i_1 i_1^* \rangle + \mid c_{21} \mid^2 \frac{d}{df}\langle e_2 e_2^* \rangle + 2\,\mathrm{Re}\left(c_{21} c_{22}^* \frac{d}{df}\langle e_2 i_2^* \rangle \right) + \mid c_{22} \mid^2 \frac{d}{df}\langle i_2 i_2^* \rangle \tag{6.8}$$

In this equation the first term can be recognised as the noise power spectral density generated by the noise matching network (including the photodiode and bias circuit) while the remaining terms correspond to the noise power and cross correlation spectral densities due to the amplifier and transformed by the presence of the network N.

6.1.1 Front end selection

Although the other elements of the total correlation matrix $\mathbf{C}_c$ in equation (6.2) are not directly relevant to the calculation of $S_{eq}(f)$ they can provide insight into the question of selection of the best front-end configuration from the point of view of noise. That is, in equation (6.2) the input network can be thought of as the first amplifier stage with chain-matrix N and noise correlation-matrix $\mathbf{C}_{c1}$, while $\mathbf{C}_{c2}$ is the noise-correlation matrix of the following amplifier stages. The merits of a given front-end topology must be then evaluated under two criteria: First, the contribution of the stage itself to the receiver noise, i.e. the magnitude of the elements of $\mathbf{C}_{c1}$ must be considered. Secondly, the capacity of the stage to reduce the contribution of the following stages to the total receiver noise must be taken into account. It is a widely known result that for the three possible configurations — common-source (CS), common-drain (CD) and common-gate (CG) — the magnitude of the elements of the noise-correlation matrix ($\mathbf{C}_{c1}$) are almost equal [87, 125, 126]. Accordingly, the choice between the three circuit configurations has to be based on the second criterion, the ability of the circuit to minimise the noise contribution of the subsequent amplifier stages. As given by equation (6.2) the matrix $\mathbf{C}_{c2}$ when referred to the input of network N is transformed by its chain parameters and each element of the transformed matrix is a weighted sum, by the elements of N, of the original elements of $\mathbf{C}_{c2}$. Since the CS configuration has the largest transfer parameters — or equivalently, the smallest chain parameters — it should thus be selected as the front-end stage whenever the best noise performance is to be achieved. On the other hand the CG configuration has the smaller transfer parameters of the three configurations and is thus the least efficient in reducing the noise contribution of the subsequent stages [87, 125].

6.1.2 Optimum noise matching

Returning now to equation (6.8) and assuming that the noise contribution of the subsequent amplifying devices is minimised by proper selection and design of the first stage it is usually

a good approximation to consider the photodiode, the noise matching network N and the front-end device as the dominant noise sources in the circuit. In this case, the noise terms involving noise generators e_2 and i_2 in figure 6.1 can be considered to be due to the first active device only. As discussed in chapter 3, the power and cross-correlation spectral densities of these generators can be related with the device noise parameters by [68]

$$\mathbf{C}_{c2} = 2\,k\,\theta_0 \begin{bmatrix} R_n & \frac{(F_{min}-1)}{2} - R_n Y_{opt} \\ \frac{(F_{min}-1)}{2} - R_n Y_{opt}^* & R_n \mid Y_{opt} \mid^2 \end{bmatrix} \tag{6.9}$$

where θ_0 is the standard reference temperature ($\theta_0 = 290\,\mathrm{K}$), R_n is the noise resistance, Y_{opt} is the optimum source admittance and F_{min} is the minimum noise factor. If the power and cross-correlation spectral densities, as expressed by equation (6.9), are replaced in the equation (6.8), this equation can now be rewritten as

$$S_{eq}(f) = \frac{d}{df}\langle i_1 i_1^* \rangle + 2\,k\,\theta_0 \mid c_{22} \mid^2 \left[R_n \mid Y_{out} - Y_{opt} \mid^2 + (F_{min} - 1)\ \mathrm{Re}(Y_{out}) \right] \tag{6.10}$$

where $Y_{out} = c_{21}/c_{22}$ is the output admittance of the network N. Since the noise matching network is passive the first term in equation (6.10) can be computed from its **Z** or **Y** matrix. Assuming that the two-port **Z**-matrix of the network N is defined — as is generally the case due, at least, to the presence of the shunt photodiode capacitance — then its correlation matrix in the chain representation is given by (equations (3.50) and (3.44) in chapter 3)

$$\mathbf{C}_{c1} = 2\,k\,\theta\,\mathbf{T}\,\mathrm{Re}(\mathbf{Z})\,\mathbf{T}^\dagger \tag{6.11}$$

where θ is the network temperature and **T** is the transformation matrix between the impedance and the chain representations given in table 3.1. From this:

$$\frac{d}{df}\langle i_1 i_1^* \rangle = 2\,k\,\theta \mid c_{21} \mid^2 \mathrm{Re}(z_{22}) \tag{6.12}$$

Since $z_{22} = Z_{out} = 1/Y_{out}$ and $Y_{out} = c_{21}/c_{22}$ equation (6.12) can be rewritten as:

$$\frac{d}{df}\langle i_1 i_1^* \rangle = 2\,k\,\theta \mid c_{22} \mid^2 \mathrm{Re}(Y_{out}) \tag{6.13}$$

Finally, by substituting (6.13) in (6.10), the optical receiver equivalent input noise current power spectral density is

$$S_{eq}(f) = 2\,k\,\theta_0 \mid c_{22} \mid^2 Y_N(f) \tag{6.14}$$

where $Y_N(f)$ will be defined here as the equivalent noise admittance of the total network and is given by:

$$Y_N(f) = \frac{\theta}{\theta_0}\mathrm{Re}(Y_{out}) + R_n \mid Y_{out} - Y_{opt} \mid^2 + (F_{min} - 1)\ \mathrm{Re}(Y_{out}) \tag{6.15}$$

From equations (6.14) and (6.15) the criteria for optimum noise matching can now be derived. These equations indicate that the equivalent input noise current spectral density can be reduced by maximising the current gain factor $1/c_{22}$ and by minimising the optical receiver equivalent noise admittance $Y_N(f)$. The noise admittance (6.15) is a function of the output admittance of the noise matching network N and as such its value can be minimised by proper design of Y_{out}. If Y_{out} is written as $Y_{out} = G_o + \jmath X_o$ then its optimum value can be obtained by solving the equations

$$\frac{\partial}{\partial G_o} Y_N(f) = 0 \tag{6.16}$$

$$\frac{\partial}{\partial X_o} Y_N(f) = 0 \tag{6.17}$$

for G_o and X_o. From these equations the optimum admittance is

$$G_o = \mathrm{Re}(Y_{opt}) + \frac{1}{2\,R_n}\left[1 - \frac{\theta}{\theta_0} - F_{min}\right] \tag{6.18}$$

$$X_o = \mathrm{Im}(Y_{opt}) \tag{6.19}$$

These show that — contrary to what as been suggested in references [123, 127] — the optimum noise matching admittance for optical receivers differs from the optimum noise figure matching that requires $Y_{out} = Y_{opt}$. It should be noticed, however, that for the most common devices, equation (6.18) may lead to a negative real part of the optimum admittance contradicting the realisability condition for a passive network. Nonetheless, equations (6.18) and (6.19) correspond to a single minimum of $Y_N(f)$ and whenever G_o as given by equation (6.18) becomes negative the optimum noise matching condition for optical receivers can be restated as

$$G_o = 0 \tag{6.20}$$

$$X_o = \mathrm{Im}(Y_{opt}) \tag{6.21}$$

with corresponding minimum equivalent noise admittance:

$$Y_N(f) = R_n\,\mathrm{Re}(Y_{opt})^2 \tag{6.22}$$

It is interesting to notice that this corresponds to the widely used high impedance approach [32, 128, 11] to receiver noise minimisation plus an additional condition that states that

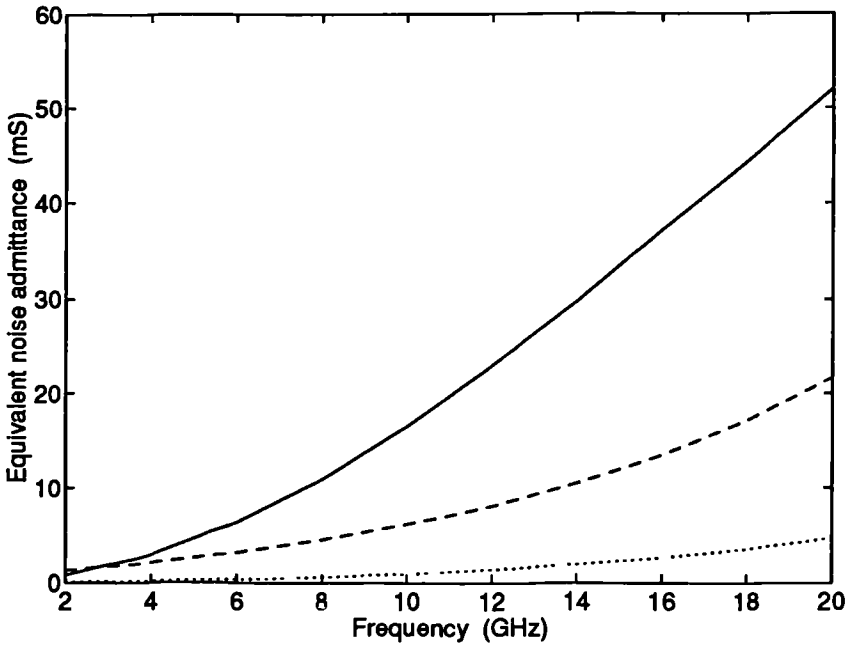

Figure 6.2: Equivalent noise admittance for three matching situations: ('——') no matching, ('– – –') matching to Y_{opt} and ('·····') matching to $\jmath\,\mathrm{Im}(Y_{opt})$

the front-end should see an admittance $Y_{out} = \jmath\,\mathrm{Im}(Y_{opt})$. Figure 6.2 represents the equivalent noise admittance $Y_N(f)$ for the GaAs foundry $4 \times 75\,\mu$m MESFET in three idealised matching situations: with no matching ('——'), with matching to Y_{opt} ('– –') and with matching to $\jmath\,\mathrm{Im}(Y_{opt})$ ('···'). It can be observed from this figure that, although matching to Y_{opt} provides already an improvement when compared with the no-matching case, matching to $\jmath\,\mathrm{Im}(Y_{opt})$ further reduces the value of the equivalent noise admittance $Y_N(f)$. As mentioned before, minimisation of $S_{eq}(f)$ amounts to the simultaneous maximisation of the current gain factor $1/c_{22}$ and minimisation of $Y_N(f)$. However, these are interrelated and consequently Y_{out} and c_{22} cannot be chosen independently. The choice of the optimum set of the chain parameters for the matching network is thus best done numerically by solving the constrained optimisation problem

$$\min\left\{\sigma_c^2 = \int_{-\infty}^{\infty} S_{eq}(f) \mid H_T(f) \mid^2 df\right\} \tag{6.23}$$

subject to the constraints

$$\mid Y_{out} - \jmath\,\mathrm{Im}(Y_{opt}) \mid < \varepsilon \qquad \text{with} \qquad Y_{out} = \frac{c_{21}}{c_{22}} \tag{6.24}$$

$$\mathrm{Re}(c_{12})\,\mathrm{Re}(c_{22}) + \mathrm{Im}(c_{12})\,\mathrm{Im}(c_{22}) \geq 0 \tag{6.25}$$

$$\mathrm{Re}(c_{11})\,\mathrm{Re}(c_{12}) + \mathrm{Im}(c_{11})\,\mathrm{Im}(c_{12}) \geq 0 \tag{6.26}$$

$$\mathrm{Re}(c_{12})\,\mathrm{Re}(c_{21}) + \mathrm{Im}(c_{11})\,\mathrm{Im}(c_{22}) \geq 0 \tag{6.27}$$

where (6.24) allows a certain deviation from the optimum matching condition to accommodate for losses in the matching network and the photodiode parasitics, while constraints (6.25) to (6.26) ensure that the matching network is realisable[1] [129]. Once the optimum set of the chain parameters is determined a network can be designed that approximates the desired response. Alternatively, a circuit topology can be chosen at the outset and its elements optimised to provide close to optimum noise matching over the frequency range of interest. This is the most common approach used in the literature with the exception of references [123, 127] where a matching network was designed to realise the minimum noise figure matching condition $Y_{out} = Y_{opt}$ and it will be used in the next section for the noise optimisation of an analogue receiver for subcarrier multiplexed applications.

6.1.3 Active device selection and optimum bias conditions

The problem of selecting the optimum device and its optimum bias condition is probably the most complex one and can be approached from the device design view point [130, 131, 132]. However, the circuit designer is normally faced with a limited choice of technologies and devices. In this case, equation (6.15) can guide the designer selection. For instance, in situations where optimum noise matching can be realised, equation (6.15) indicates that devices and bias conditions leading to the lowest values of $R_n\,\mathrm{Re}(Y_{opt})^2$ should be selected while, for example, in a high impedance approach where the optimum noise matching condition is not satisfied a low value of R_n should be preferred.

[1] Here it is assumed that the noise matching is not significantly affecting the gain of the first stage at any frequency within the range of interest. If this is not so, then either condition (6.24) has to be relaxed and a multi-objective optimisation strategy adopted that will insure that the first stage gain does not drop below a certain level or, alternatively, the noise of subsequent stages must be considered in equation (6.15). Under such circumstances the noise parameters in this equation represent the first and subsequent stages — and not only the first stage as is being assumed here.

6.2 SCM GaAs receiver with integrated tuning network

Over the past few years there has been an increased interest in developing efficient systems suitable for multichannel broadband services [133]. One of the more popular strategies proposed for distribution of such services to a high number of users is the subcarrier multiplexed (SCM) lightwave scheme. In SCM systems, each channel modulates a separate microwave subcarrier. All the subcarriers are then linearly added and the resulting signal modulates an optical carrier. Direct detection is generally employed at the receiver to recover the multiplexed signals, then standard microwave techniques can be used to select a required channel. SCM systems have been extensively studied [134, 14, 135] with successful laboratory demonstrations [136, 137] and field trials for video distribution [138] reported. For such systems to be widely used, reliable, economic, and easily producible system components have to be made available. For systems operating at frequencies in the GHz region, receiver implementation as a microwave monolithic integrated circuit (MMIC) will satisfy the requirements of reliability and reproducibility and will be economically competitive when compared to its discrete or hybrid equivalent. In this section the design of a narrow-band SCM tuned receiver, integrated with its noise tuning network as a GaAs MMIC, is discussed. The design is optimised to operate over the frequency range 1.8–2.2 GHz. Different tuning networks are examined and their performance optimised under the constraints imposed by practical implementation aspects of the GaAs process used. The noise optimisation method used is described and simulation results of the receiver's noise and frequency response are presented.

6.2.1 Noise tuning networks

Several types of tuning network have been examined in the literature for broadband [122], coherent [139] and SCM [15] optical receivers. Since SCM receivers are usually restricted to narrow-band operation [15] a wide choice of low-pass and band-pass networks can be used to realise noise matching of the front-end over the frequency range of operation [139, 140]. The most common topologies used for such applications are inductive parallel and serial tuning [15], T and Π tuning [139]. The microstrip T-equivalent of transformer tuning has also been used [141], however this type is not suitable for integration in the low GHz frequency range where the quarter wave length in GaAs exceeds 10 mm. Consequently,

only the first four types of tuning network will be considered here for integration with the receiver.

Before the tuning networks can be analysed in detail it is necessary to consider how the GaAs element non-idealities affect the four basic topologies. This can be done by considering the equivalent circuit models of the GaAs inductors and capacitors which are the basic building blocks of the tuning networks. These models were discussed in detail in chapter 3 and are capable of modelling the behaviour of the GaAs capacitors to frequencies in excess of 20 GHz and the GaAs inductors up to 80% of their s_{21} resonant frequency, which for the largest allowed planar inductor is 8 GHz. These models are, however, too complex to be useful in a first analysis and will be replaced by the simplified models shown in figures 6.3 and 6.4. These simplified models were obtained from the original ones (figures 3.5 and

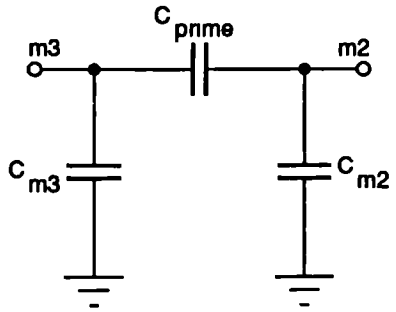

Figure 6.3: Simplified GaAs capacitor equivalent circuit

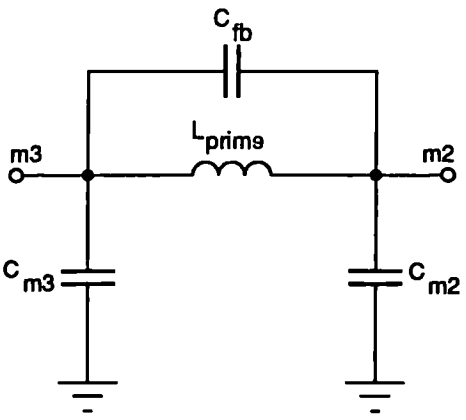

Figure 6.4: Simplified GaAs inductor equivalent circuit

3.7 in chapter 3) by neglecting the losses in both components and the parasitic inductances associated with the bottom and top plates of the MMIC capacitors. Their affects can be taken into account at a later stage using a numerical or circuit simulation program.

Figure 6.5 shows the simplified GaAs equivalent circuits for the shunt, series, T and Π tuning networks when the ideal capacitors and inductors in these networks are replaced by the GaAs models in figures 6.3 and 6.4. In figures 6.5 a) and d) the shunt parasitic capacitances of the GaAs inductors at the input and output ports were excluded from the tuning network and in the analysis they will be considered as being part of the photodiode and amplifier input capacitance respectively. In this way, each branch in the tuning network can be considered as a parallel combination of an ideal inductor and capacitor which in the

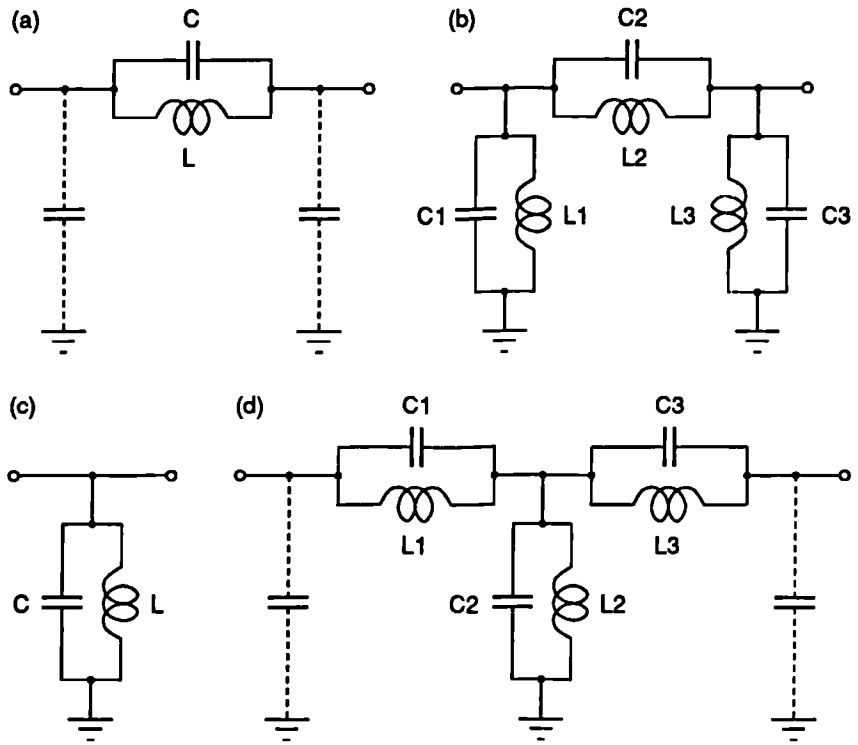

Figure 6.5: Simplified models for the GaAs implementation of: (a) Series tuning, (b) Π tuning, (c) shunt tuning and (d) T tuning

analysis will be considered as the tunable elements. In a practical implementation each of these elements can be replaced by a combination of GaAs components, including its parasitics.

The equivalent input noise spectral density $S_{eq}(f)$ can be now calculated for an optical receiver which uses any one of the four tuning networks in figure 6.5 with help of equation (6.8). To derive the specific equations for each of the tuning networks it will be further assumed that there is no thermal noise generated in the photodiode and that its equivalent circuit consists only of the junction capacitance. In this case, since the tuning networks are considered to be lossless, the first term in equation (6.8) is zero. The other terms in this equation are, however, non zero and $S_{eq}(f)$ for the four networks of figure 6.5 can be expressed as:

$$S_{eq}(f) = |A|^2 \left[|B|^2 \frac{d}{df}\langle e_2 e_2^* \rangle + 2\,\mathrm{Re}\left(B^* C \frac{d}{df}\langle e_2 i_2^* \rangle \right) + |C|^2 \frac{d}{df}\langle i_2 i_2^* \rangle \right] \tag{6.28}$$

For the series and Π-network

$$A = \frac{1}{Z_1 Z_3} \tag{6.29}$$

$$B = Z_1 + Z_2 + Z_3 \tag{6.30}$$

$$C = (Z_1 + Z_2)Z_3 \tag{6.31}$$

and for the shunt and T-network:

$$A = \frac{1}{Z_d Z_2} \tag{6.32}$$

$$B = \frac{(Z_d + Z_1)(Z_2 + Z_3) + Z_2 Z_3 + Z_{in}(Z_d + Z_1 + Z_2)}{Z_{in}} \tag{6.33}$$

$$C = (Z_d + Z_1)(Z_2 + Z_3) + Z_2 Z_3 \tag{6.34}$$

In the above equations,

$$\frac{1}{Z_i} = j\omega C_i + \frac{1}{j\omega L_i} \qquad i = 1, 2, 3 \tag{6.35}$$

$$Z_d = \frac{1}{j\omega C_d} \tag{6.36}$$

$$Z_{in} = \frac{1}{j\omega C_{in}} \tag{6.37}$$

where C_d is the photodiode capacitance and C_{in} is the preamplifier input capacitance. For the case of the Π network the capacitances C_1 and C_3 include the photodiode and the preamplifier input capacitance respectively and in the case of series tuning $C_1 = C_d$, $C_3 = C_{in}$.

Equation (6.28) was derived assuming a lossless tuning network and ignoring the thermal noise generated by the bulk resistance of the photodiode. Such assumptions serve to simplify the initial design process and provide a first measure of the effectiveness of each of the tuning networks to minimise the noise generated by the amplifier alone. They can also be used to obtain a first estimate of the values of the GaAs L's and C's to be used in the receiver design by appropriately choosing those element values that minimise the equivalent input noise spectral density $S_{eq}(f)$ as given by equation (6.28). However, to complete the design, detailed noise models that account for all the noise sources in the amplifier, losses in the tuning network and the noise generated in the photodiode itself need to be used. This process of going from equation (6.28) to a full operational noise optimised optical receiver will now be described keeping in mind the specific requirements of SCM systems and the practical limitations imposed by implementation on GaAs. Also, a critical examination of four possible receiver topologies is undertaken through a study of a set of simulation results.

6.2.2 Receiver optimisation

The choice of the optimum component values for a given tuning network depends primarily on the network's ability to maximise the signal to noise ratio (SNR) for all the received channels. It will be assumed here that all the channels are narrow band and that the receiver operation is circuit noise limited. Under these conditions optimisation of a given channel SNR amounts to minimisation of the receiver equivalent input noise spectral density at the channel carrier frequency. Since many of these channels are to be detected and amplified by the receiver, it is important to keep the value of $S_{eq}(f)$ as low as possible over the receiver bandwidth. To achieve this objective the following cost function was selected to control the optimisation process:

$$E = \lambda \cdot D + I \tag{6.38}$$

where, for the tuning range f_{min} to f_{max},

$$I = \frac{1}{f_{max} - f_{min}} \int_{f_{min}}^{f_{max}} S_{eq}(f)\, df \tag{6.39}$$

$$D = \int_{f_{min}}^{f_{max}} |S_{eq}(f) - I|\, df \tag{6.40}$$

and λ is a weighting factor. This cost function constrains the optimiser to find a solution that corresponds to a low mean value of $S_{eq}(f)$ (equation (6.39)) and avoids solutions where some channels might suffer from poor SNR (equation (6.40)) as is the case of trace (b) in figure 6.6.

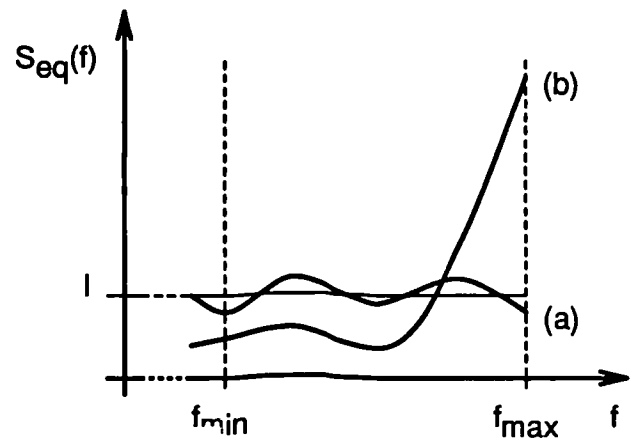

Figure 6.6: Two possible outcomes of $S_{eq}(f)$ optimisation: (a) Conditions set by equations (6.39) and (6.40) considered and (b) Condition set by equation (6.40) ignored

Initially optimisation of the tuning network was carried out for $S_{eq}(f)$, as defined in equation (6.28), with constraints applied to component values limiting them to those allowed by the GaAs process used. At this stage, only the noise contribution of the first MESFET was included. From this initial optimisation stage component values were obtained which were then used for the generation of the initial MMIC layout. Further optimisation was then carried out using a circuit analysis program[2] with full equivalent models used for all GaAs components, accounting for the noise contributions of all the amplifier stages and the thermal noise generated in the tuning network and photodiode. During the optimisation process, the noise models described in chapter 3 and the de-embedded values of P, R and C were used in the numerical simulation of the receiver noise and to calculate the power and cross-correlation spectral densities in equation (6.28).

6.2.3 Simulation results

The optimised input noise equivalent spectral densities for the three stage GaAs receiver preamplifier (described in the next section) when preceded by each of the four types of tuning network are presented in figure 6.7. The corresponding optimised component values are given in table 6.1. For all cases the tuning range was set from 1.6 to 2.4 GHz. This

	Component					
Network	L_1 (nH)	C_1 (pF)	L_2 (nH)	C_2 (pF)	L_3 (nH)	C_3 (pF)
T	5.42	0.08	6.08	0.06	2.75	0.61
Π	12.07	0.11	11.85	0.06	11.48	0.06
Series	12.6	–	–	–	–	–
Shunt	7.34	–	–	–	–	–

Table 6.1: Optimised components values

is wider than the proposed operating range (1.8 to 2.2 GHz). This choice was made to provide a more robust receiver, avoiding the possible exposure of channels located near the band edges to higher noise levels, in case the circuit parameters or the circuit response varied slightly due to process or circuit variations. When no tuning network is used the input noise spectral density varied, over the frequency band of interest, from 7.5 to 9.5 pA/$\sqrt{\text{Hz}}$. However, the use of a tuning circuit reduced this noise to less than 6 pA/$\sqrt{\text{Hz}}$ over the whole optimisation range and to less than 5 pA/$\sqrt{\text{Hz}}$ over the receiver operating range, as

[2]The circuit analysis toolbox described in chapter 3

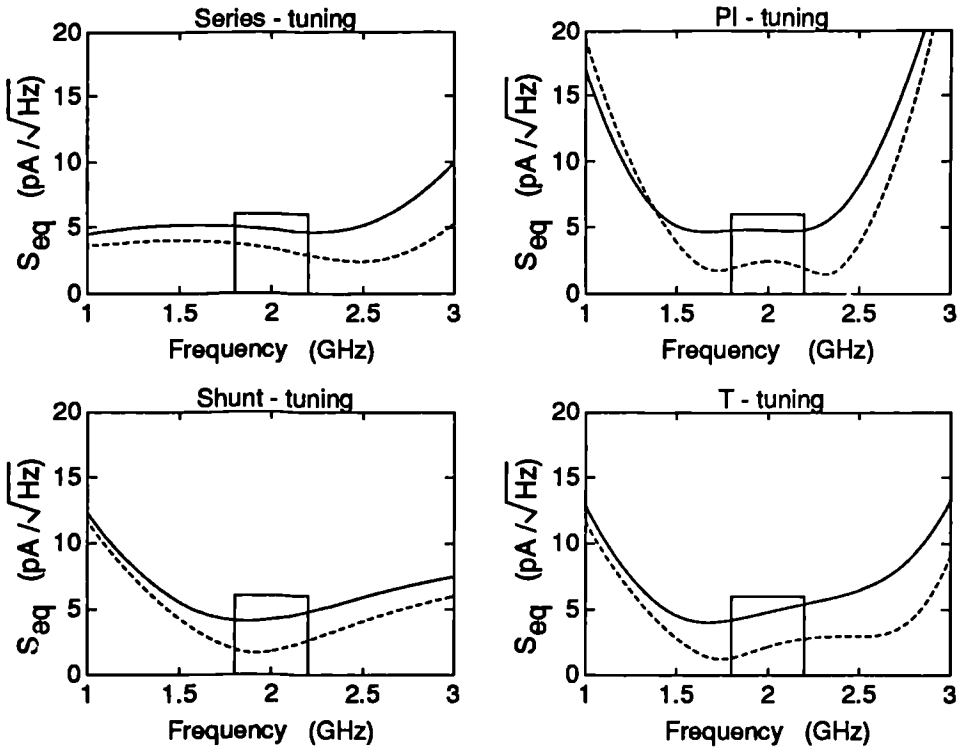

Figure 6.7: Optimised $S_{eq}(f)$ for different tuning networks: '——' full GaAs models and '– – –' equation (6.28)

shown in the graphs. The figures also contrast the results of the two phases of optimisation. From these, it is clear that when ideal components are used, the best results are obtained for the T and Π networks. However, when full GaAs equivalent models are used, these two networks were more severely affected by the process non-idealities than were the simpler series and shunt networks. Also, they show faster rise in noise outside the optimisation range. When comparing the behaviour of the series and shunt tuning networks it can be seen that there is a slight noise advantage for the shunt tuning case. However, the series tuning results display a flatter noise spectral density over the optimisation range.

Figure 6.8 compares the transimpedance gains of the receiver for the different tuning networks. For all cases a midband transimpedance higher than 70 dBΩ is predicted. The series, Π and T networks show reasonably flat gain from 1.8 to 2.2 GHz, while the shunt tuning shows a gain variation of 8 dB.

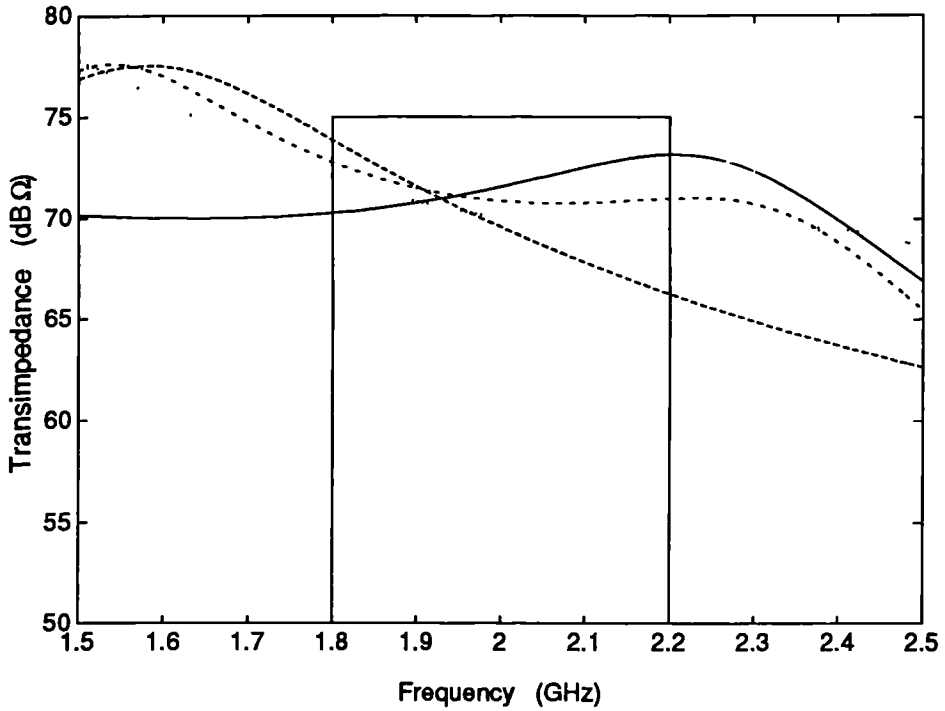

Figure 6.8: Transimpedance gain for different tuning networks: '——' series tuning , '– – –' shunt tuning, '– · –·' Π tuning and '· · ·' T tuning

6.2.4 Practical implementation

The well behaved input noise and transimpedance characteristics of the series tuning, together with its simplicity and small GaAs footprint made it the preferred option for this application. The receiver preamplifier schematic is given in figure 6.9. A 7-turn spiral inductor (L $\simeq$ 12.6 nH) was used as the tuning element. The receiver circuit comprises three amplification stages, each one of them using a 4 × 150 MESFET biased at $0.2\,I_{dss}$ for low noise operation. at the front-end a low noise common source configuration is used, followed by a cascode gain stage. The output stage is common source, providing further gain and with drain load optimised to drive 50Ω impedance. The circuit provides an on-chip bias arrangement for the photodiode. AC coupling is used between the photodiode and the first stage input to improve the dynamic range by preventing possible bias variation due to high input average optical powers, a condition commonly encountered in SCM systems.

The final layout has the dimensions 2 × 3 mm and is shown in figure 6.10. Over the operating range 1.8–2.2 GHz the simulated average noise spectral density is $5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$,

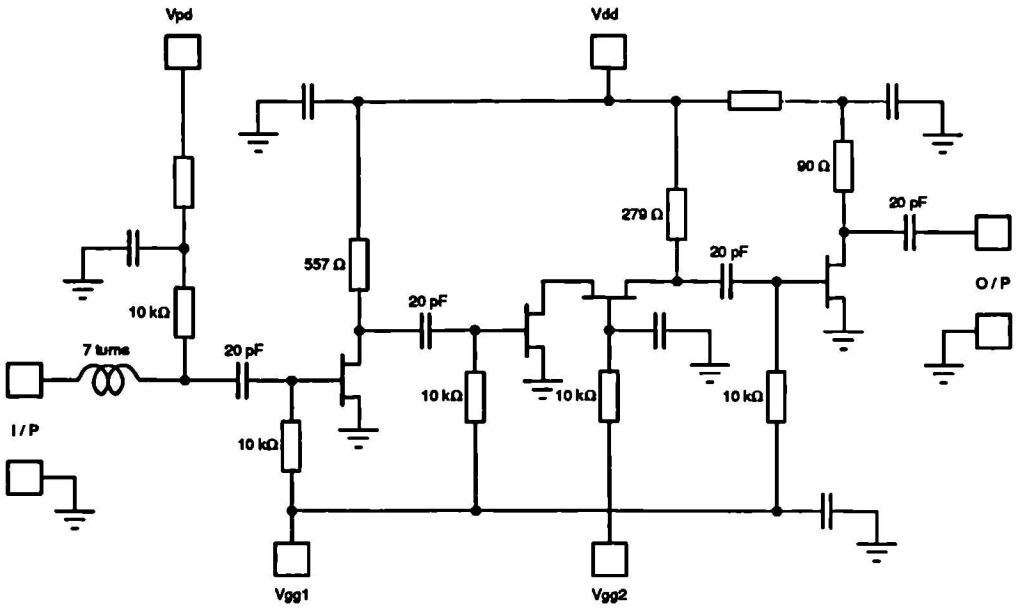

Figure 6.9: Tuned receiver schematic

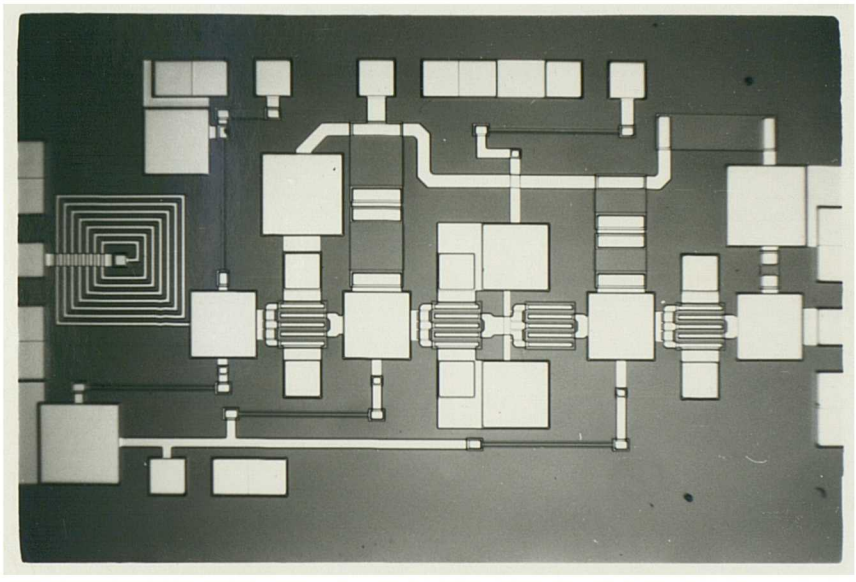

Figure 6.10: Tuned receiver photomicrograph

the transimpedance is $72 \pm 1.5\,\mathrm{dB}\Omega$, and the output VSWR is better than 1.4:1 over the entire operating band, as shown in figures 6.7 and 6.8 in the series tuning case. A PIN with 0.3 pF capacitance and $10\,\Omega$ bulk resistance was assumed for the simulation and optimisation results.

6.3 Summary

In this chapter circuit noise optimisation for optical receivers was considered. A relation was established that allows the optical receiver equivalent input noise current spectral density to be calculated using the noise matching network small signal parameters and the front-end noise parameters F_{min}, Y_{opt} and R_n. From this it was possible to derive the optimum noise matching condition for an optical receiver and it was shown this differs from the optimum matching for minimum noise figure, as has been proposed in recent studies [127].

The problem was explored further in the context of a specific practical realisation and the question of integrating the tuning network and the preamplifier as an MMIC was examined. Four tuning networks, suitable for integration, were identified and equations derived to describe the noise behaviour of optical receivers employing such networks were presented. These equations are primarily used to obtain an initial assessment of the performance of a tuned network and to generate starting values for GaAs implementation. A receiver optimisation strategy suited to SCM applications and constrained by degeneracies associated with MMIC processes was detailed and applied to the four types of tuning network.

Following the design and optimisation strategies developed, an integrated GaAs tuned optical receiver intended for use in a subcarrier multiplex system was designed. This is the first GaAs SCM receiver reported employing an integrated tuning network. The receiver was noise-optimised over the 1.6 to 2.4 GHz range, with simulation results predicting $5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ average input noise and a transimpedance of $72\,\mathrm{dB}\Omega$. The on-chip input tuning arrangement employed makes the receiver easily reproducible, robust and suitable for use in practical systems.

Chapter 7

Preliminary considerations for the realisation of InP OEIC receivers

Chapters 4 to 6 concentrated on the realisation of integrated optical receivers that incorporate intimately some form of signal processing function. The emphasis was on realisation on GaAs since this is now a mature technology with facilities readily available from the GaAs foundry. The GaAs technology possesses, however, some problems for the development of the next generation of telecommunication systems. Firstly, the standard GaAs MESFET technology does not offer the necessary speed capability to fabricate high performance optical receivers operating at 10 Gbit/s[1] and secondly, the integration of electro-optical components compatible with operation in the low-loss optical fibre windows at 1.3 and 1.5 μm is not possible on GaAs. To overcome these problems the semiconductor industry is now turning its attention to optoelectronic integrated circuits (OEICs) based on InP processes that can be used to fabricate optical and optoelectronic components that operate at the optical wavelengths of minimum loss. These processes allow monolithic integration in the same chip of optical, electrical and optoelectronic components, the ultimate goal of such technologies being the integration of fully functional optical receivers and transmitters on the same semiconductor chip. Also, new InP-based device structures have been proposed which suggest that OEIC performance will easily meet the needs of future 10 Gbit/s optical transmission systems [142, 143, 144].

This chapter explores the potential of a still developing InP technology [145] for the construction of 10 Gbit/s OEIC optical receivers. This work has been effected via a collaboration with BT Laboratories and the research activities performed are linked directly

[1]Recourse to a distributed amplifier structure had to be made in chapter 5 to achieve bandwidths compatible with 10 Gbit/s operation but at the expense of poorer noise performance.

to BT's internal requirements. The experimental nature of the InP technology used here constrained the level of complexity of the designs that could be explored, and the lack of a proper characterisation of the process imposes limitations on the accuracy of the design predictions. Consequently, the designs explored in this chapter have the relatively limited design objective of demonstrating 10 Gbit/s operation capability. Two high impedance OEIC receiver designs are proposed for fabrication on the InP process which are capable of achieving that objective. The design and test structures described here have now been transferred to BTL where further development and evaluation will be undertaken within their internal research program.

7.1 The BTL-InP process

Unlike the GaAs foundry described in chapter 3 the InP-based process used in the OEIC receiver designs discussed in this chapter is an experimental process currently being developed at BT Laboratories (BTL). For fabrication of optical receivers the process allows the integration of passive components such as planar inductors, metal-insulator-metal (MIM) capacitors, photodiodes and heterojunction MESFETs (HFETs). The integration structure is vertical, with the epitaxial layers for the HFETs and the photodiodes grown in turn. The passive structures are fabricated on semi-insulating InP. They are fabricated after mesa-isolation and after all epitaxial layers have been etched away as required. The general OEIC structure used in the BTL-InP process is shown in figure 7.1. The brittleness of the indium phosphide substrate prevents the use of through InP vias in the process.

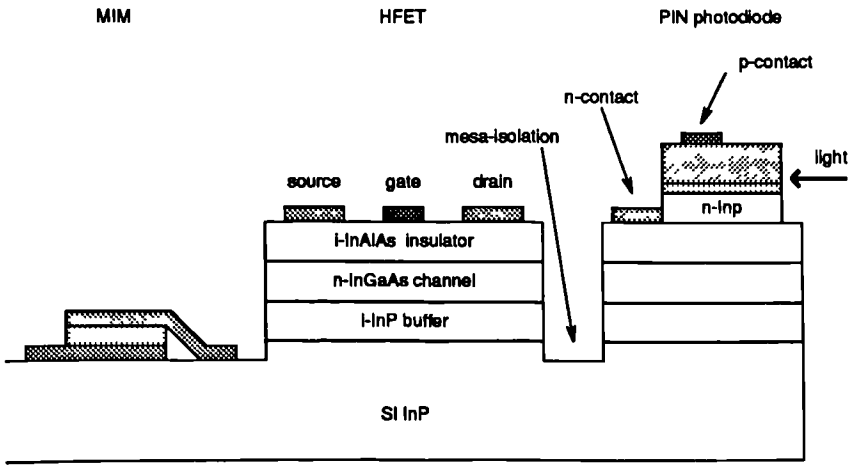

Figure 7.1: General InP OEIC structure

Consequently, a back-face ground plane (if present) can not be used for grounding purposes and any transmission lines in the OEIC must thus be constructed as coplanar waveguide structures [145].

7.1.1 InGaAs doped channel HFETs

The active devices used in the BTL-InP process are heterojunction MESFETs. The channel in these devices is formed by an *n*-doped $In_{0.53}Ga_{0.47}As$ layer. Since InGaAs has superior electron transport properties to GaAs — higher low field mobility and peak velocity [146] — the HFET has superior high frequency performance than the GaAs MESFET. However, metal-InGaAs Schottky diode barrier heights are low ($\simeq 0.3\,eV$) resulting in high gate leakage currents when standard MESFET technologies are used. This is a problem, especially for the fabrication of optical receivers where high leakage currents can contribute significantly to the degradation of receiver sensitivity. To minimise the gate leakage current the use of an insulator layer of undoped higher bandgap semiconductor (*i*-InAlAs) above the InGaAs FET channel was proposed [147]. The BTL-InP HFET uses this type of structure to reduce the gate leakage current. The device is grown on a Fe-doped semi-insulating InP substrate and its detailed layer structure is as shown in figure 7.2 [148]: 300 nm *i*-InP buffer, 10 nm *i*-$In_{0.53}Ga_{0.47}As$ spacer, 8 nm $2 \times 10^{18}\,cm^{-3}$ *n*-type $In_{0.53}Ga_{0.47}As$ channel, 5 nm *i*-$In_{0.53}Ga_{0.47}As$ spacer, 55 nm *i*-$In_{0.52}Al_{0.48}As$ insulator and a 5 nm *i*-InP cap layer. The source and drain ohmic contacts are formed in NiAuGe and the gate is defined in

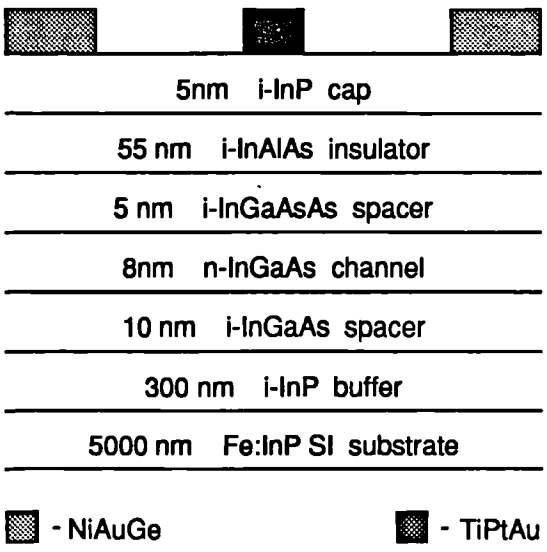

Figure 7.2: Schematic representation of the HFET layer structure

TiPtAu. In the BTL process the *i*-InP cap layer is used to passivate the device. Such devices have been fabricated at BTL with gate lengths of 1, 0.5 and 0.25 μm. The best results for these devices, measured for 100 μm gate width HFETs, are summarised in table 7.1. It is necessary to mention that the measured values of f_T were obtained from a HFET circuit model that includes the parasitic effects of the probing pads, pointing to the possibility of higher f_T figures than those reported here. However, accurate modelling of the probing pads was not available preventing the de-embedding of the devices. These models were, nonetheless, used in the design of the OEIC receivers discussed in the next section. The BTL-InP process uses similar devices to the process reported in [149], where 1.5 μm gate length HFETs were used to fabricate an OEIC receiver that achieved a 3.5 GHz −3 dB bandwidth with a transimpedance gain of 56 dBΩ allowing operation at 6 Gbit/s with a predicted sensitivity of -21.2 dBm.

HFET	1 μm	0.5 μm	0.25 μm
f_T (GHz)	18	32	45
g_m (mS/mm)	237	270	259
$g_m R_{ds}$	12.6	13.1	21

Table 7.1: Measured results for the BTL-InP HFETs

7.1.2 InGaAs edge-coupled PINs

To achieve high speed operation InGaAs edge-coupled (wave guided) PIN photodetectors are used in the BTL-InP process [150]. The device structure is shown in figure 7.3. It uses an InGaAs absorber layer allowing operation at wavelengths up to 1.67 μm. An *n*-InGaAsP

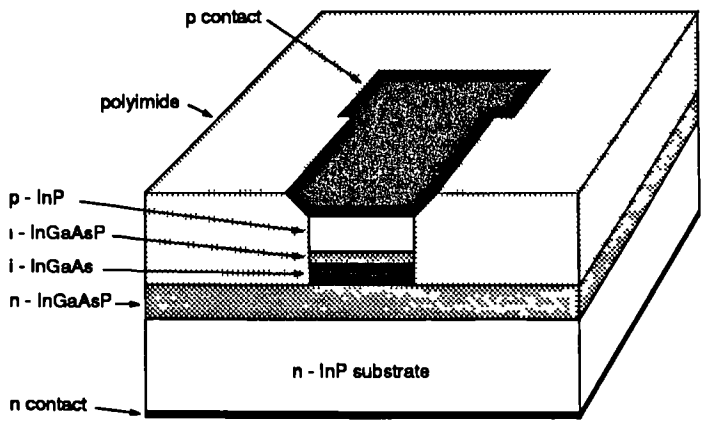

Figure 7.3: Edge-coupled InGaAs PIN structure

optical confinement layer is used between the conducting n-InP substrate and the InGaAs absorber layer to improve the optical coupling efficiency. An InGaAsP layer is also used at the p-side hetero-interface to prevent hole pile-up thereby improving the photodetector frequency response. Finally, a thick layer of polyimide is used to isolate the p-contact metal and minimise its capacitance. The edge-coupled PIN photodiode can overcome some of the limitations of the conventional PIN structures where a tradeoff between internal quantum efficiency and carrier transit time has to be made. For edge-illuminated PINs the thickness of the absorber region has little effect on the internal quantum efficiency provided the absorber region is made long enough. The InGaAs absorber layer can thus be chosen to be thin enough to give negligible carrier transit time while maintaining a high internal quantum efficiency. In this case, the photodiode operation becomes limited by the junction and the metal contact capacitances while the external quantum efficiency is essentially determined by the input coupling efficiency. The junction capacitance can, however, be minimised by having a small junction area while the contact capacitance can be minimised, as discussed before, by using a thick layer of polyimide. Such edge-coupled PINs were reported in [150]. A bandwidth of 50 GHz was achieved with 30 to 40% external quantum efficiency at 1530 nm. A 12 μm radius lens-ended single mode fibre was used for the reported results.

7.2 10 Gbit/s evaluation designs

In this section two OEIC receiver designs are described. These are to be fabricated using the BTL InP-HFET process. The designs are a first step in the evaluation of the potential of the InP-HFET process for the realisation of 10 Gbit/s OEIC receivers for use in future very high speed optical communication systems. Two almost conflicting design requirements were balanced to establish the receiver design criteria. First, the need to satisfy a BTL internal agenda, requiring the realisation of a fully operational 10 Gbit/s OEIC receiver that could be used in system demonstrations, had to be met. The second requirement was the need to keep the receiver design as simple as possible due to the experimental state of the technology and the lack of a proper process characterisation. Based on these two requirements the following design criteria were established. First, the receiver designs should achieve a bandwidth greater than or equal to 8 GHz allowing operation at 10 Gbit/s and accommodating any uncertainties in bandwidth prediction due to inaccurate device

modelling. Second, the receivers should display a transimpedance gain higher than or equal to 40 dBΩ when driving a 50 Ω load impedance and have low ripple in the pass band. Finally, a sensitivity better than -16 dBm was required.

Several designs were explored with two high impedance designs being selected for fabrication. The receivers were designed and simulated using appropriately scaled versions of the equivalent circuit for the 100 μm HFET. Since, for passive devices, no information was available ideal models were used in the design process. To gain some insight into how passive parasitics could affect the performance of the designs, the receivers were also simulated using models for the passive components similar to those used in the GaAs designs. Although this can not give accurate information about the circuit behaviour, due to the different fabrication processes and materials used, it can provide some indication of the tolerance of the designs to circuit non-idealities.

The receiver's sensitivity was also estimated. Since no noise characterisation of the active devices was available a pessimistic prediction of the receivers sensitivity was made using Ogawa's noise model for FETs [40] and the mean square value of the equivalent input noise current was calculated using equation (2.38) [11]

$$\sigma_c^2 = \left[\frac{4\,k\,\theta}{R} + 2\,q\,I_g + \frac{\Gamma}{R^2}\frac{4\,k\,\theta}{g_{mo}}\right] I_2\,B + (2\,\pi\,C_T)^2\Gamma\,\frac{4\,k\,\theta}{g_{mo}}\,I_3\,B^3 \qquad (7.1)$$

where R is the input FET bias resistor, C_T is the sum of the photodiode capacitance with the input FET gate to source capacitance, I_g is the FET input leakage current, g_{mo} is the FET transconductance, Γ is Ogawa's noise factor, B is the bit rate, θ is the temperature, q is the electronic charge and k is Boltzmann's constant. If Ogawa's noise factor is set to $\Gamma = 2$ and the Personick noise integrals are set to $I_2 = I_3 = 1$, equation (7.1) will provide an upper bound on the noise performance of the receiver designs to be discussed, particularly in the case of the second design where the use of inductive peaking in the front-end to extend the bandwidth will almost certainly have a beneficial effect on the receiver noise performance.

7.2.1 Single stage high impedance OEIC receiver

The first design to be considered essentially satisfies the requirement of simplicity. Although a low impedance design would satisfy this requirement the receiver gain and noise performance would fall short of the design criteria, established at the beginning of this section, and therefore a high impedance topology was selected. The InP OEIC receiver

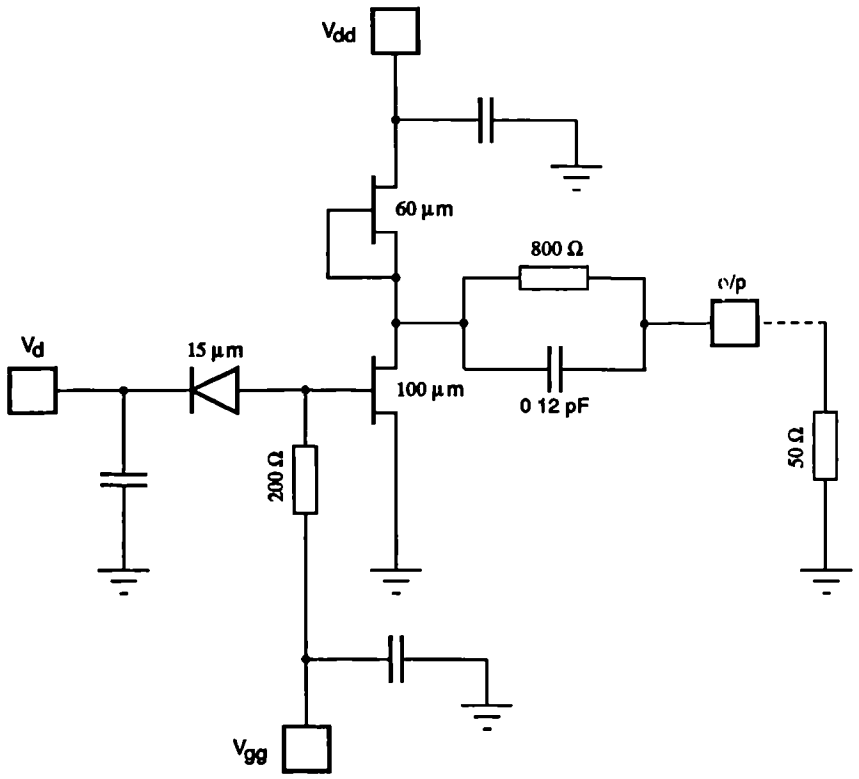

Figure 7.4: Single stage InP OEIC receiver schematic diagram

schematic diagram is shown in figure 7.4. The receiver uses an InGaAs edge-coupled PIN with absorber layer length of 15 μm, corresponding to a photodiode capacitance $C_d = 86$ fF and an estimated external quantum efficiency between 0.3 and 0.4. At a wavelength of 1530 nm these correspond to a photodiode responsivity between 0.37 and 0.49 A/W respectively. A 200 Ω load resistor was used with a 100 μm gate width CS HFET and a 60 μm HFET active load to form the amplifying stage and an equaliser was included to compensate for the input pole at 2 GHz. The two HFETs used in the design have 0.25 μm gate length and the common-source stage was biased at $0.6\,I_{dss}$ for maximum f_T. The simulated frequency response is shown in figure 7.5. Two curves are shown: the solid line corresponds to simulation using ideal passive components while the broken line corresponds to simulation results including estimated parasitics for the passive components as discussed previously. The receiver displays a transimpedance gain of 38 dBΩ and a worst case bandwidth of 6.8 GHz. From noise considerations only, the predicted sensitivities at 10 Gbit/s are -15.8 dBm and -17 dBm for the respective quantum efficiencies of 0.3 and 0.4 at 1530 nm wavelength. Finally, figure 7.6 shows the simulated eye-diagram for NRZ 10 Gbit/s data.

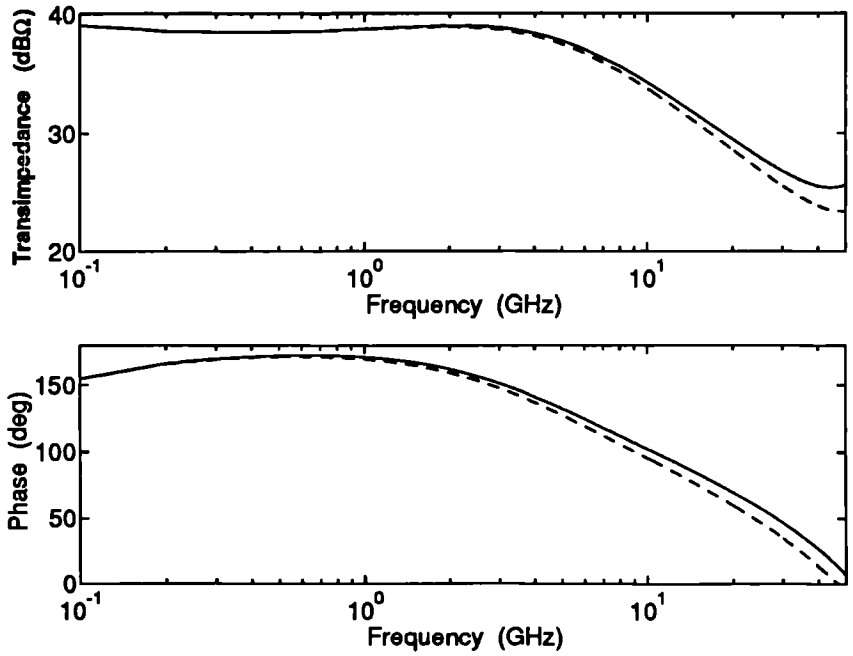

Figure 7.5: Single stage OEIC receiver frequency response: '——' ide al passives components, '– –' passives with added parasitics

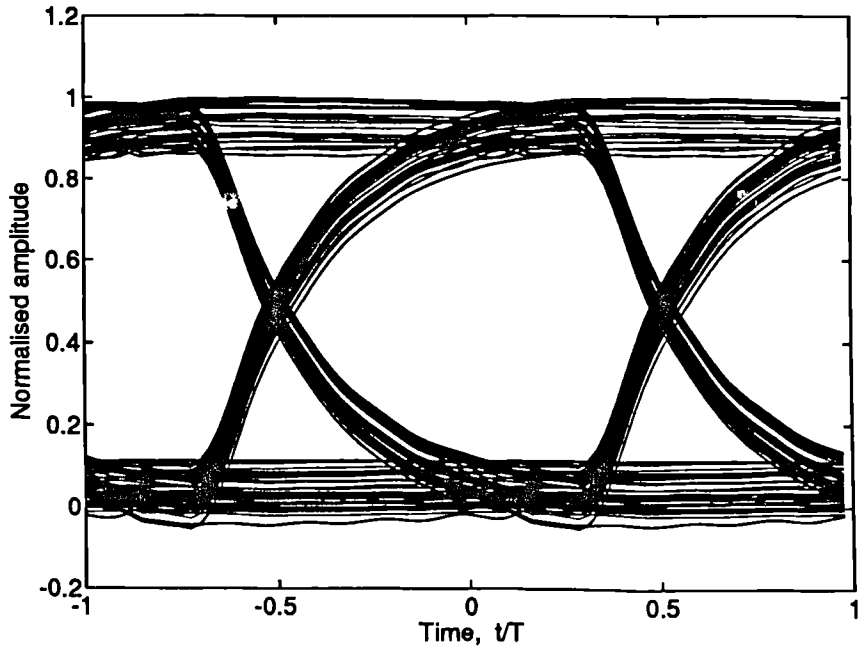

Figure 7.6: Single stage OEIC eye-diagram

7.2.2 Two stage high impedance OEIC receiver

The second OEIC receiver proposed for fabrication is also a high impedance design composed of a CS first stage followed by CD buffer stage (figure 7.7). Inductive peaking of the front-end was used to improve the receiver bandwidth while also allowing an increase in the value of the PIN load resistor to 400 Ω, thereby improving the transimpedance gain and reducing the circuit noise. The use of inductive peaking also allowed the choice of a PIN with a longer absorber layer length (20 μm, C_d = 115 fF) which improves the PIN internal quantum efficiency. As in the previous design, 0.25 μm gate length HFETs were used and the CS and CD devices were biased at 0.6 I_{dss} for maximum f_T. The results of simulation are shown in figures 7.8 and 7.9. The simulation indicates a transimpedance gain of 48 dBΩ and a worst case bandwidth of 10.7 GHz with calculated sensitivities of −16.4 dBm and −17.6 dBm for external quantum efficiencies of 0.3 and 0.4 respectively.

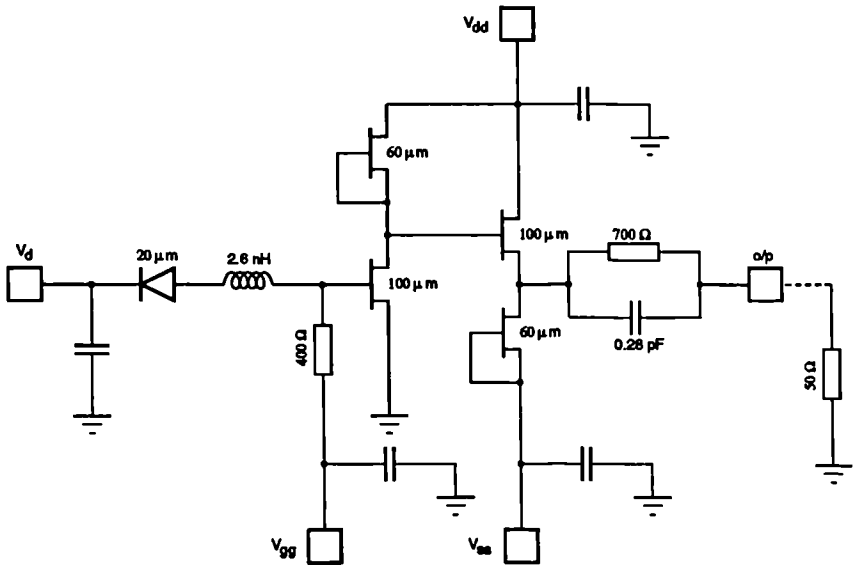

Figure 7.7: Two stage InP OEIC receiver schematic diagram

7.2.3 Test structures

As well as the two receiver designs several test structures were proposed for fabrication. These comprised: PINs of different absorber lengths, HFETs of different gate widths and Schottky diodes of different areas. These will allow further characterisation of these devices and determination of their small signal equivalent circuits as well as the large signal models for the HFETs and Schottky diodes. This will provide the necessary information

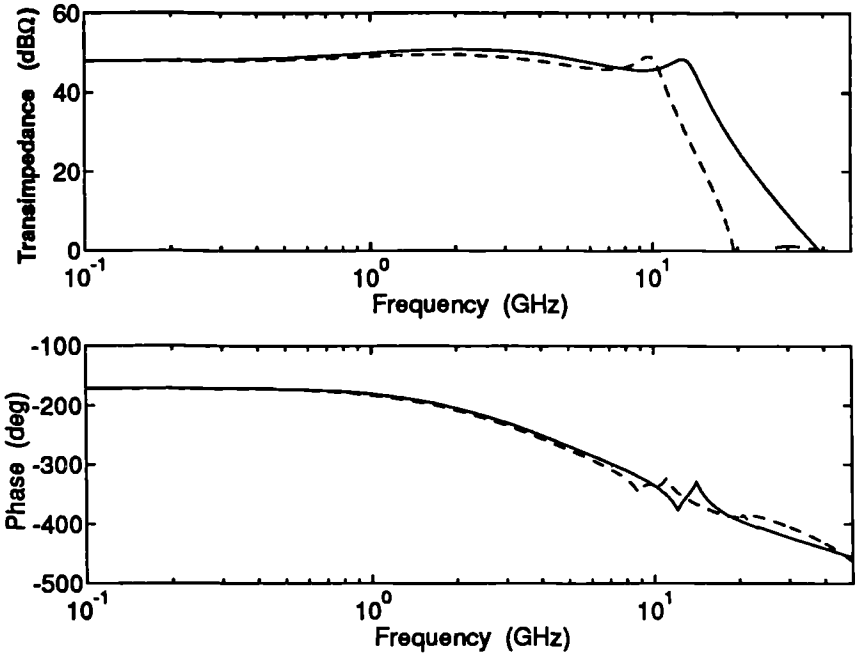

Figure 7.8: Two stage OEIC receiver frequency response: '——' ideal passives components, '– –' passives with added parasitics

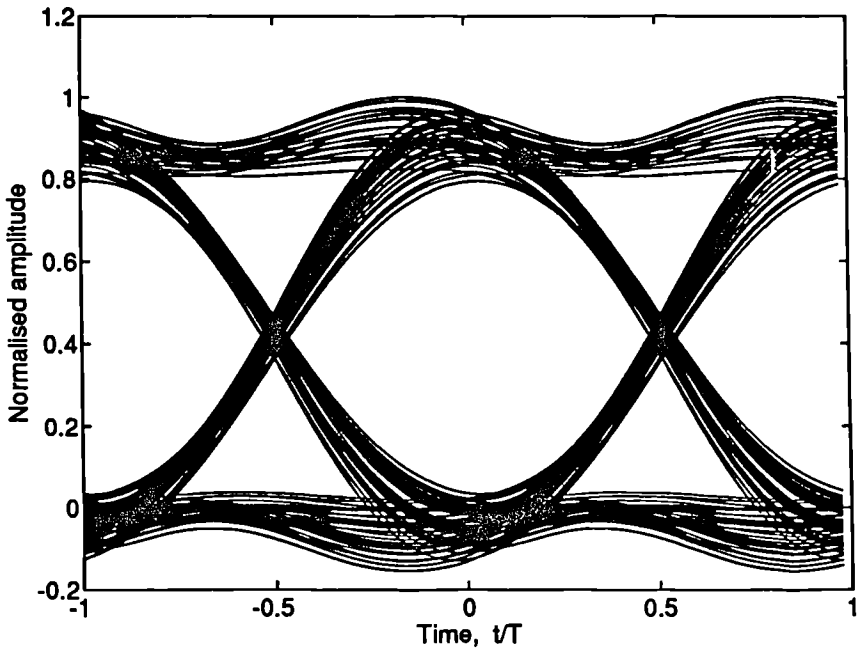

Figure 7.9: Two stage OEIC eye-diagram

for proper scaling of the equivalent circuit component values and parameters in future designs. Other test structures such as a range of resistors, capacitors, inductors and different impedance transmission lines were proposed. This second group of test structures were proposed, not for the purpose of fully characterising the InP process but to evaluate the accuracy of the modelling of passive components with an advanced full field 3-dimensional simulator such as LINMIC™ or Microwave Explorer™ [151, 152, 153]. These simulators use information about the process materials, structure and dimensions of the device being analysed to predict the device *s*-parameters. If the full field simulator accurately models the passive devices, future designs can rely on this approach and to a certain extent direct characterisation of the passive components can be avoided. Finally two sets of test pads were also proposed to allow characterisation and proper de-embedding of the measured *s*-parameters of the test structures.

7.3 Summary

In this chapter the experimental BTL-InP process was briefly described with emphasis on the InP devices used for the implementation of OEIC optical receivers that allow high speed operation, i.e. the edge-coupled PINs and the InGaAs heterojunction MESFETs. The main objective of the chapter was to evaluate the feasibility of optical receiver OEICs operating at 10 Gbit/s fabricated using the BTL-InP process. To achieve this goal, two OEIC receiver designs were proposed. The first is a single stage high impedance receiver with predicted −3 dB bandwidth of 6.8 GHz, transimpedance gain of 38 dBΩ and estimated worst case sensitivity at 10 Gbit/s of −15.8 dBm. The second design is a two stage high impedance receiver that explored the use of inductive peaking to extend the bandwidth while at the same time allowing an increase in the transimpedance gain. The predicted performance for this receiver is 10.7 GHz −3 dB bandwidth, 48 dBΩ transimpedance gain and −16.4 dBm worst case sensitivity. The simulated eye-diagrams for both receivers show that 10 Gbit/s operation is possible. Finally, some test structures were proposed for fabrication that will allow future process characterisation and the check of validity of passive component modelling using 3-dimensional full field simulators.

Chapter 8

Concluding remarks

The primary objective of this thesis has been to identify new signal processing functions for optical receivers that provide tolerance to two major impairments in the currently emerging very high speed optical systems: the strong signal dependent nature of noise due to the use of optical amplifiers in high performance systems; and timing impairments such as sampling and signal jitter which assume particular importance at very high data rates, especially in soliton and optical time division multiplexing systems. After the appropriate signal shaping functions had been derived the thesis focused on proving the feasibility of such signal designs by practical realisation. For this, GaAs monolithic integrated circuit technology was chosen due its maturity, bandwidth compatibility with today's optical systems and readily available foundry facilities. Consideration was also given to noise minimisation techniques in optical receivers for subcarrier multiplex applications. Here, emphasis was given to the integration of the noise reduction network within the optical receiver. Finally, assessment of an experimental InP-based process for the fabrication of 10 Gbit/s optical receiver OEICs was effected.

Chapter 2 started by showing that, although the commonly used raised cosine receiver equalisation is a nearly optimum solution for additive noise dominated systems, it produces receivers unduly intolerant to timing impairments in systems dominated by signal dependent noise. Accordingly, a new class of signals was derived that allows the receiver sensitivity to be optimised while maintaining good tolerance to sampling and signal jitter. The new signals were derived based on strict time domain constraints and on the knowledge that in systems dominated by signal dependent noise optimised sensitivity requires the decision threshold to be set at a low level in the vertical eye opening. It was shown that

this produced signal designs with similar time domain characteristics to those obtained by the more rigorous modified Chernoff bound receiver optimisation technique [47, 48] with a reduction in the design complexity. In this chapter, preliminary considerations concerning realisability issues were also addressed.

The GaAs technology used in the majority of the practical implementations considered in this thesis was described in chapter 3. Noise modelling of the active devices was also considered and a noise de-embedding technique was developed and used in the modelling process of the GaAs foundry MESFETs. The noise models described here were later used in the noise simulations of the active circuit implementations discussed in this work.

In chapter 4 consideration is given to the practical implementation of the signal shaping strategies discussed in chapter 2. The first design described is an APD receiver fabricated as a MMIC and optimised for operation at 4.8 Gbit/s with 50% RZ pulses. The receiver was designed to incorporate the signal shaping necessary to secure optimum noise filtering and jitter tolerant operation according to the modified Chernoff bound criterion. The second signal processing design concerned the realisation of the new signal design equalisers using passive quasi-lumped element GaAs structures and two post-detection GaAs MMIC filters were demonstrated for operation at 10 and 15 Gbit/s. Also, a novel time domain optimisation technique was developed for the accurate design of GaAs post-detection filters and was successfully applied to the optimisation of the above filters. Finally, the concept of true transimpedance receivers was applied to a GaAs MESFET receiver. Such a receiver uses a transimpedance configuration with a low impedance front-end stage to achieve a high degree of insensitivity to photodiode parasitics. In this chapter, the first common-gate transimpedance GaAs MESFET optical receiver was demonstrated and 5 Gbit/s operation was achieved with a sensitivity of better than -13 dBm.

In chapter 5 the use of distributed amplifiers for optical communications was considered. The principles of operation of the distributed amplifier were discussed and its operation as an optical receiver was critically examined. A distributed optical receiver design example was presented that achieves a bandwidth of 16.4 GHz with a transimpedance gain of 42.2 dBΩ clearly suggesting the potential of these structures for operating at bit rates well over 10 Gbit/s. The equivalence between the distributed amplifier and a transversal filter was then identified and it was thus proposed that a modified distributed amplifier may be used as a signal shaping/filtering network for multi-Gbit/s optical systems. To prove the concept two optical receiver designs for operation at 10 Gbit/s with embedded signal

shaping were presented, with one of them realising the signal shaping function necessary to implement a particular case of the new signal designs.

Chapter 6 addressed the problem of circuit noise minimisation for optical receivers. The initial treatment was generic and a relation was derived that allows the optical receiver equivalent input noise current spectral density to be calculated using the noise matching network small signal parameters and the front-end (or amplifier) noise parameters F_{min}, Y_{opt} and R_n. From this it was possible to derive the optimum noise matching condition for an optical receiver which was shown to differ from the previous proposed matching for minimum noise figure [127]. Attention was then focused on the design and optimisation of a noise tuned optical receiver for subcarrier multiplexed systems integrated as a GaAs MMIC. A critical study of tuning networks suitable for integration was undertaken and a mixed analytical/numerical optimisation strategy was proposed for the networks considered. The designed and fabricated receiver was noise-optimised over the 1.6 to 2.4 GHz range and simulation results predict $5\,\mathrm{pA}/\sqrt{Hz}$ average input noise and a transimpedance gain of 72 dBΩ.

Finally, chapter 7 was a first exploration of the potential of a still experimental InP-based process for the construction of 10 Gbit/s OEIC optical receivers. The InP-based process was briefly described and two optical receiver designs were proposed that demonstrate the potential of the technology for the realisation of 10 Gbit/s optical receivers. Both designs are high impedance receivers achieving transimpedance gains of 38 dBΩ and 48 dBΩ with bandwidths of 6.8 GHz and 10.7 GHz respectively.

The work that has been carried out for this thesis led to the identification of several areas that are worthy of further investigation. Some examples are summarised here:

- In this thesis signal designs have been investigated that maximise the receiver tolerance to timing jitter. This may now be combined with signal processing operations aimed at minimising the amount of jitter introduced by the clock recovery circuit to achieve entire receivers which are maximally tolerant to signal timing perturbations. This is especially appropriate for very high bit rate systems and for long haul amplified transmission systems based upon optical solitons for which signal jitter is an inherent performance limiting impairment;

- Distributed amplifier based optical receivers that operate close to the frequency limit

of the technology needs to be further explored. As mentioned in the text, this needs a better understanding of the noise mechanisms in distributed amplifiers so that the amplifier parameters which influence the overall noise performance can be identified and noise optimised designs obtained. Some proposed solutions, such as increasing the gate line (and possibly the drain line) impedance to reduce noise and increase the gain need to be further explored. Also, issues such as the use of input noise matching networks, gate line termination matching [98] and active gate line termination matching [107] should be addressed;

- The proposed concept of active pulse shaping/filtering using a modified distributed amplifier must now be demonstrated experimentally. This concept is expected to become more important as the frequency of operation increases. First, the required effective delay decreases as the bit rate increases, reducing the length of the matched delay lines. This results in compact layouts. Second, at very high frequencies the non-idealities of pseudo-lumped elements become dominant leaving room for either distributed microstrip/coplanar wave guide filters or for the modified distributed amplifier. The latter has the advantage of providing additional gain, which is always at a premium in high frequency systems;

- Further exploration of the BTL InP-based process is clearly needed and for this the following points are of particular importance:

  - A full characterisation of the process including optoelectronic and electrical components should be carried out and results compared to the predictions of a full-field simulator;
  - Development and validation of models for the above components could then follow;
  - A CAD tool capable of integrating in a single software package the design and simulation facilities for both electronic and optoelectronic devices would greatly ease the design process.

- Finally, the development of a high performance OEIC optical receiver operating at 40 Gbit/s is a possibility using the BTL InP-based technology. This could include the use of an SLA-PIN (and possibly an optical filter) combination [154] and a HFET distributed amplifier to achieve the required electrical bandwidth.

In summary, then, the thesis has examined in detail structures and design techniques for the realisation and optimisation of multi-gigahertz optical receivers, novel signal designs and signal processing arrangements have been identified and investigated via realisation as monolithic integrated circuits implemented in GaAs and InP technologies and appropriate ares of further investigation have been indicated.

Appendix A

New class of waveforms for binary optical transmission

As discussed in chapter 2 the following set of time domain constraints are imposed on the signal $h_o(t)$ at the input of the decision circuit

$$h_o(t) = \begin{cases} 1, & t = 0 \\ 0, & t = n \quad \text{and} \quad n \neq 0 \end{cases} \tag{A.1}$$

$$h_o(t) = \begin{cases} 0, & t = (n + 1/2) \quad \text{and} \quad n \neq 0, -1 \\ d, & t = \pm 1/2 \end{cases} \tag{A.2}$$

$$\frac{d\,h_o(t)}{dt} = 0, \qquad t = n \tag{A.3}$$

where n is an integer, d is the normalised value of the decision threshold with $d \in (0, 1/2]$ and the bit period T is normalised to unity. These correspond to: the first Nyquist criterion (A.1); the second Nyquist criterion with respect to the depressed decision threshold d (A.2); and zero signal derivative at the sampling instants (A.3). These constraints on $h_o(t)$ may be expressed concisely as

$$h_o(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - n) = \delta(t - n) \tag{A.4}$$

$$h_o(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - 1/2 - n) = d[\delta(t + 1/2) + \delta(t - 1/2)] \tag{A.5}$$

$$\frac{d\,h_o(t)}{dt} \cdot \sum_{n=-\infty}^{\infty} \delta(t - n) = 0 \tag{A.6}$$

where $\delta(\cdot)$ is the Dirac delta function. With $H_o(f)$ defined as the Fourier transform of $h_o(t)$ these correspond the following frequency domain constraints

$$H_o(f) * \sum_{n=-\infty}^{\infty} \delta(f-n) = 1. \tag{A.7}$$

$$H_o(f) * \sum_{n=-\infty}^{\infty} \delta(f-n)\, e^{-\jmath\pi f} = 2d\cos(\pi f) \tag{A.8}$$

$$\jmath 2\pi f H_o(f) * \sum_{n=-\infty}^{\infty} \delta(f-n) = 0 \tag{A.9}$$

where $*$ denotes convolution. After the convolution operation these equations can be written as:

$$\sum_{n=-\infty}^{\infty} H_o(f-n) = 1 \tag{A.10}$$

$$\sum_{n=-\infty}^{\infty} e^{\jmath\pi n} H_o(f) = 2d\cos(\pi f) \tag{A.11}$$

$$\sum_{n=-\infty}^{\infty} (f-n) H_o(f-n) = 0 \tag{A.12}$$

These equations imply three function segments in the Nyquist interval $f \in [0, 1/2)$. Considering $n = -1, 0, 1$ gives

$$\begin{bmatrix} 1 & 1 & 1 \\ -1 & 1 & -1 \\ (f+1) & f & (f-1) \end{bmatrix} \begin{bmatrix} H_o(f+1) \\ H_o(f) \\ H_o(f-1) \end{bmatrix} = \begin{bmatrix} 1 \\ 2d\cos(\pi f) \\ 0 \end{bmatrix} \tag{A.13}$$

hence

$$H_o(f-1) = \frac{1}{4} + \frac{f}{2} - \frac{d}{2}\cos(\pi f) \tag{A.14}$$

$$H_o(f) = \frac{1}{2} + d\cos(\pi f) \tag{A.15}$$

$$H_o(f+1) = \frac{1}{4} - \frac{f}{2} - \frac{d}{2}\cos(\pi f) \tag{A.16}$$

in the interval $f \in [0, 1/2)$. $H_o(f)$ may thus be written as:

$$H_o(f) = \begin{cases} \frac{1}{2} + d\cos(\pi f), & 0 \leq |f| \leq \frac{1}{2} \\ \frac{1}{2}\left[\frac{3}{2} + d\cos(\pi f) - |f|\right], & \frac{1}{2} < |f| \leq \frac{3}{2} \\ 0, & \text{elsewhere} \end{cases} \tag{A.17}$$

Finally, the time domain waveform that satisfies equations (A.1), (A.2) and (A.3) can now be obtained by means of an inverse Fourier transform of equation (A.17):

$$h_o(t) = \text{sinc}(t)\,\text{sinc}(2t) + \frac{d}{2}\left[\text{sinc}\left(t + \frac{1}{2}\right) + \text{sinc}\left(t - \frac{1}{2}\right)\right][1 - \cos(2\pi t)] \tag{A.18}$$

Appendix B

Derivation of equations (2.76), (2.77) and (2.78)

Equation (2.76)

Since the evaluation of the term with $k = -1$ in equation (2.76) depends on the relative values of $t = t_s - 1$ and the input pulse width T_s, this equation will be first rewritten as:

$$\sum_{\substack{k=-1 \\ k\neq 0}}^{\infty} h_o^2(t_s + k) = h_o^2(t_s - 1) + \sum_{k=1}^{\infty} h_o^2(t_s + k) \tag{B.1}$$

For $k \geq 1$ the relation $t_s + k \geq Ts$ is always true since, the input pulse width is in the range $T_s \in [0, 1)$ and t_s is, as discussed in text, constrained to take values $t_s \geq 0.5$. In these circumstances the sum of terms with $k \geq 1$ is always evaluated using the third conditional form of equation (2.73) and is given by:

$$\sum_{k=1}^{\infty} h_o^2(t_s + k) = \sum_{k=1}^{\infty} \left\{ \sum_{n=1}^{N} \frac{r_n}{p_n T_s} \left[1 - e^{-p_n T_s}\right] e^{p_n (t_s + k)} \sum_{m=1}^{N} \frac{r_m}{p_m T_s} \left[1 - e^{-p_m T_s}\right] e^{p_m (t_s + k)} \right\} \tag{B.2}$$

$$= \sum_{n=1}^{N} \sum_{m=1}^{N} \left\{ \frac{r_n \left(1 - e^{-p_n T_s}\right) e^{p_n t_s}}{p_n T_s} \frac{r_m \left(1 - e^{-p_m T_s}\right) e^{p_m t_s}}{p_m T_s} \sum_{k=1}^{\infty} e^{p_n k} e^{p_m k} \right\} \tag{B.3}$$

Making the substitutions

$$x_n = e^{-p_n} \tag{B.4}$$

$$a_n = \frac{r_n}{T_s} \left[1 - e^{-p_n T_s}\right] e^{p_n t_s} \tag{B.5}$$

equation (B.3) becomes:

$$\sum_{k=1}^{\infty} h_o^2(t_s + k) = \sum_{n=1}^{N} \sum_{m=1}^{N} \left\{ \frac{a_n a_m}{p_n p_m} \sum_{k=1}^{\infty} x_n x_m{}^{-k} \right\} \tag{B.6}$$

The right side infinite sum in equation (B.6) is a geometric series with limit

$$\sum_{k=1}^{\infty} x_n\, x_m{}^{-k} = \frac{1}{1-(x_n\, x_m)^{-1}} - 1 = \frac{1}{x_n\, x_m - 1} \tag{B.7}$$

and so (B.6) has a closed form expression

$$\sum_{k=1}^{\infty} h_o^2(t_s + k) = \sum_{n=1}^{N}\sum_{m=1}^{N} \frac{a_n\, a_m}{p_n\, p_m\, (x_n\, x_m - 1)} \tag{B.8}$$

Hence, equation (B.1) can finally be written as:

$$\sum_{\substack{k=-1 \\ k\neq 0}}^{\infty} h_o^2(t_s + k) = h_o^2(t_s - 1) + \sum_{n=1}^{N}\sum_{m=1}^{N} \frac{a_n\, a_m}{p_n\, p_m\, (x_n\, x_m - 1)} \tag{B.9}$$

Equation (2.77)

Equation (2.77) is readily derived form equation (B.2) by replacing t_s with $t_s + \frac{1}{2}$, making the substitution

$$b_n = \exp\left\{\frac{p_n}{2}\right\} \tag{B.10}$$

and following the steps used in the derivation of equation (B.8)

Equation (2.78)

Adopting a similar approach to the derivation of equation (2.76), equation (2.78) will be written as

$$\sum_{n=-1}^{\infty} {h'_o}^2(t_s + k) = {h'_o}^2(t_s - 1) + {h'_o}^2(t_s) + \sum_{n=1}^{\infty} {h'_o}^2(t_s + k) \tag{B.11}$$

Using (B.4) and (B.5) $h_o(t_s + k)$ and ${h'_o}^2(t_s + k)$ can be expressed for $t_s + k \geq T_s$ as:

$$h_o(t_s + k) = \sum_{n=1}^{N} a_n\, x_n{}^{-k} \tag{B.12}$$

$${h'_o}^2(t_s + k) = \sum_{n=1}^{N} p_n\, a_n\, x_n{}^{-k} \tag{B.13}$$

Comparing these two equations, it is easily seen that

$$\sum_{n=1}^{\infty} {h'_o}^2(t_s + k) \tag{B.14}$$

has a similar form to equation (B.8) but with each term in the sum multiplied by $p_n\, p_m$, giving:

$$\sum_{n=1}^{\infty} h_o'^{\,2}(t_s + k) = \sum_{n=1}^{N} \sum_{m=1}^{N} \frac{a_n\, a_m}{x_n\, x_m - 1} \tag{B.15}$$

Equation (B.11) then can be written as:

$$\sum_{n=-1}^{\infty} h_o'^{\,2}(t_s + k) = h_o'^{\,2}(t_s - 1) + h_o'^{\,2}(t_s) + \sum_{n=1}^{N} \sum_{m=1}^{N} \frac{a_n\, a_m}{x_n\, x_m - 1} \tag{B.16}$$

Appendix C

MATLAB Toolbox: Circuit Analysis

This appendix is a short description of the circuit analysis toolbox developed for use with the MATLAB program [71]. The toolbox implements the necessary functions for noise and signal analysis of two-port networks of arbitrary complexity. The toolbox allows the wide range of mathematical, signal processing functions and optimisation algorithms within MATLAB to be used for circuit analysis and optimisation.

Introduction

To maintain compatibility with MATLAB matrix structures and compact matrix operations the network frequency dependent two-port and correlation matrix are defined as $N \times 4$ matrices with each line corresponding to a different frequency f_k and columns $j = 1, 2, 3$ and 4 corresponding to the matrix elements (1,1), (1,2), (2,1) and (2,2) respectively. For example, the frequency dependent two-port matrix `X` is represented in matlab by:

$$\mathtt{X} = \begin{bmatrix} X_{11}^1 & X_{12}^1 & X_{21}^1 & X_{22}^1 \\ \vdots & \vdots & \vdots & \vdots \\ X_{11}^k & X_{12}^k & X_{21}^k & X_{22}^k \\ \vdots & \vdots & \vdots & \vdots \\ X_{11}^n & X_{12}^N & X_{21}^N & X_{22}^N \end{bmatrix} \tag{C.1}$$

where the upper script k indicates that the k-th line corresponds to the frequency point f_k. The following conventions are used:

An upper case letter followed by a lower case letter (e.g. `Cx`) is used to represent the network correlation-matrix;

An upper case letter on its own (e.g. X) is used to represent the network two-port matrix;

An upper case italic letter (e.g. X) is used to represent the network name;

A lower case letter (e.g. x) is used to represent an impedance. Lower case letters are also used to represent component values in the component functions;

The letter T is used to represent the network obtained by series, parallel or cascade connection of two networks. In a cascade connection L is used to represent the input network (left) and R the output network (right);

The letter s is used to denote the complex column frequency vector $s_k = \jmath 2\pi f_k$ with $k = 1, \ldots, N$;

Unless otherwise stated the network two-port and correlation matrix are assumed to be in the chain matrix representation.

Circuit analysis toolbox functions

The list below gives a brief description of the functionality of the main circuit analysis toolbox functions. Full documentation for each of the functions and its associated parameters is contained in the MATLAB toolbox m-files and can be accessed using the MATLAB help facility.

Elementary functions

`T = A + B` - series or parallel connection of networks A and B when the two-port matrices are in the impedance or admittance representation respectively;

`Ct = Ca + Cb` - series or parallel connection of networks A and B when the correlation matrices are in the impedance or admittance representation respectively;

`A = T - B` - de-embedding of the two-port matrix of network A in a series or parallel connection when the two-port matrices are in the impedance or admittance representation respectively;

`Ca = Ct - Cb` - de-embedding of the correlation matrix of network A in a series or parallel connection when the two-port matrices are in the impedance or admittance representation respectively;

`C = cascade(L,R)` - returns the two-port matrix of the cascade connection of networks L and R;

`[Cc,C] = ccascade(Cl,L,Cr,R)` - returns the correlation and the two-port matrix of the cascade connection of networks L and R;

`Cx = cpassive(X,θ)` - returns the correlation matrix of the passive network X at temperature θ. `Cx` and `X` are either in the admittance or impedance representation;

`[Cl,L] = deembedcl(Ct,T,Cr,R)` - de-embeds the correlation and the two-port matrix of network L in the cascade connection of L and R;

`[Cr,R] = deembedcr(Ct,T,Cl,L)` - de-embeds the correlation and the two-port matrix of network R in the cascade connection of L and R;

`L = deembedl(T,R)` - de-embeds the two-port matrix of network L in the cascade connection of L and R;

`R = deembedr(T,L)` - de-embeds the two-port matrix of network R in the cascade connection of L and R;

`[k,Δ] = k_delta(S)` - returns the parameters k and Δ used in the stability criterion. S are the network s-parameters;

`Γ = reflect_coef_y(Y,Yo)` - returns the the reflection coefficient of the admittance `Y`. `Yo` is the reference admittance (default 20 mS);

`Γ = reflect_coef_z(Z,Zo)` - returns the the reflection coefficient of the impedance `Z`. `Zo` is the reference admittance (default 50 Ω);

`X = reverse(X)` - transposes the input and output ports;

`B = series2shunt(A,z)` - converts the two-port matrix of the 'series' network A into a shunt impedance with two-port matrix `B`. The network A can be terminated in an impedance `z`, but if none is specified an open-circuit across the output port of A is assumed;

`v = vswr(s`$_{ii}$`)` - returns the standing wave ratio of either s_{11} or s_{22};

`x = zin(A,z)` - returns the input impedance of network A when loaded by the impedance `z`. When `z` is not specified an open-circuit across the output port of A is assumed;

`x = zout(A,z)` - returns the output impedance of network A when loaded by the impedance z. When z is not specified an open-circuit across the input port of A is assumed.

Conversion functions

`X = abcd2s(X)` - converts the chain-parameters to s-parameters;

`X = abcd2y(X)` - converts the chain-parameters to y-parameters;

`X = abcd2z(X)` - converts the chain-parameters to z-parameters;

`[Fmin,Yopt,Rn] = c2noise_param(Cx)` - returns the noise parameters of a network with correlation matrix `Cx`

`[Cx,X] = cabcd2cy(Cx,X)` - converts form the chain representation to the admittance representation;

`[Cx,X] = cabcd2cz(Cx,X)` - converts form the chain representation to the impedance representation;

`[Cx,X] = cce2ccb(Cx,X)` - converts the common-emitter (common-source) configuration to the common-base (common-gate) configuration;

`[Cx,X] = cce2ccc(Cx,X)` - converts the common-emitter (common-source) configuration to the common-collector (common-drain) configuration;

`X = ce2cb(X)` - converts the common-emitter (common-source) configuration to the common-base (common-gate) configuration;

`X = ce2cc(X)` - converts the common-emitter (common-source) configuration to the common-collector (common-drain) configuration;

`[Cx,X] = cy2cabcd(Cx,X)` - converts form the admittance representation to the chain representation;

`X = cy2cz(X)` - converts the y-parameters to z-parameters;

`[Cx,X] = cz2cabcd(Cx,X)` - converts form the impedance representation to the chain representation;

`X = cz2cy(X)` - converts the z-parameters to y-parameters;

`Cx = noise_param2c(Fmin,Yopt,Rn)` - returns the correlation matrix of a network with noise parameters `Fmin`, `Yopt`, `Rn`;

`X = s2abcd(X)` - converts s-parameters to chain-parameters;

`X = y2abcd(X)` - converts y-parameters to chain-parameters;

`X = y2z(X)` - converts y-parameters to z-parameters;

`X = z2abcd(X)` - converts z-parameters to chain-parameters;

`X = z2y(X)` - converts z-parameters to y-parameters;

Ideal components

`X = cap(s,c)` - returns the two-port matrix of an ideal series capacitor;

`X = ind(s,l)` - returns the two-port matrix of an ideal series inductor;

`[Cx,X] = mesfet_prc_cy(s,params,prc,`θ`)` - returns the correlation matrix of the intrinsic MESFET in the admittance representation. The P, R,and C noise model is used. It also returns the intrinsic MESFET y-matrix;

`X = mesfet_y(s,params)` - returns the y-matrix of the intrinsic MESFET;

`X = res(s,l)` - returns the two-port matrix of an ideal series resistor;

`X = series(z)` - returns the two-port matrix of a series impedance z;

`X = shunt(y)` - returns the two-port matrix of a shunt admittance y;

`X = tline(s,Zo,fo,`φ`o)` - the two-port matrix of an ideal transmission line.

GaAs Foundry components

`X = algaas254(s,l,lbw)` - returns the two-port matrix of a physical Alumina/GaAs transition (254 μm alumina);

`X = algaas635(s,l,lbw)` - returns the two-port matrix of a physical Alumina/GaAs transition (635 μm alumina);

`X = bond_pad(s,l)` - returns the two-port matrix of a bond pad;

`X = icap(s,c)` - returns the two-port matrix of an inter-digital capacitor;

`[Cx,X] = ig_mesfet_prc_cz(s,params,prc,`θ`)` - returns the correlation two-port matrices of a GaAs MESFET in the impedance representation. The P, R and C noise model is used;

`X = ig_mesfet_z(s,params)` - returns the z-matrix of a GaAs MESFET;

`X = m2line(s,w,l)` - returns the two-port matrix for a microstrip line fabricated on the M2 metallisation layer;

`X = m3line(s,w,l)` - returns the two-port matrix for a microstrip line fabricated on the M3 metallisation layer;

`X = mres(s,Rdc,Le,dW,Lu)` - returns the two-port matrix of a GaAs mesa resistor;

`X = ncap(s,c)` - returns the two-port matrix of a nitride capacitor;

`X = pcap(s,c)` - returns the two-port matrix of a polyimide capacitor;

`X = pind(s,c)` - returns the two-port matrix of a planar inductor;

`X = viahole` - returns the two-port through GaAs via hole.

Utility functions

`A = hconj(A)` - returns the Hermitian conjugate of the matrix `A` (in the toolbox format);

`A = inverse(A)` - returns the inverse of the matrix `A` (in the toolbox format);

`noise_parameters` - noise de-embedding of the GaAs foundry P, R and C noise coefficient;

`smith_chart` - plots the Smith chart.

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