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Abstract

This thesis extensively explores, for the first time, the technical feasibility and performance of real-time end-to-end optical orthogonal frequency division multiplexing (OOFDM) transmission systems by implementing field programmable gate array (FPGA)-based OOFDM transceivers incorporating entirely self-developed digital signal processing (DSP) algorithms. Commercially available 4GS/s, 8 quantization-bit digital-to-analogue (DAC) and analogue-to-digital converters (ADC) are utilised in the transceivers and low-cost intensity modulation and direct detection (IMDD) transmission systems are also employed for all transmission systems as the research focuses on cost-sensitive access and in-building networks. A series of world–first and world-only, real-time, end-to-end OOFDM transmission systems were achieved. The initial DQPSK-based transceiver designs demonstrated first a 1.5Gb/s and subsequently a 3Gb/s net bit rate over 500m multi-mode fibres (MMFs). Thorough enhancement of the transceiver's DSP design, 16-quadrature amplitude modulation (16-QAM) with additional DSP features achieved a 6Gb/s net bit rate over 300m MMF, followed by an 11.25Gb/s line rate over 500m MMFs and 25km standard single-mode fibres (SSMFs) /MetroCore™ SMFs due to the utilisation of 64-QAM with more advanced DSP functions.

The use of different intensity modulators, as alternatives to the initial DFB-based directly modulated laser (DML), was explored. A colourless OOFDM transceiver was demonstrated at 7.5Gb/s line rate over 25km SSMF using a 1GHz reflective semiconductor optical amplifier (RSOA) as an intensity modulator. To further reduce the transceiver cost, a low-cost VCSEL-based DML was successfully employed at 11.25Gb/s over 25km SSMF.

To achieve a fully autonomous OOFDM receiver a synchronous clocking technique was proposed and experimentally demonstrated at 11.25Gb/s over 25km SSMF without degradation in system performance. Over the same IMDD systems, a versatile, highly accurate, performance penalty-free solution for automatic symbol synchronisation was also proposed and experimentally demonstrated using DC offset signalling.

This research is a significant milestone in proving the technical feasibility of OOFDM for practical applications in future access and in-building networks.

Acknowledgements

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Abbreviations

A

ADC	Analogue to Digital Converter
AM	Amplitude Modulation
AMOOFDM	Adaptively Modulated Optical OFDM
APD	Avalanche Photodiode
AWG	Arbitrary Waveform Generator
AWG	Arrayed Waveguide Grating
AWGN	Additive White Gaussian Noise

B

BER	Bit Error Rate
BPON	Broadband Passive Optical Network

C

CD	Chromatic Dispersion
CDF	Cumulative Density Function
CFO	Carrier Frequency Offset
CO-OFDM	Coherent Optical Orthogonal Frequency Division Multiplexing
C-OFDM	Coded OFDM
CO	Central Office
CP	Cyclic Prefix
CPE	Carrier Phase Error
CTF	Channel Transfer Function
CW	Continuous Wave
CWDM	Course Wavelength Division Multiplexing

D

DAB	Digital Audio Broadcast
DAC	Digital to Analogue Converter
DBA	Dynamic Bandwidth Allocation
DBPSK	Differential Binary Phase Shift Keying
DCF	Dispersion Compensating Fiber
DFB	Distributed Feedback
DFT	Discrete Fourier Transform

DMD	Differential Mode Delay
DML	Directly Modulated Laser
DQPSK	Differential Quadrature Phase Shift Keying
DSL	Digital Subscriber Loop
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processing
DVB	Digital Video Broadcast

E

EDFA	Erbium-Doped Fibre Amplifier
EO	Electrical-to-Optical
EPON	Ethernet Passive Optical Network
10G-EPON	10 Gigabit-Ethernet Passive Optical Network

F

FDM	Frequency Division Multiplexing
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FPGA	Field-Programmable Gate Array
FTTH/B/P	Fiber-To-The-Home/Building/Premises
FWM	Four-Wave Mixing

G

GPON	Gigabit-capable Passive Optical Network
10G-PON	10 Gigabit- Passive Optical Network

H

HD	High-Definition
HDTV	HD Television

I

ICI	Inter-Channel-Interference
IDFT	Inverse Discrete Fourier Transform
IFFT	Inverse Fast Fourier Transform
IFR	Integrated Frequency Response
IMDD	Intensity Modulation and Direct Detection
IP	Intellectual Property

ISI	Inter-Symbol-Interference

L

LAN	Local Area Network
LD	Laser Diode
LTE	Long-term Evolution

M

MAC	Medium Access Control
MAN	Metropolitan Area Network
MIMO	Multiple Input, Multiple Output
MMF	Multi-Mode Fibre
MSL	Mode Selective Loss
MZM	Mach-Zehnder Modulator
M2M	Man To Machine

N

NG-PON	Next Generation Passive Optical Network

O

ODN	Optical Distribution Network
OE	Optical-to-Electrical
OFDM	Orthogonal Frequency Division Multiplexing
OFL	Over-Filled Launching
OLT	Optical Line Terminal
ONU	Optical Network Unit
OOFDM	Optical Orthogonal Frequency Division Multiplexing
OOFDMA	OOFDM Multiple Access
OSNR	Optical Signal-to-Noise Ratio

P

PAPR	Peak-to-Average Power Ratio
PD	Photodiode
PON	Passive Optical Network
P/S	Parallel-to-Serial
PSK	Phase Shift Keying

Q

QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

R

RB	Rayleigh backscattering
RF	Radio Frequency
ROFL	Radically Over-Filled Launching
RSOA	Reflective Semiconductor Optical Amplifier

S

SAN	Storage Area Network
SCO	Sampling Clock Offset
S/H	Sample-and-Hold
SMF	Single-Mode Fibre
SNR	Signal-to-Noise Ratio
S/P	Serial-to-Parallel
SPM	Self-Phase Modulation
SOA	Semiconductor Optical Amplifier
STO	Symbol Timing Offset

T

TIA	Transimpedance Amplifier
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access

V

VCO	Voltage-Control Oscillator
VCSEL	Vertical Cavity Surface Emitting Laser

W

WDM	Wavelength Division Multiplexing

X

XPM	Cross-Phase Modulation

Contents

1 Introduction

Contents

1.1 Optical Networks and Future Challenges

There is a constantly growing obsession with digital media around the world, the younger generations are growing up in a world where the creation, consumption and sharing of digital media by individuals is a way of life. Consumers are not only demanding more and more digital media but also require it to be delivered at faster and faster speeds. As a consequence the capacity of the world's data networks needs to evolve appropriately to ensure the growing level of digital services are delivered efficiently whilst meeting the expected end-user experience. The exponentially growing demand for higher transmission speeds is fuelled by the profusion of emerging bandwidth hungry internet services with video-centric applications clearly dominating the demands on bandwidth, the increasing levels of video resolution and the latest development of 3D video putting further demands on the required network bandwidth. The increasing bandwidth consumption is further compounded by the fact that many households can now afford multiple PCs so will consume multiple services simultaneously with each end user still demanding the same quality of service. Also a growing amount of internet traffic is originating from non-PC devices such as TVs, tablets, smart-phones, and machine-to-machine (M2M) modules, it is predicted that worldwide there will be two networked devices per capita in 2015 [1]. Another modern phenomenon which is impacting network bandwidth requirements is the increasing use of cloud computing [2], where user applications run on remote servers over the network rather than on the users' local PC. This concept is in its early stages but if it becomes widely adopted it can clearly impose additional bandwidth requirements on the world's data networks. Evidence of the increasing bandwidth demand is backed up by various studies; Cisco recently forecast [1] that average global internet traffic will increase fourfold from 2011 to 2015, whilst over the same period busy-hour traffic will increase fivefold. Also it is predicted that to meet traffic growth demands in the UK operators must offer internet connection speeds of 1Gb/s in 2016 and 10Gb/s in 2021 [3].

These new digital services and the changes in peoples' media consuming habits and expectations mean that patterns in bandwidth consumption are also changing. Users can require ultra-high bandwidth for brief periods such as when downloading high-definition (HD) movies for example, or can require a guaranteed sustained bandwidth such as when streaming video or audio for example. The changes in the bandwidth consumption patterns

mean that the data networks must not only provide a drastically increased total bandwidth, but they must have the ability to flexibly allocate the available bandwidth in a dynamic manner, this is most relevant to access networks and local area networks which perform user traffic aggregation. The ability to efficiently allocate the available bandwidth in the access network is also necessary to support the typical network operator's business model of varying tiers of service, thus subscribers only pay for the services and therefore the bandwidth they need.

As the world's communication network must evolve to meet the demands of the new multi-media age that we are witnessing and to ensure high speed end-to-end connectivity is provided across the entire network, precedence must be given to alleviating the network capacity bottlenecks. The global communication network of today is a highly complex system and is constructed and managed in a hierarchical structure with clearly defined network layers, consisting of, from top down: the long-haul core network, metropolitan area networks (MANs) or metro networks, access networks and in-building networks. The core and metro networks are now almost exclusively optical fiber networks. The access networks and in-building networks, however, employ a mixture of copper cable, optical fiber and wireless-based technology.

Considering the optical networks, long-haul transmission links in the core network operate at speeds of 10s-100s Tb/s over distances of 100s-1000s km providing intercontinental and international data links around the globe and between large cities or urban areas. Below the core network, metro networks cover geographical areas the size of a city or large urban area. These networks operate at typical data rates of 100s-1000s Gb/s and individual links can cover distances of 10s of km. The access networks provide traffic aggregation to/from commercial or residential in-building networks and interface to the metro networks. Current access networks provide aggregated data rates in the order of several 100s of Mb/s and each user connection is typically several 10s of Mb/s for residential users and a few 100s of Mb/s for commercial users, with typical link lengths of ≤20km. User premises, particularly commercial users, also utilise fiber-based networks for the various types of in-building networks such as local area networks (LANs) to connect multiple user terminals and servers to the access network and provide local interconnectivity; storage area networks (SANs) which consolidate storage devices on a dedicated network and data

center networks which interconnect a large number of high power computing recourses. These in-building networks will be generally referred to as LANs from here onwards.

When evaluating the ability of the global communications network to support future bandwidths the long-haul networks and metro networks, which have experienced significant developments in the associated transmission technologies, are not presently limiting factors. It is the access networks and LANs where the major bandwidth bottlenecks currently exist, therefore the current status and future needs of these networks are examined in detail. Firstly the fixed access network is considered. To provide increased bandwidth in the access network, worldwide operators are steadily replacing legacy copper pairs with optical fibers due to their superior transmission capacity. The different fiber-based access network topologies are commonly referred to as fiber to the home/building/premises/etc (FTTH/B/P) or more generally as FTTx. Driven by the need to minimise capital and operating expenditure a widely deployed architecture for FTTx networks is the passive optical network (PON). PON technologies reduce cost by serving multiple users over a single feeder fiber and by eliminating active network elements in the optical distribution network (ODN), therefore only maintenance-free, zero power, passive optical elements are employed in the ODN. Also the increased reach of PONs compared to copper-based access networks leads to consolidation of central offices (COs) which leads to substantial savings in network operating costs. The most common PON standards today are ITU-T G.984 Gigabit PON (GPON) [4] and IEEE 802.3ah Ethernet PON (EPON) [5]. GPON (EPON) provides maximum symmetric line rates of 2.5Gb/s (1.25Gb/s) with a reach of up to 20km, these standards are referred to as Gigabit-PONs due to the near 1Gb/s aggregate data rates. 10Gigabit-PON technologies are becoming standardised which provide an evolutionary growth of the existing Gigabit-PON standards to support symmetric aggregate data rates of 10Gb/s. There are two approved 10Gigabit-PON standards: ITU-T G987 10Gigabit PON (10G-PON) [6] and IEEE 802.3av 10Gigabit EPON (10G-EPON) [7]. The first commercial deployments of these standards is predicted for 2012, however widespread commercial roll-out of 10Gb/s FTTx networks may still be a long way from being a reality as equipment vendors face the challenge of developing sufficiently low priced 10Gigabit-PON equipment. Although 10Gigabit-PON technologies are today considered as next generation PON (NG-PON) technologies it is not realistic to consider them as future-proof solutions as even higher bandwidth demand is expected in as

little as 5 years [1] when PONs should be capable of delivering 40Gb/s or even 100Gb/s aggregate data rates to meet the widely accepted target of 1Gb/s per end-user [3].

The optical modulation techniques used in 10Gigabit-PON technologies are based on conventional ON/OFF intensity modulation techniques, these modulation methods are now reaching the limit where compensation of the fiber dispersion-induced pulse broadening effect is required. Various dispersion compensation techniques are possible however they add additional system complexity which is challenging to implement cost-effectively as bit rate goes beyond 10Gb/s. Therefore, to meet the demand for the ultra high bit rates in future PONs it is essential that new "beyond-10G-PON" technologies are developed with advanced modulation techniques that better tolerate all unwanted effects of the fiber channel and optical components and so offer superior transmission performance in a cost-effective manner. The new "beyond-10G-PON" optical transmission technologies must ideally also provide longer transmission distances for further CO consolidation and support for increasing numbers of end-user on a single PON, whilst simultaneously meeting the strict cost restrictions of the access network.

Considering fiber-based LANs, the most common type today are the 1000BASE-SX/LX variants of the Gigabit Ethernet standard [8] employing multi-mode fiber (MMF). There are a vast number of organisations around the world that have an installed fiber network based on legacy MMF (class OM1 and OM2). It was estimated in 2007 that the total length of installed legacy MMF worldwide was 21,000 million meters [9]. It is therefore highly desirable to utilise this vast installed infrastructure of MMF when upgrading LAN capacity to benefit from the enormous associated cost saving. Considering 10G Ethernet standards which can utilise legacy MMFs for the migration from 1Gb/s to 10Gb/s; the 10GBASE-LX4 technology is based on coarse wavelength division multiplexing (CWDM) supporting up to 300m transmission, the required four laser sources making this an expensive solution. On the other hand the single source 10GBASE-LRM technology based on receiver side electronic dispersion compensation is limited to 220m transmission. New optical transmission technologies that can cost-effectively support transmission at 10Gb/s over >300m of legacy MMF are therefore highly desirable. Furthermore it is predicted that even higher LAN speeds will be required in future, evidence of this is the recent approval of the 40G/100G Ethernet standard [10]. This standard however is based on multiple 10Gb/s or 25Gb/s streams, cannot operate over legacy MMF and is limited to 125m using

non-legacy MMF (OM4). Therefore, based on the future demand for higher LAN capacity and the desire to use existing fiber infrastructure for cost-effective network upgrades, new optical transmission technologies are needed that target cost-effective solutions for >40Gb/s over >300m of legacy MMF.

It should be noted that, as previously stated, in-building networks can be copper cable and/or wireless based. Copper cable technologies become limited in transmission distance as bit rates increase, for example Cat-5 twisted-pairs can only support Gigabit Ethernet up to 100m [8]. Multi-Gb/s wireless technologies are being developed, which operate at millimetre wavelengths restricting them to short-range in-room transmission [11]. These technologies therefore cannot compete with the fiber based networks in providing high speed, building-wide coverage. However, high speed in-building wireless connectivity can be achieved by employing a high speed fiber network to feed distributed wireless access points [12].

A new optical transmission technology that can meet the future requirements of both access network and LAN applications in a cost-effective manner is therefore vital to ensure global network performance is not outpaced by demand. The key features that must be offered by a suitable technology are summarised below:

- *Increased Network Data Capacity:* As previously discussed a significant boost in data capacity must be provided to end-users and therefore aggregated data rates must increase accordingly. New future-proof optical transmission technologies are therefore needed that enable network products to steadily evolve towards 100Gb/s aggregate bit rates.
- *Cost Effectiveness:* As access networks and LANs are highly cost-sensitive the technology must offer increased network performance in a cost-effective manner, both in terms of capital expenditure and operating costs. This is because of the traffic-revenue divergence effect where revenue growth significantly lags behind traffic growth as end users will not expect to pay much more for future network services as they do for today's services.
- *Compatibility:* To ease the migration to a new optical technology in both access networks and LANs, backwards compatibility with existing networks is highly advantageous. By developing new optical transmission standards that can co-exist

with existing standards over the same fiber infrastructure allows a smooth network upgrade in line with demand. The compatibility of a new technology with existing network infrastructure, even without considering co-existence, is also clearly a key cost-saving feature.

- *Network Convergence:* For access networks transmission distance is a significant factor influencing network costs. By providing PONs that can support 20-100km distances central offices can be consolidated and the metro network and access network start converging. Ideally long reach systems would be purely passive to minimise costs although active reach extension technologies can be considered.

- *Effective bandwidth management:* To fully utilise the boosted network data rates and meet users' data usage patterns the allocation of capacity must be flexible and efficient, this characteristic is commonly referred to as dynamic bandwidth allocation (DBA) where allocated bandwidth is determined according to users' instantaneously changing service requirements.

- *High Energy Efficiency:* The world's information and communication systems are estimated to account for approximately 2 percent of global carbon dioxide (CO_2) emissions, according to an estimate by Gartner Inc, a figure comparable to the aviation industry. Therefore developing new technologies which are energy efficient and can intelligently manage energy usage is highly important from an environmental perspective. An attractive side-effect of such "green" networks is that operators will also benefit from reduced operating costs.

A strong candidate for the physical layer technology in future access networks and LANs, due to its numerous advantages, is orthogonal frequency division multiplexing (OFDM) [13-16]. OFDM is an advanced multi-carrier modulation format, commonly employed in today's wired-electrical and wireless systems operating at 10s of Mb/s. OFDM has the potential to operate in the optical domain as optical OFDM (OOFDM) at multi-10Gb/s speeds [13,14] and provide a technology which can address the previously identified requirements as follows:

- *Increased Network Data Capacity:* The features of OOFDM which make it suitable for ultra-high speed optical connectivity are: i) high spectral efficiency due to the tightly spaced overlapping subcarriers, ii) high tolerance to channel dispersion by using multiple lower rate data channels and the use of a cyclic prefix

to eliminate dispersion-induced inter-symbol interference (ISI), iii) adaptive modulation of subcarriers to efficiently utilise the available channel spectral characteristics thus allowing trade off between reach and bit rate [13,14].

- *Cost Effectiveness:* OOFDM has the potential for cost effective implementation through i) exploitation of advanced semiconductor electronics for high-speed digital signal processing (DSP), which benefits from low cost when associated with high volumes, ii) use of low bandwidth and therefore lower cost optical and RF components due to the high spectral efficiency, iii) the ability to reduce optical link complexity by eliminating optical amplifiers and dispersion compensating fibers (DCFs) and iv) the ability to utilise existing fiber infrastructure [23-38,41].

- *Compatibility:* OOFDM can be implemented in a time division multiple access (TDMA) system where OOFDM symbols are only transmitted on allocated timeslots [15], this provides the potential for co-existence with other existing TDMA based standards. Alternatively, OOFDM can be overlaid on existing networks by employing a dedicated wavelength [17]. Furthermore, as mentioned above, OOFDM is highly suited to using existing fiber infrastructures due to the aforementioned adaptive modulation feature to effectively utilise fiber bandwidth.

- *Network Convergence:* Due to OOFDM's high fiber dispersion tolerance it can support long transmission distances in access networks allowing the aforementioned metro-access convergence and CO consolidation. [18].

- *Effective bandwidth management:* OOFDM can offer hybrid dynamic bandwidth allocation through the partitioning of bandwidth in both the time and frequency domains [15]. This provides dynamic bandwidth allocation with the granularity of symbols and subcarriers with full flexibility on how bandwidth is distributed.

- *High Energy Efficiency:* The energy efficiency that can be achieved with an OOFDM transceiver is presently difficult to predict, however there are good indications that high efficiency is possible, due to features such as i) OOFDM's high spectral efficiency and ability to effectively utilise the available channel spectrum results in high capacity single wavelength systems, which consume less energy than the multi-wavelength systems ii) the electronics-powered DSP can benefit from future advances in energy efficiency of semiconductor technologies, such as the highly energy efficient organic electronics [19].

It is important to stress that this thesis focuses on demonstrating the technical feasibility of real-time OOFDM with emphasis on data capacity and cost effectiveness, detailed investigations of the additional aforementioned key requirements are beyond the scope of this current research.

There are two basic types of optical systems where OOFDM can be applied. The first type is direct detection and the second type is coherent detection. A detailed comparison of the two types of systems is given in section 2.4.3, where it is shown that coherent detection systems can outperform direct detection systems in many respects, however the increased performance comes at a significantly elevated cost, this is can be acceptable in core and metro network applications, but cannot be tolerated in the cost sensitive access networks and LANs. As these are the target networks, the experiments performed in this research therefore employ intensity modulation and direct detection (IMDD) systems. It should be noted however that the DSP-based real-time OOFDM signal generation and decoding demonstrated here is also applicable to the case of coherent transmission.

The use of OOFDM for high-speed optical data networks was first proposed and demonstrated in 2005 [16] using a non-real-time experiment. Since then there has been steadily growing research activities to investigate the potential and feasibility of employing OOFDM in all optical network types. The strong interest in OOFDM clearly existing today is apparent from the dramatic increase in the number of OOFDM publications in the last few years. Initial OOFDM research work predominantly involved theoretical investigations [13,14], later experimental demonstrations based on off-line signal processing were increasingly reported. The off-line approach employs software-based signal processing for both the transmitter and receiver side DSP with high speed arbitrary waveform generators (AWGs) and digital sampling oscilloscopes (DSOs) being used for digital-to-analogue and analogue-to-digital conversion respectively. This off-line approach has shown the potential of OOFDM in long-haul applications [20,21], access applications [22-24] and LAN applications [25]. However, off-line signal processing is not restricted by the finite speed, precision and resources of modern DSP hardware required for implementing practical OOFDM transceivers. The next logical step, to further investigate the feasibility of OOFDM and its ability to meet the demands of future generations of optical networks, is to demonstrate real-time OOFDM transmission through the design and implementation of real-time OOFDM transceivers. This will allow both the practicality of the OOFDM

technique to be rigorously validated and just as importantly, offer insights into its commercial feasibility. A key question to be answered is if modern semiconductor electronics can perform the computationally intense OFDM signal processing algorithms with sufficient speed and accuracy to support the required multi-Gb/s bit rates, which significantly exceed the bit rates in any existing OFDM system.

This dissertation research successfully undertakes the design, implementation and analysis, for the first time, of real-time end-to-end OOFDM transceivers. It will be shown that real-time OOFDM transmission with line rates and electrical spectral efficiencies as high as 11.25Gb/s and 5.625b/s/Hz respectively can be achieved, over 25km SMF and 500m MMF in directly modulated laser (DML)-based IMDD systems. This is a highly significant achievement as it is a major step towards demonstrating that OOFDM is a viable future optical networking technology.

1.2 Major Achievements of the Dissertation Research

The primary objective of this research was to design, implement and analyse OOFDM transceivers and demonstrate for the first time, real-time end-to-end OOFDM data transmission. This had never before been achieved and so a major challenge was to answer the aforementioned question of whether or not modern digital semiconductor electronics could provide the speed, accuracy and processing power to implement the high-speed DSP algorithms required for OOFDM signal modulation and demodulation. A further objective was to target the real-time OOFDM systems at applications in cost-sensitive access networks and LANs, therefore simple IMDD optical links, based on directly-modulated lasers (DMLs), without in-line amplification or dispersion compensating fiber were employed. A highly important aspect of this research is the analysis of the implemented OOFDM transceivers and systems to investigate how various system parameters can be optimised to maximise system performance and also identify the factors which limit system performance.

OOFDM transceivers were design based on off-the-shelf components including field programmable gate arrays (FPGAs) for high speed DSP, DACs and ADCs. Fully custom logic designs were implemented for all DSP algorithms. Initial experiments involving

DML-based IMDD links demonstrated for the first time, real-time end-to-end OOFDM transmission at 1.5Gb/s net bit rate and, by subsequently doubling operating speed, at 3Gb/s net bit rate. The transceiver design was then further enhanced by employing higher modulation formats, variable or adaptive subcarrier power loading and on-line parameter adjustment and performance monitoring to allow rapid optimisation of system performance. The enhancements first achieved a line rate of 7.5Gb/s followed by the current highest end-to-end line rate of 11.25Gb/s.

As intensity modulators take a significant portion of the total OOFDM transceiver cost, different types of intensity modulators were fully investigated including DFB lasers, reflective semiconductor optical amplifiers (RSOAs) and vertical cavity surface emitting lasers (VCSELs). RSOA-based intensity modulators can also offer colourless transceiver operation which is highly beneficial from the perspective of network deployment and operation. As the OOFDM transmission had so far employed manual symbol synchronisation techniques and a common transmitter/receiver clock reference, practical solutions for these key synchronisation functions were explored. As synchronous clock recovery technique, based on the transmission of a dedicated clock signal, was proposed and demonstrated which did not degrade system performance in any way at 11.25Gb/s. Furthermore an automatic symbol synchronisation technique was developed based on DC-offset signalling and a sliding correlation algorithm. The demonstration of these synchronisation functions meaning that no major technical challenges remain to implementing practical OOFDM transmission systems. The synchronisation methods developed are of high significance as they are designed to support OOFDM-based PONs, where accurate synchronisation is essential.

Related to the above work there have been a total of 42 papers published in world-leading professional journals and international conferences, of these papers there have been 7 first authored journal papers and 9 first authored international conferences papers. In addition two patents on high-speed real-time OOFDM signal synchronisation techniques have also been filed. Bangor University is also now widely recognised in the optical communications research community for this work on real-time OOFDM.

The major achievements are summarised as follows:

❖ Development of a flexible hardware platform for implementing real-time OOFDM transceivers.

A hardware platform has been developed based on FPGAs and high-speed DACs and ADCs. The platform enables reconfigurable signal processing algorithms to be implemented in the digital domain, i.e. DSP, along with signal conversion to/from the analogue domain for signal transmission. In addition, suitable RF frontends have been implemented as needed for interfacing to the optical transmission link. The platform is constructed from commercially available components based on well established technologies indicating that a route to cost effective transceivers is conceivable.

❖ Development of fully custom 32 point IFFT and FFT algorithms [26-41,44].

The core functions required for OFDM signal generation and decoding are the inverse discreet Fourier transform (IDFT) and discreet Fourier transform (DFT) respectively. A computationally efficient way of implementing the IDFT and DFT is through the use of the inverse fast Fourier transform (IFFT) and fast Fourier transform (FFT) respectively. Fully custom 32 point IFFT and FFT DSP algorithms have been designed and implemented upon which all OOFDM transceiver designs are based. A custom design provides advantages over a third party IP solution such as i) control over the calculation precision at each IFFT/FFT stage so that DSP resources can be kept to a practical limit, ii) the possibility of supporting more subcarriers through scaling the IFFT/FFT, and iii) the flexibility to modify the design allowing further optimisation such as reducing logic utilisation and increasing clocking speed.

❖ World's first experimental demonstration of end-to-end real-time OOFDM transmission [26-28].

The developed hardware platform incorporating the custom IFFT/FFT algorithms along with all other necessary logic functions were integrated to successfully achieve the first ever demonstration of real-time, end-to-end OOFDM transmission. This was achieved first at 1.5Gb/s net data rate, using DQPSK modulation on all subcarriers over 500 m, 62.5/125 μm MMF in an IMDD system involving a DML. The custom IFFT/FFT algorithms were also validated in hardware at a data

throughput of ~10Gb/s. These results were a highly significant first step which strongly indicate OOFDM is a viable and practical technology with significant potential for supporting higher data rates.

❖ Enhancement of the OOFDM transceivers to achieve a series of record speed end-to-end real-time OOFDM transmissions [29-34].

The OOFDM transceiver DSP implementation was improved in stages by implementing techniques including; increasing clock speeds and sample rates, incorporating channel estimation and equalisation, using higher modulation formats and incorporating variable or adaptive power loading. Also on-line parameter adjustment and performance monitoring features provided a means of rapidly optimising system performance. This resulted in a series of record speed real-time end-to-end OOFDM experimental demonstrations all employing DML-based IMDD links; by doubling the transceiver clock and sample rates 3Gb/s net bit rate was achieved over 500m MMF. By employing 16-QAM modulation and incorporating channel estimation and equalisation in combination with a simple power loading scheme 6Gb/s transmission was achieved over 300m MMF. Finally by employing 64-QAM modulation and an enhanced adaptive power loading scheme a net bit rate of 9Gb/s (11.25Gb/s line rate) was demonstrated over both 25km SMF and 500m MMF, which is currently the fastest ever real-time end-to-end OOFDM transmission demonstration. Details of these results are included in Table 1.1. These results clearly show that OOFDM is capable of fully exploiting channel bandwidth to achieve high signal bit rates through high spectral efficiency, the highest electrical spectral efficiency demonstrated being as high as 5.625b/s/Hz. This indicates that by exploiting the higher sample rate DAC/ADCs now available and through techniques such as multiband-OOFDM or polarisation multiplexing, OOFDM has the potential to achieve the 40Gb/s to 100Gb/s required in future generation optical networks.

❖ Investigation of OOFDM transmitter performance with various optical intensity modulators such as directly modulated DFBs and VCSELs and colourless operation with RSOAs [35-40].

As the real-time transceivers are targeted at applications in cost sensitive access networks and LANs, DMLs offer the most cost-effective solution for intensity modulation. This work has initially investigated the performance of DFB-based DMLs however, although cheaper than external modulators, they still constitute a significant portion of the overall transceiver cost. VCSELs on the other hand are significantly cheaper than DFBs and so offer a highly attractive alternative. It is demonstrating that VCSEL-based DMLs can achieve similar system performance to the DFB-based DML at 11.25Gb/s over SMF and MMF. This shows that VCSEL-based OOFDM transceivers can offer a significant reduction in overall transceiver cost.

Furthermore it was demonstrated that by using of a RSOA a colourless OOFDM transceiver can be realised. The significance of a colourless transceiver is that wavelength division multiplexed PONs (WDM-PONs) are widely considered as one of the most promising strategies for high capacity access networks where each end user is allocated a dedicated operating wavelength. It is undesirable from a logistics and operational point of view to have user premise equipment with different factory-set fixed wavelengths. Equipment that can be configured in the field to operate at any wavelength in a preset band, i.e. colourless, are therefore highly advantageous from the perspective of network operation and management.

❖ Proposal and demonstration of new synchronisation techniques for OOFDM system clocking and symbol alignment [41-45].

For the aforementioned transmission experiments clocking was implemented using a common clock source electrically fed to both the transmitter and receiver. Also the OOFDM symbol alignment was achieved using a manual alignment method. Both of these approaches are of course not practical in a real system deployment. Methods were proposed and demonstrated to solve both these problems. A DSP-free synchronous receiver clocking technique based on the transmission of an auxiliary clock signal was proposed and the world's first real-time OOFDM transmission with synchronous clock recovery was experimentally demonstrated. It was shown that through optimisation of clock and OOFDM signal levels there is no system bit error rate (BER) performance degradation or optical power budget

penalty and that system stability is significantly improved. This is an important result as the technique can be applied to PONs employing OOFDMA where all network elements must be highly synchronised. The developed synchronous clocking technique achieves this with an effective, low-cost, DSP-free solution.

Furthermore a versatile automatic symbol alignment technique based on low-power DC offset signalling with a sliding correlation algorithm was proposed and demonstrated. The symbol synchronisation method provides symbol, timeslot and frame synchronisation in both point-to-point and point-to-multipoint PONs, with the essential feature of allowing the synchronisation of new end-user transceivers in a live network without disturbing existing traffic. This is believed to be the only proposed OOFDMA-PON synchronisation method that can offer this essential feature. Furthermore physical layer network security can be offered through the use of coded DC offset signalling. Patents have been filed for both synchronisation techniques.

Table 1.1 *World-First Real-Time End-to-End OOFDM Experiments*

Date	Line Rate (Gb/s)	Net Data Rate (Gb/s)	Modul-ation	Sample Rate (GS/s)	Direct Modul-ator	Link
April 2009	1.875	1.5	DQPSK	2	DFB	500m MMF
May 2009	3.75	3	DQPSK	4	DFB	500m MMF
July 2009	7.5	6	16-QAM	4	DFB	300m MMF
Oct 2009	7.5	6	16-QAM	4	RSOA	25km SSMF
Dec 2009	11.25	9	64-QAM	4	DFB	25km SSMF
Feb 2010	11.25	9	64-QAM	4	DFB	500m MMF
Oct 2010	11.25	9	64-QAM	4	VCSEL	25km SSMF

1.3 Thesis Structure

This thesis is organized into nine chapters. The work performed solely as part of this research is presented in Chapters 3-8.

This chapter has presented the challenges facing future optical networks and shown the motivation for researching real-time OOFDM transmission.

To aid understanding of the work presented in this thesis chapter 2 presents the basic principles of both OOFDM and the discreet Fourier transform. For the OOFDM principles the focus is on the IMDD transmission case as this is employed in the experimental demonstrations, however coherent OOFDM (CO-OFDM) is presented to allow comparisons between the two basic OOFDM techniques. As the FFT and IFFT are core enabling algorithms for the OOFDM transceiver the basic theory behind the implemented solution are also outlined.

In chapter 3 the real-time FPGA-based OOFDM transceiver design is presented. The fundamental OOFDM transceiver architecture and transmission system structure to enable real-time end-to-end OOFDM transmission experiments are defined, with key components and their requirements presented. Full details of the implemented high level transceiver architecture are presented outlining all discrete components and associated interconnections. The DSP functional architecture is then described with detailed descriptions of key DSP logic functions, particular focus is given to the FFT/IFFT algorithm implementation.

In chapter 4 the implemented transceivers are employed to demonstrate real-time end-to-end OOFDM transmission over DML-based IMDD links. This successfully results in the first ever real-time end-to-end OOFDM transmission at 1.5Gb/s net data rate with DQPSK modulation, error free transmission is achieved over 500m of 62.5/125μm MMF. The transceiver design is subsequent improved by doubling the operating speed to demonstrate a twofold increase in the net data rate to 3Gb/s with a BER as low as $3.3x10^{-9}$ achieved with transmission again over 500m of 62.5/125μm MMF. This work demonstrates that OOFDM is capable of multi-Gb/s transmission with excellent BER and reach performance in legacy MMF links. Furthermore in chapter 4 the technique used to validate the operation

of the IFFT and FFT logic functions is presented and it is shown that the implemented FFT/IFFT can support ~10Gb/s with the potential for supporting >40Gb/s.

Chapter 5 addresses the issue of increasing the bit rate of the OOFDM transceivers to further explore the capabilities of the OOFDM technology. This is achieved by modifying the transceiver DSP design alone. Higher QAM modulation formats are employed to give the increase in bit rates, the incorporation of channel estimation and equalisation functions based on pilot-subcarriers being necessary for operation with QAM modulation formats. By employing 16-QAM a line rate first to 7.5Gb/s is achieved and by further modification for 64-QAM a line rate of 11.25Gb/s is achieved. At the higher modulation formats employed for the increased bit rates, the system is more sensitive to the system frequency response roll-off effect, variable or adaptive power-loading techniques are employed to compensate this effect and achieve the required BER performance. A simple variable power-loading scheme being sufficient for 16-QAM, however an enhanced adaptive scheme is needed for 64-QAM. All design modifications required for operating at higher modulation formats and the variable and adaptive power-loading functions are fully described. Furthermore, additional on-line parameter adjustment and performance monitoring features, which allow rapid optimisation of system BER, are fully described. System performance is fully analysed for both transceiver designs.

In previous chapters experiments are based on a directly modulated DFB laser, in chapter 6 alternative intensity modulators are investigated. A RSOA intensity modulator is investigated to evaluate its use in achieving colourless OOFDM transceivers. It is shown that colourless operation over the C-band is possible. Furthermore the use of a low-cost VCSEL intensity modulator is also explored as this can contribute to a significant reduction in overall transceiver cost. It is demonstrated that 11.25Gb/s is possible with a low-cost, low-bandwidth VCSEL over 25km SSMF.

In the experiments in previous chapters the OOFDM transceiver clocking has been based on a common clock approach where both the transmitter and receiver are fed from the same clock reference. In chapter 7 a practical technique is presented for achieving synchronous clocking of the receiver, the technique is optimised to show that there is no penalty in terms of BER performance or power budget penalty. The great advantage of the

synchronous clocking technique, as when applied to OOFDM multiple access-based passive optical networks (OOFDMA-PONs), is illustrated.

All previous experiments relied on a manual symbol synchronisation technique, in chapter 8 a versatile OOFDM symbol synchronisation technique is proposed and experimentally demonstrated. The technique based on low power DC offset signalling and sliding correlation algorithm is described in detail and the advantages of the technique are presented, it is shown that a key feature of the technique is the ability to achieve symbol synchronisation in a live point-to-multipoint OOFDM network.

Finally, a summary of the thesis and possible future research work is presented in Chapter 9.

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2 Fundamentals of OFDM and Optical OFDM

Contents

2.1 Historical Development of OFDM

Data transmission by orthogonal frequency division multiplexing (OFDM) was first introduced in the 1960s [1-3]. The concept, first proposed by Chang [1,2], as a way to overlap the spectra of multiple independent orthogonal carriers without causing mutual interference and achieving a highly efficient use of transmission spectrum. However the early OFDM modems [3] were highly complex and therefore not viable from a technical or economic perspective for wide deployment and so initially OFDM was limited to military applications for many years. The use of the discreet Fourier transform (DFT) for the generation of OFDM signals [4,5] was first proposed by Salz and Weinstein in 1969 [4] which was a key step in making OFDM a more realistic proposition. However it was only following a paper in 1985 by Cimini on OFDM for mobile communications [6] that OFDM began to be seriously considered for application in practical communication systems. In 1995 two OFDM-based standards were formally adopted: the digital subscriber line (DSL) standard for data transmission over copper pairs and digital audio broadcast (DAB) standard for digital radio. Subsequent OFDM-standards include the digital video broadcast (DVB) standard in 1997 and the first wireless LAN (WLAN) standard in 1999. Developments in the processing power of digital semiconductor electronics were a key contributing factor to the success of OFDM, which is today established at the heart of a broad range of widely deployed communication systems. Also further evidence of the accomplishment of OFDM is its selection for the fourth generation (4G) mobile phone standard (LTE).

As OFDM has achieved huge success in wired and wireless systems its emergence in optical transmission systems is inevitable. Research on the use of OFDM in optical communications began in the late 1990s, Pan and Green first published a paper on OFDM for fiber-based cable TV [7] in 1996. It is only since around 2005 that research in optical OFDM began to rapidly increase around the world. An indication of the potential of OFDM in optical communications is evident from results of various non-real-time experiments, for example in 2009, 13.5Tb/s (135×111Gb/s) coherent OOFDM transmission over 6248km SMFs [8] and 100Gb/s single band direct detection OOFDM transmission over 500km SMFs [9] were demonstrated. Also in 2011 a 1.2Tb/s (25x48Gb/s) WDM-OFDMA-PON supporting 800 users [10] was demonstrated using the off-line

approach. Since 2009 a number of OOFDM transmission experiments employing real-time processing in either the transmitter [11-14] or the receiver [15,16] have been demonstrated with off-line processing employed in the corresponding transmitter or receiver. The work presented in this thesis is however the first and still the only, experimental demonstration of end-to-end OOFDM transmission employing both a real-time transmitter and receiver which was first achieved in 2009.

2.2 OFDM Basic Concepts

OFDM is a type of multicarrier modulation (MCM) in which a data stream at one rate is split into a number of parallel lower rate streams, the streams are separately modulated onto different frequency carriers waves, or subcarriers, for transmission over the same channel. A general MCM transmission system is depicted in Fig. 2.1. A serial binary sequence $b(t)$ is converted to N_{SC} parallel binary sequences each at $1/N_{SC}$ of the input bit rate, in each binary sequence one or more sequential bits are encoded to a complex data value $d_{k,m}$, which modulates a complex subcarrier $e^{j2\pi f_k t}$ at frequency f_k, where k and m correspond to the kth subcarrier and the mth symbol. The symbol period is T_b. In Fig. 2.1 the complex multipliers provide IQ modulation and demodulation (only the real part of the complex output being utilised). The transmitted signal $s(t)$ is the sum of all modulated subcarriers and has the general form defined by the following equations:

$$s(t) = \sum_{m=-\infty}^{+\infty} \sum_{k=1}^{N_{SC}} d_{k,m} e^{j2\pi f_k (t - mT_b)} \tag{2.1}$$

$$d_{k,m} = \left[R_{k,m} e^{j\theta_{k,m}} \right] Y(t) \tag{2.2}$$

$$Y(t) = \begin{cases} 1, & (0 < t \le T_b) \\ 0, & (t \le 0, t > T_b) \end{cases} \tag{2.3}$$

$R_{k,m}$ and $\theta_{k,m}$ are the amplitude and phase respectively of the encoded data $d_{k,m}$, $Y(t)$ is the modulation pulse shaping waveform which ensures the mth encoded data is zero outside the mth symbol. Either or both of $R_{k,m}$ and $\theta_{k,m}$ can be modulated to implement the digital data encoding.
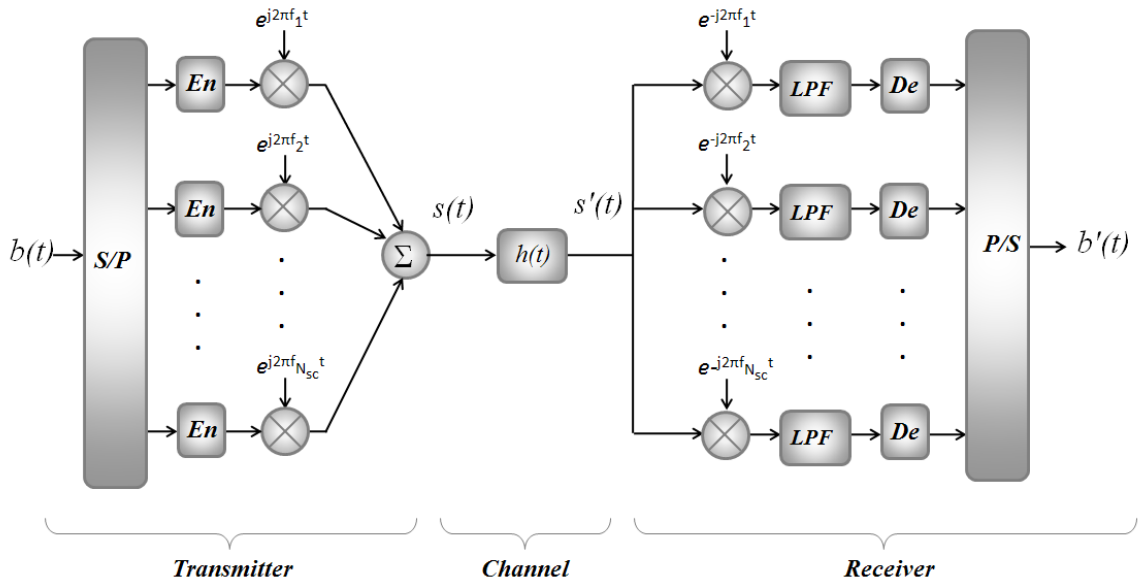
Fig. 2.1 Block diagramof a generic multicarrier transmission system(S/P:Serial-to-Parallel, P/S:Parallel-to-Serial,LPF:Low-Pass Filter, En:Encoder, De:Decoder)

The key advantage of the MCM system compared to the single carrier system is that each of the N_{SC} subcarriers in the MCM system operates at $1/N_{SC}$ of the bit rate of the corresponding single carrier system if the same total bit rate is considered. As the symbol periods are thus increased this makes the MCM system more tolerant to dispersive fading channels, such as radio channels which suffer from multipath propagation. The channel dispersion effect causes symbols to broaden and overlap each other, so called inter-symbol interference (ISI), a longer symbol can tolerate the ISI more making the MCM more tolerant to ISI. The channel dispersion also leads to channel fading where high attenuation occurs at some frequencies, the MCM system can be designed to simply avoid subcarriers where attenuation is too high without significant impact on overall data capacity. The utilisation of the subcarriers can be changed dynamically to cope with a varying channel response such as in wireless mobile systems.

In the general case of a MCM system based on frequency division multiplexing (FDM) to ensure there is no interference between subcarriers guard bands are employed between each signal band giving a signal spectrum as shown in Fig. 2.2. The guard bands are made sufficiently wide so that filters can be used to separate the bands in the receiver before

decoding. This approach is however not spectrally efficient due to wide guard bands being needed to allow for practical filters.
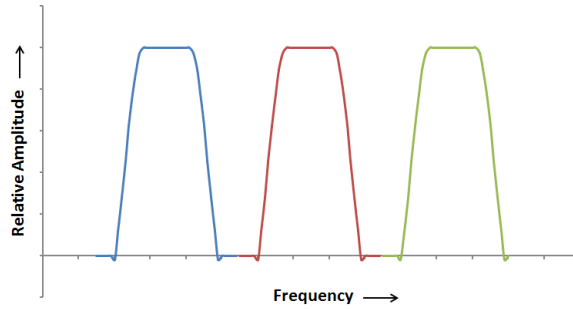
Fig. 2.2 Spectum of a FDM modulated signal

OFDM is a special case of a MCM system where the difference between any two subcarrier frequencies Δf is defined as follows:

$$\Delta f = c\,\frac{1}{T_b} \tag{2.4}$$

where c is an integer. The subcarrier frequencies employed are more generally defined as:

$$f_k = f_0 + \frac{k}{T_b} \qquad\qquad (k = 1, 2, .., N_{SC}) \tag{2.5}$$

where f_0 is a frequency offset common to all subcarriers, generally set to zero and k=(1,2,3,...N_{SC}). Example time domain waveforms of 4 subcarriers over one symbol period are shown in Fig. 2.3 with the resulting time domain signal after summation shown in Fig. 2.4. The resulting subcarriers each have a spectrum with a sin(x)/x shape centred at the subcarrier frequency, the spectra from different subcarriers overlapping each other, as shown in Fig. 2.5, making it highly spectrally efficient compared to the FDM system.
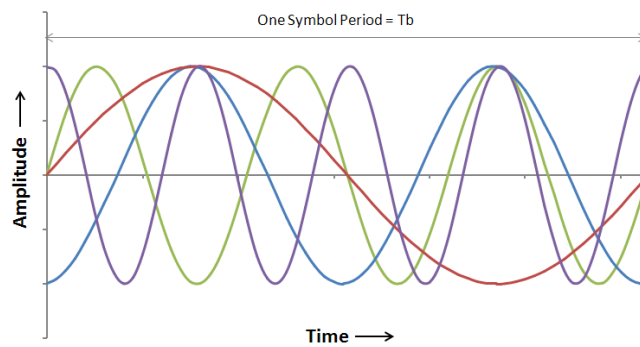
Fig. 2.3 Time domain signals of subcarriers with equal amplitudes over one symbol period. Red: frequency 1/T_b, phase 0°, Blue: frequency 2/T_b, phase 270°, Green: frequency 3/T_b, phase 0°, Purple: frequency 4/T_b, phase 90°
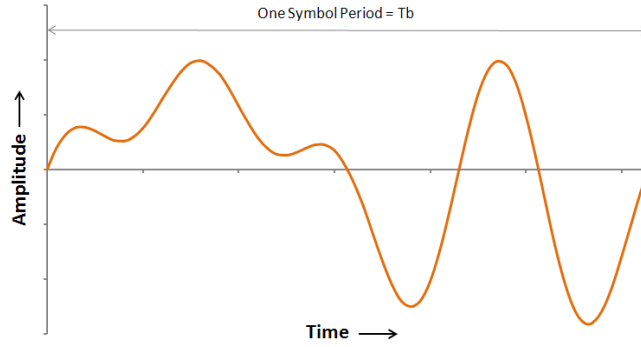
Fig. 2.4 Time domain signal of combined subcarriers after summation
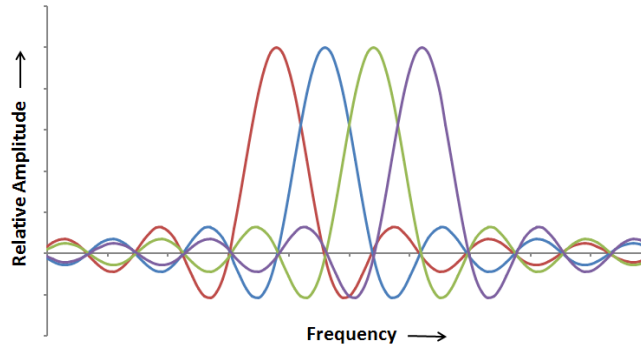
Fig. 2.5 Spectrum of OFDM modulated signal

The data encoded on individual subcarriers can be decoded despite the spectral overlapping due to the orthogonal property of the subcarriers. To decode a subcarrier at frequency f_k, the received signal $s'(t)$ is multiplied by the complex signal $e^{-2\pi f_k t}$ and integrated over the symbol period to give the detected symbol $d'_{k,m}$ as defined by Eq.(2.6). The low-pass filters in Fig. 2.1 effectively perform the integration function. Any subcarrier not at frequency f_k will integrate to 0 and so not influence the value of $d'_{k,m}$.

$$d'_{k,m} = \frac{1}{T_b} \int_0^{T_b} s'(t - mT_b)e^{-2\pi f_k t} \, dt \tag{2.6}$$

The orthogonality of the subcarriers is also revealed in the spectrum shown in Fig. 2.5 as at any specific subcarrier frequency all other subcarriers have zero amplitude.

The bit rate or line rate R_L of the OFDM system is defined as follows:

$$R_L = \frac{1}{T_b} \sum_{k=1}^{N_{SC}} b_k \tag{2.7}$$

where b_k is the number of bits encoded onto the kth subcarrier. If b bits are encoded onto each subcarrier, Eq.(2.7) can be rewritten as:

$$R_L = \frac{N_{SC}b}{T_b} \tag{2.8}$$

As subcarrier frequency spacing is $1/T_b$ the total signal bandwidth is $\sim N_{SC}/T_b$, making spectral efficiency S_{eff} in b/s/Hz as follows:

$$S_{eff} = \frac{R_L}{N_{SC}/T_b} = b \tag{2.9}$$

2.3 OFDM Transceiver Functions
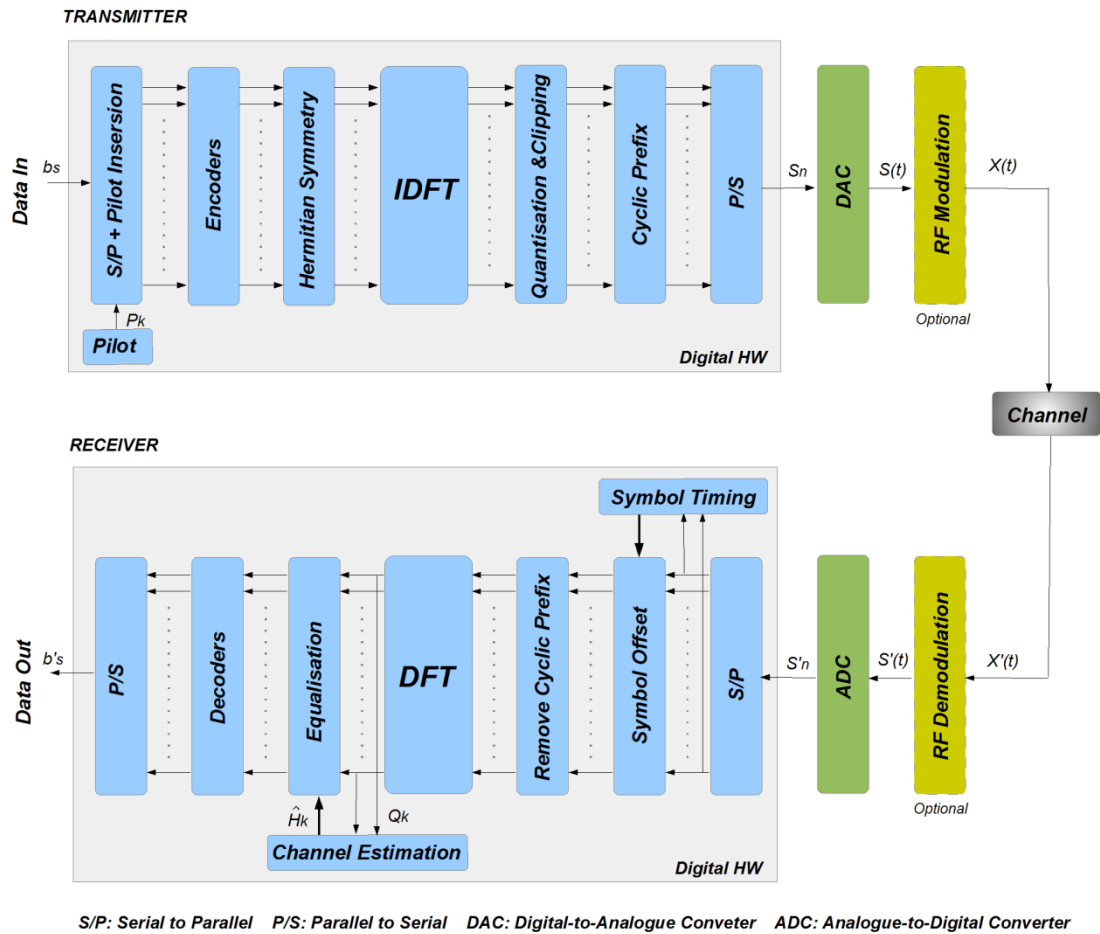
Fig. 2.6 Block Diagram of an OFDM Transmission System

This section explores the functional architecture of an OFDM transmitter and receiver describing the operation of the various functional blocks required to generate and decode OFDM signals according to the basic concepts described in section 2.2. Fig. 2.6 shows a block diagram of an OOFDM transmission system for real-valued time domain signals.

2.3.1 Encoders and Decoders

In the transmitter an incoming binary data sequence, b_s, is truncated in to a series of parallel data sets, each p bits wide, via a serial-to-parallel converter (S/P). Each data set is subdivided into N_{SC} data words, corresponding to the number of data carrying subcarriers. Each data word is then encoded to a complex number using a specific modulation format to represent a subcarrier's frequency domain amplitude and phase. For example if p=60 and N_{SC} =15, then 4 bits can be encoded onto each subcarrier. The encoder function will thus require N_{SC} encoders in parallel. It should be noted that subcarriers can use varying modulation formats, this results in variable bit loading as is discussed in section 2.4.4. The modulation formats typically employed are binary phase shift keying (BPSK), differential BPSK (DBPSK), quadrature phase shift keying (QPSK), differential QPSK (DQPSK) and 16, 32, 64, 128 or 256 quadrature amplitude modulation (QAM). As an example the 16-QAM constellation diagram is illustrated in Fig. 2.7 showing the mapping between 4-bit binary data and encoded complex values. The encoded frequency domain data of all subcarriers provides the input to the IDFT.
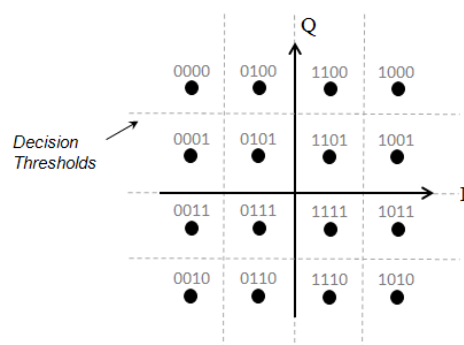
Fig. 2.7 16-QAM Encoding

In the receiver the output of the DFT provides the encoded frequency domain data values after transmission through the channel, each subcarrier is then equalised as described in section 2.3.6, before decoding can be performed to recover the transmitted binary data. Decoding employs decision thresholds to determine the most probable transmitted data value. The decision thresholds are shown in Fig. 2.7 for the 16-QAM case. The recovered data from each subcarrier are recombined to form a parallel data set and serialised via parallel-to-serial conversion (P/S) to form the recovered serial binary data sequence. It

should be noted that the serial data interfaces can in practice consist of multiple data streams with multiple S/P and P/S converters.

2.3.2 IDFT/DFT

To benefit from the advantages of OFDM a large number of subcarriers are required, to implement OFDM transceivers with discrete components would lead to a complex architecture as each subcarrier requires oscillators, mixers, filters etc in both the transmitter and receiver, making this approach impractical. OFDM modulation and demodulation can be performed by the inverse discrete Fourier transform (IDFT) and the discrete Fourier transform (DFT) [4] respectively, which allows for a more practical implementation of OFDM transceivers. In this approach the OFDM signal is processed as a discrete signal, rather than a continuous signal, in both the frequency and time domains making the approach highly suited to DSP implementation. The IDFT converts a series of N complex coefficients X_k representing the amplitude and phase of the discrete signal frequencies f_k (both positive and negative) to a series of N coefficients x_n representing the corresponding discrete complex time domain samples. The IDFT is defined as follows:

$$x_n = \frac{1}{N} \sum_{k=\frac{-N}{2}}^{\frac{N}{2}-1} X_k e^{j\frac{2\pi}{N}kn} \qquad n = -\frac{N}{2}, \ldots, 0, \ldots, \frac{N}{2} - 1 \quad (2.10)$$

The DFT converts a series of complex time domain coefficients x_n into the corresponding complex frequency domain coefficients X_k and is defined as follows:

$$X_k = \sum_{n=\frac{-N}{2}}^{\frac{N}{2}-1} x_n e^{j\frac{-2\pi}{N}kn} \qquad k = -\frac{N}{2}, \ldots, 0, \ldots, \frac{N}{2} - 1 \quad (2.11)$$

If the general equation for a MCM signal in Eq.(2.1) is modified to represent an OFDM signal, the symbol index is temporarily ignored to consider a single symbol, Eq.(2.5) is substituted with f_0=0, the sample interval becomes T_b/N and so the nth sample of $s(t)$ is as follows (n=0,1,...,N_{SC}-1):

$$s_n = \sum_{k=1}^{N_{SC}} d_k e^{j2\pi \frac{k}{T_b} t} = \sum_{k=1}^{N_{SC}} d_k e^{j2\pi \frac{k}{N} n} \tag{2.12}$$

The DFT/IDFT involve both positive and negative frequencies therefore an N point DFT/IDFT can support $(N/2)$-1 different real-valued frequencies plus zero frequency, thus $N_{SC} = (N/2)$-1. If Eq.(2.12) is rewritten to incorporate N and the negative frequencies are accounted for it becomes:

$$s_n = \sum_{k=-\frac{N}{2}}^{\frac{N}{2}-1} d_k e^{j2\pi \frac{k}{N} n} \tag{2.13}$$

which is the IDFT of d_k when comparing to Eq.(2.10), the $1/N$ multiplier in Eq.(2.10) simply providing a scaling factor. It should be noted that s_n defined by Eq.(2.13) is a complex signal and only the real part is used for transmission, where as the IDFT form in Eq.(2.10) can generate either a complex or real valued s_n due to the inclusion of negative frequencies. The generation of a complex or real valued OFDM signal is discussed in the following section.

If Eq.(2.6) is rewritten to consider a single received symbol, as shown in Eq.(2.14), it can be show in a similar way that this is the DFT of $s'(t)$. The positive frequency coefficients d'_k (k=1,2,...,N_{SC}) are therefore the received complex data that was encoded on the N_{SC} subcarriers.

$$d'_k = \frac{1}{T_b} \int_0^{T_b} s'(t) e^{-2\pi f_k t} \, dt \tag{2.14}$$

The IDFT function can therefore be used to replicate a bank of modulators in the transmitter, similarly the DFT function can be used to replicate a bank demodulators and low-pass filters in the receiver. This is a key result that allowed OFDM to be implemented in practical systems through the use of DSP for performing the IDFT and DFT functions.

To implement the IDFT and DFT efficiently with hardware-based DSP algorithms the inverse fast Fourier transform (IFFT) and fast Fourier Transform (FFT) are used as they

considerably reduce the number of complex computations required. The IFFT and FFT are described in detail in section 3.3.5.

2.3.3 IDFT Generation of Complex or Real-valued OOFDM signals

The IDFT defined in Eq.(2.10) shows that a time domain signal is constructed from both positive and negative frequencies, thus the frequency index k varies from $-N/2$ to $(N/2)$-1. It is also valid to define k from 0 to N-1 as the IDFT (and DFT) are cyclic in nature. If the frequency domain coefficients X_k for the positive frequency bins are encoded independently to the coefficients for the negative frequency bins the time domain signal will be complex valued thus consisting of both real and imaginary components. To transmit a complex time domain signal a carrier signal must be employed that can be modulated to carry two independent signals. This is achieved by modulating the in-phase carrier component with the real part of the signal and the quadrature carrier component with the imaginary part of the signal, this is the commonly employed I/Q modulation scheme. The I/Q modulated carrier will be a real-valued signal therefore the complex signal from the IDFT is effectively converted to a real-valued signal for transmission. In the receiver I/Q demodulation converts the real-valued carrier back to a complex signal for decoding.

If a transmission system only supports a single baseband signal it can only carry real-valued signals. For this case the frequency coefficients at the IDFT input must be selected to give time domain coefficients with non-zero-valued real coefficients and zero-valued imaginary coefficients at the IDFT output. This is achieved by arranging the frequency coefficients with Hermitian symmetry [17] such that encoded data is applied to the positive frequency bins only and the complex-conjugates are applied to the corresponding negative frequency bins, such that:

$$X_{-k} = X_k^* \qquad \text{k=1,2,...,}(N/2)\text{-1} \qquad (2.15)$$

and $X_0 = X_{-N/2} = 0$ as the subcarrier at zero frequency cannot carry data and due to the need for symmetry there is no corresponding positive frequency for $X_{-N/2}$.

Generating real-valued time domain signals with the DFT halves the effective number of data carrying subcarriers, however this is accompanied by a reduction in the complexity of the required transmission system.

2.3.4 Cyclic Prefix

As previously mentioned, OFDM is highly tolerant to systems with dispersive fading channels which cause the duration of each data symbol to increase due to the differential delay associated with multiple transmission signals. If the maximum differential signal delay is τ, this will cause adjacent symbols to overlap each other at the receiver for a period of τ resulting in inter-symbol-interference (ISI). ISI is illustrated in Fig. 2.8, where a single subcarrier is considered and signal power is divided equally between three different signal paths (blue, red and green) which experience different delays.
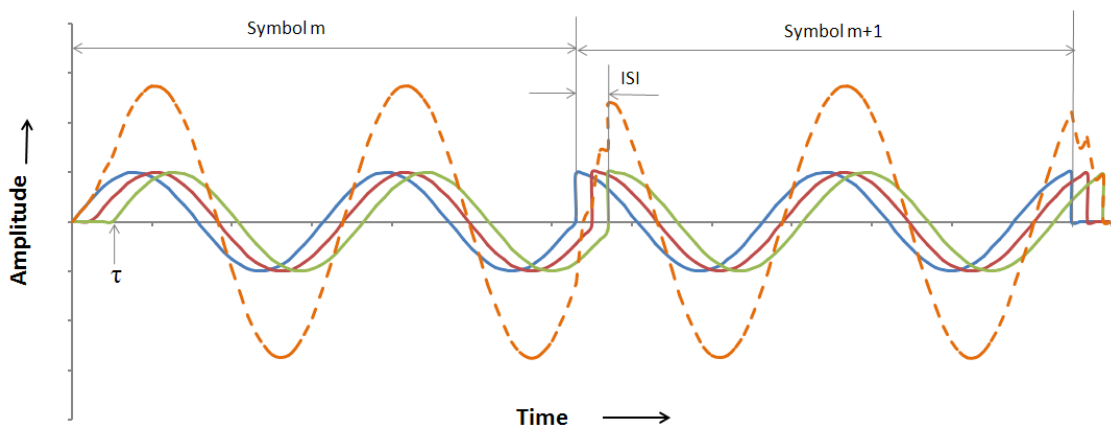
Fig. 2.8 Intersymbol Interference between two symbols for one subcarrier

The received signal is the sum of the three delayed signals (orange). At the boundary between the *m*th and (*m*+1)th symbol overlap occurs between the symbols causing the aforementioned ISI. It should also be noted however that the channel dispersion does not distort the subcarrier for the majority of the symbol duration, only at the leading and trailing edges, the dispersion does however results in a phase shift of the subcarrier. Two important features of the OFDM signal should be considered here i) the OFDM symbol period is greatly increased compared to single carrier systems operating at the same bit rate therefore tolerance to ISI is significantly increased ii) the dispersion-induced phase shift on each subcarrier is indistinguishable from any channel induced phase shift so is compensated for during channel equalisation.

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To reduce the effect of ISI a cyclic prefix can be employed. The basic principle is that a time delay is inserted between successive symbols which is longer than the maximum differential signal delay. The inter-symbol gap then accommodates the dispersion-induced symbol extension thus eliminating and interference with the subsequent symbol. The gap between the symbols however can be filled such that the distortion at the beginning of the following symbol is eliminated. This is achieved by taking a copy of the last part of the symbol and placing it in front of the symbol in the inter-symbol gap as illustrated in Fig. 2.9. This inserted signal is known as a cyclic prefix.
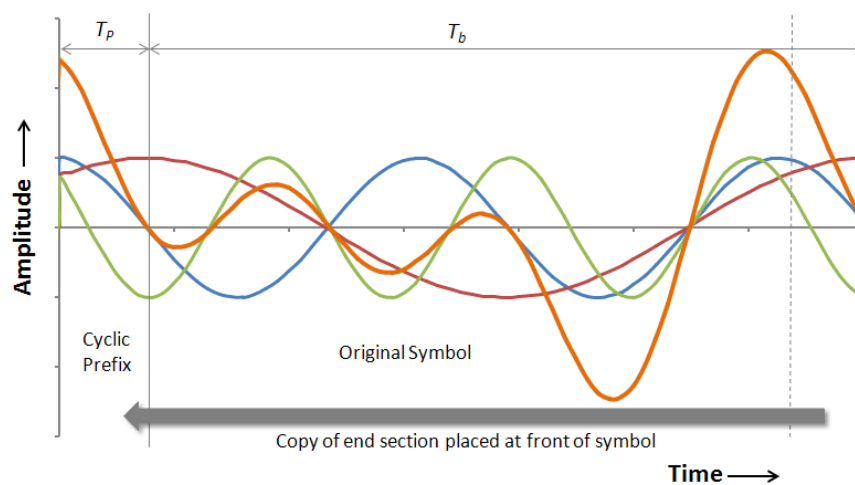
Fig. 2.9 Cyclic Prefix Insersion (Individual subcarriers:red, blue, green. Combined signal:orange)

Considering a single subcarrier, due to the orthogonal property, the cyclic prefix will provide a smooth continuation of the subcarrier phase between the cyclic prefix region and the original symbol region. At the receiver the signal within the cyclic prefix region will spread into the symbol region due to channel dispersion and prevent leading edge distortion of the symbol. By selecting the optimum window for recovering the transmitted signal and if the ISI duration is less than the cyclic prefix duration an undistorted signal over a full symbol period, T_b, can be selected for decoding. Furthermore, if the cyclic prefix is longer than the ISI period there is a sliding window for optimum signal recovery giving some tolerance on window positioning. The effect of cyclic prefix on the received signal for one subcarrier is shown in Fig. 2.10, here the symbol period indicated as symbol $m+1$ is not affected by ISI from the previous symbol, as the cyclic prefix is longer than the maximum differential signal delay. Also the symbol leading edge is undistorted due to the cyclic prefix leaving the complete symbol undistorted. The phase shift due to the channel

dispersion is also clearly seen in Fig. 2.10. The cyclic prefix is therefore able to completely remove the effect of the ISI and so is highly effective at improving system tolerance to channel dispersion.
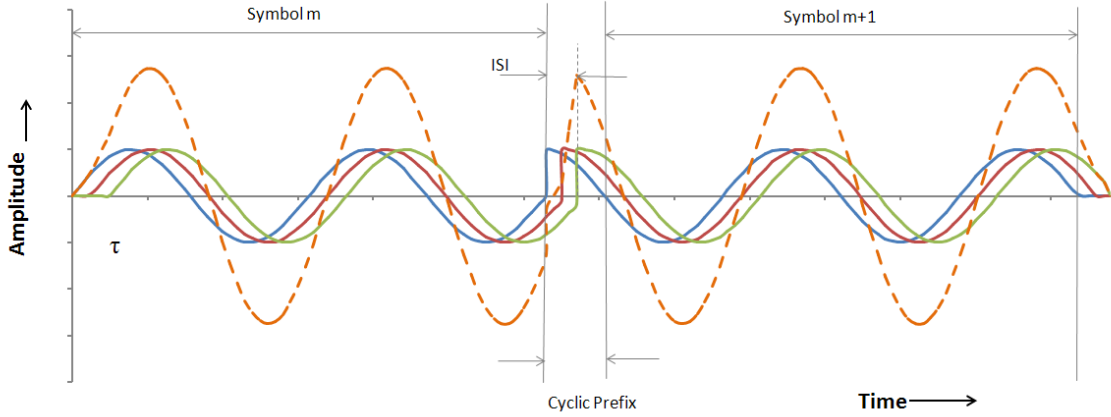
Fig. 2.10 Received symbols with cyclic prefix

The drawback of the cyclic prefix however is that effective signal bit rate, or net bit rate, is reduced if subcarrier frequencies remain fixed, as the time to transmit a complete symbol is increased by T_p, where T_p is the duration of the cyclic prefix. Total symbol length is therefore becomes T_p+T_b. A cyclic prefix parameter η can be defined as follows:

$$\eta = \frac{T_p}{T_b} \tag{2.16}$$

The signal line rate defined in Eq.(2.7,2.8) will remain the same, however with the addition of a cyclic prefix, the net bit rate R_N is now reduced compared to R_L as defined below:

$$R_N = \frac{R_L}{(1 + \eta)} \tag{2.17}$$

Spectral efficiency is also reduced by a similar factor of $1/(1 + \eta)$.

It is interesting to note that the spectrum of the transmitted subcarriers will become narrower due to the extended symbol period. If frequency spacing is unchanged the subcarrier frequencies no longer coincide with the nulls in the other subcarrier spectra. The signal spectrum is only restored to that shown in Fig. 2.5 when the cyclic prefix is removed in the OFDM receiver.

2.3.5 D-A and A-D Conversion, Quantisation and Clipping

The OFDM signal is processed in the transmitter and receiver as a digital signal, which must be converted to an analogue form for transmission. The digital-to-analogue conversion in the transmitter and analogue-to-digital conversion in the receiver are performed by a DAC and ADC respectively. The DAC/ADC technology will typically limit the maximum resolution of the OFDM signal samples rather than the DSP hardware. ADCs in particularly become limited in resolution as sample rate increases due to finite conversion times. The OFDM signal samples are therefore limited to a fixed number of bits of resolution, this has a number of effects on the signal characteristics which limit system performance;

- *Quantisation Noise*: A sample with a resolution of q bits can only represent $2^q - 1$ discreet levels, therefore quantisation nose is present which has greater effect as the signal amplitude reduces.
- *Signal Clipping*: The sample can only represent a finite range of values therefore if the signal to be converted is outside the possible range it must be limited, or clipped, to the nearest quantised level.
- *Dynamic Range*: The above two effects combine to give a limited dynamic signal range, the maximum signal amplitude is limited by the clipping effect and the minimum signal amplitude is limited by the quantisation noise.

As the signal path loss varies with transmission distance and can also vary over time the received signal's peak-to-peak amplitude will vary. To avoid signal clipping and to minimise quantisation noise the amplitude of the received signal should be adjusted to match the full-scale range of the ADC. This is achieved with an automatic gain control (AGC) circuit which monitors the peak-to-peak signal amplitude and adjusts the receiver gain accordingly.

A characteristic of OFDM signals is a high peak-to-average power ratio (PAPR). An example signal is shown in Fig. 2.11(a) with a high PAPR. If a single OFDM symbol is considered the theoretical maximum PAPR is dependent on the number of subcarriers (PAPR α $\log_{10} N_{SC}$) however the probability of this maximum occurring is low and statistically the PAPR is well below the theoretical peak but still relatively high. The

disadvantage of a high PAPR is that the quantisation noise will degrade the signal more as quantisation noise effect is higher at lower signal amplitudes. To reduce this effect the digital signal can be intentionally clipped at the transmitter and the clipped signal amplitude matched to the quantisation range of the DAC. For a signed digital signal *S(t)* before clipping, $S_{clip}(t)$ is the signal symmetrically clipped at $\pm C$, defined as follows:

$$S_{clip}(t) = \begin{cases} S(t), & -C \leq S(t) \leq C \\ C, & S(t) > C \\ -C, & S(t) < -C \end{cases} \tag{2.18}$$

If Λ is the analogue signal amplitude corresponding to the digital clipping level *C* and P_m is the corresponding average signal power, the clipping ratio ζ is defined as Λ^2 / P_m. Clipping ratio is more commonly defined in dB as $\zeta \, (dB) = 10\log_{10}(\Lambda^2 / P_m)$.
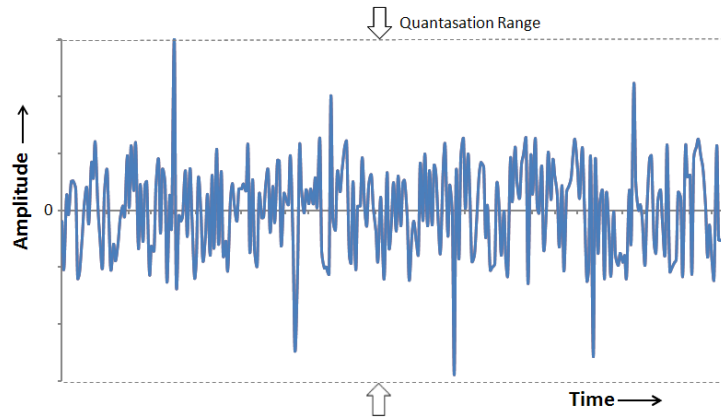
(a)
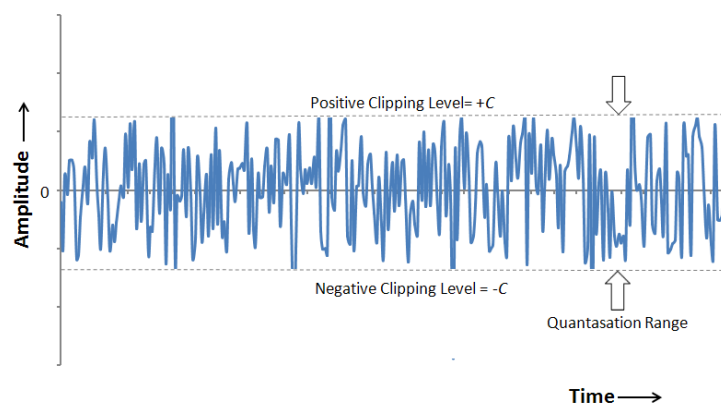
(b)

Fig. 2.11 (a) Unclipped OFDM signal with high PAPR, (b) Clipped OFDM signal with reduced PAPR

An example of a clipped OFDM signal is shown in Fig. 2.11(b) where the PAPR is reduced. The clipping will cause signal distortion however this is offset by a larger gain from lower quantisation noise. The number of signal quantisation bits and the selected clipping level are therefore key parameters that affect OFDM system performance.

2.3.6 RF Modulation

The output from the DAC in the OFDM transmitter is a baseband analogue signal, which can be directly transmitted in a baseband channel or modulated onto a carrier frequency for transmission in a limited RF band. In all existing wireless OFDM systems the signal is modulated onto an RF carrier. As stated in section 2.3.2 a carrier can support I/Q modulation so a complex time domain OFDM signal is typically used. A real-valued time domain signal can also be modulated onto a carrier, this would however only achieve half the spectral efficiency compared to the I/Q modulation case.

When RF modulation is employed the frequency of the local oscillator (LO), for down-conversion at the receiver, is ideally synchronised to the transmitter carrier frequency, if there is any carrier frequency offset (CFO) this leads to inter-channel interference and [18]. The typical method of LO synchronisation is to transmit pilot symbols which the receiver uses to detect the rate of change of carrier phase and therefore estimate CFO. The LO frequency is then adjusted based on the estimated CFO. The phase of the RF carrier must also be determined to allow correct demodulation, this can also determined with the pilot symbols to determine the absolute phase of the carrier. The carrier phase can drift in a time varying channel, such as a wireless mobile channel, so the carrier phase must be continuously tracked.

To implement RF modulation various components are needed such as mixers, oscillators, amplifiers and filters. As the OFDM signal is an analogue signal it is sensitive to distortion which is dependent upon component characteristics such as linearity, noise figure, frequency response, return loss etc. The characteristics of the RF components must therefore be considered carefully when designing the modulation and demodulation circuits.

For the case of baseband transmission there are no RF modulation-induced signal distortions. Baseband transmission is therefore preferable if possible as it can lead to reduced transceiver cost.

2.3.7 Channel Estimation and Equalisation

The frequency response of the transmission channel will introduce subcarrier amplitude and phase changes during transmission, the received signal is therefore no longer a direct representation of the transmitted signal. To compensate the effect of the channel response the inverse channel response is applied in the receiver which is termed channel equalisation. In order to perform equalisation the channel transfer function (CTF) must be estimated. An advantage of OFDM is that channel equalisation is extremely simple. As the amplitude and phase of each subcarrier is determined at a discreet frequency the CTF only needs to be known at the corresponding frequency to allow the subcarrier to be equalised. Equalisation can then be achieved by a single complex multiplication in the frequency domain.

To determine the CTF at the subcarrier frequencies, pilot symbols P_k are periodically transmitted on each subcarrier with known amplitude, A_k and phase θ_k, defined as:

$$P_k = A_k e^{j(2\pi\frac{k}{N}n+\theta_k)}$$

(2.19)

The corresponding received pilot symbol is:

$$Q_k = B_k e^{j(2\pi\frac{k}{N}n+\phi_k)} + W_k$$

(2.20)

where W_k is the noise component of the *kth* output of the receiver DFT. The CTF in the frequency domain, H_k, is then determined as:

$$H_k = \frac{Q_k - W_k}{P_k} = \frac{B_k}{A_k} e^{j(\phi_k - \theta_k)}$$

(2.21)

the CTF is estimated as:

$$\widehat{H}_k = \frac{Q_k}{P_k} = H_k + \frac{W_k}{P_k}$$

(2.22)

A large pilot symbol amplitude therefore reduces error due to noise. To further reduce the effects of channel noise the estimated CTF can be averaged over many pilot symbols as long as the channel can be considered semi-static over the averaging period. Also it is possible to only determine the CTF at distributed subcarrier frequencies and interpolate to determine the CTF at the remaining subcarriers.

To equalise the received frequency domain data, $d'_{k,m}$ encoded onto the kth subcarrier a single multiplication by the inverse CTF estimate , $\widehat{H}_k^{-1}$, is applied, the equalised encoded data value $d''_{k,m}$ is therefore defined as:

$$d''_{k,m} = \widehat{H}_k^{-1} d'_{k,m} \tag{2.23}$$

2.3.8 Synchronisation

Synchronisation is an important aspect of OFDM transmission which involves synchronisation between the transmitter and receiver of sample clock frequency and symbol timing. For OFDM systems involving modulation of RF carrier frequencies synchronisation of carrier frequency and carrier phase are also required.

Symbol Timing Offset and Synchronisation

The OFDM receiver must estimate the received symbol boundaries as accurately as possible to optimise symbol decoding, the offset between the estimated symbol boundary and the actual symbol boundary is the symbol timing offset (STO). Once the receiver has identified the symbol position, a portion of length T_b can be sampled from the region unaffected by ISI, this is then used for input to the DFT, this selected portion of the symbol is thus termed the DFT window. The symbol region where the DFT window can be safely selected will be longer than T_b if the ISI length is less than the cyclic prefix length T_p, thus allowing some variation in the start position of the DFT window. Variation in the DFT window location will induce an effective phase shift of the subcarriers however as this is indistinguishable from channel induced phase shift it will be compensated as part of the channel equalisation. If the DFT window is incorrectly selected due to excessive STO, then the effect of ISI is not removed or the DFT window will consist of parts from two symbols which will severely degrade performance.

If symbol synchronisation methods are considered for existing OFDM systems, the packet based systems, such as WLAN, require a different approach to broadcast systems, such as DVB. A WLAN receiver for example must determine the symbol location for each individual packet due to random inter-packet intervals. Whereas for the broadcast system employing continuous transmission the receiver can utilise several symbol periods to accurately acquire symbol synchronisation. Both packet-based and broadcast systems however utilise the same basic symbol synchronisation principle which is based on cross-correlation of the received signal with a known training pattern. The peak of the cross-correlation function will indicate the offset between the known training pattern and the received training pattern thus locating the symbol position. Packet-based systems utilise a training sequence within the packet preamble, whereas broadcast systems can use periodically inserted training symbols known as pilot symbols. It is also possible for broadcast systems to perform symbol synchronisation by employing auto-correlation to detect the cyclic prefix, as it is a duplicated sequence within each symbol.

Sampling Clock Offset and Synchronisation

In an OFDM based network a system reference clock will be located at one node in the network, typically the node which aggregates traffic and controls the network. Other nodes in the network must synchronise their timing to this "master" node. If an OFDM receiver is not precisely synchronised to the reference clock there will be offset between the sampling clock in the receiver compared to the sampling clock in the corresponding transmitter. Sampling clock offset (SCO) has two effects; a slow drift in the sampling positions causing subcarrier phase shift (constellation rotation) proportional to the subcarrier index and due to different subcarrier spacing in the transmitter and receiver, the discrete subcarrier frequencies utilised by the DFT in the receiver do not match the transmitted subcarrier frequencies. The mismatch of subcarrier frequencies, which is more pronounced at higher frequencies, causes inter-channel-interference (ICI) as there is no longer a single frequency component at the receiver's subcarrier frequencies.

For sampling clock synchronisation the general technique is to estimate the SCO in the receiver and then compensate for the offset. The compensation can be performed by adjusting the frequency of a voltage controlled oscillator (VCO) based on the estimated SCO, this achieves synchronous sampling as the receiver sample clock will closely track

the transmitter sample clock. Alternatively a free running asynchronous oscillator generates the receiver sample clock with a low SCO. If the SCO is small enough the resulting phase rotation of each subcarrier can be determined from the estimated SCO and therefore can be compensated for. To estimate the SCO the linear relationship between SCO induced subcarrier phase shift, $\varphi_{n,k}$, and SCO is used:

$$\varphi_{n,k} = 2\pi n k \frac{\Delta f_s}{f_s} \tag{2.24}$$

where n and k are the symbol index and subcarrier index respectively, Δf_s is the SCO in Hz and f_s is the sampling frequency in the transmitter in Hz. To determine $\varphi_{n,k}$, known pilot symbols $P_{n,k}$ are transmitted, the received pilot symbols are then defined as follows, if noise and ICI are ignored:

$$R_{n,k} = H_k P_{n,k} e^{j2\pi k n \frac{\Delta f_s}{f_s}} \tag{2.25}$$

where H_k is the channel frequency response and is assumed to be semi-static such that any phase changes due to variations in H_k occur slowly in comparison to the SCO induced phase changes.

The phase shift between two pilot symbols placed α symbols apart is then:

$$\varphi_k = \varphi_{n,k} - \varphi_{n-\alpha,k} = arg\{R_{n,k}\,R^*_{n-\alpha,k}\} = arg\left\{|H_k P_k|^2 e^{j2\pi k\alpha\frac{\Delta f_s}{f_s}}\right\} = 2\pi k\alpha \frac{\Delta f_s}{f_s} \tag{2.26}$$

therefore Δf_s is calculated from:

$$\Delta f_s = \frac{\varphi_k f_s}{2\pi k\alpha} \tag{2.27}$$

To reduce the effect of noise Δf_s would be averaged over many pilot symbols. It should be noted that pilot symbols do not need to be transmitted on all subcarriers however when pilots are used at multiple frequencies the determined SCO values are averaged.

Carrier Frequency and Phase Offset and Synchronisation

In OFDM systems that employ RF carriers the frequency of the LO used for down-conversion in the receiver is ideally exactly the same as the RF carrier frequency, any carrier frequency offset (CFO) will result in an unwanted frequency shift of the down-converted baseband signal. The frequency offset of the baseband signal results in all subcarriers undergoing the same frequency shift, this will cause ICI due to misalignment of the down-converted subcarriers with the ideal subcarrier frequencies and also an equal phase shift (constellation rotation) on all subcarriers. The CFO must therefore be estimated so that the phase shift can be corrected and small enough so that performance degradation due to ICI is acceptable. Variations in channel characteristics, especially wireless channels, can result in the phase of the received carrier slowly varying over time causing carrier phase offset (CPO), both the relative phase and the phase drift between the LO frequency and the received carrier frequency must be determined and then compensated as the demodulated I and Q values depend upon the phase relationship between the carrier frequency and the LO frequency. Both CFO and CPO can be estimated by the use of pilot tones where the phase of the received pilot tones are processed to determine an absolute phase shift corresponding to CPO and a time varying phase shift corresponding to CFO. As RF carrier modulation is not employed in the research work presented in this thesis it is not considered necessary to provide details of the fundamentals behind CFO and CPO estimation.

The sensitivity of the OOFDM system to these synchronisation issues is dependent on various system parameters, including the number of subcarriers and the modulation formats employed. For example lower modulation formats offer higher tolerance to synchronisation errors as constellation points can rotate further before crossing decision boundaries.

2.4 Optical OFDM

Optical OFDM (OOFDM) was introduced and its potential applications discussed in chapter 1. The basic principle of OOFDM is to modulate an optical carrier, at a standard telecom wavelength such as 1550nm, using an OFDM signal for transmission in optical

fiber networks. Implementation of OFDM in the optical domain follows the principles described in sections 2.2 and 2.3 with the addition of an Electrical-to-Optical (E/O) converter in the transmitter and an Optical-to-Electrical (O/E) converter in the receiver. There are two main variants of the OOFDM technique; coherent OOFDM (CO-OFDM) and Intensity Modulation and Direct Detection (IMDD) OOFDM. The next sections describe and compare the two OOFDM variants. Also OOFDM with adaptively subcarrier loading is described and the advantages and disadvantages of the OOFDM technique are outlined in detail.

2.4.1 Coherent OOFDM

CO-OFDM was first proposed by Shieh and Athaudage [19], it offers superior performance in terms of receiver sensitivity, spectral efficiency, tolerance to chromatic and polarisation dispersion and therefore offers the greater system capacity-reach performance. However this performance requires high transceiver complexity which results in higher cost compared to an IMDD OOFDM based system. The CO-OFDM system achieves the superior performance by achieving high linearity in the E/O and O/E conversion processes.
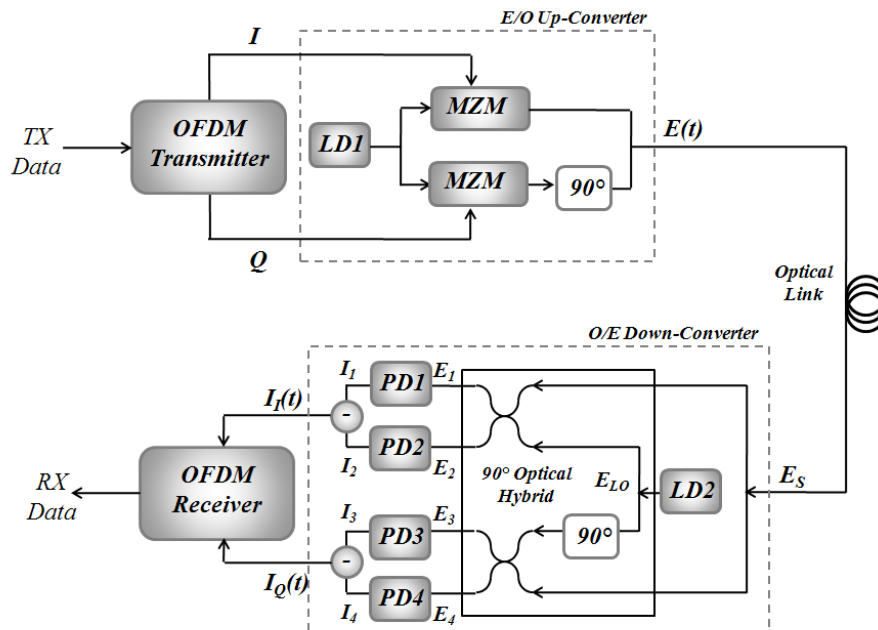
MZM: Mach-Zehnder Modulator, LD: Laser Diode (DC Bias not shown), PD: PIN Diode

Fig. 2.12 CO-OFDM Transmission System with Direct Up/Down Conversion

The block diagram of a typical CO-OFDM system is shown in Fig. 2.12, consisting of OFDM transmitter, E/O up-converter, optical channel, O/E down-converter and OFDM

receiver. CO-OFDM employs modulation of the optical field therefore it can support complex time domain signals and so both positive and negative frequency subcarriers can be used to carry data. The OFDM transmitter thus employs two DACs to convert the real and imaginary signal parts, referred to as the I and Q components respectively. Direct E/O up-conversion is performed by I/Q modulation of a continuous wave (CW) optical carrier by two Mach-Zehnder Modulators (MZMs) to up-convert the I and Q signal components. A 90° phase shift being applied to the Q component before combining with the I component to achieve the correct phase relationship. If *S(t)* represents the complex electrical OFDM signal and the MZM is assumed to provide linear conversion, the complex optical field *E(t)* is therefore defined as:

$$E(t) = A_c \cdot S(t)e^{j(\omega_{LD1}t + \phi_{LD1})} \tag{2.28}$$

where *E(t)* is the complex form of the optical field, ω_{LD1} and ϕ_{LD1} are the angular frequency and phase of the CW laser before modulation and A_C is a proportionality constant. In practice the optical field amplitude generated by a MZM is a cosine function of the driving voltage, so operation is restricted to the near linear operating region and the MZM is biased at the null point which is at the center of the linear region. The operating conditions of the MZM will therefore impact E/O up-conversion linearity and CO-OFDM system performance [20].

It is also possible to implement intermediate frequency (IF) E/O up-conversion where an electrical RF carrier is first I/Q modulated and then up-converted by a single MZM. This architecture employs fewer components than direct conversion however it increases the necessary bandwidth of various components.

The O/E down converter in Fig. 2.12 employs a local oscillator (LO) laser (LD2 with amplitude L_{LO}, angular frequency ω_{LD2} and phase and ϕ_{LD2}, for mixing with the receiver signal. A 90° optical hybrid and two pairs of balance photo detectors (PD1-4) are used for signal detection. If imbalance and loss are ignored the optical hybrid generates 4 signals from the received signal E_S and the LO signal E_{LO} defined as follows:

$$E_1 = \frac{1}{\sqrt{2}}(E_s + E_{LO}), \qquad E_2 = \frac{1}{\sqrt{2}}(E_s - E_{LO})$$

$$E_3 = \frac{1}{\sqrt{2}}(E_s - jE_{LO}), \quad E_4 = \frac{1}{\sqrt{2}}(E_s + jE_{LO}) \tag{2.29}$$

The balanced photo detector pair PD1 and PD2 (PD3 and PD4) detect and combine the signals E_1 and E_2 (E_3 and E_4) to generate photo currents I_1 and I_2 (I_3 and I_4). Using a photo-detection responsivity of unity for simplicity, I_1 and I_2 are defined as:

$$I_1 = |E_1|^2 = \frac{1}{2}\{|E_s|^2 + |E_{LO}|^2 + Re[E_s E_{LO}^*]\} \tag{2.30}$$

$$I_2 = |E_2|^2 = \frac{1}{2}\{|E_s|^2 + |E_{LO}|^2 - Re[E_s E_{LO}^*]\} \tag{2.31}$$

where * denotes complex conjugate and Re (Im) denotes the real (imaginary) part of a complex signal. The I component of the photocurrent $I_I(t)$ is determined from I_1 and I_2 as:

$$I_I(t) = I_1 - I_2 = Re[E_s E_{LO}^*] \tag{2.32}$$

It should be noted that although received ASE noise and LO laser intensity noise have been ignored the terms that would be generated, if included in Eq.(2.30,2.31), would then cancel out in Eq.(2.32) in a similar way to the signal-to-signal beat noise components cancellation by the balanced detectors.

Similarly it can be shown that the Q component of the photocurrent $I_Q(t)$ is determined from I_3 and I_4 from PD3 and PD4 as:

$$I_Q(t) = I_3 - I_4 = Im[E_s E_{LO}^*] \tag{2.33}$$

where $I_3=|E_3|^2$ and $I_4=|E_4|^2$. $I_I(t)$ and $I_Q(t)$ therefore provide real and imaginary components of $E_S^* E_{LO}$ which is the essentially a linear replica of the received optical signal down-converted by the LO laser. The photocurrents $I_I(t)$ and $I_Q(t)$ are converted to voltages by transimpedance amplifiers with gain G (V/A) making the received complex OFDM signal voltage:

$$S'(t) = G\{I_I(t) + jI_Q(t)\} = GE_s E_{LO}^* \tag{2.34}$$

The signals $GI_I(t)$ and $GI_Q(t)$ are converted by separate DACs in the OFDM receiver therefore $S'(t)$ is represented digitally by separate I and Q samples. As ω_{LD1} and ω_{LD2}

(ϕ_{LD1} and ϕ_{LD2}) will have frequency (phase) offset $\Delta\omega=\omega_{LD1}-\omega_{LD2}$ ($\Delta\phi=\phi_{LD1}-\phi_{LD2}$) then *S'(t)* can be written as:

$$S'^{(t)} = \left\{\left\{G \cdot A_c \cdot L_{LO} \cdot S(t)e^{j(\Delta\omega t+\Delta\phi)}\right\} \otimes h_o(t)\right\} + n(t) \qquad (2.35)$$

where $\otimes$ stands for convolution, *$h_o(t)$* is the channel impulse response in the optical domain and *n(t)* is a noise component. Eq.(2.35) clearly shows the linear relationship between *S'(t)* and *S(t)* and so in theory the fibre dispersion effects can be fully compensated with frequency domain equalization and cyclic prefix. To recover *S(t)* the channel response *h(t)* (and $\Delta\phi$) are equalised, also the frequency offset $\Delta\omega$ must be estimated and compensated [21] which is achieved through pilot based DSP algorithms in the receiver. Phase noise however cannot be compensated and so the LO requires a low linewidth laser [22] in the region of 100kHz.

2.4.2 IMDD OOFDM

An IMDD OOFDM system is shown in Fig. 2.13. The 5 main system elements are the same as in the CO-OFDM system. Compared to CO-OFDM the very simple E/O and O/E converters of the IMDD system significantly reduce system complexity and therefore system cost. The OOFDM system operates with a real-valued signal therefore a single DAC and ADC are required in the transmitter and receiver respectively which also lead to lower system cost. The real-valued signal can support a baseband OFDM signal with (*N*/2)-1 data carrying subcarriers as described in section 2.3.2, or a complex OFDM signal can be supported if digital I/Q modulation and demodulation of a carrier are performed by the DSP hardware of the transmitter and receiver respectively. The second approach can utilise *N*-1 data carrying subcarriers however due to the double-sideband carrier there will be no increase in spectral efficiency compared to the baseband case. In the transmitter intensity modulation (IM) is used for the E/O up-conversion, thus the power of the optical signal is varied in proportion to the generated OFDM signal. This can be achieved either by a directly modulated laser (DML), where the laser current is generated by combining the OFDM signal with a DC bias current, or by external modulation of a CW laser source with a modulator such as a MZM or a semiconductor optical amplifier (SOA). If the real-valued OFDM signal is *s(t)* and the DC bias signal is V_{DC} then, ignoring any non-linearities or laser phase noise, the intensity modulated optical signal is defined as:

$$E(t) = A_I \cdot \sqrt{V_{DC} + s(t)} \cdot e^{j(\omega_{LD}t + \phi_{LD})} \qquad (2.36)$$

where *E(t)* is the complex form of the optical field, ω_{LD} and ϕ_{LD} are the angular frequency and phase of the laser and A_I is a proportionality constant. To prevent signal distortion V_{DC} must exceed the peak value of $S_r(t)$ such that the laser is always positively biased above the lasing threshold and operates in its linear region. A significant portion of the optical signal power is therefore present at the optical carrier frequency which will limit signal extinction-ratio (ER) [23].

Considering the two IM variants, the DML is a significantly lower cost solution compared to the external modulator option, making it highly suitable for cost sensitive applications. However DMLs suffers from the non-linear frequency chirp effect which can decrease the dispersion tolerance of the OOFDM technique as it effectively increases the signal dispersion in fibers with positively dispersion coefficients [24].
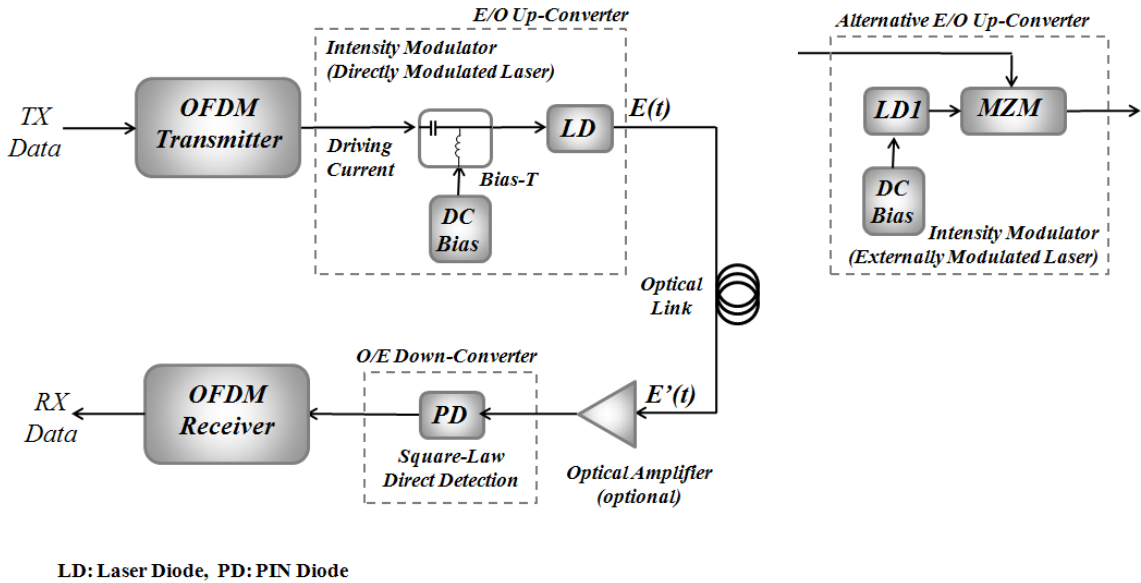

Fig. 2.13 IMDD OOFDM System

During transmission the signal can be optically amplified to compensate fiber loss, although the aim of OOFDM is to eliminate the need for amplifiers or dispersion compensating fibers (DCF) and keep the optical link as simple and therefore as low cost as possible.

At the receiver the optical signal undergoes direct detection (DD) by a square-law PIN photodetector. If the received optical signal is $E_R(t)$ and using a photo-detection responsivity of unity for simplicity, the detected photocurrent $I_R(t)$ is given as:

$$I_R(t) = |E_R(t)|^2 = \left|\left\{\left(A_I \cdot \sqrt{V_{DC} + s(t)} \cdot e^{j(\omega_{LD}t + \phi_{LD})}\right) \otimes h(t)\right\}\right|^2 + w(t) \quad (2.37)$$

where $h(t)$ is the channel impulse response and $w(t)$ represents receiver generated noise. Using the Taylor series expansion on the square root term in Eq. (2.37), ignoring the noise component and ignoring the laser phase for simplicity, the detected signal becomes:

$$I_R(t) = A_I^2 \left\{\left[\left(\sqrt{V_{DC}} + \frac{s(t)}{2\sqrt{V_{DC}}} - \frac{s^2(t)}{8(V_{DC})^{3/2}} + \cdots\right) \cdot e^{j\omega_{LD}t} \otimes h(t)\right] \right.$$

$$\left. \times \left[\left(\sqrt{V_{DC}} + \frac{s(t)}{2\sqrt{V_{DC}}} - \frac{s^2(t)}{8(V_{DC})^{3/2}} + \cdots\right) \cdot e^{j\omega_{LD}t} \otimes h(t)\right]^*\right\} \quad (2.38)$$

$$= A_I^2 \left\{V_{DC} + \frac{s(t) \otimes [h(t) + h^*(t)]}{2} - \frac{s^2(t) \otimes [h(t) + h^*(t)]}{8V_{DC}} + \cdots\right\}$$

On the right hand side of Eq.(2.38) the first term represents the DC bias component, the second term contains the OFDMs signal to be recovered and the remaining terms represent the unwanted subcarrier intermixing products due to the square-law detection.

Before sampling by an ADC the photocurrent is linearly converted to a voltage V_R by a transimpedance amplifier (TIA) and an RF gain stage suitably adjusts signal amplitude and DC offset for the ADC. A low-pass filter is also employed before the ADC as an anti-aliasing filter. The transmitted OFDM signal $s(t)$ can then be recovered after channel equalisation in the receiver DSP.

Two key disadvantages of the DD-based OOFDM systems are i) the low signal ER due to the high relative optical carrier power, as shot noise is proportional to received optical power the lower ER leads to reduced effective SNR and ii) the nonlinear square-law detection introduces unwanted subcarrier intermixing products which interfere with the received signal [25].

After the O/E down-conversion the OFDM receiver adjusts the received RF signal gain and low-pass filters the OFDM signal before sampling with a single ADC. The transmitted data is then recovered using the receiver functions described in section 2.3.

2.4.3 Comparisons between Coherent OOFDM and IMDD OOFDM

Having described the fundamental structures of the CO-OFDM system and the IMDD OOFDM system in sections 2.4.1 and 2.4.2 various aspects are compared in Table 2.1 below. The general conclusion is that CO-OFDM involves highly complex E/O and O/E conversion compared to IMDD, which can offer highly linear conversion between electrical and optical domains, thus achieving superior performance in many aspects. IMDD OOFDM in comparison is much lower in complexity which results in some performance reduction but achieves superior cost-effectiveness. CO-OFDM is thus suitable for long-haul applications whereas IMDD is ideal for cost-sensitive access networks and LANs.

Table 2.1 *Comparison of CO-OFDM and IMDD OOFDM*

	Coherent OOFDM	**IMDD OOFDM**
E/O Up-conversion	Direct or IF optical field I/Q modulation	Optical intensity modulation
O/E Down-conversion	Coherent detection with local oscillator	Square-law direct detection (no local oscillator)
OFDM Signal Format	Complex valued	Real valued
Data carrying subcarriers	N_{SC}-2	(N_{SC}/2)-1
Synchronisation	FFT window, receiver clock, LO laser offset	FFT window, receiver clock
Dispersion Tolerance	Theoretically unlimited	Limited by DMLs and square-law direct detectors
Complexity and Cost	Higher complexity & cost	Lower complexity & cost
Applications	Long-haul core networks	Access networks & LANs

2.4.4 OOFDM with Adaptive Subcarrier Loading

A major advantage of OOFDM is its unique ability to effectively utilise the available channel spectral characteristics and therefore maximise capacity-reach performance. The OOFDM signal adapts to the channel response by applying adaptive loading to its subcarriers. Adaptive loading varies the power of a subcarrier and/or the number of bits loaded onto the subcarrier, according to channel-induced signal properties such as SNR at the subcarrier frequency. If a subcarrier experiences high SNR then low power or a high modulation format would be used, likewise if a subcarrier experiences a low SNR then high power or a low modulation format would be used. By adapting the power and/or bits of each subcarrier the BER of each subcarrier can be controlled. By optimising the adaptive loading of all subcarriers the overall system BER can then be optimised. To initialise the adaptive loading parameters a suitable algorithm, involving negotiations between the transmitter and receiver, iteratively adjusts the loading parameters to achieve the minimum BER for a fixed line rate or alternatively the maximum line rate at a predetermined BER. Although adaptive loading generally compensates for system frequency response it will also allow compensation of other factors which degrade SNR at the receiver. For example if some subcarriers suffer more interference from subcarrier intermixing products than others, the subcarrier power and/or modulation formats for the affected subcarriers can be adapted accordingly. The three adaptive loading schemes are denoted: power loading, bit loading and power/bit loading [26,27]. The following sections discuss the principles of the three adaptive loading schemes in detail.

Adaptive Power Loading:

To implement adaptive power loading a common modulation format must be selected for all subcarriers which fixes the system bit rate as defined by Eq.(2.7)-(2.8). Power loading then provides pre-emphasis of the subcarrier powers in the transmitter to compensate the variations in the frequency response of the OOFDM system. Fig. 2.14 shows an example channel response and the corresponding subcarrier power levels for perfect compensation leading to equal subcarrier powers at the receiver. If the CTF is H_k and P_0(dB) is the optimum subcarrier power for a lossless channel then the adapted subcarrier power P_k(dB) of the kth subcarrier is defined as:

$$P_k(dB) = P_0(dB) - 20\log_{10}|H_k| \qquad (2.39)$$

In practice it may not be possible to achieve perfect compensation due to limited subcarrier power dynamic range in the transmitter. Also for excessively attenuated subcarriers it may be necessary to drop the subcarrier completely as BER would be unacceptable.
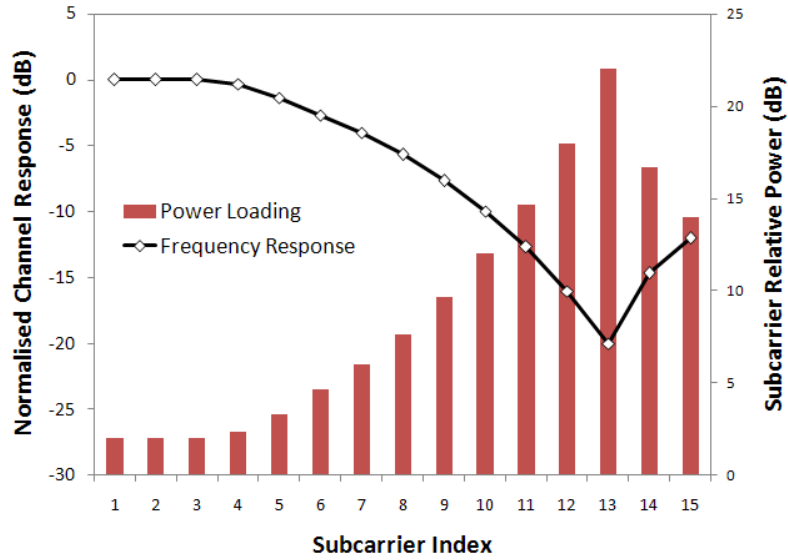
Fig. 2.14 Adaptive Power Loading Scheme

Fig. 2.15Adaptive Bit Loading Scheme

Adaptive Bit Loading:

To implement adaptive bit loading the average power of all subcarriers is set to be identical and the modulation format, which determines bits per subcarrier, is adapted according to the channel SNR at the subcarrier frequency. Where the channel SNR is larger higher modulation formats can be employed, however where the channel SNR is smaller lower

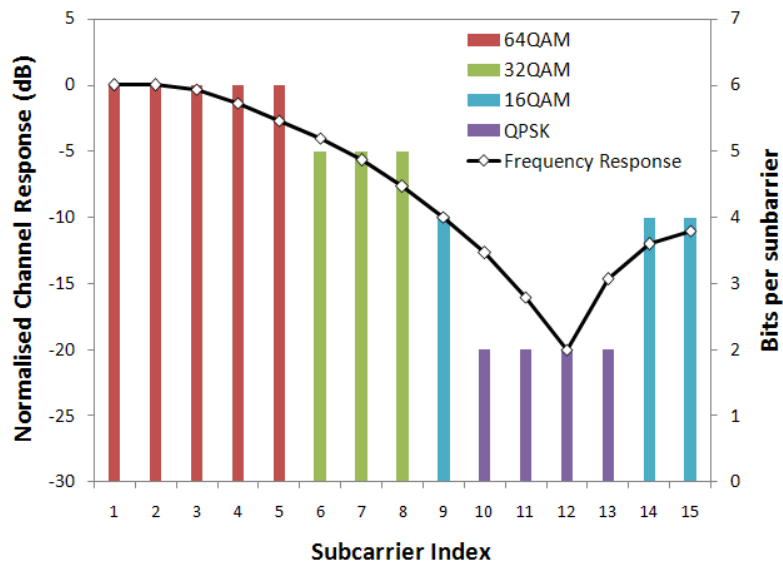modulation formats must be employed. The total bit rate of the system is as defined by Eq.(2.7),(2.17). Fig. 2.15 illustrates an example adaptive bit loading scheme.

Adaptive Power/Bit Loading:

To implement adaptive power/bit loading both the subcarrier power and modulation format can be adapted during initial transceiver and receiver negotiations. This gives greater flexibility in subcarrier properties and can lead to increased capacity-reach performance compared to the two other loading schemes. The required loading algorithm and the system complexity will however be the highest of the three schemes.

2.5 Passive Optical Networks based on OOFDM

In chapter 1 the advantages of the OOFDM technique and its potential application in PONs were presented, this section explores the advantages and different techniques for implementing OOFDM-based PONs. First it is worth outlining the basic structure of a PON access networks. PONs are point-to-multipoint networks where a single optical line terminal (OLT) at the network operator's central office (CO) supports multiple optical network units (ONUs) located at the customers' premises. Fig. 2.16 illustrates the fundamental structure of a PON where a feeder fiber, ranging from around 20-60km, from the OLT divides into multiple distribution fibers, typically up to a few km each and of varying lengths, to connect to the ONUs. The coupling between the feeder fiber and the distribution fibers can be based on power splitting or wavelength splitting. The PON ideally supports many 10s of ONUs. The architecture in Fig. 2.16 can support bidirectional transmission with downstream and upstream traffic decoupled by either separate fibers for each direction, or by employing different wavelengths. Sophisticated wavelength reuse schemes have also been proposed where upstream and downstream traffic operate at the same wavelength over a common fiber [28].
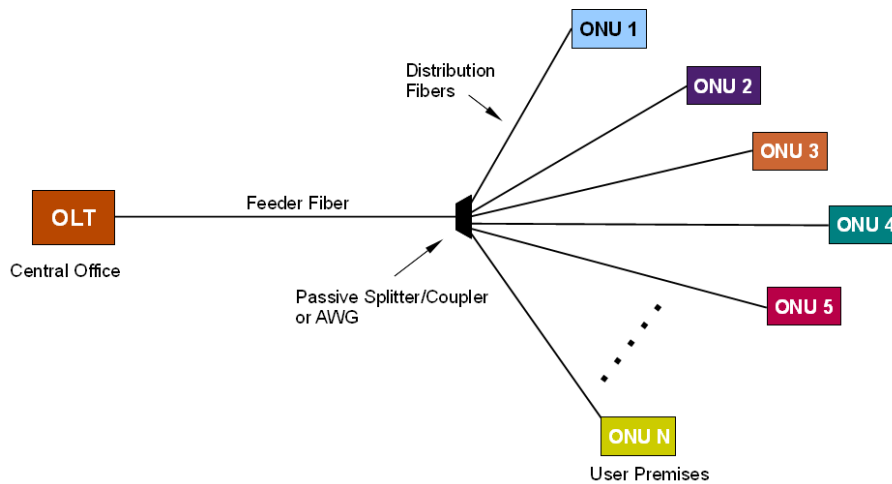
Fig. 2.16 Fundamental PON Architecture

There are three traditional types of ON/OFF keying-based PONs: time division multiplexing (TDM) PONs [29], wavelength division multiplexing (WDM) PONs [30], hybrid TDM/WDM PONs [30]. A TDM PON employs TDM to convey downstream signals from the OLT to the ONUs, and time division multiple access (TDMA) to multiplex upstream signals, on a separate wavelength, from the ONUs to the OLT. As a direct result, future high-speed TDM PON transceivers suffer serious design constrains in terms of ultra-fast burst mode operation receivers, complex scheduling algorithms and framing technologies, as well as pronounced sensitivity to packet latency. In WDM PONs, data information is transmitted over a pair of dedicated wavelengths assigned to a particular ONU for both downstream and upstream transmission directions. For widespread global deployment of WDM PONs, the most critical challenges are cost-effectiveness and flexibility [30]. Key issues that must be solved to meet these challenges are, for example, colourless network operation and the fundamental alteration to legacy PON ODNs. Whilst the restricted flexibility of WDM PONs is mainly due to the fact that dynamic bandwidth allocation (DBA) cannot be performed statistically at a sub-wavelength granularity. In hybrid TDM/WDM PONs, a number of wavelengths are utilized in each direction to link the OLT to multiple ONUs, and each individual wavelength is shared among a number of ONUs rather than being dedicated to a single ONU, therefore, it is envisaged that hybrid TDM/WDM PONs inherit, to some extent, the majority of the abovementioned technical challenges associated with TDM PONs and WDM PONs, despite the fact that future TDM/WDM PONs will gradually evolve from a fixed wavelength configuration into a tuneable wavelength configuration.

2.5.1 OOFDM-WDM PONs

The simplest way to implement a PON based on OOFDM is to employ WDM and allocate each ONU separate dedicated optical wavelengths for upstream and downstream traffic, as in a traditional WDM-PON. Fig. 2.17 illustrates a OOFDM-WDM PON, here the connection between the feeder fiber and the distribution fibers is provided by a arrayed wave guide (AWG) which multiplexes (demultiplexes) different wavelength in the downstream (upstream) direction. At the central office an AWG is required to multiplex/demultiplex the ONU signals and an OOFDM transceiver is required per ONU. This PON architecture can therefore be considered as multiple point-to-point OOFDM links.
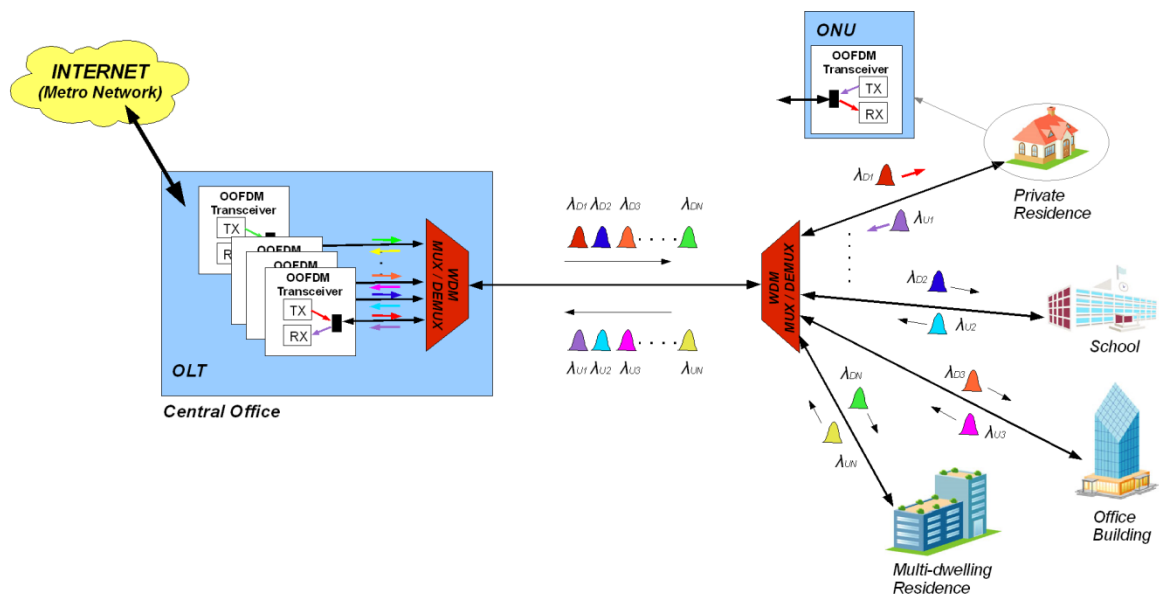
Fig. 2.17 OOFDM-WDM-based PON Architecture

The OOFDM-WDM PON also suffers from the characteristic limited flexibility of any WDM PON, in that each ONU has a fixed and dedicated maximum transmission capacity and it is not possible to implement DBA to dynamically share total PON bandwidth amongst the ONUs.

As each ONU on the OOFDM-WDM PON must operate at a different transmit wavelength this can be achieved by installing a different wavelength laser in each ONU. This is however not desirable from the perspective of manufacturing logistics and network management. Preferably all ONUs are identical and can be configured in the field (locally or remotely) for any ITU-grid wavelength within a selected operating band. An effectively

"colourless" ONU is therefore highly advantageous if it can be implemented in a cost effective manner. Colourless ONUs can be implemented with tuneable lasers and external modulators [31] or a seed laser source in the CO [32] can be transmitted downstream for modulation by an external modulator in the ONU before retransmission in the upstream direction. The transmission of OOFDM signals with cost-effective modulators that can operate over a wide wavelength range is therefore highly significant. To explore colourless OOFDM transmission chapter 6 presents the experimental demonstration of colourless real-time OOFDM transmission based on a reflective semiconductor optical amplifier (RSOA).

2.5.2 OOFDM Multiple Access PONs (OOFDMA-PONs)

An OOFDM multiple access (OOFDMA) PON [33] is a hybrid technique where bandwidth is partitioned using both time domain multiplexing (TDM) and frequency domain multiplexing (FDM). The symbol based nature of OOFDM allows bandwidth to be readily divided into timeslots for TDM and the multi-carrier characteristic offers the ability to divide bandwidth into subcarriers for FDM. It is also possible to apply a third DBA dimension by independently varying subcarrier signal modulation formats and powers to perform DBA with an extremely fine granularity [27]. This allows the total PON bandwidth to be dynamically distributed among the ONUs to meet the time varying service demands of different users.

Fig. 2.18 illustrates the basic OOFDMA PON architecture and an example OOFDMA frame structure. In the downstream direction the OOFDM signal is split by a passive splitter and the same signal is thus transmitted to all ONUs. Each ONU is pre-allocated timeslots and subcarriers and therefore only extracts the appropriate data. Data encryption is of course necessary to prevent ONUs being able to access other users' data. In the upstream direction each ONU only transmits on its allocated timeslots and subcarriers, the signals then combine at a passive coupler between the distribution fibers and feeder fiber. The OLT thus only employs a single OOFDM transceiver to support all ONUs.

In comparison with the traditional PONs mentioned above, OOFDMA PONs have demonstrated a number of salient advantages capable of satisfying the network operators' requirements for future high-speed PONs. The advantages are summarised below:

- Capable of supporting an increased number of subscribers with high signal bit rates over extended reach [34];

- Considerably improved cost-effectiveness. This is because of the full exploitation of the rapid advances in modern DSP technology, and the considerable reduction in PON system complexity owing to OOFDM's unique adaptability, excellent resistance to linear component/system impairments and efficient utilization of channel spectral characteristics [27,33-35];

- Full-scale DSP-based adaptive DBA with a fine bandwidth granularity. As mentioned above, the available channel bandwidth is shared statistically between various ONUs using dimensions of frequency, time and signal modulation format.

- Backward compatibility. The TDM aspect means OOFDMA PONs can potentially be overlaid onto existing TDM based PONs, such as (10)GPON and (10)EPON, by allocating set timeslots to the different TDM PON standards. This coexistence with different standards offers a seamless upgrading of installed legacy PONs [36];

- Excellent flexibility. OOFDM transceivers with adaptive bit and/or power loading [27] offer the PON systems great adaptability. This feature may not only facilitate the convergence of various access networks but also enable the accommodation of traditional heterogeneous services and newly emerging services over a common platform.

For upstream OOFDMA transmission synchronisation is highly critical. ONUs must be timeslot synchronised so that symbols are aligned at the OLT, one timeslot consisting of one or more symbols, and ONUs must be synchronously clocked so that both symbol alignment is maintained and subcarriers from different ONUs maintain orthogonality. There are no existing solutions for OOFDMA-PON synchronisation and no solutions have been proposed in the research literature. This thesis work proposes and demonstrates techniques for synchronous receiver clocking (chapter 7) and symbol/timeslot synchronisation (chapter 8) which can applied to OOFDMA-PONs to achieve an effective synchronisation scheme with many advantages, such as ONU synchronisation in a live PON.
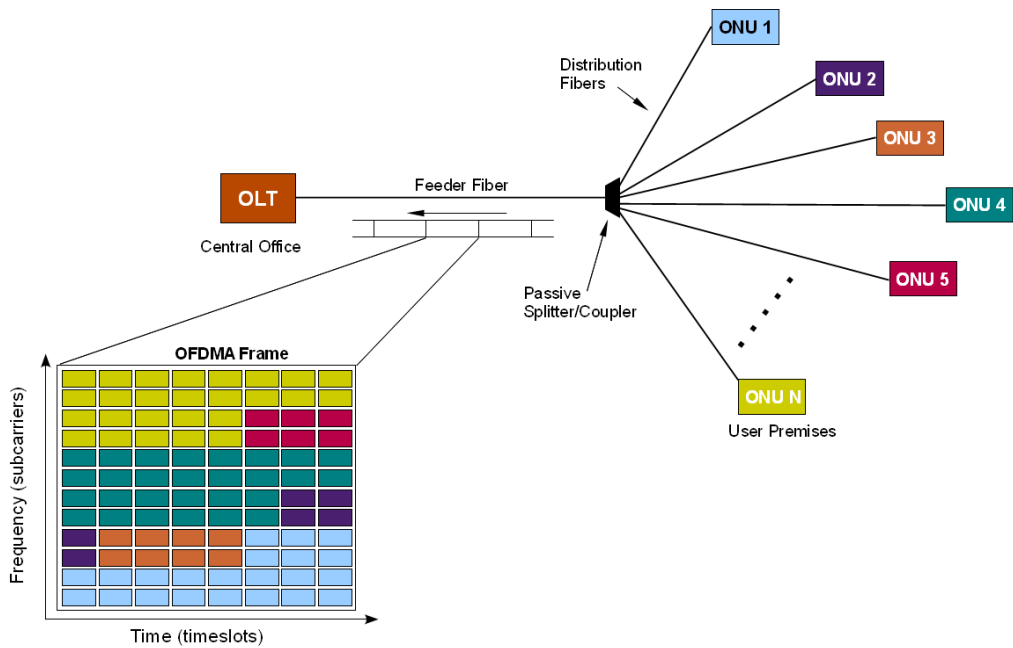
Fig. 2.18 OOFDMA based PON Architecture

2.5.3 Hybrid OOFDMA-WDM PONs

It is also possible to implement hybrid OOFDMA-WDM PONs where multiple OOFDMA PONs are overlaid on the same PON by employing different wavelengths. Fig. 2.19 illustrates an example of the downstream link in a OOFDMA-WDM PON, the upstream link would employ a similar architecture. This type of PON has the advantage that one wavelength can provide a dedicated high bandwidth link to business customers for example, whereas other wavelengths can be split using OOFDMA to provide services to multiple premises such as residential customers.
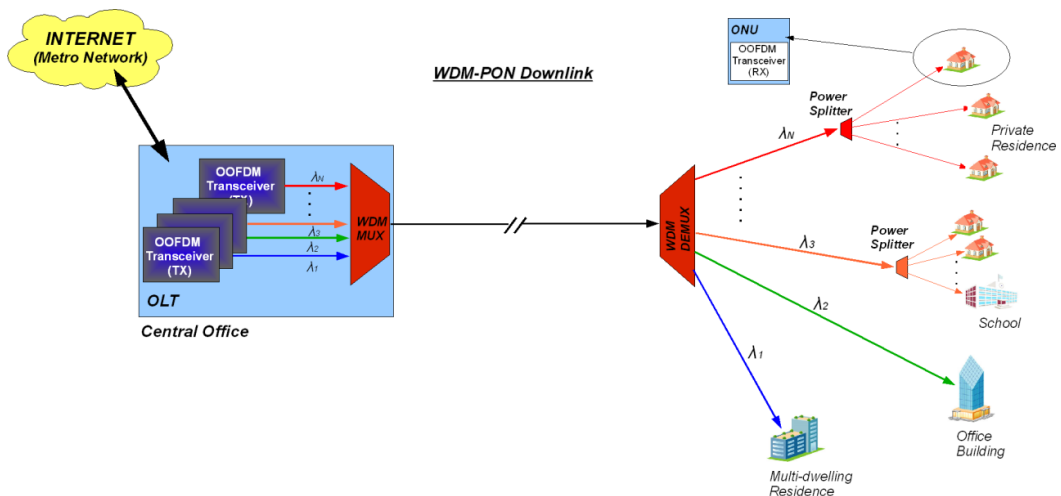
Fig. 2.19 Example Hybrid OOFDMA-WDM PON Architecture (Downstream)

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3 Real-time OOFDM Transceiver Design

Contents

3.1 Introduction

The fundamental objective of this research is to design and implement a completely real-time OOFDM transmission system, working at a target speed of at least 10Gb/s, for data transmission applications employing IMDD systems with either MMF or SMF fibers. This is of course a critical and essential step towards demonstrating the ability of OOFDM to meet the requirements of future access and in-building optical networks as explicitly defined in chapter one. This chapter provides a comprehensive description of the real-time OOFDM transceiver design and implementation. As this type of advanced optical transmission had never before been experimentally demonstrated in real-time there were a number of obvious challenges and unknown aspects clearly apparent from the outset that this research would also aim to answer. These aspects are discussed below:

Processing Power

The key underlying challenge associated with the high-speed OOFDM transceiver and its exceptionally high data rates is the high level digital processing power that would be required, so far unseen in any existing OOFDM system. Compared to the off-line approach the hardware implemented DSP algorithms are limited in speed and precision. The challenge is therefore to implement algorithms that operate with sufficient speed and accuracy without excessive logic resource usage. The research will therefore explore the ability of modern semiconductor electronics to meet the signal processing demands of OOFDM.

Ultra-High Sampling Rates

Further implementation challenges arise from the multi-GS/s sampling rates involved. The availability of high-speed DACs and ADCs had been quite limited thus restricting the component choice significantly, however more recently there has been steady growth in the availability and performance of DAC/ADCs and the technological advances are predicted to continue, OOFDM perhaps being one application which drives their development.

Digital Signal Integrity

The high sampling rates required also present technical challenges associated with maintaining signal integrity in ultra-high speed digital interfaces. The enormous

interconnect bandwidth between ADC/DAC and DSP at potential OOFDM sample rates and resolutions [1] can easily exceed 100Gb/s, commercial DAC/ADCs are now available having interface bandwidths approaching 200Gb/s [2,3], implementing these interfaces becomes a real design issue and can only be solved by advanced interconnect techniques, especially for inter-chip interfaces.

Linear Wideband RF Components

The need for linear components comes from the fact that OOFDM employs analogue signal transmission and so any component non-linearity will induce unwanted signal distortions. As RF components will exhibit some degree of non-linearity an insight into the suitability of commercial RF components for OOFDM transceivers will be obtained. Also the wideband, baseband signals involved make it challenging to find suitable RF components with constant characteristics over the entire signal band.

Linear Wideband Optical Components for IMDD

Due to the cost-sensitive applications being targeted the use of directly modulated lasers (DMLs) in the OOFDM transmitter will be evaluated. Non-linear effects associated with the direct modulation of a semiconductor laser, such as frequency chirp, result in the mapping between the OFDM signal and the optical carrier intensity not being completely linear. The ability of the OOFDM signal to tolerate the DML-induced signal distortions is a key aspect of the IMDD-based system that this research will explore. Furthermore the effect of the DML's modulation bandwidth on system performance is also a key aspect for investigation as this has a large impact on DML cost. The OOFDM receiver will be based on a square-law photo-detector for the benefit of the associated low cost. Again there are non-linear effects associated with the square–law photo-detection such as the intermodulation products created by subcarrier intermixing, which distort the received OFDM signal. Finally, there will be thermal and shot noise associated with any optical receiver which also degrades the received signal quality. The ability of the OOFDM signal to tolerate the distortions associated with the direct-detection photo-detector will also be revealed.

The initial design task was to identify the core system components required in the OOFDM transceiver and optical link and identify the critical specifications. Suitable commercially available components were then thoroughly investigated. So called "off-the-shelf"

components are utilised as it was not desirable to construct custom-built components as this would obviously be a time consuming task but more importantly that the commercial feasibility of the OOFDM technology can be demonstrated much more effectively if it can be shown that only established technologies and readily available components are needed to realise working OOFDM transceivers. Also component evaluation boards would ideally be used as building custom circuit boards would be a immensely time consuming task and of no real benefit in terms of the research goals. A modular approach was also adopted where possible such that components could be easily substituted to allow the evaluation of alternatives. Therefore as with any initial prototype, producing an integrated and compact solution was not a requirement. Once possible candidates were identified for the core system components the possible top level system architectures were studied in terms of how to interface the various components. The careful selection of components could drastically reduce the complexity of the digital interconnects which was an extremely significant factor considering the fact that high speed buses carrying several 10s of Gb/s were required.

The only practical method for implementing the high-speed DSP in a prototyping environment is with field programmable gate arrays (FPGAs) as they are unparalleled in their ability to provide a platform for rapidly evaluating, testing and optimising DSP algorithms. Modern state-of-the-art FPGAs can offer extremely high performance in terms of speed and logic resources however it was necessary to estimate the system logic requirements to give some level of assurance that the selected FPGA would deliver the needed performance. For the DSP implementation the strategy employed was to build the system in stages so that DSP functionality is minimised as much as possible in the initial designs, functionality and therefore complexity was then gradually increased with progressive design enhancements. Also it was considered necessary to implement all DSP functions from scratch as oppose to employing third party IP cores. This was considered particularly important for the IFFT/FFT algorithms, so that full control was maintained to achieve a high level of flexibility in the design. Employing third party IP cores could severely limit the controllability of critical system parameters. The design environment used for the DSP provided a design flow where DSP functions and subsystems could be modelled and simulated and then directly compiled into a suitable format for FPGA programming. This approach allows alternative designs to be rapidly compared and evaluated and functionality thoroughly tested. The DSP design environment is fully

described in section 3.5.1. One important consideration when selecting the FPGA platform was the facilities available for design debugging and signal monitoring as this can have a significant impact on development and testing time. Another important consideration at the design stage is the system test strategy to be employed as a reliable method is needed to thoroughly evaluate the performance of the OOFDM transceiver. The design of the OOFDM transceiver was found to require multi-disciplinary expertise as it covers the fields of RF design, FPGA logic design, DSP algorithm/function design, optical communications engineering, system design and test engineering.

3.2 Basic OOFDM Transceiver and System Structure

Fig. 3.1 (a) shows the basic structure of the OOFDM transceiver in terms of the key functional elements. Fig. 3.1 (b) depicts a bidirectional point-to-point transmission link based on the OOFDM transceivers employing dual fibers. There are however cases where the upstream and downstream links are different such as when employing OLT-located seed lasers feeding colourless ONUs [4] or bidirectional wavelength reuse employing a single fiber [5]. However these are advanced techniques aimed at further improving network features and cost and are not appropriate for initial experimentation. Each transceiver element can be a stand-alone component or multiple elements can be integrated into single components. As the focus of the research is not to explore the possibilities of component integration, individual components as depicted in Fig. 3.1(a) will be employed. Here separate DSP hardware components are shown for transmitter and receiver functions however a single digital device combining both functions is also suitable.
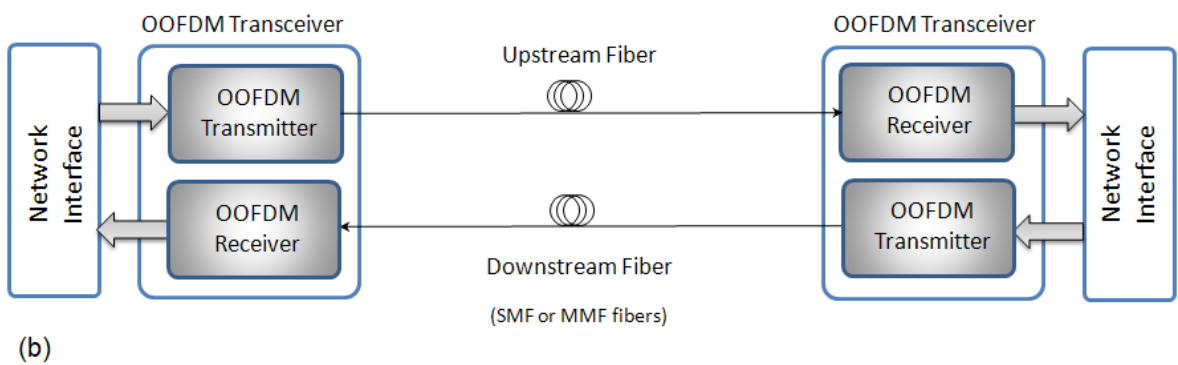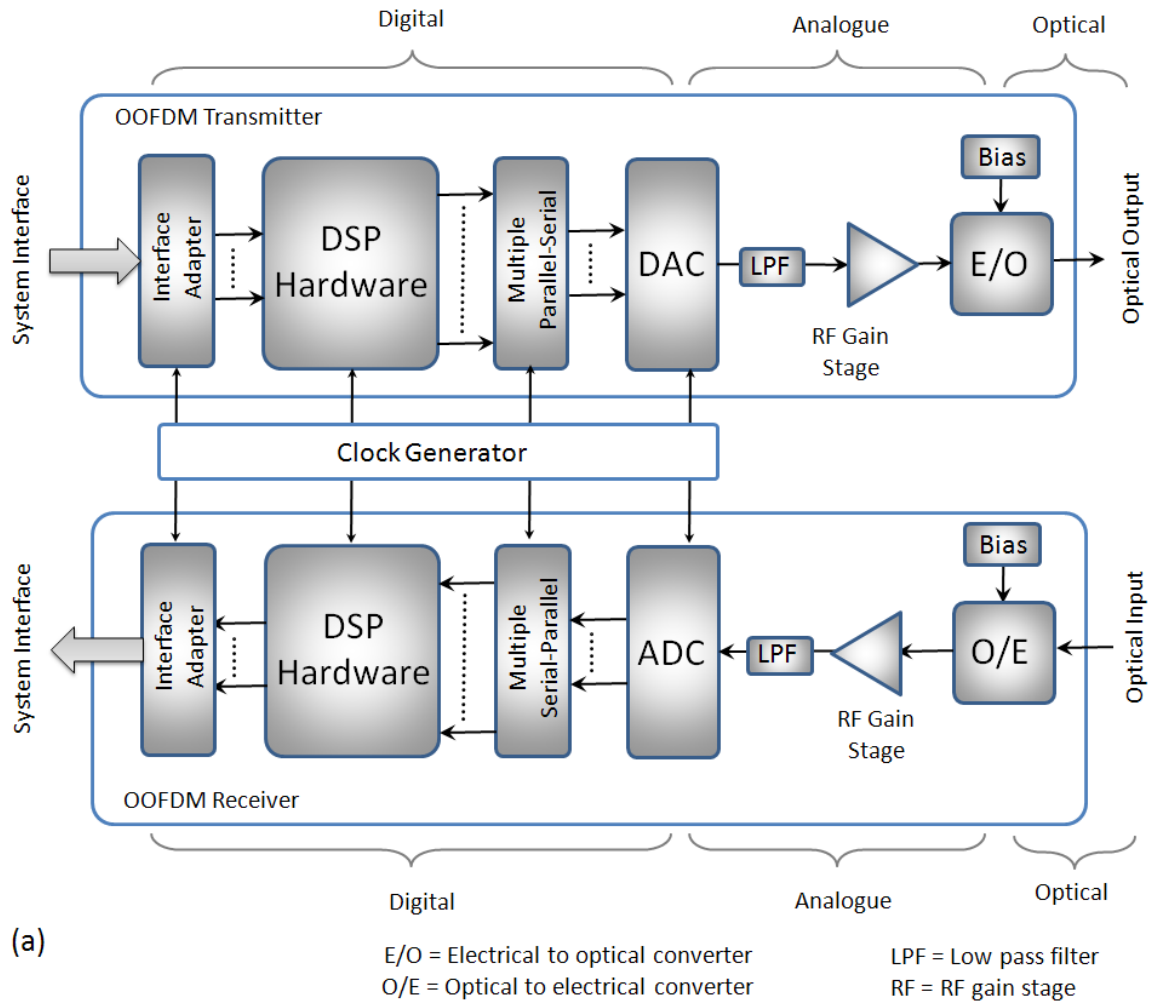
Fig. 3.1 a) Basic OOFDM transceiver structure, b) Basic point-to-point bidirectional OOFDM system

The functionality to be demonstrated is real-time, end-to-end data transmission based on OOFDM modulation, the objective is not to achieve data transmission in a fully functional

network supporting real service delivery as this would be extremely ambitious and is clearly not necessary for the analysis of the OOFDM transmission performance. The OOFDM transceivers are therefore designed to implement the physical layer only and the primary measurement of signal transmission quality will be the total system bit error rate (BER). Today's data transmission networks require virtually error free transmission, this means BERs of the order of $1x10^{-12}$ are required, however to relax physical system requirements and improve receiver sensitivity the raw BER is much higher and forward-error-correction (FEC) is employed to improve the effective BER by the use of redundant bits for error correction. To allow the use of FEC coding the minimum raw BER should ideally be $\leq 1x10^{-3}$ however FEC codes can handle BERs as high as $2.3x10^{-3}$ or even $4x10^{-3}$ [6]. FEC can be implemented at the physical level or at the MAC layer. This research will not implement FEC and will use the generally accepted FEC limits to evaluate the system performance.

The OOFDM transmitter consists of the following key components:

Interface Adaptor:

The interface adaptor is required to interface between the higher system layers which generate the raw data for transmission. Typically in network equipment this is the Medium Access Control (MAC) layer. As building a system with a full communication stack is not the aim of the present research a simple interface is needed that allows connection to a bit pattern generator (BPG). The interface must support in excess of 10Gb/s as this is the target data rate of the system.

DSP Hardware:

The DSP hardware is the logic circuitry performing all necessary algorithms and functions to generate a digital OOFDM signal. DSP can be performed by microprocessors specifically designed for executing software based DSP algorithms, however the processing speed of these devices cannot meet the processing power demanded by high-speed OOFDM therefore hardware based DSP is the only practical solution. For implementing complex digital circuitry there are two fundamental solutions: programmable logic devices or custom logic devices. There are several types of programmable logic devices available, for large complex designs the FPGA is the dominating device. An FPGA has the feature of in-circuit reconfigurability making it

unsurpassed as a prototyping solution for developing complex logic designs. Custom devices consist of hardwired logic circuits which have been design for specific dedicated applications, so called application specific integrated circuits (ASICs), or for more general functions, the so called application specific standard product (ASSP). Here the term ASIC will refer to any type of custom logic IC. ASICs are superior to FPGAs in terms of cost and power consumption however they also require significant investment for the development cost. ASICs are therefore are only justified in the case of mass produced equipment. FPGAs are the obvious choice therefore for the DSP hardware implementation as, apart from the much lower cost, they provide the only realistic solution for system prototyping, where an incremental design process with DSP algorithm experimentation and optimisation are essential.

Parallel -to- Serial Interface (DSP to DAC):

The DSP logic circuitry operates at a lower speed than the DAC. The logic circuitry will generally be clocked at a few 100MHz whereas the DAC will be clocked at a few GHz. As a constant sample rate is maintained from the DSP logic output to the DAC input and as each interface operates at different speeds the number of data bits must therefore be different on each side of the interface, the interface circuitry must function as multiple parallel-to-serial converters adapting the rate and bit width of the interconnecting bus.

Digital-to-Analogue Converter:

The DAC is a critical component in the OOFDM transmitter, it is responsible for converting the digitally generated discrete samples from the DSP logic to a continuous analogue electrical signal which can be used to modulate the optical modulator. The characteristics of the DAC can have a significant impact on the OOFDM system performance. The sample rate and the bit resolution are the fundamental parameters which directly influence achievable line rates and the BER performance. The relationship between sample rate and signal bandwidth, governed by Nyquist's sampling theorem, indicates that increased capacity can be achieved by increasing sample rate to utilise more of the available fiber bandwidth. The sample rate of the DAC, S_{DAC}, determines the maximum electrical bandwidth, B_e, and therefore optical signal bandwidth, B_o, of the OOFDM signal according to Nyquist's sampling theorem, i.e. $2 \cdot B_e < S_{DAC}$. However, the frequency response of the DAC is typically not flat up to its Nyquist rate and tends to roll-off with frequency. This low-pass response is due to two effects: firstly the inherent on-

chip filtering due to parasitic impedances at the silicon and package level. Secondly DACs commonly employ a zero-order hold output which means the sample level is held constant between samples instants. This introduces a multiplication of the output signal by the $sin(x)/x$ function in the frequency domain, thus causing a roll-off in amplitude with frequency. The bit resolution has a significant impact on performance as this determines the level of signal quantisation, theoretical work [7] has shown that there is an optimum bit resolution depending on the various system parameters employed, such as modulation format, transmission distance and clipping ratio. For the purpose of this real-time demonstration the selected bit resolution will preferably be above the theoretical optimum as it is always possible to reduce the effective resolution by fixing one or more least significant bits (LSBs) to 0. The selected DAC resolution also has an impact on the associated transmitter DSP logic functions as a higher bit resolution translates to higher precision DSP functions. There are a number of parameters which characterise a DAC's performance in terms of the signal distortion compared to an ideal DAC, a full analysis of the various DAC parameters' affect on OFDM performance is beyond the scope of this research. The digital interface of the DAC is also an important consideration because, as discussed in section 3.1, this will affect the complexity of the interface to the FPGA.

Low Pass Filter:

It is common practice to place a low pass filter at the output of the DAC, this removes the sampling images associated with any sampled signal so that ideally only the baseband signal remains. Practical filters cannot operate as ideal "brick-wall" filters so sampling images cannot be totally eliminated. The order and characteristics of the filter will therefore affect the quality of the filtering and so are important factors to consider. Ideally the filter should have a flat pass-band response, however as the OFDM signal consists of multiple narrow band signals, the variation seen by each individual subcarrier can be considered flat, any amplitude or phase variation across subcarriers introduced by the low pass filter will contribute to the total channel response and will be compensated as part of the channel equalisation. The ability of the filter to block out of band signals close to the cut-off frequency will depend on the order of the filter, the higher the order of the filter the better its blocking perform. To relax the requirements of the filter the DAC can employ oversampling such that the Nyquist frequency is higher than the signal bandwidth, this inserts a guard band between the baseband signal and the image signal thus making the filtering out of the image signal easier. It should be noted that the level of oversampling

employed with an OFDM signal can be easily controlled simply by setting one or more adjacent high frequency subcarriers to zero power, increasing the number of zero power subcarriers effectively increases the oversampling and thus the guard band to the image signal. Increasing the oversampling at a fixed sample rate is of course a trade-off between signal bandwidth and any resulting performance gain or reduction in low pass filter specification. Some parameters of the filter can lead to distortions in the OFDM signal such as impedance mismatches, therefore, for example, a high return loss is desirable across the whole signal spectrum. The influence of the various low pass filter parameters on OOFDM transceiver performance can be worth investigating however it is not the intension to perform a detail study as part of this research work.

RF Gain Stage:

An RF gain stage is required to linearly amplify (or attenuate) the analogue signal from the DAC to an appropriate level to drive the optical modulator. The characteristics of the RF gain stage will impact transceiver performance, therefore knowledge of how the various RF parameters affect performance is an important issue as the parameters can be controlled to tune the balance between performance, power consumption and cost. For the real-time transceiver design, off-the-shelf components will be used however optimisation of the transceiver's RF electronics would be an important area to explore although a detailed analysis is also beyond the scope of this research.

Optical Modulator and Bias:

The optical modulator ideally performs a linear conversion of the analogue electrical signal to an optical signal, this is more generally known as an electrical-to-optical (E/O) converter. As the target is to minimise system cost intensity modulators are to be used. Both directly modulated lasers and external modulators with a CW laser source can be employed for intensity modulation. An appropriate bias circuit is also required and it is essential that the bias conditions can be adjusted to allow for optimisation. If the optical modulator is cooled then the necessary temperature control circuitry must also be implemented. The optical modulator must generate light at a suitable wavelength for transmission in the selected fiber type, this is generally in the region of 1300nm and 1550nm. Ideally the optical modulators output power is sufficient, however if necessary an optical amplifier can be employed to boost and adjust the transmitted optical power.

The OOFDM receiver consists of the following key components:

Optical Detector and Bias:

The optical detector ideally linearly converts the received optical signal to an analogue electrical signal, this is also more generally known as an optical-to-electrical (O/E) converter. As intensity modulation is employed at the transmitter the photo-detector must generate an electrical signal proportional to the intensity of the detected light. The optical detector will generally consist of a photodiode which generates a photocurrent proportional to the square of the optical field, a so called square-law detector, combined with a trans-impedance amplifier (TIA) which amplifies and converts the photocurrent to a voltage. The photodiode should also ideally be low noise as thermal and shot noise will degrade signal-to-noise ratio (SNR) at the receiver.

RF Gain Stage:

An RF gain stage is required to linearly amplify the analogue signal from the photo detector to a suitable level for the ADC. To minimise quantisation noise the full-scale input range of the ADC should be used however if the analogue signal amplitude exceeds the full-scale range then signal clipping will occur. The RF gain must therefore be adjustable to allow the optimum analogue signal amplitude to be obtained as received optical signal power varies. In a practical system automatic gain control (AGC) must be employed however manual gain control is implemented in the experimental system.

Low Pass Filter:

A low pass filter is placed before the ADC to act as an anti-aliasing filter, this ensures that signals at frequencies above the Nyquist frequency are sufficiently attenuated such that they do not generate components in the digitally sampled baseband signal due to under-sampling. As with the low pass filter in the transmitter, the order and characteristics can affect the quality of the digitised signal and therefore the system performance. The closer the filter performance is to the ideal "brick wall" filter the better the system performance, however the required filter quality will depend on the spectral characteristics of the out-of-band signals present. An optical link with a single OOFDM baseband signal however has a unique feature which distinguishes it from other common communications systems. Typically the communication channel is divided into separate closely spaced frequency bands each carrying independent data, here strict filter requirements are essential to

sufficiently attenuate out-of-band signals and prevent them aliasing into the wanted band upon receiver sampling. For OOFDM baseband transmission only, there are no additional signal bands which must be blocked from reaching the receiver's ADC. Multiband OOFDM is of course possible and this case will increase the demand on out-of-band blocking of the low pass filter. For the case of a single baseband OOFDM signal there are three distinct sources of out-of-band signals i) noise generated by components such as the optical detector and active analogue components, ii) intermodulation products caused by component nonlinearities and iii) residual image signals generated by the DAC in the transmitter which are not totally eliminated by the low pass filter at the DAC output. The first two sources of out-of-band signals can interfere with the baseband signal due to aliasing, however the residual image signals are not necessarily problematic as they are generated by the data signal itself and so the image signal contains useful data which can be safely aliased back in to the baseband signal, any distortion of the image signals can of course degrade the baseband signal. Also, as for the low pass filter in the transmitter, the gain and phase response of the anti-aliasing filter will contribute to the total channel response which can also be compensated by the channel equalisation.

Analogue-to-Digital Converter:

The ADC converts the filtered analogue electrical signal from the RF gain stage to digital samples for subsequent processing by the DSP logic. The minimum required sample rate of the ADC, S_{ADC}, is determined by the electrical bandwidth of the OOFDM signal, B_e, according to Nyquist's sampling theorem, i.e. $S_{ADC} > 2 \cdot B_e$. A sample rate in excess of $2 \cdot B_e$ can be employed to provide oversampling which can aid in the removal of out-of-band signals through post-processing in the DSP. The digital interface is again an important consideration as this affects the complexity of the FPGA interface. Another highly desirable feature of an ADC is the generation of digital test patterns, this will aid validation of the ADC-to-FPGA interface as the FPGA can be configured to examine and check for errors in the test pattern.

The DC level of the signal at the ADC input must be set appropriately as ADCs typically operate with positive input voltages only. If the optical detector output, RF gain stage and low pass filter are DC coupled there can be a residual DC level present due to the DC bias of the received optical signal, this can be eliminated by a simple DC block. If the ADC does not incorporate a suitable DC biasing circuit then a DC level corresponding to half the

full-scale input voltage must be added to the received electrical OFDM signal. The DC offset can then be removed within the DSP logic to restore the signed sample format.

Serial -to-Parallel Interface (ADC to DSP):

The interface between the ADC and the DSP logic essentially operates in the opposite manner to the DSP to DAC interface. For this case the high speed digital signal from the ADC must be converted to a lower speed bus with increased bit width to maintain the sample rate, thus operating as multiple serial-to-parallel converters.

DSP Hardware:

The DSP hardware in the receiver performs all necessary algorithms to reconstruct the transmitted data from the received signal. As for the transmitter DSP the only practical solution for prototype implementation is the FPGA. A single FPGA can be employed for both transmitter and receiver functions or separate FPGAs can be used to provide increased logic resources and interfacing capability.

Interface Adaptor:

The interface adaptor in the receiver performs the same function as the interface adaptor in the transmitter however data flow is now from the physical layer to the higher system layer. For the initial experimentation the interface must allow connection to a bit error analyser so that BER measurements can be performed. The interface must operate in excess of 10Gb/s to comply with the target data rate of the system.

Common to both the transmitter and receiver elements of the OOFDM transceiver is the clock generation and distribution circuitry, all digital elements (FPGAs, DAC and ADC) requiring clock signals. Each element may require a different frequency clock however all clocks must be synchronised to a common reference clock to maintain synchronisation between components. High frequency clocks will be required, the FPGA will typically require a clock of the order of 100's of MHz and the DAC/ADC will typically require clocks of the order of a few GHz. The clock generator should be based on frequency synthesisers and/or programmable dividers so that clock frequencies can be adjustable to give flexibility in system clocking. At the clock frequencies used clock delay and skew can be significant factors and so adjustable clock delay is also preferable to allow further control of system clocking. It should be noted at this point that in a data transmission network a master clock source will be located at one end of the link and the receiver at the

opposite end of the link should either perform clock recovery on the received signal to generate a synchronous clock, or use a free-running asynchronous clock and compensate for the clock offset. For initial experimentation of real-time OOFDM transmission however, the only practical solution is to use a common clock for both the transmitter and receiver to ensure synchronisation.

Important system elements not depicted in Fig 3.1(a) are the power supplies for all components. The power supplies must be carefully implemented to minimise electrical noise coupling into the system, this can be from ripple or switching noise of each individual supply or from cross-talk from common source and/or ground impedances. It is also important to follow good design practises to minimise all possible noise sources both conducted and radiated, this can be especially challenging when high frequency digital signals are mixed with sensitive analogue signals. The approach used for the real-time transceiver is to use high quality bench power supplies with dedicated supplies used for each component supply voltage where possible.
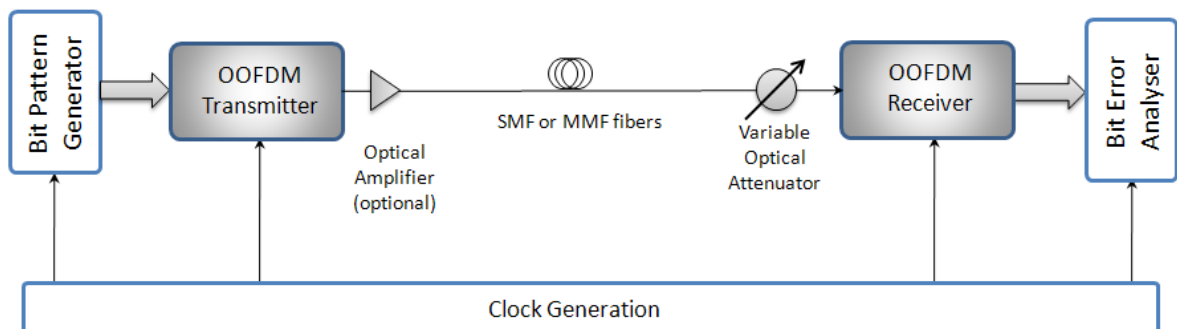
Fig. 3.2 Basic OOFDM transmission link implementation

The real-time OOFDM system setup for proof-of-concept experimentation is shown in Fig. 3.2, only a unidirectional link is necessary as the case is considered where upstream and downstream directions are identical. An optional optical amplifier is used at the transmitter to boost the transmitted optical power if needed or to allow accurate control of the transmit power level. The optical link consist of a single length of MMF or SMF fiber without inline amplification or using dispersion compensating fiber (DCF). A variable optical attenuator (VOA) is employed at the receiver to allow measurement of BER performance at varying levels of received optical power. For experimentation with MMF it was found neccesary to locate the VOA at the transmitter and use a mode-conditioning

patch cord to ensure correct interconnect between SMF and MMF based equipment and fibers.

3.3 Selected Components and Fixed System Parameters

The FPGA, DAC and ADC are the key transceiver components which were first selected concurrently so that the implementation of the high speed digital interfaces could be considered. The selected FPGA is the Stratix II GX from Altera, this was chosen as it was one of the largest devices available at the time in terms of equivalent logic elements, it offers suitable interfacing capability in terms of speed and total bandwidth and furthermore a key advantage is its availability as a development board (PCI-Express) with sufficient connectorised interfaces. As the total required logic resources were difficult to estimate a large FPGA was selected for prototyping purposes to ensure sufficient logic resources would be available and so that logic optimisation was not a necessity during the proof of concept implementation phase. A commercially available IP Core of an IFF/FFT was studied to gain an approximation of the required logic resources from which it was estimated that the Stratix II GX would be suitable.

When investigating the state-of-the-art in multi-GS/s DAC and ADC technology it was discovered that 8 bit converters with sample rates of the order of 10GS/s where common in ultra-fast sampling test equipment applications such as ADCs in wideband real-time digital sampling oscilloscopes (DSOs) and DACs in arbitrary waveform generators (AWGs). The ~10GS/s converters were however all proprietary technology implemented by the test equipment vendor and not commercially available as individual components. The DAC and ADC were therefore selected from the commercially available devices which were extremely limited and all with ≤5GS/s performance. A critical parameter of the converters is the number of quantisation bits or bit resolution. The minimum required resolution of the DAC and ADC is based on the fact that that for a given signal-modulation format, there exists a minimum quantisation-bit value, beyond which a region of quantisation-independent SNR is observed [7]. It has been shown theoretically [7] that for modulation formats as high as 128-QAM the minimum resolution required is at least 7 bits.

Table 3.1 *Selected System Components*

Component	Type	Key Parameters
FPGA	Altera: Stratix II GX EP2SGX90FF1508C3	– 36,384 Adaptive Logic Modules (90,960 Equivalent Logic Elements) – 16× 6.375Gb/s Duplex serial transceivers – High speed I/O up to 1040 Mb/s – Total RAM: ~4.3Mbits – 192 Embedded multipliers (18x18) – 48× Dedicated DSP blocks – 8× PLLs
DAC	Maxim: MAX5881	– Resolution: 12-bit – Sample rate: 4.3GS/s – Output voltage: 660mVpp – 4×8-bit LVDS ports
ADC	E2V: EV8AQ160	– Resolution: 8-bit – Sample rate: 5 GS/s – Output voltage: 600mVpp – 4×8-bit LVDS ports
E/O Converter	NEC: DFB Laser NLK5C5EBKA	– Modulation bandwidth: 10 GHz – Peak wavelength: 1530-1565 nm – Max output power: 3-4mW – Threshold current: 15-30mA – Linewidth: 0.4-0.5nm
O/E Converter	New Focus: Photoreceiver +TIA 1544-A-50	– 3dB Bandwidth: 12 GHz – Wavelength range: 950-1650 nm – Sensitivity: -17dBm [a] – Max input power: 0 dBm
Clock Source	Centallax: TG1C1A Clock Synthesiser	– Frequency Range: 0.5 – 13.5 GHz – Accuracy: ±3.0 ppm – 6 differential output channels – Sub-rate trigger output: (Clock/N)
Transmit RF Amp	Minicircuits: ZHL-1042J	25dB, 10MHz-4.2GHz
Receiver RF Amp	Miteq: AM-1616-2500	20dB, 0.01MHz -2.5GHz
Low-Pass Filter	Minicircuits: SLP-2400+	3dB bandwidth: 2.4GHz

[a] Corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}

Table 3.1 Cont' *Selected System Components*

Component	Type	Key Parameters
1:4 Demux	Inphi: 5081DX	Max data rate: 50Gb/s
4:1 Mux	Inphi: 5080MX	Max data rate: 50Gb/s
Balun	MACOM: H-183-4	Frequency range: 30MHz – 3GHz

Therefore as a typical converter resolution is 8-bits and as the effective number of bits (ENOB) is typically slightly less than the number of quantisation bits, 8-bit resolution is selected to be the minimum requirement. The selected DAC is a 12-bit 4.3GS/s device and the ADC is an 8-bit 5GS/s device as listed in table 3.1. The DAC is operated as an 8-bit device by fixing the lower 4 LSBs to zero. These converters were also selected as they can be directly interfaced to the Stratix II GX FPGAs I/O when configured for the low voltage differential signalling (LVDS) logic standard, without the need for any interfacing components. Again development boards for both devices were utilised to simplify system construction. Both the DAC and ADC development boards can be configured for 4x 8-bit LVDS ports which are compatible with the high speed mezzanine connector (HSMC) interface on the Stratix II GX PCI Express development board. The HSMC provides interconnection to 32x LVDS I/O on the Stratix II GX. The LVDS I/O can be clocked at a maximum of 1GHz, thus each I/O operates at up to 1Gb/s providing a total interface speed of 32 Gb/s or 4GS/s at 8-bits per sample. Therefore although the DAC and ADC can operate at slightly above 4GS/s the sample rate is limited by the interface speed. Separate adapter boards were developed that connect to the DAC and ADC and allow connection to the HSMC interface on the FPGA boards via two 50Ω micro-coax ribbon cables. The adapter boards where designed with 100Ω differential characteristic impedance on each differential signal connection to match the LVDS I/O and cable impedances. All signal traces were also carefully designed to achieve the same physical length to ensure differential signal delay is significantly below the 1ns bit period.

As the FPGA logic operates at a lower clock rate (50 or 100MHz) than the 1GHz interface clock, the DAC and ADC interfaces employ P/S and S/P converters which are provided as dedicated hardware functions within the FPGAs. The functional blocks depicted in Fig. 3.1 (a) as multiple P/S and multiple S/P are therefore provided as dedicated hardware functions within the Stratix II GX FPGA which greatly simplifies the external FPGA to DAC/ADC

interconnection. Full descriptions of the DAC and ADC interfaces are given in sections 3.5.3.6 and 3.5.4.1.

To provide the external system data interfaces for connection to a bit pattern generator (BPG) and a BER analyser (BEA), the FPGA's high speed Gigabit transceivers (GTRX) are utilised. The bit pattern generator (SHF BPG44) and the BER analyser (SHF EA44) utilised have serial interfaces therefore a suitable digital multiplexer and demultiplexer are necessary as the GTRXs have a maximum speed of 6.375Gb/s. The selected devices are a 4:1 digital multiplexer and 1:4 digital demultiplexer as listed in table 3.1. For operation at a total bit rate of 10 Gb/s for example each transceiver is operated at 2.5Gb/s. The GTRX interfaces are available at a PCI edge connector on the Stratix II GX development board, therefore an adapter board was also developed to adapt from the PCI edge connector into twin SMA connectors for each differential transceiver connection. A single adapter board was designed to provide access to four GTRX inputs, four GTRX outputs and also a clock input for GTRX clocking if required.

The initial implementation of the transmitter's analogue front end consisted of only a variable electrical attenuator to provide signal level adjustment. Also as the DAC provides low-pass filtering of the generated analogue signal no additional filtering component was required. For subsequent designs where a higher analogue signal level was required a 25dB RF amplifier as specified in table 3.1 was employed.

For the receiver's analogue front end a broadband 20dB RF amplifier, as specified in table 3.1, is utilised in conjunction with fixed and variable attenuators to provide manual adjustment of the total electrical signal gain. The selected low-pass filter provides a 3dB bandwidth of 2.4GHz. The RF amplifier is AC coupled so any DC level present at the PIN detector output is removed. The ADC development board generates a suitable DC input voltage at half full-scale to correctly bias the ADC input. The selected ADC has a differential input therefore a balun as specified in table 3.1 is used to convert the single ended signal to a differential signal.

The selected E/O converter for optical intensity modulation in the initial real-time transmitter is a directly modulated distributed feedback laser (DFB) as specified in table 3.1. The selected DFB is a self contained unit with an adjustable, low noise bias current source fed via a bias-T for an external 50Ω drive signal input. The unit also contains the

drive circuitry for the DFBs thermoelectric cooler (TEC). For the selected cost-sensitive OOFDM transceiver application a directly modulated laser (DML) provides a significantly more cost effective solution compared to external modulation. The laser wavelength of nominally 1550nm is a typical telecommunication wavelength corresponding to the wavelength region of minimum fiber attenuation. Although the selected DFB has a large modulation bandwidth in excess of the signal bandwidth, it should be noted that to further reduce cost a lower bandwidth laser can potentially be used. It is interesting to note here that although directly modulated lasers are the most cost effective solution for IM, the DFB can form a significant portion of the total transceiver cost, chapter 6 therefore explores the use of a low cost vertical cavity surface emitting laser (VCSEL) as the OOFDM intensity modulator.

The selected O/E converter is a square-law photodetector with integrated transimpedance amplifier (TIA) as specified in table 3.1.

Table 3.2. *Transceiver fixed system parameters*

Parameter	Value
Total number of IFFT/FFT points	32
Data-carrying subcarriers	15
n-th subcarrier frequency	n×125MHz
DAC & ADC sample rate	4GS/s
DAC & ADC resolution	8 bits
Symbol rate	100MHz
Samples per symbol (IFFT)	32 samples (8ns)
Cyclic prefix	8 samples (2ns)
Total samples per symbol	40 samples (10ns)

A key system parameter to be selected is the number of data carrying subcarriers, N_{SC}. The number of subcarriers will also determine the number of points N in the IFFT and FFT functions. For the selected IFFT/FFT implementation N must be a power of 2 such that $N=2^C$ where C is an integer. It is beneficial to make N_{SC} large as this reduces the effective overhead of the cyclic prefix and can provide greater flexibility in spectral utilisation due to the narrower subcarrier bandwidths. Investigation of the optimum number of subcarriers can be highly significant for achieving increased system performance, however as N_{SC}

increases the complexity of the IFFT/FFT logic also increases therefore a practical value for N_{SC} is required for initial experimentation. N=32 is considered to provide a suitable compromise between the number of data carrying subcarriers and the design complexity. For N=32 and an IMDD based system N_{SC} is 15. Also the length of the cyclic prefix is selected based on a maximum expected signal dispersion of 2ns. At the sample rate of 4GS/s this corresponds to 8 samples and so the cyclic prefix parameter η is 25%. The subcarrier frequency spacing and the OOFDM symbol rate are a direct consequence of the selected sample rate and IFFT/FFT size. All fixed system parameters based on the selected components and the size of the IFFT/FFT are summarised in Table 3.2.

3.4 OOFDM Transceiver High-level Architecture

3.4.1 Transmitter Architecture

Fig. 3.3 shows the detailed high-level architecture of the real-time OOFDM transmitter. For all interfaces the cable and connector types are carefully selected to match their bandwidth to that of the associated signal. 50Ω cables and terminations are used for single-ended signals and differential signals are all 100Ω.

For initial experimentation it is not practical to implement independent clock generation or recovery in the receiver, therefore a common reference clock is utilised for both the transmitter and receiver. Clock distribution employs two frequency synthesisers to generate all system clocks for both the transmitter and receiver. One synthesiser, designated FS1, operates at frequency R Hz corresponding to the system net bit rate. The second synthesiser, designated FS2 operates at frequency $r_s/2$ Hz, where r_s corresponds to the system sample rate. FS1 and FS2 are synchronised by setting FS2 to operate from its internal reference and FS1 to operate from its external reference input which is connected to FS2s reference output. FS2s sub-rate trigger output is set to generate reference clocks for both FPGAs via suitable level shifters as shown in Fig. 3.3 and Fig. 3.4. An important feature of the DSP design, which is discussed further in sections 3.5.3 and 3.5.4, is the fact that a whole OFDM symbol is processed in parallel thus all samples of one OFDM symbol are generated simultaneously to provide one new OFDM symbol every FPGA clock cycle.

As there are 40 samples per symbol the symbol rate and therefore the FPGA clock is set to $r_s/40$ Hz, the prescaler for the sub-rate trigger clock output of FS2 is thus set to 20.

The transmitter system architecture is best described by considering the signal flow: The BPG is clocked at rate $R/2$ Hz to generate a differential NRZ serial binary test pattern at rate R b/s. After suitable attenuation this feeds the 1:4 demultiplexer to generate 4 differential NRZ binary signals each at rate $R/4$ b/s. After blocking the DC levels the 4 signals are fed via the custom adapter board to the FPGAs high speed transceivers inputs on the FPGA development board. The total aggregate interface speed is limited by the speed of the transceivers to a maximum of 25.5Gb/s. The transceivers are hard-wired dedicated circuitry within the FPGA which can be configured via the Quartus II software by instantiating the ALT2GXB Megafunction in the top level system design. The receiver channels of the transceivers incorporate functions such as differential input buffers, PLL, clock recovery unit (CRU), deserialiser and FIFO buffer. The deserialiser within each receiver channel performs the S/P function to convert the high-speed serial data stream into a lower-speed parallel signal compatible with the processing speed of the logic array. A range of deserialisation factors can be selected. The CRU performs clock data recovery (CDR) thus an external interface clock is not required. The first-in-first-out (FIFO) buffers are employed to account for any phase variation between the transceiver clocks and the logic array clock. The transceiver block also incorporates a loopback function for testing purposes, this is utilised to validate the interface operation by looping back the data from BPG to BEA.

The data received via the GTRXs is then clocked into the FPGAs logic array where the pre-programmed logic will perform the high-speed real-time DSP functions to generate the OFDM signal samples. Full details of the DSP functionality is given in section 3.5.

As one OFDM symbol consists of 32 IFFT samples plus 8 cyclic prefix samples, 8-bits per sample results in 320 bits per symbol generated from the logic array every clock cycle. The interface to the DAC is via the 32 LVDS outputs, these are driven by dedicated high-speed I/O circuitry within the FPGA, this circuitry is configured via the ALTLVDS Megafunction from within Quartus II. The ALTLVDS block contains programmable serialisers for each output thus performing the P/S function depicted in Fig. 3.1 (a). As the
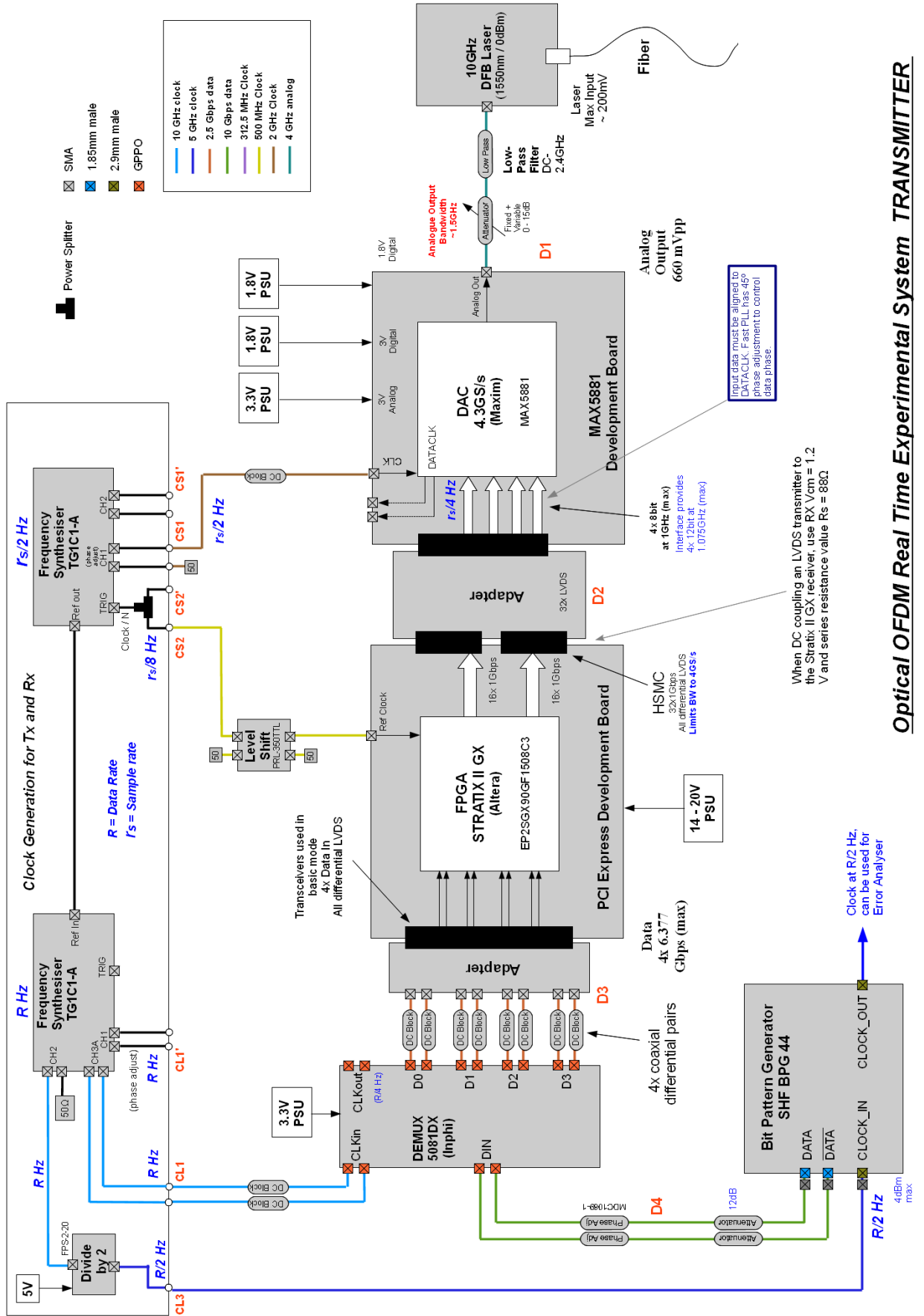
Fig. 3.3 OOFDM Transmitter Top Level Architecture

32-bit LVDS interface width is 4 samples it must be operated at $r_s/4$ Hz and as the symbol rate is $r_s/40$ Hz the serialisation factor is selected as 10:1.

In order to correctly present the OFDM samples to the DAC input ports the 320 OFDM symbol bits must be correctly mapped to the ALTLVDS inputs. The logic block performing the bit mapping function is described in section 3.5.3.6.

The DAC requires a reference clock at half the sample rate which is fed form FS2. The DAC consists of four interleaved converters each operating at 1GS/s so the 2GHz clock is further subdivided to 1GHz internally in the DAC. In order to ensure the DAC input data and the internal DAC clock are correctly phase aligned the phase of the FS2 clock output can be manually adjusted. To test the DAC interface FPGA designs were implemented to digitally generate sine waves at different frequencies. The DAC output was then observed via a high-speed sampling oscilloscope to view the generated sine waves. Correct generation of the sine waves was verified at a sample rate of 4GS/s, this verified operation of the FPGA, the FPGA to DAC interface including the custom adapter boards, the DAC and the associate system clocking.

The DAC development board converts the DACs differential output to a 50Ω single end output configured with a maximum output voltage of 660mVpp. For initial experimentation the DAC output was not amplified and a variable RF attenuator is employed to control the analogue signal level which directly modulates the DFB laser. A low-pass filter as specified in Table 3.2 is shown before the DFB input in Fig. 3.3, however this was found to be unnecessary due to the low-pass filtering effect of the DAC at the chip level and due to the evaluation board analogue interface. For initial experimentation the output from the DFB was directly coupled into the fiber without optical amplification.

Photographs of the real-time OOFDM transceiver electronics are shown in Fig. 3.5 where the transmitter section is shown in the lower part of the photograph. The use of the FPGAs integrated S/P and P/S dedicated hardware shows how the interconnectivity between the FPGAs and the converters is simplified.

3.4.2 Receiver Architecture

Fig. 3.4 shows the detailed high-level architecture of the real-time OOFDM receiver. The basic architecture is similar to that of the transmitter however signal flow is now in the opposite direction initiating from the incoming optical signal and terminating at the BEA. Clock distribution is also similar to that of the transmitter.

The received optical signal from the fiber is coupled directly to the photodetector consisting of PIN and TIA, the electrical output from the photodetector is then low-pass filtered before amplification by a fixed 20dB RF amplifier, this is followed by variable attenuators to allow manual control of electrical signal level. As the received optical power level is adjusted during experimentation the electrical gain is adjusted to compensate the optical varying attenuation and maintain the optimum signal amplitude at the ADC input. As the ADC development board has a differential input the signal is converted from single-ended to differential via a balun as specified in Table 3.1.

The interface between the ADC and the FPGA is the reverse of the corresponding interface in the transmitter, now the ALTLVDS dedicated hardware receiver channels are employed. Programmable deserialisers perform the S/P function to convert the 4 parallel samples from the ADC into 320 parallel bits at the logic array interface corresponding to the length of one symbol. The 320 parallel bits from the ALTLVDS block will be 40 consecutive samples arbitrarily located within the received signal. Symbol alignment is therefore required within the FPGA before a symbol can be processed. Symbol alignment is described in section 3.5.4.3. The 32 deserialisers in ALTLVDS interface must also be synchronised so that they all operate with the same signal latency. Synchronisation of the ADC interface is a process required each time the system is powered up. The synchronisation process involves connecting the FPGAs in a digital back-to-back configuration and sending a training pattern from the transmitter FPGA, the interface synchronisation is fully described in section 3.5.4.1. To achieve the aforementioned digital back-to-back configuration two DAC adapter boards are connected together to allow cables from each FPGA board to be connected. This configuration results in a reorganisation of the bit locations and so the effect must be reversed within the receiver FPGA when this configuration is used.

To validate the operation of the ADC interface the ADC test pattern generation function was utilised. An FPGA design is implemented which allows the 40 samples from the ALTLVDS interface to be probed via the SignalTap II integrated logic analyser. With the ADC configured to generate a test pattern the internal FPGA samples are viewed to check for compliance with the test pattern. A more advanced FPGA design was also implemented to generate a similar test pattern and automatically verify the received samples correspond to the transmitted test pattern.

Further verification of the system was performed by connecting the FPGA boards in the digital back-to-back configuration and generating sine wave in the transmitter FPGA. The received signal in the receiver FPGA was then viewed via the SignalTap II application to verify that the received signal was also a sine wave.

The real-time OOFDM receiver also provides connection to the BEA via the four transmit channels of the high-speed transceivers which provide the required P/S function. A custom adapter board provides the interconnection between the transceiver interface on the FPGA development board and a 4:1 multiplexer. The multiplexer combines the four transceiver signals to a single serial bit stream which is connected to the BEA via a suitable attenuator.

As previously mentioned the real-time OFDM transmitter and receiver can be connected in a digital back-to-back configuration. Other configurations are possible to allow step-by-step performance verification and analysis of the system. The other configurations possible are i) analogue back-to-back where the DAC output is connected to the ADC via a low-pass filter, attenuator and balun, ii) optical back-to-back where the DFB (or other E/O) output is connected via an optical attenuator to the photodectector (or other O/E) and iii) the full OOFDM transmission system incorportating the transmission fiber.
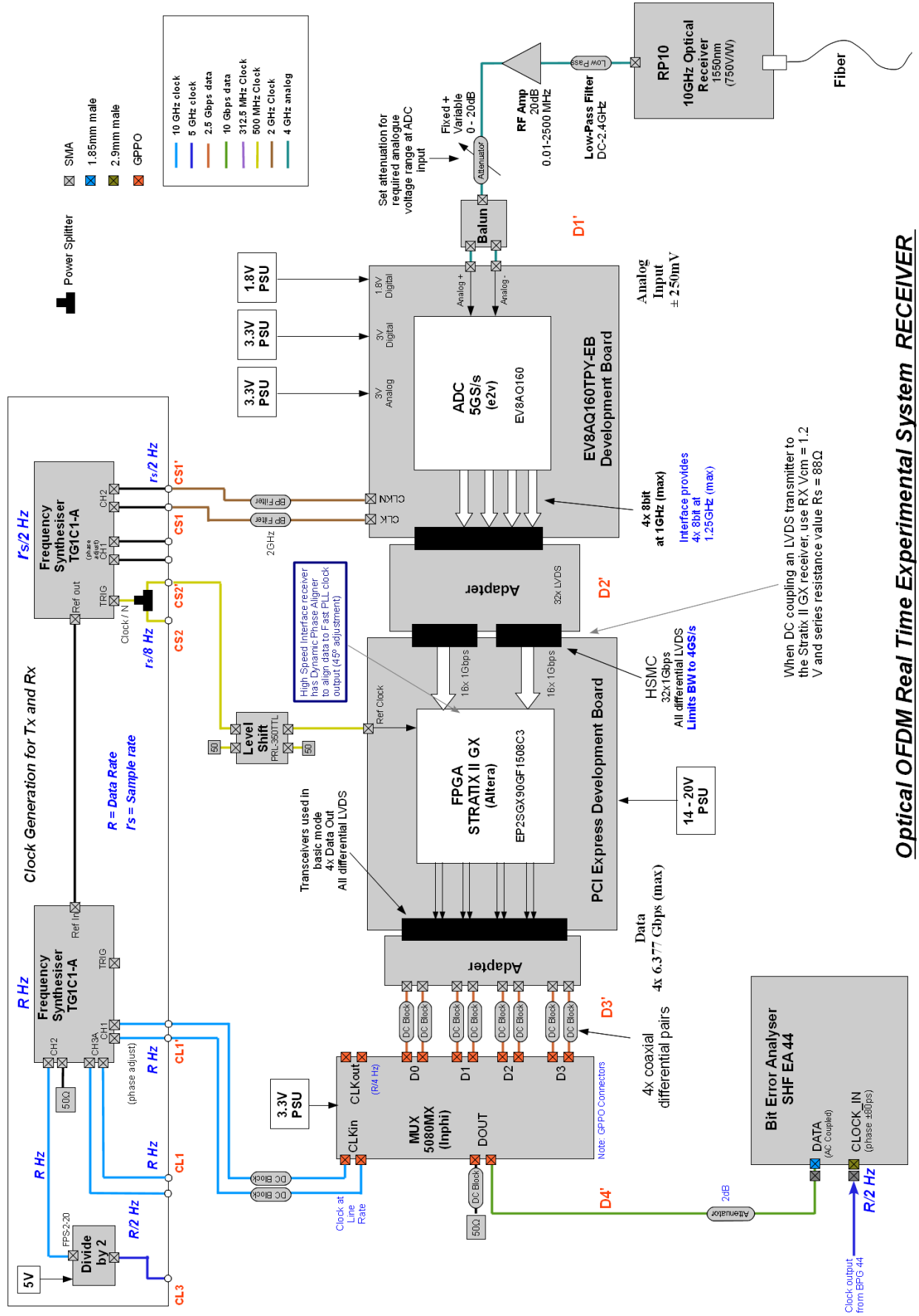
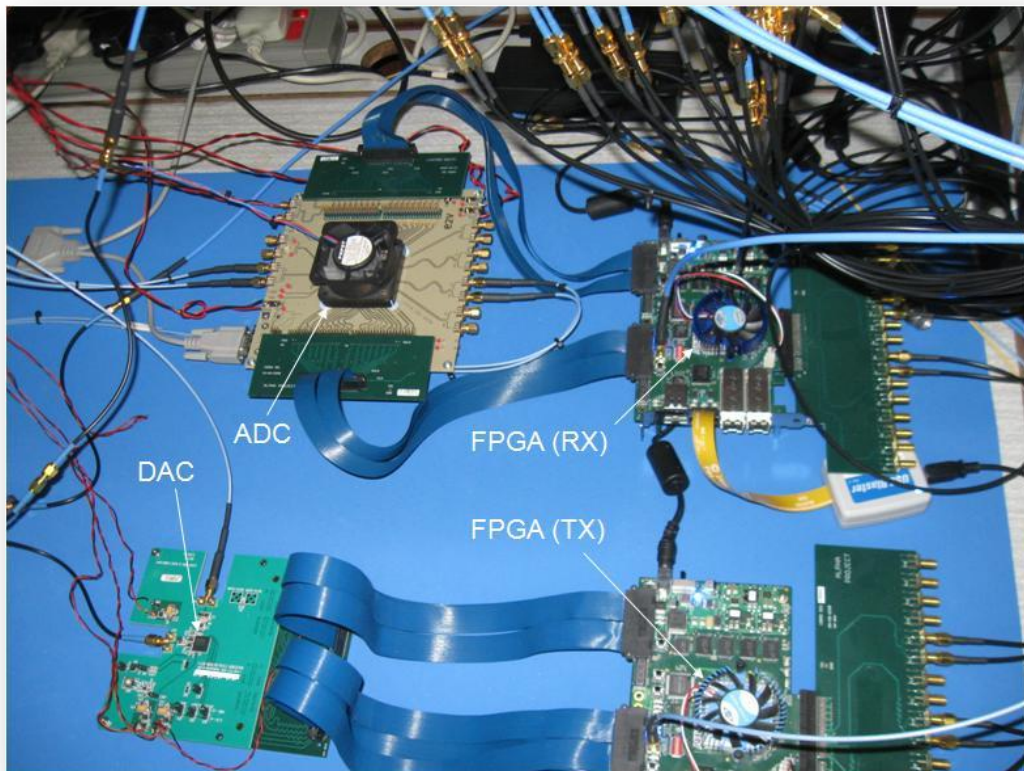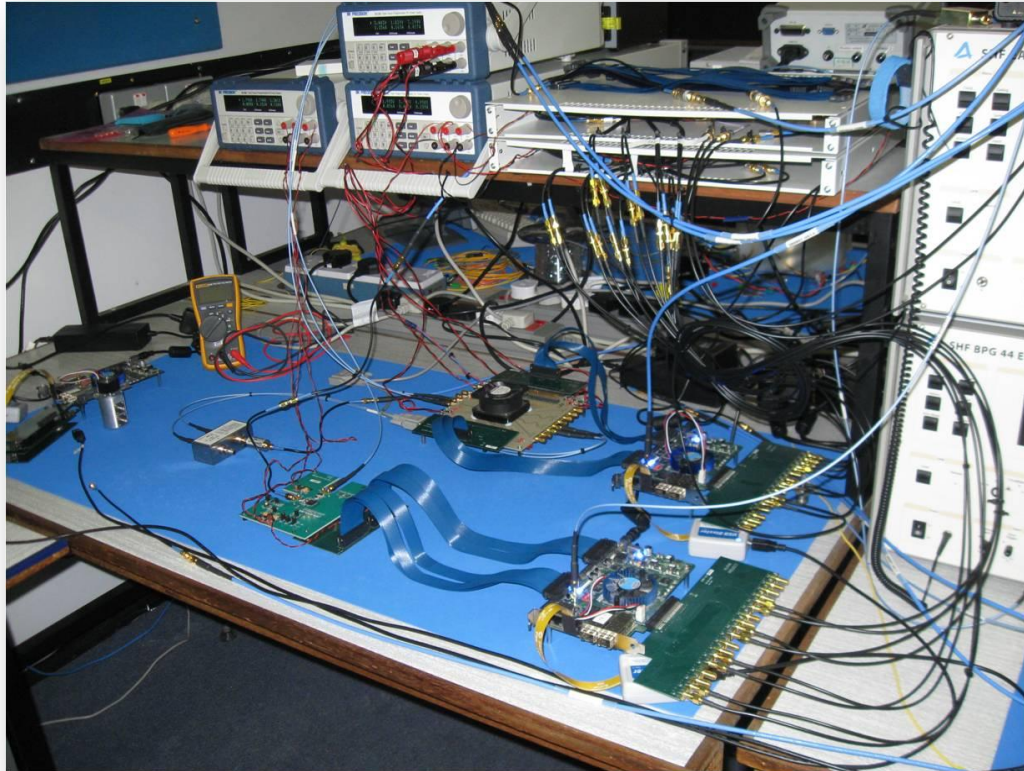*Fig. 3.4 OOFDM Receiver Top Level Arcitecture*

Fig. 3.5 Implemented Real-time OOFDM transceiver electronics

3.5 DSP Architecture Design

3.5.1 Design Environment and Testing Strategy

To design the DSP logic for configuring the FPGAs a design environment and design flow is employed that allows individual functional blocks, subsystems and the high level system to be constructed and verified at different levels of abstraction. MatLab™ and Simulink™ provide a comprehensive system modelling and simulation environment with a graphical user interface for building hierarchical system models. Models are constructed from component toolboxes which are comprehensive libraries of fundamental building blocks. Simulink supports modelling and simulation in discreet-time for compatibility with digitally sampled logic. Multi-rate systems are also supported such as in the case of a multiple clock logic system. The environment allows rapid evaluation of different designs and model verification can be performed at different levels. Altera's DSP Builder™ is a design toolbox that integrates with Simulink™ to provide a library of circuit elements from which designs can be directly compiled into a hardware description language (HDL). Verilog HDL (VHDL) is employed in this case. Individual DSP functions or sub-systems are first designed and constructed in Simulink with DSP Builder™ library elements. Initial design verification is then performed by addition of suitable test circuitry for test pattern generation and output data analysis and display, for example Vector Scopes can be used to view constellation diagrams. Data can also be directly output as MatLab™ variables for further processing and analysis. The test circuit elements can be selected from other Simulink™ toolboxes in addition to DSP Builder™ as they are not included in the compiled design. The Simulink™ design is simulated to verify operation and can be rapidly modified to evaluate alternative logic designs. Once the design is verified in Simulink™ a version, without the additional test circuitry, is compiled to generate a VHDL representation of the design. It should be noted that VHDL generation from DSP Builder™ models does not result in highly optimised logic, in terms of silicon area or power consumption, compared to direct coding in VHDL. However, for the proof-of-concept purpose logic optimisation is not critical unless required for enhancing processing performance.

Quartus II™ is Altera's FPGA design software which provides a comprehensive FPGA design environment. System designs are constructed by integrating multiple VHDL-based

functional blocks, in this case created in Simulink™ with DSP Builder™. The complete design is then synthesised to generate a netlist based on primitive logic gates. The netlist is then fitted to the FPGA logic array and the FPGA programming file generated. The Quartus II™ software incorporates an embedded logic analyser, SignalTap II™, which allows the state of predefined nodes to be probed during operation, this is used for design debugging purposes and to extract key system performance parameters during operation such as bit error counts and channel response. An example SignalTap II™ output is shown in Fig. *3.6*. The Stratix II GX FPGA also has embedded memory which can be incorporated into the design to store system parameters which can then be updated in real-time via the Memory Content Editor within Quartus II™. This feature is fully exploited in later design enhancements to enable the rapid online optimisation of various system parameters which directly impact system performance.
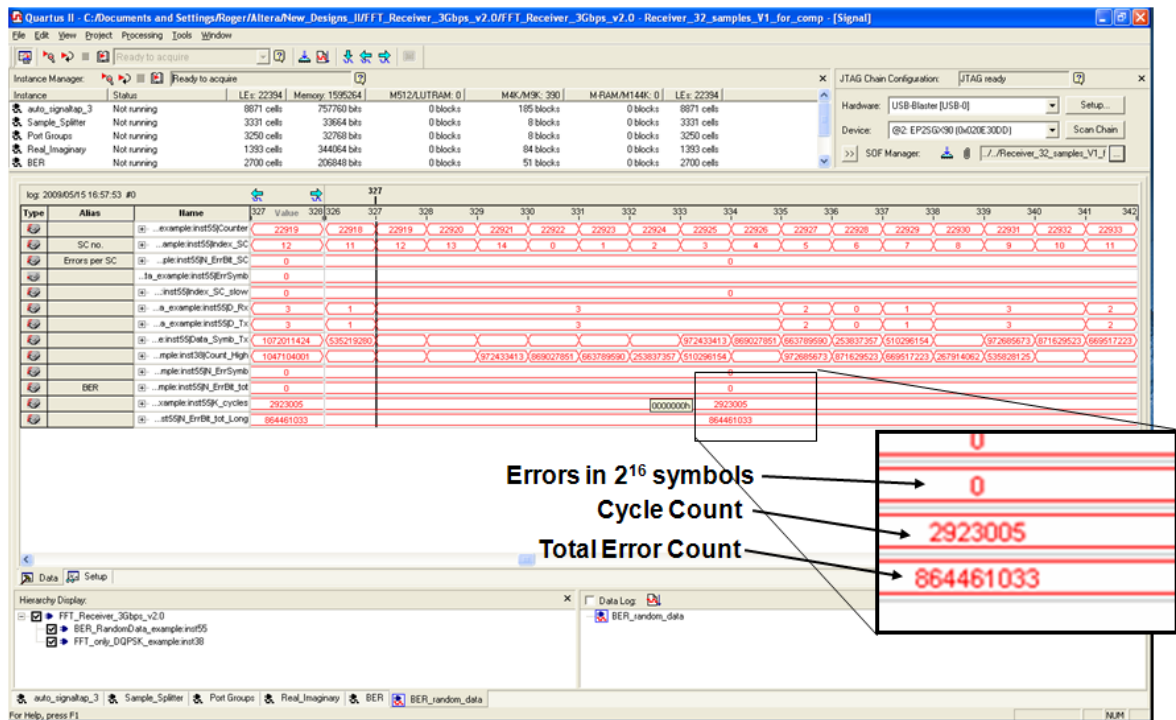
Fig. 3.6 Performance monitoring with Signal Tap II Embedded Logic Analyser

3.5.2 IFFT/FFT DSP Design and Verification

The IDFT and DFT are the fundamental algorithms at the heart of the OOFDM transceiver and indeed all OFDM-based systems, the successful design and verification of the implemented DSP algorithms are therefore crucial to the operation of the real-time OOFDM transceiver and so will be discussed in detail in this section.

The IDFT and DFT are the algorithms which perform the simultaneous transformation of multiple subcarriers between the frequency domain and the time domain and vice-versa. To explicitly compute x_n and X_k from the definitions of an N point IDFT and DFT, as given in Eq.(2.10) and Eq.(2.11) respectively, would require approximately N^2 complex multiplications and N^2 complex additions. For a hardware-based implementation of the transforms it is highly advantageous to minimise computational complexity in order to minimise design complexity. Furthermore the extremely high IDFT/DFT real-time computational throughput inherent to OOFDM implies that a highly parallel and pipelined architecture is necessary, this makes it difficult to reuse complex functions for more than one calculation during one transform cycle. Therefore, minimising the number of discreet instances of complex functions in the algorithm is vitally important if ultimately silicon cost and power consumption targets are to be met. It is worth noting here that in the case of off-line OOFDM experiments the number of complex calculations involved in the software based IDFT/DFT algorithm is of no direct significance and no optimisation has been reported in any of the off-line OOFDM work.

The FFT and IFFT are highly computationally efficient algorithms for computing the DFT and IDFT respectively, drastically reducing computational complexity makes them highly appropriate for implementation in physical hardware. The FFT was first introduced by John Tukey and James Cooley in 1965 in their seminal paper "An algorithm for the Machine Calculation of Complex Fourier Series" [8]. The FFT is regarded by some as one of most important numerical algorithms of our lifetime, indeed virtually all OFDM-based systems are dependent on the FFT algorithm. Therefore due to the IFFT/FFT's highly efficient use of complex operations and therefore logic resources, the IFFT and FFT are implemented in the real-time OOFDM transmitter and receiver respectively. It is also important to highlight the fact that OOFDM system performance can be improved by employing a large number of subcarriers, this requires higher order IDFT/DFT algorithms thus the logic efficiency benefits associated with the IFFT/FFT algorithm are more significant as subcarrier count increases. The IFFT can be created from an FFT by simple modification of the so called "twiddle factors", as discussed in section 3.5.2.1, therefore the following discussions will concentrate on the FFT although they are equally applicable to the IFFT.

The fundamental principle of the FFT is to take the input sequence of N coefficients and split it into smaller sub-sequences. For this description we split the original sequence into two sequences of length $N/2$. Two DFTs of length N/2 can now be performed and the resulting two $N/2$ output sequences can be recombined to form the N point output sequence of the original DFT. The recombination process takes care of the associated time shift between the sequences. This splitting approach can be continued on the sub-sequences by further division of the sub-sequences for $M = \log_2N$ total steps until the N-point DFT is replaced by N DFTs of length 1. The DFT operation is now trivial as the DFT of a 1 point sequence is itself. The task of the FFT is then to correctly recombine the transformed 1-point sequences according to the splitting method thus recombining the N 1-point sequences into N/2 2-point sequences, and then these into N/4 4-point sequences and so on until the final single N-point transform sequence X_k is formed.

When the original sequence and all sub-sequences are equally divided at each step this is a radix-2 FFT as $N=2^M$ where M is the number of recombination steps. Other radixes are created when the sequence is split into more than two sub-sequences at each stage, for example if the original sequence is first split into 4 sub-sequences and this is repeated for $M = \log_4N$ steps, $N=4^M$ and it is a radix-4 FFT. The possible radix values that can be employed are therefore dependent on the required value of N. To allow more flexibility in the value of N it is also possible to create mixed radix FFTs.

A detailed examination of the conversion of one N-point DFT into two $N/2$-point DFTs will be presented as this also explains the origin of the fundamental building block of the FFT, the butterfly operator. If the original time domain sequence x_n is split into its even and odd sequences of $y_n=x_{2n}$ and $z_n=x_{2n+1}$ respectively for n=0,1,..,(N/2)-1 and substituted into the IDFT as defined in Eq.(2.11) this becomes:

$$X_k = \sum_{n=0}^{\frac{N}{2}-1} \{ y_n\omega_N^{-2nk} + z_n\omega_N^{-(2n+1)k} \} \tag{3.1}$$

where $\omega_N = e^{\,\mathrm{j}2\pi/N}$. Eq.(3.1) can be rewritten using the relation $\omega_N^{-2nk} = \omega_{N/2}^{-nk}$ as:

$$X_k = \sum_{n=0}^{\frac{N}{2}-1} y_n \omega_{N/2}^{-nk} + \omega_N^{-k} \sum_{n=0}^{\frac{N}{2}-1} z_n \omega_{N/2}^{-nk} \tag{3.2}$$

The original DFT has now been expressed as a simple combination of two DFTs each of length $N/2$. The DFT on the right of Eq.(3.2) is multiplied by the factor ω_N^{-k} which accounts for the relative time shift between the sub-sequences and is known as the twiddle factor. If these $N/2$-point DFTs are denoted as Y_k and Z_k respectively we can write:

$$X_k = Y_k + \omega_N^{-k} Z_k \tag{3.3}$$

$$X_{k+\frac{N}{2}} = Y_{k+\frac{N}{2}} + \omega_N^{-(k+\frac{N}{2})} Z_{k+\frac{N}{2}} \tag{3.4}$$

for k = 0,1,..(N/2)-1. Eq.(3.4) can be further simplified as $\omega_N^{-N/2} = -1$ and Y_k and Z_k have a period of $N/2$, which gives the following pair of equations known as butterfly operators:

$$X_k = Y_k + \omega_N^{-k} Z_k \tag{3.5}$$

$$X_{k+\frac{N}{2}} = Y_k - \omega_N^{-k} Z_k \tag{3.6}$$

These butterfly operators are the fundamental FFT building blocks used at the recombination stages of the radix-2 FFT and are generally depicted by the symbol shown in Fig. 3.7. To convert two sub-sequences Y_k and Z_k to the single N-point sequence X_k will require $N/2$ discreet butterfly operators.
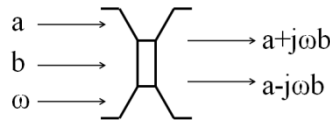

Fig. 3.7 Radix -2, Decimation-in-Time, Butterfly Element

Different radix values and sequence splitting methods will have their own corresponding butterfly elements. The radix-4 butterfly for example has 4 coefficient inputs, three twiddle factor input and 4 coefficient outputs.

The selected splitting method can affect the order of the sequence reordering and the sequence recombination. The above example splits the original sequence and the sub-sequences into even and odd sequences, this requires the input coefficients x_n to first be reordered and then the sequences to be recombined. As x_n is reordered this type of FFT architecture is known as decimation-in-time. If however the splitting method divides according to the first-half and last-half sub-sequences, x_n and $x_{n+N/2}$, where n=0,1,..,(N/2)-1, the FFT first performs the recombination of the naturally ordered input sequence and then reorders the X_k coefficients. This type of FFT architecture is therefore known as decimation-in-frequency.

The selected architecture for the FFT and IFFT implemented in the real-time OOFDM transceiver is based on the fact that a 32-point DFT is required. A radix-2 FFT can be used as $N = 32 = 2^5$. Although other radix levels can potentially offer a small reduction in complexity for certain architectures no other radix level can support 32-point sequences. Increasing N to allow for higher radixes will simply increase the overall logic recourses further. There is no difference in the complexity of decimation-in-time and decimation-in-frequency therefore decimation-in-time is selected as the associated radix-2 butterfly element is available as a DSP Builder™ primitive component. The implemented FFT architecture is therefore the Cooley-Tukey radix-2 decimation-in-time.

To implement the IFFT it is only necessary to modify the twiddle factors which is apparent from the opposite sign of the exponential power in the IDFT in Eq.(2.10) compared to the DFT in Eq.(2.11). Thus for the IFFT the twiddle factors are now ω_N^{k}. In the Simulink™ model for the FFT the twiddle factors are defined as a model parameter which consists of a 1xN array of twiddle factors associated with k=0,1,…,N-1. To convert the FFT model to an IFFT model the twiddle factor values are simply replaced with their complex conjugates.

It is important to considering the saving in computational complexity achieved by the implemented FFT architecture compared to the explicit computation according to the DFT definition in Eq.(2.11). Explicit computation requires approximately N^2 complex multiplications and N^2 complex additions. However now there are 5 recombination stages each with 16 butterfly operators making a total of 80 butterflies. More generally a radix -2 N-point FFT will have $(N/2)\log_2 N$ butterfly operators, each consisting of one complex multiplier and two complex additions. Thus in total there are $(N/2)\log_2 N$ complex

multipliers and $N\log_2 N$ complex additions. For the case of the implemented 32-point FFT the computational saving is ~92% for the complex multiplications and ~84% for the complex additions. The actual saving is higher when taking into account the instances where the twiddle factors are unity. The immense computational efficiency of the IFFT is clear from the savings achieved. Furthermore the computational saving increases further with higher values of *N*. For a hardware-based implementation of the DFT the FFT is therefore indispensable due to the advantages associated with the vast reduction in the required logic resources, such as lower cost and lower power consumption. The FFT and IFFT will still constitute one of the largest logic functions, if not the largest logic function in the OOFDM transceiver and so the optimisation of the FFT logic is an important issue. The ultimate optimisation of the FFT/IFFT logic is not a critical requirement in this research as the primary focus is to first prove the practicality of real-time OOFDM transmission with real-time hardware-based FFT/IFFT algorithms.

3.5.2.1 IFFT/FFT DSP Algorithm design

In contrast to the software-based IFFT/FFT algorithms employed in the off-line OOFDM transmission systems [9-11] the hardware-based IFFT/FFT algorithms for the real-time OOFDM system are restricted by the limited speed and precision of the DSP logic. Thus a key challenge for the IFFT/FFT implementation is to achieve enough speed and precision whilst maintaining acceptable logic utilisation.

As the IFFT/FFT must perform one complete transform during each OFDM symbol period the transform throughput is dictated by the required symbol rate. The approach adopted to meet the transform throughput rate is to employ a parallel input port, which can support all 32 complex inputs in parallel, and pipeline the recombination stages. The logic function can therefore accept a new transform input sequence on each clock cycle although it takes multiple clock cycles to compute the output transform sequence. In this way the clock frequency required is equal to the symbol rate which will be in the order of a few 100 MHz and within the clocking range of the digital logic.

The bit resolution of the various IFFT/FFT internal logic values, including the inputs, outputs and all intermediate recombination values, will impact both the FFT accuracy and the logic resource utilisation. All logic values must be represented by a finite number of bits, which will inevitably result in quantisation errors at the complex operator outputs.

100

Higher bit resolutions are therefore desirable to minimise quantisation errors however this leads to an increased demand on logic resources. The bit resolutions must therefore be selected to achieve a balance between the overall FFT accuracy and logic usage. The bit resolution of all input values is selected as 8-bit signed complex values as the received OFDM signal at the FFT input is quantised to 8-bits and this is also is sufficient to accurately represent high modulation formats (up to at least 256-QAM) at the IFFT input in the transmitter. The bit resolution of the complex-valued twiddle factors will also influence accuracy and logic usage. First it is worth considering the format used for the twiddle factors. According to the definition the twiddle factors are complex vectors with unity magnitude and varying arguments, thus the real and imaginary values are fractional. However the twiddle factors can be scaled up to avoid the need for fractional binary values if this is compensated by appropriate scaling of the "a" or "b" input to achieve a uniform scaling of the complex outputs. The output bit resolutions however are only dependent on the input bit resolutions and are independent any twiddle factor scaling. The input and output bit resolutions for the radix-2 butterfly operator are shown in Fig. 3.8 (a) for the general case. Fig. 3.8 (b) shows the bit resolutions for the case where suitable downscaling of the "b" input is used to limit the growth in bit resolution from input to output. For the first recombination stage the twiddle factors have a value of +1 therefore do not contribute to increased bit resolution at the butterfly outputs as the complex multiplication is omitted. For the first stage the butterfly additions thus result in 9-bit complex outputs. The output bit resolutions for the following recombination stages are shown in table 3.1 based on the bit expansion illustrated in Fig. 3.8 (a) with 8-bit complex inputs and 8-bit complex twiddle factors. The bit resolutions are obviously excessive especially considering that these are all complex values, the final output stage will have a total of $45 \times 2 \times 32 = 2885$ bits. Limiting the precision at each recombination stage is therefore necessary to reduce logic utilisation whilst maintaining sufficient computational accuracy.
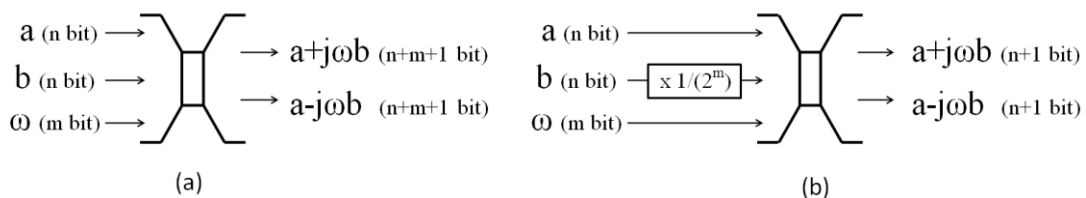

Fig. 3.8 Radix-2 Butterfly Elements with parameter bit resolutions
(a)Without "b" scaling, (b) With "b" scaling

Table.3.1 Bit Resolutions without Precision Limiting for
8-bit Inputs and 8-bit Twiddle Factors

Butterfly Stage	Input bit resolutions	Output bit resolutions
1	8	9*
2	9	18
3	18	27
4	27	36
5	36	45

* Twiddle factor =1 removing complex multiplier

The top level Simulink™ model for the IFFT is shown in Fig. 3.9. The 256-bit input bus is split into 32 8-bit values which constitute the 16 pairs of real and imaginary values corresponding to the 16 complex subcarrier coefficients, including the zero valued DC coefficient. These are passed to a block which generates the complex conjugates of each input and arranges the 32 complex values with Hermitian symmetry, as described in section 2.3.3, needed for the generation of real valued time domain coefficients. The IFFT block performs the 32-point IFFT and the resulting 32-point clipped sequence of real values is concatenated into a 256-bit output bus. The top level schematic of the IFFT block is shown in Fig. 3.10 where the different computational stages are shown. The characteristic inter-stage connection pattern between the butterfly stages is indicative of the recursive even-odd sequence splitting method used for the decimation-in-time architecture. The necessary clipping function is also included as the last stage although this is not directly part of the IFFT algorithm. To limit bit escalation as the signals flow through the IFFT stages the following approach is adopted:

- For the first butterfly stage as twiddle factors = 1, the multiplication operation is absent and no precision limiting is employed. This stage is therefore implemented with butterfly operators constructed from two complex add/subtract operators as shown in the schematic in Fig. 3.11.
- An intermediate stage then scales all next stage "a" inputs by a scaling factor *SF* where $SF = 2^L$ and *L* is an integer. The schematic for this stage is shown in Fig. 3.12.
- The second butterfly stage employs a twiddle factor scaling factor of *SF*. The butterfly outputs are thus scaled by *SF*. The schematic for the second stage butterflies is shown in Fig. 3.13.

- For the 3rd, 4th and 5th butterfly stages all "b" inputs are prescale by 1/*SF* and twiddle factor scaling of *SF* is again employ. The scaling factor *SF* is selected to be of the form 2^{L} so that "b" scaling is thus simply performed by removing *L* LSBs from the input value. The scaling factors will therefore cancel in the output values and output bit precision has been reduced by *L* bits. The structure of the 3rd, 4th and 5th butterfly stages is similar to that of the 2nd stage butterflies shown in Fig. 3.13 where the "b" prescaling blocks for the next stage are incorporated. The 5th stage is the last stage therefore does not incorporate "b" prescaling blocks.

The 2nd stage butterflies' "b" inputs are not prescaled as this would lead to a low bit resolution causing large quantisation errors. The FFT and IFFT Simulink™ models were designed with *L* as a model parameter which could be easily edited to change the "b" scaling factors and the twiddle factor scaling factors within the model, thus allowing rapid investigation of an optimum scaling factor. Selecting *L*=5 for *SF*=32 was found to give a high level of IFFT/FFT accuracy as presented in section 3.5.2.2, whilst achieving an acceptable level of bit escalation. The FFT bit resolutions corresponding to the precision limiting case with *SF*=32 are given in table 3.2. It is clear that bit resolutions have been considerably reduced compared to the non-precision limited case.
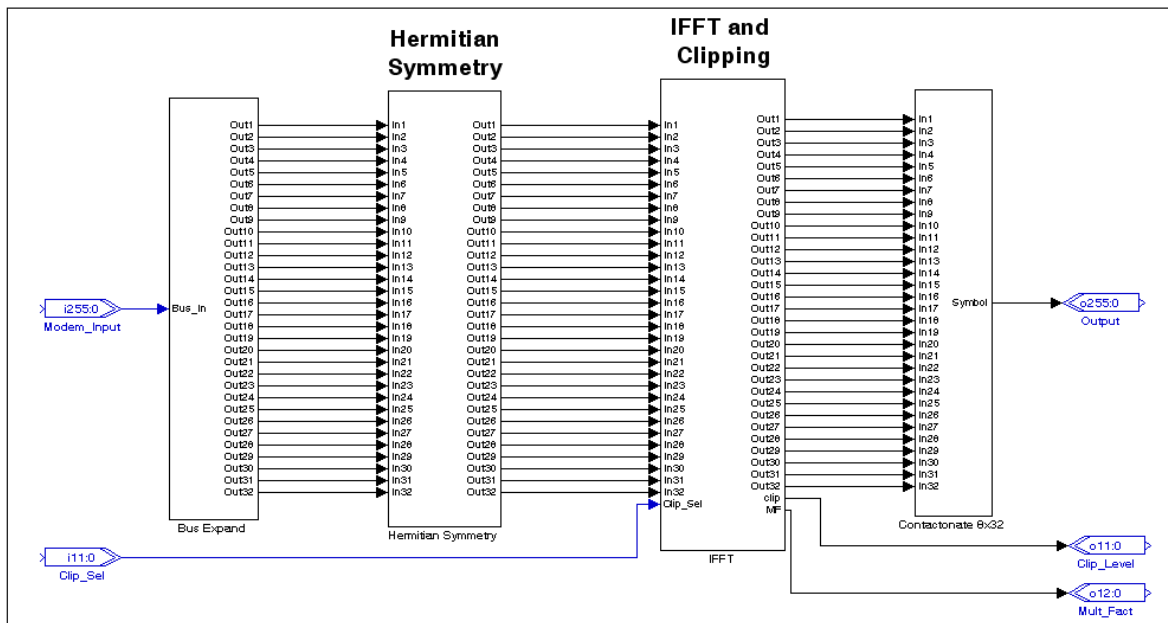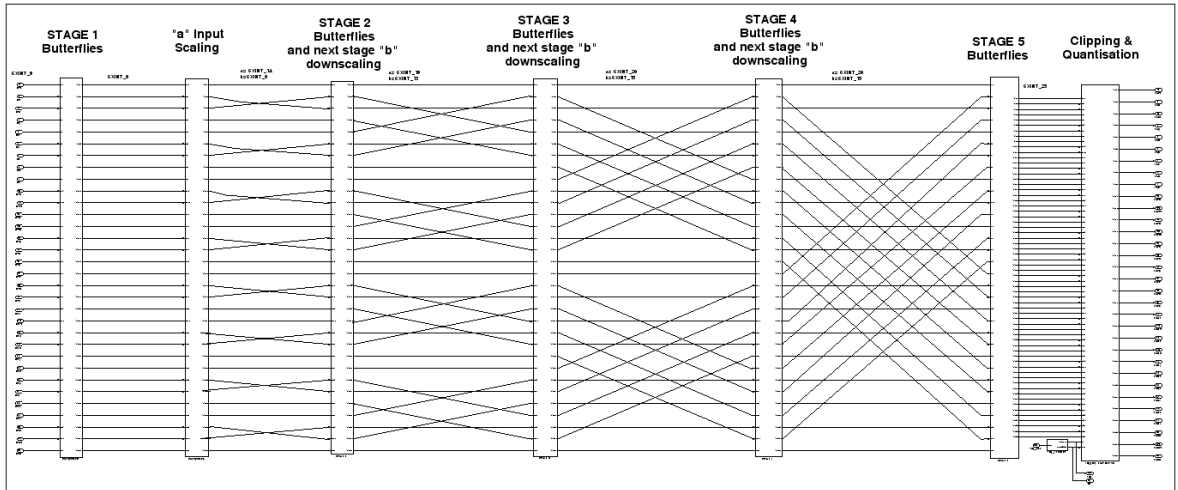

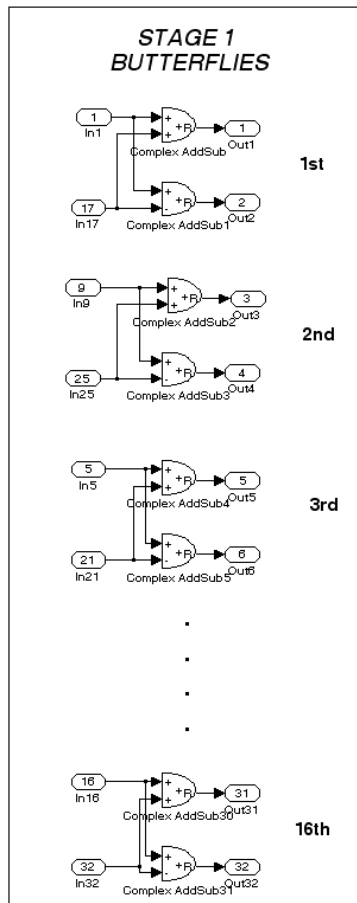*Fig. 3.9 IFFT Block Top Level Model*

Fig. 3.10 IFFT Block

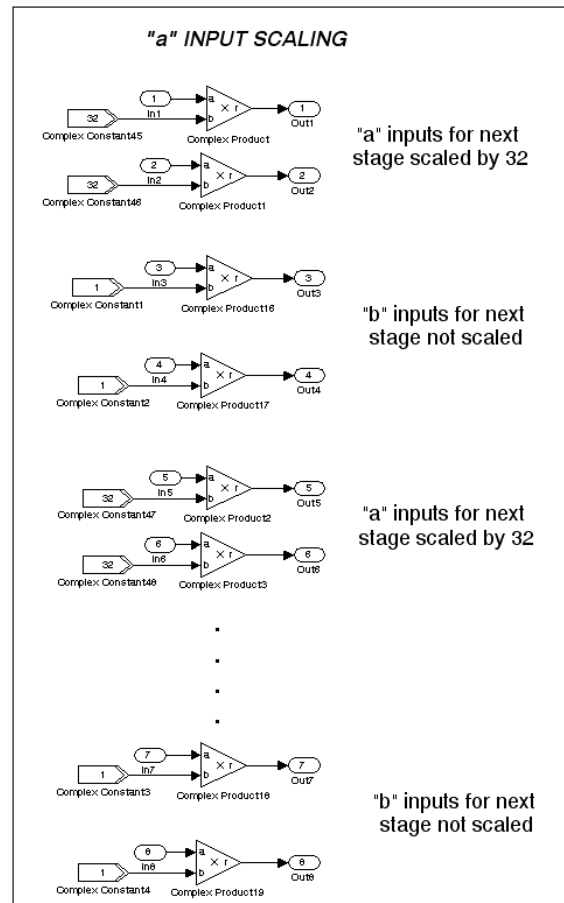*Fig. 3.11 First Stage Butterflies without multiplication operator*

Fig. 3.12 "a" Input Scaling

Table.3.2 Bit Resolutions with Precision Limiting for
8-bit Inputs and 5-bit Twiddle Factors

Stage	Input bit resolutions (a/b)	Output bit resolutions
1st Butterflies	8/8	9*
"a" scaling	9	14/9
2nd Butterflies	14/9	15
3rd Butterflies	15/10	16
4th Butterflies	16/11	17
5th Butterflies	17/12	18
Clipping	18/18	8

* Twiddle factor =1 removing complex multiplier

The implemented IFFT and FFT algorithms each use less than 20% of the Stratix II GX logic resources, this is based on the fact that the IFFT/FFT back-to-back design described in section 3.5.2.2, which includes 16-QAM modulators and demodulators and a test data generator, utilises 40% of the FPGA logic.
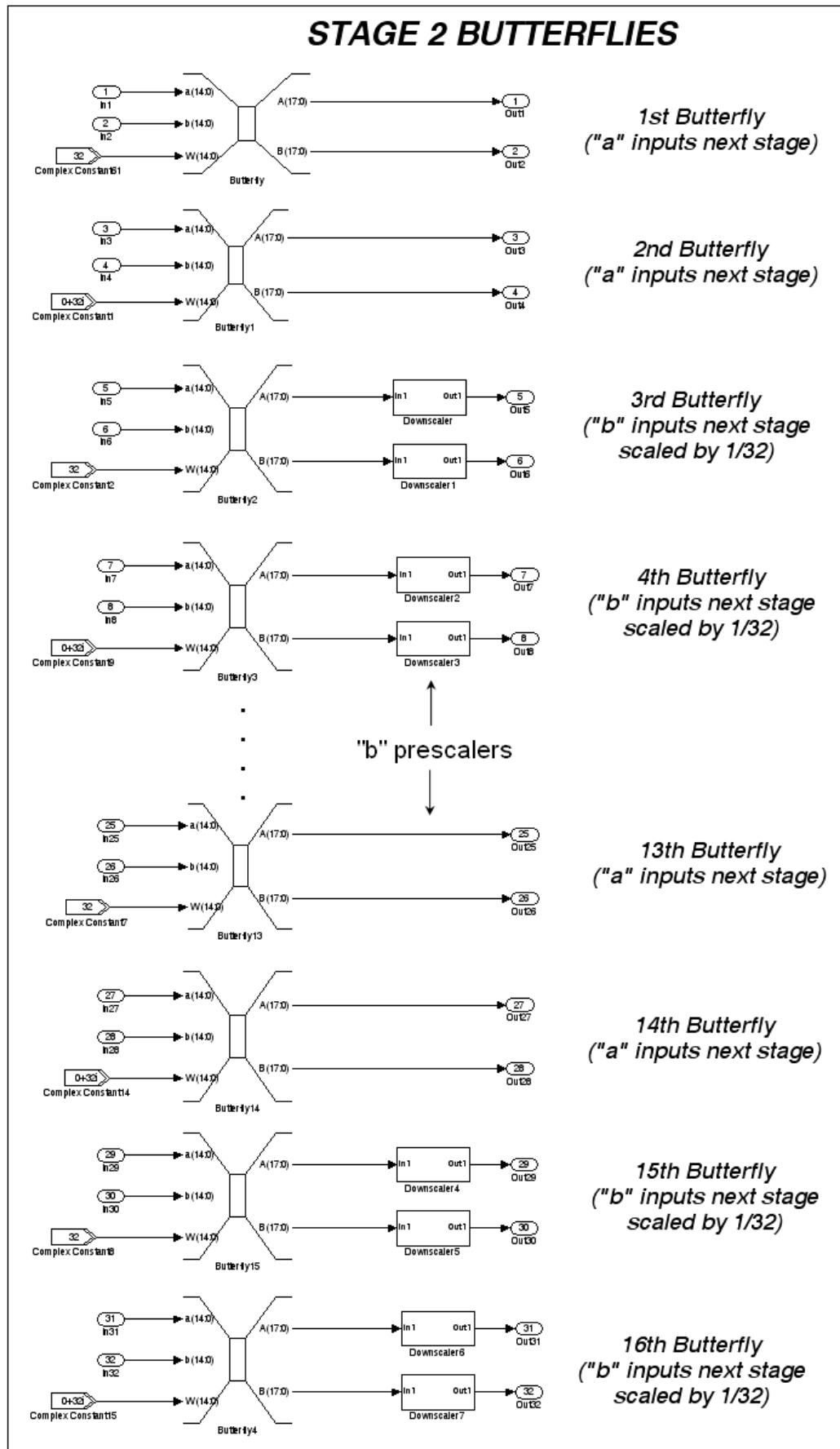
Fig. 3.13 Stage 2 Butterflies and Next Stage "b" scaling

It should be noted that the twiddle factors have the characteristic that the number of different twiddle factors doubles with increasing recombination stage, therefore higher bit resolution is required to accurately represent twiddle factors as the recombination stage increases. This characteristic could be exploited to reduce logic usage by tailoring the twiddle factor resolution to the required accuracy and also designing the butterfly elements' multipliers accordingly. The DSB Builder™ butterfly elements can be configured for different input bit resolutions however all inputs must have the same bit resolution. The selected scaling factor and therefore bit resolution of the twiddle factors is thus based on the worst case which is stage 5 where there are 16 different twiddle factors.

The system will operate with 8-bit samples so clipping and quantisation of the IFFT output is essential for testing the operation of the FFT with a clipped OFDM input. For this reason the clipping and quantisation block is included as the last stage in the IFFT function. The block contains 32 instances of the clipping logic function shown in Fig. 3.14 so that all parallel samples are simultaneously clipped at $\pm C$ where C is the clipping level. Comparators compare the input sample against $+C$ and $-C$ which is set by an external input. The comparator outputs directly control a multiplexer which selects the input sample if it is within the range $-C$ to $+C$, selects $+C$ if the sample exceeds $+C$ and selects the $-C$ if the sample is less than $-C$. The input sample is thus clipped to the range $\pm C$.
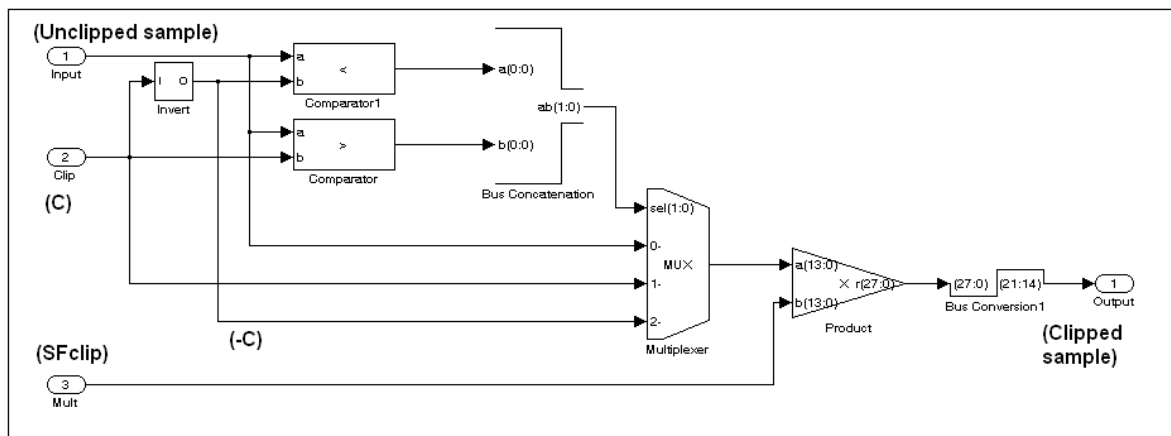
Fig. 3.14 Clipping Logic

To quantise the clipped samples to 8-bits, each sample is first multiplied by a scaling factor, SF_{clip}, corresponding to $(2^{21}-1)/C$. The clipped range then corresponds to the full range represented by a 22-bit signed value. Quantisation to 8-bit signed values is then simply performed by truncating the value to the 8 MSBs. Furthermore by restricting C to a minimum value of 256, SF_{clip} will have a maximum value of 8192 and so can be limited to

13 bits resolution thus minimising the size of the required multipliers performing the sample scaling.

3.5.2.2 Design Verification of IFFT/FFT DSP algorithms

During FPGA logic design all DSP logic functions were extensively tested to verify their operation following the test strategy described in section 3.5.1. As the 32 point IFFT and FFT blocks perform the key OFDM algorithms the test and verification of these blocks is described here in more detail as successful implementation of the IFFT and FFT in the FPGA was a significant milestone towards achieving the first end-to-end real-time OOFDM demonstration. The adopted test solution allowed initial evaluation of the IFFT/FFT performance at virtually 10Gb/s throughput. The IFFT/FTT functions were first tested and functionally verified in a Simulink™ model including pseudorandom data generation, 15x 16-QAM data encoders, IFFT, FFT, 15x 16-QAM data decoders and an error detector/counter.
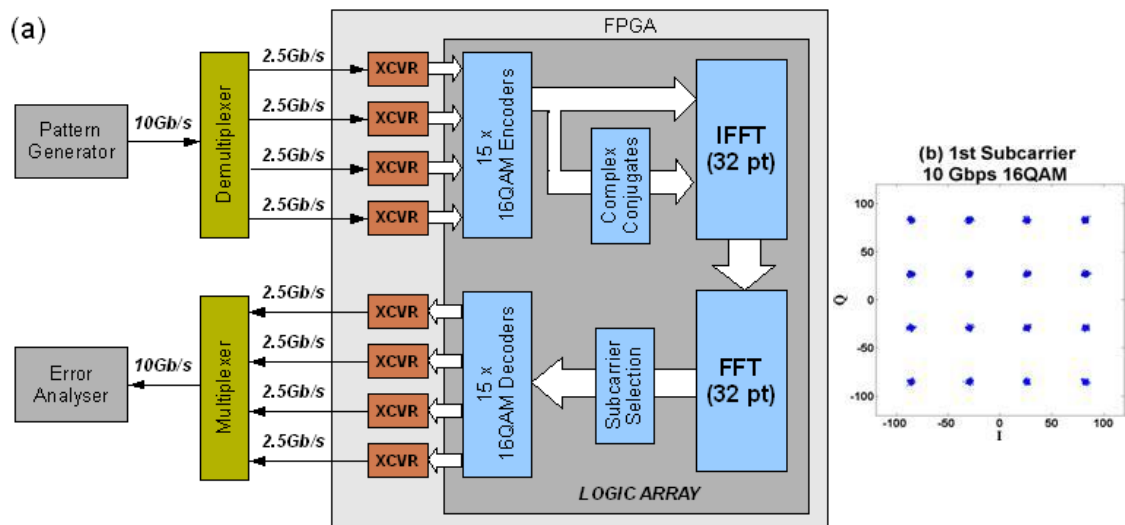
Fig. 3.15 (a) Experimental system for evaluating IFFT/FFT logic functions; (b) constellation of 16-QAM-encoded first subcarrier after FFT

To evaluate the operation of the IFFT and FFT designs in the FPGA both the IFFT and FFT DSP blocks are implemented in the same FPGA in a back-to-back configuration, as represented in Fig. 3.15 (a). Fig. 3.16 shows the corresponding Quartus II™ schematic diagram for the implemented design. 10Gb/s incoming data is generated externally from a BPG. This serial binary data stream is demultiplexed into four 2.5Gb/s streams for input to the FPGA via the four high-speed deserialising transceivers. 16 bit parallel data from each

transceiver combine to form a 64 bit parallel word, of which 60 bits (15x4 bits) are fed to 15 parallel 16-QAM encoders and the remaining 4 bits are simply passed directly through to one of the serialising output transceivers via a suitable delay (not shown in Fig. 3.15 (a) for simplicity). This approach is to avoid the need for a bus width conversion function and results in an IFFT/FFT data throughput of 9.375Gb/s. The 16-QAM encoders generate complex data for input to the IFFT logic function. The 15 encoded complex numbers and the zero-valued subcarrier 0 corresponding to zero frequency are mapped into 32 complex values such that they satisfy Hermitian symmetry according to the method described in section 2.3.3. This therefore results in the generation of 32 real-valued time domain samples at the output of the IFFT to be compatible with the generation of real-valued signals required in IMDD systems.

These 32 12-bit signed samples from the IFFT function forming an OFDM symbol are clipped to a range of ±1000 and quantised to 8-bits within the IFFT block. The 32 samples are then fed directly to the input of the FFT function. From the output of the FFT, the 15 data-carrying subcarriers in the positive frequency bins are selected, which are then decoded by 15 parallel 16-QAM decoders. The resulting 60 bit parallel data is combined with the aforementioned delayed 4 bits and then fed to four high-speed 16 bit serialising transceivers operating at 2.5Gb/s output. The four data streams are multiplexed to a single 10Gb/s data stream, as previously described in section 3.4.2, and BER is measured with an error analyser. The FPGA runs at a clock speed of 156.26MHz, which is equal to the symbol rate, as discussed in section 3.3.5. It should be noted that the components, test equipment, data interface configuration and the system clocking are closely based on the system architecture described in sections 3.4.1 and 3.4.2 with the modification made for operation with a single FPGA.

Zero bit errors are detected by the error analyser at 10Gb/s operation. The constellation of the first subcarrier at the FFT output is shown in Fig. 3.15(b) and is typical of all subcarriers. This result validates the operation of the IFFT and FFT logic functions in the FPGA and clearly shows that the real-time DSP is capable of supporting at least 9.375Gb/s IMDD-based OOFDM transmission. If CO-OFDM transmission is considered, where both positive and negative subcarrier frequencies can carry independent data, the supported bit rates is doubled to 18.75Gb/s. It is also estimated that, the use of higher modulation formats, higher clock speeds and more subcarriers can allow the developed IFFT/FFT

algorithms to operate at throughputs in excess of 40Gb/s. This DSP performance estimation is highly significant as it indicates that, in terms of electrical components, the limiting factor for OOFDM transceiver bit rate is not the DSP performance but the DAC and ADC technology which must offer high performance at sufficiently high sample rates.
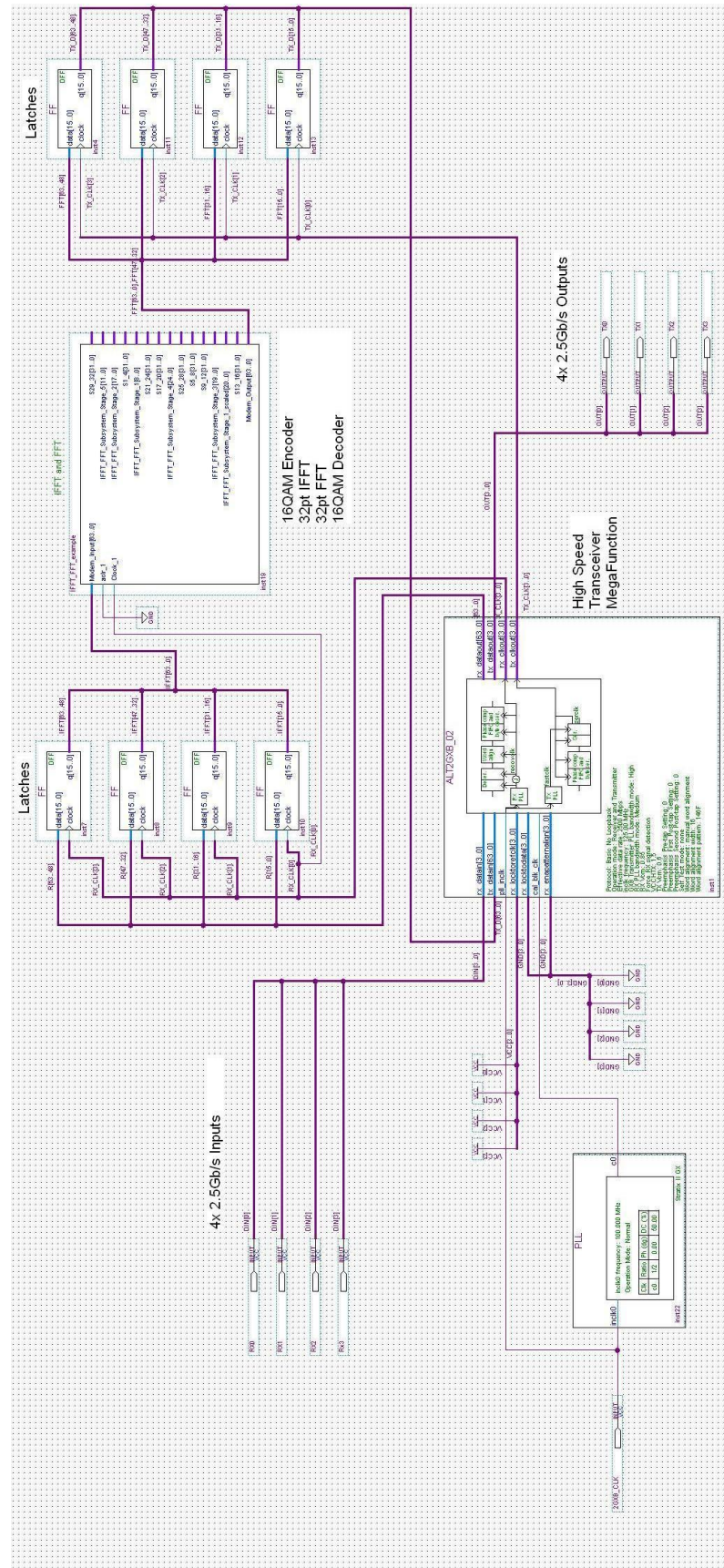
Fig. 3.16 Quartus II Design for IFFT/FFT Back-to-Back Testing

3.5.3 Transmitter DSP Architecture

Fig. 3.17 shows the top level Quartus II™ schematic diagram of the transmitter's FPGA logic design. Each block in the design is denoted with a letter for referencing the blocks in the following architecture description. The reference clock input connects via a PLL, block A, which reduces jitter on the incoming clock signal without changing the clock frequency. The output from the PLL is the master system clock and is distributed to all other blocks.

The logic design adopts a highly parallel processing architecture such that each functional block processes all frequency domain subcarriers and time domain samples of one symbol in parallel. The adopted FPGA master clock frequency is therefore equivalent to the OOFDM symbol rate. To meet the required throughput a function employs operation pipelining as necessary, this will increase the function's latency but throughput is maintained at the symbol rate. This approach results in an acceptable value for the FPGA clock frequency in the order of a few 100's of MHz. The maximum clock frequency typically being 300-400MHz. At the maximum system sample rate of 4GS/s the symbol rate is 100MHz therefore the system clock is also 100MHz. To reduce logic resources an architecture could be developed where the parallel data set employed is a partial symbol, however additional circuitry is required to manipulate and store the intermediate partial symbol values required to build up a complete symbol. Reducing the size of the parallel data set also requires a corresponding increase in the FPGA clock frequency to maintain the required symbol throughput. The adopted architecture of the implemented IFFT/FFT simultaneously process all time domain and frequency domain coefficients therefore adopting this approach for all functional blocks was chosen as the resulting architecture has lower complexity although not necessarily the optimum logic usage. Although logic optimisation is an essential design step for this initial research logic optimisation is not a priority.

3.5.3.1 Operating Modes

The transmitter logic can operate in three different modes:

- Mode 1: Generates a synchronised and identical 10-bit training pattern on each of the 32 LVDS outputs at the DAC interface for the purpose of ADC interface synchronisation in the receiver.

- Mode 2: Generates a predefined synchronisation signal that repeats every symbol period and is used for initial symbol alignment in the receiver using a manual synchronisation method.

- Mode 3: Generates the OFDM signal using internal test data generation.

Two push buttons on the FPGA board control the mode selection by setting the select inputs of the 2x320 bit multiplexer, block G, and the 2x256 multiplexer, block C as shown in table 3.3. LEDs are used to indicate the state of the multiplexer select inputs.

Table 3.3. *Transmitter Mode Selection*

Block C select	Block G select	Mode
1	X	1: Training pattern generation
0	0	2: Symbol synchronisation pattern
0	1	3: OFDM signal generation

The 32 LVDS outputs, denoted R, on the right-hand side of Fig. 3.17 are the DAC interface signals. These signals interface via the previously described ALTLVDS function, block H. The ALTLVDS function must be configured for the required interface clock frequency, $r_s/4$ Hz. At the maximum sample rate of 4GS/s the interface is configured for 1GHz operation. The 10:1 serialisers of the ALTLVDS function are fed by 320-bit wide parallel data every clock cycle, the data source depending on the selected operating mode.
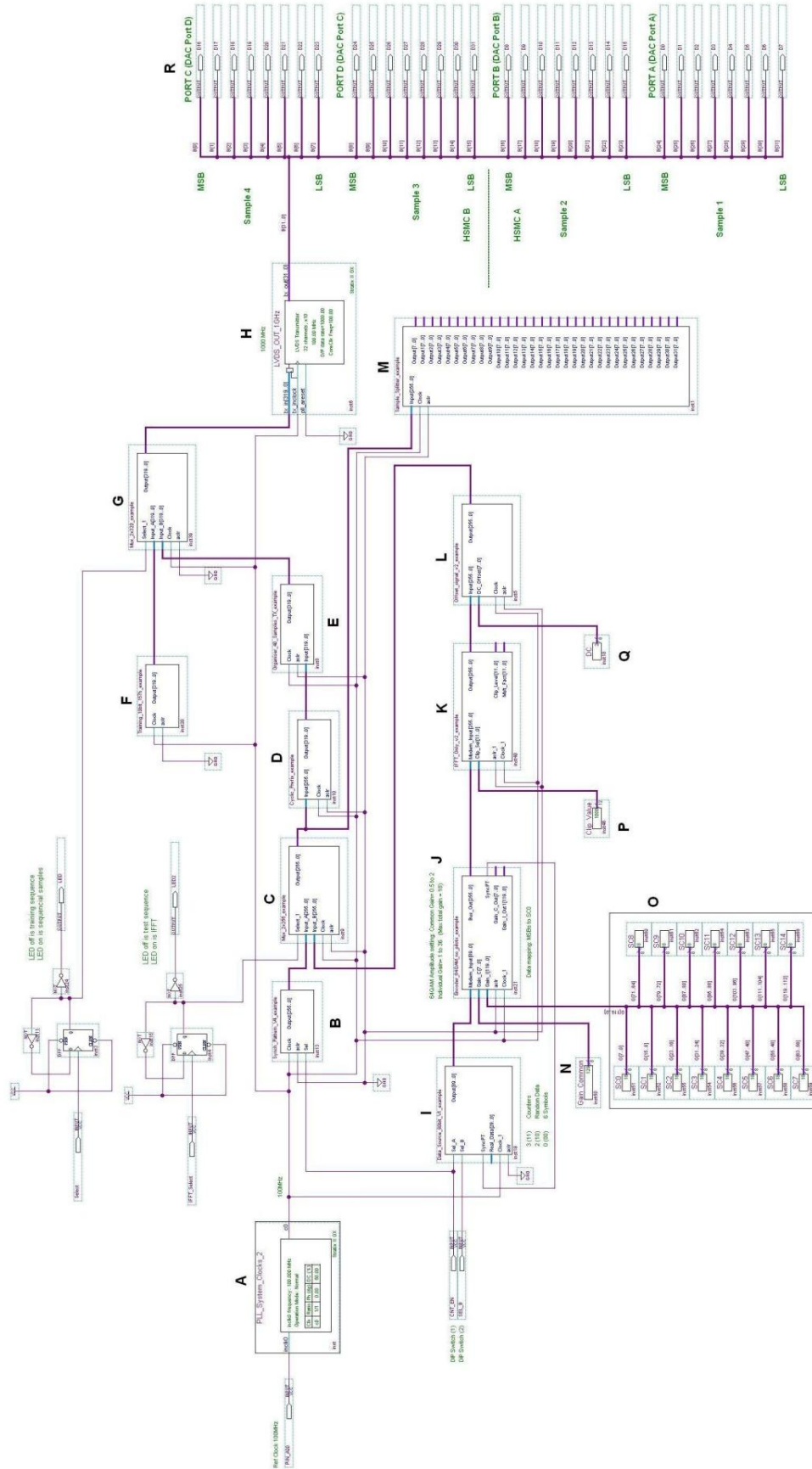
Fig. 3.17 Real-Time OOFDM Transmitter DSP Architecture

3.5.3.2 Training Sequence Generation

The training sequence is required for synchronisation of the 32 deserialisers in the receiver's ALTLVDS function which interfaces to the ADC. To generate the training sequence at the DAC interface, mode 1 is selected to connect the 32x 10-bit fixed training data from block F to the input of the ALTLVDS function. The training sequence block applies fixed 10-bit data of 157 Hex to each of the ALTLVDS 10:1 serialisers.

The training pattern is selected such that it contains no repeat patterns and the 10-bit word can be identified within a repeated serial sequence. All 32 LVDS outputs will therefore transmit the same repeating 10-bit synchronised training sequence. The receiver FPGA can then align the deserialisers in its ALTLVDS function, the alignment procedure is described to section 3.5.4.1.

3.5.3.3 Synchronisation Signal Generation

The synchronisation signal is required for initial symbol alignment in the OOFDM receiver. To generate the synchronisation signal, mode 2 is selected to connect the fixed 32-sample synchronisation pattern from block B to the DAC interface via blocks D and E. The synchronisation pattern is set to produce a positive and negative pulse over the full 8-bit DAC range by setting the nth sample value $s(n)$ as defined in Eq.(3.1) where n=1 to 32.

$$s(n) = \begin{cases} 255, & n = 1,2,3,4,5 \\ 127, & n = 6,7,..,11,12 \\ 0, & n = 13,14,15,16,17 \\ 127, & n = 18,19,...,31,32 \end{cases} \qquad (3.1)$$

Block D adds an 8-sample cyclic prefix to the 32-samples selected by the multiplexer block C, which is either the synchronisation pattern or the OFDM signal. The cyclic prefix block contains no logic and simply maps 32 input samples to 40 output samples according to the cyclic prefix generation method defined in section 2.3.4. Cyclic prefix is only required when the OFDM signal is selected, however when the synchronisation signal is selected block D inserts eight samples of 127 at the start of the signal which simply extends the spacing between pulses. The resultant digital waveform is illustrated in Fig. 3.18 (a). The start of the first positive pulse indicates the start of the IFFT window. The corresponding output waveform from the DAC when generating the synchronisation

signal is shown in Fig. 3.18 (b) where the cursors indicate a 10ns symbol period with the start aligned to the IFFT window.
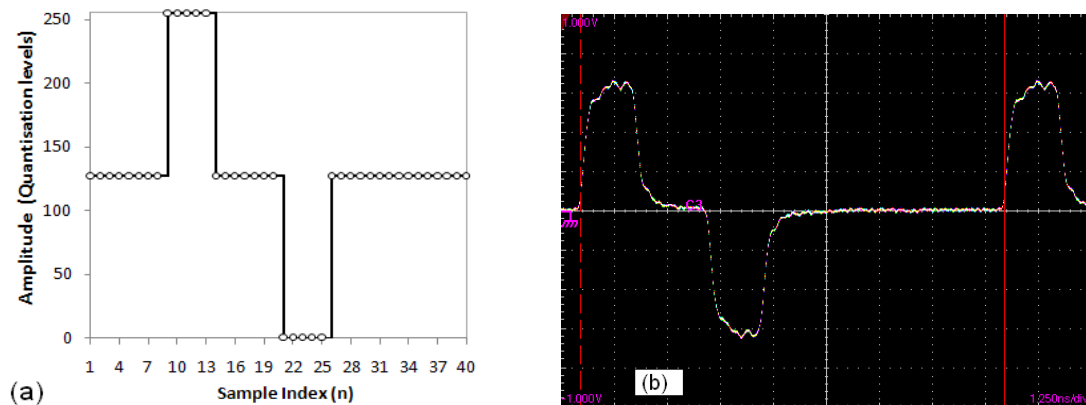

Fig. 3.18 Synchronisation Signal (a) Digital Samples (b) Analogue signal at DAC output

The receiver symbol alignment method employing the synchronisation symbol is described in section 3.5.4.3.

It is worth noting here that the samples at the multiplexer output, block C, are also fed to a separate block, denoted M, which contains no logic and simply provides all 32-samples as block outputs. This is used so that the Signal Tap II™ logic analyser can be configured to probe the samples at this block which remains unchanged. Samples can be probed at other functional blocks however any changes to the blocks can require the Signal Tap II signals to be redefined. Examination of the generated samples with the Signal Tap II™ embedded logic analyser aids in the verification of the design.

After the cyclic prefix is added in block D, the 40 samples are ready for transfer to the DAC for conversion to analogue signals, the Sample Organiser function, block E, performs the task of correctly organising the samples and the sample bits for input to the ALTLVDS serialisers so that the data is correctly presented on the DAC interface. Fig. 3.19 (a,b) and Fig. 3.20 shows various levels of the Simulink model for block D. Fig. 3.20 (a) is the top level, the first block on the left-hand side separates the 320-bit bus to 40×8-bit samples, the ALTLVDS Driver block on the right-hand side, performs the mapping function and is shown in Fig. 3.20 (b). Here 4 ALTLVDS Bit Mapper blocks provide the interface to each of the 4 DAC ports. Sample mapping is first performed to feed the correct samples to the ALTLVDS Bit Mappers. There are 4 parallel DAC ports, 1 to 4, which must be supplied with 4 consecutive samples. Each ALTLVDS Bit Mapper thus requires samples spaced at

4 sample intervals, the samples fed to the bit mapper feeding port p are therefore the $[p+(4 \cdot n)]$th samples where p=1 to 4 and n=0 to 9. The ALTLVDS Bit Mapper blocks, shown in Fig. 3.20, correctly map the sample bits to the interface bits. The 10×8-bit samples fed to each bit mapper are converted to 8x 10-bit words, where each 10-bit word
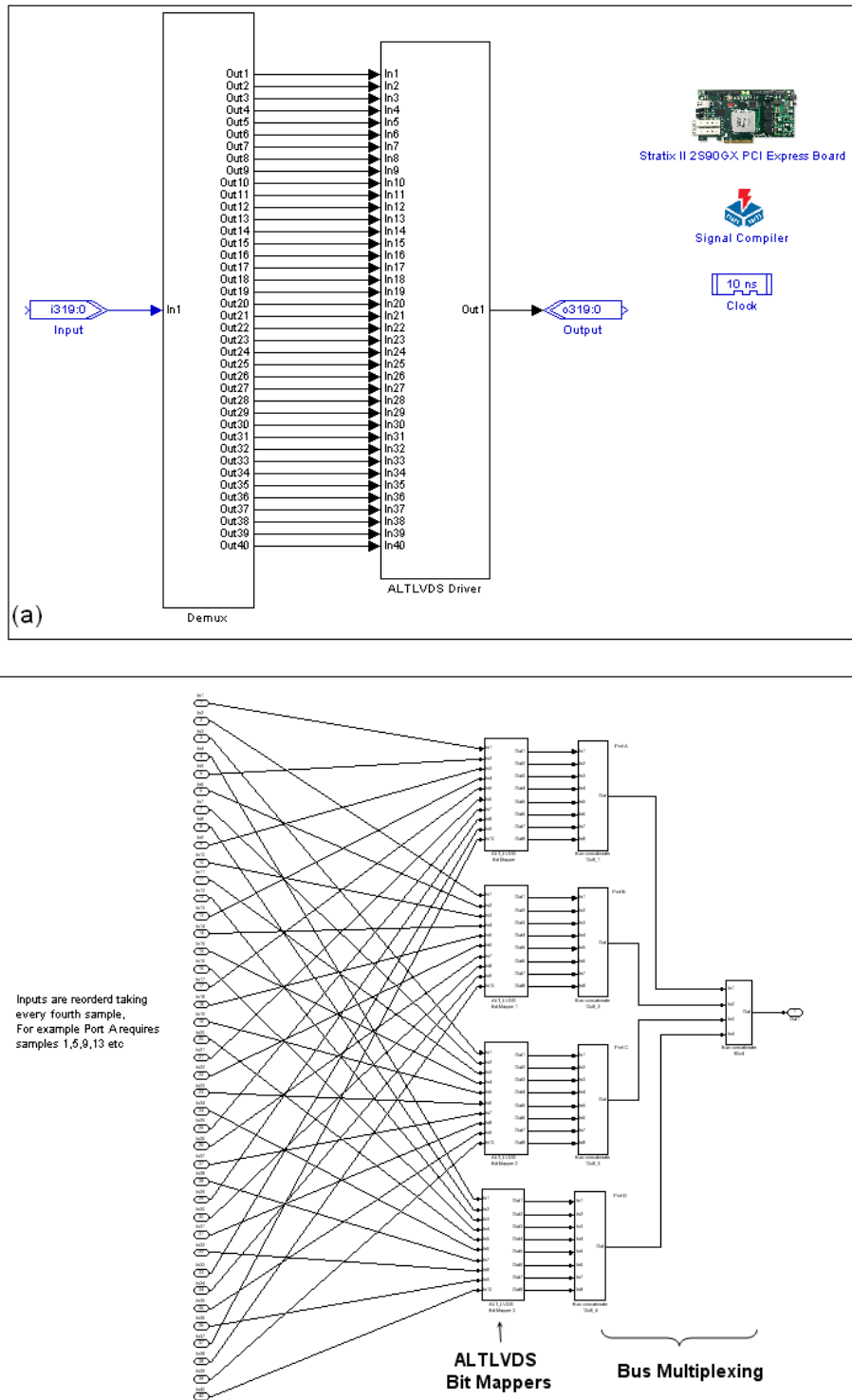

Fig. 3.19 Sample Organiser (a) Top Level Schematic, (b) ALTLVDS Driver Block
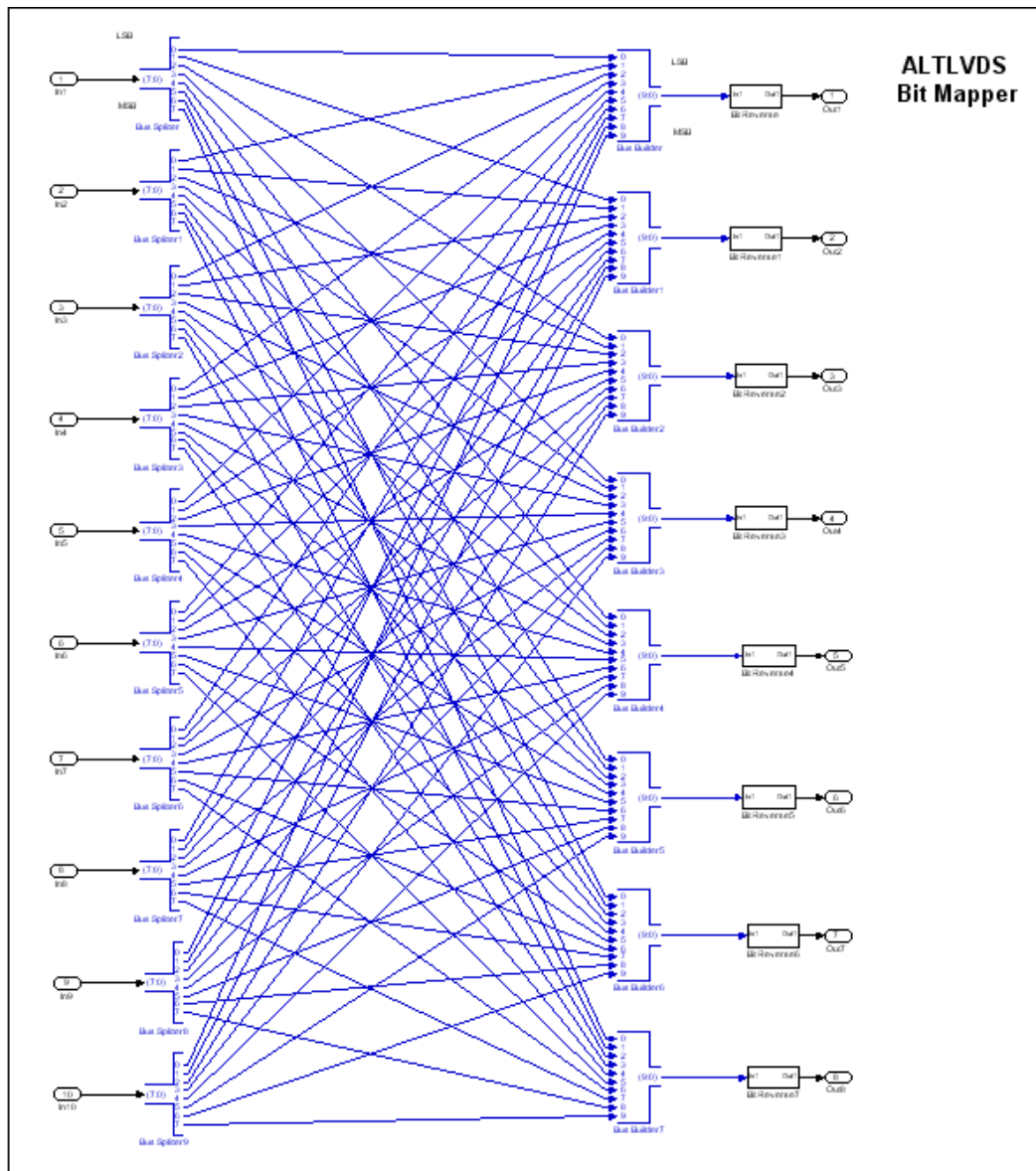
Fig. 3.20 Sample Organiser, ALTLVDS Bit Mapper

contains the bits from the same bit location in each input sample. For example the first 10-bit word consists of all the 1st bits from samples 1 to 10, more generally the nth 10-bit word consists of all the nth bits from input samples 1 to 10. The 4 ALTLVDS bit mapper blocks thus generate 32×10-bit words for input to the 32 10:1 serialisers in the ALTLVDS function described in section 3.4.1. The digital samples will thus be correctly transferred to the DAC inputs ports.

3.5.3.4. OFDM Signal Generation

When OFDM signal generation mode 3 is selected, the blocks involved in generating the IFFT symbol portion of the OFDM signal are i) Data Generation, block I, ii) Data Encoding, block J, iii) *IFFT* including signal clipping and quantisation, block K and iv) Signed to Unsigned Conversion, block L.
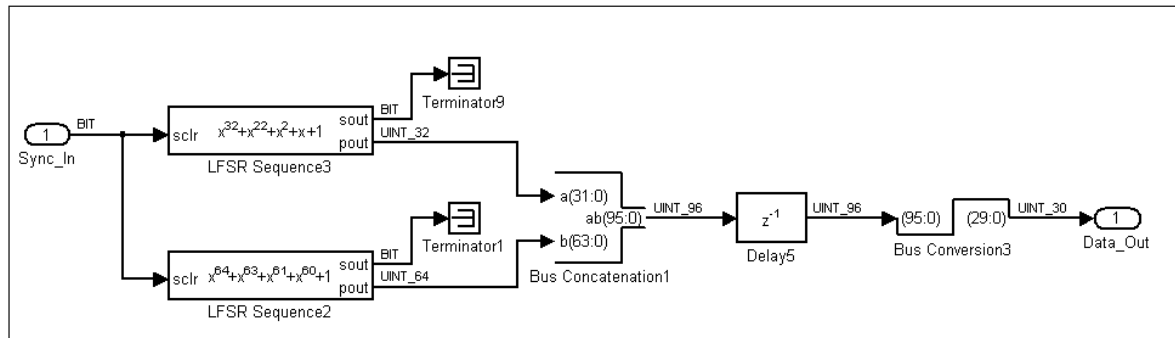

Fig. 3.21 Data Source

Data generation is performed internally to the FPGA in preference to employing the external data input as this allows individual subcarrier BERs to be analysed in the receiver FPGA, in addition to measuring the total system BER. Using an external BPG and BEA only allows total system BER to be measured. Total errors and individual subcarrier errors are counted in the receiver by generating an identical test pattern, synchronising it to the received data sequence and continuously counting bit errors over a predefined number of bits. Fig. 3.21 shows the Simulink schematic diagram of the data generation block. Two pseudo random bit sequence (PRBS) generators are employed of length 32 and 64 bits which are configured with feedback taps to generate PRBS sequence lengths of 2^{32}-1 and 2^{64}-1 respectively. The parallel outputs from each PRBS generator are concatenated to form a 96 bit parallel output. The appropriate number of LSBs are then selected from the 96 bit word according to the required number of bits per OFDM symbol. In Fig. 3.21, for example, the 30 LSBs are selected to provide 2 bits per subcarrier. The number of LSBs required is set as a Simulink™ block parameter so that it can be simply edited to modify the output data width of the model to match the desired data width. As the parallel output data from the PRBS generators are used the effective serial transmitted bit sequence will not be a conventional PRBS sequence, this is because it is not possible to generate conventional serial PRBS sequences at the required bit rate due to the limited FPGA clock speed.

The data generator shown in Fig. 3.21 shows an external 'Synch_In' input signal which is used to synchronously reset both PRBS generators to an initial register value of F0F0F0F0 Hex. This is used with the pilot subcarrier insertion function so that the data sequence can be synchronised with the pilot subcarriers start label. This then allows the corresponding data sequence generator in the receiver to be synchronised with the received data via the pilot subcarrier label. A description of channel estimation through the use of pilot subcarriers is given in chapter 5. For the initial real-time OOFDM transceiver, as DQPSK modulation was employed, channel estimation was not required therefore the 'Sync_In' signal was not used for the initial design and the PRBS generators were free running.

As stated above, in the initial real-time OOFDM transceiver design DQPSK modulation is selected. The reason for this is to avoid the need for the added complexity of channel estimation and equalisation in the initial design. As DQPSK modulation is based on subcarrier phase changes between successive symbols the change in absolute subcarrier phase due to the channel response is immaterial for DQPSK. Subsequent designs employ QAM modulation for which channel estimation and equalisation is essential as the absolute subcarrier phase carries information. The full model of the data encoding block employing 16 QAM is described here. Further modifications to this block implemented in subsequent designs are described in the appropriate chapters. The top level Simulink™ model schematic is shown in Fig. 3.22 (a). The subsystem "16QAM_TOP" contains the lower layers of the encoding function and has two inputs: the 56-bit wide "Modem_Input" which is fed from the data generation block and "Amp" which controls the peak amplitude of all subcarriers. To allow adjustment of the subcarrier amplitudes during operation one of 8 alternative amplitudes is set based on the setting of two external switches. The block "Amplitude Calc" uses a look up table (LUT) to select one of the 8 input values 21, 24, 27, 30, 33, 36, 39 and 42 based on the 2-bit input set by the switches, this is subsequently fed to the 16QAM_TOP block and used as a subcarrier multiplication factor at the encoders' outputs. The schematic of the 16QAM_TOP block is shown in Fig. 3.22 (b) on the left-hand side the 56-bit bus is split into 14×4-bit values which are fed into the pilot tone insertion block.
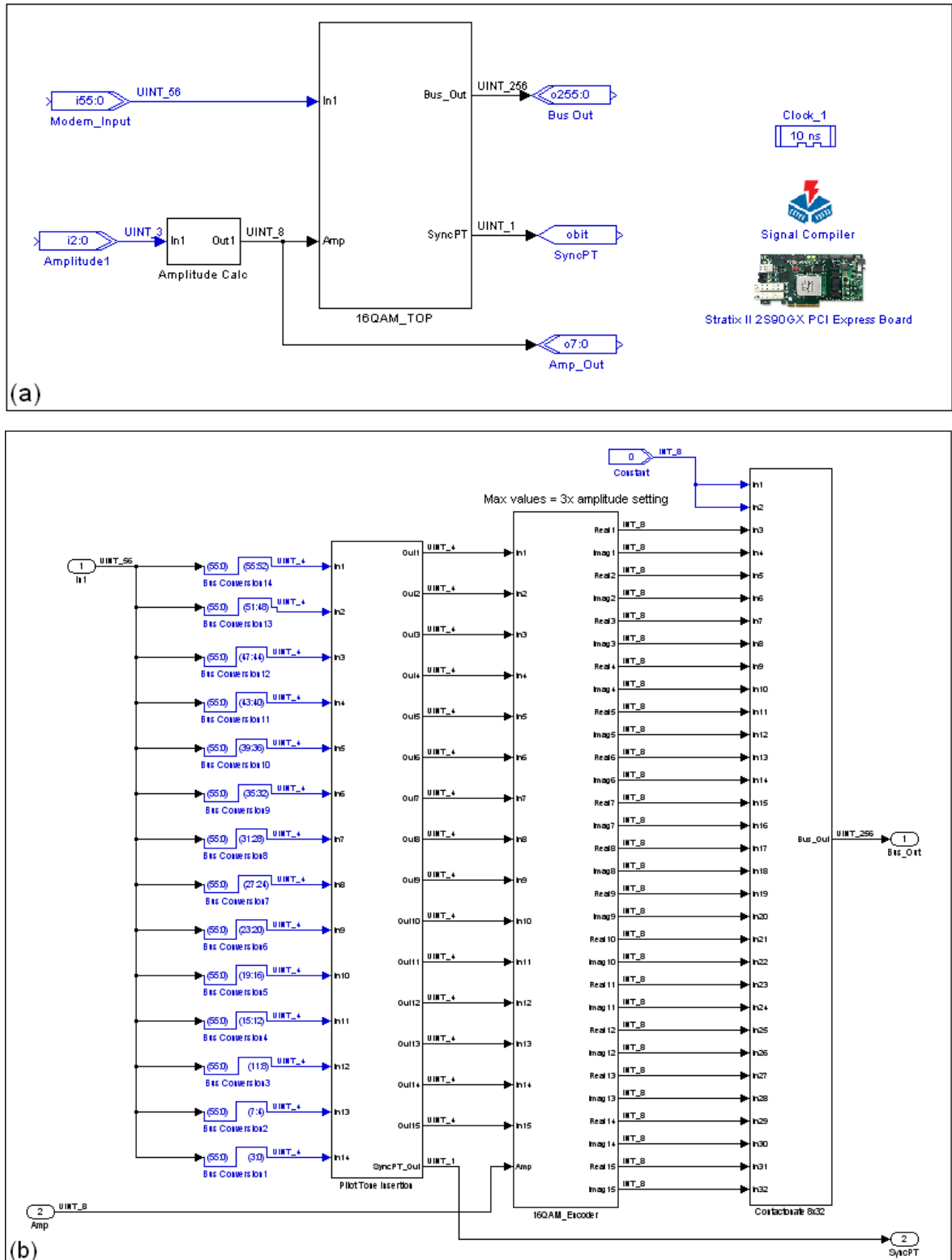
Fig. 3.22 16-QAM Encoding Function (a) Top level, (b) Data Bus Splitting, Pilot Insertion, Encoders and Bus Concatonation
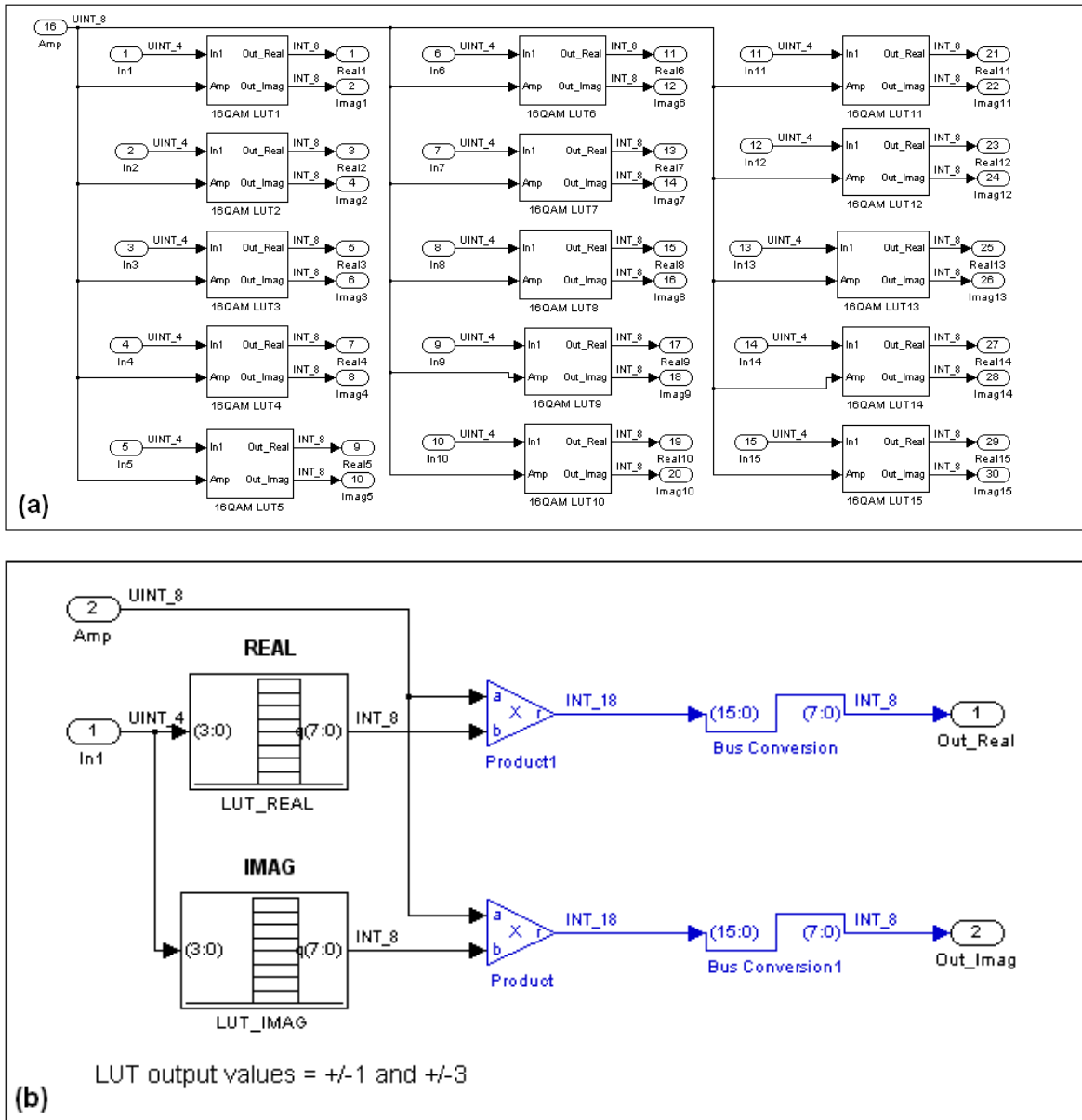
Fig. 3.23 16-QAM Encoding Function Cont. (a) 15x 16-QAM Encoders, (b) 16-QAM Encoder

The Pilot Tone Insertion block combines the test data with a 4-bit pilot data signal to generate 15×4-bit data values, thus providing the required total of 15 data values for encoding by the 16QAM_Encoder block onto the 15 subcarriers. The operation of the Pilot Tone Insertion block is explained in section 5.2.1.1. The 16QAM_Encoder block produces a complex value per subcarrier according to the 16QAM modulation scheme. The 15 complex values generated by the 16QAM_Encoder block are output as pairs of 8-bit real and imaginary values. After combination with two zero valued 8-bit values the 32 8-bit data values are concatenated into a 256-bit output bus. The two zero valued 8-bit values combined with the encoded data are required to provide the real and imaginary values for

the zero frequency subcarrier which must be set to zero amplitude. Fig. 3.23 (a) shows the schematic for the 16QAM_Encoder block which consists of 15 individual 16QAM encoders, labelled 16QAM LUT1-16QAM LUT15, the design of each encoder is as shown in Fig. 3.23 (b). The principle of the encoder design, also used for the design of higher modulation formats, is to use LUTs to map the input data to the corresponding encoded complex value. There are thus two LUTs, one for the real part and one for the imaginary part, both fed with the same 4-bit input data. The two LUTs generate a 16 QAM encoded signal with a real and imaginary constellation point spacing of 2, the extreme corners of the constellation pattern are therefore located at ±3, ±3. The generated real and imaginary values are then both multiplied by the aforementioned 1 of 8 possible multiplication factors. For example if the minimum (maximum) multiplication factor of 21 (42) is selected the real and imaginary values each have a minimum (maximum) peak values of ±63 (±126).
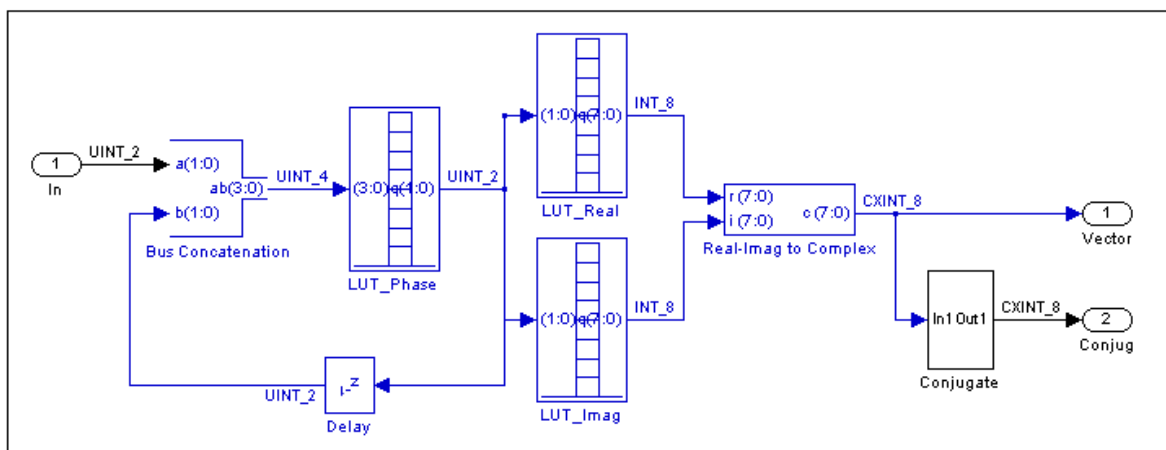
Fig. 3.24 Individual DQPSK Encoder

The design for the individual DQPSK encoder is shown in Fig. 3.24. Here the required subcarrier phase is first determined by a LUT with the output fed back to the input and combined with the data to be encoded. The real and imaginary parts of the complex subcarrier value are then generated from the phase value with LUTs as in the 16 QAM design. The encoded subcarrier amplitude for this case was fixed to give peak real and imaginary values at ±100.

In Fig. 3.17 there are memory cells shown connecting to the encoding block. These were added in subsequent designs to allow encoding parameter control via online memory content update. The memory cell denoted N controls a common gain factor for all subcarriers and the 15 memory cells denoted O control individual gain factors for each

subcarrier. The use of these parameters for design enhancements is fully described in sections 5.2 and 5.3.

The 32 complex outputs from the encoder block provide the inputs to the 32 point IFFT function, block K, which is implemented as described in section 3.5.2.1 and includes the clipping and quantisation block. The clipping value used to clip the signed 12-bit samples, before quantisation to 8-bits, was fixed in the Simulink™ design for the initial transmitter design at 1.5 Gb/s net bit rate. For the second transmitter design at 3Gb/s net bit rate the clipping value was selected from one of eight values by three external switches. For all subsequent designs the clipping value control was improved to give full control by employing an 11-bit unsigned value in embedded memory which could be updated to any possible value between 0 and 2047, this is shown in Fig. 3.17 as the memory cell denoted P connecting to the IFFT block.

The outputs from the IFFT block are signed 8-bit values. As the DAC requires unsigned 8-bit values block L converts the signed values to unsigned values by adding 128 to each sample and selecting the 8 LSBs to remove the sign bit. In a subsequent design this block was modified to add an alternating low-level DC offset to the symbol for the purpose of symbol synchronisation. The proposed symbol synchronisation technique and the modification to block L, is fully described in chapter 8. Fig. 3.3 shows a memory cell, denoted Q, connected to block L this is the DC offset value employed in the symbol synchronisation transmitter design which can be adjusted and optimised during operation.

3.5.4. Receiver DSP Architecture

Fig. 3.25 shows the top level Quartus II™ schematic diagram of the receiver's FPGA logic design. Each block in the design is again denoted with a letter for referencing the blocks in the following architecture description. As in the case of the transmitter the reference clock input connects via a PLL, block A, to provide the master system clock for distribution to all other blocks. The same parallel architecture used in the transmitter is also adopted in the receiver such that a whole symbol is processed concurrently and the FPGA master clock is equal to the symbol rate.

3.5.4.1 ADC Interface and Interface Synchronisation

The ADC interface in the receiver essentially performs the reverse operation of the DAC interface in the transmitter. The 32 LVDS inputs, shown on the left in Fig. 3.25, interface to the 4x 8-bit output ports on the ADC and interface via the 2 16-bit ALTLVDS functional blocks C1 and C2. The ALTLVDS blocks perform 1:10 deserialisation on each input to generate 320-bit parallel data corresponding in length to one symbol. The 320-bits are reorganised in the Sample Organiser, block F, to reconstruct the corresponding 40×8-bit samples. The operation of block F is the reverse of the sample organiser block H in the transmitter. The output of block F constitutes 40 consecutive 8-bit samples from the received OOFDM signal, these 40 samples are however arbitrarily aligned to the OOFDM symbol boundaries thus effectively constitute the received symbol with STO. These 40 samples can be referred to as the pre-alignment symbol. Block G is a bank of D-type flip flops added to act as a register for the Sample Organiser output.

The 10:1 deserialisers in the ALTLVDS block do not have the same latency after power up so synchronisation is required to ensure all the serialisers operate with the same delay. This is achieved by configuring the system in a digital back-to-back configuration and transmitting the training pattern at the transmitter FPGA as described in section 3.5.3.2. The Word Aligner, block D, operates by sending pulses to the 32 rx_channel_data_align inputs of the ALTLVDS functions, shifting the associated deserialised data until the required pattern is detected in the parallel data output. All deserialisers will then be aligned with the same delay.
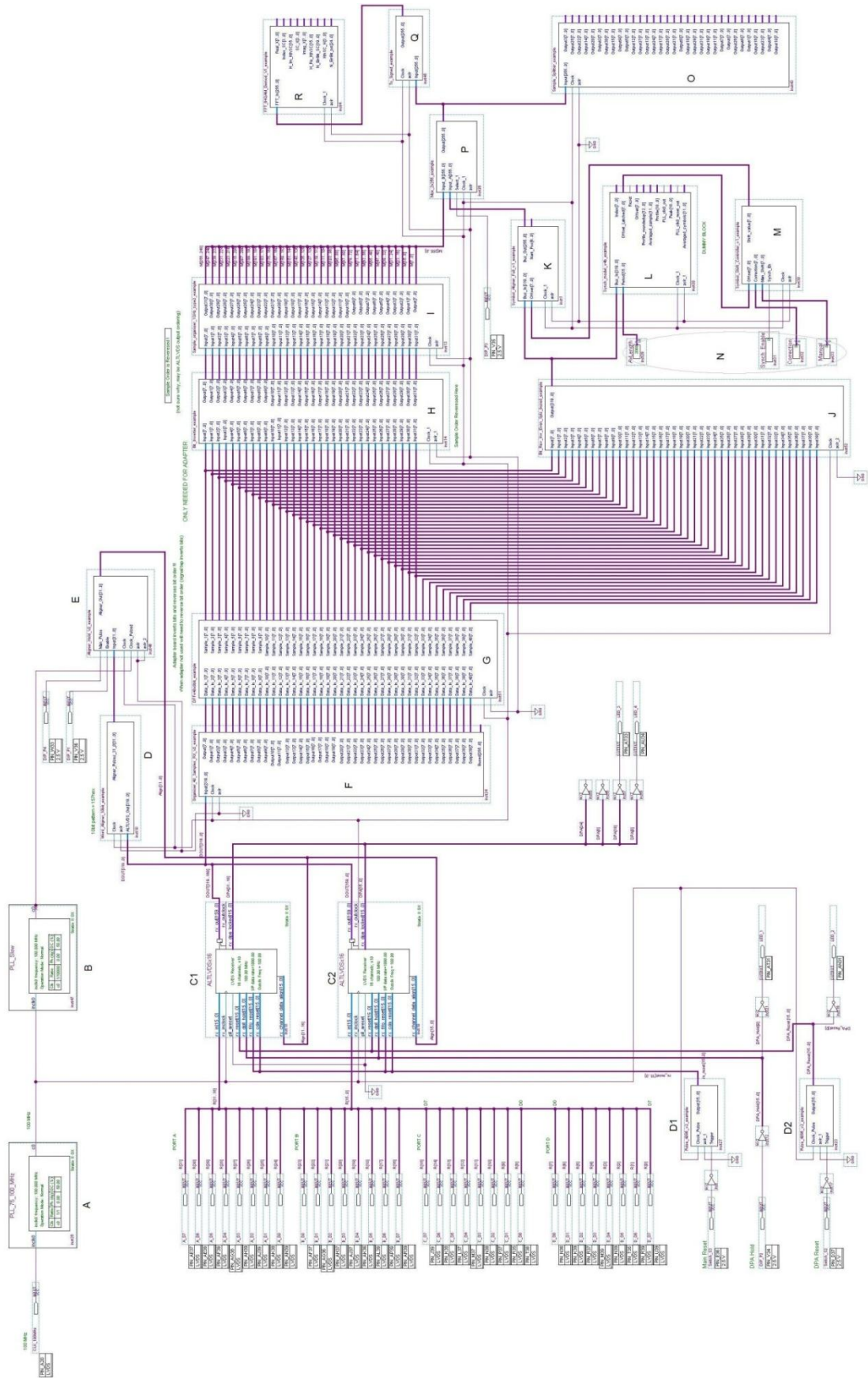
Fig. 3.25 Real-Time OOFDM Receiver DSP Architecture

The alignment pulses generated by the Word Aligner pass via the Aligner Hold function, block E, which performs two basic functions: i) An external switch setting allows the pulses to pass through during interface alignment and blocks the pulse during normal operation, ii) allows manual generation of alignment pulses via an external switch. This second function is used during symbol alignment as once the interface is synchronised applying alignment pulses to all 32 deserialisers simultaneously results in an increased time delay of $r_s/4$ as the interface is clocked at $r_s/4$. This delay corresponds to a time shift of 4 samples in the reconstructed 40 samples output from block F. This is used as a coarse adjustment for the manual symbol alignment procedure described in section 3.5.4.3.

3.5.4.2 Sample Manipulation for Different System Configurations

As discussed in section 3.4.2 the digital back-to-back configuration alters the bit locations at the receiver's ADC interface, this requires correction in the receiver and is performed by blocks H and I. Block H inverts all bits as the back-to-back connector arrangement used for the digital back-to-back configuration swaps over the differential LVDS pairs causing bit inversion. Block I corrects the sample reordering caused by the digital back-to-back configuration.

For all system configurations involving conversion of the digital OFDM signal to an analogue signal the signal samples are routed via block J which corrects for the fact that the bit locations on each ADC port are not identical and are arranged such that port A (C) is the mirror image of port B (D).

To select the digital back-to-back configuration or analogue configurations the two alternate signal paths are selected via a 2-port 256-bit multiplexer, block P, the select input being controlled by an external switch.

3.5.4.3 Symbol Alignment

Symbol alignment is a critical receiver function as correct IFFT window alignment is essential for data detection as described in section 2.3.8. A manual symbol alignment method can be adopted for initial experimentation due to the quasi-static nature of the optical channel. Symbol alignment must be performed at initial receiver set up and readjustment of symbol alignment is only needed when the alignment drifts sufficiently to

degrade BER performance. It is interesting to note here that it would typically take somewhere in the order of 10 minutes before any drift in symbol alignment could be detected and then BER would only increase slowly over time if alignment drift was not corrected.

To fully control symbol alignment, the coarse 4-sample adjustment, as described in section 3.5.4.1 is used in combination with the Symbol Aligner, block K. The Symbol Aligner can impose a further offset from 0 to 7 samples in one sample increments. The Symbol Aligner is implemented as an array of 32x 8-port 8-bit multiplexers. 32 multiplexers are required as the cyclic prefix is removed during the alignment process and each multiplexer output corresponds to one OFDM sample from the IFFT window. The top level Simulink™ model is shown in Fig. 3.26. The 320-bit input bus is split into 40 8-bit samples, the first 39 samples are passed to the Alignment subsystem and the 32 output samples then concatenated to a 256-bit output bus. The Alignment subsystem only requires 39 input samples as the 32 output samples can be shifted by a maximum offset of 7 samples. Fig. 3.27 and Fig. 3.28 show the structure and connectivity of the multiplexer array. The 8-port multiplexers are staggered along the incoming 39 samples to give the required relative offsets. Each multiplexer's select port is then driven by the same offset value to select the 1 of 8 possible inputs. The offset value driving the multiplexer's select inputs was originally derived from a modulo 7 counter clocked by an external switch to allow adjustment. Later designs employ an embedded memory cell to store the offset value. Both methods provide online adjustment of the symbol offset.
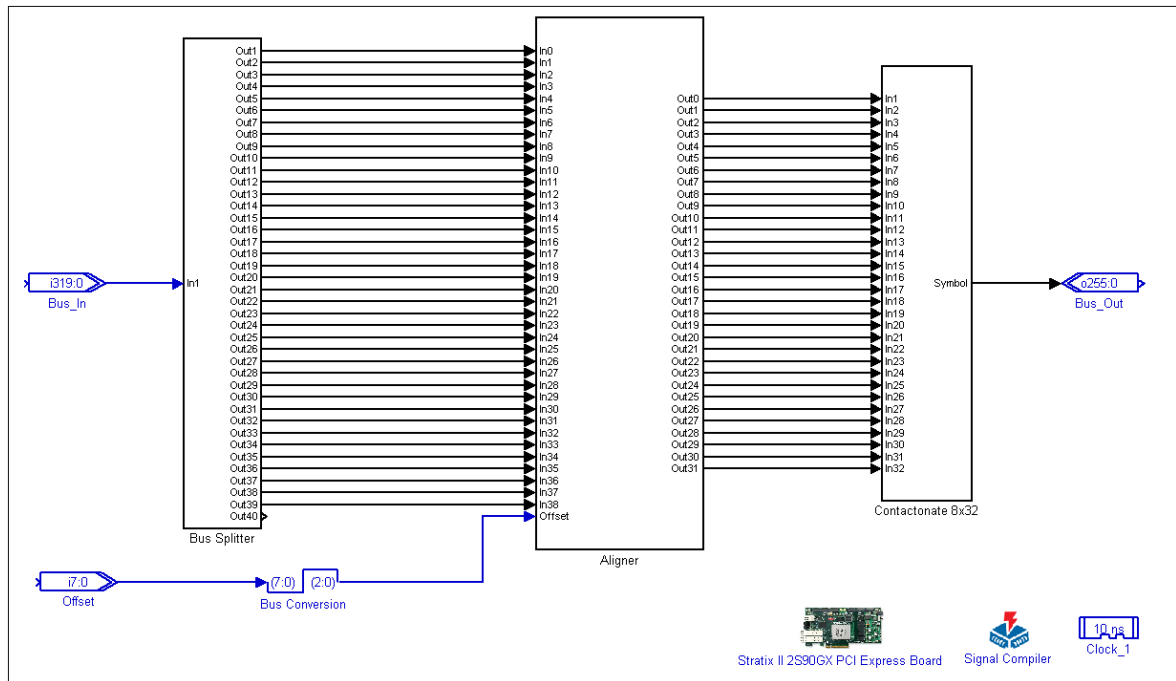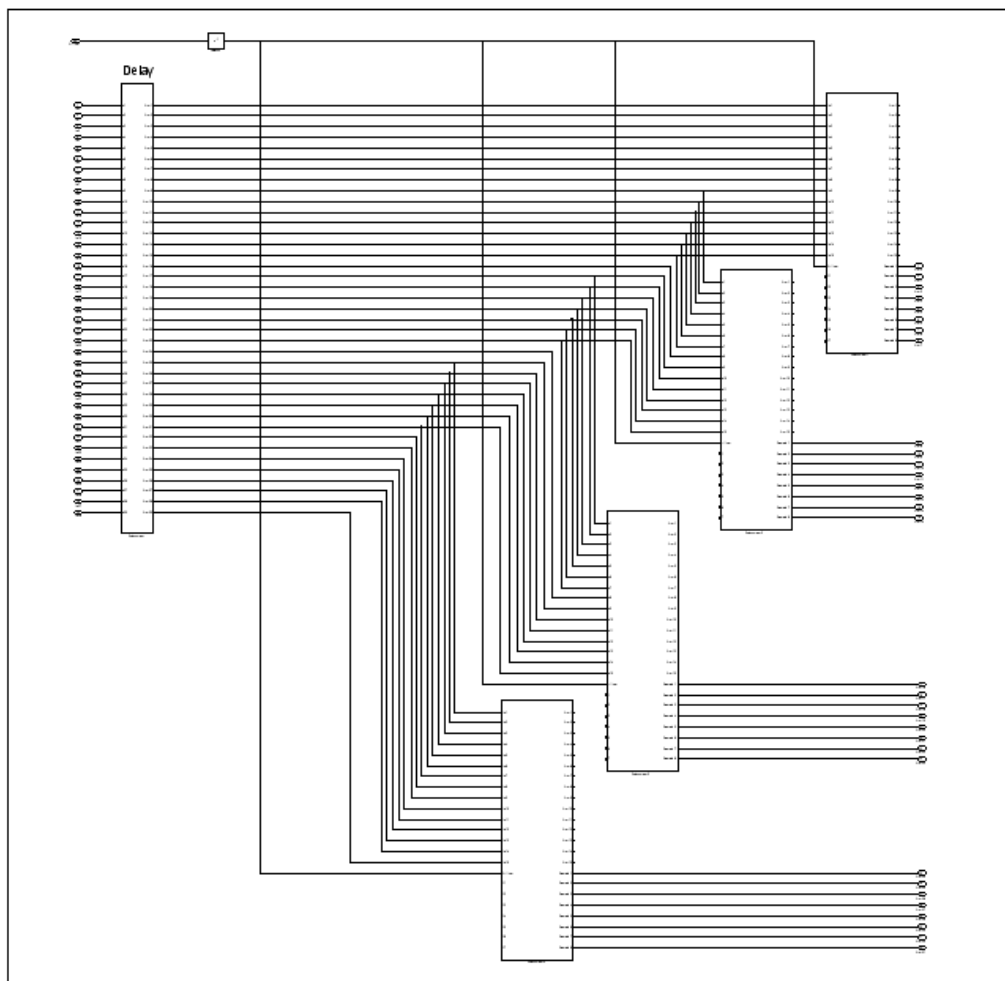
Fig. 3.26 Symbol Aligner Top Level

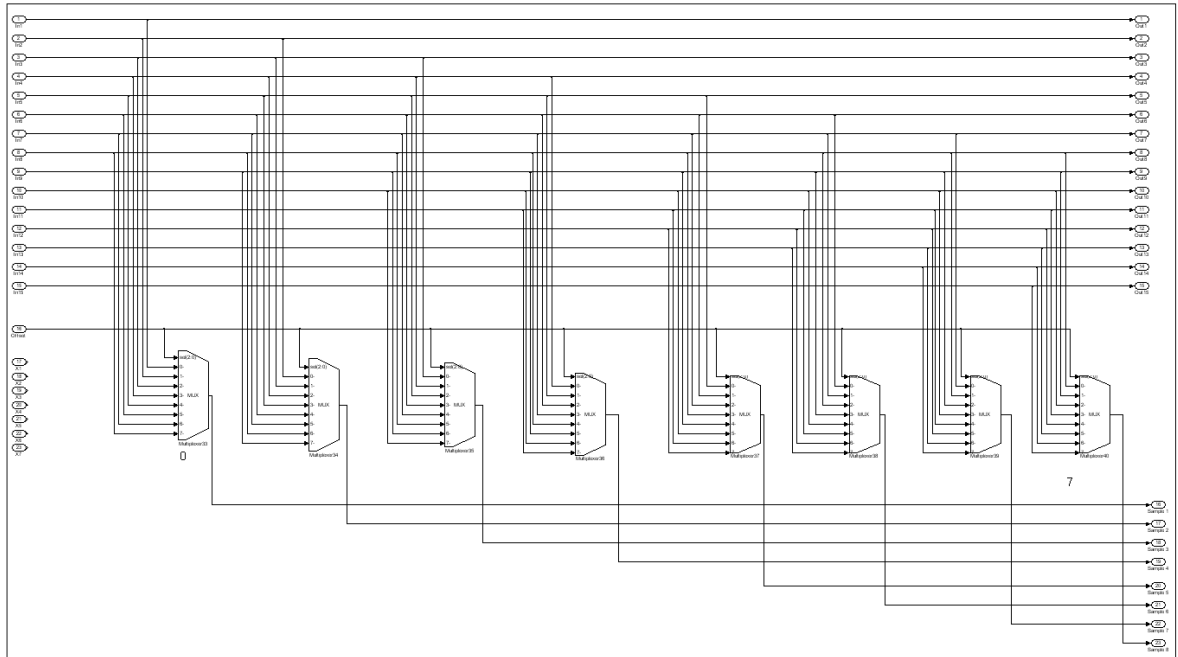Fig. 3.27 Aligner Subsystem in Symbol Aligner

Fig. 3.28 Multiplexer bank

To detect when symbol alignment is achieved the transmitter is configured to transmit the symbol alignment signal, as described in section 3.5.3.3. The realigned symbol is observed via the Sample Splitter, block O, which is a logic-free block used to provide stable probing points for the SignalTap II logic analyser. The realigned symbol can then be observed by extracting the sample values from Signal Tap II and exporting to MatLab for plotting. The symbol offset is adjusted until the leading edge of the first positive pulse of the synchronisation signal, which indicates the start of the IFFT symbol portion, is aligned to the first sample of the observed realigned symbol. It is also possible to verify that the correct symbol offset is selected when the system is operational by minimising the BER.

3.5.4.4 OFDM Signal Detection

All OFDM signal detection and error counting functions are implemented in a single OFDM Decoder block in the Quartus II™ design, block R in Fig. 3.25. This block was created as a complete model in Simulink™ to aid design verification before implementation in the FPGA. This single block is the key DSP element in the receiver design as it takes the received, aligned OFDM symbols and recovers the encoded data. The incorporation of the error counter function is for the sole purpose of system performance analysis and would not typically be incorporated in a commercial design as an external BER analyser would generally be employed for system testing.

The top level schematic for the OFDM Decoder is shown in Fig. 3.29. The incoming 256-bit data bus is expanded to 32×8-bit samples providing 32 consecutive samples from a symbol's IFFT window. These samples are directly fed to the 32 point FFT block which is implemented as described in section 3.5.2.1. It is should be noted that the Quartus II™ receiver design includes block Q before the OFDM Decoder block which converts the received unsigned samples to signed samples. This conversion removes the received samples DC component resulting from the ADC-generated half-scale offset. In theory a DC component at an FFT input will not affect the non-zero frequency coefficients, however to comply with the 8-bit signed input range of the FFT inputs the DC components must be removed.
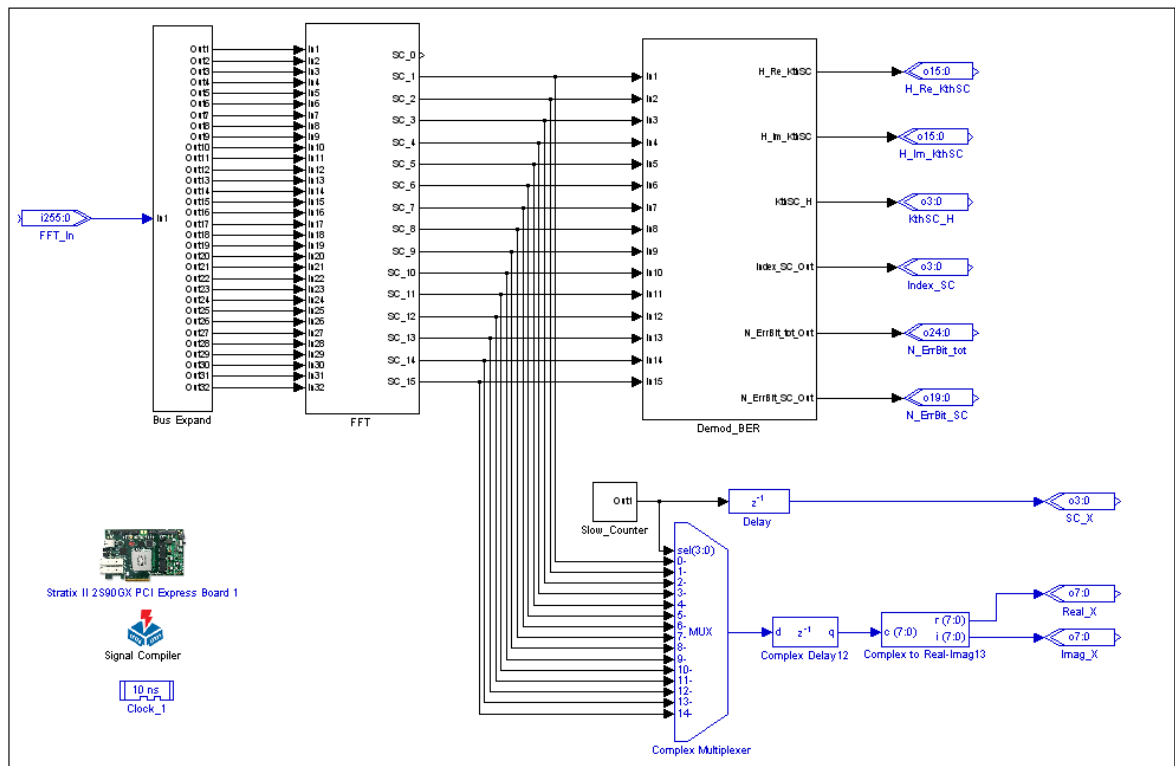
Fig. 3.29 OFDM Signal Detection Top Level

The FFT outputs the complex frequency coefficients for each of the received subcarriers, these are input to the Demodulation and BER block shown in Fig. 3.30. The received frequency domain subcarriers are also fed to the circuitry shown in the bottom right of Fig. 3.29 which employs a multiplexer and suitable counter to output the real and imaginary components of each subcarrier in turn. These values are accessed via SignalTap II™ and exported to MatLab in order to plot the individual subcarrier constellation diagrams. This ability to extract received subcarrier constellation diagrams from an

operational system is a vital feature used for instantly assessing system performance. This feature has also proven highly valuable during system debugging as irregular or distorted constellation diagrams are a clear indication of system malfunction.

Fig. 3.30 Demodulators and BER Analysis Block (Demod_BER)

The top level schematic of the Demodulation and BER block is shown in Fig. 3.30. This consists of four sub-blocks, a brief description of these blocks is first given with detailed descriptions following. From left to right these blocks are: i) Channel Estimation and Pilo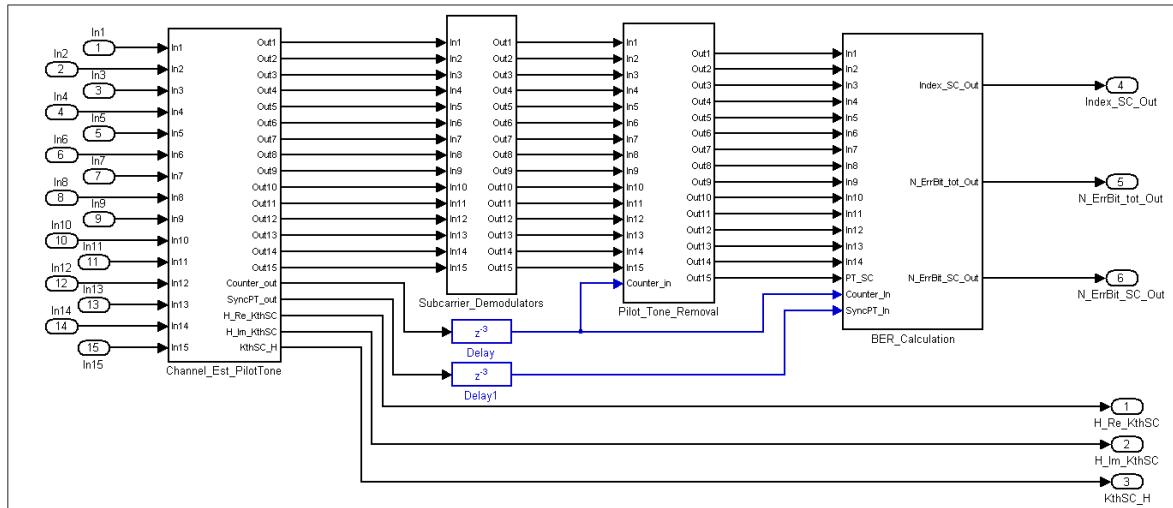t Tone Detection block which detects the pilot tone location, estimates the channel response and equalises each subcarrier. ii) Subcarrier Demodulators block which performs parallel decoding according to the employed modulation format on each subcarriers, iii) Pilot Tone Removal block which removes the pilot tone from the incoming data and iv) BER Calculation block which counts errors in order to allow BER to be determined.

The Channel Estimation and Pilot Tone Detection block and Pilot Tone Removal block were introduced to the enhanced designs employing 16-QAM modulation format or higher, these blocks are covered in chapter 5.

The design of the Subcarrier Demodulators block is dependent on the modulation format employed. The demodulator implementation described here is for 64-QAM, a similar design structure is employed in the 16-QAM and 32-QAM demodulators also implemented. The Subcarrier Demodulators block contains 15 instances of the 64-QAM demodulator shown in Fig. 3.31. The principle employed is to detect the nearest ideal constellation point to the received constellation point by comparing the real and imaginary

parts with threshold levels located equidistantly from constellation points, threshold levels are illustrated in the 16-QAM example in Fig. 2.7. The real and imaginary parts employ the same threshold levels which are located according to the incoming constellation size determined by the equalisation function. 64-QAM will require 7 thresholds for both the real and imaginary axis. Two comparator blocks, whose low level design is shown in Fig. 3.32, are used to separately detect the real and imaginary coordinates of the constellation point by comparison with all threshold levels. Summation of all comparator output bits gives 8 unique values corresponding to the detected constellation point location. The 3-bit outputs from the two comparator blocks are concatenated to give a 6-bit value where each of the 64 values corresponds to one of the 64 constellation point locations. To map the generated 6-bit value to the corresponding encoded data value a LUT is employed which is suitably configured for the required mapping function.
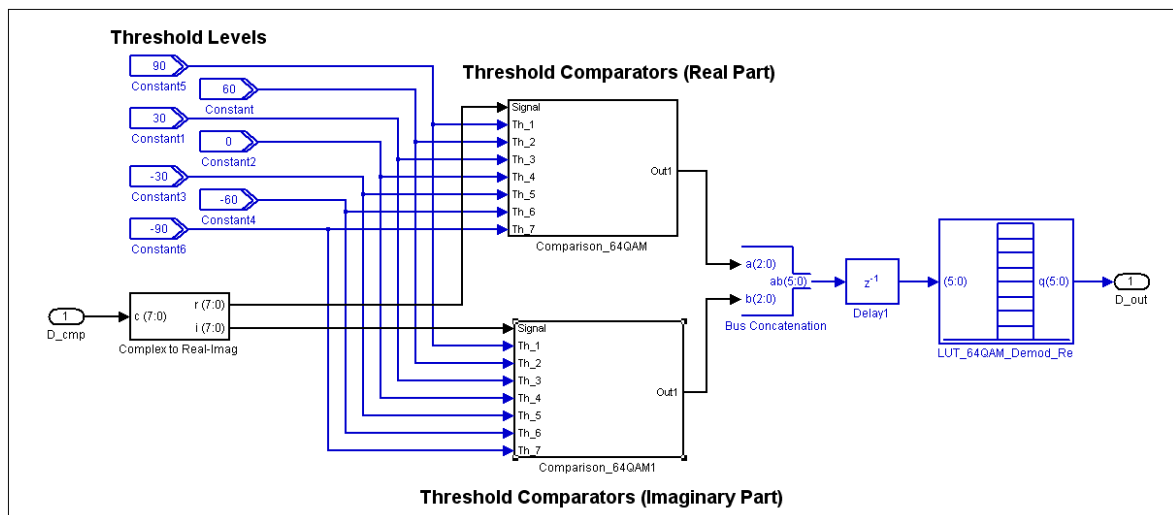
Fig. 3.31 64-QAM Demodulator

The BER Calculation block top level schematic is shown in Fig. 3.33. This design is the more advance design that counts errors on individual subcarriers. The initial implementation of this block only counted the total channel errors and was therefore a much simpler design. The block counts errors in a single subcarrier of every symbol over a period of 88,500 symbols. Thus to cycle through all subcarriers requires a period of $15 \times 88,500$ symbols. The multiplexer at the top of Fig. 3.33 selects the parallel data from a single received subcarrier. The select input for the multiplexer is incremented every 88,500 symbols to successively select each received subcarrier data in turn. To generate the test data for comparison with the received data, a test pattern generator block identical to that in the transmitter is used. The associated circuitry following the test pattern generator is

required to separate the data into 14 parallel streams corresponding to the subcarriers carrying test data and rearranges the data to account for the insertion of pilot subcarriers. It should be noted that although pilot subcarriers require a capacity of one subcarrier leaving a capacity of 14 subcarriers to carry test data, test data is still transported on all subcarriers due to pilot data successively occupying each subcarrier in turn, thus it is possible to determine the error count for all 15 subcarriers and therefore the BER performance of the complete channel. The test data generator is synchronised with the received data via a synchronisation signal generated by the Channel Estimation and Pilot Tone Detection block. The regenerated serialised symbol data and the received serialised symbol data, each 6-bits wide when 64-QAM is employed, are fed to the Error Counter block for error detection and counting.
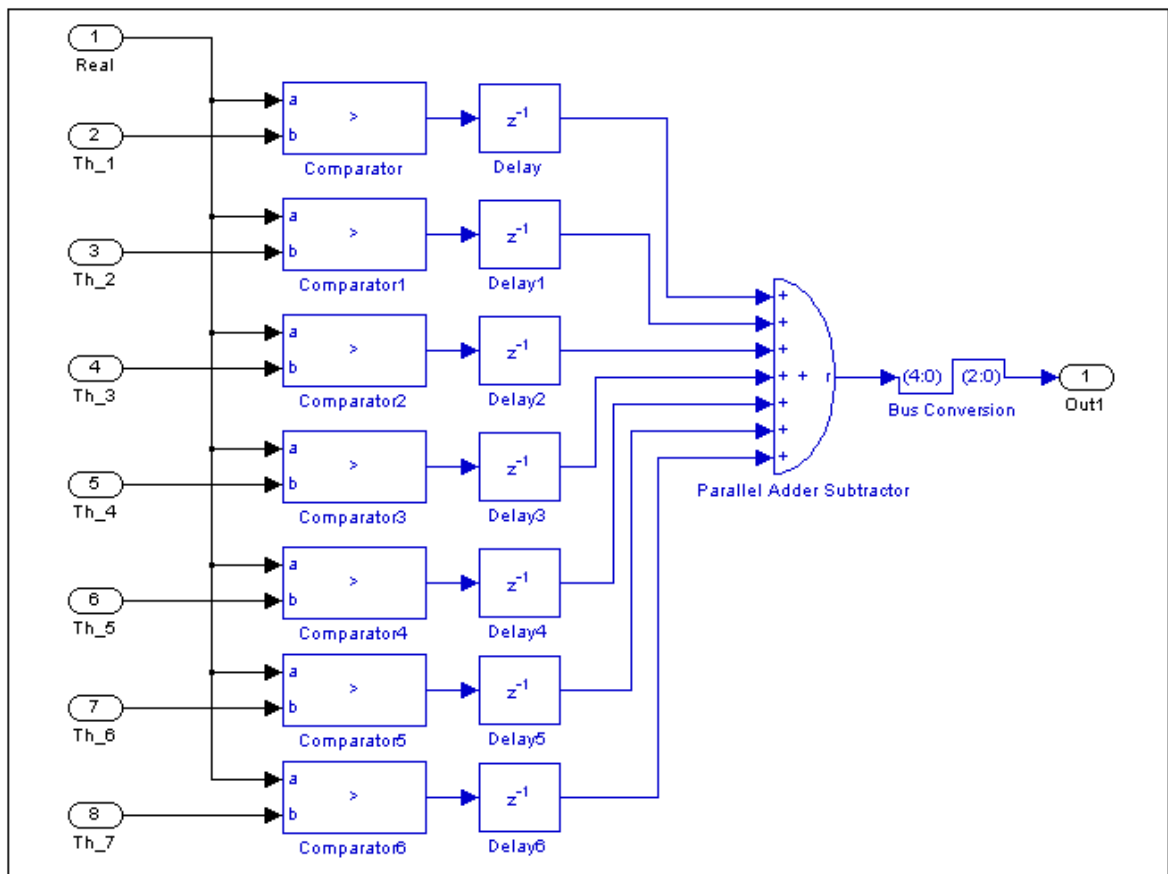
Fig. 3.32 Threshold Comparator Block
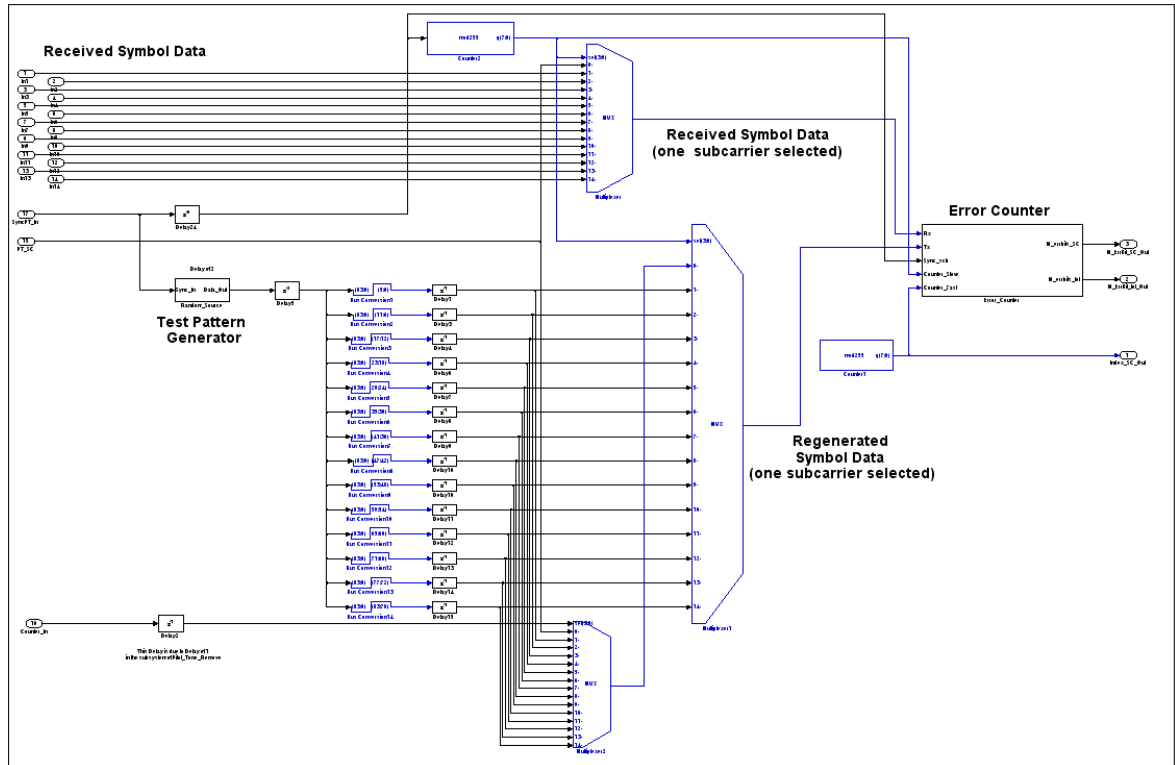
Fig. 3.33 BER_Calculation Block

The Error Counter block is shown in Fig. 3.34. In order generate error counts for individual subcarriers and the whole channel the principle adopted is as follows:

- The synchronisation signal, SynchPT, generated by the Channel Estimation and Pilot Tone Detection block and aligned to the test data sequence of length 88,500 symbols, is employed to increment a modulo 15 counter which acts as a subcarrier index counter. The counter output thus determines the subcarrier for which errors are counted. The counter is located in the BER Calculation block and is also used for selecting the appropriate inputs to the Error Counter block.

- The incoming 6-bit wide received data and regenerated test data are compared with a 6-bit XOR gate to detect any bit errors. The 6 error bits are subsequently summed to give the total errors for the associated subcarrier and symbol. An error count accumulator circuit accumulates the error count for the duration of the test data period.

- The SynchPT signal latches the accumulated total subcarrier error counts to a 15-port demultiplexer which acts as a storage element. The select input of the demultiplexer being fed by the subcarrier index counter. The SynchPT signal is also used to reset the error count accumulator.

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- The outputs from the 15-port demultiplexer are fed to a 15 input summation function to determine the total error count for the channel.

- The outputs from the 15-port demultiplexer are also re-multiplexed together for serial output to SignalTap II ™. The total error count for the channel is also output to SignalTap II ™.
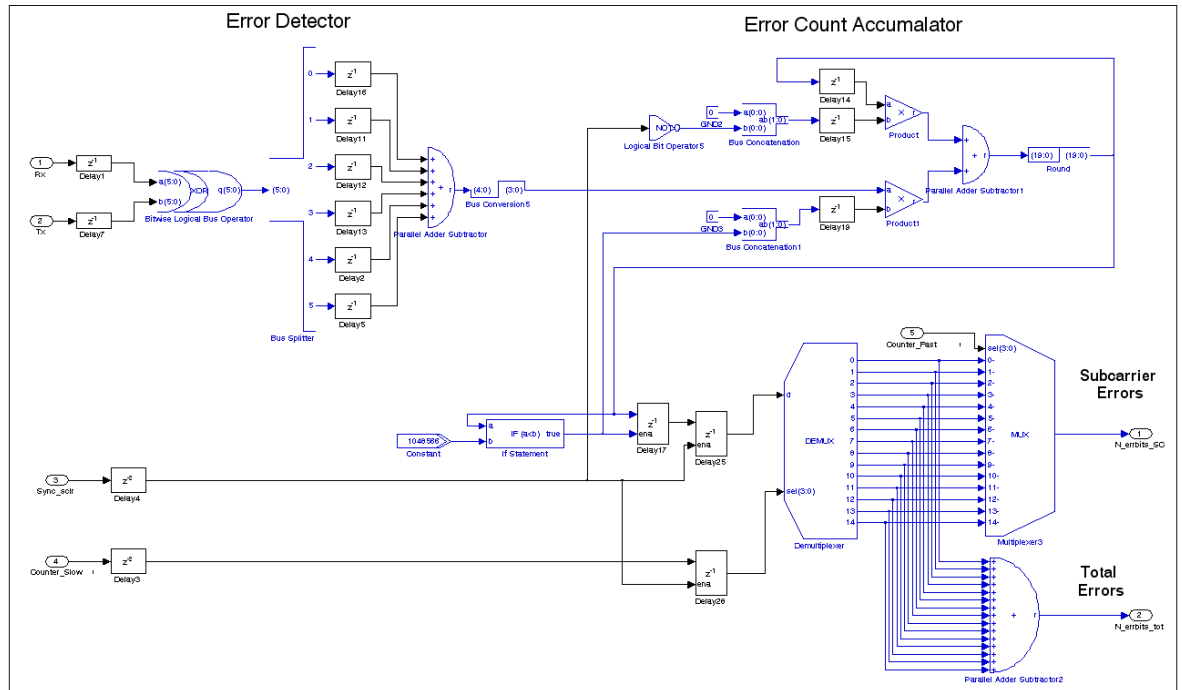
Fig. 3.34 Error Counter Block

Live performance monitoring of the real-time OODFDM system is thus achieved as the following parameters can be directly observed during live data transmission.

1. Total Channel BER.
2. Individual subcarrier BER and therefore subcarrier error distribution.
3. Constellation diagrams before channel equalisation.
4. System frequency response can also be determined from data output by the Channel Estimation and Pilot Tone Detection block, as described in section 5.2.1.4.

3.6 Conclusions

The developed FPGA-based system provides a versatile platform for high-speed DSP-based pre-processing of transmission data and post-processing of received data in the digital domain with conversion of the high speed signal to/from the analogue domain.

The developed platform consists of multi-GHz signal bandwidths, such as the 32Gb/s digital interfaces between FPGA and DAC/ADC. All system interfaces, clock distribution circuits and power supply systems have thus been carefully designed to ensure signal integrity requirements are achieved and analogue noise levels are minimised.

The real-time transmitter DSP architecture has been designed to generate high-speed OFDM signals to be converted to intensity modulated optical signals. The real-time receiver DSP architecture has been designed to perform the signal detection function to recover the transmitted data from the electrical OFDM signal generated by direct-detection of the received optical signal.

The OOFDM transmitter has been designed to incorporate the essential functions of on-line parameter adjustment. Combined with the real-time performance monitoring functions in the OOFDM receiver provides a means of rapidly optimising system performance for minimising system BER.

The performance of the custom-built 32-point IFFT and FFT algorithms has been demonstrated by implementing a back-to-back design in a single FPGA. IFFT/FFT operation has been verified at ~10Gb/s and estimated performance is of the order of >40Gb/s.

Through integration with suitable RF gain stages and E/O and O/E converters the developed OOFDM transmitter and receiver electronics can enable the first experimental demonstration of real-time end-to-end OOFDM transmission. The performance of the OOFDM modulation technique can be investigated for the first time in various types of IMDD optical links. Different types of intensity modulators and both MMF and SMF fibers can be employed as a first step towards exploring the potential of OOFDM in access network and in-building network applications.

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4 First Experimental Demonstrations of Real-time End-to-End OOFDM Transmission

Contents

4.1 Introduction

Chapter 3 described the design of the electronic elements of the real-time OOFDM transceivers, in this chapter the electronics is integrated with appropriate RF gain stages and optical components to form the complete OOFDM transmitter and receiver. As cost sensitive access and LAN applications are targeted, as stated in section 1.1, the OOFDM transmitter employs directly modulated DFB lasers (DMLs), the OOFDM receiver employs a simple direct-detection PIN detector and IMDD OOFDM transmission systems are formed free from any inline optical amplifiers or dispersion compensating fibers (DCFs). Experimental OOFDM transmission systems are therefore constructed for the first time to demonstrate and analyse the real-time end-to-end generation, transmission and detection of OOFDM signals.

The first transmission experiments verify the operation of the OOFDM transceivers using various back-to-back configurations and then explore OOFDM transmission performance over legacy MMF fibers. The performance of legacy MMF fibers is important as the reuse of the vast installed infrastructure of legacy MMF-based networks will lead to immense economical benefits when upgrading the capacity of existing LANs. Extremely high costs are involved when legacy MMFs are replaced with modern high performance MMFs especially when upgrading large LANs associated with corporate networks. Legacy MMFs however, were not designed to support the high bit rate transmission standards which are now emerging, such as 10Gigabit Ethernet. Clear evidence of this is that the single source 10GBASE-LRM 10Gigabit Ethernet standard, based on receiver side electronic dispersion compensation, is limited to a transmission distance of 220m.

The dominating property of MMF that distorts the received optical signal and starts limiting data rate is differential mode delay (DMD). DMD is a result of the excitation of multiple modes within the MMF at the input facet, the modes propagating at different speeds through the fiber. The effect causes a differential time delay between different modes at the receiver. This leads to a temporal broadening effect. From the system bandwidth point of view, the DMD effect results in a reduction of the effective bandwidth of the MMF. Generally speaking, for a given wavelength, a larger MMF core diameter leads to more modes and therefore results in a higher DMD effect and lower MMF bandwidth. The two dominating types of MMFs are OM1 and OM2. OM1 MMF has a core

diameter of 62.5μm compared to 50μm core diameter for OM2 MMF. Clearly, advanced modulation formats with high spectral efficiency, such as OOFDM, are therefore greatly beneficial in effectively utilising the limited bandwidth of the legacy MMF. OM1 MMF represents the worst case in terms of signal distortion and fiber bandwidth thus OM1 MMF is selected for demonstrating the performance of the OOFDM transceivers in legacy MMF systems.

For LAN applications it is highly advantageous to support data transmission over at least 300m of legacy MMF as the maximum reach in installed in-building fiber backbones is typically around 300m [1]. Initial experiments are therefore performed with 500m of OM1 MMF.

4.2   Real-time OOFDM transmission at 1.5 and 3 Gb/s net bit rates over 500m MMF

4.2.1 OOFDM transceiver architecture for 1.5 and 3 Gb/s

The DSP architecture of the transmitter and receiver were described in detail in chapter 3. Fig. 4.1 shows the top-level architectures of the 1.5Gb/s / 3Gb/s real-time transmitter (top) and the real-time receiver (bottom) implemented in the FPGAs. For initial testing the encoding and decoding functions employ DQPSK on all subcarriers as this does not require channel estimation or equalisation functions. The system is initially run at a sample rate of 2GS/s as this relaxes system timing constraints. The system is therefore operated with FPGA clocks of 50MHz and DAC/ADC clocks of 1GHz. DQPSK encoding on all 15 data-carrying subcarriers and a symbol rate of 50MHz leads to a raw line rate of 1.875Gb/s, which corresponds to a net bit rate of 1.5Gb/s due to the 25% cyclic prefix overhead. It should be noted that all digital transceiver parameters are all selected before design compilation, parameters such as subcarrier amplitude at the IFFT input and clipping level, are determined from the values selected in the Simulink™ simulations. The embedded logic analyser, Signal Tap II™, is employed to monitor signals in the receiver during operation, the monitored signals are: i) the symbol samples at the FFT input to observe the synchronisation symbol for the purpose of symbol alignment, as described in sections
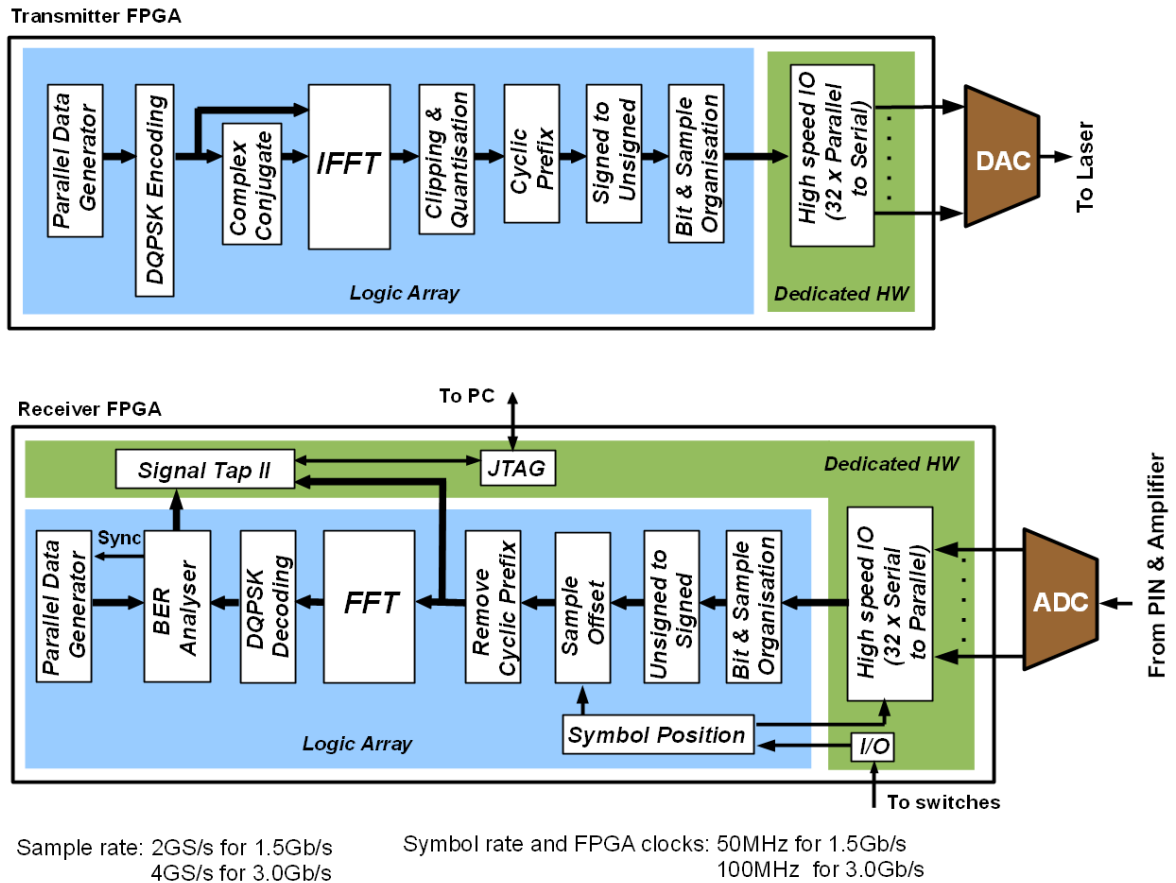
Fig. 4.1 Real-time OOFDM Transceiver Architecture for 1.5 and 3Gb/s net bit rates

3.5.3.3 and 3.5.4.3, ii) the error count in 1×10^6 symbols from the BER analyser in order to determine BER and iii) the complex frequency domain subcarrier coefficients at the FFT output for observation of DQPSK subcarrier constellations.

After the performance of the 1.5Gb/s OOFDM transmission system was fully verified and analysed, as described in section 4.3.3, the transceiver was modified for operation at 3Gb/s net bit rate. The 3Gb/s transceiver employs the same DSP architecture as the 1.5Gb/s transceiver, however the FPGA logic design is adapted for clocking at 100MHz (twice the previous speed) to support a doubling of the symbol rate. The sample rate of the DAC and ADC is also increased from 2GS/s to 4GS/s. This is accompanied with a doubling of the data rate of the associated digital interface with the FPGAs. Clearly, these modifications improve the operating speed and therefore bit rate of the OOFDM transceiver by a factor of 2 for a fixed signal modulation format. To achieve a doubling of the FPGA operating speed design modifications were required to ensure that the tighter signal timing constraints are met. Design debugging was achieved by using the embedded logic analyser,

Signal Tap II™, to observe signal integrity at various points in the design and identify where errors occur due to violation of signal timings. To ensure the signal integrity the signal propagation delay between registers must be decreased to be in line with the increase in clock frequency. This is achieved by increasing the length of the pipeline stages employed in various functional blocks, either manually, by additional signal registers, or by specifying increased pipeline lengths in the DSP-Builder functional elements in Simulink™.

A further enhancement of the 3Gb/s transmitter was the live selection of clipping level from 8 different levels, the selected level being determined from the state of 3 binary switches feeding 3 FPGA input ports. The set clipping level is $\pm\{1125+[(n+1)\times125]\}$ where n is in the range 0 to 7 and set by the external switches. The signal range before clipping is ±2047.

4.2.2 Experimental system setup for 1.5 and 3 Gb/s

VEA: Variable Electrical Attenuator   VOA: Variable Optical Attenuator
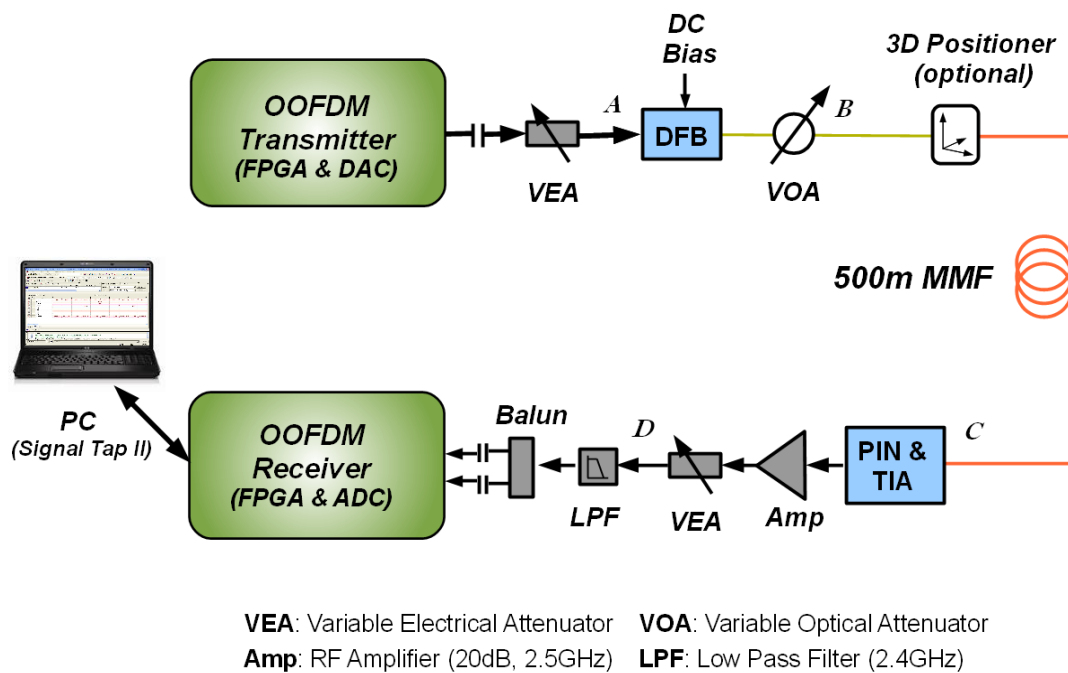Amp: RF Amplifier (20dB, 2.5GHz)   LPF: Low Pass Filter (2.4GHz)

Fig. 4.2 Real-Time OOFDM Experimental System Setup for 1.5Gb/s and 3GB/s Net Bit Rates

Fig. 4.2 shows the experimental system setup for real-time OOFDM transmission at 1.5 and 3Gb/s net bit rates. The system consists of a simple IMDD link based on a DFB-based DML. The voltage level of the electrical signal from the DAC is first attenuated as required

to provide an optimum modulating current for the employed DFB laser. The optimised modulating current is combined with an adjustable DC bias current to drive the single-mode 1550nm DFB laser with a 3-dB modulation bandwidth of approximately 10GHz and a maximum optical output power of approximately 0dBm. The OOFDM signal emerging from the DML is fed using SMF patch cords via an optical attenuator for control of transmit optical power, to an optional 3D positioner which controls the launch condition into the MMF. When the 3D positioner is not used the output from the VOA is coupled to the MMF via a mode conditioning patch cord. The attenuated optical signal is coupled, into a 500m 62.5/125μm OM1 MMF having a 3-dB optical bandwidth of approximately 675MHz·km and a linear loss of 0.6dB/km.

At the receiver, the OOFDM signal transmitted through the MMF link is detected using a MMF pigtailed, 12GHz linear PIN detector with transimpedance amplifier (TIA). The PIN has a receiver sensitivity of -17dBm (corresponding to 10Gb/s non-return-to-zero data error free system at a BER of 1.0×10^{-9}). The optical-to-electrical converted signal is first amplified with a 2.5GHz, 20dB RF amplifier and then attenuated as necessary to optimise the signal amplitude to suit the ADC's input range of ±250mV. Such adjustment also provides electrical gain control to compensate for optical signal attenuation. After passing through an electrical low-pass filter, the signal is converted via a balun to a differential signal and then digitized by the 4GS/s, 8-bit ADC in the receiver. The digitized samples are then passed to the receiver FPGA via the high-speed interface as described in section 3.4.2. It should be noted that, the RF amplifier and the low-pass filter have virtually flat response over the spectral region corresponding to the OOFDM signal (2GHz for the 4GS/s ADC/DAC), therefore, these two electrical components do not introduce significant spectral distortions into the OOFDM signal. The system frequency response roll-off effect, observed in Fig. 4.10, is mainly due to the characteristics of the DAC employed in the transmitter which is discussed further in section 4.3.4.

To examine performance robustness to different offset launch conditions at 3Gb/s, the optical signal from the DFB laser is coupled into the MMF via a 3D positioner, which enables the fine adjustment of the position of laser launch spot to emulate different launch offsets. The definition of the launch offset is illustrated in Fig. 4.3. As a reference point, the central launch position is identified first by adjusting the position of the laser launch spot in the X and Y dimensions until the optical power received at the far end of the MMF

is maximised with the corresponding offset ranges being symmetrical and maximized in both the X and Y dimensions. For the MMF adopted in the experiments, the maximum offset range without affecting significantly the output optical power is approximately ±25μm.
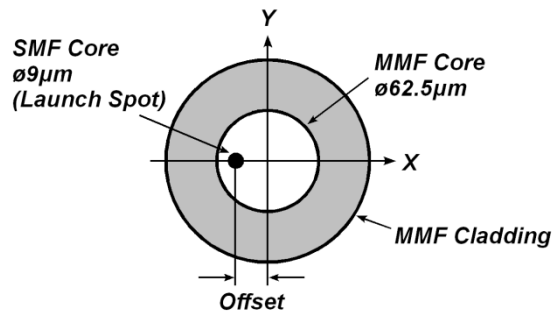
Fig. 4.3 Launch offset

4.2.3 Experimental results at 1.5Gb/s

To test the developed real-time DSP functions only, investigations are first undertaken of the performance of a digital back-to-back configuration where the output bus of the transmitter FPGA is connected to the input bus of the receiver FPGA. The serial-to-parallel converters at the receiver FPGA's inputs are first synchronised using the procedure described in section 3.5.4.1. The signal transmitted by the transmitter FPGA is then set to the OFDM signal and the error count observed in the receiver FPGA. Operation with an error count of zero is achieved, indicating a BER of zero, which verifies the operation of all DSP functional blocks.
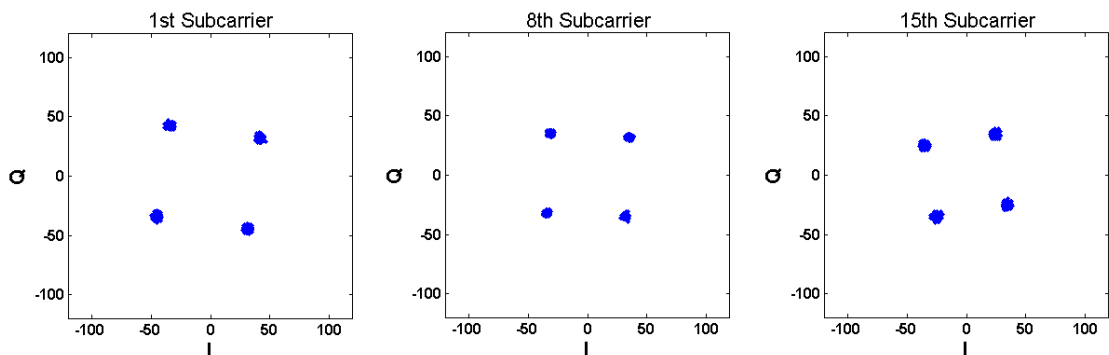
Fig. 4.4 Received 1.5Gb/s constellations for analogue back-to-back configuration

By including the DAC and ADC, the system is tested in an analogue back-to-back configuration, in which points A and D, as shown in Fig. 4.2, are directly connected with the electrical attenuator being set to 3dB. With the sampling rate of 2GS/s and DQPSK, 1.5Gb/s net bit rate transmission is achieved at a BER of zero, the corresponding constellations of the 1st, 8th and 15th subcarriers are shown in Fig. 4.4, where all subcarriers exhibit clean constellations with low noise and distortion, suggesting that all unwanted system noise sources and distortions have been kept sufficiently low so that their combined effect results in a high SNR on all subcarriers. The varied constellation rotations observed in Fig. 4.4 can be attributed to the frequency dependent phase changes introduced by the analogue front-ends of the DAC and ADC. The observed high SNR has the advantage that higher modulation formats can potentially be employed to increase system bit rate, increasingly higher modulation formats requiring increasingly higher SNRs for the same BER. The sources of system noise and distortion that have been suitably limited include: DSP quantisation noise, DAC/ADC quantisation noise, DAC/ADC power supply noise, inter-circuit crosstalk, power supply coupling and clock timing jitter.

Further experimental measurements are performed in an optical back-to-back configuration, in which points B and C, as shown in Fig. 4.2, are connected. For such a case, the transmitter side electrical attenuator, the optical attenuator and the receiver's total electrical gain are set to 5dB, ≤6dB and 3dB, respectively, also a DFB bias current of 38mA is adopted. As shown in Fig. 4.5, for optical launch powers of >-12dBm, 1.5Gb/s transmission at a BER of $\ll 1.0 \times 10^{-9}$ is obtainable. At an optical launch power of -11.5dBm the displayed error count is stable at zero, although this is approximated to 1×10^{-11} for display purposes in Fig. 4.5. For this configuration Fig. 4.6 shows received constellations of the 1st and 15th subcarriers corresponding to the case of zero error count in Fig. 4.6(a,b) and BER of 1×10^{-3} in Fig. 4.6(c,d). The constellations in Fig. 4.6(a,b) show that the SNR of the received subcarriers has decreased slightly compared to the analogue back-to-back case. This reduction in SNR can be attributed three factors: i) DML-induced distortion due to nonlinear intensity modulator effects such as frequency chirp, ii) shot noise and thermal noise associated with the photodetector and iii) subcarrier intermixing upon direct photon detection in the receiver [5,6]. Fig. 4.6 also shows a a more severe roll-off in subcarrier amplitude from the first to last subcarrier compared to the small roll-off in the analogue back-to-back case. This effect can be attributed to the selected operating

condition of the DFB laser which may not coincide with the conditions for maximum bandwidth but instead achieves increased SNR in the required signal spectral region.

Finally, experimental measurements are undertaken of 1.5Gb/s transmission over a 500m IMDD MMF link illustrated in Fig. 4.2. The measured BER as a function of optical launch power is plotted in Fig. 4.5. At an optical launch power of -11.2dBm the displayed error count is stable at zero, this is approximated to 1×10^{-11} for display purposes in Fig. 4.5. Corresponding received constellations of the 1st, 8th and 15th subcarriers are shown in Fig. 4.7 for BERs of 1.1×10^{-8} in Fig. 4.7(a-c) and 1.2×10^{-3} in Fig. 4.7 (d-f). When comparing the constellations of the optical back-to-back case in Fig. 4.6(a,b) and the 500m MMF link case in Fig 4.7(a-c) it would appear that SNR has been reduced, however these constellations are taken at slightly different received optical powers which accounts for the apparent difference in the observed SNR. The similar performance of the two aforementioned cases, as shown in Fig. 4.5, indicates that there is negligible change in SNR due to transmission through the 500m MMF link.

A power penalty of only ~0.2dB at a BER of 1.0×10^{-3} is observed in Fig. 4.5 indicating that the DMD effect is almost entirely compensated. This indicates that the cyclic prefix length is sufficient to absorb the ISI region of the OOFDM symbols.

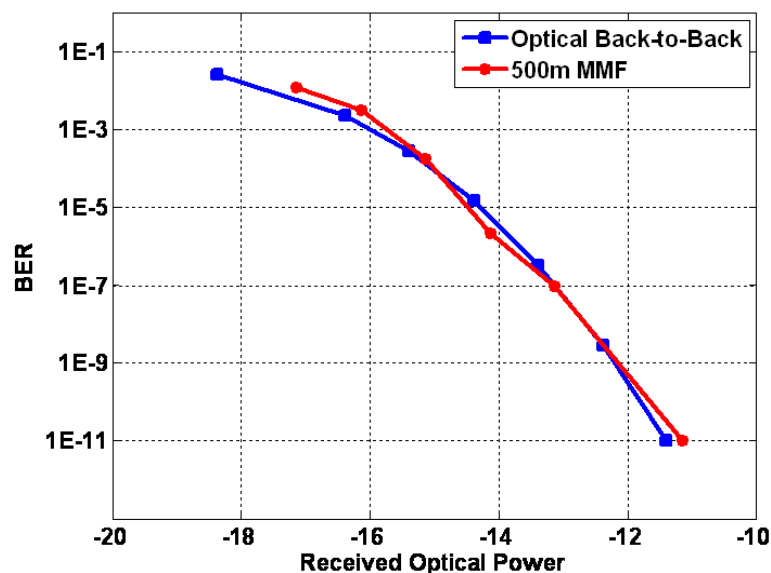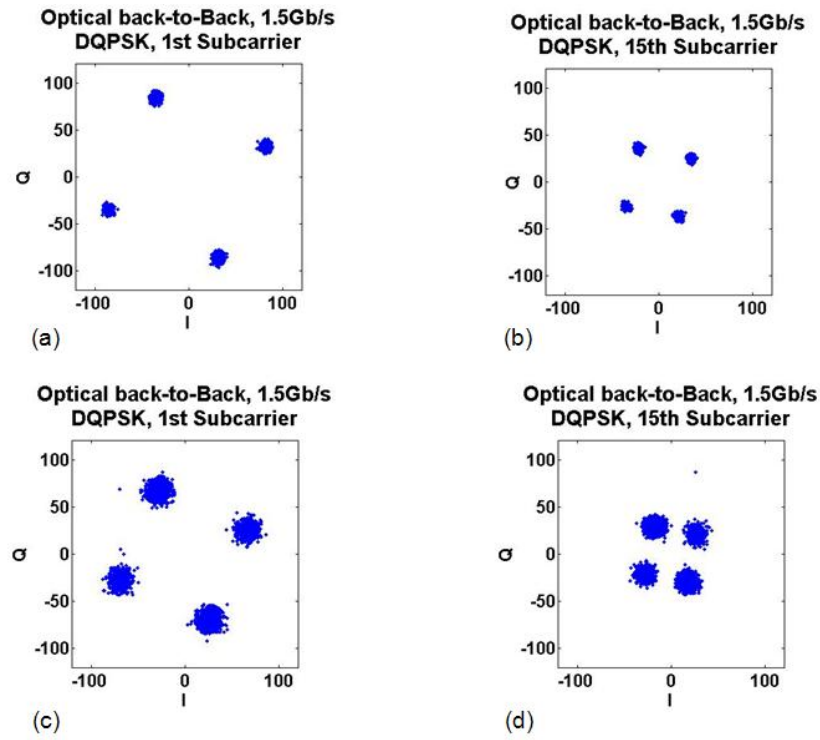*Fig. 4.5 Real-time OOFDM transceiver performance at 1.5 Gb/s net bit rate*

Fig. 4.6 Constellations of various DQPSK-encoded subcarriers for 1.5Gb/s transmission on optical back-to-back configuration at BER of zero (a,b) and BER of 1x10^{-3} (c,d)
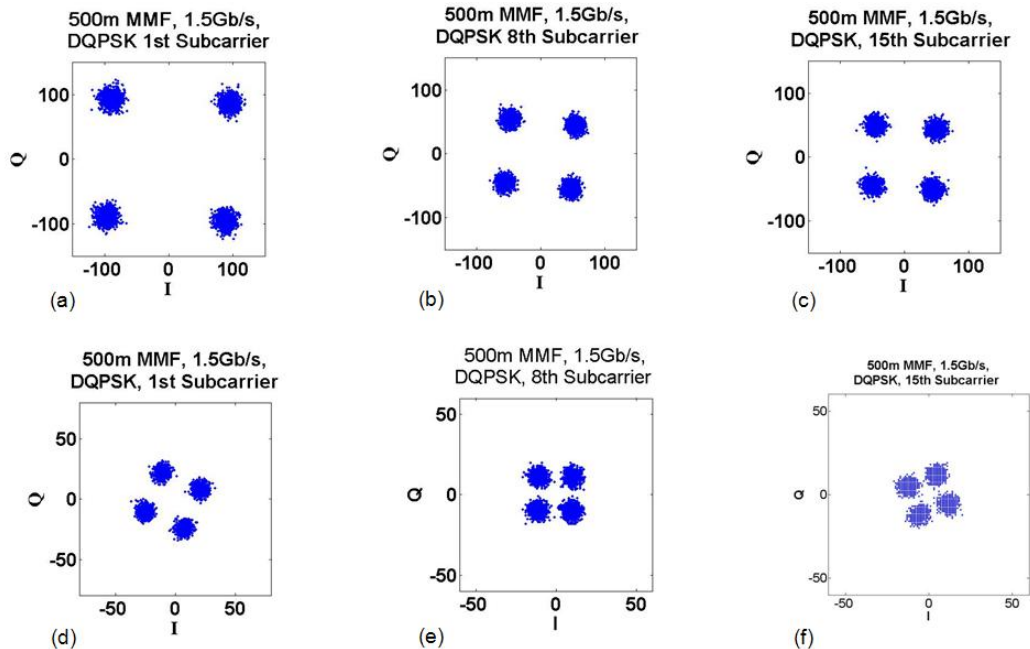
Fig. 4.7 Constellations of various DQPSK-encoded subcarriers for 1.5Gb/s transmission over 500m MMF at BER of 1.1x10^{-8}(a-c) and BER of 1.2x10^{-3} (d-f)

4.2.4 Experimental results at 3Gb/s

Experimental measurements are first performed of the transmission performance of 3Gb/s
net bit rate DQPSK-encoded OOFDM signals in an IMDD 500m MMF system involving
the DML, as shown in Fig. 4.2. The electrical spectrum of the transmitted 3Gb/s OOFDM
signal (point A in Fig. 4.2) was firstly examined and is shown in Fig. 4.8. As the sample
rate is 4GS/s the OOFDM signal occupies the spectral region between 0 and 2GHz and a
roll-off in subcarrier amplitude can be seen at the higher frequencies. The roll-off effect is
due to the DAC and results from i) the low-pass on-chip filtering at the DAC output and ii)
the sin(x)/x response inherent to zero-hold DACs. In the region from 2GHz to ~2.5GHz the
residual sampling image signal is observed, this is due to the first-order low-pass filter
which can not totally remove the image signal. It should be noted that no guard band is
employed between the baseband signal and the image signal and that the whole Nyquist
band is used for signal transmission.
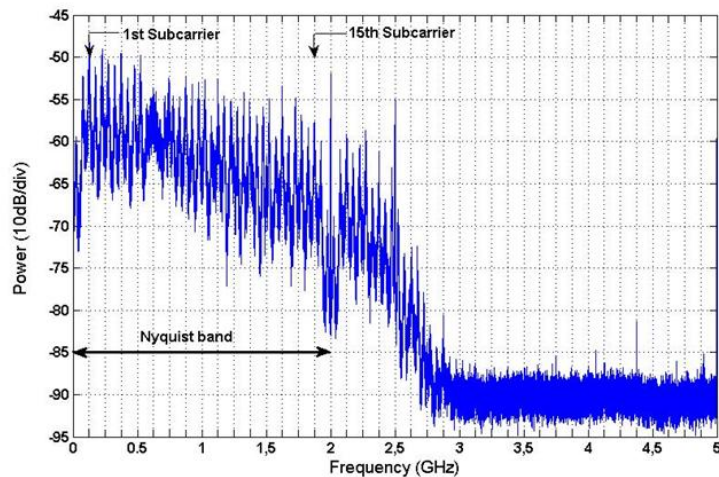
Fig. 4.8 Electrical spectrum of OFDM signal at transmitter

To analyse system performance the measured BER as a function of optical launch power is
plotted in Fig. 4.9 for cases of optical back-to-back and 500m MMF transmission. For the
optical back-to-back configuration point B is connected to point C in Fig. 4.2 with a mode
conditioning patch cord. For the 500m MMF transmission mode conditioning patch chord
is used to couple the optical signal into the MMF. The DFB bias current is set to 38mA.
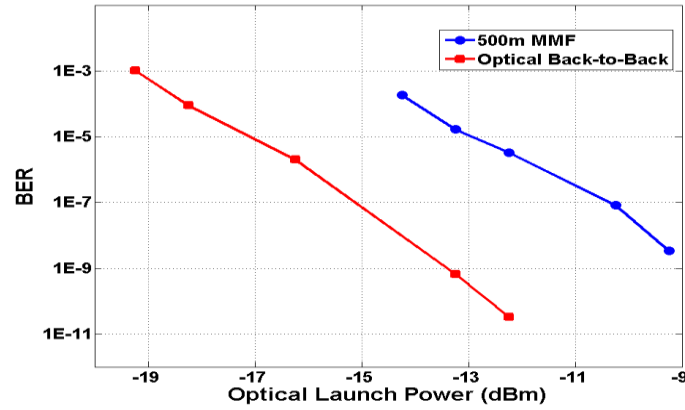
Fig. 4.9 BER performance of 3Gb/s DQPSK-encoded OOFDM signal transmission over a 500m MMF.

It can be seen from Fig. 4.9 that, for the optical back-to-back case, a BER as low as 3.3×10^{-11} is achieved at optical launch powers of >-12dBm and for the case of 500m MMF transmission, a BER as low as 3.3×10^{-9} is achieved at optical launch powers of >-9.2dBm. In particular, for both cases there is no error floor observed within the BER ranges of practical interest. Taking into account the total linear link loss of about 1dB, an optical power penalty of approximately 3dB at a BER of 1.0×10^{-4} can be obtained from Fig. 4.9. This penalty mainly results from the MMF-induced DMD effect [2]. It should be noted that the use of adaptive power loading can significantly reduce the optical power penalty, as discussed in Chapter 5.

After transmitting through the 500m MMF, the constellations of the 1st, 9th and 15th subcarriers are presented in Fig. 4.10 for two representative BERs of 3.3×10^{-9} and 1.8×10^{-4}. As seen in Fig. 4.10, the subcarrier amplitude decreases rapidly for subcarriers locating at high frequencies. The roll-off effect is mainly due to the analogue electrical components (DAC) involved in the transceiver, as very similar behaviour also occurs for an analogue electrical back-to-back case where the electrical signal from the attenuator in the transmitter is directly linked to the low-pass filter in the receiver without any optical components being involved. The degree of subcarrier attenuation at higher subcarrier frequencies is increased in comparison to that observed by the 1.5Gb/s transmission system as seen in Fig. 4.7, this is due to the fact that as sample rate has been doubled the OOFDM signal now occupies a spectral bandwidth up to ~2GHz compared to ~1GHz at 1.5Gb/s. The wider spectral bandwidth therefore suffers more from the frequency roll-off effect.

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The clear constellations in Fig. 4.10 show that BER is similar across all subcarriers and the low total BER shows that the frequency roll-off effect has negligible impact on system BER performance.
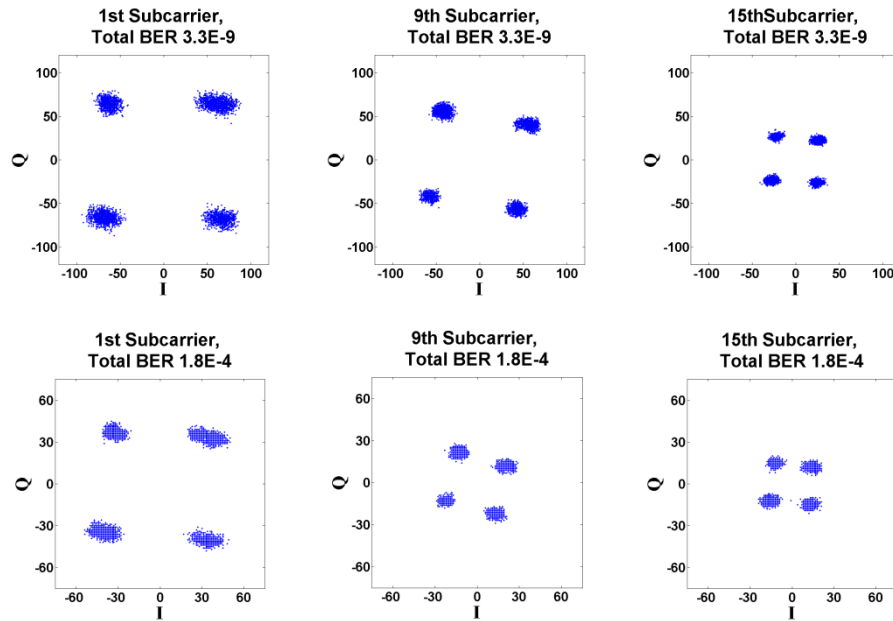
Fig. 4.10 Constellations of various DQPSK-encoded subcarriers for 3Gb/s signals after transmitting through 500m MMF.
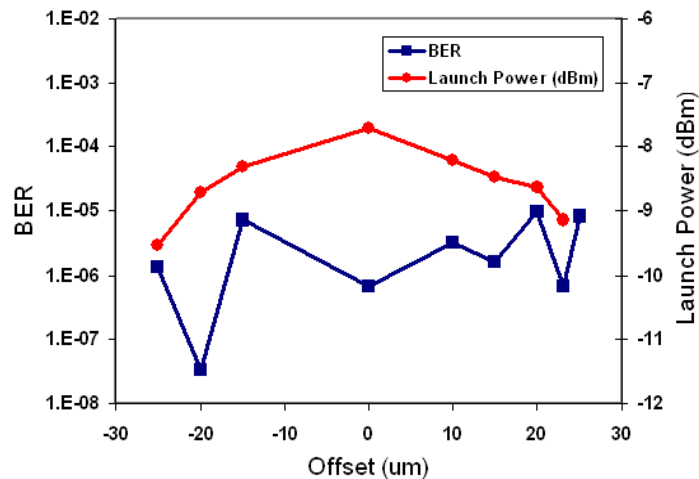
Fig. 4.11 BER and optical launch power versus launch offset for 3Gb/s over 500m MMF transmission of DQPSK-encoded OOFDM signals.

Experimental explorations are also undertaken of performance robustness to different offset launch conditions. The transmission link configuration and the transceiver parameters are identical to those used in obtaining Fig. 4.2, except that a 3D positioner is utilised here. For 3Gb/s transmission of DQPSK-encoded OOFDM signals over the 500m

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MMF, the measured BER versus launch offset is given in Fig. 4.11, in which the variation of the corresponding optical launch power at the input facet of the MMF link is also presented. Fig. 4.11 shows excellent performance robustness with BERs of $<1.0 \times 10^{-5}$ being maintained over the entire launch offset range from -25μm to 25μm. In particular, as expected, an improved BER performance occurs at the conventional offset launch region (around ±20μm) [3]. The results imply that the adopted cyclic prefix is sufficiently longer than DMDs associated with different launch offsets [4]. It is also expected that both the performance robustness and the corresponding transmission capacity can be improved further if use is made of adaptive modulation on different subcarriers within an OOFDM symbol [4].

4.3   Conclusions

For the first time real-time OOFDM transceivers based on off-the-shelf components including FPGAs, DACs and ADCs have been successfully employed to experimentally demonstrate real-time end-to-end OOFDM transmission at 1.5Gb/s net bit rate employing DQPSK modulated subcarriers. The real-time end-to-end OOFDM transmission was achieved over 500m OM1 MMF in a simple DML-based IMDD link with virtually error-free transmission.

The 1.5Gb/s real-time OOFDM transceivers were modified for operation with a twofold increase in speed to achieve a net bit rate of 3Gb/s whilst maintaining DQPSK subcarrier modulation. Transmission at 3Gb/s was then also demonstrated over 500m OM1 MMF in a DML-based IMDD link with total system BER as low as 3.3×10^{-9} at an optical launch power of -9.2dBm. The developed 3Gb/s OOFDM transmitter also incorporated live modification of clipping ratio for performance optimisation. In addition, excellent performance robustness has also been observed to various offset launch conditions at 3Gb/s.

This work is a significant first step in the exploration of the practicality of the OOFDM technique as it demonstrates that modern semiconductor electronics can perform the required computationally intense algorithms with sufficient speed and precision in real-time. Furthermore the operation at extremely low BERs clearly indicates that there is

potential for achieving higher transmission capacity. The developed transceivers therefore provide a solid platform to further explore real-time OOFDM transmission at higher speeds through design improvements in the associated DSP algorithms.

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5 Design Improvements for Increased OOFDM Transceiver Capacity

Contents

5.1 Introduction

In the previous chapter the developed OOFDM transceivers were successfully employed to experimentally demonstrated real-time OOFDM transmission at net bit rates of 1.5Gb/s and 3Gb/s using DQPSK modulation on all subcarriers with identical electrical power. The next logical step in exploring the viability of the OOFDM technique for meeting future network demands is to investigate the possibility of achieving higher line rates with the real-time OOFDM transceivers. The same high level platform and transmission system is employed with modifications only implemented to the DSP design. To maintain cost-effectiveness, the DML-based IMDD links are considered and the signal sample rate and bandwidth are maintained at 4GS/s and 2GHz, respectively. As the signal bandwidth is not enlarged the spectral efficiency of the system must be enhanced in order to achieve increased line rates.

The characteristic of OFDM modulation which is now exploited is that higher modulation formats can be imposed on the subcarriers (not all subcarriers necessarily using the same modulation format), this will achieve the required increase in spectral efficiency. However the higher modulation formats increase the demands on SNR for achieving a fixed BER performance. The subcarrier's SNR ultimately determines the highest modulation format it can use. A characteristic of OFDM modulation, which can potentially be exploited to maximise the performance, is that the BER of each subcarrier is only dependent on the SNR at the corresponding subcarrier frequency. Controlling the distribution of SNR across the signal spectral region can therefore provide a means of maximising performance.

For a given transmission system, employing high subcarrier modulation formats whilst all other system parameters are maintained constant results in a reduction in the system BER. However, for the 3Gb/s OOFDM transceiver the high BER performance of 1.2×10^{-9} over 500m MMF indicates the strong potential for operating at higher modulation formats as there is clearly a large margin before the FEC limit, typically 1×10^{-3}, is reached.

This chapter first describes a modification to the transceiver design to employ high signal modulation formats on all subcarriers to increase the raw line rate to 7.5Gb/s and beyond. For example, if 16-QAM is employed, it encodes 4 bits per subcarrier in each OFDM symbol, thus the bits per subcarrier are double compared to DQPSK. To enable the higher line rate, two essential functions are also incorporated: i) channel estimation and equalisation and ii) variable power loading. Channel estimation and equalisation is required with QAM modulation formats as the absolute subcarrier phase and amplitude contains information and not, as with DQPSK, only the relative phase. The amplitude and phase of all received subcarriers vary with the transmission link dependent channel transfer function (CTF). Known pilot signals are therefore transmitted which can be identified at the receiver and used to estimate the CTF at each subcarrier frequency. This information is then be used to equalise the individual subcarriers before data recovery. Furthermore, it has also been discovered that the system frequency response roll-off, which manifests as increasing attenuation with increasing subcarrier frequency, has a significant impact on system performance and that pre-compensation of subcarrier amplitudes in the transmitter, also referred to as variable power loading, can significantly improve the system performance.

This chapter also presents a further design modification to employ 64-QAM on all subcarriers to further increase the raw line rate to 11.25Gb/s. 64-QAM encodes 6 bits per subcarrier thus achieving a 1.5 times increase in bit rate compared to 16-QAM, and the same channel estimation and equalisation function is utilised with 64-QAM without any modifications needed. However, as 64-QAM requires a higher SNR for a fixed BER the transmission channel's frequency response roll-off effect, which results in increasing attenuation for increasing subcarrier frequency, has a more pronounced impact on system performance. The development of an improved variable power loading technique, offering both increased adjustment and full live control of subcarrier power levels, is, therefore, essential to achieve an acceptable BER performance.

In addition to the aforementioned key functional improvements, advanced features for on-line parameter optimisation and performance monitoring are also implemented. The on-line control of signal clipping level is improved to allow clipping at any level within the IFFT output range in preference to selection from a limited number of preset values. The frequency response of the system from IFFT input in the transmitter to FFT output in the

receiver can be determined using the channel estimation function. Also the BER analyser function is modified to measure the BER of individual subcarriers such that the BER distribution across the subcarriers can be measured. These advanced on-line parameter adjustment and monitoring functions provide a highly effective means of analysing and adaptively optimising system performance as described in sections 5.2.2 and 5.3.3.

All changes made to each transceiver design are described in detail and the performance of the OOFDM transceiver designs are fully analysed in simple DML-based IMDD links based on both MMF and SMF fibers. Real-time OOFDM transmission is successfully demonstrated first at 7.5Gb/s over 300m MMFs and subsequently at 11.25Gb/s over 500m MMFs and 25km SMFs.

5.2 7.5Gb/s Real-time OOFDM Transmission over 300m MMF using Channel Estimation and Variable Power Loading

5.2.1 OOFDM Transceiver Architecture for 7.5Gb/s

Fig. 5.1 shows the detailed architectures of the 7.5Gb/s real-time transmitter (top) and the real-time receiver (bottom) implemented in the FPGAs which are based on the 3Gb/s transceiver design with new functional blocks added and some existing blocks modified, these blocks are highlighted in yellow and orange respectively in Fig. 5.1. System clock frequencies are maintained at 100MHz for both the transmitter and receiver FPGAs and 2GHz for the 4GS/s DAC and ADC, the clocks are generated from a common reference source as in the 3Gb/s design.

Compared to the previous design the DQPSK encoders are replaced by 16-QAM encoders thus each subcarrier encodes 4 bits instead of 2 and so the total line rate is raised to 7.5Gb/s. As the same 25% cyclic prefix is used the net bit rate is increased to 6Gb/s. As previously mentioned, to employ 16-QAM modulation it is necessary to include channel estimation and equalisation functions. Suitable functional blocks were implemented in [1] and operated with a sampling rate of 2GS/s for a net bit rate of 3Gb/s, these blocks are now incorporated into the new design operating at 4GS/s for a net bit rate of 6Gb/s. Also as 16-QAM is more sensitive to the system frequency response roll-off effect, it is necessary to

implement a variable power loading function to compensate the associated roll-off in subcarrier amplitudes, as with equal subcarrier powers acceptable system BERs cannot be achieved. By implementing a simple 3-level subcarrier power loading function it is shown that the roll-off effect can be compensated sufficiently to achieve acceptable system BER performance as shown in section 5.2.2. Furthermore advanced on-line performance monitoring and live parameter optimisation functionalities have been implemented to accommodate the increased number of bits per symbol and provide the advanced functions as described in section 5.1.
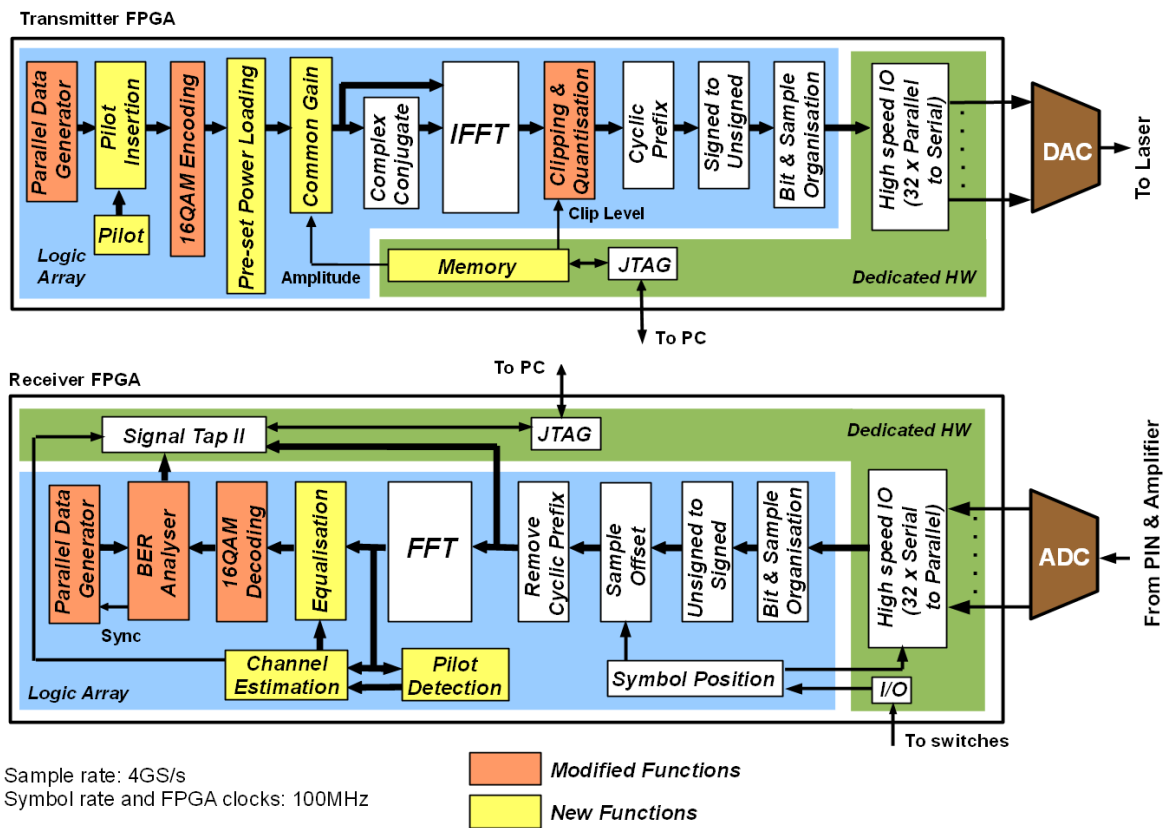
Fig. 5.1 Real-time OOFDM Transceiver Architecture for 6Gb/s net bit rate

As a detailed description has been given of the initial DSP architecture supporting 1.5Gb/s and 3Gb/s in chapters 3 and 4 the modifications and additions to the DSP architecture for increased bit rates are described here. In the transmitter FPGA the parallel data generator is modified to produce a 56-bit wide parallel pseudo random bit sequence of length 88,500 words (4.956×10^6 bits) which is employed as information data.

5.2.1.1 Pilot Insertion

Following the parallel data generator the Pilot Insertion function is incorporated, here one extra parallel bit sequence of a 4-bit fixed pattern, representing known pilot subcarrier data, is diagonally mapped into the time-frequency OOFDM symbol space as shown in Fig. 5.2. Mathematically, the pilot and data-bearing subcarrier mapping on to the frequency domain subcarriers $X_{k,m}$ can be expressed as:

$$X_{k,m} = \begin{cases} p_{k,m} & (m-k) = qN_s \\ d_{k,m} & (m-k) \neq qN_s \end{cases} \qquad q = 0,1,2,3,\dots \qquad (5.1)$$

where m is the index of the OOFDM symbols, k is the index of the subcarriers within the symbol and $p_{k,m}$ and $d_{k,m}$ are the complex valued pilot and data-bearing subcarriers, respectively.
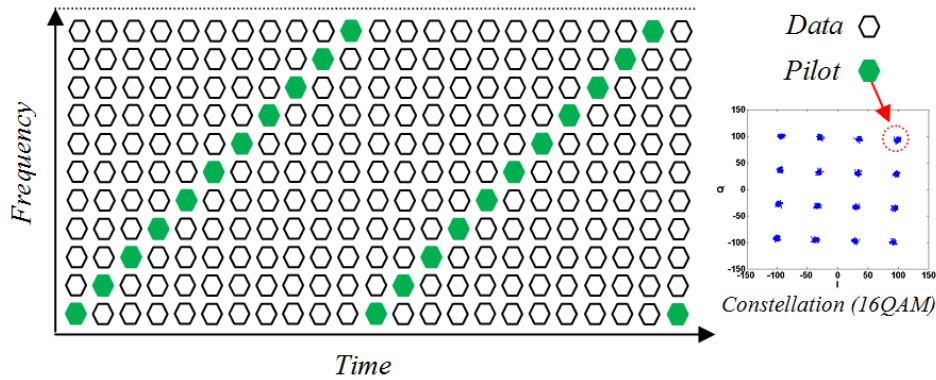
Fig. 5.2 Pilot and data bearing subcarrier mapping in the OOFDM time-frequency symbol space.

To maximise the SNR of the received pilot subcarrier for increased CTF estimation accuracy, the fixed pilot pattern corresponds to one of the four diagonal end points of the 16-QAM constellation or even higher modulation constellations, as shown in Fig. 5.2. The employed pilot-data mapping allows highly accurate, interpolation-free channel estimation at all subcarrier frequencies within the entire signal spectrum. In addition, buffering of the information data is not required as 14 subcarriers are always available in each symbol to permit continuous data flow. The 60-bit wide data constructed from the data and pilot bit sequences is employed to feed the 15 parallel 16-QAM encoders.

5.2.1.2 Variable Power Loading

In the 16-QAM encoding block, the peak signal amplitude of all individual encoders are identical, the following Preset Power Loading block multiplies each individual complex encoder output by a pre-selected fixed gain value set before design compilation. The gain values are selected to implement a variable power loading scheme where the power distribution is based on a 3-level approach such that subcarrier amplitude can be one of three values and increases with increasing subcarrier frequency in a stair-like profile. The power loading profile is manually determined using Eq. (2.40), as live adjustment is not possible the profile is unlikely to be the absolute optimum.

To control the total signal power the amplitudes of the 15 encoded subcarriers, carrying either information data or pilot data, can be adjusted in the following Common Gain block which multiplies all subcarriers by a common scaling factor in the range 0 to 2. The scaling factor is derived from an 8 bit unsigned value in the range 0 to 255 stored in the embedded memory which can be updated during live data transmission via the JTAG interface using the Quartus II memory content editor function. The variable power loading profile, which is fixed at design compilation time, sets the relative subcarrier powers. However, to obtain the optimum signal amplitudes for the limited dynamic range of the IFFT input the absolute power levels of all subcarriers at the IFFT input can be adjusted simultaneously on-line as the system is operating.

5.2.1.3 Enhanced Clipping Level Control

The transmitter functions between the Common Gain block and the high-speed interface to the DAC are identical to the previous 3Gb/s implementation except that here the on-line control of clipping level is significantly enhanced to allow precise control and improved optimisation of signal clipping ratio. The digital variable that sets the positive and negative clipping levels of all 12 bit signed samples at the IFFT output, as described in section 3.5.2.1, is now provided by an 11 bit unsigned data value stored in embedded memory which can be modified on-line as previously described. This feature allows the impact of changing the clipping level, and therefore the clipping ratio, on BER to be instantly observed and permits rapid optimisation of clipping ratio to maximise system performance. The number of quantization bits of the clipping and quantisation function remains at 8 to

match the resolution of the employed DAC. The length of cyclic prefix added to each symbol remains at 8 samples, maintaining 40 samples per symbol. The FPGA clock and symbol rate of 100MHz and the sample rate of 4GS/s also remain unchanged.

In the receiver FPGA all functional blocks from the high-speed ADC interface up to and including the FFT block are identical to those in the 3Gb/s architecture. Manual symbol synchronisation is performed as described in sections 3.5.3.3 and 3.5.4.3. Again the FPGA clock frequency (symbol rate) and sample rate are unchanged at 100MHz and 4GS/s respectively.

5.2.1.4 Pilot Detection, Channel Estimation and Equalisation

At the FFT output, 15 subcarriers in the positive frequency bins are selected for channel estimation and subsequent data recovery. When transmission is first established the Pilot Detection block locates the symbols with the first subcarrier being a pilot subcarrier, these symbols are regarded as a pilot subcarrier reference points. At the output of the FFT, the identification of the received pilot subcarriers is first made by performing the following two operations to subcarrier 1 of different symbols:

$$D_{m,1} = \mathcal{X}_{m,1} \cdot \mathcal{X}^*_{(m+N_s),1} \tag{5.2}$$

$$Q_{m,1} = \frac{1}{C} \left| \sum_{i=0}^{C-1} D_{(m+iN_s),1} \right|^2 \tag{5.3}$$

where $X_{m,1}$ ($X^*_{(m+Ns),1}$) is the received complex (complex conjugate) value of subcarrier 1 of the m-th [$(m+N_S)$-th] symbol. C is a preset integer number determining the total number of N_s symbol-spaced D values used for averaging. As the pilot mapping sequence repeats every N_S symbols, $Q_{m,1}$ must be determined for Ns adjacent symbol locations. For the implemented design 15 values of $Q_{m,1}$ are therefore determined. The data-bearing subcarriers are modulated with complex values encoded using an effectively random data sequence, this results in minimised Q values due to the averaging process. Each of the pilot subcarriers is modulated with a fixed complex number with maximal amplitude, causing the occurrence of a Q peak corresponding to the symbol locations where subcarrier 1 is the pilot subcarrier, as shown in Fig. 5.3. A large C will make the Q peak more distinguishable, but this requires a longer time and more logic resources to conduct the

averaging operation, therefore *C* should be optimised. Experimental measurements show that *C* = 16 is adequate for all the systems of interest in the systems presented in the thesis and is therefore adopted for all receiver designs. By locating the peak in the 15 detected *Q* values the symbol where subcarrier 1 is the pilot is identified, based on this reference pilot, all other pilot subcarriers in subsequent symbols can be easily identified due to their fixed relative positions. In the implemented design the pilot detection function operates continuously, however after identifying the reference pilot subcarriers, the pilot detection process could be terminated and only needs to be reactivated following a break in the transmission.
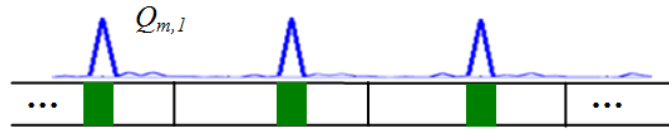
Fig. 5.3 Pilot subcarrier identification using Q peaks after FFT in the receiver.

Making use of the assigned transmitted pilot subcarriers and the received pilot subcarriers, the channel estimation block determines the complex system frequency response, H_k (k= 1, 2, …N_s), by performing the operation defined below:

$$H_k = \frac{1}{M} \sum_{i=0}^{M-1} \frac{R_{(k+iN_s),k}}{p_{(k+iN_s),k}} = \frac{1}{M \cdot P} \sum_{i=0}^{M-1} R_{(k+iN_s),k} \tag{5.1}$$

where N_s is the total number of non-zero-power subcarriers in the positive frequency bins. $R_{(k+iNs),k}$ $(p_{(k+iNs),k})$ is the received (effectively assigned) complex value of the k-th pilot subcarrier in the $(k+iN_s)$-th symbol. As a constant value, *P*, is used for the pilot subcarriers the simplified expression on the right of Eq. (5.1) is used. To reduce the noise effect associated with the transmission system, frequency response averaging is performed over *M* received/assigned pilot subcarriers at each frequency. Here *M* is taken to be 32, which is an optimum value identified experimentally in [1]. It should be noted that all other channel estimation parameters that are not explicitly mentioned above, are taken to be identical to those presented in [1].

The system frequency response obtained in the channel estimation function is then used by the channel equalisation block to equalise each individual subcarrier using the following operation:

$$X_{m,k} = (H_k)^{-1} \, \mathcal{X}_{m,k} \qquad (5.2)$$

where $\mathcal{X}_{m,k}$ is the received complex value of the k-th subcarrier in the m-th symbol. The equalised subcarriers, $X_{m,k}$, are then decoded with 15 parallel 16-QAM demodulators. The real and imaginary parts of the 15 complex frequency response parameters H_k determined by the channel estimation block are probed by the Signal Tap II™ embedded logic analyser, H_1 to H_{15} are then extracted by the Signal Tap II™ application in order to view the live system frequency response from IFFT input to FFT output. This feature is utilised to determine suitable levels for the preset variable power loading profile employed in the transmitter.

It is important to note that, due to the quasi-static nature of the optical channel a low CTF estimate update rate can be employed without degrading system performance. The channel estimation technique can therefore only insert pilot data in periodic bursts of pilots, this allows all 15 subcarriers to be used for data transmission between pilot bursts. The insertion rate of the pilot bursts can be as low as 10Hz [1], corresponding to an extremely low overhead of 0.001% for the channel estimation function.

5.2.1.5 Subcarrier BER Distribution and Total BER Measurement

The recovered bit sequence is analysed by the improved BER Analysis function described in section 3.5.4.4. It is worth noting here that this block performs the removal of the pilot data from the test data before detecting errors and performs BER analysis across all subcarriers, even though only 14 subcarriers transport data in any one symbol. Both the total channel bit error count and the individual subcarrier error counts over 88,500 symbols are continuously measured, updated and displayed, via Signal Tap II™, with the BER analyser. This allows the calculation and display of the total channel BER, BER_T, and the subcarrier BER, BER_K, which have the following relationship

$$BER_T = \frac{1}{N_s} \sum_{K=1}^{N_s} BER_K \qquad (5.3)$$

The on-line BER and system frequency response monitoring enables the transmission performance to be optimised by fine adjustment of the transceiver parameters such as electrical gain and DML operating conditions.

VEA: Variable Electrical Attenuator   **VOA**: Variable Optical Attenuator
Amp: RF Amplifier (20dB, 2.5GHz)   **LPF**: Low Pass Filter (2.4GHz)
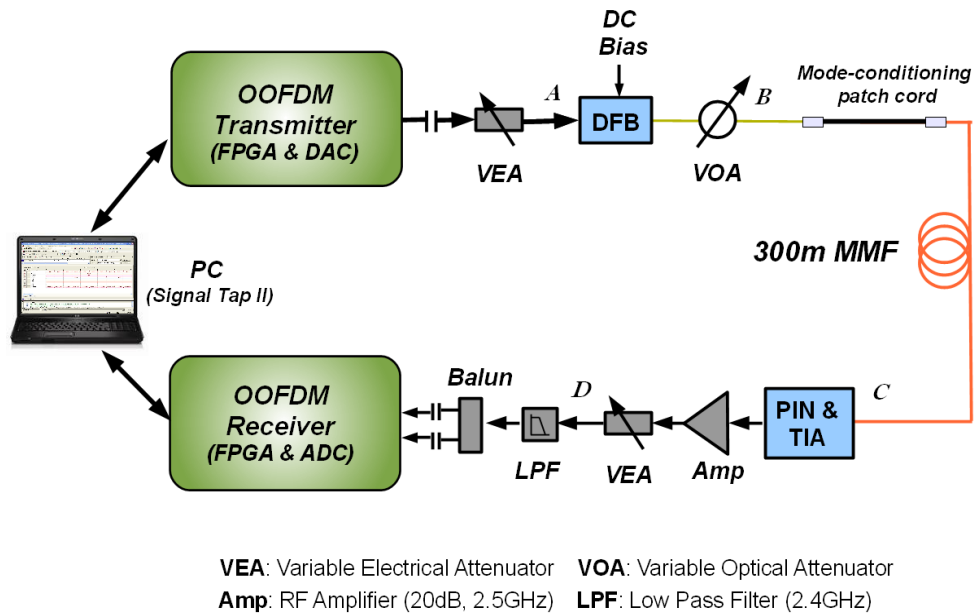
Fig. 5.4 Real-Time OOFDM Experimental System Setup for 7.5 Gb/s line rate

5.2.2 Experimental System Setup for 7.5Gb/s

Fig. 5.4 shows the real-time experimental system setup for the real-time OOFDM transmission at 7.5Gb/s line rate. The set up employed here is virtually identical to the set up used for the 1.5Gb/s and 3Gb/s experiments described in section 4.2.2, all optical and electrical components are unchanged and the only difference is that a 300m span of the 62.5/125μm OM1 MMF, having a 3-dB optical bandwidth of approximately 675MHz·km and a linear loss of 0.6dB/km, is now employed. This type of fiber is again employed to demonstrate operation with legacy MMFs, this is due to the considerable benefits associated with installed fiber reuse as previously described in chapter 4. A 300m length of fiber is selected as this is the typical span in in-building networks and so provides a realistic reach target for the increased bit rate real-time OOFDM transceiver. The optical signal is launched into the MMF via a mode-conditioning patch cord. As in the previous

experiments the DFB operating parameters that are adjusted on-line for performance optimisation are the modulating current peak-to-peak amplitude and DC bias current. Also, as in the previous experiments, electrical gain control is employed in the receiver to compensate for optical signal attenuation.

5.2.3 Experimental Results at 7.5Gb/s

As already discussed in section 5.2.1, with the 100MHz FPGA operating speeds and the 4GS/s sample rates of the DAC/ADC, 7.5Gb/s line rate real-time OOFDM signals are produced when 16-QAM is taken on all the 15 information-bearing subcarriers. Due to the 25% cyclic prefix a net bit rate of 6Gb/s is obtained. It should be pointed out, in particular, that the obtained 6Gb/s transmission capacity can be utilised almost entirely to carry payload data. This originates from the following three facts: 1) the 6Gb/s signal bit rate is obtained after subtracting the transmission capacity corresponding to the cyclic prefix from the raw signal line rate of 7.5Gb/s; 2) as described in section 5.2.1.4, subcarrier-assisted channel estimation requires an extremely low overhead, and 3) no other training sequences are employed in the transmission system. In this section, extensive use is made of the 7.5Gb/s 16-QAM-encoded OOFDM signals to explore: 1) the effectiveness of the variable power loading scheme, and 2) the transmission performance of the 7.5Gb/s 16-QAM-encoded real-time OOFDM signals over the DML-based IMDD OM1 MMF system illustrated in Fig. 5.4. The performance and stability of the channel estimation technique at 3Gb/s net bit rate has been presented in detail in [1]. All the experimental measurements presented in this section are based on an optimised DFB bias current of 37mA, which gives an optical output power of -4.2dBm.
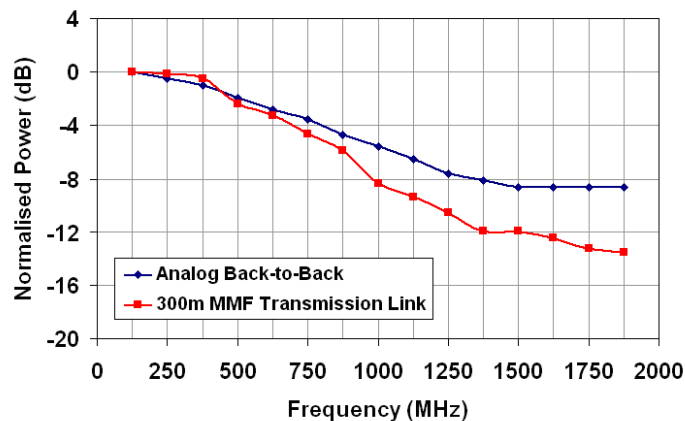

Fig. 5.5 Measured system frequency responses for analogue back-to-back and 300m MMF transmission link configuration.

5.2.3.1 Effectiveness of the 3-Level Variable Power Loading Scheme

When equal power loading is employed, such that all subcarriers have identical amplitudes in the transmitter, an unacceptable total channel BER is measured that is worse than 1.0×10^{-2}. This is due to the severe roll-off in the subcarrier amplitudes in the receiver, as discussed in detail later in this section. In order to implement a variable power loading scheme to compensate for the subcarrier amplitude roll-off effect, it is essential that the system frequency response is first determined as this is directly related to the received subcarrier power variation.

The measured frequency responses of the transmission systems from the IFFT input in the transmitter to the FFT output in the receiver are shown in Fig. 5.5 for two different scenarios: a) a transmission system with the 300m OM1 MMF being considered, and b) an analogue back-to-back case, where the electrical attenuator in the transmitter is directly connected to the low-pass filter in the receiver, such that point *A* is connected to point *D* in Fig. 5.4. In obtaining Fig. 5.5, equal digital subcarrier amplitudes in the transmitter are applied, and the resulting system frequency responses are normalised to the first subcarrier power. It can be seen from Fig. 5.5 that the system frequency responses decay very rapidly within the signal spectral region from 0.125GHz to 1.875GHz. Comparisons between the curves for these two frequency responses imply that the system frequency response roll-off effect is mainly due to effects of the analogue electrical elements including, for example, DAC output filtering and the sin(x)/x response inherent to a zero-order hold DAC output, as the associated digital electronics have flat frequency responses. In addition, as demonstrated in Fig. 5.5, the inclusion of optical components in the transmission system further decreases the frequency response in the high frequency region. The 300m MMF employed is the major contributor to the optical component-induced frequency response roll-off effect, as both the DFB modulation bandwidth and the PIN bandwidth are much larger than that corresponding to the 300m MMF. The observed rapid system frequency response roll-off effect indicates that the use of variable power loading can be critical for achieving acceptable BERs over all subcarriers.

In the 300m MMF transmission system, the implementation and effectiveness of the variable power loading scheme are explored in Fig. 5.6, where the received digital subcarrier amplitudes prior to channel equalization are plotted against subcarrier number

for the cases of utilising equal power loading and variable power loading. In Fig. 5.6, the variable power-loaded digital subcarrier amplitudes in the transmitter are also given, together with the relative error bits defined as a percentage ratio between the total number of detected error bits on a specific subcarrier and the corresponding total number of error bits aggregated over the entire transmission channel.
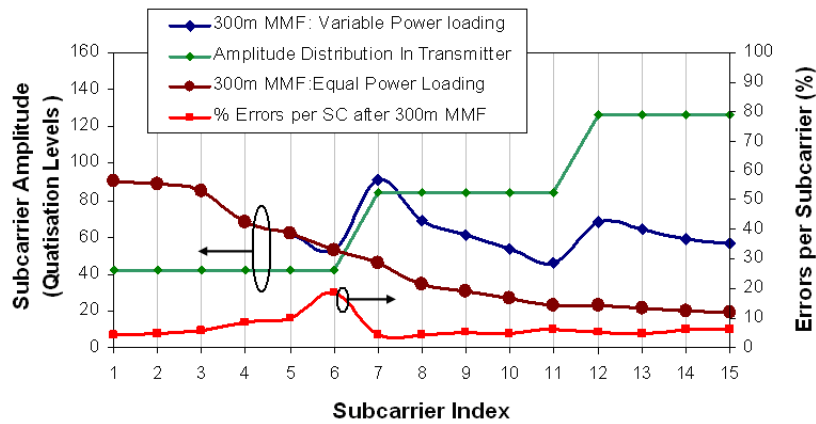
Fig. 5.6 Received subcarrier amplitudes for equal power loading and variable power loading. Variable power-loaded subcarrier amplitudes in the transmitter and their corresponding relative error bits after transmitting through a 300m MMF are also shown.
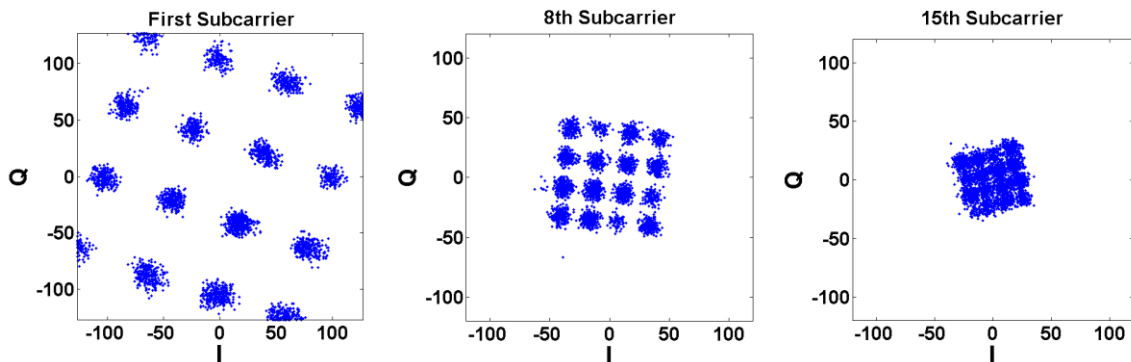
Fig. 5.7 Constellations of different subcarriers of real-time 6Gb/s 16-QAM-encoded OOFDM signals with equal power loading after transmitting through a 300m MMF. The measured total channel BER is approximately 1.0×10-2.

It can be seen in Fig. 5.6 that, for equal power loading, the received digital subcarrier amplitudes are very similar to the system frequency response presented in Fig. 5.5, thus resulting in significant amplitude differences between the low and high frequency subcarriers. As a direct result, the complex values of the low frequency subcarriers at the output of the FFT may overflow the range of the 8-bit signed value, whilst the constellation points of the high frequency subcarriers may start to merge together. The severity of the

above-mentioned phenomena can be easily understood by examining Fig. 5.7, where the constellations recorded before channel equalization in the receiver are shown for the 1st, 8th and 15th subcarriers. In such a case, the measured total channel BER is worse than 1.0×10^{-2}.
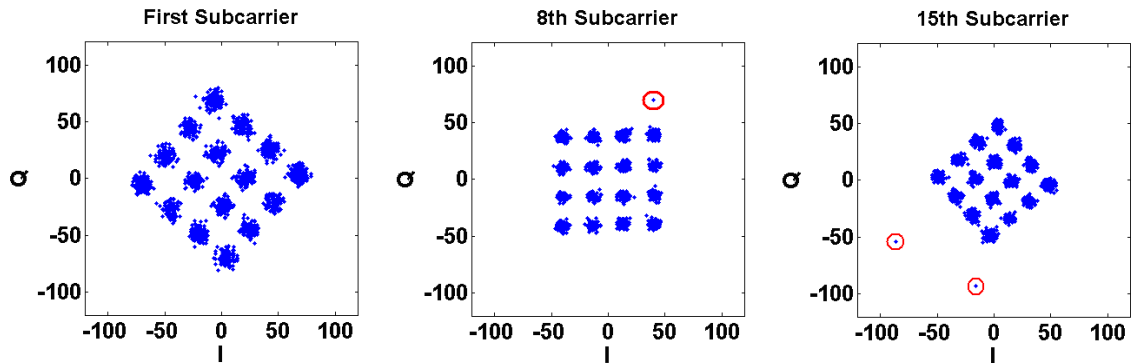
Fig. 5.8 Constellations of different subcarriers of real-time 6Gb/s 16-QAM-encoded OOFDM signals with the optimised three-level variable power loading scheme after transmitting through a 300m MMF. The measured total channel BER is $3.4 \times 10-4$. Spurious constellation points are circled in red.

In sharp contrast, experimental measurements show that the total channel BER can be reduced significantly to a value as low as 3.4×10^{-4} when use is made of a variable power loading scheme, which just consists of three discrete power levels, as seen in Fig. 5.6. For a specific transmission system, the subcarrier amplitude at each level is adjusted to ensure that similar error bits occur over different subcarriers and the total channel BER is also minimised simultaneously. As shown in Fig. 5.6, the optimised stair-like subcarrier amplitude distribution in the transmitter brings about a reduced variation in received subcarrier amplitude, and more importantly, an almost uniform distribution of relative error bits over different subcarriers. The resulting constellations recorded prior to channel equalisation (corresponding to a total channel BER of 3.4×10^{-4}) for the 1st, 8th and 15th subcarriers are given in Fig. 5.8, in which clearly distinguishable constellations are observed. The above analysis indicate that variable power loading is very effective in compensating for the system frequency response roll-off effect, and that the use of a coarse variable power loading scheme with just three power levels is sufficiently accurate for the implemented system discussed here.

5.2.3.2 Transmission Performance of 7.5Gb/s Real-time OOFDM Signals

Based on the optimised three-level variable power loading scheme, real-time end-to-end transmission of 7.5Gb/s 16-QAM-encoded OOFDM signals is achieved experimentally over a 300m OM1 MMF IMDD system involving a DML. Fig. 5.9 shows the corresponding total channel BER performance for both the 300m MMF system and the optical back-to-back configuration.

It is shown in Fig. 5.9 that, for the optical back-to-back configuration, a minimum BER of 3.3×10^{-4} is obtainable at a received optical power of -7.2dBm and that for the case of 300m MMF transmission, a minimum BER of 3.4×10^{-4} is obtainable at a received optical power of -7.7dBm. At a BER of 1.0×10^{-3} a power penalty of ~ 0.5dB is observed, mainly resulting from the differential mode delay (DMD) effect [2] and the modal noise effect [3]. In comparison with the performance of real-time 3Gb/s DQPSK-encoded OOFDM signals over 500m MMFs presented in section 4.2.4 and reported in [4,5], here the minimum received optical power required for achieving a BER of 1.0×10^{-3} is increased by ~5.5dB, and the power penalty is decreased by 3.5dB. The increase in received optical power is to satisfy the higher modulation format-induced increase in SNR, the increase in optical power is in excellent agreement with the theoretical prediction [15]. The reduction in power penalty arises from the decrease in the DMD effect due to the shorter transmission distance [6].
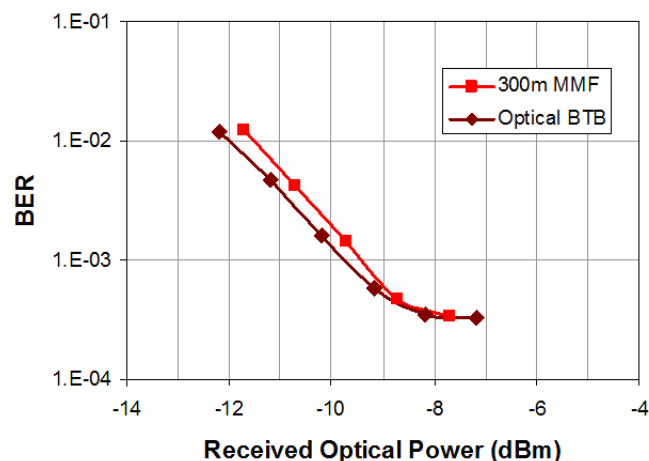
Fig. 5.9 BER performance of real-time 6Gb/s 16-QAM-encoded OOFDM signal transmission over a 300m MMF and a back-to-back link configuration.

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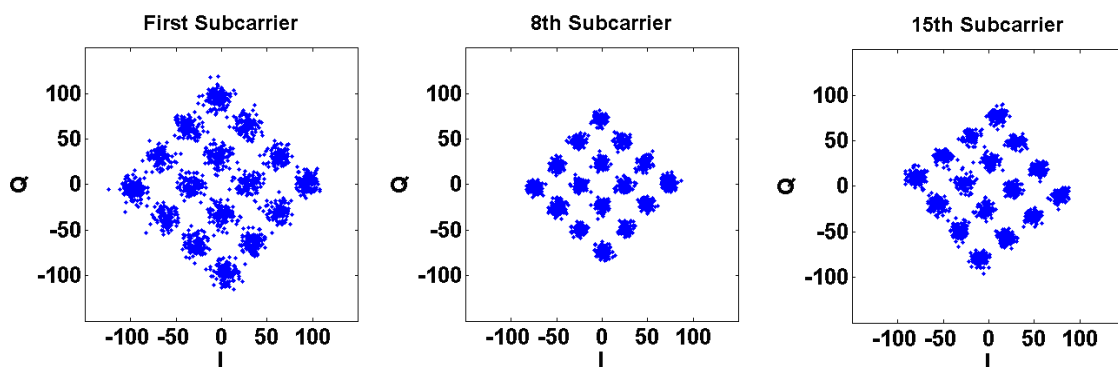
Fig. 5.10 Optical back-to-back constellations of different 16-QAM-encoded subcarriers before equalisation at a net signal bit rate of 6Gb/s and total channel BER of 1×10^{-3}.
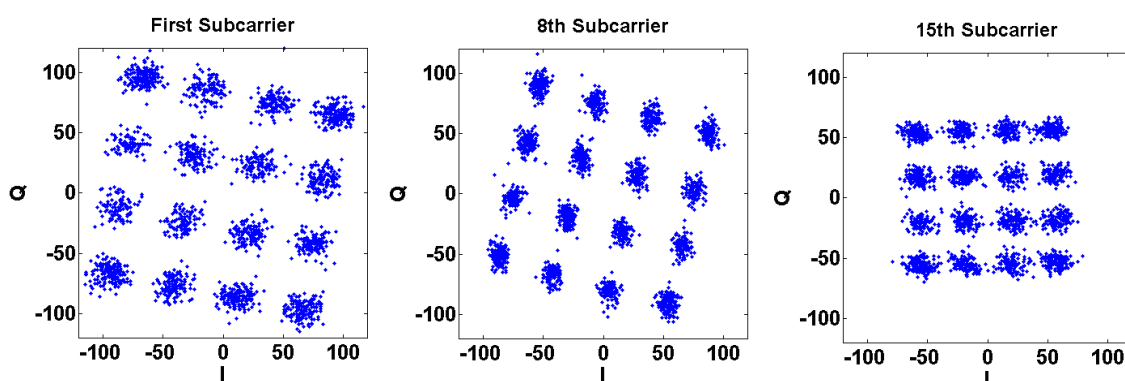
Fig. 5.11 300m MMF transmission constellations of different 16-QAM-encoded subcarriers before equalisation at a net signal bit rate of 6Gb/s and total channel BER of $1x10^{-3}$.

The corresponding received constellations measured before conducting channel equalization at a BER of 1.0×10^{-3} for the 1st, 8th and 15th subcarriers are shown in Fig. 5.10 and Fig. 5.11 for the optical back-to-back and 300m MMF cases, respectively. In Fig. 5.10, the first subcarrier constellations are the worst, this originates mainly from subcarrier intermixing-induced signal spectral distortions in the vicinity of the optical carrier upon direct detection in the receiver [7].

It is also observed in Fig. 5.9 that error floors exist for both considered cases. This is mainly due to the existence of spurious constellation points, which are circled in red in Fig. 5.8. Based on the measured constellations of the subcarriers shown in Fig. 5.8, a BER of $<3.0x10^{-5}$ is calculated if the red-circled spurious points are removed. These spurious points may arise due to timing irregularities in the ADC interface, as a BER of zero is obtainable in a digital back-to-back configuration where transmitter and receiver FPGA's

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are directly connected, and very similar minimum BERs are observed in the analogue back-to-back configuration compared to the optical back-to-back case.

5.3 11.25Gb/s Real-time OOFDM Transmission over 25km SMF and 500m MMF using Enhanced Adaptive Power Loading

5.3.1 OOFDM Transceiver Architecture for 11.25Gb/s

Fig. *5.12* shows the detailed architectures of the real-time 11.25Gb/s OOFDM transmitter (top) and receiver (bottom) implemented in the FPGAs, key transceiver parameters are also summarised in table 5.1. The transceiver architectures employing real-time DSP for IFFT/FFT algorithms, channel estimation, symbol synchronization, on-line performance monitoring and live parameter optimization, are based on those of the 7.5Gb/s transceiver design described in section 5.2.1, with modifications made in the following three aspects: 1) The subcarrier encoding in the transmitter and decoding in the receiver use 64-QAM modulation; 2) An advanced adaptive power loading technique in the transmitter is incorporated, which supports, in addition to the live common gain control for all subcarriers, live control of each individual subcarrier amplitude; 3) Analogue noise coupled into the digital-to-analogue converter and analogue-to-digital converter (DAC/ADC) is reduced. As detailed descriptions of the 7.5Gb/s real-time transceiver architectures have been presented in section 5.2.1, this section outlines the details of the DSP architecture design changes for increasing line rate to 11.25Gb/s. The new functional blocks and the modified blocks are highlighted in yellow and orange respectively in Fig. *5.12*. Again the system clock frequencies are maintained at 100MHz for both the transmitter and receiver FPGAs and 2GHz for the 4GS/s DAC and ADC, the clocks are generated from a common reference source as in all previous designs.

In the transmitter FPGA, the parallel data generator, pilot generator and pilot insertion blocks are adapted to support 64-QAM encoded subcarriers which encode 6 bits per symbol. An 84 bit wide pseudo random data sequence, of length 88,500 words, and a fixed 6 bit wide pilot data pattern, is combined into the data sequence, to generate 90 bits for each OFDM symbol containing 15 information-bearing subcarriers in the positive frequency bins. The pilot data sequence is employed for pilot subcarrier assisted channel

estimation as described in sections 5.2.1.1 and 5.2.1.4. Similarly, in the receiver FPGA, the parallel data generator and BER analyser blocks are also modified to accommodate the 90 parallel bits per symbol. The BER analyser continuously counts errors every 88,500 symbols, which corresponds to the total test pattern length of 7,965,000 bits in the 11.25Gb/s transceiver design.
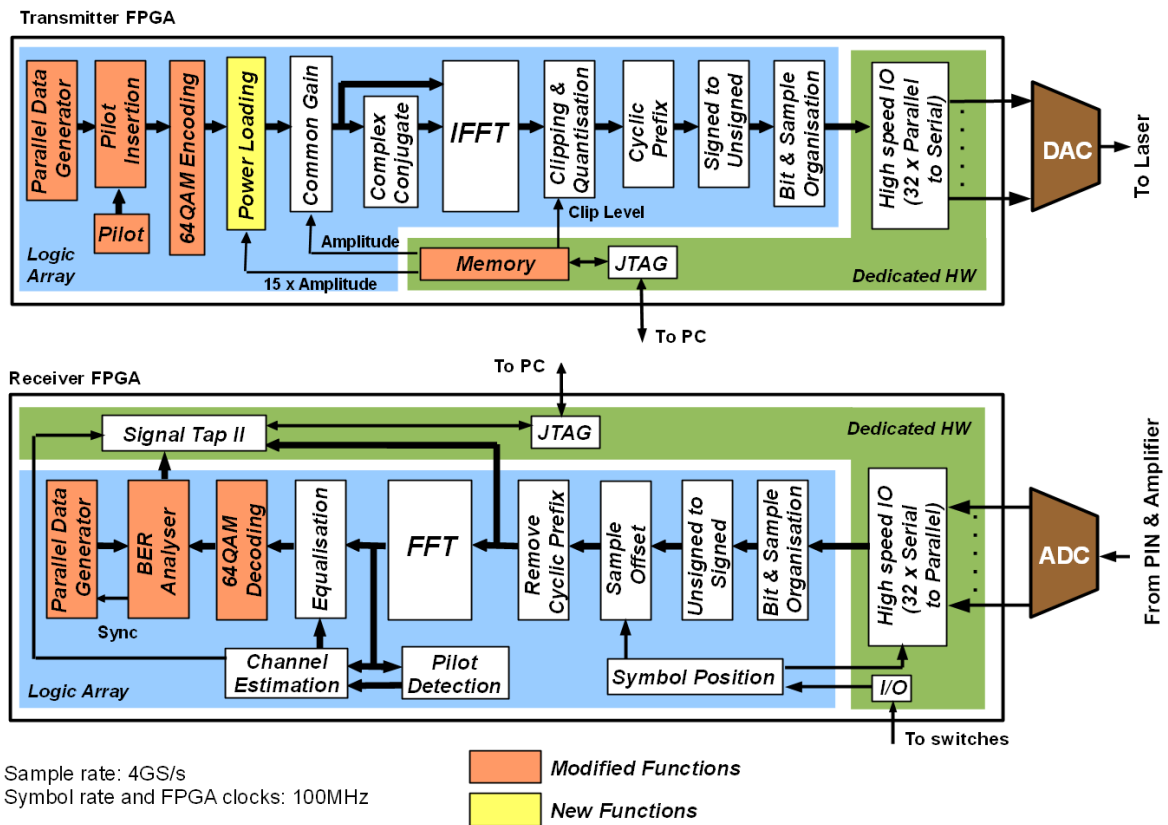
Fig. 5.12 Real-time OOFDM Transceiver Architecture for 9Gb/s net bit rate

The adaptive power loading function in the transmitter, as defined in section 2.4.4, is significantly improved to support increased resolution of individual subcarrier power levels combined with live adjustment. The 64-QAM encoder blocks are modified to include individual subcarrier gain control in addition to the common gain control as shown in Fig. 5.13. The individual gain factors for each of the 15 encoders are provided by an embedded memory cell which can be edited online. The finer control allows the subcarrier power to be set more closely to the ideal power level as defined by Eq. (2.40) for the corresponding CTF. The live adjustment feature allows iterative fine adjustment based on measured individual subcarrier BERs. It should be noted that the subcarrier power levels defined by Eq. (2.40) are for CTF roll-off compensation only. However, other effects such

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as ICI and subcarrier intermixing can lead to an effective decrease in a subcarrier's SNR thus making the optimum subcarrier amplitudes deviate to some extent from those defined by Eq. (2.40). The unwanted noise effects cannot be accurately predetermined so iterative power loading profile adjustment allows the optimum subcarrier power levels to be determined. For initial experimentation manual power loading profile adjustment is used, however a practical OOFDM transceiver would employ an automatic loading algorithm [8].
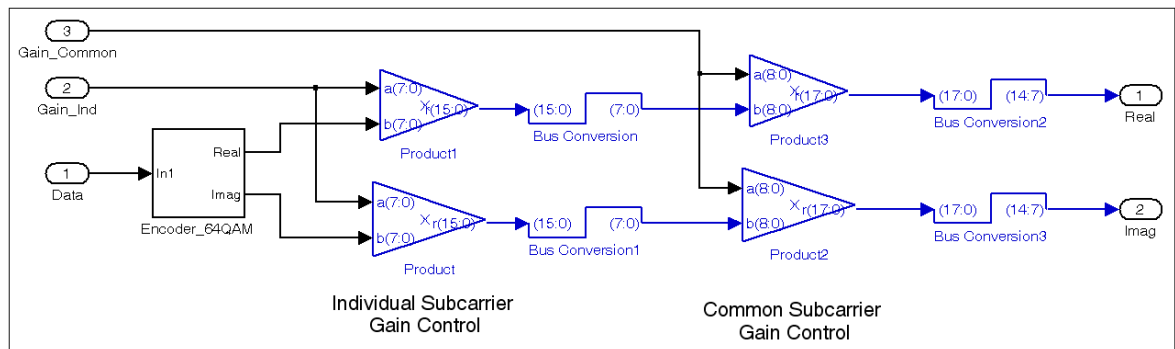
Fig. 5.13 64-QAM Encoder Block Incorporating Individual and Common Subcarrier Gain Control

Table 5.1. *Transceiver and System Parameters*

Parameter	Value
Total number of IFFT/FFT points	32
Data-carrying subcarriers	15
n-th subcarrier frequency	$n \times 125$MHz
Modulation format on all subcarriers	64-QAM
DAC & ADC sample rate	4GS/s
DAC & ADC resolution	8 bits
Symbol rate	100MHz
Samples per symbol (IFFT)	32 samples (8ns)
Cyclic prefix	8 samples (2ns)
Total samples per symbol	40 samples (10ns)
Error count period	88,500 symbols (7965000bits)
Raw signal bit rate	11.25Gb/s
Net signal bit rate (cyclic prefix 25%)	9Gb/s
DFB laser wavelength	1550nm
DFB laser modulation bandwidth	10GHz
DFB laser bias current	36mA(SMF) , 38mA (MMF)
DFB laser driving voltage	400mVpp(SMF), 650mVpp(MMF)
EDFA output power	10dBm
PIN detector bandwidth	12GHz
PIN detector sensitivity	-17dBm[a]
RF amplifier gain (3dB bandwidth)	20dB (2.5GHz)
Low pass filter bandwidth (3dB)	2.4GHz
SSMF dispersion parameter at 1550nm	18ps/(nm·km)
MetroCor™ dispersion parameter at 1550nm	-7.6 ps/(nm·km)
OM2 MMF attenuation	~0.25 dB/km

[a] Corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}

Each of the 15 complex subcarriers generated by the 64-QAM encoding block have peak real and imaginary values of ± 7, this is the smallest amplitude achievable for the 8×8 point constellation due to the digital quantisation. To adjust subcarrier power in the transmitter the adaptive power loading block provides a separate complex multiplier function for each subcarrier with the associated multiplication factors derived from dedicated internal memory locations. The multiplication factors can therefore be updated on-line using the Quatrus II memory content editor function. The multiplication factors are integer scalar values in the range 1 to 18, thus each subcarrier power can be set to one of 18 possible values. The upper limit of 18 is a result of the scaled subcarriers' real and imaginary parts being restricted to 8 bits signed values. The peak amplitudes of the real and imaginary subcarrier components at the output of the adaptive power loading block can therefore be set to 7,14,21,...,126. The independent control of individual subcarrier amplitude combined with the common subcarrier gain control block therefore allows live adaptation of the power loading profile and total signal power for rapid performance optimisation as described in section 5.3.2.1.

In the receiver FPGA all functional blocks are similar to those in the 7.5Gb/s design expect, as previously described, the parallel data generator and BER analyser are updated for 84 bit wide data. Also the decoder block is modified to support 64-QAM. It is important to note that the pilot detection, channel estimation and equalisation functions do not need modifying as the design is modulation format independent if only QAM formats are used. This is because the pilot subcarriers are based on the same peak amplitude constellation points regardless of actual modulation format. The symbol alignment in the receiver is performed manually following the procedure described in sections 3.5.3.3 and 3.5.4.3.

It should be noted that the 11.25Gb/s receiver logic design is 82% larger than the corresponding transmitter logic design, this is mainly due to the channel estimation, symbol alignment and BER measurement functions.

It can be easily derived that, at a the symbol rate of 100MHz and sample rate of 4GS/s, the 64-QAM-encoded OOFDM signal has a raw signal bit rate of 11.25Gb/s which corresponds to an electrical spectral efficiency as high as 5.625bit/s/Hz. For achieving a specific OOFDM transmission capacity, a high electrical spectral efficiency considerably

relaxes the bandwidth requirements of key components such as DACs/ADCs and DMLs. As a 25% cyclic prefix (2ns) is utilised here, the net signal bit rate is 9Gb/s. The use of a shorter cyclic prefix (if it can be tolerated) gives a higher net data rate. For example, a 12.5% cyclic prefix (1ns) results in a net signal bit rate of 10.125Gb/s.

5.3.2 Experimental System Setups for 11.25Gb/s over 25km SMF and 500m MMF

Fig. 5.14 and Fig. 5.15 show the experimental system setups for real-time OOFDM transmission over 25km SMF and 500m MMF respectively. Key system parameters are also listed in Table 5.1.
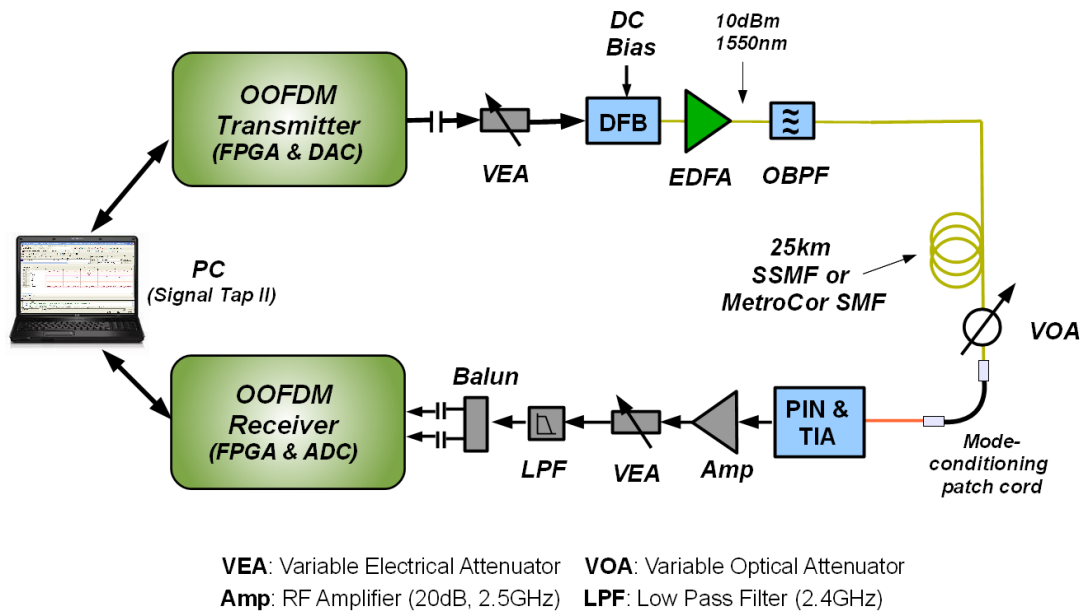
Fig. 5.14 Real-Time OOFDM Experimental System Setup for 11.25 Gb/s line rate over 25km SSMF & MetroCor^{TM} SMF

Firstly considering the 11.25Gb/s OOFDM system setup for the 25km SMF illustrated in Fig. 5.14**.** The power level of the analogue electrical signal from the OOFDM transmitter's DAC is optimised by a variable electrical attenuator before directly driving, in combination with an adjustable bias current, the 1550nm DFB laser. The output of the DFB laser biased at an optimum current of 36mA is -4.7dBm, which is boosted to 10dBm by a variable gain erbium doped fibre amplifier (EDFA). The optical signal is then band-pass filtered to minimise ASE noise before being injected, at an optical launch power of 7dBm, into a 25km standard SMF (SSMF) or MetroCor™ SMF link. It should be noted that the use of

the EDFA is to optimise the optical launch power level. As cost-effectiveness is critical for the considered applications a DML with sufficient output power would be used in a practice.

In the receiver, the received optical signal first passes through a variable optical attenuator (VOA) to control the received optical power, and is then coupled into a MMF pigtailed 12GHz linear PIN detector with TIA. The electrical output from the PIN is amplified by a fixed 20dB gain RF amplifier plus a variable electrical attenuator to allow the optimisation of the electrical signal power level in preparation for digitisation. The electrical signal is then low-pass filtered and converted to a differential signal before digitisation by the 8 bit, 4GS/s ADC in the OOFDM receiver.
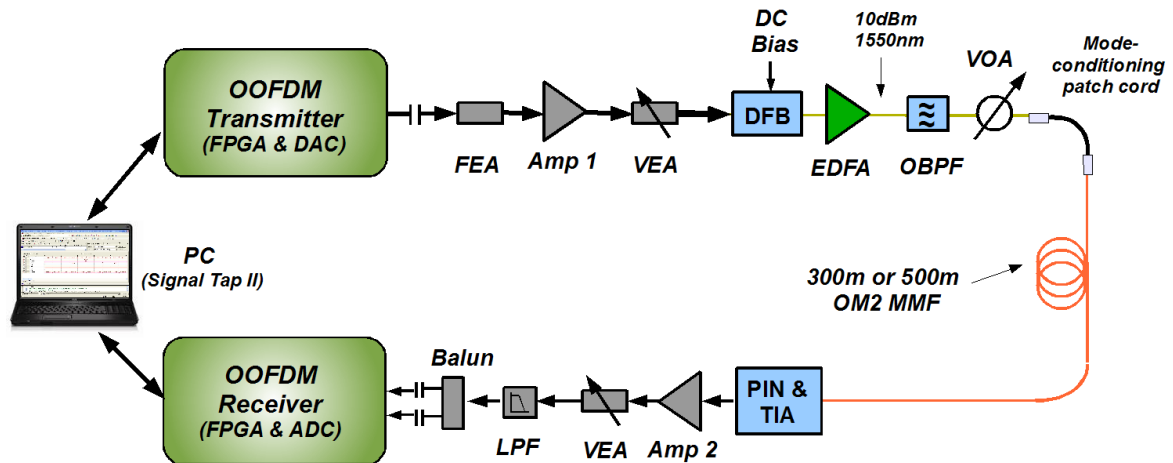
VEA: Variable Electrical Attenuator   FEA: Fixed Electrical Attenuator   OBPF: Optical Bandpass Filter
Amp 1: RF Amplifier (25dB, 4.2GHz) Amp 2: RF Amplifier (20dB, 2.5GHz) LPF: Low Pass Filter (2.4GHz)
VOA: Variable Optical Attenuator

Fig. 5.15 Real-Time OOFDM Experimental System Setup for 11.25 GB/s line rate over 500m OM2 MMF

Considering the 11.25Gb/s OOFDM system setup for the 500m MMF as illustrated in Fig. 5.15, this is similar to the setup for 25km SMF, except that the SMF is replaced by the MMF and the VOA and mode conditioning patch cord must be placed at the transmitter side as the VOA must interface to SMF fibers. Also an RF amplifier is included at the transmitter side before the DFB to increase the maximum driving voltage, a fixed electrical attenuator was required at the RF amplifier's input to avoid exceeding the maximum input voltage, a suitable value is found to be 5dB.

5.3.3. Experimental Results at 11.25Gb/s over 25km SSMF and MetroCor™ SMF

To explore the impairments of the different system elements including, digital electrical components, analogue electrical components, optical components and types of fiber on the performance of the developed real-time OOFDM transceivers at the increased operating rate of 11.25Gb/s, detailed performance analyses are undertaken for four different system configurations described below with reference to Fig. *5.14*.

- Case I. Digital back-to-back: The digital output of the transmitter FPGA is directly connected to the digital input of the receiver FPGA.
- Case II. Analogue back-to-back: The DAC output in the transmitter is directly connected to the electrical attenuator input in the receiver.
- Case III. Optical back-to-back: The optical band-pass filter output is directly connected to the variable optical attenuator input.
- Case IV. 25km links of SSMF and MetroCor™ SMF: This represents the entire transmission system.

5.3.3.1. Adaptive Power Loading Scheme

For the aforementioned various system configurations, the associated system frequency responses are shown in Fig. 5.16, which are measured on-line at the subcarrier frequencies as the effective power loss from the input of the IFFT in the transmitter to the output of the FFT in the receiver and subsequently normalised to the first subcarrier power. The case I system frequency response is not plotted in Fig. 5.16, since it exhibits, as expected, a flat system frequency response. Very similar to that observed in [9,10], case II has a power roll-off of approximately 8dB from the first to last subcarrier, as shown in Fig. 5.16. This is a direct result of the on-chip filtering in the DAC and its inherent sin(x)/x response. Whilst case III has a power roll-off of approximately 11dB over the same signal spectral region. Compared to case II, the extra 3dB power roll-off in case III is due to the frequency chirp associated with the employed DML [11]. It is also very interesting to note that, in case IV, the system frequency responses of the 25km SSMF link and the 25km MetroCor™ link occur at different sides of the case III response, this is because chromatic dispersion of SSMF (MetroCor™ SMF) has an identical (opposite) sign compared to that

corresponding to the DML frequency chirp, thus giving rise to the enhanced (reduced) chromatic dispersion effect [12].
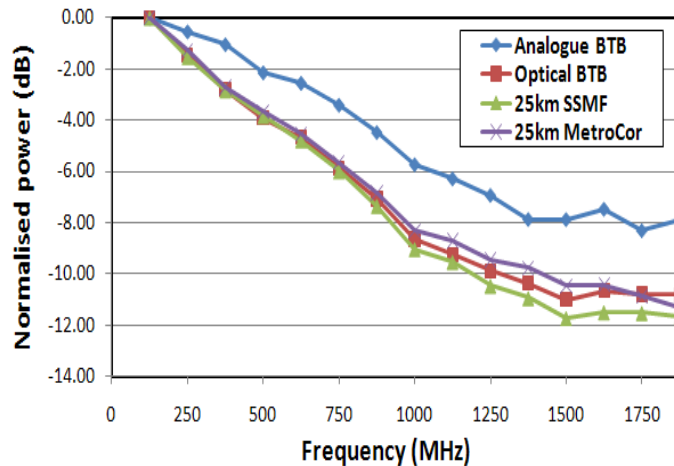
Fig. 5.16 System frequency responses for various system configurations.

The total 12dB power roll-off in case IV within the signal spectral region observed in Fig. 5.16 means that, if equal subcarrier power is applied in the transmitter, a large variation in the received subcarrier powers in the receiver will occur, thus leading to an unacceptably high total channel BER. However, by using adaptive power loading in the transmitter, the system frequency response roll-off effect can be pre-compensated. The effectiveness of such a technique is examined in Fig. 5.17, where the normalised loaded subcarrier power distribution in the transmitter is presented for the various system configurations, together with the corresponding normalised received subcarrier power distributions in the receiver.

To gain an in-depth understanding of the physical mechanisms underpinning the resulting loaded/received subcarrier power behaviours shown in Fig. 5.17, discussions are first made of the implementation of the adaptive power loading technique in the real-time OOFDM transceivers. The encoded electrical signal amplitude at the output of each of the 15 64-QAM encoders has the same peak value, *A,* to which two independent multiplication operations, denoted here as $\hat{p}_i$ and $\hat{G}_{com}$, are subsequently applied, here $\hat{p}_i$ represents the multiplication by an on-line controlled individual gain factor, P_i, of the *i*-th subcarrier amplitude; and $\hat{G}_{com}$ represents the multiplication by an on-line controlled common gain factor, G_{com}, of all subcarrier amplitudes. After these two operations, the *i*-th subcarrier has a peak amplitude of AP_iG_{com}. Clearly, the loaded subcarrier power profile is

determined by P_i. The use of the common gain factor, G_{com} is to adjust the amplitudes of all the subcarriers simultaneously to ensure that the 32 complex signal values at the input of the IFFT are set at an optimum level. Generally speaking, for achieving the highest calculation precision, the signal level should be as high as possible. However, if the signal level exceeds a specific threshold, internal IFFT parameters can overflow their assigned ranges. To determine an optimum loaded subcarrier power profile for a given system, the initial step is to use an on-line measured system frequency response to estimate the loaded subcarrier powers required for achieving equal subcarrier powers in the receiver. Making use of such an estimated profile, the BER distribution across all the subcarriers is then

Fig. 5.17 Transmitted and received subcarrier power levels for various system configurations.
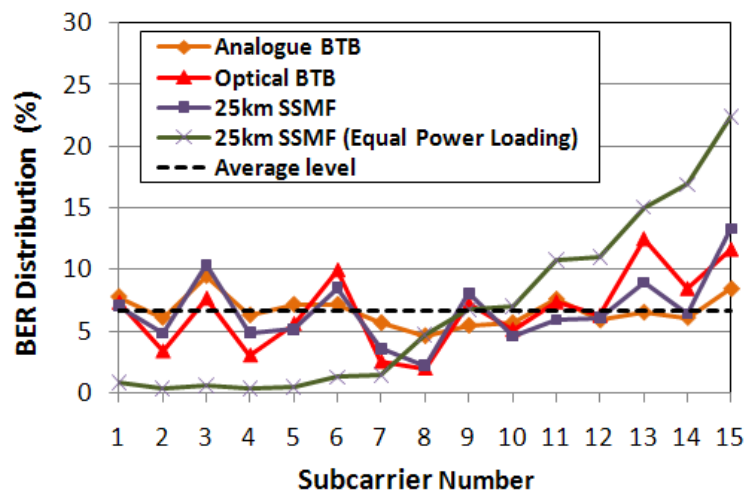
Fig. 5.18 Subcarrier error distribution for various system configurations with adaptive power loading (Total BER ~$8x10^{-4}$). For comparison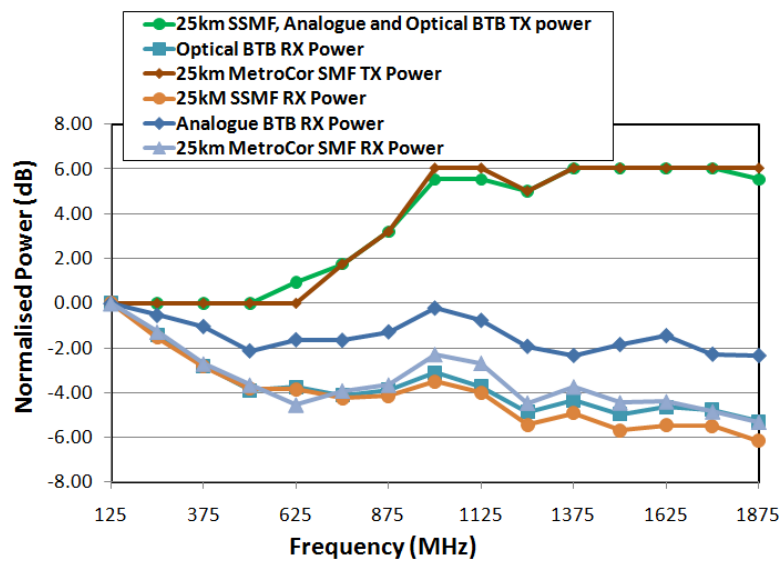s, the error distribution with equal power loading is also plotted for case IV with a 25km SSMF (Total BER=$8x10^{-3}$).

measured, based on which the loaded subcarrier power profile can be finely optimised on-line to evenly distribute errors across the subcarriers and simultaneously minimise the total channel BER. As an example, a representative optimised BER distribution across all the subcarriers is shown in Fig. 5.18 for various system configurations.

Having described how the adaptive power loading technique is implemented, attention is then focussed on discussing in detail the loaded and received subcarrier power behaviours observed in Fig. 5.17. It should be pointed out that, for fair comparisons in Fig. 5.17, the loaded subcarrier power distributions for case II and III are taken to be similar to that corresponding to case IV, where the loaded subcarrier power profile is optimised for the 25km SSMF. Comparisons between Fig. 5.17 and Fig. 5.16 indicate that, for a fixed loaded subcarrier power profile, the difference in the received subcarrier power profiles for the various system configurations considered corresponds to the difference in the corresponding system frequency responses.

In Fig. 5.17 the loaded (received) subcarrier power profile is seen to have three distinct regions: Region 1 corresponds to the first 4 subcarriers. Over such a region, the loaded subcarrier power level is flat and the received subcarrier power level decays almost linearly. The occurrence of such a power developing trend is due to the effect of direct photon detection-induced unwanted subcarrier intermixing. This effect introduces the strongest spectral distortions to the first subcarrier and relatively weakens for other subcarriers with higher frequencies [13]. This means that the low frequency subcarriers require higher powers to mitigate the effect. Here it is also worth addressing that, for the subcarriers in Region 1, the minimum loaded power level is also determined by the relative quantisation noise, as a reduction in loaded subcarrier power level causes an increase in quantisation noise. The next four subcarriers form Region 2, where the loaded subcarrier power level linearly increases, resulting from the steep decay in the system frequency response. Over such a region, the received subcarrier power level does not vary considerably, suggesting that the subcarrier intermixing effect is negligible. Finally, all the remaining subcarriers are located in Region 3, over which the loaded subcarrier power levels are virtually flat. This is because of two reasons: 1) Region 3 corresponds to a frequency range where the system frequency response roll-off is less steep, and 2) The maximum loaded subcarrier power level is determined by the dynamic power range of the IFFT.

It can also be seen in Fig. 5.17 that, for the received subcarrier power profiles in all the system configurations, there exist distinguishable subcarrier power peaks centred at the middle subcarriers. This can be explained by considering the effect of imperfect subcarrier orthogonality-induced inter-channel interference (ICI) [14]. Imperfect orthogonality between different subcarriers within a symbol arises due to the quasi-periodic structure of time domain OFDM symbols. The accumulation of the ICI effect brings about the strongest spectral distortions occurring over the middle subcarriers.

From the above analysis, it is clear that, for an optimum loaded subcarrier power profile, there still exists a residual roll-off in the received subcarrier power levels, as shown in Fig. 5.17. However, such a residual roll-off can be tolerated. This is confirmed in Fig. 5.18, in which the distribution of errors across the subcarriers is plotted for case II, III and IV with a 25km SSMF. The adaptive power loading technique can successfully achieve an acceptable total channel BER as shown in section 5.3.3.3, with the residual received subcarrier power roll-off as large as ~6dB (corresponding to a 12dB variation in frequency response) to give a resulting error distribution that varies by just ±5% from the average level as shown in Fig. 5.18. In comparison, when equal power loading is employed for case IV with a 25km SSMF, the error distribution increases rapidly for higher subcarrier frequencies, as shown in Fig. 5.18, and the corresponding total channel BER is increased to an unacceptable level of 8×10^{-3}.

5.3.2.2. Dependence of Optimum Clipping Ratio on Power Loading Profile

The discussion in section 5.3.2.1 indicates that, adaptive power loading is capable of offering, in an adaptive manner, an optimally loaded subcarrier power profile for a specific system frequency response. This raises a very interesting open question, i.e., whether or not a variation in the loaded subcarrier power profile also alters the signal clipping characteristics. The provision of an answer to the open question is crucial, as the transmission performance of high signal modulation format-encoded OOFDM signals is very sensitive to signal clipping [15-17].

The signal samples at the output of the IFFT prior to clipping are signed 12 bit values, which cover the range from -2048 to 2047. The level at which the signal is clipped, *C*, can thus be set to a value between 0 and 2047. If the unclipped signal is *S(t)*, the clipped signal $S_{clip}(t)$ is given by:

$$S_{clip}(t) = \begin{cases} S(t), & -C \leq S(t) \leq C \\ C, & S(t) > C \\ -C, & S(t) < -C \end{cases} \tag{5.4}$$
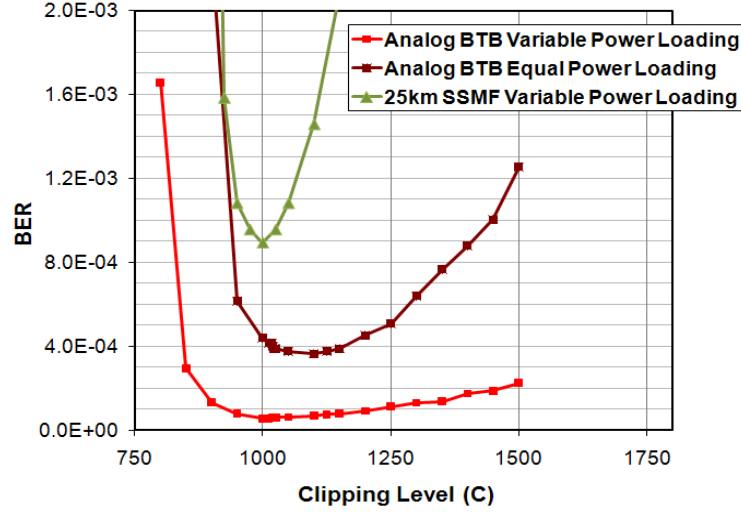
Fig. 5.19 Variation of BER with clipping level for an analogue back-to-back configuration (case II) and a 25km SSMF link (case IV).

Within the dynamic amplitude range of –C to +C, the clipped signal is then quantised to cover the signed 8 bit range from -128 to +127. The general definition of clipping ratio ξ in dB has a form of [16]

$$\xi(dB) = 10 \log_{10}\left[\frac{\Lambda}{P_m}\right] \tag{5.5}$$

where Λ is the maximum peak power of the clipped signal and P_m is the average signal power. To include the digital system parameters relevant to adaptive power loading in the ξ definition, Eq.(5.5) can be re-written in the following form

$$\xi(dB) = 10 \log_{10} \frac{C^2}{P_M (A \cdot G_{COM} \cdot G_{IFFT})^2 \sum_{i=1}^{15} P_i^2} \tag{5.6}$$

where P_M is the average power of the M modulation format-encoded signal with unit peak amplitude (here M is 64-QAM), G_{IFFT} is the gain factor representing signal scaling associated with the IFFT function. It can be seen from Eq.(5.6) that the optimum clipping ratio of a signal is dependent on the joint effect of the on-line variable parameters, which

include the clipping level C, the common gain factor G_{com} and the individual subcarrier gain factors P_i.

For fixed $G_{com,}$ and G_{IFFT} , as well as the loaded subcarrier power profile optimised for the 25km SSMF link shown in Fig. 5.17, the measured BER against clipping level C for case II and case IV is presented in Fig. 5.19 under the condition of adaptive power loading and also equal power loading for case II. The BER variation with C for the 25km SSMF link with equal power loading is not plotted, as the minimum BER is above an acceptable level. Fig. 5.19 shows that, for case II with equal power loading, the optimum clipping level is 1100, which, however, decreases to 1000 when adaptive power loading is adopted. These two optimum clipping levels of 1100 and 1000 correspond to signal clipping ratios of 12.2dB and 12.7dB, respectively, measured at the DAC output. This reveals that the optimum clipping ratio is dependent on the loaded subcarrier power profile and there is a significant variation in the clipping level C required to achieve the optimum clipping ratios.

For case IV with the 25km SSMF link, Fig. 5.19 shows that the optimum value of C is the same as for case II. However, the BER in case IV is more sensitive to C. This is because the optical signal also experiences additional optical noise and distortions, which make the optical signal less tolerant to both the increasing clipping distortion as C decreases below the optimum value and the increased quantisation noise as C increases above the optimum value. Experimental measurements also show that the optimum C value for case III and case IV with the MetroCor™ SMF is the same as for case IV with the SSMF link and case II, provided that the same loaded subcarrier power profile and G_{com} value are utilised.

5.3.3.3. Transmission Performance 11.25Gb/s Real-time OOFDM Signals

Making use of the optimum loaded subcarrier power profile and the corresponding optimum clipping setting, experimental measurements are undertaken of the transmission performance of 11.25Gb/s real-time 64-QAM-encoded OOFDM signals over DML-based IMDD systems without in-line optical amplification and dispersion compensation. In the experimental measurements, the 25km links of SSMF and MetroCor™ SMF are employed. For case III and case IV, the measured BER against received optical power is shown in Fig. 5.20. In obtaining Fig. 5.20, the electrical gain at the receiver is adjusted as the received optical power setting varies to maintain the electrical signal amplitude at the ADC

input at an optimum level. The minimum achieved BERs and the corresponding received optical powers at a BER of 1×10^{-3} are summarized in Table 5.2 for the different cases considered here.

Table 5.2. *11.25Gb/s real-time OOFDM transceiver performance*

Configuration	Minimum BER	Received optical power at BER=1.0×10^{-3}
Digital back-to-back	0	-
Analogue back-to-back	6.0×10^{-5}	-
Optical back-to-back	8.0×10^{-4}	-6.3dBm
25km SSMF link	8.50×10^{-4}	-6.0dBm
25km MetroCor™ link	8.80×10^{-4}	-6.5dBm

For case III, the transmission performance of real-time OOFDM signals is mainly limited by additive white Gaussian noise (AWGN). Over such a channel, by comparing the transmission performance of the present 64-QAM-encoded OOFDM signal with that corresponding to the 16-QAM-encoded signal having the same spectral bandwidth reported in section 5.2.2.2, it can be found that, 64-QAM modulation increases the minimum received optical power required for achieving a BER of 1.0×10^{-3} by approximately 4dB. Such an optical power increase is well in line with the theoretical prediction [16]. In addition, as shown in Fig. 5.20, the measured power penalty at a BER of 1×10^{-3} for the 25km SSMF is 0.3dB, whilst the power penalty for the 25km MetroCor™ SMF reduces to -0.2dB. The observation of negative power penalty is also in excellent agreement with the results obtained for a 3Gb/s real-time 16-QAM-encoded real-time OOFDM transceiver design, where a negative power penalty of -0.6dB was measured for a 25km MetroCor™ SMF [1]. Furthermore, similar results using numerical simulations reported in [18] have also verified the occurrence of positive and negative power penalties, depending upon the use of SSMFs and MetroCor™ SMFs, respectively, in the DML-based IMDD transmission systems. The physical origin of the observed power penalty characteristics is mainly attributed to the following two reasons: 1) the fibre chromatic dispersion-induced OOFDM phase shift cannot be preserved perfectly in the electrical domain owing to direct photon detection in the receiver. A MetroCor™ (SSMF) fibre has a negative (positive) dispersion parameter, which can compensate (enhance) the frequency chirp effect associated with the DML, thus leading to a reduced (enlarged) total phase shift of the received signal in the electrical domain; 2) the reduced (enlarged) phase shift also decreases (increases) the subcarrier intermixing effect upon direct detection.
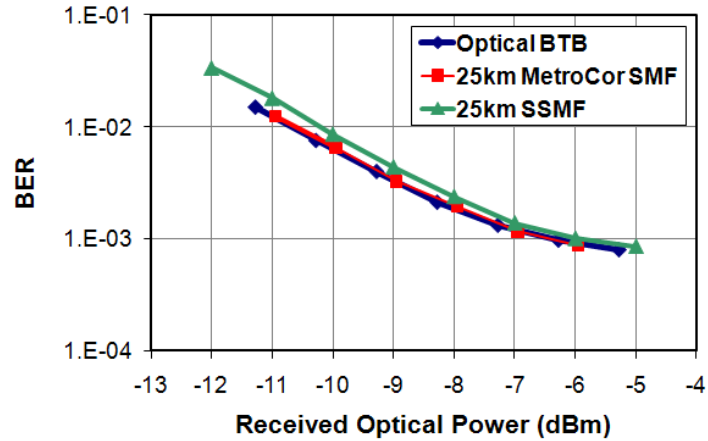
Fig. 5.20 BER performance of real-time 11.25Gb/s 64-QAM-encoded OOFDM signal transmission over 25km SSMF, 25km MetroCor™ SMF and optical back-to-back link configurations.

To explore the factors limiting the minimum achievable BERs shown in Fig. 5.20, representative constellations of single subcarriers, recorded prior to performing equalisation in the receiver, are presented in Fig. 5.21 for the various system configurations. Case I gives a zero BER as listed in Table 5.2, and the corresponding constellation presented in Fig. 5.21(a) shows very little deviation from the ideal case. Whilst in case II, the minimum BER increases to 6×10^{-5}, and the corresponding constellation plotted in Fig. 5.21(b) shows an increase in noise and distortion due to the non-ideal sampling, analogue noise and frequency response roll-off of the DAC and ADC. In case III the minimum BER increases approximately by one order of magnitude to 8.0×10^{-4}, and the corresponding constellation of the first subcarrier in Fig. 5.21(c) shows a significant increase in the noise content. Moreover, for case IV with two types of SMFs being employed, as seen in Fig. 5.20 and Table 5.2, the minimum BERs are very similar to that obtained in case III. Fig. 5.21(d-f) show the constellations for the 1st , 8th and 15th subcarriers for the 25km SSMF link, and Fig. 5.21(g-i) show similar constellations for the 25km MetroCor™ SMF link. Comparing Fig. 5.21(d) and Fig. 5.21(g) with Fig. 5.21(c) indicates clearly that there is little increase in the noise content. The received constellations for the SMF fibers in Fig. 5.21(d-i) also clearly show the residual roll-off in subcarrier amplitude with increasing subcarrier frequency.

All the aforementioned facts indicate that, in addition to the analogue electrical component-induced signal distortions, DML-induced signal waveform distortions and subcarrier intermixing upon direct photon detection in the receiver are major factors

limiting the minimum achievable total channel BER. To confirm the above statement, numerical simulations have been performed in [19]. It was shown that, based on numerical parameters identical to those adopted in the experimental system, the simulated minimum BERs agree very well with the experimental results. However, when the DML is replaced by an ideal intensity modulator with the DML-induced frequency chirp being included, a minimum BER as low as 6.0×10^{-5} is obtainable. On the other hand, a reduction in the subcarrier intermixing effect by padding zeros at all the subcarriers between subcarrier 1 and subcarrier 7, can lower the minimum total BER to $< 1.0 \times 10^{-4}$ for subcarriers 8 to 15 in
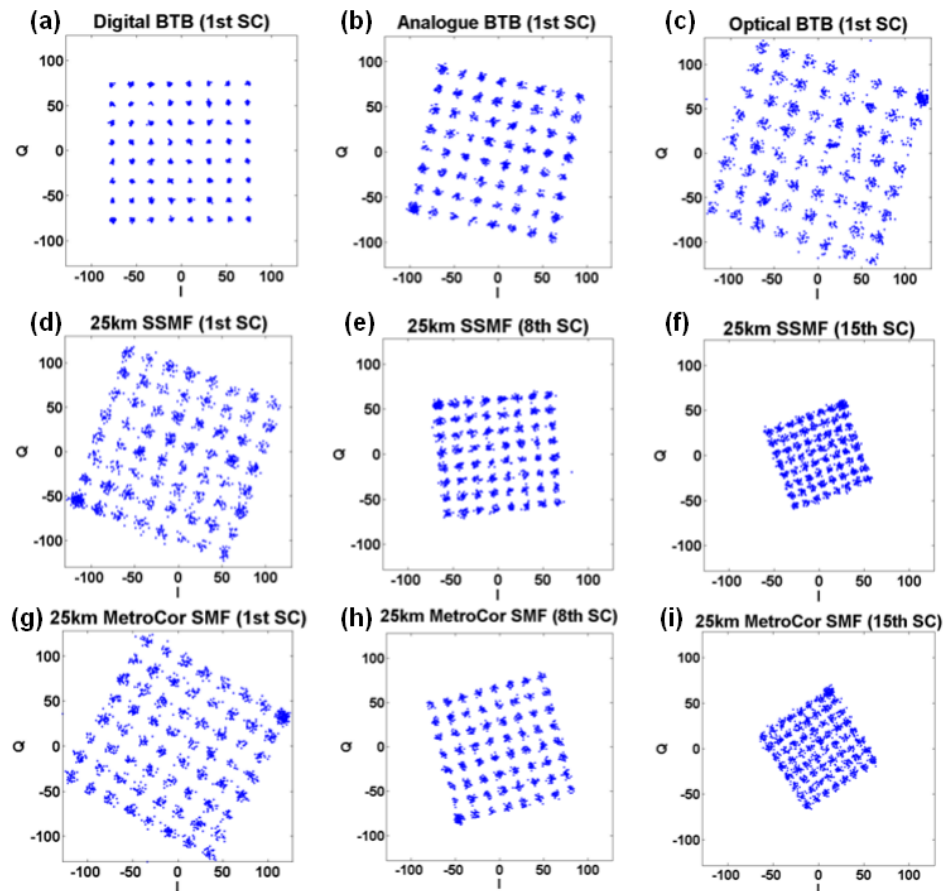
Fig. 5.21 Received constellations of a single subcarrier before equalisation (a) Digital back-to-back, total channel BER=0 (b) Analogue back-to-back, total channel BER=6.0x10-5 (c) Optical back-to-back, total channel BER=8.0x10-4 (d,e,f) 25km SSMF, total channel BER=8.5x10−4,(g,h,i) 25km MetroCor SMF, total channel BER = 8.8x10−4.

the present DML-based IMDD experimental system. The simulation results indicate that further system optimisation can still be made to provide a large BER margin for practical system implementation.

5.3.3.4 Effectiveness of Adaptive Power Loading

From previous discussions, it is clear that adaptive power loading is essential to allow the successful demonstration of the 11.25Gb/s real-time 64-QAM-encoded OOFDM transceivers. As an alternative to adaptive power loading, two other adaptive loading algorithms can also be employed to compensate the system frequency response roll-off. These alternative adaptive loading algorithms are bit loading and bit-power loading:

The bit-loading algorithm is characterised by the variation of modulation format on each subcarrier whilst maintaining the same fixed mean power level on all subcarriers. Each subcarrier can therefore be loaded with a varying number of bits. This is also known as adaptive modulation [20-23]. Generally speaking, a high (low) modulation format is used on a subcarrier suffering a low (high) attenuation.

In the bit-power loading algorithm both the modulation format and power level are varied on each subcarriers, this can be implemented for example by utilising a procedure reported in [24].

Comparisons between the three loading algorithms in OOFDM systems have been reported using numerical simulations in [19], using SMF-based IMDD links and in [25] using IMDD-based MMF links. Comparisons have also been performed experimentally using the real-time OOFDM transceivers and IMDD-based SSMF links in [26]. It should be noted that in [19] the theoretical model of the OOFDM transceiver employs parameters identical to those adopted in the real-time transceiver, including the DML and PIN detector. The simulations in [19] should therefore reliably predict the performance of the real-time system, evidence of this is the strong correlation between the power loading simulation results and experimental results for 25km SSMF. The comparisons in [19] show the simulated signal capacity versus reach performance for the three algorithms can support almost identical signal capacities for SSMF links of up to 100km. In particular, at 25km SSMF transmission, power loading can achieve 11.25Gb/s compared to 12.25Gb/s supported by power-bit loading. The results in [25] show that for MMF links of less than 300m, the simpler power-loading algorithm is just as effective (~93%) as the more complex power-bit loading algorithm for maximising the OOFDM MMF system capacity at a given transmission distance. The experimental results in [26] show that very similar signal capacity versus reach performance at 4GS/s is achieved for power-bit loading

(11.75Gb/s) and power-loading (11.25Gb/s) for SSMF links up to 25km, the difference becoming even lower for 35km SSMF.

Even though power-loading generally results in slightly lower transmission capacity compared to bit-loading and power-bit loading, it has been shown that the difference is not significant. This result is extremely important when the complexity of the different loading algorithms is considered as power-loading is far the simplest algorithm to implement, it has been shown in [26] that when considering FPGA logic resources the power loading-based design only requires ~1/3 of the recourses of the power-bit loading-based design. This leads to the conclusion that power-loading is a highly effective adaptive loading algorithm which can achieve high system performance whilst minimising transceiver cost through significantly reduced DSP complexity.

5.3.4. Experimental Results at 11.25Gb/s over 500m MMF

Fig. 5.22 shows the system frequency response of the 500m MMF system setup given in Fig. 5.15, which is measured from the input of the IFFT in the transmitter to the output of the FFT in the receiver. The response is normalised to the power of the first subcarrier at 125MHz. The observed ~11.5dB roll-off over the entire signal spectrum is mainly due to: 1) the on-chip output filtering of the DAC and its inherent sin(x)/x response, 2) the DMD effect. If all the transmitted subcarriers have equal powers in the transmitter, the received subcarrier power variation of ~11.5dB is too large to produce an acceptable total channel BER.
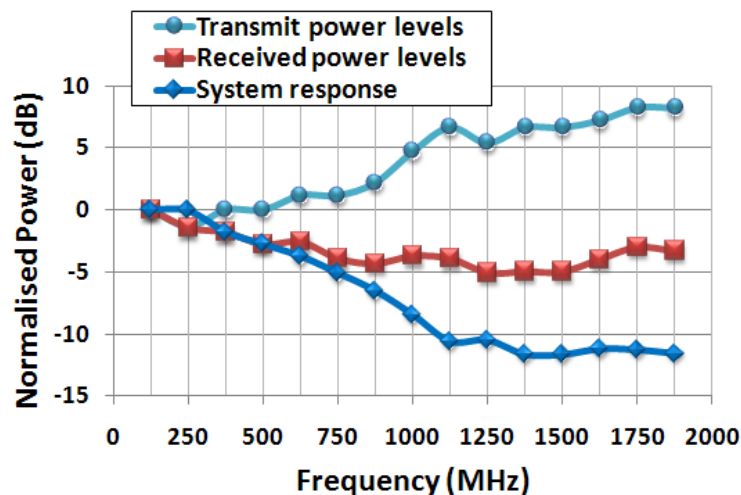
Fig. 5.22 Transmitted and received subcarrier powers and system frequency response for the 500m MMF system.
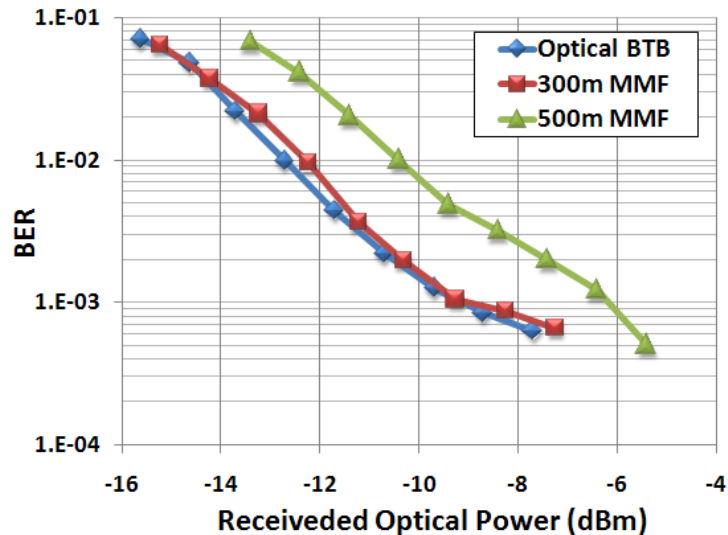
Fig. 5.23 BER performance of real-time 11.25-Gb/s 64-QAM-encoded OOFDM signal transmission over 300m and 500m MMF

To effectively compensate for the system frequency response roll-off effect, use is again made of the adaptive power loading technique described in section 5.3.1 and the procedure for optimising the power loading profile described in section 5.3.3.1. The resulting optimum power loading profile across all the subcarriers prior to the IFFT in the transmitter is shown in Fig. 5.22, where the corresponding received subcarrier power levels recorded immediately after the FFT in the receiver are also plotted. The received subcarrier powers vary within a range as small as 5dB and lead to an almost uniform error distribution across all the subcarriers. It should be noted that the optimum clipping level is also dependent upon adaptive power loading as detailed in section 5.3.2.2

Making use of the adaptive power loading profile illustrated in Fig. 5.22, the measured BER performance is shown in Fig. 5.23 for three different cases: optical back-to-back, a 300m MMF and a 500m MMF. For the 500m (300m) MMF link, a minimum BER of 4.5×10^{-4} (6.6×10^{-4}) is obtained, and the corresponding received constellations prior to channel estimation are plotted in Fig. 5.25 (Fig. 5.24) for the 1st, 8th and 15th subcarriers.

It can be seen in Fig. 5.23 that, for the 500m MMF link, the minimum received optical power required for achieving a BER of 1×10^{-3} is approximately -6.3dBm, implying that the optical power budget can be as high as 12dB when a typical 6dBm DFB laser is employed.

Fig. 5.23 also shows that, for the 300m MMF, the measured power penalty at a total channel BER of 1×10^{-3} is negligible, suggesting that the adopted cyclic prefix is

sufficiently long to completely compensate for the DMD effect associated with the link. However, when the transmission distance is increased to 500m, a power penalty of approximately 3dB occurs, which is attributed to the effects of long transmission distance-induced large DMDs. This indicates the ISI which results from the DMD effect is not fully compensated by the cyclic prefix.
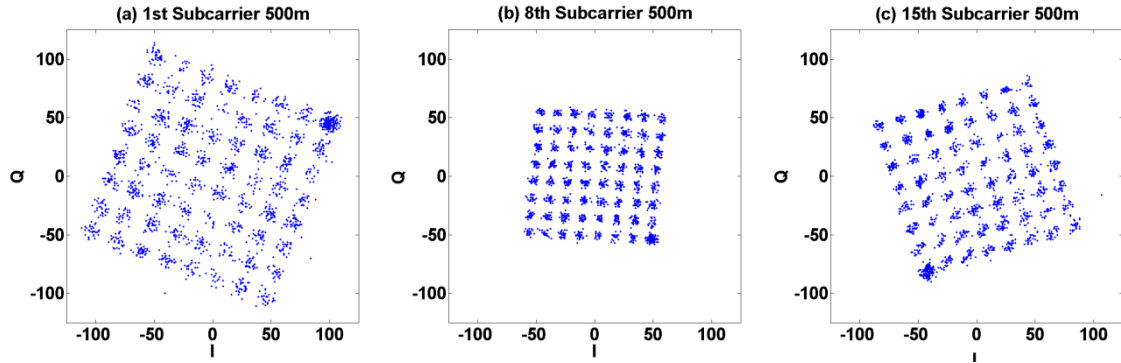
Fig. 5.24 Received subcarrier constellations before channel equalization after 500-m MMF transmission. (a) 1ˢᵗ Subcarrier, (b) 8th Subcarrier, (c) 15th Subcarrier.
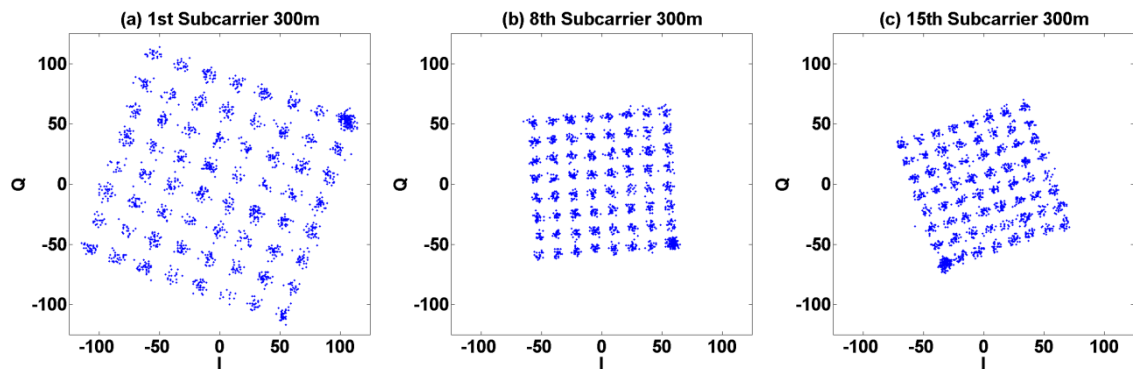
Fig. 5.25 Received subcarrier constellations before channel equalization after 300m MMF transmission. (a) 1ˢᵗ Subcarrier, (b) 8th Subcarrier, (c) 15th Subcarrier.

The modal noise effect is due to the spatial separation of the different modes propagating through the MMF, the interference of the different spatial modes causes a random distribution of the optical field intensity across a section of fiber [27]. Due to effects including variations in optical source wavelength, physical vibration of the fiber and temperature effects the optical field intensity distribution is unstable and changes slowly over time. Due to non-perfect alignment at fiber connectors and a small area PIN detector that cannot capture all the power over the entire fiber end surface, the changing intensity distribution results in changing power levels coupled across the connectors and finally onto the PIN detector's surface. The received optical power variation due to the modal noise

effect was observed in the 500m MMF system and manifested as a slow variation in the total channel BER. It would take several 10's minutes for a noticeable BER drift to occur which could then be correct by adjusting the receiver's electrical gain (or optical attenuation) accordingly. This indicates that automatic gain control can be used to compensate any drift in the received electrical signal level, and thus significantly minimise the modal noise effect. In the experimental investigations it is estimated that the modal noise effect contributes approximately 1dB power penalty for the 500m MMF, whilst for the 300m MMF the modal noise effect is negligible.

5.4 Conclusions

By adopting the pilot subcarrier-assisted channel estimation technique and implementing a simple three-level variable power loading scheme, 7.5Gb/s real-time FPGA-based OOFDM transceivers have been experimentally demonstrated. The transceivers also have crucial functionalities of on-line performance monitoring and live optimisation of key parameters including signal clipping, subcarrier power and DML operating conditions. It has been shown that variable power loading is an effective means of compensating for the rapid system frequency response roll-off effect. Real-time end-to-end transmission of a 7.5Gb/s 16-QAM-encoded OOFDM signal over a 300m OM1 MMF with a power penalty of 0.5dB and an electrical spectral efficiency of 3.75 bit/s/Hz has been successfully achieved in a DML-based IMDD system.

By further improving the OOFDM transceiver design 11.25Gb/s real-time OOFDM transceivers utilizing 64-QAM encoding/decoding and significantly improved adaptive power loading on each individual subcarrier have been experimentally demonstrated. The advanced transceiver functionalities of on-line performance monitoring, live system parameter optimization where again demonstrated to be highly effective for optimising system performance. Real-time end-to-end transmission of an 11.25Gb/s 64-QAM-encoded OOFDM signal with a high electrical spectral efficiency of 5.625bit/s/Hz has been successfully achieved over 25km of standard and MetroCor™ SMFs with respective power penalties of 0.3dB and -0.2dB at a BER of 1.0×10^{-3} in a DML-based IMDD system without in-line optical amplification and chromatic dispersion compensation.

Successfully breaking through the 10Gb/s barrier over 25km SMF, provides clear evidence that OOFDM has strong potential as an effective physical layer technology for next generation 10 Gigabit-PONs.

Real-time end-to-end transmission of an 11.25Gb/s 64-QAM-encoded OOFDM signal has also been demonstrated over 500m of legacy OM2 MMF with a power penalty of 3dB at a BER of 1.0×10^{-3} in a DML-based IMDD system. Modal noise is observed to contribute an estimated 1dB to the overall power penalty. This result is significant because, as described in chapter 1, current 10G Ethernet standards suffer from high cost and/or $\leq$ 300m transmission distance with legacy MMF. It has been shown that OOFDM has the potential to offer cost-effective 10G Ethernet LANs over legacy MMF infrastructure with operation well beyond 300m.

These experiments employing the developed 11.25Gb/s OOFDM transceivers are currently the only and therefore also the fastest ever demonstrations of real-time end-to-end OOFDM transmission.

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6 OOFDM Transmission with RSOAs and VCSELs as Intensity Modulators

Contents

6.1 Introduction

In this chapter alternative types of OOFDM optical intensity modulators are investigated for real-time OOFDM transceivers. Firstly, to achieve a cost-effective colourless transceiver, a reflective semiconductor optical amplifier (RSOA) with a bandwidth of only 1GHz is used to demonstrate real-time OOFDM transmission over the entire C-band at 7.5Gb/s over 25km SSMF. Secondly, with the aim of further reducing OOFDM transceiver cost, a vertical cavity surface emitting laser (VCSEL) is directly modulated to demonstrate real-time OOFDM transmission at 11.25Gb/s over 25km SSMF.

6.1.1 WDM-PONs and Colourless ONUs

Wavelength division multiplexing PONs (WDM-PONs) are widely considered as one of the most promising strategies for satisfying the exponentially increasing end-users' demands for broadband services in next generation optical access systems [1]. In a conventional WDM-PON a pair of dedicated wavelengths is assigned to each ONU for upstream and downstream transmission, thus WDM-PONs effectively provide multiple independent point-to-point links. This dedicated channel architecture offers highly attractive features; most important is the significant increase in aggregate network capacity as the bandwidth provided to each user no longer shared, thus providing a sustained and guaranteed high capacity per user. Another important advantage is that conventional TDM-PONs, such as GPONs and EPONs, only require a minor upgrade to enable their gradual evolution to WDM-PONs [1]. Furthermore the reduced link loss due to the absence of a passive splitter provides advantages of large split ratios and extended transmission reach. Other advantages include enhanced end-user privacy, protocol transparency and network scalability [1]. For widespread deployment of WDM-PONs, the most critical challenges are flexibility and cost-effectiveness. OOFDM has been considered as one of the strongest contenders for practical application in WDM-PONs due to the significant reduction in network complexity, enhanced flexibility and potential for cost-effective implementation [2]. Enhanced flexibility in OOFDM-based WDM-PONs can be achieved, for example, with hybrid WDM-OOFDMA PONs which can dynamically share the available bandwidth on a single wavelength amongst multiple ONUs. This is accomplished by exploiting OOFDM's ability to offer dynamic provision of hybrid bandwidth allocation in both the frequency and time domains [2].

To make WDM-PONs viable two key requirements are cost-effective networks and easy network deployment and operation. A major challenge to meeting these requirements is the provision of cost-effective colourless optical transmitters in the ONUs. A conventional solution to implementing colourless ONUs is to employ a tuneable laser source located in the ONU [1]. This approach however currently suffers from the lack of suitably cheap tuneable lasers, although the reliability offered by its simplicity and overall performance can make this approach favourable if volume production of low-cost tuneable lasers is realised.
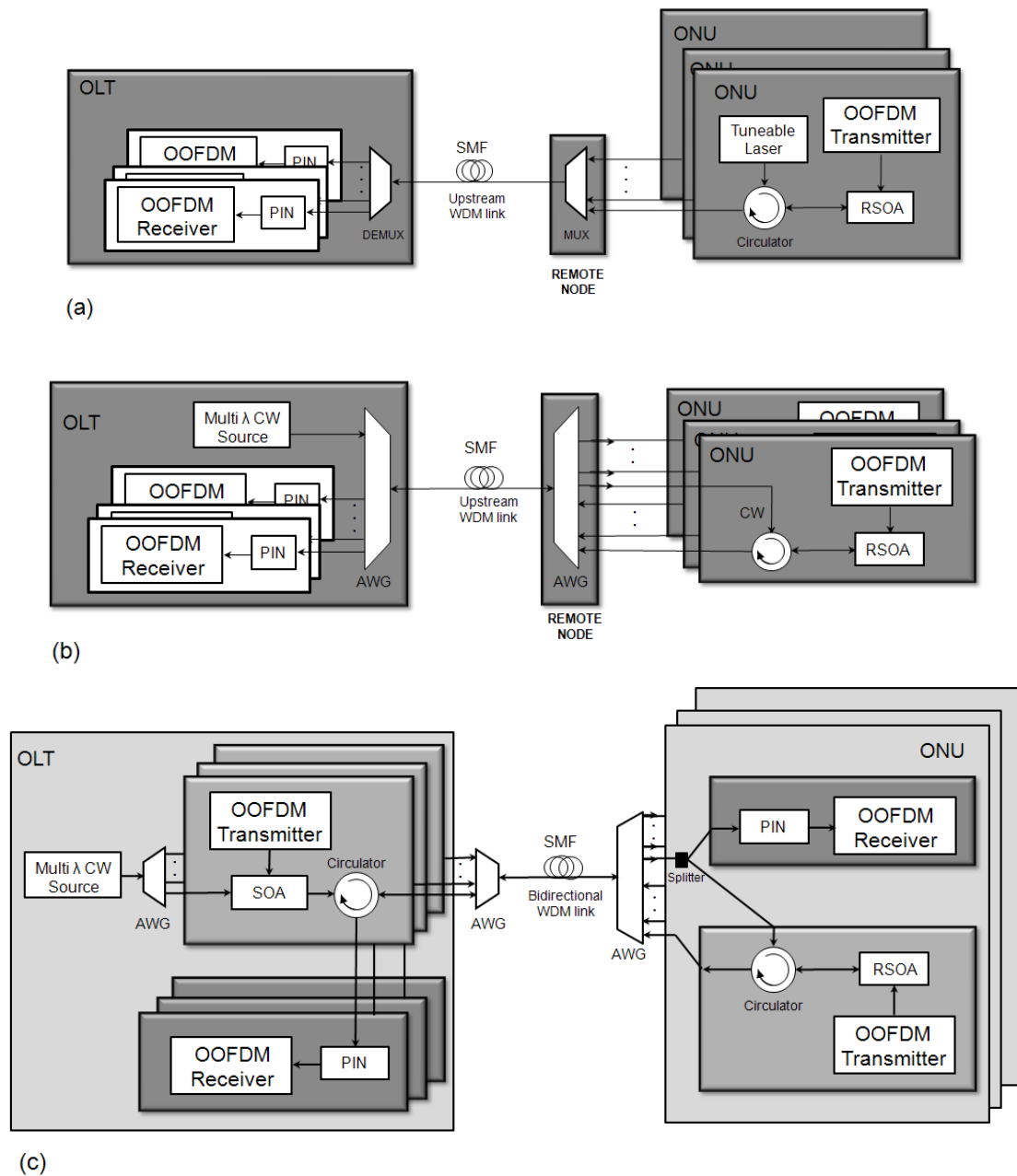

Fig. 6.1 Colourless OOFDM ONUs in WDM-PONs using an RSOA as an intensity modulator. (a) Tuneable laser in ONU, (b) carrier distribution in OLT, (c) bidirectional wavelength reuse.

An alternative approach to solving the challenge of colourless ONUs is remote upstream carrier distribution, where a multiple wavelength CW laser source located in the central office is sent downstream with the downstream traffic, the CW carriers are distributed to the ONUs via an arrayed waveguide (AWG) located in the remote node, finally intensity modulators located in the ONUs modulate the CW carriers before multiplexing in the remote node's AWG for upstream transmission [1]. For this case, if signal bandwidth is sufficiently large the upstream signal can suffer from interference from its associated unmodulated carrier due to Rayleigh backscattering (RB) noise [3]. A variation on the remote upstream carrier distribution solution is bidirectional wavelength reuse where the downstream optical signal is amplified and re-modulated for upstream transmission [3]. This approach requires an increase in network complexity due to additional optical components for signal routing however it halves the number of lasers required in the OLT compared to the remote CW distribution solution. Bidirectional wavelength reuse can also suffers from the RB noise effect which affects both downstream and upstream signals. It has been shown that the RB noise effect can have a significant impact on performance and, under certain conditions, can halve the upstream signal line rate [3]. A second effect that can also limit upstream transmission performance is cross-talk from a residual downstream signal if the downstream signal is not fully erased before re-modulation.

For all of the aforementioned colourless ONU solutions an optical intensity modulator is required in the ONU to modulate the upstream signal. RSOAs as intensity modulators in ONUs has been extensively investigated [4,5], since RSOAs have salient advantages including, simultaneous signal modulation and optical amplification, low component cost, compactness, low power dissipation, full coverage of the entire fiber transmission window and large-scale monolithic integration capability. Fig. 6.1(a-c) shows three different WDM-PON uplink architectures employing an RSOA to implement the aforementioned colourless ONU solutions.

An indication of the effectiveness of RSOAs-based colourless ONUs in WDM-OOFDM PONs is given by the an off-line DSP-based system, which successfully demonstrated upstream 10Gb/s OOFDM transmission over a 20km WDM-PON based on remote CW carrier distribution to a colourless 1GHz RSOA-based ONU [4]. This demonstration employed adaptive bit loading over 63 data-carrying subcarriers to compensate for the limited RSOA modulation bandwidth.

The work presented here is the first experimental demonstration of real-time OOFDM transceivers in simple IMDD SSMF systems employing a colourless RSOA intensity modulator (RSOA-IM) as depicted in Fig. 6.1(a). The real-time OOFDM transceivers allow system performance optimisation through the use of the on-line performance monitoring, live DSP parameter optimization and live RSOA-IM operating condition optimisation. Real-time end-to-end OOFDM transmission is demonstrated with operation over virtually the entire C-band (1530 -1565nm) at 7.5Gb/s line rate over 25km SSMF.

6.1.2 VCSELs for Further Reduced OOFDM Transceiver Cost

In order to enable the mass deployment of OOFDM-based PON systems it is critical that network equipment meets the stringent cost targets associated with access networks. Solutions must therefore be explored to minimise the cost of all individual OOFDM transceiver components. The DSP logic and DAC/ADC devices are key areas where costs can be minimised through optimised semiconductor designs and chip-scale integration of DSP logic and DAC/ADC components into a single mixed-signal ASIC solution. ASICs are highly suited to high equipment volumes, as associated with widespread PON deployment, to absorb the high development costs and achieve low per unit costs. Also modern mixed-signal integrated circuits (ICs) can support the multi-GHz RF devices required for the OOFDM transceiver's front end circuits, thus again exploiting the low-cost benefits of semiconductor integration. The cost of the OOFDM transceivers optical components must also be addressed if the overall cost target is to be met. The DFB-based DML, as used in all previous experiments presented in this thesis, is much cheaper than an external intensity modulator based solution, however it still contributes a significant portion of the overall transceiver cost. The investigation of low cost DMLs for OOFDM transmission is therefore highly important.

The use of a VCSEL as the intensity modulator in real-time OOFDM transmitters is highly desirable due to the significantly lower cost of VCSELs compared to their DFB counterparts. VCSELs also have the important characteristics of high reliability, long lifetime and easy testing and packaging [6]. It is the surface emitting property of the VCSEL that gives it great advantages over edge emitting lasers. Standard IC fabrication technologies can be employed which simplify device handling. More importantly VCSELs can be tested before cutting from the wafer thus eliminating the need to expend any further

production resources on faulty devices. Production costs are therefore significantly reduced which leads to the lower device cost. There are challenges associated with employing VCSELs as intensity modulators in IMDD PON systems due to the typical VCSEL properties of low modulation bandwidth, nonlinear modulation characteristics and frequency chirp [7]. Experimental demonstrations using the off-line DSP approach [8,9] have shown the great potential of using VCSELs in OOFDM-based systems. In particular an off-line DSP based system using adaptive bit-loading demonstrated 10Gb/s OOFDM IMDD transmission over 100km SMF using a VCSEL-based DML [9]. VCSELs are also being investigated for other applications to where bandwidth-bottlenecks have emerged. For example, VCSELs are also highly suited to the application of high capacity, power efficient optical interconnects for applications such as for intra-chip, chip-to-chip, board-to-board and rack-to-rack interconnectivity. Directly modulated VCSELs supporting a record 44Gb/s NRZ transmission over 2m of MMF have recently been reported [10].

A VCSEL-based OOFDM transceiver is thus highly desirable due to the significant impact on overall transceiver cost. To determine the viability of VSCEL-based OOFDM transceivers for cost-sensitive PON applications, this chapter explores the performance of a VSCEL as the intensity modulator in the 11.25Gb/s real-time OOFDM transceiver over 25km SSMF.

The cost-saving benefit of VCSEL-based OOFDM transceivers also applies to in-building MMF-based networks. Although not investigated as part of this thesis, investigations employing the VCSEL-based real-time OOFDM transceivers and MMF links is reported in [11] where it is shown that 11.25Gb/s transmission can be achieved over 800m of OM2 MMF.

6.2 Experimental Demonstration of Real-time OOFDM Transmission at 7.5 Gb/s over 25-km SSMF using a 1-GHz RSOA

This chapter first presents the performance of a RSOA intensity modulator (RSOA-IM)-based real-time OOFDM transceiver with on-line performance monitoring and live parameter optimisation in a simple IMDD SSMF system. The live control of digital system parameters including signal clipping level, total digital signal power and individual subcarrier power levels, is again utilised to optimise system performance. The compensation of the system frequency response roll-off effect reported in chapters 4 and 5 is essential to boost the BER performance. The adaptive transceiver results in a highly optimised transceiver performance with the ability to optimise link dependent parameters, such as the adaptive power loading profile, upon link establishment and provides performance robustness to constantly changing environments.

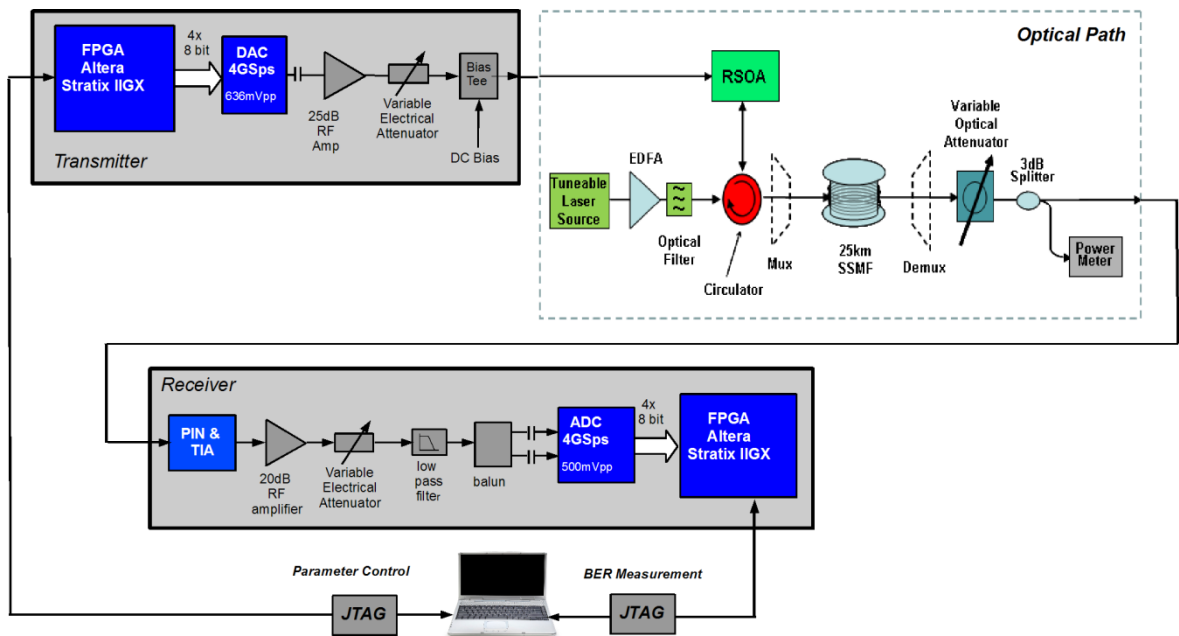### 6.2.1 Real-Time Experimental System Setup

Fig. 6.2 Experimental system setup for real-time OOFDM transmission using an RSOA as an intensity modulator

Fig. 6.2 shows the real-time experimental system setup. The 7.5Gb/s OOFDM transceiver design is as described in section 5.2.1, except the enhanced power-loading function, described in section 5.3.1, is also incorporated. Here a RSOA is employed as an intensity modulator and as the RSOA requires a high driving voltage of several volts an RF amplifier is included to amplify the electrical OOFDM signal. It should be noted that the optimisation of the RSOA driving voltage is critical as this can minimise the RSOA-IM-induced nonlinear effects, this is due to the opposing effects of unwanted signal clipping and beneficial higher signal extinction ratio associated with higher driving currents [12]. All fixed system parameters are identical to the 7.5Gb/s design, thus 32 subcarriers are employed with 15 conveying data, an 8-sample cyclic prefix is added to the 32 samples giving 40 samples per symbol and the FPGA clock is maintained at 100MHz giving a 100MHz symbol rate. The 8-bit DAC/ADC operate at 4GS/s and 16-QAM is taken on all the 15 information-bearing subcarriers. The OOFDM transceiver with the aforementioned parameters produces a raw signal bit rate of 7.5Gb/s, of which 6Gb/s is used to carry user data due to the selected cyclic prefix length of 2ns.

The optical transmitter components, as shown in Fig. 6.2, consist of a CW optical wave supplied by a tuneable laser source. The CW optical wave first passes through an EDFA followed by a 0.8nm optical filter for adjustment of CW optical powers and reduction of ASE respectively, then after passing through an optical circulator with 1.4dB insertion loss, it is injected, at an optical power of 5dBm, into a polarization-insensitive RSOA with a small-signal electrical 3-dB modulation bandwidth of 1.125GHz. The 2GHz 3.4Vpp electrical analogue OFDM signal and a 77mA DC bias current are combined in a 6GHz bias tee and then modulate the CW optical wave in the RSOA operating at a temperature of 13°C. The modulated real-time OOFDM signal is transmitted through a 25km SSMF, in which optical MUX/DEMUX may be inserted for WDM-PONs. The optical components employed at the receiver are identical to those employed in the SMF-based experimental setup in section 5.3.2. Here the optical signal also passes through a 3dB coupler after the variable optical attenuator for the purpose of received optical power measurement. The optical system is free from in-line optical amplification and chromatic dispersion compensation. The above-mentioned RSOA driving and bias currents, temperature and 5dBm CW optical power are identical for all measurements at the different optical wavelengths within the C-band.

6.2.2 Experimental Results
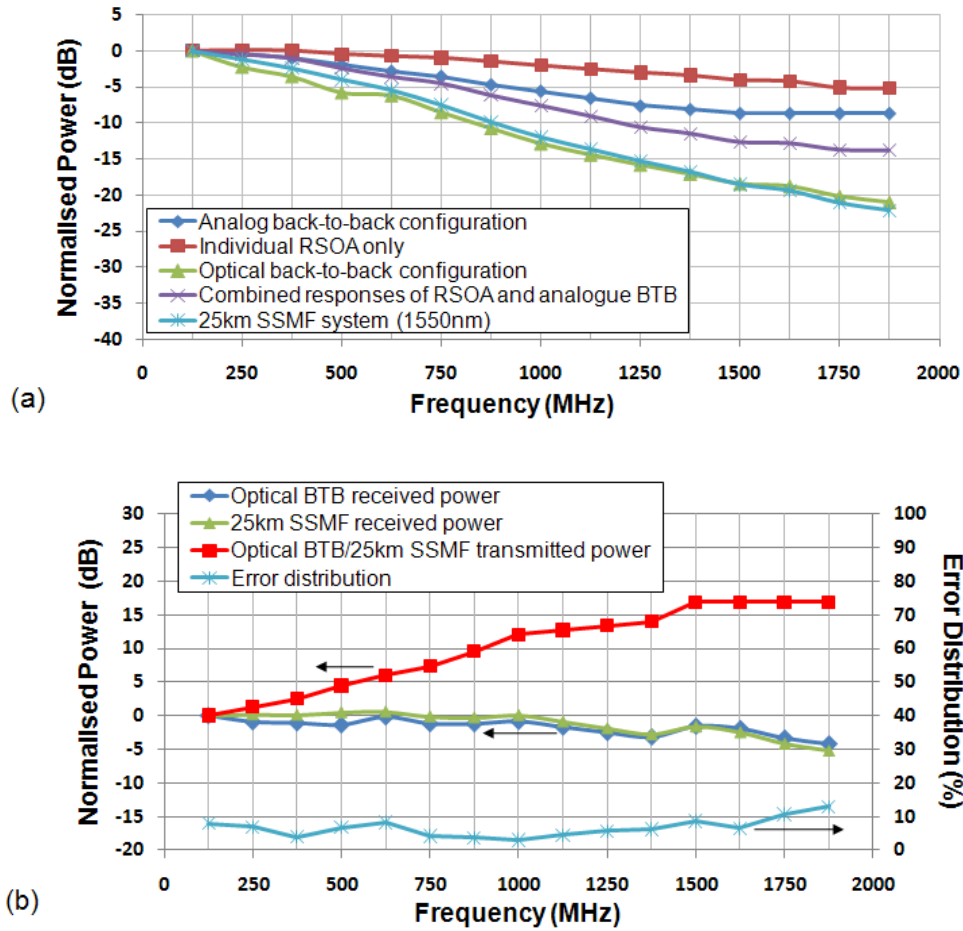
Fig. 6.3 (a) Frequency responses for different cases. (b) Normalized transmitted and received subcarrier powers and error distribution for optical back-to-back and 25-km SSMF configurations. The optical systems operate at wavelengths of 1550 nm.

The measured frequency responses normalised to the 1st subcarrier are plotted in Fig. 6.3(a) for different scenarios: 1) an individual RSOA; 2) an electrical analogue back-to-back configuration, whose frequency response decay is mainly caused by the DAC; 3) mathematically added responses between the RSOA and the analogue back-to-back; 4) an optical back-to-back configuration, and finally 5) an entire 25km SSMF system. For cases 2)-5), the frequency responses are measured from the IFFT input in the transmitter to the FFT output in the receiver. It can be seen from Fig. 6.3(a) that the 25km system frequency response decay within the signal spectral region is approximately 22dB. Comparisons between different curves imply that such a rapid roll-off is mainly attributed to the following three factors: i) the DAC due to its output filtering and inherent sin(x)/x response; ii) the RSOA due to its narrow modulation bandwidth, and most importantly, iii)

the signal spectral distortion due to the dynamic RSOA frequency chirp effect [12] The last factor explaining the difference between case 3) and case 4). Based on the above analysis, it is easy to understand that, when equal subcarrier powers are considered, the complex values of the low frequency subcarriers may overflow the dynamic output range of the FFT, whilst the constellation points of the high frequency subcarriers may be severely merged. This results in an unacceptably high total channel BER.
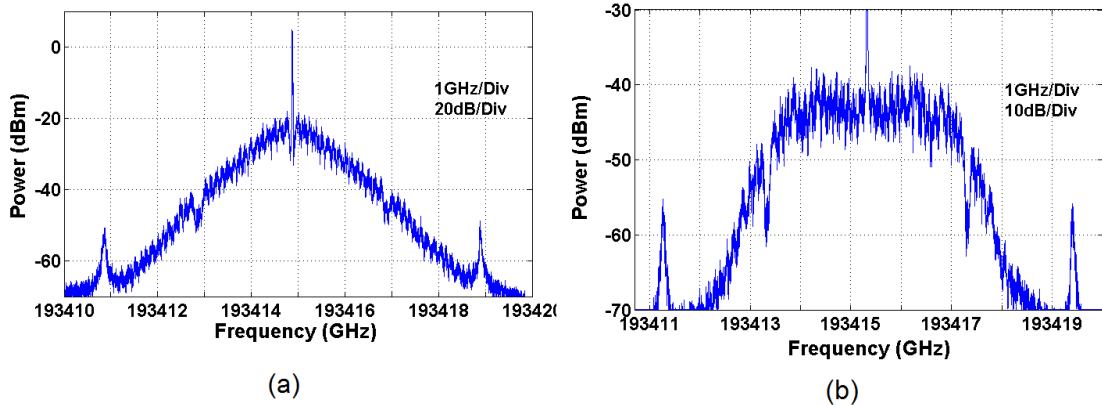
Fig. 6.4 Real-time OOFDM signal spectrum at RSOA output. (a) with equal power loading; (b) with adaptive power loading.

For the optical back-to-back and 25km SSMF transmission cases, the implementation and effectiveness of the adaptive power loading technique are explored in Fig. 6.3(b), where the adaptive power-loaded subcarrier power in the transmitter and the received subcarrier power prior to channel equalization in the receiver, all normalised to the 1st subcarrier, are plotted against subcarrier frequency, together with the resulting subcarrier BER distribution for 25km SSMF. In obtaining Fig. 6.3(b), the digital subcarrier amplitude of each subcarrier in the transmitter is adjusted finely to ensure that an almost uniform BER distribution (<10% variation) occurs over all the subcarriers and the total channel BER is also minimized simultaneously. Compared with Fig. 6.3(a), Fig. 6.3(b) indicates that, as expected, the system frequency response decay induced by the DAC, individual RSOA frequency response and the RSOA frequency chirp-induced dynamic spectral distortions can be compensated sufficiently by the adaptive power loading technique. The effectiveness of adaptive power loading is also confirmed in Fig. 6.4, where a sharply decaying OOFDM signal spectra at the RSOA-IM output for the case excluding adaptive power loading is observed in Fig. 6.4(a), whereas a flat top OOFDM signal spectra at the RSOA-IM output for the case including adaptive power loading is observed in Fig. 6.4(b). Here it is worth mentioning the following two facts: 1) A further increase in the relative

amplitude of the high frequency subcarriers causes the low frequency subcarriers to experience higher small-amplitude-induced quantization noise effect, 2) for the current transceiver design, the maximum variation in the relative subcarrier power levels is mainly determined by the dynamic range of the IFFT.

Fig. 6.5 (a) BER performance for optical back-to-back configuration and transmission over a 25-km SSMF for different wavelengths. Various received constellations of different subcarriers before channel equalization for optical BTB (b)–(d) and after 25-km SSMF transmission (e)–(g). (b) 1st subcarrier. (c) 8th subcarrier. (d) 15th subcarrier. (e) 1st subcarrier. (f) 8th subcarrier. (g) 15th subcarrier.

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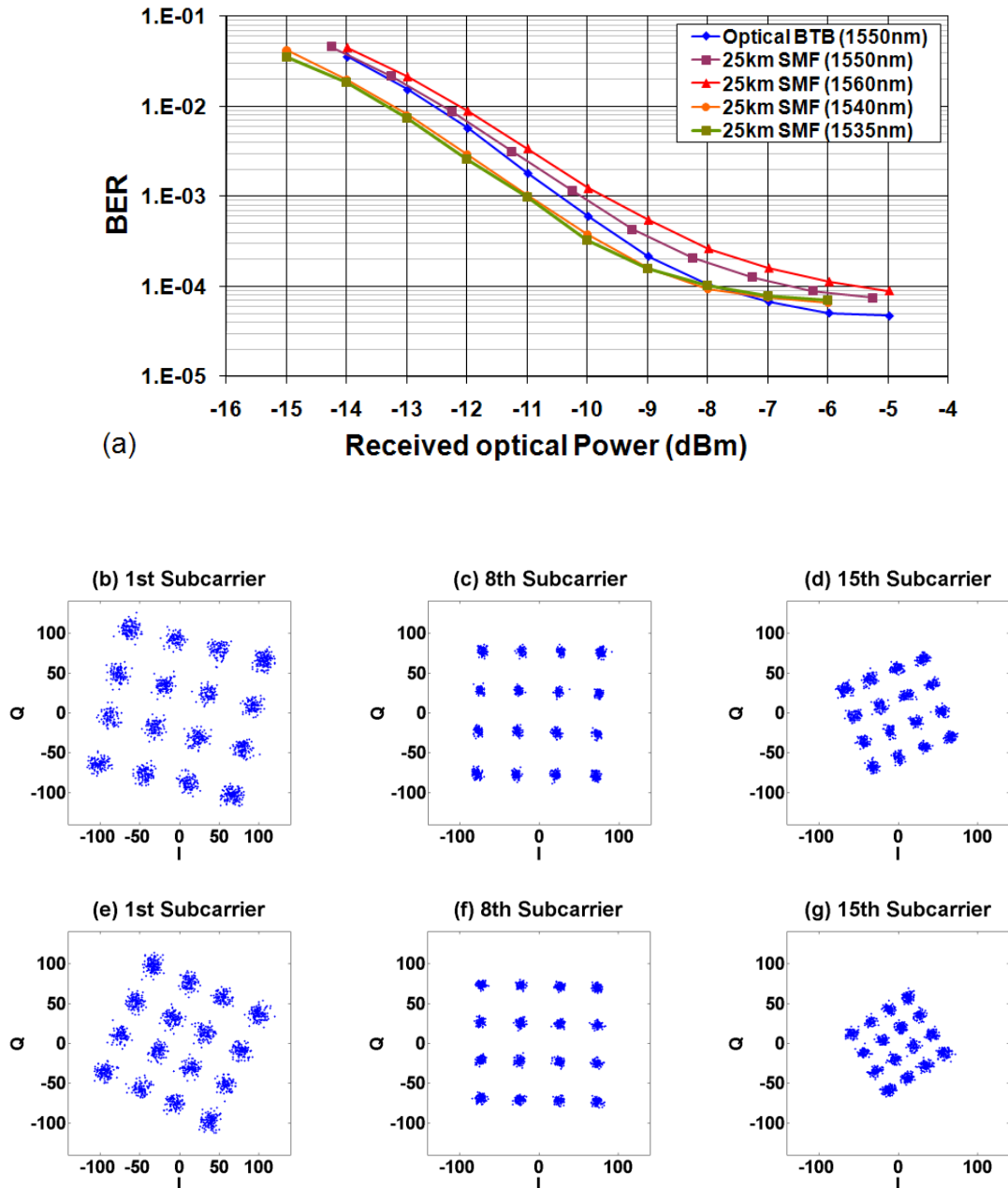Making use of the optimised subcarrier amplitude distribution, the BER performance of the real-time 7.5Gb/s OOFDM signals over 25km SSMF is shown in Fig. 6.5(a) for different wavelengths. The corresponding constellations at 1550nm recorded prior to performing channel equalisation in the receiver for representative subcarriers are also presented in Fig. 6.5(b-d) for the optical back-to-back case, and in Fig. 6.5(e-g) for the 25km SSMF transmission case. It can be seen from Fig. 6.5(a) that, for all the wavelengths across the C-band, BERs of $<9.0 \times 10^{-5}$ and power penalties of <0.5dB are achieved. These results indicate that the real-time RSOA-IM-based transceivers are capable of supporting colourless operation. The wavelength dependent minimum received optical power at a BER of 1×10^{-3}, as shown in Fig. 6.5(a), originates mainly from the wavelength-induced variation in extinction ratio of the RSOA modulated signals [12]. In Fig. 6.3(a), cases 4) and 5) have similar frequency responses, which, however, correspond to different BER performance, as seen in Fig. 6.5(a). This is attributed to the long transmission distance-enhanced subcarrier intermixing effect occurring upon photo-detection [6]. The effects of subcarrier intermixing and RSOA-induced small signal extinction ratio limit the minimum achievable BERs observed in Fig. 6.5(a).

6.3 Real-time Demonstration of Low-cost VCSEL-based OOFDM Transmission at 11.25Gb/s over 25km SSMF.

6.3.1 Real-Time Experimental System Setup

Fig. 6.6 shows the experimental system setup for the real-time OOFDM transceiver employing a low-cost, uncooled, 1550nm VCSEL as the DML. The system set up is identical to that employed in the 11.25Gb/s DFB-based set up with 25km SSMF in section 5.3.2 except here the DFB is replaced with a VCSEL with a specified small-signal modulation bandwidth of 3.63GHz. The DSP architecture of the transmitter and receiver are also identical to that employed in the 11.25Gb/s transceiver design as described in section 5.3.1. The transmitter DSP's on-line adjustment of subcarrier power-loading profile, digital signal amplitude and clipping level, together with the on-line monitoring features in the receiver DSP are fully utilised to optimise system performance. Furthermore the

operating conditions of the VCSEL can be rapidly optimised during system operation to determine the optimum bias current and driving voltage.

VEA: Variable Electrical Attenuator   **VOA**: Variable Optical Attenuator
Amp: RF Amplifier (20dB, 2.5GHz)   **LPF**: Low Pass Filter (2.4GHz)
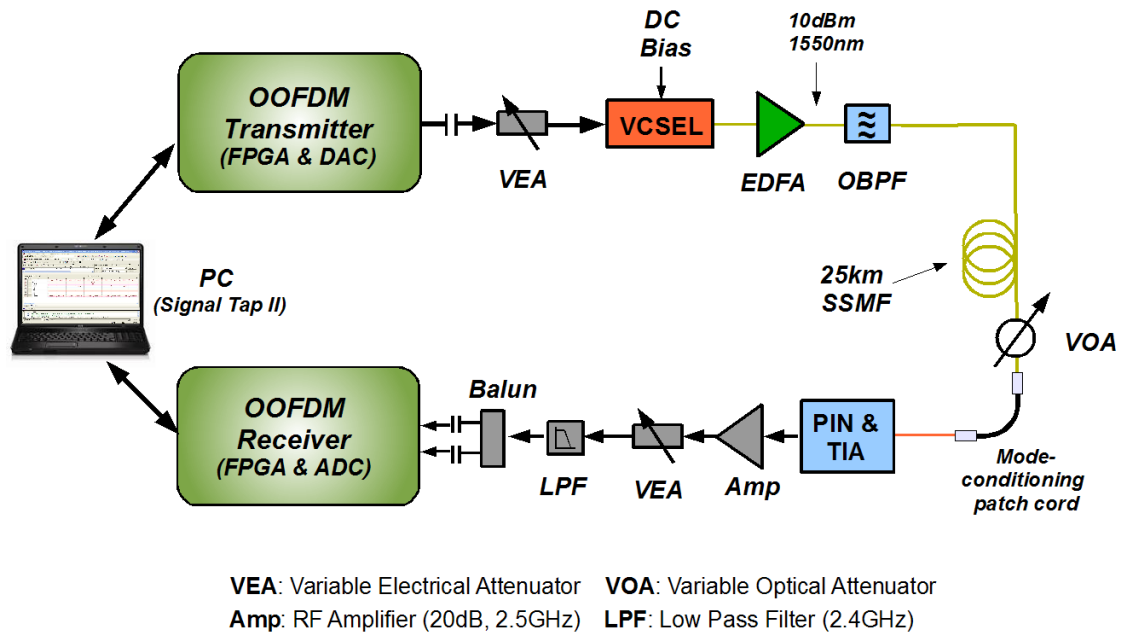
Fig. 6.6 Real-Time VCSEL-based OOFDM Experimental System Setup for 11.25 Gb/s line rate over 25km SSMF

The real-valued OFDM signal output by the DAC in the transmitter is adjusted by a variable electrical attenuator to provide an optimised driving voltage. The driving signal is combined with an adjustable bias current via a bias tee to directly modulate the fiber-tailed VCSEL. The VCSEL operating conditions are adjusted in combination with the other on-line adjustable system parameters to optimise the system performance and minimise the total channel BER. The determined optimum driving voltage and bias current are 320mVpp and 5.57mA respectively. For the aforementioned operating conditions the VCSEL output power is -5.4dBm. An EDFA boosts the optical power to 10dBm so that after the ASE filter the optical launch power to the 25km SSMF is 7.8dBm.

6.3.2 Experimental Results

To identify optimum operating conditions of the VCSEL intensity modulator and simultaneously explore the maximum achievable transmission performance of the 25km SSMF-based IMDD transmission system, the following three different system configurations are investigated:

- Case I: Analogue back-to-back. The DAC output in the transmitter is directly connected to the variable electrical attenuator input in the receiver.

- Case II: Optical back-to-back. The optical output of the band-pass filter in the transmitter is directly connected to the variable optical attenuator input in the receiver.

- Case III: The complete 25km SSMF link, as shown in Fig. 6.6.
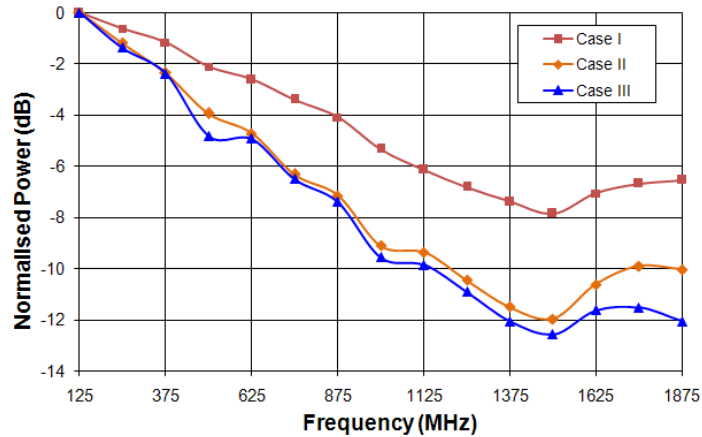
Fig. 6.7 System frequency responses of different system configurations: Case I: Analog back-to-back; Case II: Optical back-to-back and Case III: Entire IMDD 25km VCSEL-based SSMF system.

For the aforementioned system configurations, Fig. 6.7 shows the associated system frequency responses measured as described in section 5.3.3.1. For Case I, a maximum 7.85dB system frequency response roll-off occurs, which is a direct result of the on-chip filtering in the DAC and its inherent $sin(x)/x$ response, as previously observed in chapter 5. The slight difference in the frequency response characteristic observed here compared to that in section 5.3.3.1 is because although the DAC type is the same the individual component is different. Compared to Case I, Case II shows an extra 4dB system frequency response roll-off at high subcarrier frequencies. This is mainly attributed to nonlinearities of the VCSEL intensity modulator under the adopted operating conditions. Compared to the corresponding case with the DFB presented in section 5.3.3.1, the VCSEL exhibits an additional 1dB of roll-off, this is in line with its lower modulation bandwidth. In Case III, a maximum 12.5dB system frequency response roll-off is observed in the high subcarrier frequency region. The observed system frequency response difference between Case II and Case III is due to the IMDD nature of the transmission system and the VCSEL frequency chirp effect. Although the maximum frequency response roll-off in Case III is only 0.5dB larger compared to the corresponding case with the DFB in section 5.3.3.1, it can be seen

from Fig. 6.7 that the additional roll-off at the higher subcarrier frequencies can be as high as 2dB suggesting that the VCSEL exhibits increased chirp in comparison to the DFB.
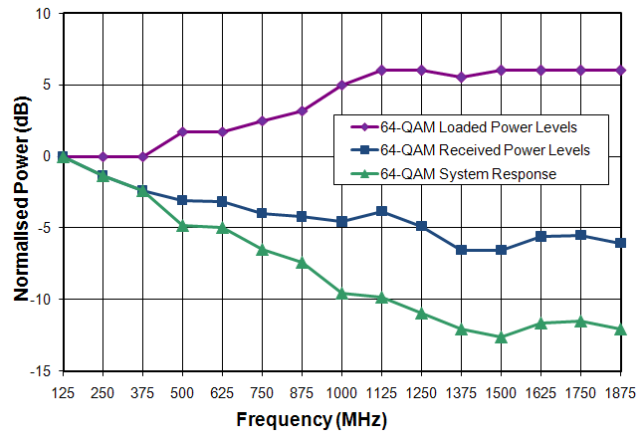
Fig. 6.8 Loaded and received subcarrier power levels and system frequency response for 25km SSMF link
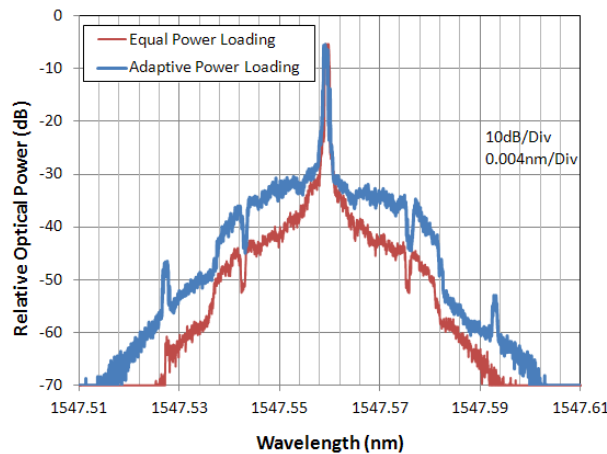
Fig. 6.9 OOFDM signal spectra at the output of the VCSEL intensity modulator with equal power loading and adaptive power loading.

For Case III the effectiveness of adaptive power loading, described in section 5.3.1, in combating the system frequency response roll-off effect is examined in Fig. 6.8, where the optimised subcarrier power loading profile in the transmitter is presented together with the received subcarrier power distribution in the receiver, all of which are normalized to the power of the corresponding first subcarrier. As expected, Fig. 6.8 indicates that adaptive power loading is highly effective at compensating for the VCSEL-based IMDD OOFDM system frequency response roll-off effect. To further verify the above statement, the 64-QAM-encoded OOFDM signal spectra at the output of the VCSEL intensity modulator with equal power loading and adaptive power loading are compared in Fig. 6.9. It can be seen that, for the case of utilising equal power loading, a sharp decay of the OOFDM

signal spectrum occurs. In comparison, adaptive power loading gives rise to a relatively flat OOFDM signal spectrum.

Under the optimised subcarrier power loading profile presented in Fig. 6.8, the measured subcarrier error distribution is shown in Fig. 6.10 for Case III. It can be seen in Fig. 6.10 that adaptive power loading enables almost uniform subcarrier error distributions with less than ± 12.5% variation. This confirms, once again, that the adaptive power loading technique can effectively compensate for the system frequency response roll-off effect, this results in an acceptable total channel BER which is unattainable with the equal power loading. The occurrence of the highest error peak corresponding to the 15th subcarrier in Fig. 6.10 is mainly due to the following two physical mechanisms: (1) the residual received power roll-off effect induced by the finite dynamic subcarrier power variation range, as shown in Fig. 6.8; (2) imperfect subcarrier orthogonality-induced inter-channel interference (ICI). Imperfect orthogonality between different subcarriers within a symbol arises due to the quasi-periodic structure of time domain OFDM symbols. Such an error peak can be considerably reduced when the signal extinction ratio of the OOFDM signal is increased [14].
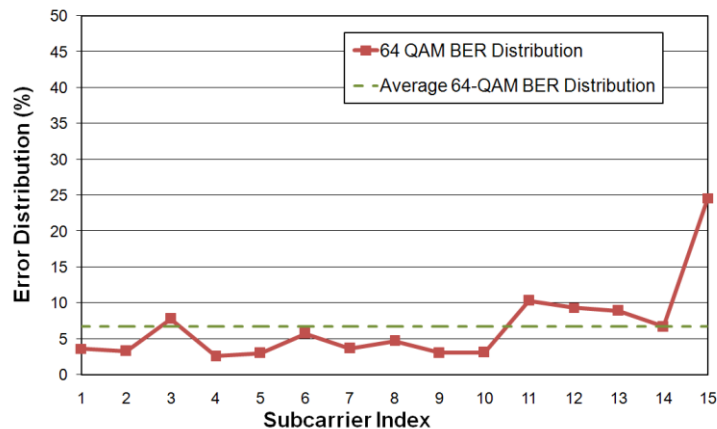
*Fig. 6.10 Typical subcarrier error distribution over 25km
SSMF when adaptive power loading is used.*

Based on optimised system parameters including the optimum subcarrier power loading profile, VCSEL-based real-time end-to-end transmission of 11.25Gb/s 64-QAM-encoded OOFDM signals is experimentally demonstrated over 25km SSMF IMDD system. Fig. 6.11 shows the measured total channel BER performance for both Case II and Case III.

From Fig. 6.11, it is observed that, for 11.25Gb/s 64-QAM-encoded OOFDM signals, the total channel BERs of 1.1×10^{-3} and 1.2×10^{-3} are obtainable for Case II and Case III, respectively. The corresponding power penalty when considering a FEC limit of 4×10^{-3} [13] is approximately 0.5dB. The main physical factor limiting the minimum achievable BER is the relatively low extinction ratio of the VCSEL intensity-modulated OOFDM signal [14]. Generally speaking, a small signal extinction ratio reduces the effective signal-to-noise ratio (SNR) of a received OOFDM signal for a specific photon detector. Therefore, an OOFDM signal encoded using a high signal modulation format is more susceptible to the effective SNR reduction, compared to an OOFDM signal encoded using a low signal modulation format. The error-floor like BER performance observed in Fig. 6.11 is a result of the low signal extinction ratio-induced small effective SNR of the received OOFDM signal.
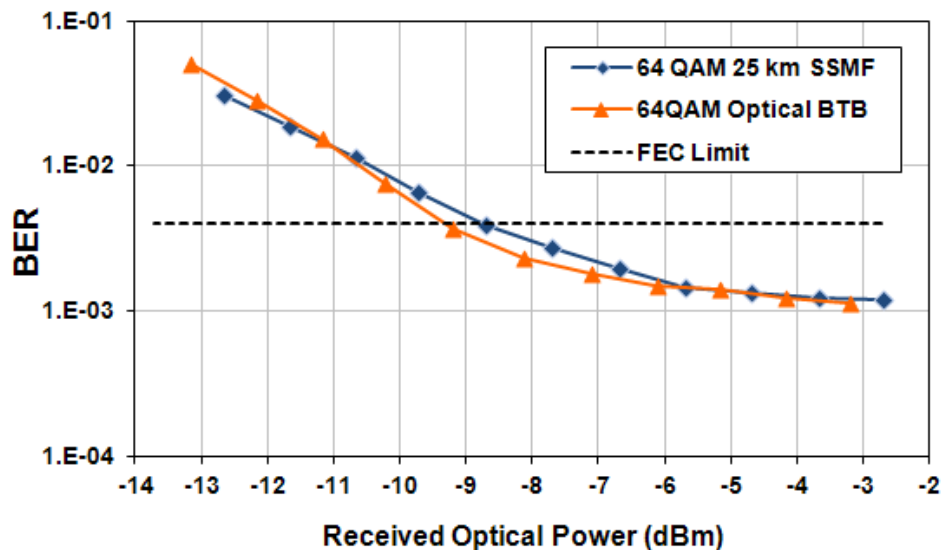
Fig. 6.11 BER performance for optical back-to-back and transmission over 25km SSMFs.

Representative constellations of individual subcarriers of the 11.25Gb/s 64-QAM-encoded OOFDM signals corresponding to the total channel BERs of 1.1×10^{-3} for Case II and 1.2×10^{-3} for Case III are presented in Fig. 6.12. These constellations are recorded prior to channel equalization in the receiver. As expected the constellations show a variation in amplitude level with subcarrier frequency corresponding to the power variation shown in Fig. 6.8. The low deviation between the corresponding Case II and Case II constellations is

in agreement with the small BER difference between these two cases, as shown in Fig. 6.11.
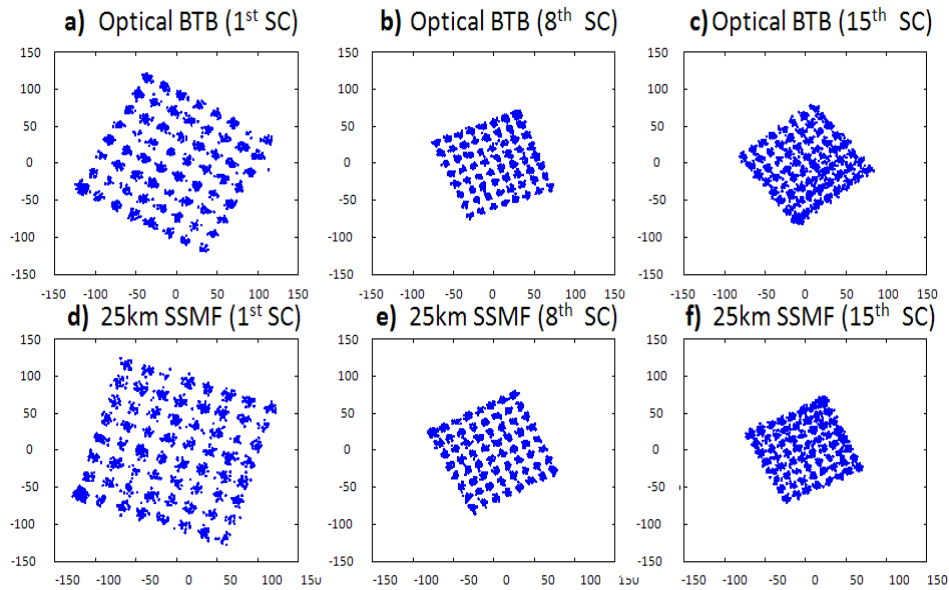
Fig. 6.12 Received 64-QAM constellations of individual subcarriers before equalization. (a, b, c) Optical back-to-back, total channel BER = 1.1×10^{-3}, (d, e, f) 25km SSMF, total channel BER = 1.2×10^{-3}.

6.4 Conclusions

This chapter first presented the experimental demonstration of real-time OOFDM transmission at 7.5Gb/s over 25km SSMF across the C-band using a 1GHz RSOA as an intensity modulator. The RSOA's narrow modulation bandwidth and dynamic frequency chirp effect significantly contribute to the system frequency response roll-off which is as large as 22dB for the 25km SSMF transmission link. The adaptive power loading technique is shown to be highly effective in compensating for the large system frequency response roll-off to achieve BERs of $<9.0\times10^{-5}$ and power penalties of <0.5dB for all the wavelengths across the C-band. The significance of this result is that it clearly demonstrates the feasibility of implementing RSOA-based colourless ONUs for application in OOFDM-WDM PONs. Colourless ONUs being required to facilitate the essential characteristics of OOFDM-WDM PONs of cost-effectiveness, flexibility and manageability.

Secondly this chapter experimentally explored the feasibility of employing low-cost uncooled VCSELs as the intensity modulator in the real-time OOFDM transmission system. The VCSEL-based OOFDM transceiver was employed to demonstrate real-time end-to-end IDMM transmission of 11.25Gb/s 64-QAM-encoded OOFDM signals over 25km SSMF with a minimum BER of 1.2×10^{-3}. This showed that the VCSEL with a modulation bandwidth of 3.6GHz can achieve a similar performance to a DFB with a modulation bandwidth approximately 3 times larger. It has been identified that the low extinction ratio of the VCSEL-IM OOFDM signal is the dominant factor limiting the maximum obtainable system performance.

Considering the fact that conventional DFB lasers take a significant portion of the total OOFDM transceiver cost, this work is of great value as it demonstrates the potential of utilising low-cost VCSELs as part of the solution for realising low-cost OOFDM transceivers. Demonstrating the feasibility of low cost OOFDM transceivers is an essential step required before mass production can further reduce transceiver cost necessary for mass deployment of OOFDM-based PONs.

VCSEL technology is still undergoing intensive research and improved devices are expected in the near future. Highly linear VCSELs with large modulation bandwidths (>10GHz) and with steep L-I curves are already becoming commercially available. Also one important area that manufacturers are addressing is the clear need to increase VCSEL output power to eliminate any need for optical amplification. VCSELs are therefore highly important devices which can be instrumental to achieving low-cost OOFDM transceivers for 40Gb/s and beyond.

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7 A Synchronous Clock Recovery Technique for OOFDM Transmission

Contents

7.1   Introduction

In all previously presented real-time end-to-end OOFDM systems, the transmitter and receiver both derived their required clock signals from a common reference clock, as do the real-time OOFDM receivers in off-line experiments [1,2]. It is obvious that, in a practical system, the receiver must independently generate a suitable clock to provide an accurate timing signal for all clocked functions in the receiver. Generally speaking, for any transmission system, there are two distinct receiver clock generation methods: asynchronous and synchronous. In an asynchronously clocked system, the receiver operates with an independent oscillator, and uses the received signal to accurately detect the offset between the transmitter and receiver clocks, the offset effects are then compensated for in the receiver; while in a synchronously clocked system, the receiver extracts a synchronous clock signal from the received signal based on embedded timing information.

For asynchronously clocked OOFDM transmission, sampling clock offset (SCO) and symbol timing offset (STO) may occur, which, if not suitably compensated, degrade the system performance due to the ICI and ISI effects [3,4]. The necessary compensation of the SCO and STO effects inevitably requires additional DSP resources which add extra complexity to the receiver. In addition, depending on the transceiver implementation, individual SCO compensation may be needed for each subcarrier, therefore, DSP resources increase with the number of subcarriers. Off-line OOFDM experiments employ asynchronous clock recovery techniques and typically compensate for the SCO effect by detecting the drift in phase of pilot tones. Real-time asynchronously clocked OOFDM transmission [4] has been experimentally demonstrated at 11.25Gb/s, which employs DSP to extract timing information directly from the OOFDM signal through detection of any drift in cyclic prefix position. OOFDM symbol realignment then compensates both the SCO and STO effects [4].

Conversely, synchronously clocked OOFDM is free from the SCO and STO effects, assuming fast tracking of any transmitter clock drift, sampling instance errors are only caused by residual jitter of the receiver's sampling clock. However, extracting timing information directly from the noise-like, analogue, high-speed OOFDM signal is challenging and also requires additional DSP functionality in the receiver.

A simple, DSP-free synchronous clocking technique [5-7] is proposed and experimentally demonstrated in a real-time end-to-end IMDD OOFDM system at 11.25Gb/s over 25km SSMF using a DML. In this chapter, in-depth investigations of the DSP-free synchronous clocking technique are undertaken in the aforementioned 11.25Gb/s OOFDM transmission systems in terms of: a) identification of optimum operating conditions for maximisation of the system transmission performance, and b) examination of system performance robustness. It is shown that a high quality receiver clock can be recovered from the received optical signal, and more importantly, that there is no BER degradation or optical power budget penalty compared to the common clocking approach. It is also shown that the synchronous clocking technique leads to a significant improvement in system stability.

This work is a vital milestone towards the realisation of practical OOFDM systems as it provides a simple and effective solution to the obligatory receiver clocking function. This work also has particular significance for synchronisation of OOFDM multiple access-based passive optical networks (OOFDMA-PONs) as described in section 2.5.2. For operating the OOFDMA-PON, all network elements must be highly synchronised, this is because OOFDMA divides bandwidth between users using dimensions of both frequency and time [13]: subcarriers provide bandwidth partitioning in the frequency domain and timeslots provide bandwidth partitioning in the time domain. Dynamic bandwidth allocation (DBA) can therefore be performed with a high granularity as represented by the individual "data blocks" as shown in Fig. 2.18. and Fig. 7.1. In downstream transmission, the signal timing for all users is synchronised due to the common OLT. Whilst in upstream transmission, clock offset between different optical network units (ONUs) can result in offsets in both the frequency and time domains, thus causing the "data blocks" to merge in both dimensions, as shown in Fig. 7.1(b). The offsets in the frequency domain destroy orthogonality between subcarriers, resulting in inter-subcarrier leakage: the offsets in the time domain lead to severe merging of timeslots/frames if no mechanism is employed to maintain timeslot/frame alignment. Therefore, it can be far more practical to implement OOFDMA-PONs using synchronously clocked ONUs, because of the following two key reasons: firstly, subcarrier orthogonality is preserved in the upstream signals, secondly, any timeslot/frame drifts between ONUs are eliminated thus avoiding the need for additional DSP functionality to track and readjust timeslot offsets.

OOFDMA-PONs can also potentially support multiple time-division-multiplexed (TDM) PON standards [8]. This coexistence of different standards has the advantage that subscribers can be gradually migrated to the higher speed next generation PON standards such as OOFDMA, without changes to the network infrastructure. Backwards compatibility of OOFDMA-PONs and its overlay with existing PON standards is only possible if the entire PON can be synchronised together with inter-timeslot allocation management. The OOFDM synchronisation technique presented in this chapter therefore has great potential for drastically simplifying the implementation of OOFDMA-PONs.
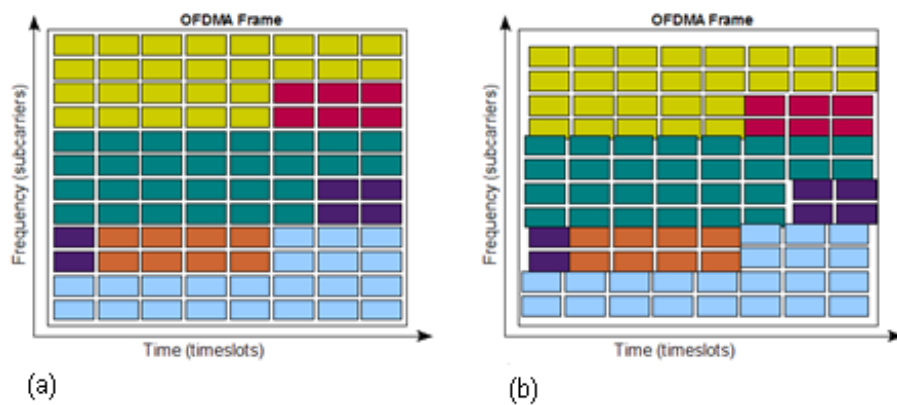
Fig. 7.1 a) OOFDMA upstream frame with synchronously clocked ONUs, b) OOFDMA upstream frame with asynchronously clocked ONUs without compensation (colours represent "data blocks" from individual ONUs).

7.2 Principle of Synchronous OOFDM Clocking Technique

The proposed and implemented synchronous clocking technique [5-7], as illustrated in

Fig. 7.2, overcomes the difficulty of extracting timing information directly from the OOFDM data signal by combining a dedicated electrical timing signal, here referred to as the synchronisation clock, S_{CLK} , with the generated electrical OFDM signal, S_{OOFDM}. In the OOFDM transmitter, S_{CLK} and S_{OOFDM} are summed together electrically to produce a combined signal S_{COMB}, which is utilised to directly modulate the intensity of an optical laser source. The synchronisation clock is a sine wave at a frequency outside the OFDM signal band. The transmitter requires at least two high level clock signals namely $C_{TXLOGIC}$ and C_{DAC}: $C_{TXLOGIC}$ clocks the transmitter's digital logic and C_{DAC} is used by the DAC to

generate the sampling clock, either directly or indirectly. $C_{TXLOGIC}$, C_{DAC} and S_{CLK} are all generated from a common reference clock, C_{REF}, as all clocks must be synchronous.
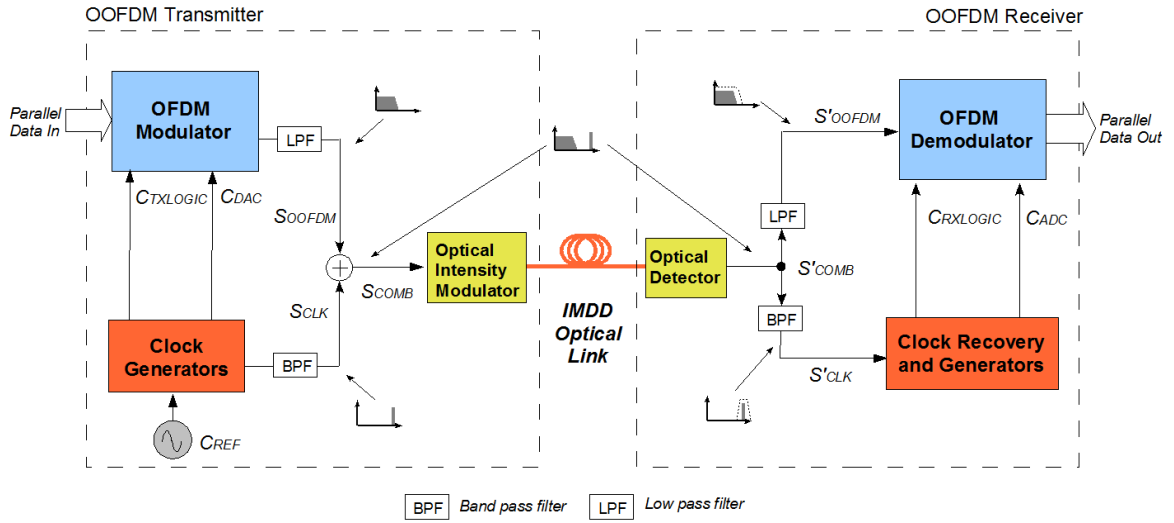
Fig. 7.2 Basic system configuration for synchronously clocked OOFDM system

In the transmitter, after being combined with an appropriate DC bias current, the S_{COMB} signal directly modulates the intensity of an optical laser source to generate an OOFDM signal for transmission. The total bandwidth of the signal S_{COMB} is much lower than the bandwidths of any optical filters or WDM multiplexers/demultiplexers potentially in the optical signal path, such that it can pass transparently through the system from transmitter to receiver. After transmission through the optical system, the received intensity-modulated OOFDM signal is directly detected by a photo-detector in the receiver to produce an electrical signal S'_{COMB}. This signal is then split to extract the received OFDM signal, S'_{OOFDM}, by low-pass filtering, and also to extract the received synchronisation clock, S'_{CLK}, by band-pass filtering. S'_{OOFDM} is appropriately amplified and digitised for subsequent DSP to recover the transmitted data. The received, jittered clock signal S'_{CLK} is pre-scaled to reduce its frequency before driving a phase locked loop (PLL) which generates a receiver clock, from which all required receiver clocks can be produced. The PLL can convert the received clock frequency and also provides a high level of jitter suppression such that stable, low jittered clocks are produced to drive the receiver's electronics. Similar to the transmitter, the receiver also requires two high level clocks $C_{RXLOGIC}$ and C_{ADC}: $C_{RXLOGIC}$ is the clock for the receiver's digital logic and C_{ADC} is the clock for the receiver's ADC. The ADC generates the sampling clock either directly or indirectly from C_{ADC}. It should be emphasized that all clocks in the transmitter and

receiver, in particular the DAC and ADC sampling clocks, are synchronous and originate from C_{REF} in the transmitter, thus the SCO effect is negligible.

The basic method of transmitting and recovering the synchronisation clock is relatively straightforward. However, applying it to a real-time OOFDM system provides an extremely effective, low complexity, low cost and robust clocking solution which avoids the need for any DSP for receiver clock generation. Although the basic clock transmission principle is relatively simple, the clock must be transmitted independently to the OFDM signal yet as the signals are transmitted simultaneously through the same optical system, careful system design is required to identify optimum operating conditions where the clock and data transmission functions can satisfactorily coexist.

It should be noted that the use of the proposed synchronous clocking technique for both upstream and downstream traffic in OOFDMA-PONs, does not require any additional clocks to be generated, as the additional transmitter and receiver can utilise the available clocks. The clock driving the digital logic can drive both the transmitter and receiver logic, which would most likely be in the same integrated circuit, likewise the DAC/ADC clock can be used to drive both DAC and ADC simultaneously.

7.3 Experimental Setup for Real-time OOFDM Synchronous Clock Recovery

Fig. 7.3 shows the experimental setup for the synchronously clocked real-time OOFDM system at 11.25Gb/s. As implementation of the 11.25Gb/s real-time OOFDM data generation/detection has been presented in detail in section 5.3, this section focuses attention on the implementation and optimisation of the synchronous clocking technique. In the FPGA-based real-time OOFDM transmitter and receiver, 64-QAM encoding/decoding is employed on all 15 subcarriers, giving a raw data rate of 11.25Gb/s. To achieve optimum system performance, the FPGA design uses the same channel estimation, adaptive power loading, live parameter control, symbol alignment and on-line performance analysis functions as described in chapters 3 to 5. All the key fixed system parameters are as employed in the 11.25Gb/s experiment described in section 5.3. Fig. 7.3 indicates all RF amplifier gains and RF filter cut-off frequencies. In comparison to the

11.25Gb/s set up in section 5.3, in the transmitter an RF amplifier is introduced to increase the OFDM signal power from the DAC to compensate the coupler loss and, in combination with electrical attenuators, to increase the adjustment range of the signal power. In the receiver an RF amplifier is also used before the splitter to compensate its loss.

Although the clock generation has similarities with that employed in previous experiments the complete clocking system will be described for clarity. At the transmitter, a frequency synthesiser functions as the master clock source operating at 4GHz with an accuracy of ≤3ppm. This clock is also internally pre-scaled to provide a 100MHz clock for the transmitter FPGA ($C_{TXLOGIC}$) (100MHz is the OOFDM symbol rate). One 4GHz output from the frequency synthesiser is divided by 2, band-pass filtered and amplified to generate a 2GHz sine wave signal for the 4GS/s DAC (C_{DAC}). The DAC consists of four interleaved converters each operating at 1GS/s so the 2GHz clock is further subdivided to 1GHz internally in the DAC. A second 4GHz output is band-pass filtered and variably attenuated to provide the dedicated 4GHz synchronization clock signal (S_{CLK}). The amplitude of S_{CLK} can be adjusted directly with the synthesiser's output level adjustment and the variable electrical attenuator is also used to extend the adjustment range. The electrical OFDM signal from the DAC (S_{OOFDM}) is amplified, low-pass filtered and variably attenuated before combination with the synchronization clock via a resistive RF coupler. The signal from the coupler (S_{COMB}) is attenuated and combined via a bias-T with an optimised DC bias current to directly modulate the 10GHz, 1550nm DFB laser. After boosting the DFB output power with an EDFA and optical band-pass filtering to reduce ASE, the optical launch power is set at 6dBm. The transmission link consists of 25km SSMF which has an 18ps/nm/km chromatic dispersion parameter and a linear loss of 0.2dB/km at 1550 nm.

At the receiver a variable optical attenuator is used to control the received optical power prior to the 12.4GHz linear PIN detector. The electrically amplified output of the PIN (S'_{COMB}) is split by a 2-way resistive RF splitter. One output that feeds the OOFDM receiver is low-pass filtered to remove the clock signal and provide anti-aliasing filtering. Having been amplified and suitably attenuated, the signal (S'_{OOMDM}) is then fed to the differential input of the 4GS/s ADC via a balun. As the received optical power varies, S'_{OOMDM}'s electrical gain is also adjusted accordingly to optimise the signal amplitude at the ADC input. Automatic gain control (AGC) can of course be implemented by measuring the received signal amplitude, and controlling a variable gain amplifier (VGA). The second

output is amplified by a high gain amplifier (30dB) and band-pass filtered to extract only the 4GHz synchronisation clock signal (S'_{CLK}). A prescaler reduces the clock frequency to 10MHz, which is then low-pass filtered and used as the external reference for a clock synthesizer generating the 2GHz clock for the receiver's ADC (C_{ADC}), this clock is also pre-scaled to generate the 100MHz receiver FPGA clock ($C_{RXLOGIC}$). In the present system setup, the clock synthesizer in the receiver effectively operates as a PLL, such a clock synthesizer can, however, be easily replaced by a low-cost, fixed frequency PLL and a 1/20 prescaler.
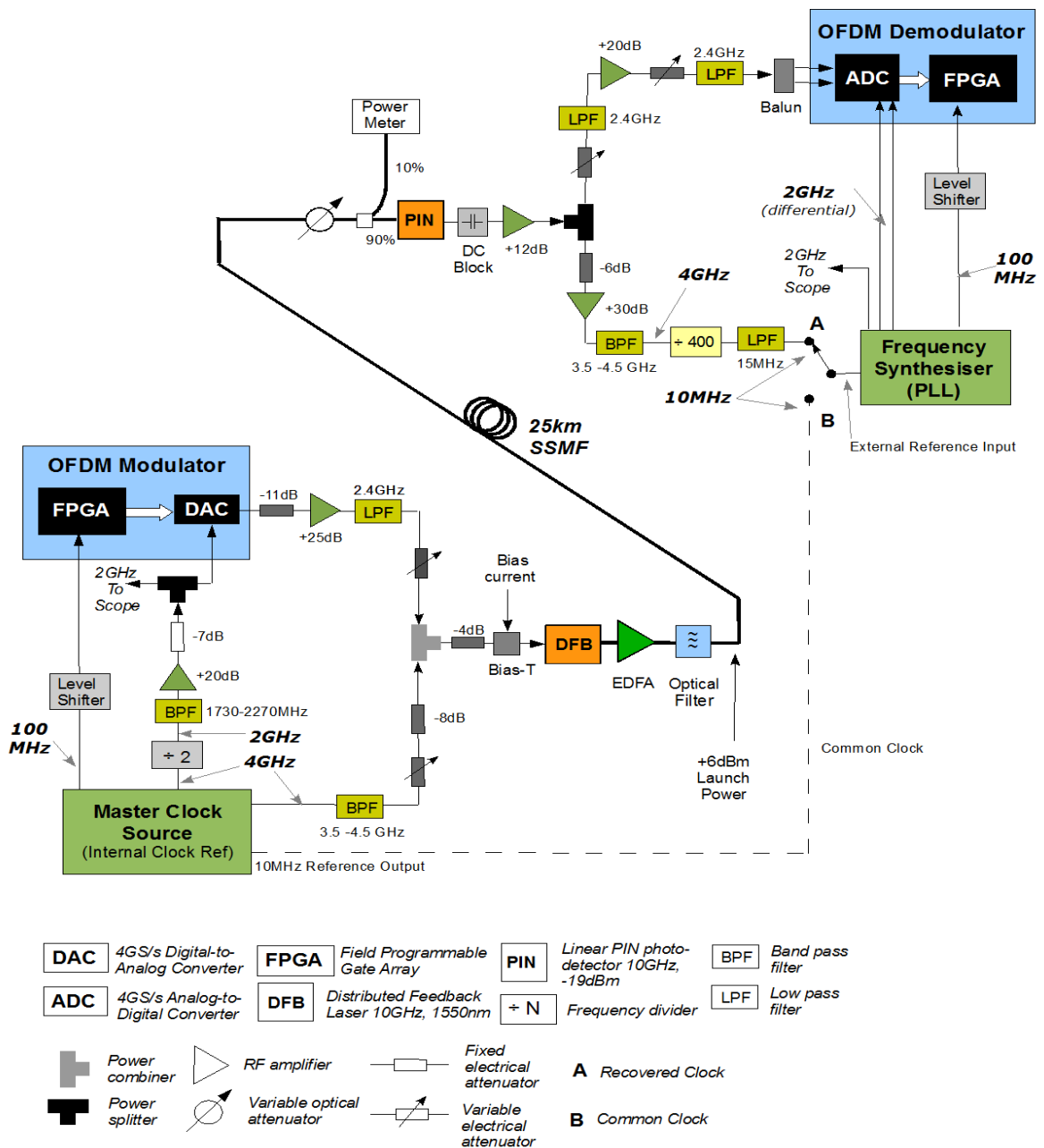

Fig. 7.3 Experimental system setup for real-time OOFDM transmission at 11.25Gb/s with synchronous clock recovery.

To configure the system to also operate with the common clock method as used in previous experiments, the 10MHz reference output from the transmitter's clock synthesiser is directly connected to the external reference input of the receiver's frequency synthesiser. This is illustrated in Fig. 7.3 where the external reference input is connected to point A to use the recovered clock and to point B to use the common clock. Changing between the recovered clock and the common clock in this way enables a direct comparison of the two clocking methods under exactly the same system setup and operating conditions. The optimum signal clipping ratio and adaptive subcarrier power loading profile are obtained for the 25km IMDD SSMF system using the common clock configuration and employed for all measurements. This ensures any performance variations observed are only due to the two different clocking methods.

7.4 Experimental Results

7.4.1 Operation of Synchronously Clocked OOFDM System

The DML-modulated 11.25Gb/s OOFDM signals with the 4GHz synchronisation clock are transmitted simultaneously over an IMDD 25km SSMF system with successful clock and data recovery in the receiver. Fig. 7.4 shows electrical signal waveforms at various points in the system subject to optimum operating conditions identified in section 7.4.2. It should be noted that all peak-to-peak signal levels in Fig. 7.4 include ~20mVpp of internal oscilloscope noise. At the selected operating conditions, the RF signal powers at the bias-T input are approximately -16dBm for the synchronisation clock and -9.6dBm for the OFDM signal, the synchronisation clock power is therefore 6.4dB lower than the power of the OFDM signal. In the optical domain this corresponds to a power difference of 3.2dB.

Fig. 7.5 shows the electrical spectra of both the transmitted signal S_{COMB} and received signal S'_{COMB} measured with the same resolution bandwidth (3MHz). The OFDM signal occupies the baseband frequency region of <2GHz, above which the residual OFDM image signal due to imperfect low-pass filtering in the transmitter is also observed. However, it is not necessary to insert a capacity-reducing guard band to permit the image signal to be completely removed by filtering. The synchronisation clock is clearly seen at 4GHz and it is evident that there is a frequency spacing of more than 1GHz below the

(a) 4GHz Clock signal at Bias-T input (100mVpp)

(b) OFDM signal at Bias-T input (599mVpp, 73.8mVrms, Clipping ratio 12.2dB)

(c) Combined signal at Bias-T input (655mVpp), [1ns/div]

(d) Combined signal at receiver, after 12dB amplification (453mVpp), [100ps/div]

(e) Received 4GHz clock after amplification and band-pass filtering at -6.5dBm received optical power (922mVpp)

(f) Received 4GHz clock after amplification and band-pass filtering at -13.5dBm received optical power (235mVpp)

(g) OFDM signal in receiver after low-pass filter, amplification and attenuation (425mVpp, 48mVrms, clipping ratio 12.9dB)
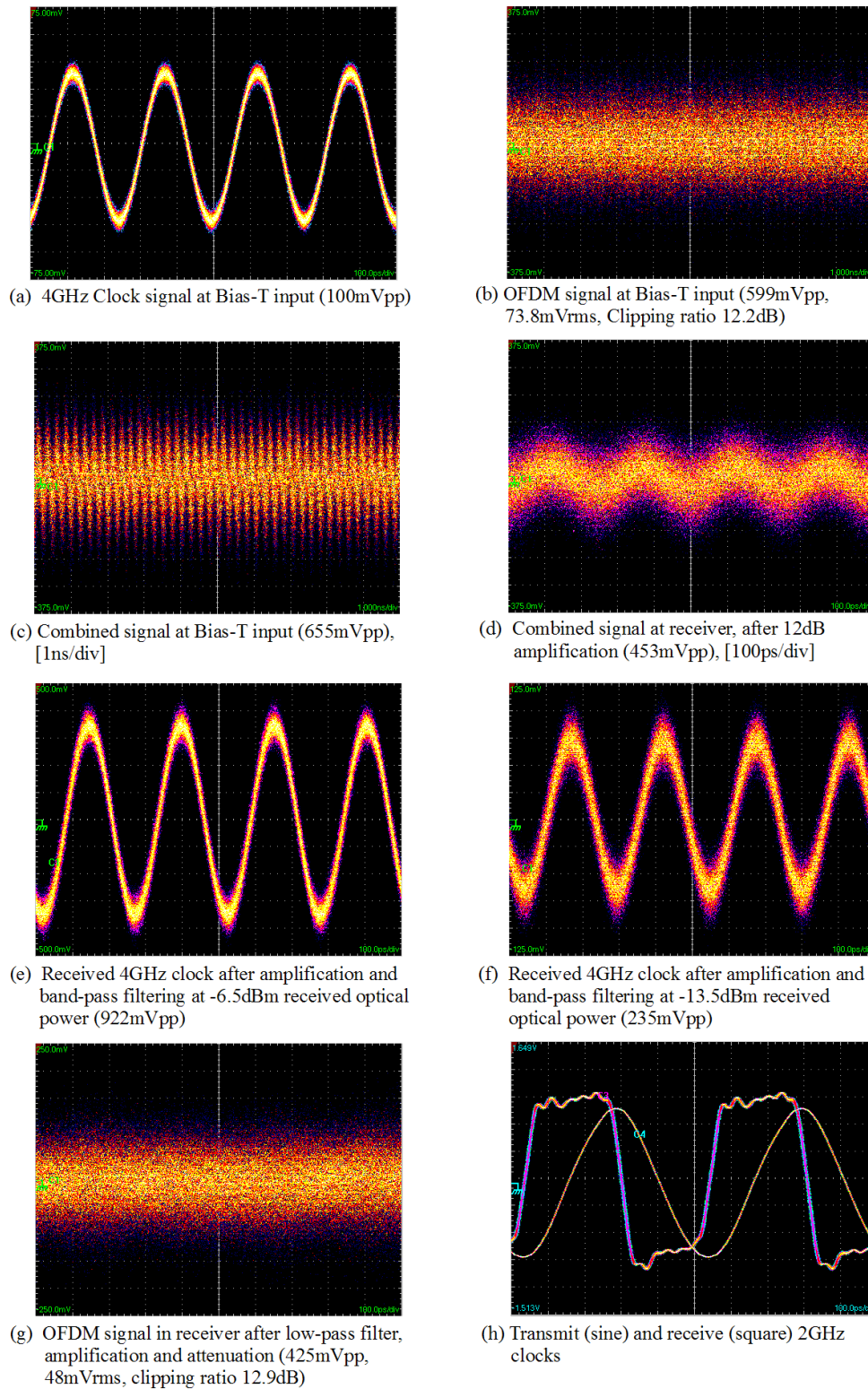
(h) Transmit (sine) and receive (square) 2GHz clocks

Fig. 7.4 Signal waveforms of the OFDM data signal, 4GHz synchronisation clock, combined signal and 2GHz system clocks measured in the transmitter and receiver.

clock to allow easy separation of the synchronisation signal from the OFDM signal by low order filters having a pass-band width as wide as 1GHz. To reduce the total bandwidth of the signal and thus the bandwidths of required optical and electrical components, the frequency of S_{CLK} can be reduced, this, however, increases the requirements of the band-pass filter in terms of narrower pass-band width and out-of-band blocking. The low-pass filtering used to extract the OFDM signal would similarly require higher performance to ensure any of the synchronisation clock signal remaining after filtering does not generate a significant aliasing product in the OFDM signal region as a result of under-sampling. More importantly, as the frequency spacing between the synchronisation clock and the OFDM signal band reduces, a threshold may be reached where unwanted interferences occur between the synchronisation clock and the OFDM signal band. Future research work is planned to investigate the dependence of the system performance on synchronisation clock frequency.

Fig. 7.5 Spectra of transmitted signal (at Bias-T input) and received signal (after first receiver RF amplifier)

7.4.2 Optimisation of Synchronously Clocked OOFDM System

To examine if any BER performance degradation occurs due to the presence of the synchronisation clock signal, the optimum electrical signal levels of the synchronisation clock and OFDM signals are investigated. Firstly, irrespective of the system BER, the allowed values of the S_{OOFDM} signal level and the S_{CLK} signal level under which synchronisation can be maintained is determined. Synchronisation is defined as the state

where the receiver's clock recovery circuit generates stable clocks locked to the transmitter's clocks. To detect whether or not the system is synchronised, the 2GHz DAC and ADC clocks are simultaneously fed to an oscilloscope from the test points indicated in Fig. 7.3, it is then possible to observe when the receiver clocks are stable and locked to the transmitter clock, as shown in Fig. 7.4(h).
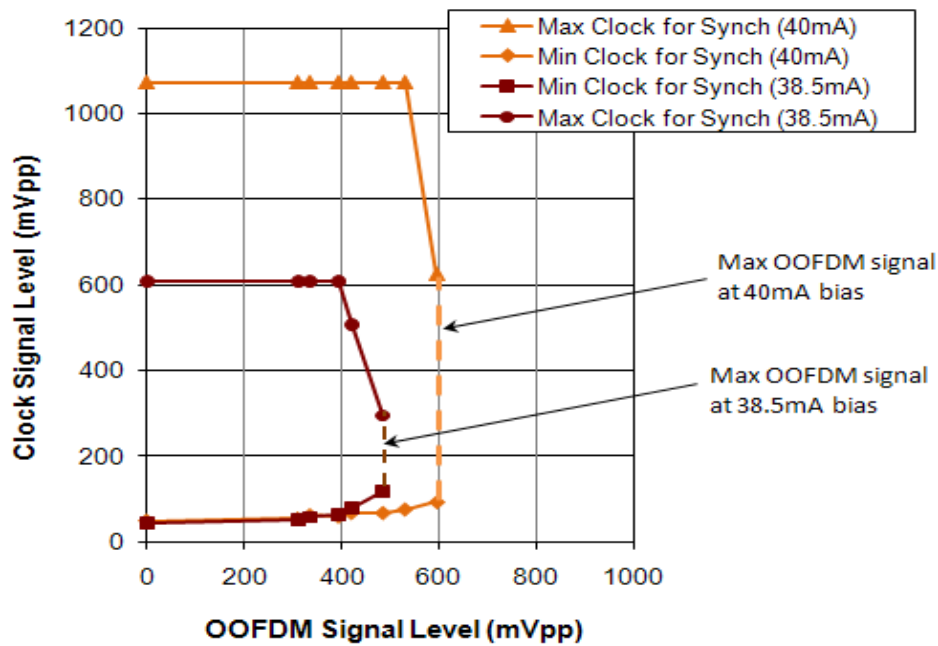
Fig. 7.6 Synchronisation region for varying OOFDM signal and clock levels

Fig. 7.6 plots both the maximum and minimum clock levels for synchronisation as the OFDM signal level is varied. Both signal levels are measured at the input to the bias-T (50Ω). The effect of laser bias current on the synchronisation range is also illustrated in Fig. 7.6. As expected, if the bias current is too low (<38.5mA) the clock and OFDM signal ranges over which synchronisation can be achieved are reduced; whilst for a bias current at 40mA a large synchronisation range is achieved. Further increase of the bias current beyond 40mA (42mA maximum) only has the effect of allowing a small increase in the maximum clock level at higher OFDM signal regions. At the 40mA bias current, the maximum permitted OFDM signal level to maintain synchronisation is approximately 600mVpp. It is worth pointing out however that the DFB laser can be driven up to around 900mVpp.

To further explore the impact of the synchronisation clock on the system performance, for the cases of the synchronisation clock present and absent, the system BER is measured as the peak-to-peak (PTP) amplitude of the OFDM signal is varied for the system configuration using the common clock. The system set up and parameters considered are identical for both cases. The measured results are shown in Fig. 7.7. In obtaining Fig. 7.7, the synchronisation clock amplitude is selected as 100mVpp, as this value provides a low clock amplitude sufficient to maintain synchronisation with a small margin above the minimum required clock level. A 40mA bias current is also used, as this provides the maximum range for the OFDM signal level where synchronisation can be achieved. It should also be noted that the above-mentioned bias current setting is also determined by the DML used.
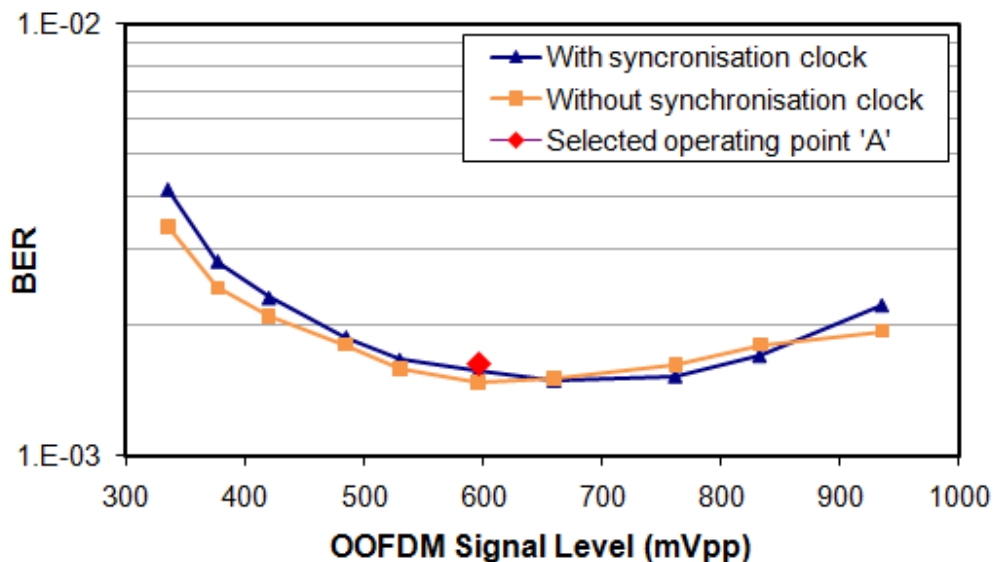
Fig. 7.7 BER variation with OOFDM electrical signal level (at bias-T input) with 40mA bias current, measured with and without the synchronisation clock present and operating with the common clock configuration.

Fig. 7.7 shows that the OFDM signal level has an exploitable operating region from approximately 530mVpp to 760mVpp where the OFDM signal power-dependent BER variation is negligible. More importantly, it is also shown that the presence of the synchronisation clock at the selected level has almost negligible impact on the system BER performances within the aforementioned exploitable operating region. Therefore, if an OFDM signal level of 600mVpp is selected, this is both within the exploitable operating region and the synchronisation region, so even though the OFDM signal level must be

limited to ~600mVpp to allow receiver synchronisation, this is still adequate to achieve optimum system performance.

In all experimental results presented below, the operating point (point A in Fig. 7.7) is selected, which corresponds to an OFDM signal level of 600mVpp, a synchronisation clock level of 100mVpp and a bias current of 40mA. This point allows operation with synchronous clock recovery in the receiver without any BER degradation compared to the minimum BER achieved with the common clock configuration. In Fig. 7.7, the occurrence of the minimum BERs for both cases considered is a direct result of the driving signal-induced variations in signal distortion/clipping and extinction ratio of the intensity modulated signals: A high OFDM signal level leads to a large OOFDM signal extinction ratio. This increases the effective signal-to-noise ratio (SNR) in the receiver, thus decreasing the BER; whereas a high OFDM signal level also causes increased signal waveform distortions and severe signal clipping, leading to an increase in BER. The co-existence of these opposing effects results in the trough shaped curve shown in Fig. 7.7. It is contrary to the expectation that when the synchronisation clock is introduced this would lead to a degradation in system performance due to the higher driving signal-induced signal distortion, which is not accompanied by an improvement in the effective extinction ratio of the OOFDM signal. An increase in the peak DFB driving voltage, however, only occurs when the positive (negative) clock signal peaks coincide with the OOFDM positive (negative) signal peaks, these new peaks have higher frequency content so any increase in distortion/clipping mainly occurs to the high frequency clock rather than the lower frequency OOFDM signal. The clock signal can therefore be introduced to increase the DFB driving voltage without degrading the BER performance.
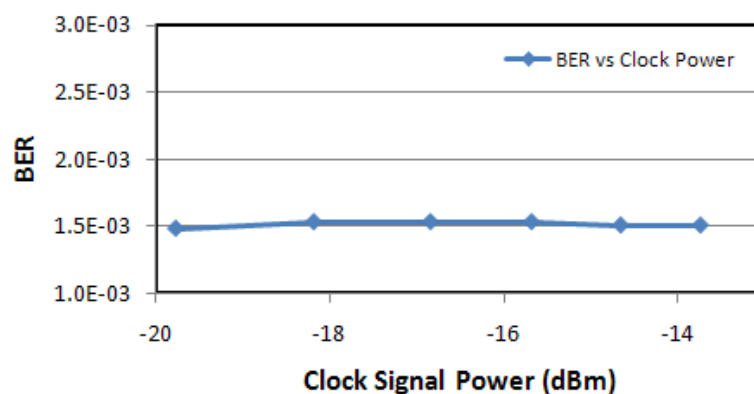

Fig. 7.8 BER variation with synchronisation clock power under optimum operating conditions

Having discussed the OFDM signal voltage dependent system BER performance, Fig. 7.8 is plotted to investigate the influence of the synchronisation clock power level on the system BER performance. In obtaining Fig. 7.8, the transmission system is configured for synchronous clocking subject to the optimum OFDM signal voltage identified in Fig. 7.7. It can be seen in Fig. 7.8 that the clock signal power can be varied over a range of at least 6dB without affecting the system BER. Such a wide dynamic range implies that the system is very robust to variations in the clock signal power. It should also be noted that, to maintain synchronisation, the tested clock signal power region is limited to the maximum output adjustment range of the frequency synthesiser employed in the experiments, the dynamic clock range may therefore exceed 6dB.

7.4.3 Performance of Synchronously Clocked OOFDM System

For 11.25Gb/s over 25km SSMF OOFDM signal transmission in the DML-based IMDD system under the identified optimum operating conditions, the system BER performance as a function of received optical power is plotted in Fig. 7.9 for both the common clock configuration and the synchronous clock configuration. The results clearly show that the BER performance of these two cases are identical, implying that the synchronous clocking technique allows a high quality clock to be recovered in the receiver, and more importantly, that the technique does not result in any BER or optical power budget degradation. The high quality of the recovered clock can also be seen in Fig. 7.4(h), where the 2GHz clock in the receiver (C_{ADC}) with a peak-to-peak jitter as small as 10ps is clearly locked to the 2GHz clock in the transmitter (C_{DAC}). Furthermore, Fig. 7.10 presents comparisons of subcarrier constellations measured before equalisation in the receiver, between the common and recovered clock cases. The observed high resemblance between corresponding subcarrier constellations further verifies the high performance of the synchronous clocking technique.

The optical back-to-back BER performance is plotted in Fig. 7.9, which shows that there is an optical power penalty of <1dB at a widely adopted forward error correction (FEC) limit of 2.3×10^{-3}. Furthermore, the minimum BER achieved for both clocking methods is ~1.5×10^{-3}, which is slightly higher than that obtained in section 5.3.3.3 for 11.25Gb/s transmission over 25km SSMF with the common clocking approach. Such a difference is due to the utilisation of extra electrical components including amplifiers, couplers and

splitters, as illustrated in Fig. 7.3. These additional components give rise to increased noise and signal distortions. A main source of distortion is believed to originate from the RF component ports, which do not offer a sufficiently high and uniform return loss over the wide signal spectral range (0-4GHz).
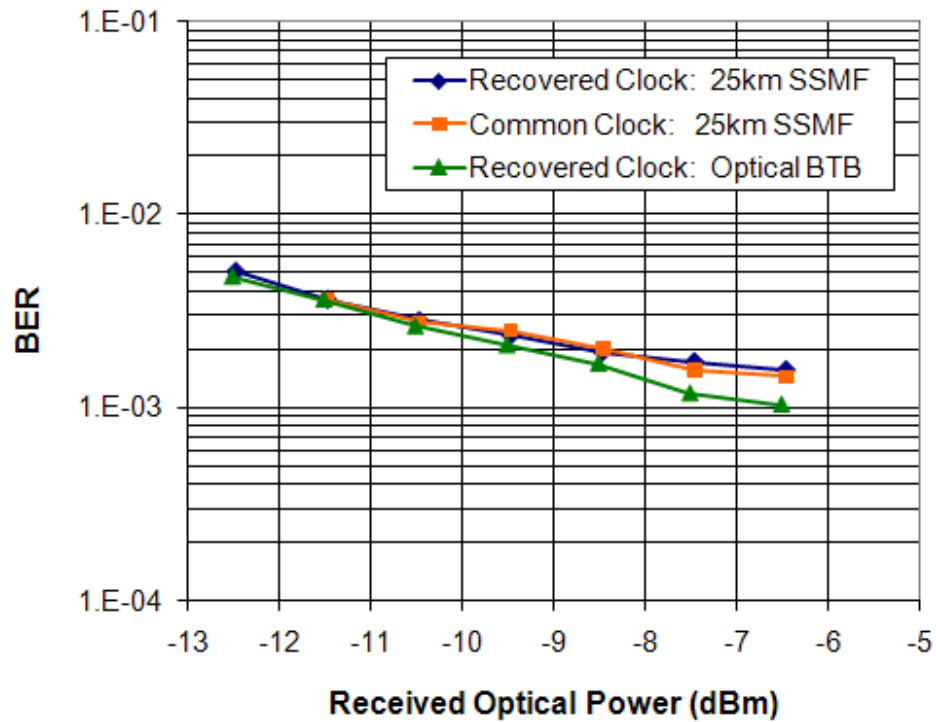
Fig. 7.9 BER performance of real-time 11.25Gb/s OOFDM with recovered clock and common clock for IMDD 25km SSMF and optical back-to-back performance with recovered clock.

Experimental measurements also indicate that the clock recovery can operate with a received optical power as low as -13.5dBm. This is also verified in Fig. 7.4(f), where the received 4GHz clock at a received optical power of -13.5dBm shows more jitter and noise compared to the received 4GHz clock at a received optical power of -6.5dBm, as presented in Fig. 7.4(e). The 7dB reduction in received optical power does not have an effect similar to a 14dB reduction in transmitter's electrical power, as such an electrical power reduction destroys the system synchronisation. This implies that the proposed technique is highly tolerant to variations in the received optical power, further demonstrating the robustness of the synchronous clocking technique.
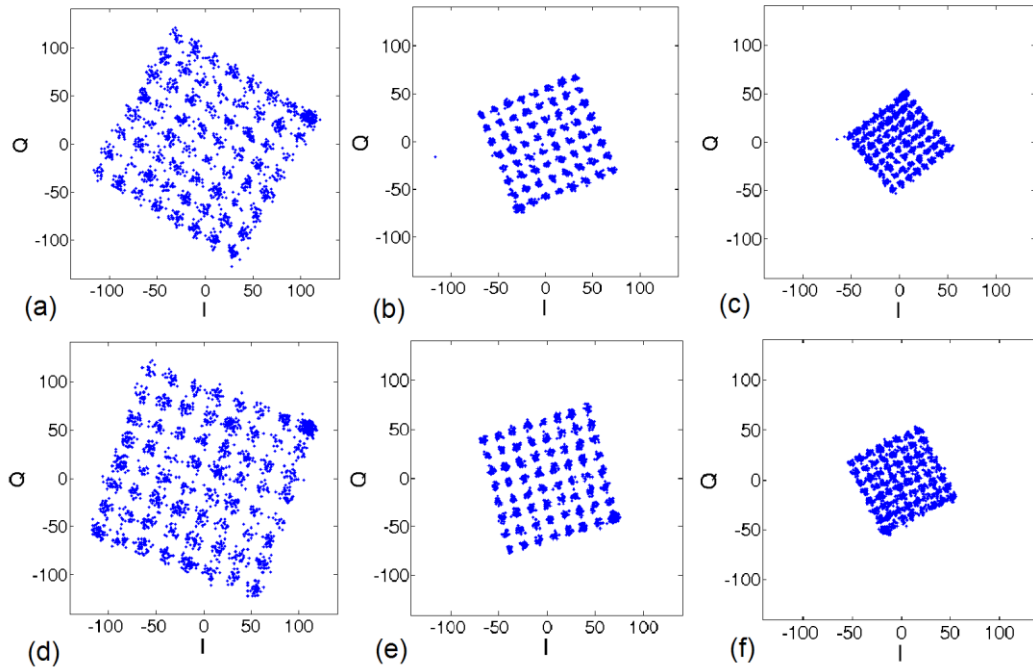
Fig. 7.10 Received 64-QAM subcarrier constellations before channel equalisation for 25km SSMF with common clock (a) 1st SC, (b) 8th SC, (c) 15th SC and recovered clock (d) 1st SC, (e) 8th SC, 15th SC

7.4.5 Performance Stability of Synchronously Clocked OOFDM System

The system performance stability over time is examined for both the common clock and synchronous clock methods. It is known that the DFB laser wavelength may drift slowly with small changes in laser temperature. When the common clock configuration is used, a drift in laser wavelength results in a wavelength-dependent differential time delay between the clock signal and the received OFDM signal. As manual symbol alignment is used, the change in the differential time delay effectively shifts the symbol alignment in the receiver, thus leading to the BER degradation. This is the physical mechanism underpinning the BER evolutions shown in Fig. 7.11(a), where the first plot shows the BER increasing after initial symbol alignment as the symbol alignment deteriorates; whilst the second plot shows the BER reducing as the symbol alignment improves. When the BER drifts it is always possible to restore the system operation to the minimum BER by only readjusting the symbol alignment.

In sharp contrast, when BER stability is observed with the synchronous clocking technique, it is seen to be significantly more stable as shown in Fig. 7.11(b). The BER can

remain stable for over one hour before symbol realignment is needed. The improved stability is due to the fact that the clock signal is transmitted with the OOFDM signal, therefore any change in the signal propagation time due to the laser wavelength drift is experienced by both the OFDM signal and the clock, therefore no significant differential time shift is produced within the experimental measurement period to significantly degrade the symbol alignment and hence the BER. However, the DFB wavelength drift with small changes in laser temperature can still result in very small BER deteriorations over a long period of time, as observed in Fig. 7.11(b). This is mainly due to the wavelength dependent chromatic dispersion-induced differential time delay between the OFDM signal and the clock signal. This BER drift effect is now due to the small differential wavelength variation as opposed to the absolute wavelength change in the common clock case, thus dramatically reducing the impact on the BER drift.
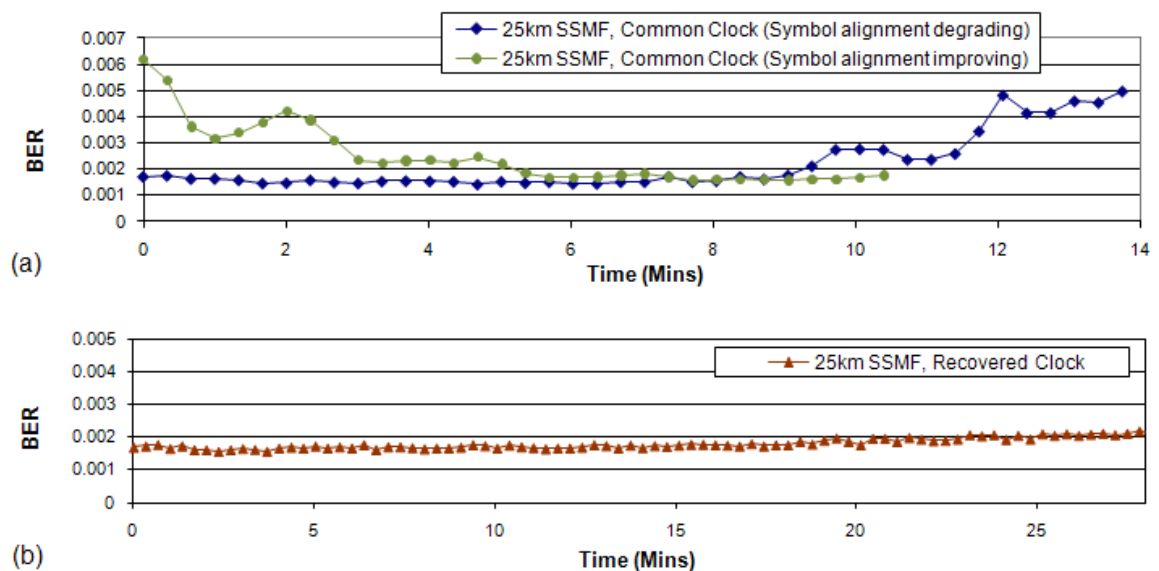
Fig. 7.11 BER performance stability for (a) common clock configuration and (b) synchronous clocking configuration

7.5 Conclusion

Synchronous clock recovery has been proposed, experimentally demonstrated and optimised in a real-time end-to-end DML-based 11.25Gb/s OOFDM IMDD system. The technique offers a low-cost, low-complexity, DSP-fee, robust solution with no BER performance or optical power budget penalty and achieves improved BER stability. The

work presented here is a vital step towards the realisation of practical OOFDM transmission systems. Furthermore this work is also important as it potentially offers a simple and highly effective solution for network synchronisation in OOFDMA PONs. An important area for future research work is to implement the proposed synchronisation technique in OOFDMA PONs.

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8   An   OOFDM   Symbol   Alignment   Technique Based on Low Power DC Offset Signalling

Contents

8.1 Introduction

In chapter 7, real-time end-to-end OOFDM transmission has been demonstrated with the inclusion of a synchronous clock recovery solution for independent receiver operation. However symbol synchronisation for STO compensation in the receiver has been performed using a manual alignment technique. Automated symbol alignment is also a major technical challenge to achieving a fully autonomous synchronised OOFDM system. As a principal application of OOFDM of interest of the thesis is point-to-multipoint PONs, which can be supported by the synchronous clocking technique, a symbol synchronisation method suitable for point-to-multipoint PON applications in addition to point-to-point systems is an essential requirement to make OOFDM-based PONs a practical reality.

Synchronisation methods for STO compensation in existing OFDM standards were discussed in section 2.3.8, where the fundamental principle was to insert training patterns or employ repeated sequences in the transmitted signal and perform cross-correlation or auto-correlation in the receiver to locate the known patterns and thus identify the symbol positions. These approaches rely on the fact that only one network element is transmitting at once and uses the actual OFDM signal for the symbol synchronisation. A synchronisation technique based on exploiting the repeated cyclic prefix within an OOFDM symbol has been demonstrated in the real-time end-to-end OOFDM system by Jin, et al. [1-3], this solution is a DSP receiver function based on subtraction operations to reduce complexity compared to the multiplication operations used in conventional correlation. The technique [1-3] is highly effective and accurate for point-to-point OOFDM systems including OOFDM-WDM-PONs implemented as multiple point-to-point links. The aforementioned technique can also be applied to point-to-multipoint PONs with a common optical channel, such as OOFDMA-PONs, however in this case the existing upstream network traffic must be interrupted during initial ONU symbol alignment and during symbol alignment tracking and realignment.

The symbol synchronisation technique proposed and demonstrated here is designed to achieve symbol, timeslot and frame alignment of an ONU's upstream and downstream signals without the need to interrupt existing upstream ONU traffic. This is a highly advantageous synchronisation function which can provide a simple and effective means for

synchronisation in OOFDMA PONs. As far as the author is aware, no solutions have been published to address this fundamental OOFDMA-PON synchronisation issue.

Here a symbol synchronisation technique is proposed and experimentally demonstrated that meets the requirements of upstream OOFDMA-PON synchronisation when used in combination with the previously described synchronous clocking technique as it is essential that all ONUs in the PON are synchronously clocked [4,5]. The proposed symbol synchronisation technique is based on the transmission of a low power DC offset signal and a simple addition/subtraction-based cross-correlation function in the receiver. The operating principle of the technique is fully described in section 8.2. The characteristic advantages of the technique are summarised below:

- Low complexity and high accuracy: The technique is purely a DSP function so does not require any additional discreet optical or electrical components. The DSP logic is based solely on addition/subtraction operators thus not requiring any multipliers. Also no extra transmission bandwidth is required.

- High operation speeds: The technique is suitable for OOFDM optical transmission systems at any arbitrary bit rates.

- Wide flexibility: The technique can be implemented in both point-to-point and point-to-multipoint OOFDM transmission systems.

- Added physical layer network security: The technique offers an effective means of making communications by an unauthorised user virtually impossible.

- Compatibility: Excellent compatibility with existing network architectures and services.

- Highly practical: Able to operate in a live point-to-multipoint network without introducing any disruption to existing network traffic.

8.2 Symbol Synchronisation Operating Principle

The symbol synchronisation technique [4,5] is based on the principle that the DC level of each OOFDM symbol has no influence on the non-zero frequency subcarriers at the output of the FFT, a different DC offset can therefore be applied to each individual OOFDM symbol. This operation produces an encoded synchronization signal, S_{ALIGN}, which is added to the OOFDM signal, S_{OOFDM}, at the transmitter. For simplicity but without losing generality, two different DC offsets with identical amplitude but opposite polarities, $+P$ and $-P$, are added alternately to successive symbols, S_{ALIGN} is thus a square wave with a period of 2 symbol periods of $2 \cdot T_S$ and a peak-to-peak amplitude of $2P$. The transmitted signal S_{TX} as illustrated in Fig. 8.1. is as follows:
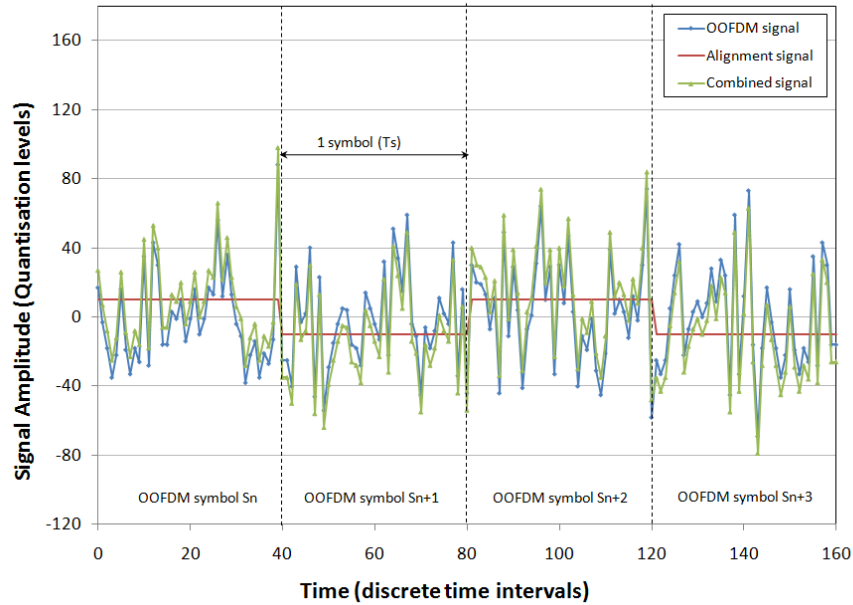
$$S_{TX} = S_{OOFDM} + S_{ALIGN} \tag{8.1}$$

Fig. 8.1 OOFDM signal combined with synchronisation DC offset signal

The corresponding received signal S_{RX} can be written as:

$$S_{RX} = S'_{OOFDM} + S'_{ALIGN} + S_N \tag{8.2}$$

where S_N represents system noise.

In the receiver, a cross-correlation method is used to detect the position of S'_{ALIGN}. A signal S_{CORR} is generated which has an identical waveform shape to S_{ALIGN} and amplitude of ± 1 to simplify computation. By computing the cross-correlation between S_{RX} and S_{CORR}, symbol alignment offset can be determined based on the location of the correlation peaks. This is because there is no correlation between S_{CORR} and either S'_{OOFDM} or S_N due to their Gaussian random characteristics, the cross-correlation is therefore entirely dependent on S'_{ALIGN}. An arbitrarily positioned sequence of $2 \cdot M \cdot Z$ samples is processed, where Z is the total number of samples in an OOFDM symbol, and M is a sufficiently large integer selected to give clear correlation peaks. As S_{ALIGN} is cyclic, a symbol summation, or accumulation, can be performed before the cross-correlation. A signal S_{SUM} is calculated using Eq. (8.3) where $S_{SUM}(n)$ is the nth sample within S_{SUM} and $n=1$ to Z. S_{SUM} is thus the sum of M sequences of Z consecutive samples spaced at intervals of $2 \cdot Z$ samples. If M is large enough the waveform of S_{SUM} will take on the shape of S_{ALIGN} as the Gaussian random characteristics of S'_{OOFDM} and S_N results in their summations both tending to zero. The exact shape of S_{SUM} will depend on the symbol alignment offset relative to the arbitrarily selected samples, signal transitions from positive to negative, and vice-versa, will coincide with the OOFDM symbol boundaries.

$$S_{SUM}(n) = \sum_{k=0}^{M-1} S_{RX}(n + 2kZ)$$

$$= \sum_{k=0}^{M-1} [S'_{OOFDM}(n + 2kZ) + S'_{ALIGN}(n + 2kZ) + S'_N(n + 2kZ)] \quad (8.3)$$

The cross-correlation is then performed between S_{SUM} and S_{CORR} with the relative offset, v, of S_{CORR} varied from 0 to (2·Z)-1 and the correlation *COR(v)* for each offset calculated using Eq.(8.4). The sequence of values *COR(0)* to COR_{2Z-1} provides a correlation profile, C_{PROF}, where the position of the peaks indicate the offset where the highest correlation between S'_{ALIGN} and S_{CORR} occurs thus identifying the position of the OOFDM symbol.

$$COR(v) = \sum_{k=0}^{(2Z)-1} S_{SUM}(k) \cdot S_{CORR}(k + v) \quad (8.4)$$

A positive (negative) peak will occur in C_{PROF} when S_{CORR} and S'_{ALIGN} are in phase (in opposite phase) both of which indicate symbol alignment as S_{CORR} and S_{ALIGN} have a period

of $2 \cdot T_S$. By taking $|COR(v)|$ only positive peaks then occur in C_{PROF} and it is only necessary to select Z samples in every $2 \cdot Z$ samples to ensure a peak is detected. Fig. 8.2 shows the ideal variation of $|COR(v)|$ against offset v for an arbitrary symbol alignment offset of w_0. It should be noted however that the maximum allowed DC offset amplitude is limited as it affects the DC bias point of the directly modulated laser (DML), and the total signal amplitude is limited by the full-scale ranges of the DAC/ADC.
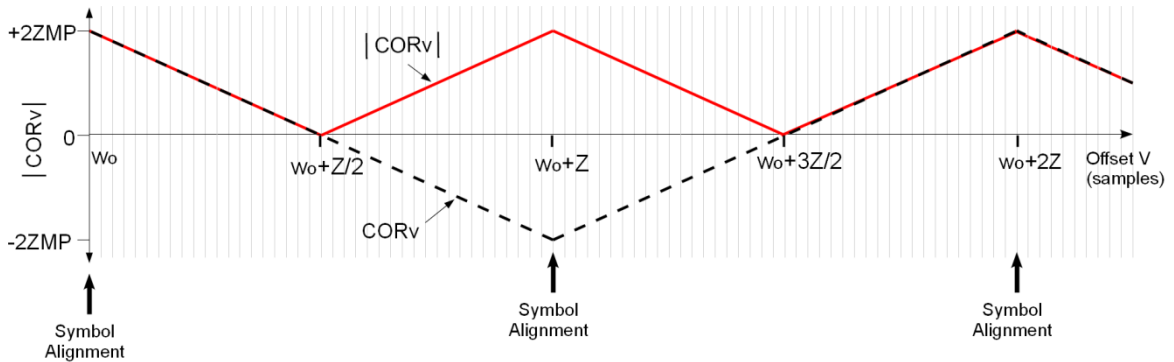
Fig. 8.2 Ideal correlation profile for symbol alignment offset w_0.

As previously discussed the symbol synchronisation technique is designed for application in OOFDMA-PONs to achieve downstream and upstream alignment of symbols, timeslots and frames. Here the mechanism for achieving synchronisation of an ONU to a live PON is described. For downstream symbol alignment, the OLT continuously transmits a synchronisation signal which all ONUs use for symbol alignment. In the upstream direction, the OLT controls the synchronisation process, allowing only one ONU to transmit a synchronisation signal at any one time, for each ONU the OLT detects its symbol offset and then notifies it so that it can correctly realign its symbol positions. By constructing the synchronisation signal from a coded sequence of DC offsets enhancements can be made that offer a number of key features. For upstream and downstream frame/timeslot alignment a suitably coded synchronisation signal with the same length as one or more OOFDMA frames allows the OLT to detect an ONU's frame alignment offset by performing a cross-correlation over a period equivalent to one or more coded sequence lengths. ONU frame alignment offset is detected and then corrected in the ONU, thus each ONU is timeslot aligned to the network before initiating OOFDMA signal transmission and hence avoiding any upstream ONU signal collisions in the operational network. Symbol offset can drift slowly over time, as described in section 7.4.5, therefore

the OLT would then periodically track and correct any symbol offset drift for each ONU in turn.

Furthermore, by coding the downstream synchronisation signal with a sufficiently long encrypted key code will make it virtually impossible for an unauthorised user to achieve synchronisation thus achieving network security at the physical layer.

8.3 Symbol Synchronisation DSP Algorithm Implementation
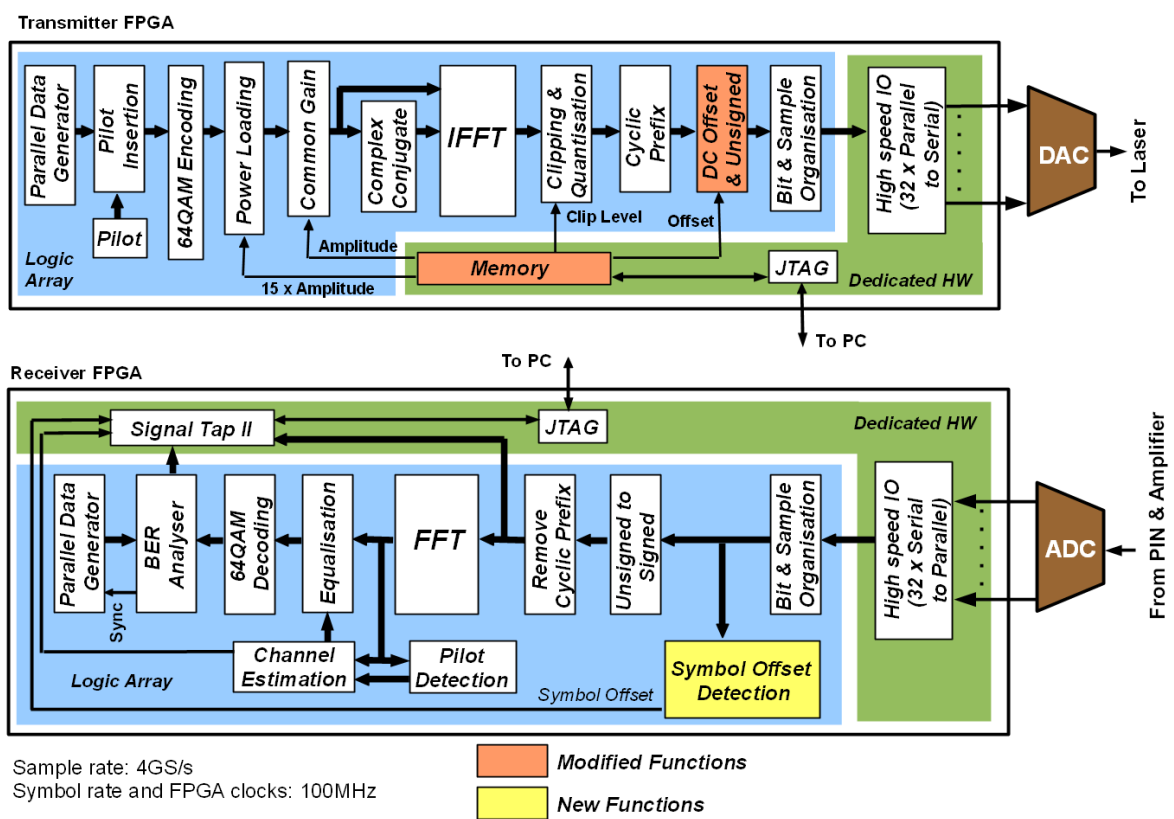
Fig. 8.3 Real-time OOFDM Transceiver Architectures for 11.25Gb/s Line Rate with Symbol Synchronisation Functions

Fig. 8.3 shows the DSP functional architecture for the transmitter and receiver designs with symbol offset detection functions included. The design modifications compared to the 11.25Gb/s functional architectures described in section 5.3.2 are highlighted. The transmitter is modified to incorporate the "DC offset" function. Whereas the receiver incorporates the "Symbol Offset Detection" function which detects symbol offset according to the principle described in section 8.2.

8.3.1 Offset Signal Addition in the Transmitter

Compared to the design in section 5.3.2 the transmitter's FPGA hardware is modified to allow an on-line adjustable DC offset to be added to the OFDM signal's symbols. The block in the original design that performs the conversion to unsigned samples is modified to add the DC offset signal. The Simulink top level model is shown in Fig. 8.4. The 256-bit input bus is expanded to extract the 32x 8-bit signed OFDM signal samples in parallel, these are passed to the "Offset_Adder" block which adds a single value to all samples simultaneously, the value to be added is generated by the "Offset_Generator" block. The 32 modified signal samples are then concatenated back into a 256-bit output bus.

The "Offset Generator" block is shown in Fig. 8.6. The required DC offset value P is acquired from an embedded memory cell which can be edited during operation. The negative offset is generated and a 2 port multiplexer and a 1-bit counter are employed to generate an offset signal which alternates between +P and −P every symbol period. The generated DC offset signal is then added to 128 which implements the signed to unsigned conversion of the samples during the subsequent addition.

The top level of the "Offset_Adder" block is shown in Fig. 8.5, where 32 identical blocks are shown, each block adding the value from the "Offset Generator" to one of the 32 samples. The schematic of the individual offset adder blocks is shown in Fig. 8.7. A simple adder is used to add the offset to the samples, however circuitry is also implemented to limit the sample values to the 8-bit unsigned range of 0 to 255. Alternatively the DC offset could be added to the samples before clipping and quantisation to avoid the extra resources needed for the range limiting function, however for this case as the clipping level is adjusted the subsequent scaling for quantisation would also scale the DC offset. Avoiding the dependency of absolute DC offset value on clipping level simplifies the parameter optimisation processes.
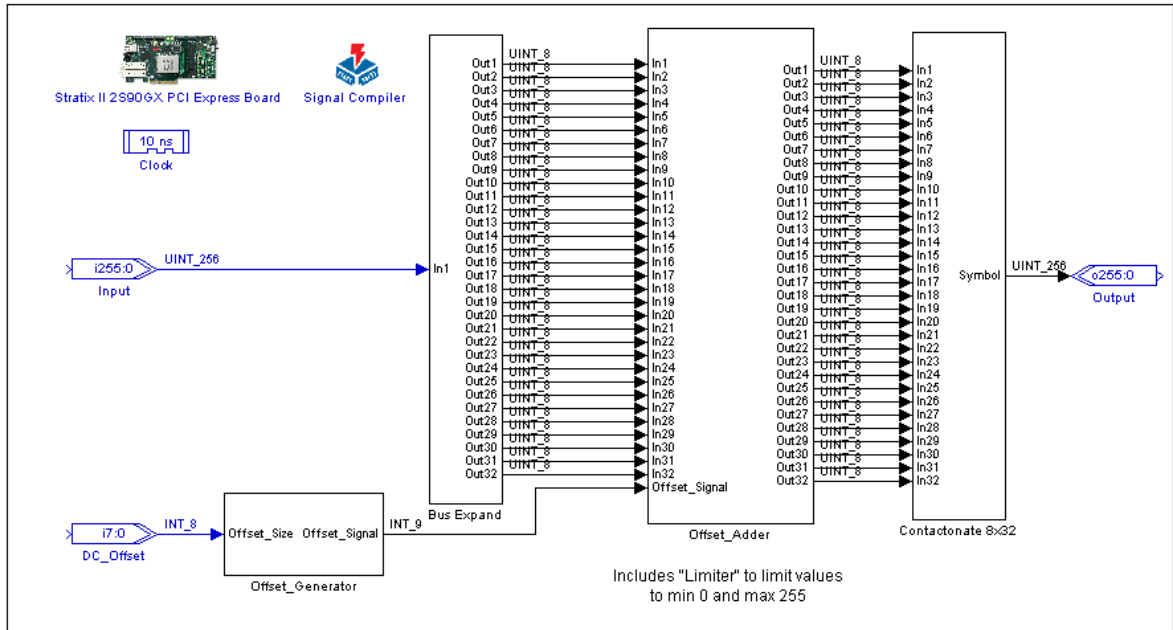
Fig. 8.4 Offset Signal Block Top Level
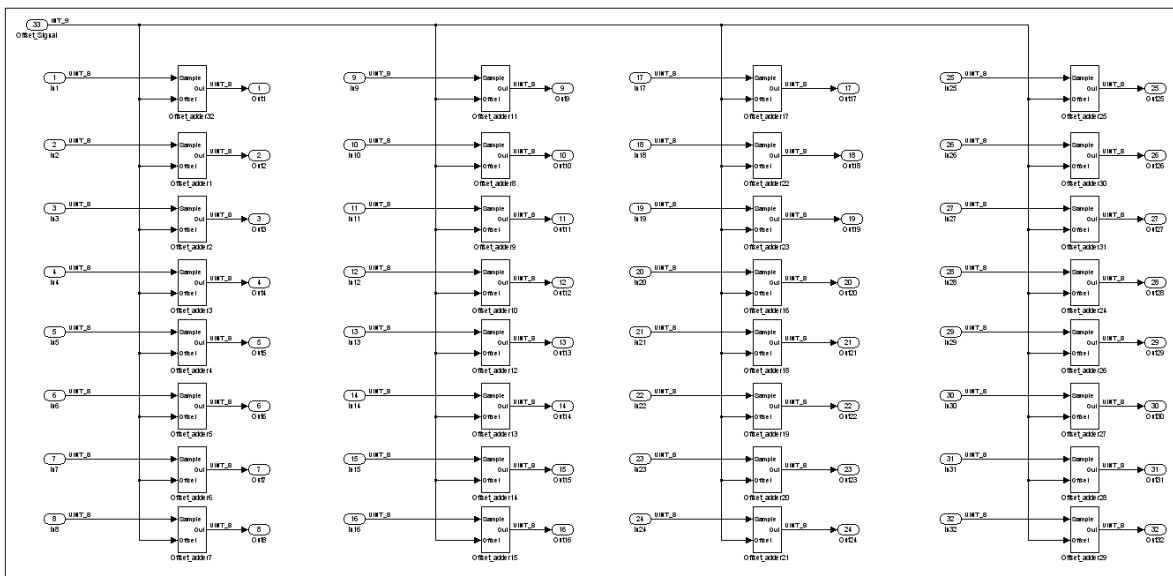
Fig. 8.5 Offset Adder Block
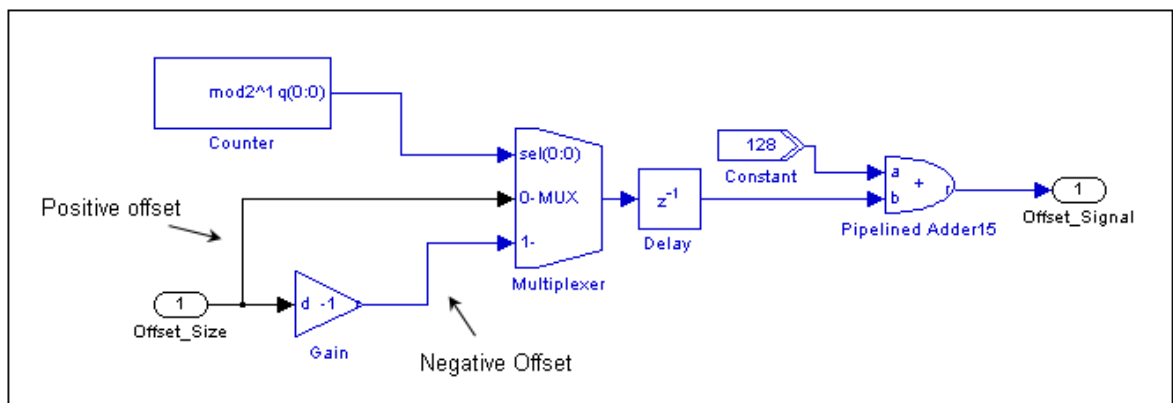
Fig. 8.6 Offset Signal Generator

248
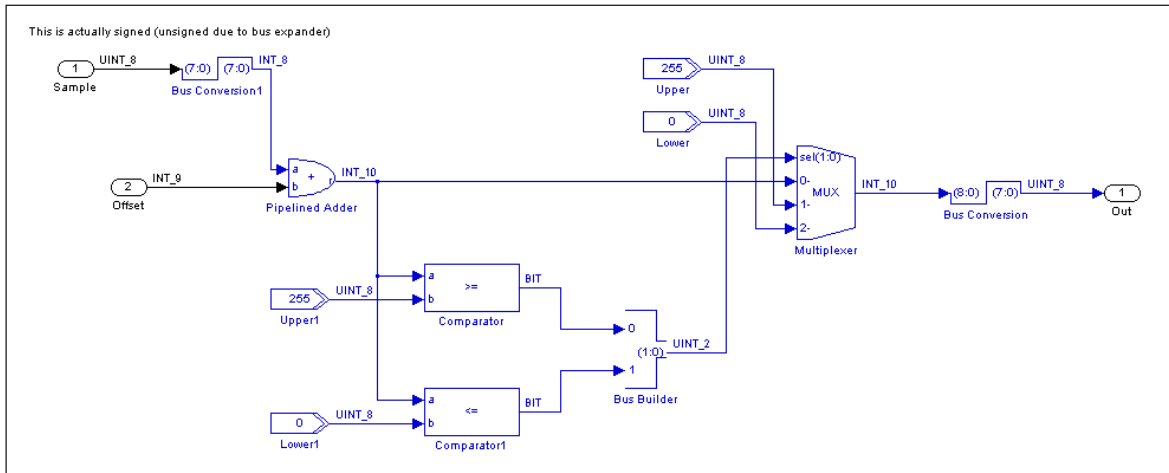
Fig. 8.7 Offset Signal Adder and Limiter Block

8.3.2 Symbol Offset Detection in the Receiver

The receiver's FPGA hardware is modified to incorporate a "Symbol Offset Detector" block implementing the cross-correlation algorithm as defined in section 8.2 and 8.3. Fig. 8.8 shows the top level Simulink™ model of the "Symbol Offset Detector". The 320-bit input bus, updated at the symbol rate, is first separated into 40×8-bit samples and then input to a bank of D-type flip-flops clocked at half the symbol rate, this therefore only captures 40 consecutive samples out of every 80 consecutive input samples. This is due to the fact that the synchronisation signal period is 80 samples and only 40 samples need to be processed to ensure capture of a symbol edge. These 40 samples then feed the "Symbol Synchroniser" block which performs the cross-correlation function.

The schematic of the "Symbol Synchroniser" block is shown in Fig. 8.9. An accumulation function is first individually performed on each of the 40 incoming samples by the "Accumulators" block which contains 40 parallel instances of the individual sample accumulator function as shown in Fig. 8.10. The 40 output samples of the "Accumulators" block will form a signal corresponding to S_{SUM} with a waveform shape similar to the synchronisation signal S_{ALIGN}. Following the "Accumulators" block is the "Correlators" block which simultaneously performs 40 separate correlation functions between the accumulated signal S_{SUM} and the 40 different versions of the alignment signal, corresponding to $S_{CORR,}$ as the relative offset is varied from 0 to 39 samples. The "Correlators" block outputs the unchanged input samples, corresponding to S_{SUM}, and the correlator outputs which form the correlation profile corresponding to $C_{PROF.}$ In order to

observe the S_{SUM} and C_{PROF} waveforms and minimise Signal Tap II nodes, two "Parallel-to-Serial" blocks are implemented which capture the signals and output them in serial form. Signal Tap II is used to capture the serial outputs and allows observation of the associated signal waveforms. To detect the symbol offset the C_{PROF} samples are fed to a peak detector block which employs a sequence of comparators and multiplexers to iteratively select the peak sample vale from C_{PROF} and generate the corresponding sample offset value. The only output required from the "Symbol Synchroniser" block is the detected symbol offset, the other output signals shown in Fig. 8.8 are for viewing the various signals for analysis and debugging purposes.
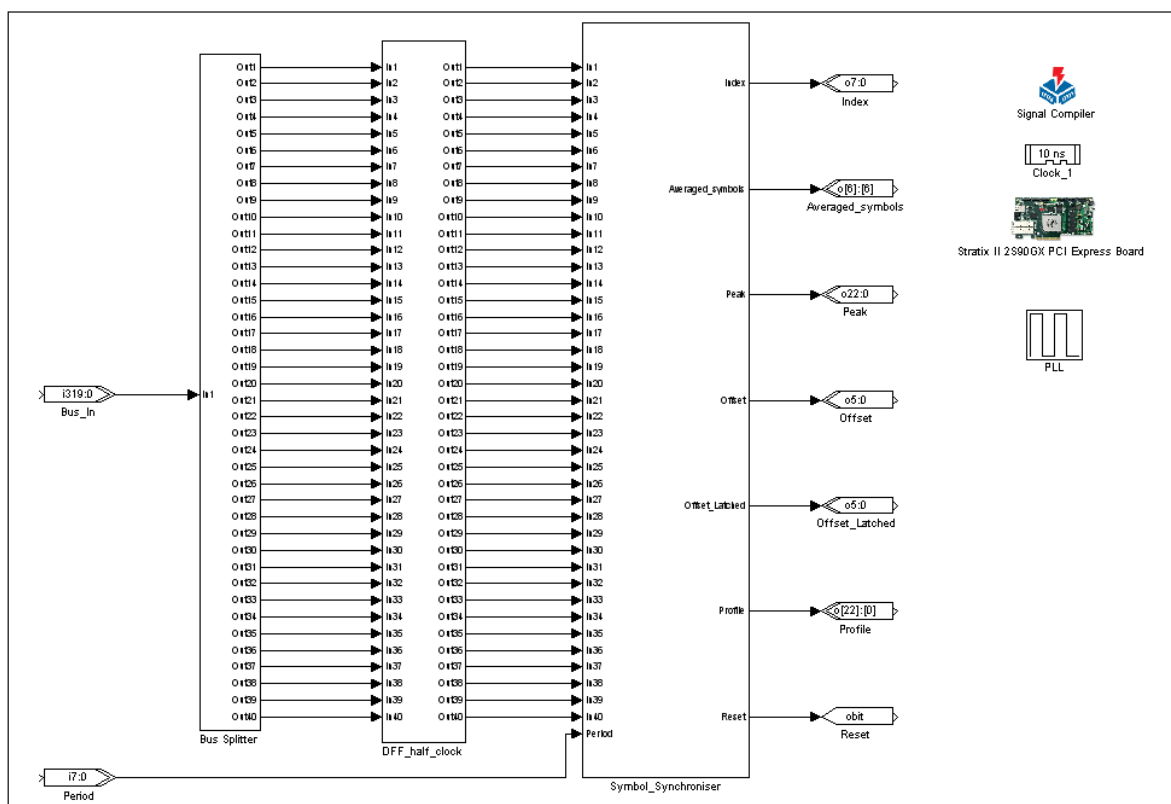
Fig. 8.8 Symbol Offset Detection: Top Level Simulink Model

A reset generator block, as shown in Fig. 8.9, generates a reset signal after a fixed number of symbol periods corresponding to the correlation period of $2 \cdot M$ symbols. To allow optimisation of the correlation period the parameter M is stored in an embedded memory cell which can be updated online. At the end of each correlation period the reset signal resets the accumulators to zero, latches the resultant symbol offset value output from the peak detector block and also latches the S_{SUM} and C_{PROF} waveforms at the input of the two

"Parallel-to-Serial" blocks. S_{SUM} and C_{PROF} waveforms and the symbol offset value are therefore updated every $2 \cdot M$ symbols.
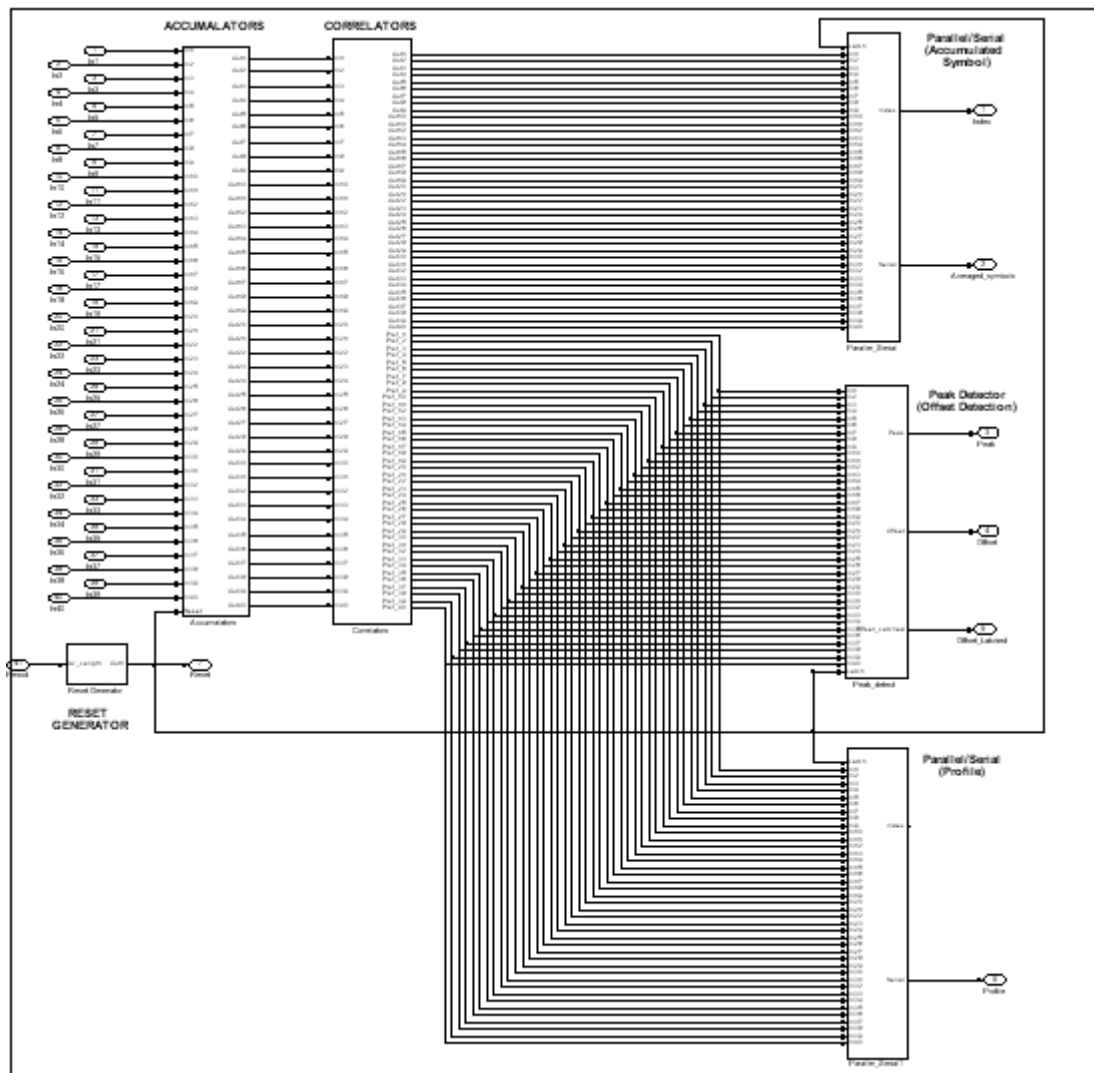
Fig. 8.9 Symbol Synchroniser Block

The operation of the individual sample accumulator, as shown in Fig. 8.10, will be described further. The block first removes the DC level (127) associated with the unsigned ADC samples to generate signed 8-bit samples, a 2 input adder is then used as an accumulator by feeding back the output to one of the inputs. To reset the output to zero the output is fed via a 2-input multiplexer, with zero at one input, so that the accumulator output can effectively be forced to the zero to reset the accumulator.
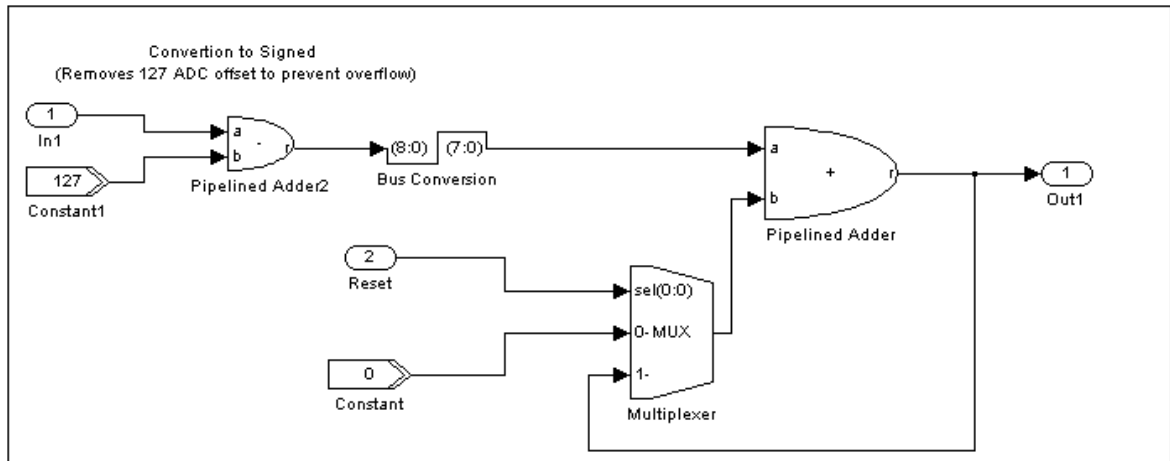
Fig. 8.10 Individual Sample Accumalator

The structure of the "Correlators" block is depicted by Fig. 8.11 and Fig. 8.12 (a,b). The structure allows the S_{SUM} signal to pass through whilst simultaneously connecting to the inputs of 40 correlator blocks. Each correlator block performs a unique correlation with a version of S_{CORR} with a specific offset value, v. As previously stated $S_{CORR}(v)$ is selected to have amplitude of ± 1 therefore no multiplication operations are required and the corresponding sign of $S_{CORR}(v)$ determines if the S_{SUM} sample is added or subtracted when performing the effective sample summation. $S_{CORR}(0)$ will have all values set to +1 for example so the correlation simply consists of the summation of all S_{SUM} samples. Fig. 8.12(b) shows the correlator for $S_{CORR}(8)$, the first 8 samples of S_{SUM} must be multiplied by -1 therefore these samples are subtracted and the remaining samples added to perform the correlation. More generally, for correlation with signal $S_{CORR}(v)$ the first v samples of S_{SUM} are subtracted and the remaining samples added.
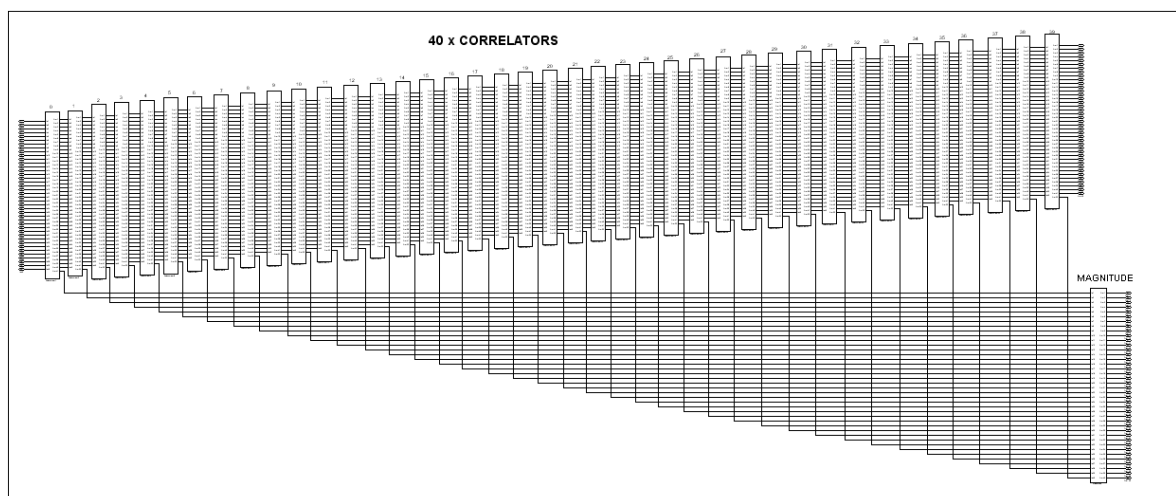
Fig. 8.11 Correlator Block with 40 Parallel Correlators for Offset Values 0-39
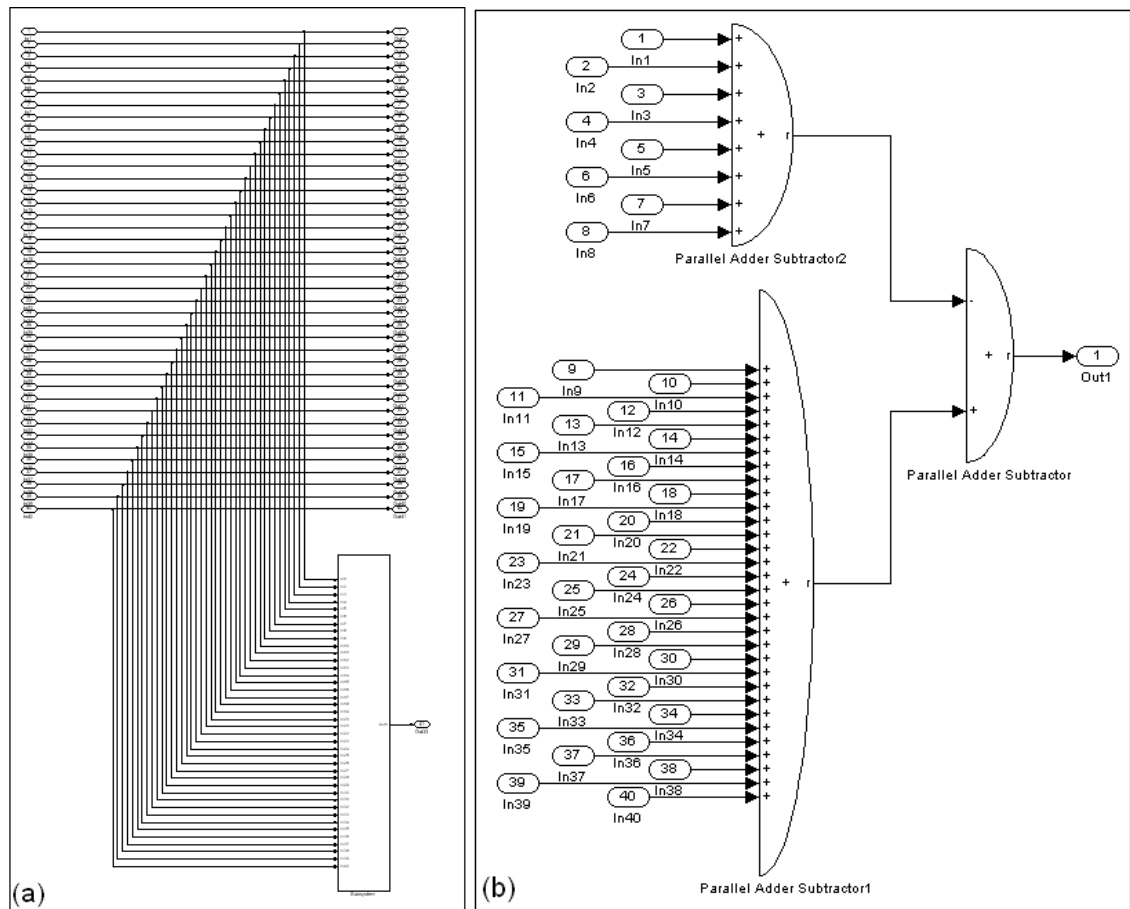
Fig. 8.12 Individual Correlator for Specific Offset (a) Correlator Top Level, (b) Low Level Block for Offset of 8 Samples

It is important to note that the correlation function does not need to be performed by parallel correlator blocks as this approach may not be the most efficient use of logic resources. Alternatively, the S_{SUM} signal can be held in a register after the end of each correlation period, a single correlator block can then be employed to perform 40 separate correlations in sequence with the S_{CORR} signal being updated appropriately between correlations. The sequence of correlation values generated forming C_{PROF} must then be stored to registers for input to the peak detector.

8.4 Experimental System Setup
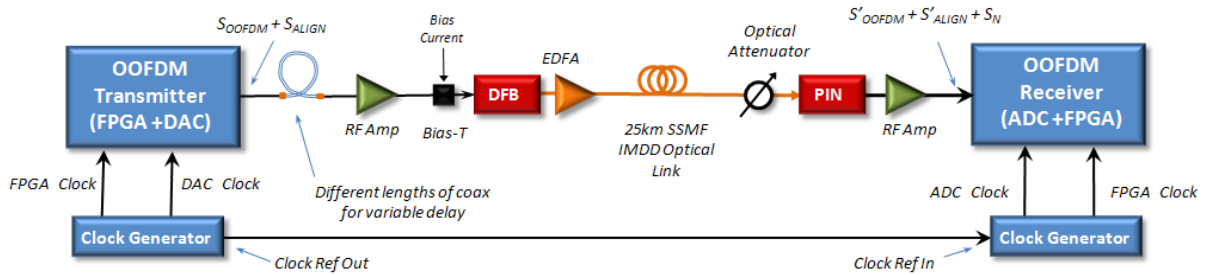
Fig. 8.13 Experimental SystemSet Up for Symbol Synchronisation

The experimental real-time OOFDM system setup operating at 11.25Gb/s raw data rate is shown in Fig. 8.13. The system is a point-to-point IMDD link with 25km SSMF employing a DML in the transmitter, the set up is virtually identical to that used in section 5.3.2 for the initial 11.25Gb/s experiment. All fixed DSP system parameters are unchanged and live adaptation of system parameters such as clipping level, subcarrier power levels and DML operating conditions is again utilised to optimise the system performance. The same DFB is employed with the addition of a 25dB RF amplifier, in combination with variable attenuators added before the bias-T, this is because it was found that increasing the DFB drive voltage achieved a slight improvement in BER performance. At the receiver the photodetector and RF gain stage are identical to that employed in section 5.3.2. The optimised DFB operating conditions were a bias current of 40mA and a driving voltage of ~600mVpp. To verify correct symbol offset detection, varying signal delays are introduced in the transmitter by inserting 25 cm increments of RF cable, the delay of one 25cm cable section corresponding to approximately 5 sample periods (1.25ns).

8.5 Experimental Results

The DC offset level and correlation period parameters where varied to determine suitable operating values for stable symbol offset output values. As expected, dependence between the DC offset level and the correlation period was observed. The amplitude of the cross-correlation peak depends on both the DC offset level and the correlation period, therefore to achieve a clear cross-correlation peak the correlation period must be increased as the DC offset level decreases. Lower levels of DC offset are desirable, to minimise any unwanted

interference effects and large correlation periods are acceptable due to the quasi-static nature of the optical channel. Therefore the DC level is minimised as much as possible by increasing the correlation period. It was found possible to utilise a DC offset value as low as only ± 1 quantisation level (0.78% of DAC/ADC 8 bit range) if *M* is set to 5000, this resulted in stable symbol offset values updated every 100μs.

With the aforementioned settings, S_{SUM} and C_{PROF} waveforms were observed for various symbol alignment offsets. Example S_{SUM} and normalised C_{PROF} waveforms are shown in Fig. 8.14 and Fig. 8.15 respectively. S_{SUM} has some reasonably high residual noise content however the general waveform shapes clearly resemble portions of the synchronisation signal as predicted, examples of both rising and falling edges are seen and no edge is present for offset = 0 also as predicted. The normalised C_{PROF} waveforms are well defined, clean, stable profiles with clear peaks indicating the cross-correlation is uninfluenced by the residual noise content in the S_{SUM} waveforms.
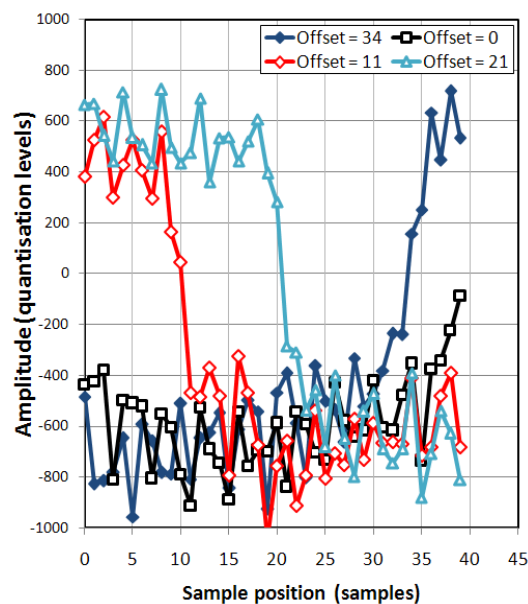
Fig. 8.14 S_{SUM} for various symbol alignment offset values
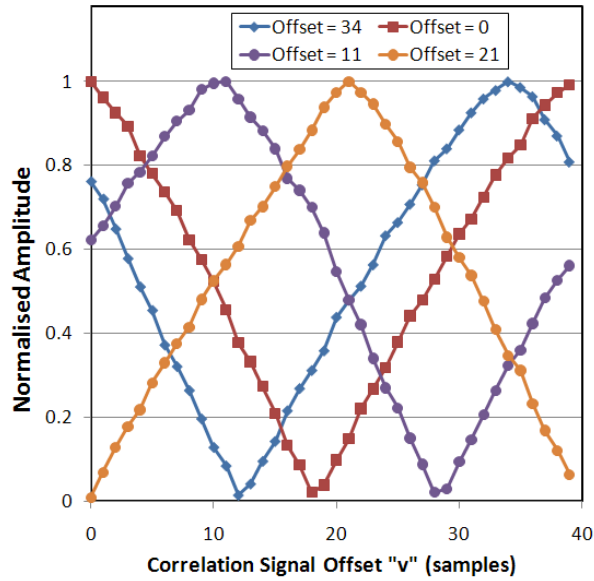
Fig. 8.15 C$_{PROF}$ for Various Symbol Alignment Offset Values

Fig. 8.16 shows the detected symbol alignment offsets for various RF cable lengths, the linear variation indicates the high accuracy of the technique as symbol offset will increase in direct proportion to the additional RF cable length. The RF cable delay is based on manufacturers data so is reasonably accurate, the detected symbol offset is therefore estimated to be $< \pm 1$ sample period. Such deviation in symbol alignment can be tolerated as a sufficiently long cyclic prefix allows an offset in the FFT window location without performance degradation.
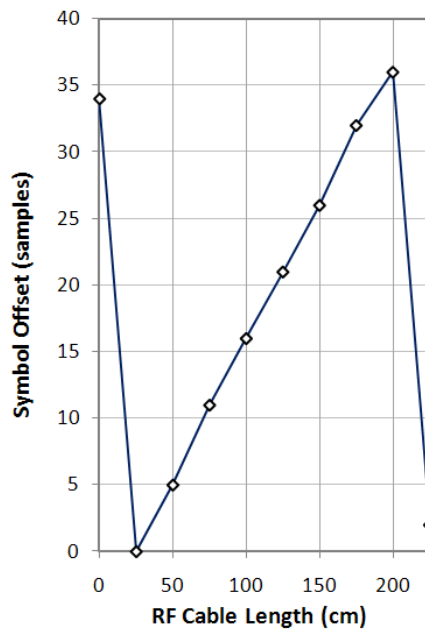
Fig. 8.16 Symbol Alignment Offset for Various RF Cable Delays

Under the aforementioned operating conditions, Fig. 8.17 shows the BER performance curve at 11.25Gb/s for 25km SSMF with DC offset amplitudes of 0 (no S_{ALIGN} signal) and ±1 quantisation levels, the identical results in each case show there is no system performance penalty due to the synchronisation signal.
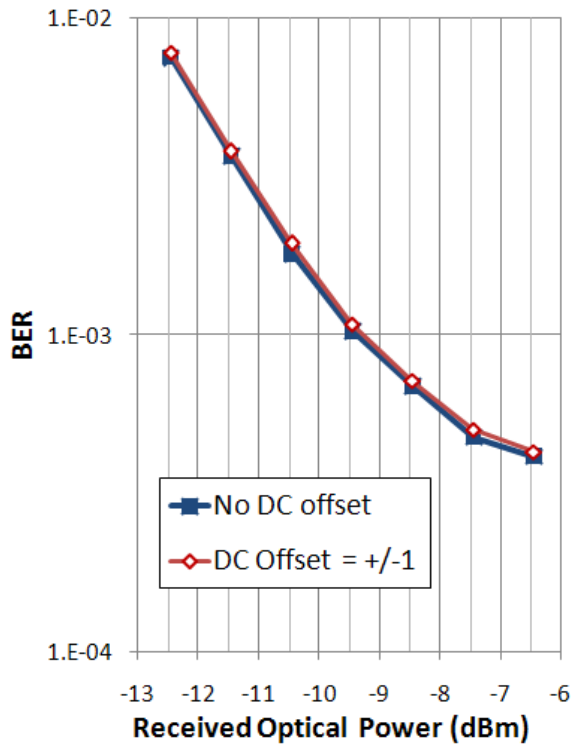
Fig. 8.17 11.25Gb/s BER performance curves for synchronisation signals with DC offset amplitude of 0 and ±1 quantisation level.

8.6 Conclusion

A DSP-based solution has been proposed for symbol synchronisation in point-to-point and point-to-multipoint OOFDM transmission systems. Accurate symbol offset detection has been experimentally verified in a real-time point-to-point IMDD OOFDM link at 11.25Gb/s based on a DML.

The technique offers the critical feature of ONU symbol, time slot and frame synchronisation to an operational network such as point-to-multipoint PONs. A significant characteristic of the technique is the ability to achieve upstream ONU synchronisation where multiple users share the same upstream optical channel. This is the only known

solution which allows ONUs to be installed in an operational PON without disrupting or interrupting exiting network traffic.

The symbol synchronisation technique also offers the advantages of added physical layer network security through suitable encoding of the DC offset sequence with a security key code. Only authorised users with access to the key code can synchronise using the cross-correlation technique.

Furthermore the combination of the symbol synchronisation technique and the synchronous clocking technique can achieve highly synchronised OOFDM-PONs with highly accurate symbol timing which is essential for maximising network performance. Achieving highly synchronised OOFDM-PONs also has the potential to allow overlay with existing TDM-based PONs. This compatibility feature allows network operators to perform progressive upgrade of PONs by gradual migrate of users from existing PON technologies to the more advanced OOFDM technology.

Furthermore, by achieving a low-cost and effective solution for symbol synchronisation no further major technical challenges remain to achieving fully autonomous OOFDM transmission systems.

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9 Conclusions and Future Work

9.1 Conclusions

The global communications network must evolve to meet the changing demands of the digital communication age. Future generations of optical networks must provide; increased data capacity to meet the exponentially growing demand in bandwidth, cost effectiveness to ensure commercial viability, backwards compatibility for gradual network migration, network convergence for simplified infrastructure and reduced operating costs and finally effective bandwidth management for optimal service delivery. Meeting these requirements is the most challenging in access and in-building networks as these networks are currently the main bottlenecks in the global network. Furthermore these networks are also the most cost sensitive and must be the most versatile in terms of flexibility of bandwidth management. As discussed in Chapter 1 it is clear that advanced optical modulation techniques are essential to meet these future network requirements. OOFDM is an advanced multi-carrier modulation format which has the necessary characteristics to meet the aforementioned challenges. OOFDM has therefore undergone ever-increasing research activity in recent years with many theoretical investigations [1,2] and experimental demonstrations [3-8] involving off-line processing.

The research work presented in this thesis explores the feasibility of implementing real-time end-to-end OOFDM data transmission through the design and implementation of OOFDM transceivers using only commercially available components. The transceivers are based on FPGA technology, due to their unparalleled ability for rapid prototyping of high-speed DSP algorithms. By successfully demonstrating that the necessary OOFDM algorithms can be performed with sufficient speed and accuracy in real-time a highly critical step in assessing the technical feasibility of OOFDM is achieved. For the implemented transceivers it has been shown that modern semiconductor electronics are not the limiting factor in terms of achievable system capacity and that DAC and ADC bandwidth are the main factors limiting the system capacity. It is worth noting that due to

recent advances in DAC and ADC technology, devices are now commercially available with bandwidths exceeding 10GHz [9,10] potentially enabling the development of higher capacity OOFDM transceivers. The design and implementation of the OOFDM transceiver electronics is presented in detail in Chapter 3. The high level system design in terms of the discreet system elements is presented in conjunction with detailed descriptions of the DSP architecture and functional blocks. System modelling using MatLab™ and Simulink™ provided a highly effective design approach to allow exploration and verification of DSP designs before porting to the FPGAs.

The developed OOFDM transceivers successfully achieved the first and still the only experimental demonstration of a series of real-time end-to-end OOFDM data transmissions in simple IMDD transmission systems based on DMLs. Chapter 4 describes the first experimental demonstrations of real-time end-to-end OOFDM data transmission at net bit rates of 1.5Gb/s and 3Gb/s over 500m of OM1 MMF. The 3Gb/s transceiver design employed a doubling of the system clock speed and sample rate and also incorporated limited clipping level optimisation through live selection of preset levels. Transmission performance over 500m OM1 MMFs has been explored in order to demonstrate that OOFDM can be highly cost-effective through utilisation of the vast infrastructure of legacy MMF fibers installed worldwide [11]. By employing DQPSK on all subcarriers and equal subcarrier powers the 3Gb/s, 500m MMF system achieved a BER as low as 3.3×10^{-9}. This performance clearly showed that OOFDM is capable of multi-Gb/s data transmission in legacy MMF and the high performance indicates the potential for increased data rates.

Further development of the real-time OOFDM transceivers has been investigated in Chapter 5 to explore the feasibility of operation at higher bit rates. Increased bit rate was achieved through the increased spectral efficiency associated with employing higher modulation formats. By employing 16-QAM encoding/decoding on all subcarriers the system line rate was increased to 7.5Gb/s. To allow 16-QAM modulation the transceiver modifications included the essential features of channel estimation and equalisation in combination with a simple 3-level variable power loading scheme to compensate for the system frequency roll-off effect. The 3-level variable power loading scheme employing preset subcarrier power levels is shown to be sufficient to achieve a minimum BER of 3.4×10^{-4} after transmission through 300m of OM1 MMF. The 7.5Gb/s transmitter design also incorporated enhanced live clipping level control with unlimited adjustment. Also

enhanced receiver features were incorporated for monitoring BER distribution across individual subcarriers and capturing of the system frequency response from IFFT input in the transmitter to the FFT output in the receiver. The enhanced parameter adjustment and monitoring features enabled a great improvement in the live optimisation of the OOFDM system performance. The performance of the 16-QAM-based system is more sensitive to the subcarrier SNRs [12] which is evident from the increased minimum BER.

A further increase in system bit rate has also been explored in Chapter 5. A line rate of 11.25Gb/s has been demonstrated though the use of 64-QAM on all subcarriers to achieve a high electrical spectral efficiency of 5.625b/s/Hz with the fixed bandwidth of the 4GS/s DAC and ADC. An improved adaptive power loading scheme has been implemented which provides both increased control and on-line adjustment of individual subcarrier power levels. The enhanced control of subcarrier power loading profile is highly effective at compensating the system frequency roll-off effect, to which the 64-QAM modulated OOFDM signals are more sensitive. By utilising all the incorporated on-line parameter adjustment and monitoring functions the rapid optimisation of system BER performance was again possible. The combination of on-line, fine adjustment of subcarrier powers and the BER distribution monitoring feature allowed the subcarrier transmit power loading profiles to be highly optimised. This enhanced adaptive power loading scheme achieved a virtually uniform distribution of errors across all subcarriers whilst minimising the total system BER to an acceptable level. The 11.25Gb/s OOFDM transceiver has demonstrated real-time end-to-end data transmission over simple IMDD links based on both 25km of SSMF and 500m of OM2 MMF with minimum BERs of 8.5×10^{-4} and 4.5×10^{-4} respectively. These results are highly important as they give a clear indication that OOFDM has potential for application in cost-sensitive access and in-building networks.

The physical mechanisms limiting the minimum BER observed at 11.25Gb/s for transmission over 25km of SMF are believed to be; i) the low signal extinction ratio associated with modulating DMLs with high PAPR OFDM signals, ii) the intensity modulation-induced frequency chirp effect associated with the DML and iii) the subcarrier intermixing effect associated with square-law direct detection in the receiver [13,14]. This is strongly supported by theoretical investigations reported in [15] where a comprehensive theoretical OOFDM system model is compared with the real-time OOFDM system. The aforementioned effects are identified as the dominant BER limiting factors.

Chapter 6 explores the use of alternative intensity modulators in the real-time OOFDM transmitter. Colourless ONUs are critical for realising practical, low-cost and manageable WDM-OOFDM PONs through drastically simplifying ONU manufacturing logistics and reducing network implementation and management complexity. RSOAs offer the advantages of simultaneous signal modulation and optical amplification, low component cost, compactness, low power dissipation, full coverage of the entire fiber transmission window and large-scale monolithic integration capability. Therefore the implementation and performance of a colourless OOFDM transmitter based on a 1GHz RSOA as an intensity modulator in combination with a tuneable laser source has been explored. The colourless transmitter successfully demonstrated operation over the entire C-band at 7.5Gb/s line rate over a simple IMDD link of 25km SSMF. A large 22dB system frequency response roll-off was observed due to the RSOA's low modulation bandwidth and dynamic frequency chirp effect. This large roll-off was effectively compensated by exploiting the transceivers adaptive power loading leading to the minimum BER of $<9\times10^{-5}$ for all wavelengths tested over the C-band. This result clearly shows that RSOA-based colourless OOFDM transceivers are technically feasible.

VCSELs are low-cost lasers with additional advantages of high reliability, long lifetime and easy testing and packaging. Due to their ability for direct-modulation they are highly attractive for application in OOFDM transmitters to achieve a significant cost saving compared to the typically employed DFB laser. Chapter 6 therefore investigates the performance of an 11.25Gb/s VCSEL-based real-time OOFDM transceiver in simple IMDD links based on 25km SSMF. It is shown that through the use of adaptive power loading and live optimisation of VCSEL operating conditions the VCSEL-based real-time OOFDM transceivers can achieve minimum BERs of 1.2×10^{-3} which is below typical FEC limits. This result is extremely important as it demonstrates that the DML, which is a key OOFDM transceiver component, can be implemented with an extremely low cost device contributing to the essential target of achieving low-cost OOFDM transceivers required by access and in-building network applications.

To enable the deployment of practical OOFDM transmission systems it is essential that an independent receiver clocking solution is implemented. In Chapter 7 a low-cost, low-

complexity, DSP-fee and robust synchronous clocking technique is proposed and experimentally demonstrated in the real-time end-to-end IMDD OOFDM system at 11.25Gb/s over 25km SSMF using a DML. The technique employs a dedicated clock signal, located outside the OOFDM frequency band, transmitted simultaneously with the OOFDM signal. The OOFDM receiver employs simple filtering to separate the clock from the OOFDM signal before clock regeneration with a traditional PLL-based clock recovery circuit. The clock and OOFDM signal peak-to-peak levels driving the DML where optimised to demonstrate that no BER performance or optical power budget penalty is caused by the addition of the clock signal. As the synchronously clocked receiver's clocks are locked to the transmitter clocks the STO and SCO effects become negligible. It was also demonstrated that the synchronous clocking technique achieves improved BER stability compared to the case where a common reference is used to directly clock the transmitter and receiver. In OOFDMA PON networks highly synchronised ONUs are essential for achieving network operation, the proposed synchronous clocking solution is therefore of great importance as it potentially offers a simple and highly effective solution for network synchronisation of OOFDMA PONs.

The last major technical challenge to achieving a fully autonomous synchronised OOFDM system is automated symbol alignment. Also as PONs are a principal application of OOFDM, a symbol synchronisation method suitable for point-to-multipoint PON applications in addition to point-to-point systems is an essential requirement to make OOFDM-based PONs a practical reality. Chapter 8 proposes and experimentally demonstrates a DSP-based symbol alignment technique based on the transmission of a low power DC offset signal and a cross-correlation function in the receiver. The technique has been experimentally verified at 11.25Gb/s real-time point-to-point 25km SSMF IMDD link employing a DML. The technique offers the critical feature of ONU symbol, time slot and frame synchronisation in an operational PON without the need to interrupt the existing network traffic. The symbol synchronisation technique also offers the added advantage of physical layer network security through suitable encoding of the DC offset sequence with a security key code. Furthermore the combination of the symbol synchronisation technique and the synchronous clocking technique can achieve highly synchronised PONs, this has the potential for the coexistence of timeslot-based OOFDM PONs with existing TDM-based PONs. This compatibility feature allows network operators to perform progressive

PON upgrade by gradual migrate of users from existing PON technologies to the more advanced OOFDM technology.

By successfully achieving the real-time demonstration of end-to-end OOFDM data transmission in both MMFs and SMFs, and by addressing all key technical challenges, it can be concluded that OOFDM is a technically feasible optical transmission technology with great potential for application in both future access and in-building networks.

As a final conclusion an opinion is tendered on the fundamental limits for real-time OOFDM signal generation and detection based on current technology trends. The data rate of an OOFDM transceiver is the product of two fundamental parameters, namely signal bandwidth and spectral efficiency. The sample rate of DACs and ADCs is considered to be the key limiting factor for signal bandwidth. Based on current DAC/ADC technology trends, 100GS/s devices are considered realistic in the near future giving signal bandwidths of ~50GHz. DSP technology is not expected to be a major limiting factor as highly parallel architectures exploit increasing chip area to limit logic clock speeds. Power consumption, however, may be an issue for large DSP designs. Considering spectral efficiency, it has been experimentally demonstrated that real-time OOFDM can achieve values in the region of 5b/s/Hz in simple IMDD systems without employing polarisation division multiplexing. It is believed that in IMDD systems spectral efficiency is mainly limited by signal distortions induced by analogue (electrical and optical) component nonlinearities. The increased requirements on system synchronisation associated with higher sample rates can also result in performance limitations. Based on signal bandwidths of the order of 50GHz, spectral efficiencies of 5b/s/Hz and limitations associated with operating at higher clock speeds, it is believed that single channel OOFDM transceivers could potentially support the real-time generation and detection of OOFDM signals at data rates in excess of 200Gb/s.

9.2 Future Work

The work performed in this thesis has shown OOFDM to be a strong candidate for future generations of optical access and in-building networks. However further research is essential to fully explore OOFDM's ability to meet all the identified network requirements.

The future research areas identified below are considered as critical for fully validating OOFDM as an enabling technology for future optical networks. Future research activities have been identified based on short term activities employing the implemented real-time transceiver and long term activities requiring the development of new OOFDM transceivers:

Short Term Research Activities:

1) Further analysis of the symbol alignment technique presented in Chapter 8 is required to fully verify the system performance at 11.25Gb/s over 25km SSMF when symbol offset is automatically updated based on the detected symbol offset. Asynchronous clocking can be explored through implementing automatic symbol alignment.

2) The symbol alignment technique should also be demonstrated with encoded DC offset sequences to show that the technique can implement physical layer security and timeslot and frame detection functions.

3) A simple upstream OOFDMA PON consisting of at least two OOFDM transmitters, (representing the ONUs) and one OOFDM receiver (representing the OLT) is to be implemented with symbol offset adjustment implemented in the transmitters. Symbol synchronisation of both transmitters will verify the important feature of ONU symbol synchronisation in an operational PON without disturbing existing network traffic.

Long Term Research Activities:

1) Experimental Demonstration of Real-Time OOFDM Transceivers with Increased Capacity.

To meet future network demands OOFDM transceivers should be capable of delivering 40Gb/s and beyond. To increase transceiver capacity there are a number of approaches that can be adopted these include:

- Exploiting the advances in DAC and ADC technology to implement transceivers with increased sample rates and therefore increased signal bandwidth. Converters are now available with sample rates well in excess of 10GS/s making 40Gb/s real-time OOFDM transceivers a realistic target.

- Dual-band OOFDM [16] can increase total system capacity without the need for higher bandwidth DAC/ADCs. By employing electrical upconversion with an RF carrier two independent electrical OFDM signal bands can be generated for modulation onto the same optical carrier for transmission over the same IMDD link. The OOFDM receiver can then decodes data from a single OOFDM band.

- Polarisation multiplexed OOFDM (POLMUX-OOFDM) [17] modulates an OOFDM signal onto each polarisation of the optical carrier to achieve a doubling of spectral efficiency. This approach can be employed with direct-detect in the receiver however this requires post-detection DSP algorithms to compensate for the cross-polarization interference effect [17].

2) Reduced Cost OOFDM Transceivers

As a principle application for OOFDM transceivers is in the cost-sensitive access and in-building networks further research is required to determine suitable means of increasing the OOFDM transceiver cost–effectiveness. The two main approaches that can be explored are i) use of low cost electrical and optical components in combination with DSP techniques to compensate the lower performance associated with lower cost components and ii) reducing the complexity of the transceiver's DSP through algorithm design optimisation and logic circuit optimisation, this leads to lower logic utilisation resulting in reduced production costs.

3) Techniques for Increased Optical Power Budget

For future PON networks optical power budgets up to a maximum of 30dB are required [18]. As the demonstrated real-time system has an optical power budget in the region of 15dB this must be improved significantly in order to meet future network requirements. This is a key area where research is vital to explore and identify practical and cost-effective techniques for increasing the sensitivity of OOFDM receivers necessary for the higher optical power budgets. OOFDM has the property that line rate to be traded off against system performance meaning reducing the operating bit rate will increase the optical power budget. Therefore increasing signal bandwidth through higher sample rate DAC/ADCs can also be used to achieve a balance between improvement in system line rate and optical power budget. Some promising techniques have been theoretically explored, for example investigations have shown that an optical bandpass filter with

wavelength offset relative to the optical carrier placed after the DML can increase optical power budget by as much as 7dB [15], this technique therefore merits experimental verification.

4) Demonstration of OOFDM-based PONs

As OOFDM is considered as a potential technology for future generation PONs it is essential that experimental research is performed with PONs constructed from OLTs and ONUs employing real-time OOFDM transceivers. This research is essential, particularly in PONs based on power splitting, to explore ONU interaction and interference in relation to the impact on network performance. Experimentation with OOFDM-based PONs is essential to answer questions such as how many ONUs a PON can support and what factors influence the number of ONUs that can be supported. There are also many challenges that need to be solved in order to achieve low cost, practical and robust OOFDM-based PONs, such challenges to be addressed include the problem of optical beat interference (OBI) between ONU lasers in power-splitting-based PONs, and exploration and comparison of various techniques for implementing colourless ONUs for application in WDM-OOFDM PONs. A further area to be investigated is the implementation of hybrid TDM-OOFDM PONs to demonstrate backwards compatibility with existing TDM-based PONs.

5) Integration of OOFDM Transceivers into a Communication System Platform for Customer Service Trials

To fully validate OOFDM as a physical layer technology it must be fully integrated into a system to allow system testing at all layers up to the application level. In particular this requires the media access control (MAC) layer control functions to be developed for interfacing to the OOFDM physical layer. This will enable field trials of real customer services over OOFDM-based networks which is an essential step before any new technology can be adopted in the real-world.

As a final note, largely due to the success of this work on real-time OOFDM transceivers, Bangor University is coordinating a PIANO+ funded project known as OCEAN (OOFDM for Cost Effective Access Networks) involving both partners from industry and research institutes. The project attempts to address, at different levels, all the research areas identified above with the aim of developing and trialling product like OOFDM transceivers

with improved performance and features. Furthermore the project aims to perform a comprehensive techno-economic analysis of OOFDM technology and, through bodies such as FSAN, aims to drive inputs to facilitate the development of global PON standards.

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Appendix

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A.2 Publications

A.2.1 Publications in Journals

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Real-time implementation of optical OFDM transmitters and receivers for practical end-to-end optical transmission systems

R.P. Giddings, X.Q. Jin, H.H. Kee, X.L. Yang and J.M. Tang

Real-time optical OFDM transceivers are successfully demonstrated for the first time, which support 1.5 Gbit/s transmission over 500 m 62.5/125 μm multimode fibres in an intensity-modulation and direct-detection system involving a directly modulated DFB laser. The implemented transceivers only use standard commercially available components.

Introduction: The concept of optical orthogonal frequency division multiplexing (OOFDM) was first proposed in 2005 [1]; soon afterwards, opportunities of employing OOFDM signals converted by directly modulated DFB lasers (DMLs) were theoretically explored over multimode fibre (MMF)-based LANs [2] and singlemode fibre (SMF)-based MANs [3]. Since then, extensive investigations of OOFDM transceivers of various configurations have been reported in long-haul [4, 5], MANs [6] and LANs [7]. However, all experimental works published so far have been undertaken using non-real-time signal processing approaches, which do not consider the limitations imposed by the precision and speed of practical digital signal processing (DSP) hardware. The experimental demonstration of real-time OOFDM transceivers is critical for not only rigorously validating the OOFDM technique but also establishing a solid platform for evaluating its feasibility for practical implementation. In an optical back-to-back system, a real-time coherent OOFDM receiver has been reported recently [4], which is, however, not able to perform real-time data transmission owing to the absence of a corresponding real-time transmitter.

In this Letter, a real-time OOFDM transmitter and receiver based on standard commercially available components including FPGAs and ADCs/DACs are demonstrated experimentally for the first time. Transmission performance is investigated over a DML-based intensity-modulation and direct-detection (IMDD) MMF system. Results suggest that OOFDM has great potential for providing a viable solution for practical implementation in high capacity optical networks of various architectures.
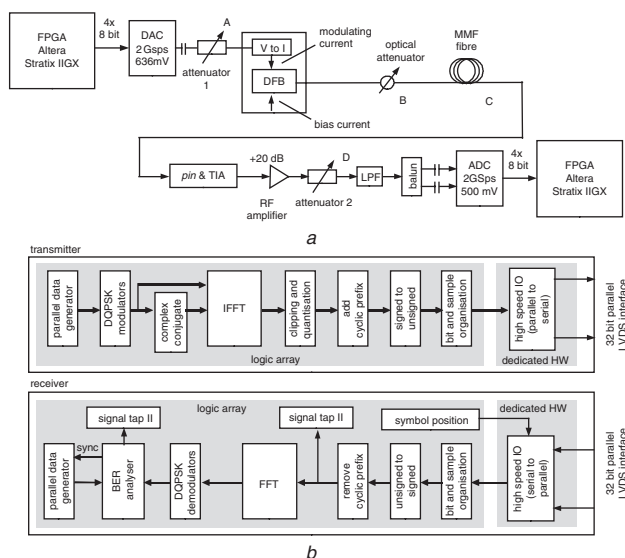

Fig. 1 *Experimental transmission system, and real-time OOFDM transceiver architectures*

a Experimental transmission system
b Real-time OOFDM transceiver architectures

Real-time OOFDM transceivers and experimental setup: Fig. 1a shows the real-time experimental system configuration. The transmitter consists of an Altera Stratix II GX FPGA, which performs the real-time DSP on the data source and outputs four 8-bit samples in parallel at a rate of 500 MHz. These samples are fed to an 8-bit DAC running at 2GS/s. The analogue electrical signal having a 1 GHz bandwidth is attenuated by a variable attenuator to adjust the modulating current injected into a

1550 nm DML having a 10 GHz modulation bandwidth. The OOFDM signal from the DML is coupled into a 500 m 62.5/125 μm MMF link having a 3 dB optical bandwidth of 1200 MHzkm. At the receiver, a 12 GHz *pin* with a TIA converts the transmitted optical signal to the electrical domain. The electrical signal is amplified by a 2.5 GHz, 20 dB RF amplifier and attenuated as needed to adjust the signal amplitude. The lowpass filtered, single ended electrical signal is converted via a balun to a differential signal to feed an 8-bit ADC operating at 2GS/s, whose digital interface format is identical to the DAC input in the transmitter. Finally, the digital samples are fed to a second Altera Stratix II GX FPGA, which performs the real-time DSP on the received symbols and determines the BER. Clock synthesisers based on a common reference clock are used to generate the system clocks for the transmitter and the receiver.

Fig. 1b shows the transmitter (top) and receiver (bottom) architectures implemented in the DSP hardware. The digital logic is entirely implemented with self-designed logic blocks. The real-time IFFT/FFT logic function is a 32 point, decimation in time, pipelined architecture, the key parameters of which can be fully adjusted and optimised to minimise the finite computational error inherent in physical DSP hardware.

In the transmitter, except for the digital back-to-back case, DQPSK is considered as this does not require pilot tones to perform channel estimation. 32 subcarriers are used, of which 15 carry data. A 30-bit parallel data sequence feeds 15 DQPSK modulators which generate the complex data for the data-carrying subcarriers. To achieve a real-valued IFFT output, the data-carrying subcarriers are arranged to satisfy the Hermitian symmetry with respect to their complex conjugate counterparts [2]. The signed, 32 real-valued IFFT outputs are clipped at a clipping ratio of 11.6 dB and quantised to 8 bits. A cyclic prefix of eight samples is added to each symbol, producing 40 samples per symbol. The DAC sampling rate of 2 GHz gives a symbol rate of 50 MHz. The signed samples are converted to unsigned values as the DAC requires positive values only. Sample reordering and bit arrangement are then performed to present the symbol data to the 32 high-speed, 10:1, serialisers in the required order and to ensure that the serialisers feed the four sample interface to the DAC in the correct sequence. In the receiver, an inverse DSP procedure, compared to that described above, is used to recover the received data, as shown in Fig. 1b.
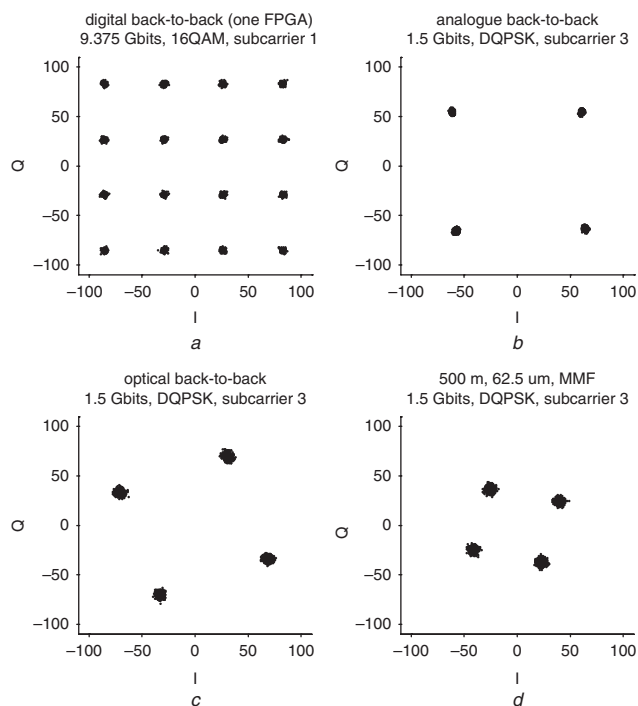

Fig. 2 *Constellations of received OOFDM signals for different system configurations*

To achieve symbol alignment, a test symbol of a fixed pattern is sent repeatedly by the transmitter, the received test symbol is detected and analysed using the Signal Tap II, embedded logic analyser and the Altera Quartus II software; the measured sample offset is compensated

for by adding an appropriate time delay. As shown in Fig. 1b, a BER analyser block continuously detects and counts errors occurring within one million symbols. The error count is viewed via the Signal Tap II embedded analyser and an average BER is obtained over a large number of readings.

Results: To evaluate the developed real-time DSP function only, investigations were first undertaken of the performance of the digital back-to-back transmitter and receiver implemented within a single FPGA without involving the DAC/ADC. Based on a symbol rate of 156.25 MHz (less than half of the maximum FPGA clock speed), 9.375 Gbit/s at a BER of zero was achieved using 16QAM on all the data-carrying subcarriers. Fig. 2a shows a clear constellation of subcarrier 1. This confirms the capability of the developed DSP function for supporting high-speed OOFDM data transmission.

By including the DAC/ADC, experimental measurements are also conducted in an analogue back-to-back transmitter and receiver configuration, in which points A and D, as shown in Fig. 1a, are directly connected with attenuator 1 being set to 3 dB. With the sampling rate of 2GS/s and DQPSK, 1.5 Gbit/s transmission is achieved at a BER of zero with a constellation of subcarrier 3 being shown in Fig. 2b. Further experimental measurements are also performed in an optical back-to-back configuration, in which points B and C, as shown in Fig. 1a, are connected. For such a case, attenuator 1, the optical attenuator and the receiver's electrical gain are taken to be 5, $\leq$6 and 3 dB, respectively, also a DFB bias current of 38 mA is adopted. As shown in Fig. 3, for optical launch powers of > -12 dBm, 1.5 Gbit/s transmission at a BER of $<<1.0 \times 10^{-9}$ is obtainable with the constellation of subcarrier 3 being shown in Fig. 2c.
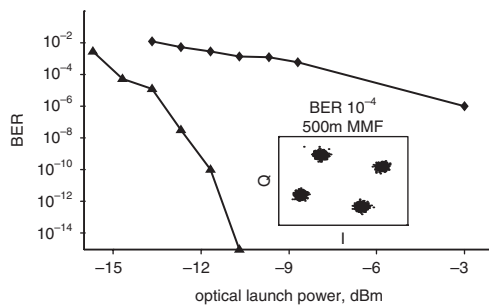

Fig. 3 *Measured BER performance for 1.5 Gbit/s transmission over 500 m MMF link*

—▲—optical back-to-back
—◆—500 m MMF link

Finally, experimental measurements are undertaken of 1.5 Gbit/s transmission over a 500 m MMF IMDD link illustrated in Fig. 1a.

The measured BER against optical launch power is plotted in Fig. 3. For an optical launch power of -3 dBm, a BER of $<1.0 \times 10^{-6}$ is observed with a constellation of subcarrier 3 being shown in Fig. 2d (a corresponding constellation for a BER of 1.0×10^{-4} is included in Fig. 3). A power penalty of 5.8 dB at a BER of 1.0×10^{-3} is observed in Fig. 3. In addition, the OOFDM transmission performance is insensitive to different launch conditions.

Conclusion: The first real-time OOFDM transceivers have been demonstrated successfully for 1.5 Gbit/s transmission over a 500 m IMDD MMF system. The transceivers are potentially capable of supporting much higher data rates, when use is made of higher modulation formats and faster DAC/ADC sampling rates.

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Experimental demonstration of real-time 3Gb/s optical OFDM transceivers

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Abstract: Real-time optical orthogonal frequency-division multiplexing (OOFDM) transceivers based on off-the-shelf components including FPGAs are experimentally demonstrated, for the first time, incorporating key functionalities such as live transceiver optimisation and advanced channel estimation, and also utilising self-developed IFFT/FFT logic algorithms verified at 10Gb/s. The fastest ever real-time end-to-end transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m multi-mode fibers is achieved with BERs of $<3.3 \times 10^{-9}$ in intensity-modulation and direct-detection systems employing directly modulated DFB lasers. Excellent performance robustness is also observed to various offset launch conditions. This work is a significant breakthrough in demonstrating the great potential of OOFDM for practical implementation in optical networks.

OCIS codes: (060.0060) Fiber optics and optical communications; (060.4080) Modulation; (060.3510) Laser, fiber.

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1. Introduction

Optical orthogonal frequency division multiplexing (OOFDM) [1] has already demonstrated a number of unique and inherent advantages including, for example, great resistance to dispersion impairments, efficient utilization of channel spectral characteristics, potential cost-effectiveness due to full use of mature digital signal processing (DSP), dynamic provision of hybrid bandwidth allocation in both the frequency and time domains, and significant reduction in optical network complexity. As a direct result of the aforementioned features, OOFDM has gained overwhelming research and development interest and, more importantly, is regarded as one of the strongest contenders for enabling the next generation high capacity optical networks required to meet the exponentially growing demand for broadband transmission. Over the past several years, world-wide extensive experimental investigations of the transmission performance of OOFDM of various variants have been reported for all the optical network scenarios including long-haul systems [2,3], metropolitan area networks [4,5] and local area networks [6,7].

However, all the experimental works published previously [1–7] are based on transmission of OOFDM signals originating from arbitrary waveform generators (AWGs) utilising off-line signal processing-generated waveforms. At the receiver, the received OOFDM signals are captured by digital storage oscilloscopes (DSO) and processed off-line to recover the received data. These off-line signal processing approaches do not consider the limitations imposed by the precision and speed of practical DSP hardware required for realizing real-time transmission. Therefore, the experimental demonstration of real-time OOFDM transceivers is critical for not only rigorously validating the OOFDM technique but also establishing a solid platform for evaluating the feasibility of the technique for practical implementation in optical networks.

To implement real-time OOFDM transceivers, highly complex, computationally intense and high-speed signal processing algorithms must be performed in real-time. Although OFDM has already been adopted widely in wireless and wired transmission systems, these systems currently, however, operate at signal bit rates of the order of several tens of Mb/s [8], which are approximately 1000 times lower than those targeted by OOFDM. Thus it is apparent that the real-time signal processing power of an OOFDM system needs to be in the region of three orders of magnitude higher, compared to the existing OFDM-based systems.

The achievement of real-time end-to-end OOFDM transceivers based on real-time DSP with sufficiently high speed and precision is a significant breakthrough in demonstrating the great potential of the OOFDM technique for practical implementation in high capacity optical networks of various architectures. In April 2009, we have reported the world-first implementation of real-time OOFDM transceivers, which support end-to-end transmission of a 1.5Gb/s differential quadrature phase shift keying (DQPSK)-encoded signal over a 500m multi-mode fibre (MMF)-based, intensity-modulation and direct-detection (IMDD) system incorporating a directly modulated DFB laser (DML) [9]. One month later, the real-time OOFDM transmission capacity was doubled, and a transmission of 3Gb/s DQPSK-encoded OOFDM signal over a 500m MMF in the abovementioned transmission system has been successfully demonstrated experimentally [10]. In addition, a real-time OOFDM transceiver incorporating an advanced channel estimation technique proposed by our research group has

also been implemented, which enables the successful demonstration of 3Gb/s 16-quadrature amplitude modulation (QAM)-encoded real-time OOFDM transmission, in one case, over 75km MetroCor single-mode fibres (SMFs) with negative power penalty in a DML-based IMDD system without in-line optical amplification and chromatic dispersion compensation [10]. Here it is worth addressing that a real-time coherent optical receiver has recently been reported [11], which is, however, not capable of performing end-to-end real-time transmission, as off-line signal processing is still applied in the corresponding transmitter.

In this paper, we report in detail, for the first time, a considerably improved real-time OOFDM transceiver design incorporating a number of newly developed functionalities compared to those reported in [9,10]. Based on the improved transceivers, the fastest ever real-time transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m MMFs with bit error rates (BERs) of $<3.3\text{x}10^{-9}$ has been achieved in DML-based IMDD systems. Excellent performance robustness is also observed to various offset launch conditions. Moreover, transmission performance comparisons are also made between DQPSK- and 16-QAM- encoded 3Gb/s OOFDM signals in the abovementioned transmission systems.

2. Real-time DSP for IFFT/FFT algorithms

2.1 IFFT/FFT algorithms for real-time OOFDM transceivers

OFDM is a multi-carrier modulation technique where a single high-speed data stream is divided into a number of low-speed data streams, which are then separately modulated onto harmonically related, parallel subcarriers. The subcarriers are considered to be orthogonal as their overlapping spectra have the property that they do not interfere at the discrete subcarrier frequencies, thus resulting in high spectral efficiency. At the transmitter, the frequency domain subcarriers must be transformed into a time domain symbol, and at the receiver the time domain symbol must be transformed into the frequency domain subcarriers. As the subcarriers are positioned at equally spaced frequencies, widely used transforms such as the inverse discrete Fourier transform (IDFT) and discrete Fourier transform (DFT) can be adopted. For practical implementation, these transforms are replaced with the more efficient Fast Fourier transform (FFT) and inverse FFT (IFFT) as the computational complexity is significantly reduced. However, for any OFDM-based system, the IFFT and FFT transforms are still the most computationally intense functions, therefore, the real-time implementation of the FFT/FFT algorithms poses one of the greatest challenges for achieving real-time system implementation.

Here, we utilise off-the-shelf field-programmable gate arrays (FPGAs) for real-time hardware-based DSP. We have developed our own custom implementation of a 32 point IFFT/FFT logic function employing a radix-2 decimation-in-time structure comprising of 2-point butterfly elements as the core computational building blocks. To achieve high-speed performance, the IFFT/FFT logic function design is based on a highly pipelined architecture using a number of extensively paralleled processing stages. The custom design permits full control and optimisation of the logic function parameters. The computational precision at each stage of the IFFT/FFT can be controlled to allow the overall calculation precision to be maximised whilst maintaining acceptable logic resource utilisation. In addition, the design can also be scaled to support longer transform lengths required for an increased number of subcarriers, and adapted for higher clock speeds for increased symbol rates. Moreover, the developed IFFT/FFT function also includes adjustable clipping and quantisation of the output samples.

It should be noted that, the developed IFFT/FFT logic function is applicable for all OOFDM application scenarios. Here such a design is applied to an IMDD transmission system of interest in this paper.

2.2 Evaluation of implemented real-time IFFT/FFT logic functions at 10Gb/s

To evaluate the performance of the developed IFFT/FFT logic designs alone, at 10Gb/s, both the IFFT and FFT functions are implemented in the same FPGA in a back-to-back configuration, as shown in Fig. 1(a). 10Gb/s incoming data is generated externally from a pattern generator. This single data stream is demultiplexed into four 2.5Gb/s streams for input to the FPGA via four high-speed deserialising transceivers. The parallel data from the transceivers is combined and fed to 15 parallel 16-QAM encoders to generate complex data for input to the IFFT logic function. The 15 encoded complex numbers fill the positive frequency bins, and subcarrier 0 corresponding to zero frequency in the electrical domain must be set to zero. For these 16 subcarriers, their 16 complex conjugate counterparts are generated and positioned in the negative frequency bins in such a way that Hermitian symmetry is satisfied between them. This results in the generation of 32 real-valued time domain samples at the output of the IFFT to be compatible with the generation of real-valued signals required in IMDD systems, as discussed in Section 3.
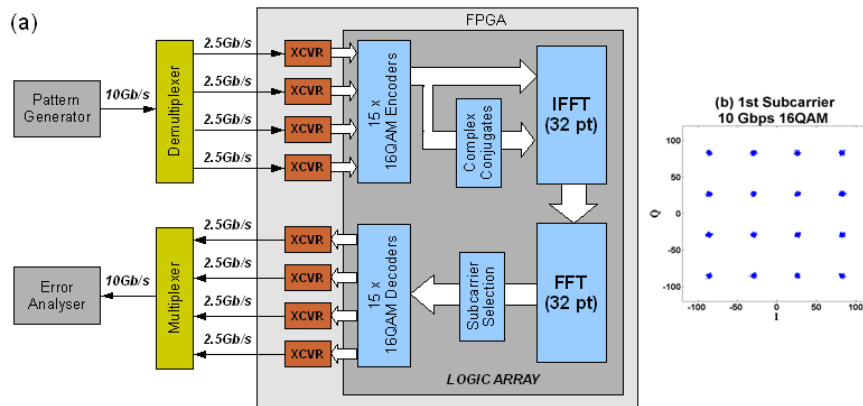
Fig. 1. (a) Experimental system for evaluating IFFT/FFT logic functions; (b) constellation of 16-QAM-encoded first subcarrier after FFT.

These 32 samples from the IFFT function forming an OFDM symbol are clipped and quantised to 8-bits, and are fed directly to the input of the FFT function. From the output of the FFT, the 15 data-carrying subcarriers in the positive frequency bins are selected, which are then decoded by 15 parallel 16-QAM decoders. The resulting parallel data is fed to four high-speed serialising transceivers. The four data streams at 2.5Gb/s are multiplexed to a single 10Gb/s data stream and BER is measured with an error analyser. The FPGA runs at a clock speed of 156.26MHz, which is equal to the symbol rate, as discussed in Section 3.1. The clocks for all the system elements are generated with clock synthesisers using a common reference source.

Zero bit errors are detected by the error analyser at 10Gb/s operation. The constellation of the first subcarrier at the FFT output is shown in Fig. 1(b) and is typical of all subcarriers. This clearly shows that the real-time DSP is capable of supporting at least 10Gb/s OOFDM transmission. It is also estimated that, the use of higher modulation formats, higher clock speeds and more subcarriers can allow the developed IFFT/FFT algorithms to operate at approximately 40Gb/s.

3. Real-time OOFDM transceiver architecture and experimental system

3.1 Real-time transceiver architecture

Figure 2 shows the detailed architectures of the real-time transmitter (top) and the real-time receiver (bottom) developed. The transceiver design has a fully pipelined architecture so that data flow is continuous with very limited buffering of OOFDM symbols. For each OOFDM symbol all samples are processed in parallel.
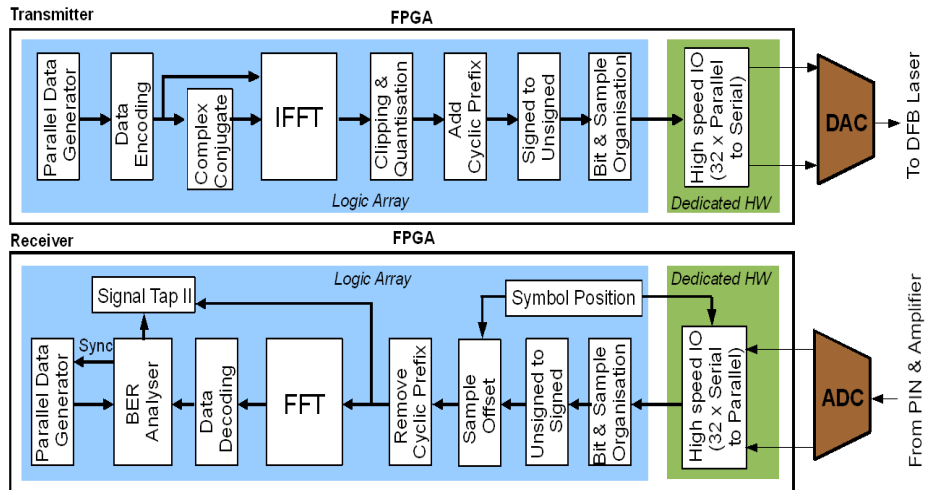
Fig. 2. Real-time OOFDM transceiver architecture.

In the transmitter, a 32 point IFFT is used to support 32 subcarriers, of which 15 carry encoded real data. A parallel pseudo random data source feeds 15 encoders, each of which encodes the data using a specific signal modulation format producing a complex number representing one of the 15 data-carrying subcarriers in the frequency domain. Use is made of these 15 subcarriers to generate 32 real-valued time domain samples, according to the method described in Section 2.2.

After the IFFT, the 32 signed, real-valued samples are clipped and quantized. The number of quantization bits is set to 8, which matches the resolution of the employed DAC. Whilst the clipping ratio can be adjusted, during operation, from a number of preset levels to optimize the transceiver performance. To mitigate the inter-symbol interference (ISI) effect caused by modal dispersion, a cyclic prefix of 8 samples is added to each symbol, giving rise to 40 samples per symbol. The internal system clock is set to be 100MHz, and the parallel processing approach results in a 100MHz symbol rate. The 100MHz symbol rate and 40 samples per symbol give a sample rate of 4GS/s. The relationship between the symbol rate, S, and the signal line rate, R, can be expressed as

$$S = \frac{R}{bN} \qquad (1)$$

where b is the number of binary bits encoded on each subcarrier within a symbol, and N is the total number of data-bearing subcarriers in the positive frequency bins. The signed samples are converted to unsigned values by adding an appropriate DC offset, as the DAC requires positive values only. After performing sample ordering and bit arrangement, the unsigned 40 samples are streamed to the DAC interface at 4GS/s. An entire symbol consisting of 320 bits is fed in parallel to 32 high speed 10:1 dedicated hardware serialisers, the interface thus consists of 4 samples transferred in parallel at a rate of 1GHz, giving the required aggregated sample rate of 4GS/s. The DAC generates an analogue electrical OOFDM signal having a maximum peak-to-peak voltage of 636mV. Finally, this signal is used to directly modulate the DML.

At the receiver, after performing optical-to-electrical conversion using a PIN, the analogue electrical signal is digitised by a 8-bit ADC operating at 4GS/s. A digital interface, which is identical to that of the DAC in the transmitter, transfers the digital samples at 4GS/s to the second FPGA. The 32 high speed, 1:10, dedicated hardware deserialisers capture 40 received samples in parallel. Bit rearrangement and sample ordering is also performed to reconstruct

the samples in the correct order. As required by the FFT function, the samples must be converted to signed values by removing the ADC DC-level code.

Here, symbol alignment is vital to ensure that the 40 parallel samples captured by the deserialisers in the receiver originate from the same symbol generated in the transmitter. Symbol alignment is performed by continuous transmission of symbols of a fixed pattern over the transmission system. By using the FPGA embedded logic analyser (SignalTap II) with JTAG connection to a PC, the captured samples of the fixed symbols can be viewed, thus the sample offset is determined and subsequently compensated by adjusting the inserted sample offset accordingly. It should be pointed out, in particular, that such a symbol alignment process is performed only once at the establishment of a transmission connection.

The first 8 samples of each of the captured symbols are removed, as they correspond to the cyclic prefix added in the transmitter. This leaves 32 samples for input to the 32 point FFT function, which determines the phase and amplitude of each subcarrier. At the FFT output, 15 subcarriers in the positive frequency bins are selected for decoding, subsequently the recovered data bits from each symbol are analysed by a BER analyser function, which regenerates the transmitted bit pattern, synchronises it with the received pattern and continuously detects and counts bit errors.

The bit error count over 100 million symbols is continuously updated and displayed with the embedded logic analyser, this enables fine adjustment of the system parameters to maximize the transmission performance. In addition, the logic analyser also displays and continuously updates the total number of bit errors and the corresponding symbols accumulated since the start of a transmission session. This enables the measurement of BERs at unlimited low values, provided that a sufficiently long operation time is allowed.

For the present demonstration, system clocks for both the transmitter and the receiver are generated from a common reference source. However, it is worth mentioning that, we have developed an advanced technique for clock recovery in the receiver, which, according to simulation results, has sufficiently high accuracy and does not require highly stable and expensive voltage control oscillators. As the thrust of the present paper is to demonstrate experimentally the proof-in-principle of the real-time OOFDM transceivers, the clock recovery technique is, therefore, not implemented in the real-time OOFDM transceivers presented in this paper. The implementation and transmission performance of real-time OOFDM transceivers incorporating clock recovery will be reported elsewhere in due course.

DQPSK signal modulation has the property that no channel estimation is necessary, as data is encoded using differential phase change only. To further improve the transmission capacity, the use of higher signal modulation formats such as M-ary QAM is essential. In M-ary QAM systems, the involvement of both amplitude and phase values means that channel estimation is vital. Very recently, we have developed a novel pilot subcarrier-assisted channel estimation technique [10], which has a number of salient advantages including, for example, high accuracy, low complexity, small pilot bandwidth usage, excellent stability and buffer-free data flow. The detailed operating principles of the technique have been reported in [10], in which rigorous evaluations of the technique have also been made under various operating conditions. In this paper, the channel estimation technique is implemented, and comparisons of the transmission performance are made between DQPSK-encoded and 16-QAM-encoded OOFDM signals at 3Gb/s.

3.2 Transceiver architecture improvements

Compared to the transceiver design reported in [9,10], a number of important new functionalities have been developed, fully verified and incorporated in the transceiver considered. These new functionalities are summarized as followings:

  • The FPGA logic design is adapted for clocking at 100MHz (twice the previous speed) to support a doubling of the symbol rate. The sample rate of the DAC and ADC is also increased from 2GS/s to 4GS/s. This is accompanied with a doubling of the data rate of the associated digital interface with the FPGAs. Clearly, these amendments

improve the operating speed of the OOFDM transceiver by a factor of 2 for a fixed signal modulation format.

- As already mentioned in Section 3.1, the advanced channel estimation technique is implemented, supporting not only the use of arbitrary modulation formats on subcarriers but also live measurements of end-to-end channel frequency responses. This feature enhances significantly the robustness and flexibility of the transceiver, and also provides an effective means for live monitoring of channel quality.

- Live transceiver optimisation. Such property is realised due to the inclusion of the following two new features: a) provision of real-time BERs for all individual subcarriers; b) key transceiver parameters such as signal clipping ratio can be adjusted while the transceiver is still in operation. This feature is very useful for achieving a highly optimised transceiver design for practical implementation.
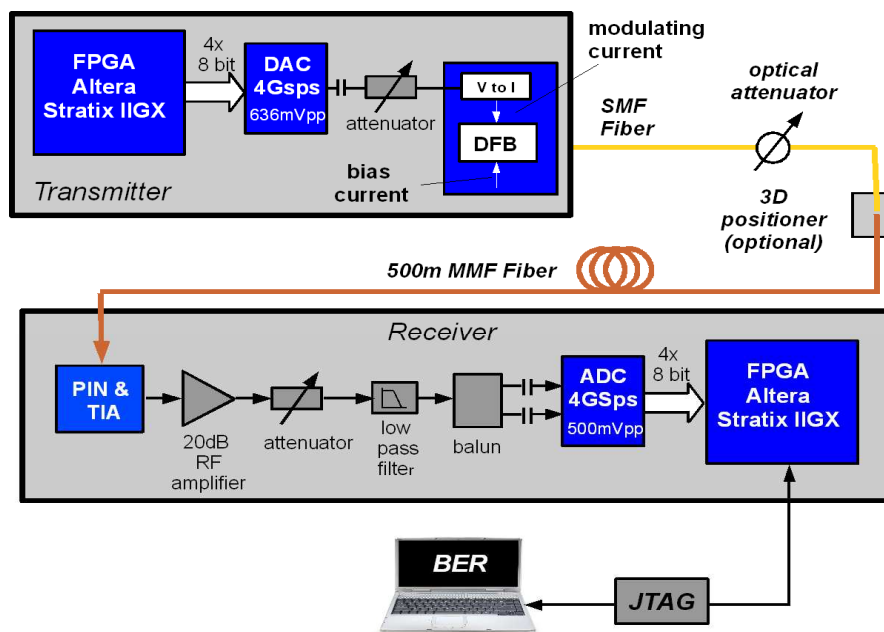

Fig. 3. Experimental system setup.

3.3 Experimental system setup

Figure 3 shows the real-time experimental system setup. The electrical signal from the DAC is first attenuated as required to optimise the modulating current, then it is employed, together with an adjustable DC bias current, to modulate a single-mode 1550nm DFB laser with a 3-dB modulation bandwidth of approximately 10GHz. The OOFDM signal from the DFB laser is coupled, via a variable optical attenuator and an optional 3D positioner, into a 500m 62.5/125μm OM1 MMF having a 3dB optical bandwidth of about 675MHz·km and a linear loss of 0.6dB/km. An optical attenuator is used to control the optical power launched into the MMF link.

At the receiver, the OOFDM signal is detected using a 20GHz PIN with TIA. The PIN has a receiver sensitivity of −17dBm (corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}). The optical-to-electrical converted signal is first amplified with a 2.5GHz, 20dB RF amplifier, then attenuated as necessary to optimise the signal amplitude to suit the ADC's input range. This adjustment also provides electrical gain control to compensate for optical signal attenuation. After passing through an electrical low-pass filter with a 3-dB

bandwidth of 2.4GHz, the signal is converted via a balun to a differential signal and then digitized by a 4GS/s, 8-bit ADC in the receiver. It should be noted that, the bandwidths of the RF amplifier and the low-pass filter are larger than that corresponding to the OOFDM signal (2GHz for the 4GS/s ADC/DAC). Therefore, these two electrical components do not introduce significant spectral distortions into the OOFDM signal. The system frequency response roll-off effect observed in Fig. 6 and Fig. 9, is mainly due to the DAC employed in the transmitter.
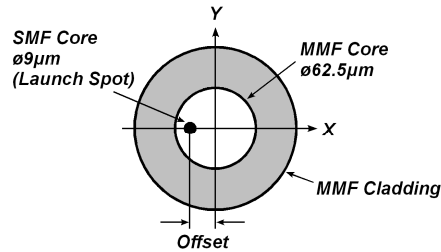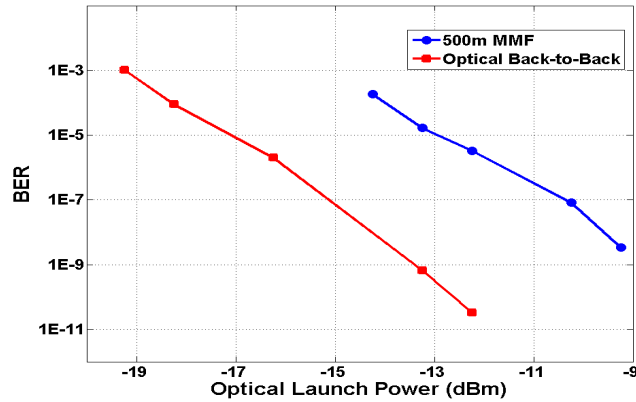

Fig. 4. Launch offset

Fig. 5. BER performance of 3Gb/s DQPSK-encoded OOFDM signal transmission over a 500m MMF.

To examine performance robustness to different offset launch conditions, the optical signal from the DFB laser can be coupled into the MMF via a 3D positioner, which enables the fine adjustment of position of laser launch spot to emulate different launch offsets. The definition of the offset can be found in Fig. 4. As a reference point, the central launch position is identified first by adjusting the position of the laser launch spot in the X and Y dimensions until the optical power received at the far end of the MMF is maximised with the corresponding offset ranges being symmetrical and maximized in both the X and Y dimensions. For the MMF adopted in the experiments, the maximum offset range without affecting significantly the output optical power is about ± 25μm.

4. Experimental results

4.1. DQPSK-encoded OOFDM transmission performance

Experimental measurements are first performed of the transmission performance of 3Gb/s DQPSK-encoded OOFDM signals in an IMDD 500m MMF system involving the DML, as shown in Fig. 3. The measured BER as a function of optical launch power is plotted in Fig. 5 for cases of optical back-to-back and 500m MMF transmission. The FPGAs operate at a clock

speed of 100MHz, and the sample rates of the DAC/ADC are 4GS/s. The DFB bias current is set to 38mA. A 1m mode conditioning patch chord is used to couple the optical signal into the MMF transmission system.
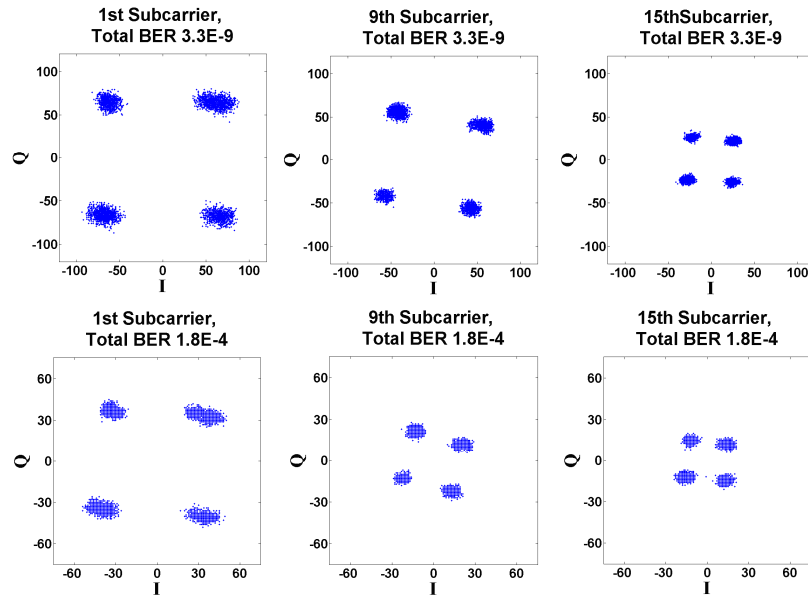

Fig. 6. Constellations of various DQPSK-encoded subcarriers for 3Gb/s signals after transmitting through the 500m MMF.

It can be seen from Fig. 5 that, for the case of 500m MMF transmission (optical back-to-back), a BER as low as 3.3×10^{-9} (3.3×10^{-11}) is achieved at optical launch powers of >-9.2dBm (>-12dBm). In particular, for both cases there is no error floor observed within the BER ranges of practical interest. Taking into account the total linear link loss of about 1dB, an optical power penalty of approximately 3dB at a BER of 1.0×10^{-4} can be obtained from Fig. 5. This penalty mainly results from the MMF-induced differential mode delay (DMD) effect [12].

After transmitting through the 500m MMF, the constellations of the 1st, 9th and 15th subcarriers are presented in Fig. 6 for two representative BERs of 3.3×10^{-9} and 1.8×10^{-4}. As seen in Fig. 6, the subcarrier amplitude decreases rapidly for subcarriers locating at high frequencies. The roll-off effect is mainly due to the analogue electrical components (DAC) involved in the transceiver, as very similar behaviour also occurs for an analogue electrical back-to-back case where the electrical signal from the attenuator in the transmitter is directly linked to the low-pass filter in the receiver without any optical components being involved.

4.2. Performance robustness to different offset launch conditions

Experimental explorations are also undertaken of performance robustness to different offset launch conditions. The transmission link configuration and the transceiver parameters are identical to those used in obtaining Fig. 5, except that a 3D positioner is utilised here, as shown in Fig. 3. For 3Gb/s transmission of DQPSK-encoded OOFDM signals over the 500m MMF, the measured BER versus launch offset is given in Fig. 7, in which the variation of the corresponding optical launch power at the input facet of the MMF link is also presented. Figure 7 shows excellent performance robustness with BERs of $<1.0 \times 10^{-5}$ being maintained over the entire launch offset range from −25μm to 25μm. In particular, as expected, an improved BER performance occurs at the conventional offset launch region (around ± 20μm) [13]. The results imply that the adopted cyclic prefix is sufficiently longer than DMDs associated with different launch offsets [14]. It is also expected that both the performance

robustness and the corresponding transmission capacity can be improved further if use is made of adaptive modulation on different subcarriers within an OOFDM symbol [14].
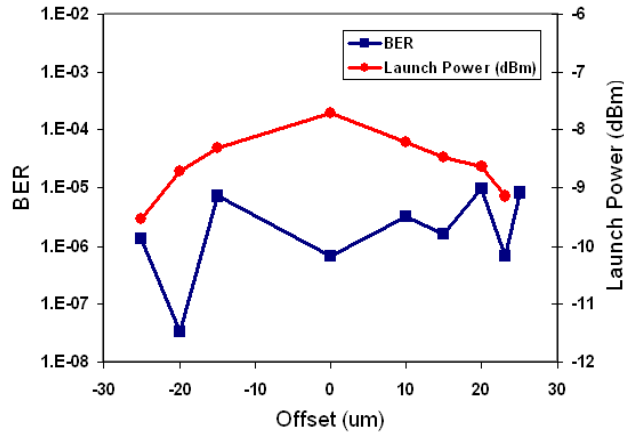
Fig. 7. BER and optical launch power versus launch offset for 3Gb/s over 500m MMF transmission of DQPSK-encoded OOFDM signals.
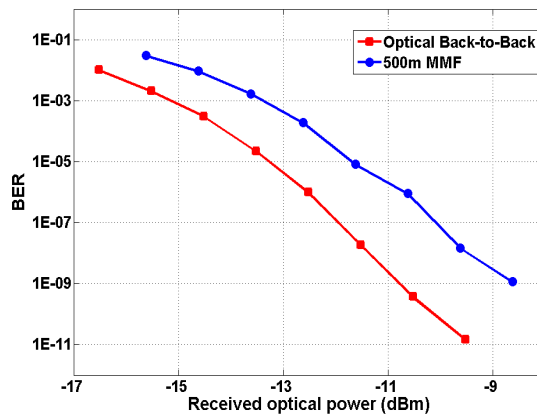
Fig. 8. BER performance for 16-QAM encoded 3Gb/s OOFDM signal transmission over a 500m MMF.

4.3. 16-QAM-encoded OOFDM transmission performance

With the FPGAs' operating speeds and the sample rates of the DAC/ADC being set at 50MHz and 2GS/s, respectively, as well as incorporating the channel estimation technique in the OOFDM transceiver design, a 3Gb/s OOFDM signal can be produced when 16-QAM is taken on all the 15 data-carrying subcarriers. The explorations of the transmission performance of the 16-QAM-encoded 3Gb/s OOFDM signal over the transmission system identical to that used in obtaining Fig. 5, not only enable us to evaluate thoroughly the transceiver design, but also provide an excellent opportunity for comparing the transmission performance of different modulation format-encoded OOFDM signals for achieving the signal bit rate of 3Gb/s.

Fig. 9. Constellations of 16-QAM-encoded subcarriers for 3Gb/s OOFDM signals after transmitting through a 500m MMF.

For the above-mentioned transmission system scenario, the measured BER versus received optical power is shown in Fig. 8, in obtaining which, the DFB bias current is set to 36mA. It is shown in Fig. 8 that for received optical powers of >-8.6dBm (>-9.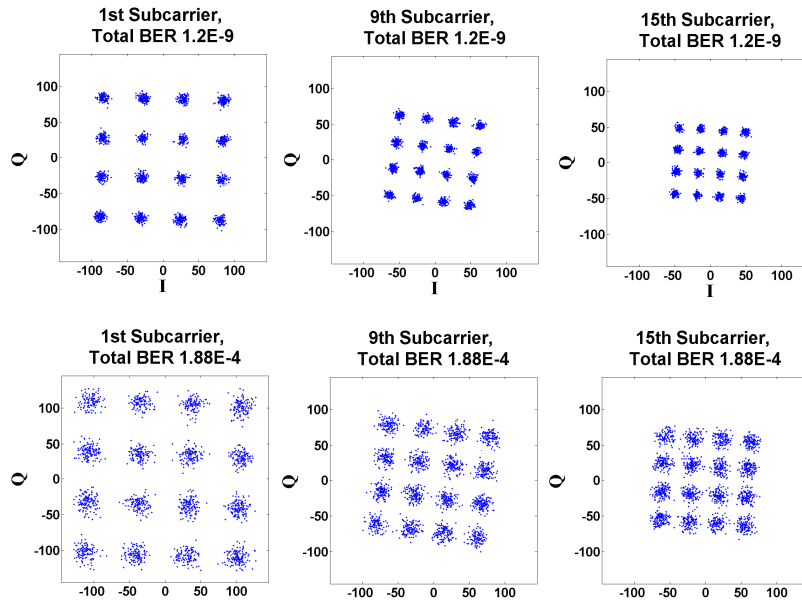5dBm), BERs lower than 1.2×10^{-9} (1.5×10^{-11}) are measured for 500m MMF transmission (optical back-to-back), and that no error floor is observed. As optical back-to-back systems at low received optical power regions are additive white Gaussian noise (AWGN)-limited, comparisons of optical back-to-back performances between Fig. 8 and Fig. 5 show that, for achieving a BER of 1.0×10^{-4}, a 3.7dB increase in optical power is required if DQPSK is replaced by 16-QAM. This is in excellent agreement with theoretical predictions published previously [15]. In addition, Fig. 8 also shows a power penalty of approximately 2dB at a BER of 1.0×10^{-4}, which is lower than that shown in Fig. 5. The physics underpinning such a difference is that, the cyclic prefix duration corresponding to the 3Gb/s 16-QAM-encoded signal is doubled in comparison with that corresponding to the 3Gb/s DQPSK-encoded signal. This provides a better compensation of the DMD effect. In addition, compared to the DQPSK-encoded signal, the transmission bandwidth associated with the 16-QAM-encoded signal is halved. As a direct result, it can be seen from Fig. 9 that the roll-off effect is not as significant as those observed in Fig. 6. Similar to Fig. 6, Fig. 9 presents the constellations of the 1st, 9th and 15th subcarriers prior to channel equalization for two representative BERs of 1.2×10^{-9} and 1.88×10^{-4} after transmitting through the 500m MMF.

5. Conclusion

Real-time OOFDM transceivers based on off-the-shelf components including FPGAs, DACs and ADCs have been experimentally demonstrated successfully at 3Gb/s transmission, for the first time, utilising self-developed IFFT/FFT logic algorithms verified at 10Gb/s. The developed transceivers also incorporate a number of key functionalities including live transceiver optimisation and advanced channel estimation. The fastest ever real-time end-to-end transmission of 3Gb/s DQPSK- and 16-QAM-encoded OOFDM signals over 500m MMFs has been achieved with BERs of $<3.3\times10^{-9}$ in DML-based IMDD systems. In addition, excellent performance robustness has also been observed to various offset launch conditions. This work is a significant breakthrough in demonstrating the great potential of the OOFDM technique for practical implementation in optical networks of various architectures.

Considering the FPGA-based DSP nature of the real-time OOFDM transceiver, extensive research is currently being undertaken in our research group to further improve the transceiver design and performance, and new exciting results are appearing. It is strongly envisaged that a significant increase in transmission capacity may be achieved in the near future, which will be reported elsewhere in due course. In addition, it is estimated that the cost of a DFB-based intensity modulator takes a majority of the total cost of a real-time OOFDM transceiver. For cost-sensitive application scenarios, it is, therefore, greatly beneficial if use can be made of very cheap intensity modulators such as vertical cavity surface emitting lasers (VCSELs) and reflective semiconductor optical amplifiers (RSOAs), real-time OOFDM transceiver performance using these low cost intensity modulators is therefore also to be investigated.

First experimental demonstration of 6Gb/s real-time optical OFDM transceivers incorporating channel estimation and variable power loading

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Abstract: The fastest ever 6Gb/s real-time FPGA-based optical orthogonal frequency division multiplexing (OOFDM) transceivers utilizing channel estimation are experimentally demonstrated, for the first time, with variable power loading being incorporated to effectively compensate for the rapid system frequency response roll-off effect. The implemented transceivers are constructed entirely from off-the-shelf components and incorporate crucial functionalities of on-line performance monitoring and live optimization of key parameters including signal clipping, subcarrier power and operating conditions of directly modulated DFB lasers (DMLs). Real-time end-to-end transmission of a 6Gb/s 16-QAM-encoded OOFDM signal over 300m OM1 multi-mode fiber with a power penalty of 0.5dB is successfully achieved in an intensity-modulation and direct-detection system employing a DML.

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1. Introduction

Since the original proposal of the concept of optical orthogonal frequency division multiplexing (OOFDM) in 2005 [1], great effort has been expended on investigating the transmission performance of various OOFDM variants for different optical network scenarios including long-haul systems [2,3], metropolitan area networks [4,5] and local area networks [6,7], this is because the OOFDM technique has demonstrated a number of unique and inherent advantages including, for example, great resistance to dispersion impairments, efficient utilization of channel spectral characteristics, potential for cost-effective implementation due to the rapid advances in modern digital signal processing (DSP) technology, dynamic provision of hybrid bandwidth allocation in both the frequency and time domains, and significant reduction in optical network complexity.

However, all the experimental works reported so far [1–7] have been undertaken using off-line DSP approaches, which do not consider the limitations imposed by the precision and speed of practical DSP hardware required for realizing real-time OOFDM transmission. The experimental demonstration of real-time OOFDM transceivers is critical for not only rigorously evaluating the OOFDM technique but also establishing a solid platform for exploring the feasibility of the technique for practical implementation in optical networks of various architectures. The implementation of highly complex, computationally intense and high-speed signal processing algorithms with sufficient precision and the availability of high-speed data converters with large number of quantization bits are the major challenges in experimentally demonstrating real-time OOFDM transceivers. It is, however, noted that multi-gigabit real-time OOFDM receivers have been demonstrated in coherent transmission systems, where off-line DSP approaches are still adopted in corresponding transmitters [8,9].

In April 2009, we made a significant breakthrough in experimentally demonstrating the world-first real-time OOFDM transceivers based on real-time DSP implemented with Altera Stratix II GX field-programmable gate arrays (FPGAs) [10]. The implemented transceivers support real-time end-to-end transmission of a 1.5Gb/s differential quadrature phase shift keying (DQPSK)-encoded OOFDM signal over a 500m multi-mode fibre (MMF)-based, intensity-modulation and direct-detection (IMDD) system incorporating a directly modulated DFB laser (DML) [10]. In May 2009, considerable improvement in the real-time OOFDM transceiver architectures was made, and real-time end-to-end transmission of a 3Gb/s DQPSK-encoded OOFDM signal with a bit error rate (BER) as low as 3.3×10^{-9} was successfully achieved over a 500m MMF with excellent performance robustness to various

offset launch conditions [11,12]. In June 2009, we proposed, implemented and experimentally verified a novel pilot subcarrier-assisted channel estimation technique [13], which offers a number of salient features including high accuracy, low complexity, small pilot bandwidth usage, excellent stability and buffer-free data flow. Based on the channel estimation technique, 3Gb/s 16-quadrature amplitude modulation (QAM)-encoded real-time end-to-end OOFDM transmission has been demonstrated, in one case over a 75km MetroCor single-mode fibre (SMF) with a −2dB power penalty in a DML-based IMDD system without in-line optical amplification and chromatic dispersion compensation [13]. As strong evidence of the accuracy of the proposed channel estimation technique, BERs as low as 1.0×10^{-10} have been observed [13]. In July 2009, the fastest ever 6Gb/s real-time OOFDM transceivers using 16-QAM encoding in a DML-based IMDD MMF transmission link was achieved and announced in the presentation of our OECC'2009 postdeadline paper [14].

In this paper, the 6Gb/s real-time 16-QAM OOFDM transceiver architecture is reported in detail. The design is an adaptation of a previously reported architecture using DQPSK at 3Gb/s [11,12]. 16-QAM encoding/decoding is also utilised by incorporating the novel pilot subcarrier-assisted channel estimation technique developed and rigorously validated in [13]. In addition, a variable power loading scheme is also implemented experimentally here, for the first time, in real-time OOFDM signal transmission. Furthermore, enhanced functionalities of on-line performance monitoring and live parameter optimisation are exploited. The improved transceiver architecture provides opportunities for not only the use of high modulation formats but also the on-line performance monitoring of the system frequency responses, based on which variable power loading on different subcarriers can be performed providing pre-equalisation to compensate for any amplitude variations in the system frequency response. Live parameter optimisation provides an effective means of optimising, during signal transmission, key parameters including, for example, signal clipping, subcarrier amplitude and operating conditions of DMLs. The live optimisation is conducted based on on-line monitoring of individual subcarrier BER and total channel BER.

With the improved OOFDM transceiver design, the fastest ever real-time end-to-end transmission of 6Gb/s 16-QAM-encoded OOFDM modulated data is achieved over 300m OM1 MMFs in DML-based IMDD transmission systems. Here, it is worth emphasising that such ground-breaking results are obtained by adopting

- Off-the-shelf electrical components including FPGAs, digital-to-analogue converters (DACs) and analogue-to-digital converters (ADCs)

- Cost-effective conventional optical components such as DMLs

- Worst-case OM1 MMFs

- An extremely simple single-channel IMDD system configuration without utilising optical amplification and mode-selective techniques [15].

Therefore, this work is a significant milestone demonstrating the true practicality of real-time OOFDM transceivers for providing multi-gigabit transmission bandwidths in cost-sensitive optical networks. In addition, it should be pointed out, in particular, that the implemented real-time OOFDM architectures are also very versatile, they can be employed in not only MMF-, plastic optical fibre- (POF)- and SMF-based IMDD transmission systems but also SMF-based coherent long-haul transmission systems after modifications to the transceiver design.

2. Real-time OOFDM transceiver architecture and experimental system setup

Figure 1 shows the detailed architectures of the real-time transmitter (top) and the real-time receiver (bottom) implemented in FPGAs. As detailed descriptions of the real-time transceiver architectures using DQPSK have already been made in [12], here an outline of the real-time transceivers using 16-QAM is provided with emphasis being given to the practical

implementations of channel estimation, variable power loading and improved functionalities of on-line performance monitoring and live parameter optimisation.
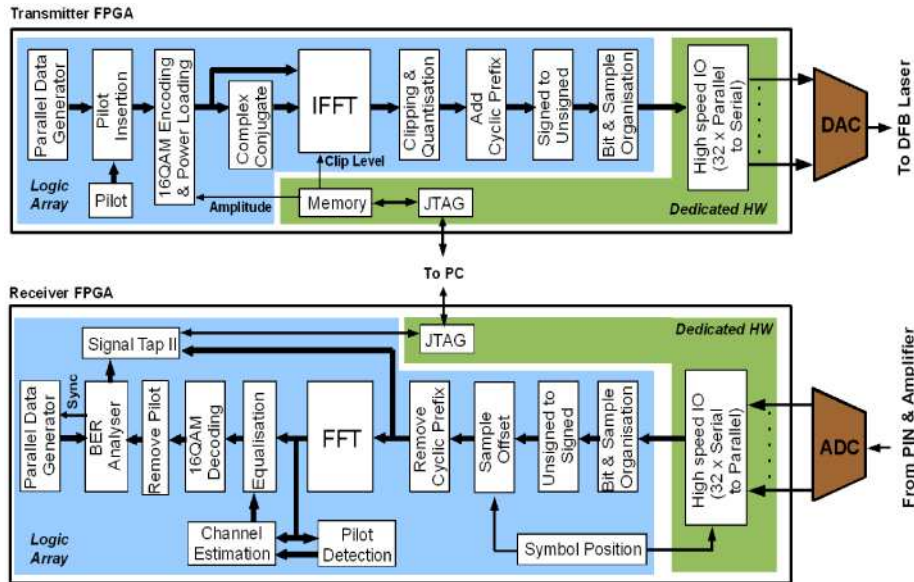

Fig. 1. Real-time OOFDM transceiver architectures with channel estimation, variable power loading and improved functionalities of on-line performance monitoring and live parameter optimisation.

2.1 IFFT/FFT logic function

The core algorithms required for OFDM signal processing are the inverse fast Fourier transform (IFFT) and fast Fourier transform (FFT). We have developed our own custom implementation of a 32 point IFFT/FFT logic function employing a radix-2 decimation-in-time structure consisting of 2-point butterfly elements as the core computational building blocks [10–14]. To achieve high-speed performance, the IFFT/FFT logic function design is based on a highly pipelined architecture using a number of extensively paralleled processing stages. In comparison with using commercially available functions, the self-developed IFFT/FFT logic function has a number of salient advantages listed as followings [12]:

- Full control and optimisation of key logic function parameters. The parameters include computational precision at each stage of the IFFT/FFT function, as well as clipping and quantization of output samples.

- Ease of scalability for accommodating a larger number of subcarriers and excellent adaptability for supporting higher clock speeds.

- Control of FPGA logic resource usage.

The IFFT/FFT logic function design has been validated for 9.375Gb/s operation [10,12]. Experimental measurements suggest that the design can also be scaled to support higher data rates potentially in excess of 40Gb/s in the Altera Stratix II GX FPGA employed in the transceivers.

2.2 Real-time transmitter

In the transmitter, the 32 point IFFT logic function supports 32 equally spaced subcarrier frequencies of which 15 are located in the positive frequency bins occupying the whole Nyquist band, therefore no oversampling is adopted for the system considered in this paper. A 56-bit wide parallel pseudo random bit sequence of length 88,500 words (4.779×10^6 bits) is

employed as information data. One extra parallel bit sequence of a fixed 4-bit wide pattern is used to represent pilot data. To maximise the signal to noise ratio of the received pilot data in the receiver, the fixed pilot pattern corresponds to one of the four diagonal end points of the 16-QAM constellation. Prior to feeding 15 16-QAM encoders, the pilot data is embedded in the information data in such a way that the pilot data occurs on successive subcarriers in consecutive OOFDM symbols [13]. Such pilot data allocation allows highly accurate, interpolation-free channel estimation on all the subcarriers across the entire signal spectrum. In addition, it does not require buffering of the information data transported on the other subcarriers, as there are always 14 subcarriers available in each symbol to convey information data. The 60-bit wide data constructed from the information and pilot data bit sequences is employed to feed the 15 parallel 16-QAM encoders. The peak signal amplitude is fixed for each encoder according to the power loading distribution in use. To control the total signal power the amplitudes of the 15 subcarriers, carrying either the encoded information data or pilot data, can be adjusted with a common scaling factor stored in the embedded memory, which can be updated during live data transmission via the JTAG interface. Such live amplitude adjustment can also be easily extended to allow independent subcarrier power control, which is crucial for implementing advanced power and bit loading algorithms [7].

At the input of the IFFT, the aforementioned 15 subcarriers and one extra subcarrier having zero power at zero frequency are arranged to satisfy the Hermitian symmetry with respect to their complex conjugate counterparts. The self-developed IFFT logic function is then employed to perform the IFFT to all the 32 subcarriers. At the output of the IFFT, real-valued OOFDM symbols having 32 samples are produced.

After the IFFT, the 32 signed, real-valued samples are clipped and quantized. The clipping level is also stored in the embedded memory and can be updated, during live transmission, to optimise the transceiver performance. The number of quantization bits is set to 8 to match the resolution of the employed DAC. To mitigate the inter-symbol interference (ISI) effect caused by optical dispersion, a cyclic prefix of 8 samples is added to each symbol, giving rise to 40 samples per symbol. The internal system clock is set to 100MHz, and the parallel signal processing approach results in a 100MHz symbol rate. The 100MHz symbol rate and 40 samples per symbol give a sample rate of 4GS/s. The signed samples are converted to unsigned values by adding an appropriate DC offset, as the DAC requires positive values only. After performing sample ordering and bit arrangement, the unsigned 40 samples are streamed to the DAC interface at 4GS/s. The entire symbol consisting of 320 bits is fed in parallel to 32 high speed 10:1 dedicated hardware serialisers, the interface thus consists of 4 samples transferred in parallel at a rate of 1GHz, giving the required aggregated sample rate of 4GS/s. The DAC generates an analogue electrical OOFDM signal having a maximum peak-to-peak voltage of 636mV, the electrical signal is then used to directly modulate a DML, as described in Section 2.4.

2.3 Real-time receiver

At the receiver, after performing optical-to-electrical conversion using a PIN, the analogue electrical signal is amplified as necessary, low pass filtered and then digitised by an 8-bit ADC operating at 4GS/s. A digital interface, which is identical to that of the DAC in the transmitter, transfers the digital samples at 4GS/s to the second FPGA. The 32 high-speed, 1:10, dedicated hardware deserialisers capture 40 received samples in parallel. Bit rearrangement and sample ordering is also performed to reconstruct the samples in the correct order. As required by the FFT function, the samples must be converted to signed values by subtracting the corresponding ADC DC level.

Symbol synchronisation is vital to ensure that the 40 parallel samples captured by the deserialisers in the receiver originate from the same symbol generated in the transmitter. Symbol synchronisation is performed by continuous transmission of symbols of known fixed patterns over the transmission system. By using the FPGA embedded logic analyser (SignalTap II) via a JTAG connection to a PC, the captured samples of the fixed pattern symbols can be viewed, thus the sample offset is determined and subsequently compensated

by adjusting the inserted sample offset accordingly. It should be pointed out, in particular, that such a symbol synchronisation process is performed only once at the establishment of a transmission connection.

After symbol synchronisation, the first 8 samples of each of the captured symbols are removed, as they correspond to the cyclic prefix added in the transmitter. This gives rise to 32 samples per symbol for input to the 32 point FFT function, which determines the phase and amplitude of each subcarrier.

At the FFT output, 15 subcarriers in the positive frequency bins are selected for channel estimation and subsequent data recovery. As described in detail in [13], at the start of transmission, the position of a symbol with its first subcarrier being the pilot subcarrier is first detected, which is regarded as a pilot subcarrier reference point. Based on the reference point, all the pilot subcarriers in the subsequent symbols can be identified easily based on their fixed relative positions. Making use of the assigned and received pilot subcarriers, the system frequency response, H_k (k= 1, 2, …N_s), can be obtained by performing the operation given below

$$H_k = \frac{1}{M} \sum_{i=0}^{M-1} \frac{R_{(k+iN_s),k}}{p_{(k+iN_s),k}}$$ (1)

where N_s is the total number of non-zero-power subcarriers in the positive frequency bins. $R_{(k+iN_s),k}$ ($p_{(k+iN_s),k}$) is the received (effectively assigned) complex value of the k-th pilot subcarrier in the $(k+iN_s)$-th symbol. To effectively reduce the noise effect associated with the transmission system, frequency response averaging is performed over M received/assigned pilot subcarriers of the same frequency. Here M is taken to be 32, which is an optimum value identified experimentally in [13]. It should be noted that all other channel estimation parameters that are not explicitly mentioned above, are taken to be the values identical to those presented in [13].

Having obtained the system frequency response, channel equalization is conducted using the following operation

$$X_{m,k} = \left(H_k\right)^{-1} \chi_{m,k}$$ (2)

where $\chi_{m,k}$ is the received complex value of the k-th subcarrier in the m-th symbol. The equalised subcarriers, $X_{m,k}$, are then decoded with 15 parallel 16-QAM demodulators. After removing the pilot subcarrier data, the transmitted data is finally recovered. It is important to note that the channel estimation technique allows pilot data to only be inserted as regular bursts of pilots, allowing all the 15 subcarriers to be used for data transmission between pilot bursts. The insertion rate of the pilot bursts can be as low as 10Hz, leading to an extremely low overhead for channel estimation [13]. In addition, use is also made of the measured system frequency response to adjust the subcarrier amplitude in the transmitter to enable the implementation of variable power loading.

The recovered bit sequence is analysed by a BER logic function. Both the total channel bit error count and the individual subcarrier error counts over 88,500 symbols are continuously measured, updated and displayed with the BER analyser. This allows the calculation and display of the total channel BER, BER_T, and the subcarrier BER, BER_K, which have the following relationship

$$BER_T = \frac{1}{N_s} \sum_{K=1}^{N_s} BER_K$$ (3)

The on-line BER and system frequency response monitoring enables the transmission performance to be optimised by fine adjustment of the transceiver parameters, electrical gain and DML operating conditions. In addition, the BER analyser logic also displays and continuously updates the total number of error bits and the corresponding symbol count accumulated since the start of a transmission session. This enables the measurement of BER_T at unlimited low values, provided that a sufficiently long operation time is allowed.

For the current transceiver design, system clocks for both the transmitter and the receiver are generated from a common reference source. The FPGAs use a 100MHz reference clock and both the DAC and ADC use a 2GHz reference clock. Here, it is worth mentioning that, very recently we have proposed and theoretically verified a high-speed and accurate synchronisation technique, which automatically performs clock recovery and symbol alignment in the FPGA of the receiver without requiring highly stable and expensive voltage controlled oscillators. The implementation and transmission performance of such an advanced clock recovery technique in the real-time OOFDM transmission systems is beyond the scope of the present paper and will be reported elsewhere in due course.
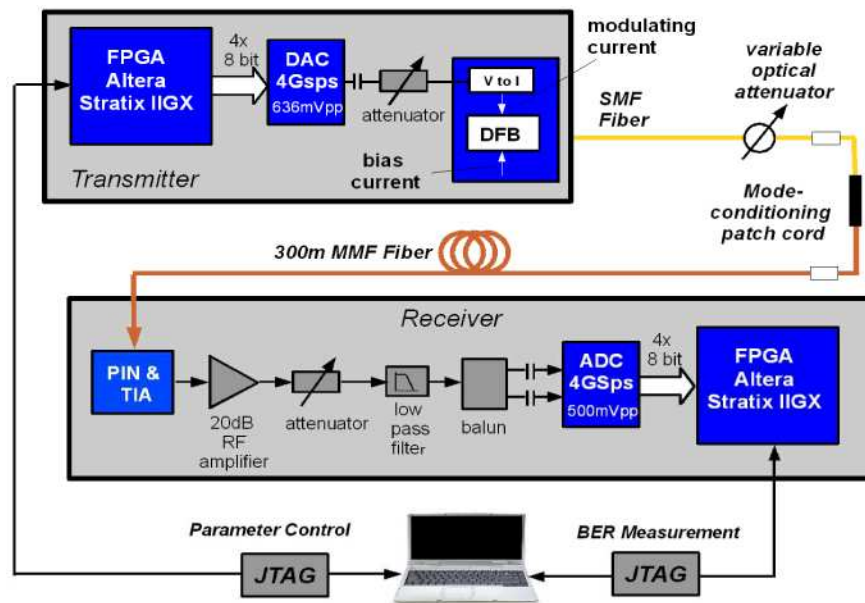

Fig. 2. Real-time experimental system setup.

2.4 Experimental system setup

Figure 2 shows the real-time experimental system setup. The voltage level of the electrical signal from the DAC is first attenuated as required to provide, after voltage to current conversion, an optimum modulating current. The optimised modulating current is then combined with an adjustable DC bias current to drive a single-mode 1550nm DFB laser with a 3-dB modulation bandwidth of approximately 10GHz and a maximum optical output power of about 0dBm. The OOFDM signal emerging from the DML is coupled, via a SMF patch chord, to a variable optical attenuator, which is utilized to control the optical power launched into the MMF link. The attenuated optical signal is coupled, via a mode-conditioning patch cord, into a 300m 62.5/125μm OM1 MMF having a 3-dB optical bandwidth of approximately 675MHz•km and a linear loss of 0.6dB/km.

At the receiver, the OOFDM signal transmitted through the MMF link is detected using a MMF pigtailed, 20GHz PIN detector with TIA. The PIN has a receiver sensitivity of −17dBm (corresponding to 10Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}). The optical-to-

electrical converted signal is first amplified with a 2.5GHz, 20dB RF amplifier, then attenuated as necessary to optimise the signal amplitude to suit the ADC's input range of ±250mV. Such adjustment also provides electrical gain control to compensate for optical signal attenuation. After passing through an electrical low-pass filter, the signal is converted via a balun to a differential signal and then digitized by a 4GS/s, 8-bit ADC in the receiver.

3. Experimental results

As already discussed in Section 2, with the 100MHz FPGA operating speeds and the 4GS/s sample rates of the DAC/ADC, the fastest ever 6Gb/s real-time OOFDM signals are produced when 16-QAM is taken on all the 15 information-bearing subcarriers. It should be pointed out, in particular, that the obtained 6Gb/s transmission capacity can be utilised almost entirely to carry useful data. This originates from the following three facts: 1) the 6Gb/s signal bit rate is obtained after subtracting the transmission capacity corresponding to the cyclic prefix from the raw signal line rate of 7.5Gb/s; 2) as described in Section 2.3, subcarrier-assisted channel estimation requires an extremely low overhead, and 3) no other training sequences are employed in the transmission system. In this section, extensive use is made of the 6Gb/s 16-QAM-encoded OOFDM signals to explore: 1) the effectiveness of the variable power loading scheme, and 2) the transmission performance of the 6Gb/s 16-QAM-encoded real-time OOFDM signals over the DML-based IMDD OM1 MMF system illustrated in Fig. 2. The performance and stability of the channel estimation technique has already been presented in detail in [13], therefore no further discussions on such a topic are made in this paper. All the experimental measurements presented in this section are based on an optimised DFB bias current of 37mA, which gives an optical output power of −4.2dBm.
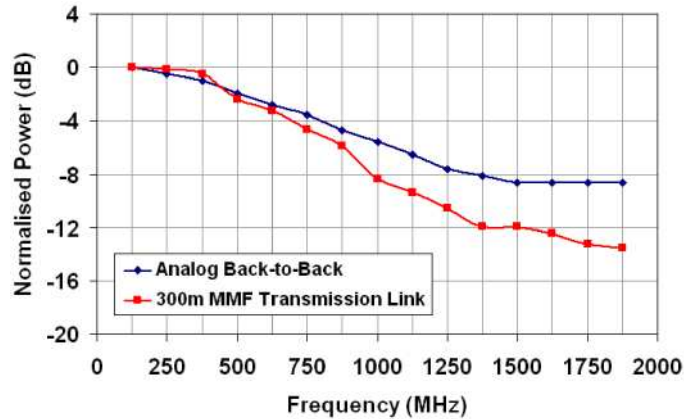

Fig. 3. Measured system frequency responses for analogue back-to-back and 300m MMF transmission link configuration.

3.1. Effectiveness of the variable power loading scheme

The measured frequency responses of the transmission systems from the IFFT in the transmitter to the FFT in the receiver are shown in Fig. 3 for two different scenarios: a) a transmission system with the 300m OM1 MMF being considered, and b) an analogue back-to-back case, where the electrical attenuator in the transmitter is directly connected to the low-pass filter in the receiver, as shown in Fig. 2. In obtaining Fig. 3, equal digital subcarrier amplitudes in the transmitter are applied, and the resulting frequency responses are normalised to the first subcarrier power. It can be seen from Fig. 3 that the system frequency responses decay very rapidly within the signal spectral region from 0.125GHz to 1.875GHz. Comparisons between the curves for these two frequency responses imply that the system frequency response roll-off effect is mainly due to effects of the analogue electrical elements including, for example, DAC output filtering and the sin(x)/x response inherent to a zero-

order hold DAC output, as the associated digital electronics have flat frequency responses. In addition, as demonstrated in Fig. 3, the inclusion of optical components in the transmission system decreases further the frequency response in the high frequency region. The 300m MMF employed is the major contributor to the optical component-induced frequency response roll-off effect, as both the DFB modulation bandwidth and the PIN bandwidth are much larger than that corresponding to the 300m MMF. The observed rapid system frequency response roll-off effect indicates that the use of variable power loading is essential to achieve acceptable BERs over all subcarriers.

In the 300m MMF transmission system, the implementation and effectiveness of the variable power loading scheme are explored in Fig. 4, where the received digital subcarrier amplitudes prior to channel equalization are plotted against subcarrier number for the cases of utilising equal power loading and variable power loading. In Fig. 4, the variable power-loaded digital subcarrier amplitudes in the transmitter are also given, together with the relative error bits defined as a percentage ratio between the total number of detected error bits on a specific subcarrier and the corresponding total number of error bits aggregated over the entire transmission channel.
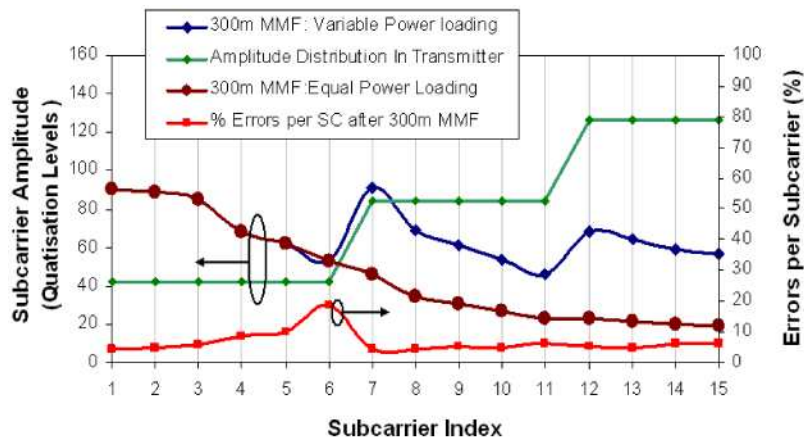

Fig. 4. Received subcarrier amplitudes for equal power loading and variable power loading. Variable power-loaded subcarrier amplitudes in the transmitter and their corresponding relative error bits after transmitting through a 300m MMF are also shown.
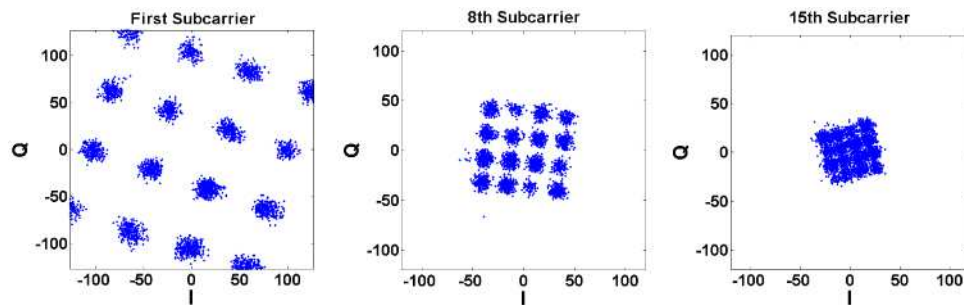
Fig. 5. Constellations of different subcarriers of real-time 6Gb/s 16-QAM-encoded OOFDM signals with equal power loading after transmitting through a 300m MMF. The measured total channel BER is approximately 1.0×10^{-2}.

It can be seen in Fig. 4 that, for equal power loading, the received digital subcarrier amplitudes are very similar to the system frequency response presented in Fig. 3, thus resulting in significant amplitude differences between the low and high frequency subcarriers. As a direct result, the complex values of the low frequency subcarriers at the output of the FFT may overflow the range of the 8-bit signed value, whilst the constellation points of the

high frequency subcarriers may start to merge together. The severity of the above-mentioned phenomena can be easily understood by examining Fig. 5, where the constellations recorded before channel equalization in the receiver are shown for the 1st, 8th and 15th subcarriers. In such a case, the measured total channel BER is worse than 1.0×10^{-2}.
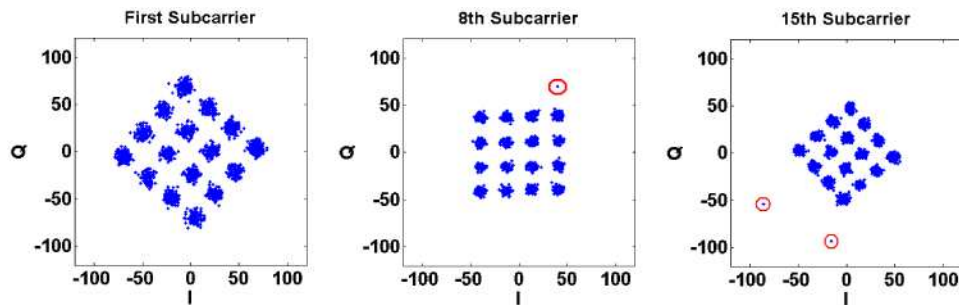

Fig. 6. Constellations of different subcarriers of real-time 6Gb/s 16-QAM-encoded OOFDM signals with the optimised three-level variable power loading scheme after transmitting through a 300m MMF. The measured total channel BER is 3.4×10^{-4}. Spurious constellation points are circled in red.

In sharp contrast, experimental measurements show that the total channel BER can be reduced significantly to a value as low as 3.4×10^{-4} when use is made of a variable power loading scheme, which just consists of three discrete power levels, as seen in Fig. 4. For a specific transmission system, the subcarrier amplitude at each level is adjusted to ensure that similar error bits occur over different subcarriers and the total channel BER is also minimized simultaneously. As shown in Fig. 4, the optimised stair-like subcarrier amplitude distribution in the transmitter brings about a reduced variation in received subcarrier amplitude, and more importantly, an almost uniform distribution of relative error bits over different subcarriers. The resulting constellations recorded prior to channel equalisation (corresponding to a total channel BER of 3.4×10^{-4}) for the 1st, 8th and 15th subcarriers are given in Fig. 6, in which clearly distinguishable constellations are observed. The above analysis indicate that variable power loading is very effective in compensating for the system frequency response roll-off effect, and that the use of a coarse variable power loading scheme with just three power levels is sufficiently accurate for the systems of interest of the present paper.

It is worth mentioning that, experimental investigations are currently being undertaken using adaptive power and bit loading algorithms on each subcarrier to further improve the real-time transceiver performance. Results will be reported elsewhere in due course.

3.2. Transmission performance of 6Gb/s real-time 16-QAM-encoded OOFDM signals with variable power loading

Based on the optimised three-level variable power loading scheme, the fastest ever real-time end-to-end transmission of 6Gb/s 16-QAM-encoded OOFDM signals is achieved experimentally over a 300m OM1 MMF IMDD system involving a DML. Figure 7 shows the corresponding total channel BER performance for both the 300m MMF system and the optical back-to-back configuration.

It is shown in Fig. 7 that, for the case of 300m MMF transmission (optical back-to-back), a minimum BER of 3.4×10^{-4} (3.3×10^{-4}) is obtainable at a received optical power of -7.7dBm (-7.2dBm). At a BER of 1.0×10^{-3} a power penalty of ~0.5dB is observed, mainly resulting from the differential mode delay (DMD) effect [16] and the modal noise effect [17]. In comparison with the performance of real-time 3Gb/s 16-QAM-encoded OOFDM signals over 500m MMFs [11,12], here, the minimum received optical power required for achieving a BER of 1.0×10^{-3} is increased by 5.8dB, and the power penalty is decreased by 1.5dB. The increase in received optical power is because the 6Gb/s OOFDM signals have twice the spectral bandwidths, which are more severely impacted by the system frequency response

roll-off effect, whilst the reduced power penalty arises from the decrease in the DMD effect due to the shorter transmission distance [18].
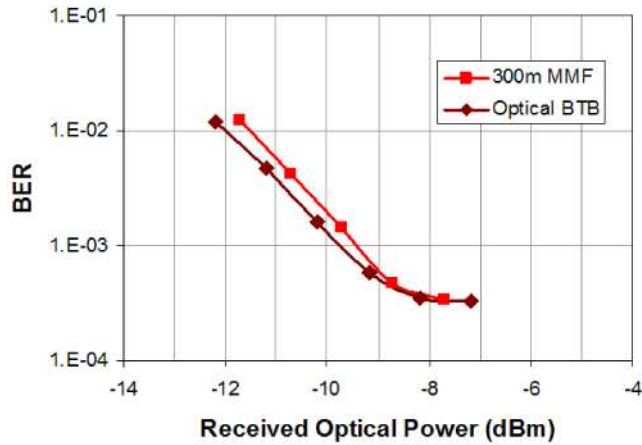

Fig. 7. BER performance of real-time 6Gb/s 16-QAM-encoded OOFDM signal transmission over a 300m MMF and a back-to-back link configuration.
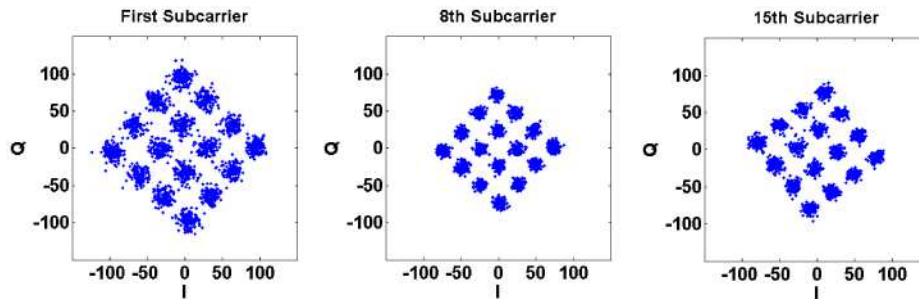
Fig. 8. Optical back-to-back constellations of different 16-QAM-encoded subcarriers before equalisation at a signal bit rate of 6Gb/s and total channel BER of 1×10^{-3}.
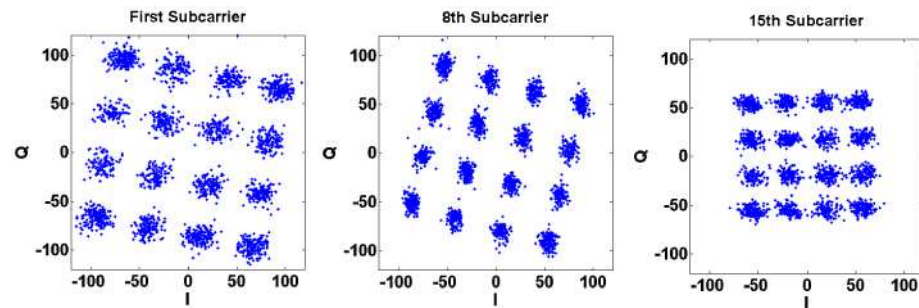
Fig. 9. 300m MMF transmission constellations of different 16-QAM-encoded subcarriers before equalisation at a signal bit rate of 6Gb/s and total channel BER of 1×10^{-3}.

The corresponding received constellations measured before conducting channel equalization at a BER of 1.0×10^{-3} for the 1st, 8th and 15th subcarriers are shown in Fig. 8 and Fig. 9 for the optical back-to-back and 300m MMF cases, respectively. In Fig. 8, the first subcarrier constellations are the worst, this originates mainly from subcarrier beating-induced signal spectral distortions in the vicinity of the optical carrier upon direct detection in the receiver [19].

It is also observed in Fig. 7 that error floors exist for both considered cases. This is mainly due to the existence of spurious constellation points, which are circled in red in Fig. 6. Based on the measured constellations of the subcarriers shown in Fig. 6, a BER of $<3.0 \times 10^{-5}$ is calculated if the red-circled spurious points are removed. These spurious points may arise due to timing irregularities in the ADC interface, as a BER of zero is obtainable in the digital back-to-back configuration, and very similar minimum BERs are observed in the analogue back-to-back configuration compared to the optical back-to-back case. Experimental investigations are currently underway to eliminate these spurious constellation points.

4. Conclusions

Based on a recently proposed pilot subcarrier-assisted channel estimation technique and a simple three-level variable power loading scheme, the fastest ever 6Gb/s real-time FPGA-based OOFDM transceivers have been experimentally demonstrated, for the first time, which have crucial functionalities of on-line performance monitoring and live optimization of key parameters including signal clipping, subcarrier power and DML operating conditions. The developed transceivers use commercially available components with FPGAs for real-time DSP and 4GS/s, 8bit DACs and ADCs. It has been shown that variable power loading is an effective means for compensating for the rapid system frequency response roll-off effect. Real-time end-to-end transmission of a 6Gb/s 16-QAM-encoded OOFDM signal over a 300m OM1 MMF with a power penalty of 0.5dB and a spectral efficiency of 3 bit/s/Hz has been successfully achieved in a DML-based IMDD system.

Acknowledgments

Experimental demonstration of a record high 11.25Gb/s real-time optical OFDM transceiver supporting 25km SMF end-to-end transmission in simple IMDD systems

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Abstract: The fastest ever 11.25Gb/s real-time FPGA-based optical orthogonal frequency division multiplexing (OOFDM) transceivers utilizing 64-QAM encoding/decoding and significantly improved variable power loading are experimentally demonstrated, for the first time, incorporating advanced functionalities of on-line performance monitoring, live system parameter optimization and channel estimation. Real-time end-to-end transmission of an 11.25Gb/s 64-QAM-encoded OOFDM signal with a high electrical spectral efficiency of 5.625bit/s/Hz over 25km of standard and MetroCor single-mode fibres is successfully achieved with respective power penalties of 0.3dB and −0.2dB at a BER of 1.0×10^{-3} in a directly modulated DFB laser-based intensity modulation and direct detection system without in-line optical amplification and chromatic dispersion compensation. The impacts of variable power loading as well as electrical and optical components on the transmission performance of the demonstrated transceivers are experimentally explored in detail. In addition, numerical simulations also show that variable power loading is an extremely effective means of escalating system performance to its maximum potential.

OCIS codes: (060.0060) Fiber optics and optical communications; (060.4080) Modulation; (060.3510) Laser, fiber.

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1. Introduction

With the exponentially increasing end-users' demands for broadband services and the availability of enormous transmission capacities in core networks, the existing access networks have become critical bottlenecks for fully utilising the core network bandwidths to provide end-users with desired services [1]. To address such a challenge, great effort has been expended on exploring various techniques for enabling cost-effective, flexible and "future-proof" next generation passive optical networks (NG-PONs) [2]. Of those techniques, optical orthogonal frequency division multiplexing (OOFDM) [3,4] has attracted extensive research and development interests, since it has a number of inherent and unique advantages including, for example, potential for providing cost-effective technical solutions by fully exploiting the rapid advances in modern digital signal processing (DSP) technology, and considerable reduction in optical network complexity owing to its great resistance to dispersion impairments and efficient utilization of channel spectral characteristics. Apart from the above-mentioned advantages, OOFDM is also capable of offering, in both the frequency and time domains, hybrid dynamic allocation of broad bandwidth among various end-users.

To develop NG-PONs with the desired features, intensity modulation and direct detection (IMDD) OOFDM [5] is a very promising solution, as it is capable of offering further reductions in both the network complexity and the installation and maintenance cost without considerably compromising its flexibility and robustness. In addition, compared to other intensity modulators such as conventional external intensity modulators, directly modulated

DFB lasers (DMLs) are preferable due to their many advantages, including low cost, compactness, low power consumption, relatively low driving voltage and high output power [6].

The experimental demonstration of real-time OOFDM transceivers is vital for enabling the practical realization of the great potential of OOFDM in NG-PONs. The implementation of highly complex, computationally intense and high-speed signal processing algorithms with sufficient precision and the availability of high-speed data converters with a sufficient number of quantization bits are the major challenges in experimentally implementing real-time OOFDM transceivers. It is, however, noted that real-time OOFDM transmitters [7,8] or receivers [9] have been experimentally demonstrated in external modulator-based transmission systems, where off-line DSP approaches are still adopted in the corresponding transceiver counterpart in the systems.

Our first ground-breaking real-time end-to-end OOFDM transceivers incorporating DMLs were demonstrated experimentally in April 2009 [10], since then the transceiver design has very rapidly evolved in several stages with the achieved net signal bit rates being 1.5Gb/s [10], 3Gb/s [11,12], 5.25Gb/s [13] and 6Gb/s [14,15]. The continuation of the momentum has cumulated in the current cutting-edge OOFDM transceiver design, based on which real-time 64-quadrature amplitude modulation (QAM)-encoded end-to-end OOFDM transmission is successfully demonstrated experimentally, for the first time, at a record-breaking raw signal bit rate of 11.25Gb/s and a large electrical spectral efficiency of 5.625bit/s/Hz in simple DML-based IMDD 25km single-mode fibre (SMF) systems.

Here, it is worth highlighting the key aggregated features incorporated in the present advanced OOFDM transceiver design:

- Implemented entirely from commercially available electrical and optical components.

- Completely self-developed logic functions for the core DSP algorithms of inverse fast Fourier transform (IFFT) and FFT. This not only gives full control of system parameters for performance optimisation, but also allows future re-scaling to support even higher signal bit rates, an increased number of subcarriers and other new functionalities.

- Live adjustment of system parameters for live system performance optimisation. These system parameters include:

  - Digital system parameters such as signal clipping level, individual subcarrier amplitude, total digital signal amplitude and symbol alignment.

  - Operating conditions of optical intensity modulators such as DMLs [10–14] and reflective semiconductor optical amplifiers (RSOAs) [15].

  - Analogue electrical RF signal power levels.

- On-line performance monitoring of total channel bit error rate (BER), individual subcarrier BER and system frequency response.

- A pilot subcarrier-assisted channel estimation function with key advantages including, for example, high accuracy, low complexity, small pilot bandwidth usage, excellent stability and buffer-free data flow [11].

- A significantly improved variable power loading technique with independent power control of all subcarriers. This technique provides an extremely simple and effective approach to maximize the transmission capacity to the highest potential by compensating for the effects of system frequency response roll-off and optical nonlinearity.

It should also be pointed out, in particular, that the current transceiver design incorporates a DML in a simple IMDD SMF system without the need for in-line optical amplification and dispersion compensation. In addition, the live parameter optimisation ability of the real-time transceivers demonstrated here is an important feature which, in contrast to the partially real-time systems [7–9], allows the rapid exploration of the optimum system operating conditions to facilitate the realisation of a highly optimised transceiver design.
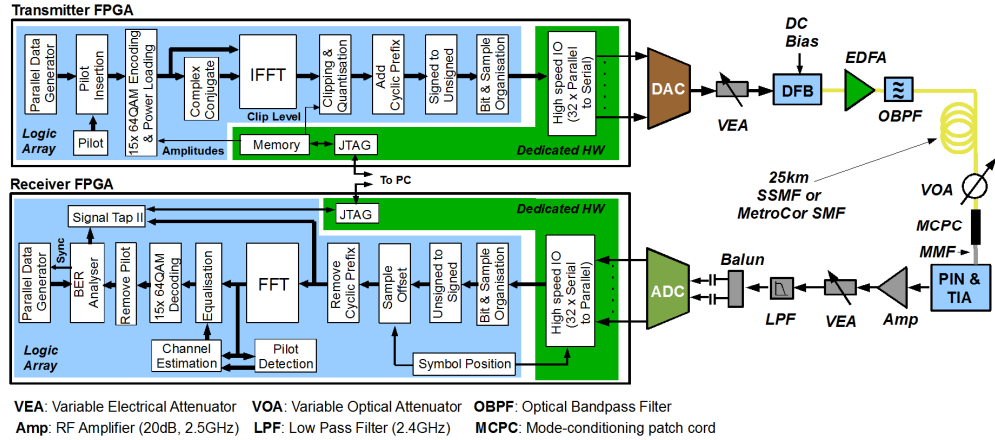

VEA: Variable Electrical Attenuator   **VOA**: Variable Optical Attenuator   **OBPF**: Optical Bandpass Filter
Amp: RF Amplifier (20dB, 2.5GHz)   **LPF**: Low Pass Filter (2.4GHz)   **MCPC**: Mode-conditioning patch cord

Fig. 1. Real-time FPGA-based OOFDM transceiver architectures and experimental system setup.

2. Real-time OOFDM transceiver architecture and experimental system setup

Figure 1 shows the detailed architectures of the real-time OOFDM transmitter and receiver implemented in Altera Stratix II GX FPGAs and the 25km SMF system setup, whose key parameters are listed in Table 1. The transceiver architectures employing real-time DSP for IFFT/FFT algorithms, channel estimation, symbol synchronization, on-line performance monitoring and live parameter optimization, are similar to those reported in [14], except that extensive modifications to the present transceiver design are made in the following three aspects: 1) The subcarrier encoding in the transmitter and decoding in the receiver use 64-QAM modulation; 2) An advanced variable power loading technique in the transmitter is incorporated, which supports, in addition to the live common gain control for all subcarriers, live control of each individual subcarrier amplitude; 3) Analogue noise coupled into the digital-to-analogue converter and analogue-to-digital converter (DAC/ADC) is reduced. As detailed descriptions have already been reported of the real-time transceiver architectures in [14], an outline of the transceiver design and experimental system setup is, therefore, presented below.

In the transmitter, as each subcarrier supports 6 bits per symbol, the design is adapted to provide an 84 bit wide pseudo random data sequence, of length 88,500 words, and a fixed 6 bit wide pilot data pattern, which is combined into the data sequence, to generate 90 bits for each OFDM symbol containing 15 information-bearing subcarriers in the positive frequency bins. The pilot data sequence is employed for pilot subcarrier assisted channel estimation described explicitly in [11]. Similarly, in the receiver, the design is also modified to accommodate the 90 parallel bits per symbol. The BER analyser continuously counts errors every 88,500 symbols, which corresponds to the total test pattern length of 7,965,000 bits in the present transceiver design. In the experiments, the test pattern is continuously repeated and the corresponding error count value is continuously updated, the FPGA's embedded logic analyser displays the error count value on a PC via a JTAG connection which is updated roughly once every second. The error count is observed over a long period of time to ensure that an accurate BER is recorded.

The 8 bit digital OFDM samples are generated by the real-time DSP in the transmitter FPGA at a rate of 4GS/s. Four samples are transferred in parallel by a 32 bit wide bus running at 1GHz to an 8 bit, 4GS/s DAC for conversion to an analogue electrical signal. The analogue electrical signal power level is then optimised by a variable electrical attenuator to directly drive, in combination with an adjustable bias current, a 1550nm DFB laser. The output of the DFB laser biased at an optimum current of 36mA is −4.7dBm, which is boosted to 10dBm by a variable gain erbium doped fibre amplifier (EDFA). The optical signal is then band-pass filtered to minimise ASE noise before being injected, at an optical launch power of 7dBm, into the 25km standard SMF (SSMF) or MetroCor SMF system. It should be noted that the use of the EDFA is to vary only the optical launch power for BER performance measurements.

Table 1. Transceiver and system parameters

Parameter	Value
Total number of IFFT/FFT points	32
Data-carrying subcarriers	15
n-th subcarrier frequency	$n \times 125$MHz
Modulation format on all subcarriers	64-QAM
DAC & ADC sample rate	4GS/s
DAC & ADC resolution	8 bits
Symbol rate	100MHz
Samples per symbol (IFFT)	32 samples (8ns)
Cyclic prefix	8 samples (2ns)
Total samples per symbol	40 samples (10ns)
Error count period	88,500 symbols (7965000bits)
Raw signal bit rate	11.25Gb/s
Net signal bit rate (cyclic prefix 25%)	9Gb/s
DFB laser wavelength	1550nm
DFB laser modulation bandwidth	10GHz
DFB laser bias current	36mA
DFB laser driving voltage	400mVpp
EDFA output power	10dBm
PIN detector bandwidth	12GHz
PIN detector sensitivity	−17dBm [a]
RF amplifier gain (3dB bandwidth)	20dB (2.5GHz)
Low pass filter bandwidth (3dB)	2.4GHz
SSMF dispersion parameter at 1550nm	18ps/(nm·km)
MetroCor dispersion parameter at 1550nm	−7.6 ps/(nm·km)

[a] Corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}

In the receiver, the received optical signal first passes through a variable optical attenuator for the control of the received optical power, and is then coupled into a PIN detector. The electrical output from the PIN is amplified by a fixed 20dB gain RF amplifier plus a variable electrical attenuator to allow the optimisation of the electrical signal power level in preparation for digitisation. The electrical signal is then low-pass filtered and converted to a differential signal before digitisation by an 8 bit, 4GS/s ADC. The digitised samples are then transferred to a receiver FPGA with a bus similar to that adopted in the DAC interface. Finally, the receiver FPGA performs a series of real-time functions as illustrated in Fig. 1, to recover the received data. The most computationally intense function in the receiver, which utilises the majority of the logic resources, is the FFT algorithm. It is also interesting to note that the receiver logic design is currently 82% larger than the transmitter which is mainly due to the channel estimation, symbol alignment and BER measurement functions.

The transmitter and receiver clocks are both generated from a common reference source with the DAC/ADC and FPGAs using a 2GHz and 100MHz clock, respectively. The symbol alignment in the receiver is performed manually following the procedure described in [11–14]. Here it is worth mentioning that, to perform clock information extraction and symbol alignment in the receiver of a real-time OOFDM transmission system, a novel synchronisation technique [16] has been proposed, implemented and experimentally evaluated by our research group. In particular, the proposed synchronisation technique minimizes the sampling clock offset (SCO) effect, which occurs when two independent reference clocks are involved in a single transmission system. The SCO effect may cause the received symbols to be sampled at the non-ideal sampling points, resulting in interference between different subcarriers. Detailed discussions of the operating principle and performance of the synchronisation technique is beyond the scope of the present paper, and will be reported in detail elsewhere in due course.

From the above descriptions, it can be easily derived that, at a symbol rate of 100MHz and a sample rate of 4GS/s, the 64-QAM-encoded OOFDM signal has a record-high raw signal bit rate of 11.25Gb/s and a large electrical spectral efficiency of 5.625bit/s/Hz. As a 25% cyclic prefix (2ns) is utilised here, the net signal bit rate is 9Gb/s. The use of a shorter cyclic prefix (if it can be tolerated) gives a higher net data rate. For example, a 12.5% cyclic prefix (1ns) results in a net signal bit rate of 10.125Gb/s. It should be noted that, for achieving a specific OOFDM transmission capacity, a high electrical spectral efficiency considerably relaxes the requirement on bandwidths of key components such as DACs/ADCs and DMLs.

3. Experimental results

To explore the impairments of different system elements including, digital electrical components, analogue electrical components, optical components and types of fiber on the performance of the developed real-time OOFDM transceivers, in this paper, detailed performance analyses are undertaken for four different system configurations described below with reference to Fig. 1.

- Case I. Digital back-to-back: The digital output of the transmitter FPGA is directly connected to the digital input of the receiver FPGA.

- Case II. Analogue back-to-back: The DAC output in the transmitter is directly connected to the electrical attenuator input in the receiver.

- Case III. Optical back-to-back: The optical band-pass filter output is directly connected to the variable optical attenuator input.

- Case IV. 25km links of SSMF and MetroCor SMF: This represents the entire transmission system.

3.1 Variable power loading scheme

For the aforementioned various system configurations, the associated system frequency responses are shown in Fig. 2, which are measured on-line at the subcarrier frequencies as the effective power loss from the input of the IFFT in the transmitter to the output of the FFT in the receiver and subsequently normalised to the first subcarrier power. The case I system frequency response is not plotted in Fig. 2, since it exhibits, as expected, a flat system frequency response. Very similar to that observed in [14,15], case II has a power roll-off of approximately 8dB from the first to last subcarrier, as shown in Fig. 2. This is a direct result of the on-chip filtering in the DAC and its inherent sin(x)/x response. Whilst case III has a power roll-off of approximately11dB over the same signal spectral region. Compared to case II, the extra 3dB power roll-off in case III is due to the positive transient frequency chirp associated with the employed DML [17]. It is also very interesting to note that, in case IV, the system frequency responses of the 25km SSMF link and the 25km MetroCor link occur at different sides of the case III response, this is because chromatic dispersion of SSMF

(MetroCor SMF) has an identical (opposite) sign compared to that corresponding to the DML transient frequency chirp, thus giving rise to the enhanced (reduced) chromatic dispersion effect [18].
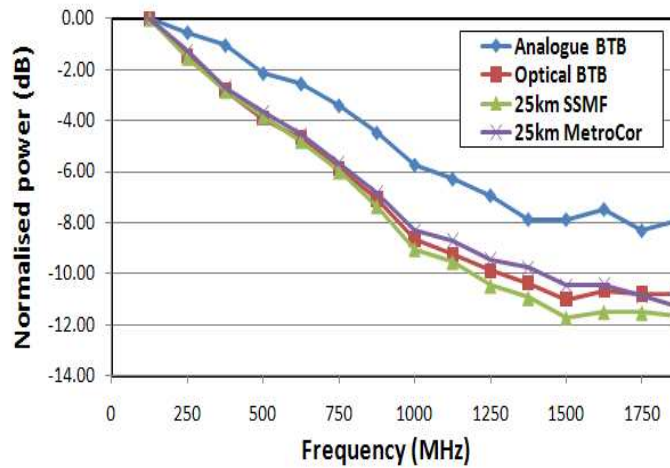

Fig. 2. System frequency responses for various system configurations.

The total 12dB power roll-off in case IV within the signal spectral region observed in Fig. 2 means that, if equal subcarrier power is applied in the transmitter, a large variation in the received subcarrier powers in the receiver will occur, thus leading to an unacceptably high total channel BER. However, by using variable power loading in the transmitter, the system frequency response roll-off effect can be pre-compensated. The effectiveness of such a technique is examined in Fig. 3, where the normalised loaded subcarrier power distribution in the transmitter is presented for the various system configurations, together with the corresponding normalised received subcarrier power distributions in the receiver.

To gain an in-depth understanding of the physical mechanisms underpinning the resulting loaded/received subcarrier power behaviours shown in Fig. 3, discussions are first made of the implementation of the variable power loading technique in the real-time OOFDM transceivers. The encoded electrical signal amplitude at the output of each of the 15 64-QAM encoders has the same peak value, A, to which two independent multiplication operations, denoted here as $\hat{p}_i$ and $\hat{G}_{com}$, are subsequently applied, here $\hat{p}_i$ represents the multiplication by an on-line controlled individual gain factor, P_i, of the i-th subcarrier amplitude; and $\hat{G}_{com}$ represents the multiplication by an on-line controlled common gain factor, G_{com}, of all subcarrier amplitudes. After these two operations, the i-th subcarrier has a peak amplitude of AP_iG_{com}. Clearly, the loaded subcarrier power profile is determined by P_i. The use of the common gain factor, G_{com} is to adjust the amplitudes of all the subcarriers simultaneously to ensure that the 32 complex signal values at the input of the IFFT are set at an optimum level. Generally speaking, for achieving the highest calculation precision, the signal level should be as high as possible. However, if the signal level exceeds a specific threshold, internal IFFT parameters can overflow their assigned ranges. To determine an optimum loaded subcarrier power profile for a given system, the initial step is to use an on-line measured system frequency response to estimate the loaded subcarrier powers required for achieving equal subcarrier powers in the receiver. Making use of such an estimated profile, the BER distribution across all the subcarriers is then measured, based on which the loaded subcarrier power profile can be finely optimised on-line to evenly distribute errors across the subcarriers

and simultaneously minimise the total channel BER. As an example, a representative optimised BER distribution across all the subcarriers is shown in Fig. 4.
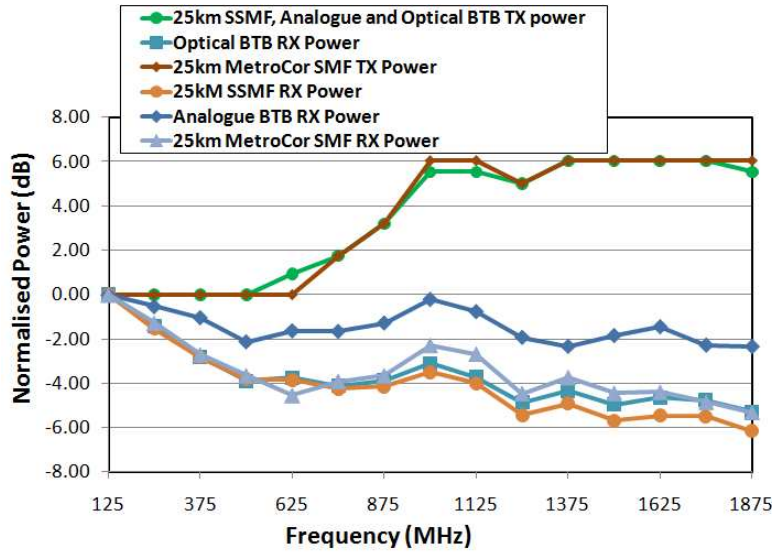

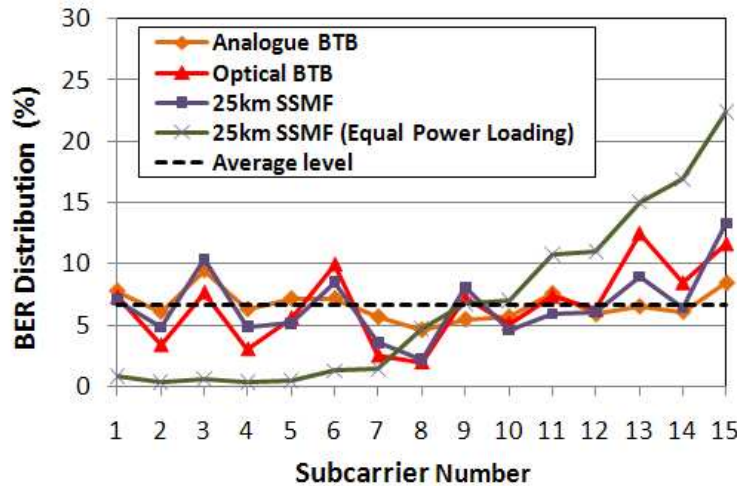Fig. 3. Transmitted and received subcarrier power levels for various system configurations.

Fig. 4. Error distribution across subcarriers for various system configurations when variable power loading is used. For comparisons, the error distribution obtained under equal power loading is also plotted for case IV with a 25km SSMF.

Having described how the variable power loading technique is implemented, attention is then focussed on discussing in detail the loaded and received subcarrier power behaviours observed in Fig. 3. It should be pointed out that, for fair comparisons in Fig. 3, the loaded subcarrier power distributions for case II and III are taken to be similar to that corresponding to case IV, where the loaded subcarrier power profile is optimised for the 25km SSMF. Comparisons between Fig. 3 and Fig. 2 indicate that, for a fixed loaded subcarrier power profile, the difference in the received subcarrier power profiles for the various system configurations considered corresponds to the difference in the corresponding system frequency responses.

In Fig. 3 the loaded (received) subcarrier power profile is seen to have three distinct regions: Region 1 corresponds to the first 4 subcarriers. Over such a region, the loaded subcarrier power level is flat and the received subcarrier power level decays almost linearly. The occurrence of such a power developing trend is due to the effect of direct photon detection-induced unwanted subcarrier intermixing. This effect introduces the strongest spectral distortions to the first subcarrier and relatively weakens for other subcarriers with higher frequencies [19]. This means that the low frequency subcarriers require higher powers to mitigate the effect. Here it is also worth addressing that, for the subcarriers in Region 1, the minimum loaded power level is also determined by the relative quantisation noise, as a reduction in loaded subcarrier power level causes an increase in quantisation noise. The next four subcarriers form Region 2, where the loaded subcarrier power level linearly increases, resulting from the steep decay in the system frequency response. Over such a region, the received subcarrier power level does not vary considerably, suggesting that the subcarrier intermixing effect is negligible. Finally, all the remaining subcarriers are located in Region 3, over which the loaded subcarrier power levels are virtually flat. This is because of two reasons: 1) Region 3 corresponds to a frequency range where the system frequency response roll-off is less steep, and 2) The maximum loaded subcarrier power level is determined by the dynamic power range of the IFFT.

It can also be seen in Fig. 3 that, for the received subcarrier power profiles in all the system configurations, there exist distinguishable subcarrier power peaks centred at the middle subcarriers. This can be explained by considering the effect of imperfect subcarrier orthogonality-induced inter-channel interference (ICI) [20]. Imperfect orthogonality between different subcarriers within a symbol arises due to the quasi-periodic structure of time domain OFDM symbols. The accumulation of the ICI effect brings about the strongest spectral distortions occurring over the middle subcarriers.

From the above analysis, it is clear that, for an optimum loaded subcarrier power profile, there still exists a residual roll-off in the received subcarrier power levels, as shown in Fig. 3. However, such a residual roll-off can be tolerated. This is confirmed in Fig. 4, in which the distribution of errors across the subcarriers is plotted for case II, III and IV with a 25km SSMF. The variable power loading technique can successfully achieve an acceptable total channel BER as shown in Section 3.3, with the residual received subcarrier power roll-off as large as ~6dB (corresponding to a 12dB variation in frequency response) to give a resulting error distribution that varies by just ± 5% from the average level as shown in Fig. 4. In comparison, when equal power loading is employed for case IV with a 25km SSMF, the error distribution increases rapidly for higher subcarrier frequencies, as shown in Fig. 4, and the corresponding total channel BER is increased to an unacceptable level of 8×10^{-3}.

3.2 Dependence of optimum clipping ratio on variable power loading profile

The discussions in Section 3.1 indicate that, variable power loading is capable of offering, in an adaptive manner, an optimally loaded subcarrier power profile for a specific system frequency response. This raises a very interesting open question, i.e., whether or not a variation in the loaded subcarrier power profile also alters the signal clipping characteristics. The provision of an answer to the open question is crucial, as the transmission performance of high signal modulation format-encoded OOFDM signals is very sensitive to signal clipping [13,21,22].

The signal samples at the output of the IFFT prior to clipping are signed 12 bit values, which cover the range from −2048 to 2047. The level at which the signal is clipped, C, can thus be set to a value between 0 and 2047. If the unclipped signal is $S(t)$, the clipped signal $S_{clip}(t)$ is given by

$$S_{clip}(t) = \begin{cases} S(t), & -C \leq S(t) \leq C \\ C, & S(t) > C \\ -C, & S(t) < -C \end{cases} \tag{1}$$
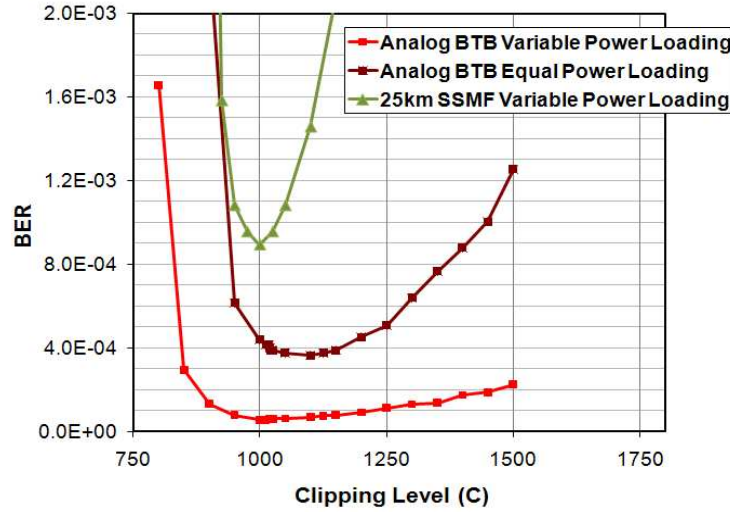

Fig. 5. Variation of BER with clipping level for an analogue back-to-back configuration (case II) and a 25km SSMF link (case IV).

Within the dynamic amplitude range of [-C,C], the clipped signal is then quantised to cover the signed 8 bit range from -128 to $+127$. The general definition of clipping ratio ξ in dB has a form of [21]

$$\xi(dB) = 10\log_{10}\left[\frac{\Lambda}{P_m}\right] \tag{2}$$

where Λ is the maximum peak power of the clipped signal and P_m is the average signal power. To include the digital system parameters relevant to variable power loading in the ξ definition, Eq. (2) can be re-written in the following form

$$\xi(dB) = 10\log_{10}\frac{C^2}{P_M\left(AG_{com}G_{IFFT}\right)^2\sum_{i=1}^{15}P_i^2} \tag{3}$$

where P_M is the average power of the M modulation format-encoded signal with unit peak amplitude (in this paper M is 64-QAM), G_{IFFT} is the gain factor representing signal scaling associated with the IFFT function. It can be seen from Eq. (3) that the optimum clipping ratio of a signal is dependent on the joint effect of the on-line variable parameters, which include the clipping level C, the common gain factor G_{com} and the individual subcarrier gain factors P_i.

For fixed G_{com}, and G_{IFFT}, as well as the loaded subcarrier power profile optimised for the 25km SSMF link shown in Fig. 3, the measured BER against clipping level C for case II and case IV is presented in Fig. 5 under the condition of variable power loading and also equal power loading for case II. The BER variation with C for the 25km SSMF link with equal power loading is not plotted, as the minimum BER is above an acceptable level. Figure 5 shows that, for case II with equal power loading, the optimum clipping level is 1100, which,

however, decreases to 1000 when variable power loading is adopted. These two optimum clipping levels of 1100 and 1000 correspond to signal clipping ratios of 12.2dB and 12.7dB, respectively, measured at the DAC output. This reveals that the optimum clipping ratio is dependent on the loaded subcarrier power profile and there is a significant variation in the clipping level C required to achieve the optimum clipping ratios.

Table 2. 11.25Gb/s real-time OOFDM transceiver performance

Configuration	Minimum BER	Received optical power at BER $= 1.0 \times 10^{-3}$
Digital back-to-back CASE	0	-
Analogue back-to-back	6.0×10^{-5}	-
Optical back-to-back	8.0×10^{-4}	-6.3dBm
25km SSMF link	8.50×10^{-4}	-6.0dBm
25km MetroCor link	8.80×10^{-4}	-6.5dBm

For case IV with the 25km SSMF link, Fig. 5 shows that the optimum value of C is the same as for case II. However, the BER in case IV is more sensitive to C. This is because the optical signal also experiences additional optical noise and distortions, which make the optical signal less tolerant to both the increasing clipping distortion as C decreases below the optimum value and the increased quantisation noise as C increases above the optimum value. Experimental measurements also show that the optimum C value for case III and case IV with the MetroCor SMF is the same as for case IV with the SSMF link and case II, provided that the same loaded subcarrier power profile and G_{com} value are utilised.

3.3 Transmission performance of real-time 11.25Gb/s 64-QAM-encoded OOFDM signals

Making use of the optimum loaded subcarrier power profile and the corresponding optimum clipping setting, experimental measurements are undertaken of the transmission performance of 11.25Gb/s real-time 64-QAM-encoded OOFDM signals over DML-based IMDD systems without in-line optical amplification and dispersion compensation. In the experimental measurements, the 25km links of SSMF and MetroCor SMF are employed. For case III and case IV, the measured BER against received optical power is shown in Fig. 6. In obtaining Fig. 6, the electrical gain at the receiver is adjusted as the received optical power setting varies to maintain the electrical signal amplitude at the ADC input at an optimum level. The minimum achieved BERs and the corresponding received optical powers at a BER of 1×10^{-3} are summarized in Table 2 for the different cases considered here.

For case III, the transmission performance of real-time OOFDM signals is mainly limited by additive white Gaussian noise (AWGN). Over such a channel, by comparing the transmission performance of the present 64-QAM-encoded OOFDM signal with that corresponding to the 16-QAM-encoded signal having the same spectral bandwidth [14], it can be found that, 64-QAM modulation increases the minimum received optical power required for achieving a BER of 1.0×10^{-3} by approximately 4dB. Such an optical power increase is well in line with the theoretical prediction [21]. In addition, as shown in Fig. 6, the measured power penalty at a BER of 1×10^{-3} for the 25km SSMF is 0.3dB, whilst the power penalty for the 25km MetroCor SMF reduces to -0.2dB. The observation of negative power penalty is also in excellent agreement with the results obtained for the 3Gb/s real-time 16-QAM-encoded real-time OOFDM transceiver design, where a negative power penalty of -0.6dB was measured for a 25km MetroCor SMF [11]. Furthermore, our numerical simulations have also verified the occurrence of positive and negative power penalties, depending upon the use of SSMFs and MetroCor SMFs, respectively, in the DML-based IMDD transmission systems. The physical origin of the observed power penalty characteristics is mainly attributed to the following two reasons: 1) the fibre chromatic dispersion-induced OOFDM phase shift cannot

be preserved perfectly in the electrical domain owing to direct photon detection in the receiver. A MetroCor (SSMF) fibre has a negative (positive) dispersion parameter, which can compensate (enhance) the positive transient frequency chirp effect associated with the DML, thus leading to a reduced (enlarged) total phase shift of the received signal in the electrical domain; 2) the reduced (enlarged) phase shift also decreases (increases) the subcarrier intermixing effect upon direct detection.
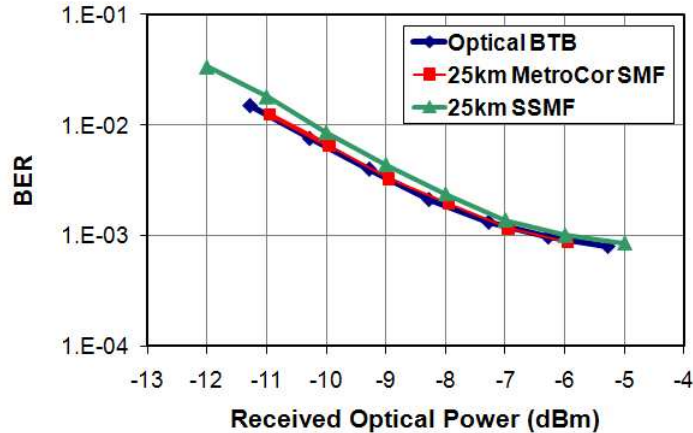

Fig. 6. BER performance of real-time 11.25Gb/s 64-QAM-encoded OOFDM signal transmission over 25km SSMF, 25km MetroCor SMF and optical back-to-back link configurations.

To explore the factors limiting the minimum achievable BERs shown in Fig. 6, representative constellations of single subcarriers, recorded prior to performing equalization in the receiver, are presented in Fig. 7 for the various system configurations. Case I gives a zero BER as listed in Table 2, and the corresponding constellation presented in Fig. 7(a) shows very little deviation from the ideal case. Whilst in case II, the minimum BER increases to 6×10^{-5}, and the corresponding constellation plotted in Fig. 7(b) shows an increase in noise and distortion due to the non-ideal sampling, analogue noise and frequency response roll-off of the DAC and ADC. In case III the minimum BER increases approximately by one order of magnitude to 8.0×10^{-4}, and the corresponding constellation of the first subcarrier in Fig. 7(c) shows a significant increase in the noise content. Moreover, for case IV with two types of SMFs being employed, as seen in Fig. 6 and Table 2, the minimum BERs are very similar to that obtained in case III. Figure 7(d)–7(f) show the constellations for the 1st, 8th and 15th subcarriers for the 25km SSMF link, and Fig. 7(g)–7(i) show similar constellations for the 25km MetroCor SMF link. Comparing Fig. 7(d) and Fig. 7(g) with Fig. 7(c) indicates clearly that there is little increase in the noise content. The received constellations for the SMF fibers in Fig. 7(d)–7(i) also clearly show the residual roll-off in subcarrier amplitude with increasing subcarrier frequency.

All the aforementioned facts indicate that, in addition to the analog electrical component-induced signal distortions, DML-induced signal waveform distortions and subcarrier intermixing upon direct photon detection in the receiver are major factors limiting the minimum achievable total channel BER. To confirm the above statement, numerical simulations are performed. It is shown that, based on numerical parameters identical to those adopted in the experimental system, the simulated minimum BERs agree very well with the experimental results. However, when the DML is replaced by an ideal intensity modulator with the DML-induced positive transient frequency chirp being included, a minimum BER as low as 6.0×10^{-5} is obtainable. On the other hand, a reduction in the subcarrier intermixing

effect by padding zeros at all the subcarriers between subcarrier 1 and subcarrier 7, can lower the minimum total BER to $<1.0 \times 10^{-4}$ for subcarriers 8 to 15 in the present DML-based IMDD experimental system. The simulation results indicate that further system optimization can still be made to provide a large BER margin for practical system implementation.
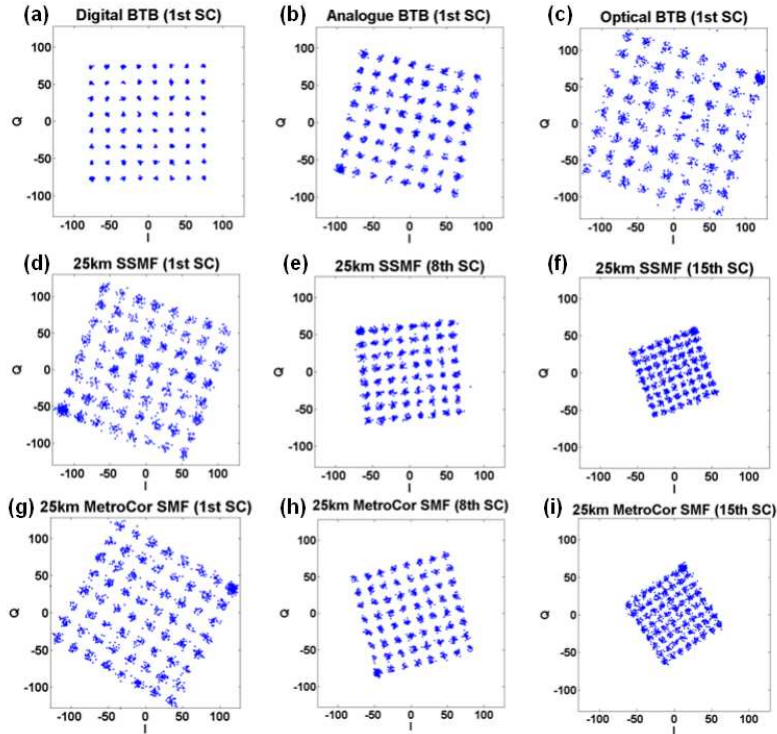

Fig. 7. Received constellations of a single subcarrier before equalisation (a) Digital back-to-back, total channel BER = 0 (b) Analogue back-to-back, total channel BER = 6.0×10^{-5} (c) Optical back-to-back, total channel BER = 8.0×10^{-4} (d,e,f) 25km SSMF, total channel BER = 8.5×10^{-4},(g,h,i) 25km MetroCor SMF, total channel BER = 8.8×10^{-4}.

4. Effectiveness of variable power loading

From previous discussions, it is clear that variable power loading is essential to allow the successful demonstration of the 11.25Gb/s real-time 64-QAM-encoded OOFDM transceivers. In this section, numerical simulations are undertaken to explore the feasibility of using variable power loading to maximize the OOFDM signal transmission capacity. To conduct such explorations, comparisons are made between three widely used algorithms outlined below:

1) Variable power loading: As already demonstrated experimentally, a fixed signal modulation format (64-QAM in this paper) is taken on all the subcarriers and the individual subcarrier powers are optimised according to the system frequency response.

2) Variable bit loading: The modulation format on each subcarrier is varied whilst maintaining the same fixed mean power level on all subcarriers. This is also known as adaptive modulation [19–22]. Generally speaking, a high (low) modulation format is used on a subcarrier suffering a low (high) power roll-off.

3) Combined variable power and bit loading: Both the modulation format and power are varied on all subcarriers, utilising a procedure reported in [23].

For fair comparisons between these three algorithms, it is worth highlighting the following three aspects: a) for a given transmission system, the total electrical signal powers generated by all the algorithms are set to be identical, and comparisons of maximum achievable transmission capacity at a BER of 1.0×10^{-3} are made; b) In executing algorithms 2) and 3), the signal modulation format taken on each subcarrier varies from differential binary phase shift keying (DBPSK), differential quadrature phase shift keying (DQPSK), 8-QAM to 256-QAM, and c) Any subcarrier suffering a very high transmission loss may be dropped completely if the following condition is met: for algorithm 1 only, errors are too large to achieve the required total channel BER; for algorithms 2) and 3), errors are too large to achieve the required total channel BER even when the lowest modulation format is employed.
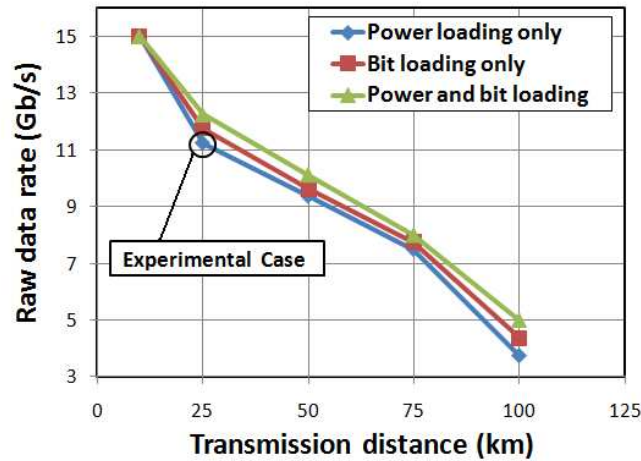

Fig. 8. Raw signal line rate versus reach for power loading, bit loading and power & bit loading. SSMFs are considered.

A comprehensive theoretical OOFDM system model developed in [20] is adopted, which includes OOFDM transceivers, DMLs, SMFs and square-law photon detectors. All the device and system parameters used in the numerical simulations are identical to those adopted in the present experiments, and all other parameters that are not made known in the experiments are taken from [20].

For IMDD SSMF systems, the simulated signal capacity versus reach performance is shown in Fig. 8 for the three algorithms. It can be seen from Fig. 8 that the three algorithms can support almost identical signal capacities for SSMF links of up to 100km. In particular, at 25km SSMF transmission, variable power loading can achieve 11.25Gb/s compared to 12.25Gb/s supported by combined power and bit loading. Numerical simulations are also performed for MetroCor SMFs and a transmission performance very similar (<1% deviation) to that observed in Fig. 8 is obtained.

Variable power loading is very simple and easy to implement in real-time OOFDM transceivers, whist the other two algorithms require extremely sophisticated designs to accommodate variations in both the number of bits per symbol and the selective modulation formats. Therefore, variable power loading is a cost-effective approach for optimising OOFDM transceiver performance to its maximum potential.

5. Conclusions

The fastest ever 11.25Gb/s real-time FPGA-based OOFDM transceivers utilizing 64-QAM encoding/decoding and significantly improved variable power loading on each individual

subcarrier have been experimentally demonstrated, for the first time, incorporating advanced functionalities of on-line performance monitoring, live system parameter optimization and automatic channel estimation. The implemented transceivers are constructed entirely from off-the-shelf electrical and optical components. Real-time end-to-end transmission of an 11.25Gb/s 64-QAM-encoded OOFDM signal with a high electrical spectral efficiency of 5.625bit/s/Hz over 25km of standard and MetroCor SMFs has been successfully achieved with respective power penalties of 0.3dB and -0.2dB at a BER of 1.0×10^{-3} in a DML-based IMDD system without in-line optical amplification and chromatic dispersion compensation. The impacts of variable power loading as well as electrical and optical components on the transmission performance of the implemented transceivers have been experimentally explored in detail. In addition, numerical simulations have also shown that variable power loading is capable of maximizing the system performance to its fullest potential. By successfully breaking through the 10Gb/s barrier, this work indicates that OOFDM can be justified as a viable and practical physical layer solution for NG-PONs.

Active research activities are currently being undertaken in our research group to implement combined variable power and bit loading in real-time OOFDM transceivers to verify the theoretical predictions. In addition, to further reduce the transceiver cost, investigations are also being conducted of utilizing very cheap optical intensity modulators such as vertical cavity surface emitting lasers (VCSELs) and reflective semiconductor optical amplifiers (RSOAs) in real-time OOFDM transceivers.

Acknowledgments

Experimental Demonstration of Real-Time Optical OFDM Transmission at 7.5 Gb/s Over 25-km SSMF Using a 1-GHz RSOA

R. P. Giddings, E. Hugues-Salas, X. Q. Jin, J. L. Wei, and J. M. Tang

Abstract—The 7.5-Gb/s real-time end-to-end optical orthogonal frequency-division-multiplexing (OOFDM) transceivers incorporating variable power loading on each individual subcarrier are demonstrated experimentally using a live-optimized reflective semiconductor optical amplifier intensity modulator having a modulation bandwidth as narrow as 1 GHz. Real-time OOFDM signal transmission at 7.5 Gb/s over 25-km standard single-mode fiber is achieved across the C-band in simple intensity modulation and direct detection systems without in-line optical amplification and dispersion compensation.

Index Terms—Optical fiber communication, optical modulation, orthogonal frequency-division multiplexing (OFDM), semiconductor optical amplifiers (SOAs).

I. INTRODUCTION

WAVELENGTH-DIVISION-MULTIPLEXED passive optical networks (WDM-PONs) have widely been considered as one of the most promising strategies for satisfying the exponentially increasing end-users' demands for broadband services. For widespread deployment of WDM-PONs, the most critical challenges are cost-effectiveness and flexibility. To achieve cost-effective WDM-PONs, the employment of reflective semiconductor optical amplifiers (RSOAs) in optical network units (ONUs) has been extensively investigated [1], since RSOAs have salient advantages including simultaneous signal modulation and optical amplification, provision of centralized colorless wavelength management and bidirectional transmission support. On the other hand, to enhance the flexibility of WDM-PONs and maintain their compatibility with existing time-division-multiplexed (TDM) PONs, optical orthogonal frequency-division multiplexing (OOFDM) has been considered as one of the strongest contenders for practical applications, since OOFDM has inherent and unique advantages including dynamic provision of hybrid bandwidth allocation

in both the frequency and time domains, significant reduction in network complexity, and potential for cost-effective implementation [2]. In practice, for a given WDM channel, the aforementioned compatibility can be achieved by mapping data from different synchronized TDM end-users onto different OFDM subcarriers [2]. Therefore, it is greatly beneficial if use is made of OOFDM transceivers incorporating RSOAs as intensity modulators in intensity modulation and direct detection (IMDD) standard single-mode fiber (SSMF)-based transmission systems for WDM-PONs. To address such an interesting topic, excellent experimental results have been reported [3], which are, however, obtained utilizing off-line digital signal processing (DSP) approaches without live RSOA operating condition optimization.

Recently, we have made a significant breakthrough in experimentally demonstrating a series of world-first real-time 10-GHz directly modulated distributed-feedback (DFB) laser-based OOFDM transceivers with the latest record-breaking net signal bit rates of 6 Gb/s [4]. More recently, we have also reported, for the first time, the experimental demonstration of 7.5-Gb/s real-time OOFDM transceivers incorporating an RSOA intensity modulator (RSOA-IM) with a modulation bandwidth as narrow as 1.125 GHz [5].

In this letter, we report the significantly improved performance of RSOA-IM-based real-time OOFDM transceivers with on-line performance monitoring and live parameter optimization in simple IMDD SSMF systems. Compared to [5], for all the wavelengths considered, minimum bit-error rates (BERs) presented here are reduced by a factor of >10, which is also simultaneously accompanied with a >3-dB reduction in minimum optical launch power required at a BER of 1×10^{-3}. Such improvements are due to further transceiver optimizations in the following two aspects: 1) The current design can provide a higher electrical OFDM driving current, which can effectively minimize the RSOA-IM-induced nonlinear effects [6]. 2) The analog electrical noise associated with digital-to-analog converters (DACs) is reduced, practically eliminating the spurious constellation points observed in [5]. In addition, live control of total digital signal power, signal clipping level, and digital amplitude of individual subcarriers (referred to as variable power loading) are still utilized to compensate for the system frequency response roll-off effect [4], [5]. Such transceiver optimization will result in a highly optimized transceiver design with the ability to optimize link-dependent parameters, such as variable power loading profile, upon link establishment and provide performance robustness to constantly changing environments.
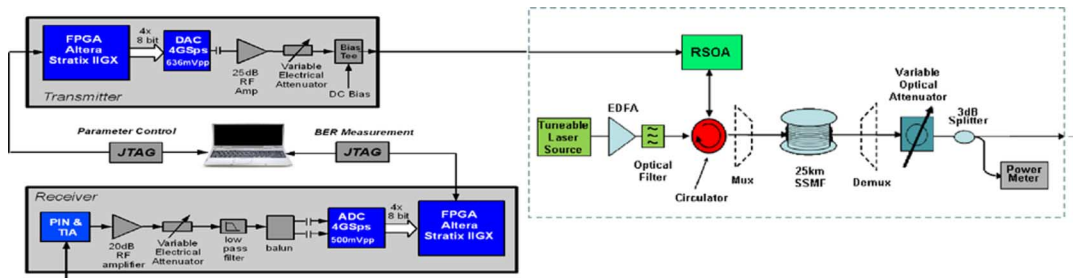
Fig. 1. Experimental system setup for real-time OOFDM transmission using an RSOA (CIP SOA-RL-OEC-1550) as an intensity modulator.

II. REAL-TIME EXPERIMENTAL SYSTEM SETUP

Fig. 1 shows the real-time experimental system setup. The field-programmable gate array (FPGA)-based OOFDM transceiver architecture employing real-time DSP for inverse fast Fourier transform (IFFT) and FFT algorithms, channel estimation, symbol synchronization, BER measurement, on-line performance monitoring, and live parameter optimization, are similar to those reported in [5], where an RSOA is employed as an intensity modulator and the amplitude of each subcarrier is independently adjustable on-line. Here 32 subcarriers are employed with 15 conveying data. An 8-sample cyclic prefix is added to the 32 samples clipped with a clipping ratio of 14.5 dB, giving 40 samples per symbol. The internal system clock is set to 100 MHz and the parallel signal processing approach results in a 100-MHz symbol rate. The 8-bit DAC operates at 4 GS/s, producing a 2-GHz signal bandwidth. Sixteen-QAM is taken on all the 15 information-bearing subcarriers. The OOFDM transceiver with the aforementioned parameters produces a raw signal bit rate of 7.5 Gb/s, of which 6 Gb/s is used to carry user data due to the selected cyclic prefix length of 2 ns.

As shown in Fig. 1, at the transmitter, after passing through an erbium-doped fiber amplifier followed by an 0.8-nm optical filter for adjustment of continuous-wave (CW) optical powers, and an optical circulator with 1.4-dB insertion loss, a CW optical wave supplied by a tunable laser source is injected, at an optical power of 5 dBm, into a polarization-insensitive RSOA with an electrical 3-dB modulation bandwidth of 1.125 GHz. The 2-GHz 3.4-Vpp electrical analog OFDM signal and a 77-mA dc bias current are combined in a 6-GHz bias tee and then modulate the CW optical wave in the RSOA operating at a temperature of 13 °C. The modulated real-time OOFDM signal is transmitted through a 25-km SSMF, in which optical multiplexer and demultiplexer may be inserted for WDM-PONs. The received optical signal passes through a variable optical attenuator and a 3-dB coupler, a 12-GHz p-i-n photodetector with a receiver sensitivity of −17 dBm is employed to convert the received OOFDM signal into the electrical domain for digitization by an 8-bit 4-GS/s analog-to-digital converter (ADC), a second FPGA then performs real-time DSP [4]. The optical system is free from in-line optical amplification and chromatic dispersion compensation. The above-mentioned RSOA driving and bias currents, temperature and 5-dBm CW optical power are fixed for different optical wavelengths within the C-band.

III. EXPERIMENTAL RESULTS

The measured frequency responses normalized to the first subcarrier are plotted in Fig. 2(a) for different scenarios: 1) an
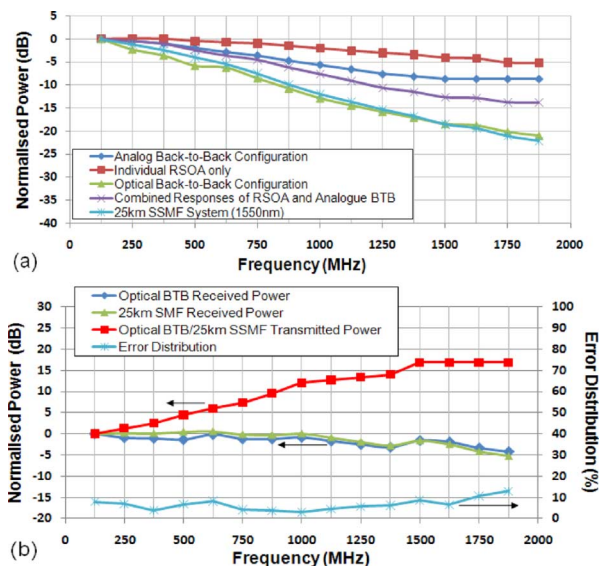

Fig. 2. (a) Frequency responses for different cases. (b) Normalized transmitted and received subcarrier powers and error distribution for optical back-to-back and 25-km SSMF configurations. The optical systems operate at wavelengths of 1550 nm.

individual RSOA; 2) an electrical analog back-to-back configuration, whose frequency response decay is mainly caused by the DAC; 3) mathematically added responses of the RSOA and the analog back-to-back; 4) an optical back-to-back configuration; and finally 5) an entire 25-km SSMF system. For Cases 2–5, the frequency responses are measured from the IFFT input in the transmitter to the FFT output in the receiver. It can be seen from Fig. 2(a) that the 25-km system frequency response decay within the signal spectral region is approximately 22 dB, which is 4 dB smaller than that reported in [5] due to the RSOA operating condition optimization. Comparisons between different curves imply that such a rapid roll-off is mainly attributed to the following three factors: 1) the DAC due to its output filtering and inherent $\sin(x)/x$ response; 2) the RSOA due to its narrow modulation bandwidth; and most importantly, 3) the signal spectral distortion due to the dynamic RSOA frequency chirp effect [6] (difference between Case 3 and Case 4). Based on the above analysis, it is easy to understand that, when equal subcarrier powers are considered, the complex values of the low-frequency subcarriers may overflow the dynamic output range of the FFT, while the constellation points of the high-frequency subcarriers may be severely merged. This results in an unacceptably high total channel BER.

For the optical back-to-back and 25-km SSMF transmission cases, the implementation and effectiveness of the variable power loading technique are explored in Fig. 2(b), where the
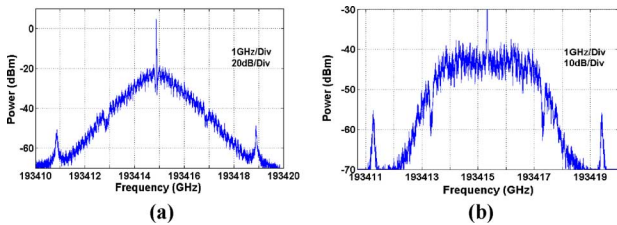
Fig. 3. Real-time OOFDM signal spectrum at RSOA output. (a) With equal power loading; (b) with variable power loading. (Measured using Apex Technologies OSA AP2440A, 20-MHz resolution.)

variable power-loaded subcarrier power in the transmitter and the received subcarrier power prior to channel equalization in the receiver, all normalized to the first subcarrier, are plotted against subcarrier frequency, together with the resulting subcarrier BER distribution for 25-km SSMF. In obtaining Fig. 2(b), the digital subcarrier amplitude of each subcarrier in the transmitter is finely adjusted to ensure that an almost uniform BER distribution (<10% variation) occurs over all the subcarriers and the total channel BER is also minimized simultaneously. Compared with Fig. 2(a), Fig. 2(b) indicates that, as expected, the system frequency response decay induced by the DAC, individual RSOA frequency response, and the RSOA frequency chirp-induced dynamic spectral distortions can be compensated sufficiently by the variable power loading technique. The effectiveness of variable power loading is also confirmed in Fig. 3, where a sharp decay (flat top) OOFDM signal spectral at the RSOA-IM output for the cases of excluding (including) variable power loading are observed in Fig. 3(a) [Fig. 3(b)]. Here it is worth mentioning the following two facts: 1) A further increase in the relative amplitude of the high-frequency subcarriers causes the low-frequency subcarriers to experience higher small-amplitude-induced quantization noise effect; 2) for the current transceiver design, the maximum variation in the relative subcarrier power levels is mainly determined by the dynamic range of the IFFT.

Based on the optimized subcarrier amplitude distribution, the BER performance of the real-time 7.5-Gb/s OOFDM signals over 25-km SSMF is shown in Fig. 4(a) for different wavelengths. The corresponding constellations at 1550 nm recorded prior to performing channel equalization in the receiver for representative subcarriers are also presented in Fig. 4(b)–(d) for the optical back-to-back case, and in Fig. 4(e)–(g) for the 25-km SSMF transmission case. Fig. 4(a) shows that, for all the wavelengths across the C-band, BERs of $< 9.0 \times 10^{-5}$ and power penalties of <0.5 dB are achieved. In addition, in comparison with [5], for all the wavelengths considered, Fig. 4(a) also shows a >3-dB reduction in minimum received optical power required at a BER of 1×10^{-3}. These results indicate that the real-time RSOA-IM-based transceivers are capable of supporting colorless operation. The wavelength-dependent minimum received optical power at a BER of 1×10^{-3}, as shown in Fig. 4(a), originates mainly from the wavelength-induced variation in extinction ratio of the RSOA modulated signals [6]. In Fig. 2(a), Cases 4 and 5 have similar frequency responses, which, however, correspond to different BER performance, as seen in Fig. 4(a). This is attributed to the long transmission distance-enhanced subcarrier intermixing effect occurring upon photodetection [6]. The effects of subcarrier intermixing and RSOA-induced small
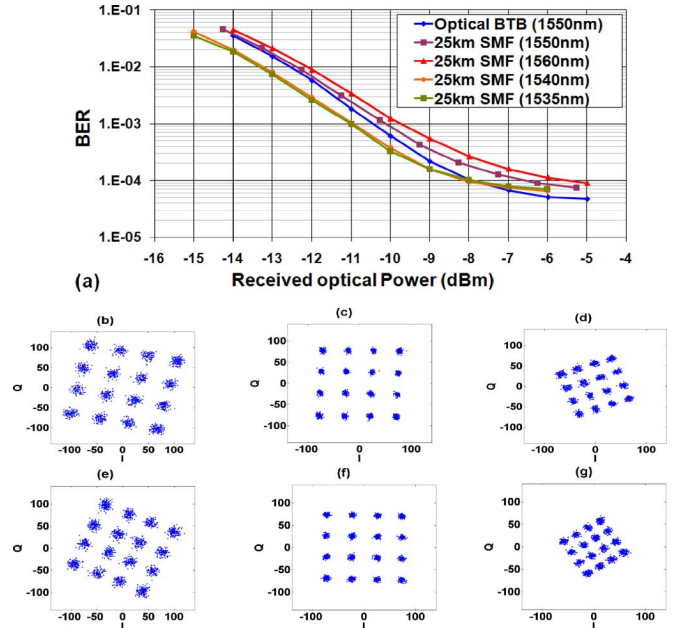

Fig. 4. (a) BER performance for optical back-to-back configuration and transmission over a 25-km SSMF for different wavelengths. Various received constellations of different subcarriers before channel equalization for optical BTB (b)–(d) and after 25-km SSMF transmission (e)–(g). (a), (b) 1st subcarrier. (c) 8th subcarrier. (d) 15th subcarrier. (e) 1st subcarrier. (f) 8th subcarrier. (g) 15th subcarrier.

signal extinction ratio limit the minimum achievable BERs observed in Fig. 4(a).

IV. CONCLUSION

The experimentally demonstrated real-time OOFDM transmission at 7.5 Gb/s over 25-km SSMF across the C-band has potential applications in cost-effective colorless ONUs for WDM-PONs. Our recent theoretical investigations also show that, without considering all limitations imposed by the adopted electrical and optical components, the current OOFDM transceivers at 4 GS/s, using the present RSOA under high optical gain saturation, are capable of supporting a maximum of 12.5-Gb/s OOFDM transmission over 25-km SSMF.

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Experimental Demonstration of Real-Time Optical OFDM Transmission at 11.25 Gb/s Over 500-m MMFs Employing Directly Modulated DFB Lasers

R. P. Giddings, E. Hugues-Salas, Benoit Charbonnier, and J. M. Tang

Abstract—The fastest ever 11.25-Gb/s real-time end-to-end optical orthogonal frequency-division-multiplexing (OOFDM) transmission over 500-m multimode fibers (MMFs) with a high electrical spectral efficiency of 5.625 bit/s/Hz is experimentally demonstrated, for the first time, in a simple intensity modulation and direct detection (IMDD) system employing a directly modulated distributed-feedback (DFB) laser. An optical power budget as high as 12 dB is achieved with a minimum received optical power of -6.3 dBm for a total channel bit-error rate of 1×10^{-3}. The field programmable gate array (FPGA)-based OOFDM transceivers also have functionalities including variable power loading, performance monitoring, and on-line parameter adjustment.

Index Terms—Optical fiber communication, optical modulation, orthogonal frequency-division multiplexing (OFDM).

I. INTRODUCTION

RECENT years have seen an exponentially growing demand for higher transmission bandwidths in local area networks (LANs). A vast majority of the existing LANs are based on multimode fibers (MMFs) [1]. The cost of upgrading the installed MMF-based LANs from today's typical 1 Gb/s to $>$ 10 Gb/s can be drastically reduced if a high-speed single wavelength transmission technique is realized, which is compatible with legacy MMFs. It is also greatly advantageous if the technique also has essential features including cost-effectiveness, low power consumption, compactness and insusceptibility to the variation in launch conditions. Based on coarse wavelength division multiplexing (WDM) (receiver sided electronic dispersion compensation), the 10GBASE-LX4 (10GBASE-LRM) technology has demonstrated the ability to utilize legacy MMFs for the initial migration to 10 Gb/s transmission over 300 m (up to 220 m).

To further extend the signal bit rate and/or reach of MMF systems, there is extensive ongoing research into alternative techniques such as mode-field matched center launch [2] and spatial light modulation [3]. These techniques are, however, strongly system-dependent, and significant technical challenges still remain to be solved before they are viable for future mass deployment.

Owing to its inherent advantages including excellent resistance to a large amount of differential mode delay (DMD), adaptive and highly efficient utilization of channel spectral characteristics, as well as potential for cost-effective implementation, optical OFDM (OOFDM) is a promising "future-proof" solution that has demonstrated great potential to support > 50 Gb/s over 300 m transmission in 99.5% of already installed legacy MMFs, irrespective of launch conditions and implementation-related impairments [4]. Equally importantly, very recently we have made a significant breakthrough in experimentally demonstrating 11.25 Gb/s end-to-end real-time OOFDM transmission over 25 km standard single-mode fibers (SMFs) in simple intensity-modulation and direct detection (IMDD) systems involving directly modulated DFB lasers (DMLs) [5]. A 12.1 Gb/s real-time OOFDM transmitter [6], a 41.25 Gb/s real-time OOFDM receiver [7] and a real-time coherent receiver [8] have also been experimentally achieved in SMF systems.

In this Letter, the real-time OOFDM transceiver reported in [5] is further improved by including an electrical amplifier in the transmitter to extend the range of the available DML driving current and further optimize the DML operating conditions. As a direct result, compared to [5], for the optical back-to-back case the minimum optical power required for achieving a total channel bit error rate (BER) of 1×10^{-3} is reduced by approximately 3 dB. In addition, the feasibility of implementing the improved DML-based real-time OOFDM transceivers is reported, for the first time, in simple MMF links. Furthermore, the impacts of various MMF system impairments are also vigorously examined on the maximum achievable data rate versus reach performance.

II. REAL-TIME OOFDM TRANSCEIVERS AND EXPERIMENTAL SYSTEM SETUP

Fig. 1 shows the detailed architectures of the real-time OOFDM transmitter and receiver, and the DML-based IMDD link employing a 50/125 μm MMF. Full descriptions of the field programmable gate array (FPGA)-based transceiver architectures and their functionalities can be found in [5].

In the transmitter, pseudo random data is generated as a stream of 84-bit parallel words, which are combined with a fixed 6-bit pilot word used for channel estimation [9]. The combined 90-bit word is mapped onto 15 parallel 64-quadrature amplitude modulation (QAM) encoders, each of which has an
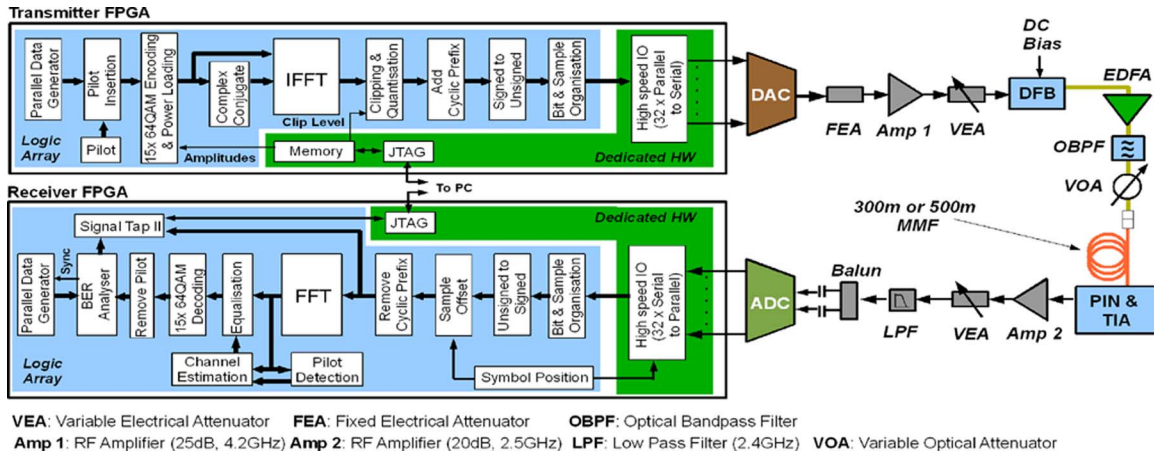
Fig. 1. Real-time FPGA-based OOFDM transceiver architectures and experimental system setup.

independent on-line adjustable gain-factor for variable power loading [5]. To generate only real-valued samples required for IMDD transmission, Hermitian symmetry is applied to the 15 generated complex values (together with a zero-valued component) and their complex conjugate counterparts, next, a self-developed 32-pt inverse fast Fourier transform (IFFT) logic function is applied to transform the 32 frequency-domain sub-carriers to 32 real-valued time-domain samples. Clipping and 8-bit quantization are then performed, followed by insertion of an 8 sample cyclic prefix to form a complete 40-sample OFDM symbol. The real-valued symbol is converted from signed to unsigned and subsequently rearranged for transfer over a 32-bit high-speed interface to a 4 GS/s 8-bit digital-to-analogue converter (DAC). The DAC output is amplified and adjusted by a variable electrical attenuator to produce an optimized driving signal having an amplitude of ~ 640 mVpp. After combining the driving signal with an optimized DC bias current of 38 mA, the combined electrical OFDM signal is employed to directly modulate a 10 GHz bandwidth, 1550 nm DFB laser. Having boosted the optical signal power, a variable optical attenuator is utilized to adjust the optical signal power which has a maximum possible launch power of ~ 2.4 dBm, the optical signal is launched into the MMF link via a commercially available mode conditioning patch cord. It should be noted that the DFB laser linewidth effect is negligible in the IMDD systems for OOFDM signals encoded using signal modulation formats as high as 128-QAM [10].

At the receiver, a 12 GHz, -17 dBm, linear PIN detector with a MMF pigtail directly detects the transmitted optical signal. Prior to digitization by a 4 GS/s 8-bit analogue-to-digital converter (ADC), the converted and amplified electrical signal level is optimized by a variable electrical attenuator, which is followed by a low-pass anti-aliasing filter. As the full Nyquist bandwidth is used with no guard band, the nonideal filtering results in some residual aliasing products being present at the high frequency subcarriers. The digitized samples are transferred to the receiver FPGA over an interface similar to that used by the DAC. Manual symbol synchronization is applied, using the approach reported in [5], [9], to initialize the receiver process. For each received symbol the cyclic prefix is removed before a 32-pt FFT converts the real-valued time-domain symbol into 32 frequency-domain subcarriers from which 15 data-carrying subcarriers are selected. Subsequently, pilot-data detection is performed for channel estimation. Based on the estimated channel transfer function each subcarrier is equalized before data decoding is performed to recover the transmitted data.

Key features of the real-time OOFDM receiver design are on-line monitoring of the total channel BER, the BER of each individual subcarrier, the system frequency response and the BER distribution across the subcarriers. Such on-line monitoring functions are crucial for optimizing not only the subcarrier power loading profile adopted in the transmitter, but also the transceiver operating parameters such as the signal clipping level, the overall radio frequency (RF) signal power and the DFB operating conditions. In addition, the SignalTap II embedded logic analyzer also allows the real-time observation of internal signals in the receiver FPGA such that the aforementioned BERs and system frequency responses can be continuously extracted and viewed. It should be pointed out, in particular, that, when measuring a BER, the errors are counted over 88,500 symbols (7,965,000 bits in total), and the measured errors are continuously updated and displayed. To further improve the accuracy of the BER measurement, for a specific MMF link, a mean value of different readings recorded over a period of several minutes is taken.

The DAC/ADC sampling speed of 4 GS/s and a total 90 bits of data per symbol give rise to a raw data rate of 11.25 Gb/s. The 25% cyclic prefix results in a 9 Gb/s net data rate. If a shorter cyclic prefix can be tolerated, the net data rate can be increased. However, a reduction in cyclic prefix decreases the system tolerance to DMD. An optimum cyclic prefix could be found by redesign of the FPGA-based DSP process for control of cyclic prefix length. The actual data rate offered to an end-user will be reduced due to the use of forward error correction (FEC). It should also be noted that the overhead occupied by the pilot-data is negligible ($\ll 1\%$), as the pilot-data does not need to be transmitted continuously [9].

III. EXPERIMENTAL RESULTS

Fig. 2 shows the system frequency response of the 500 m MMF link, which is measured from the input of the IFFT in the transmitter to the output of the FFT in the receiver. The response is normalized to the power of the first subcarrier at 125 MHz. The observed ~ 11.5 dB roll-off over the entire signal spectrum is mainly due to: 1) the on-chip output filtering of the DAC and its inherent $\sin(x)/x$ response, 2) the DMD effect. If all the
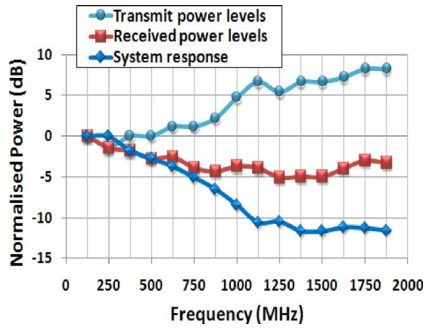
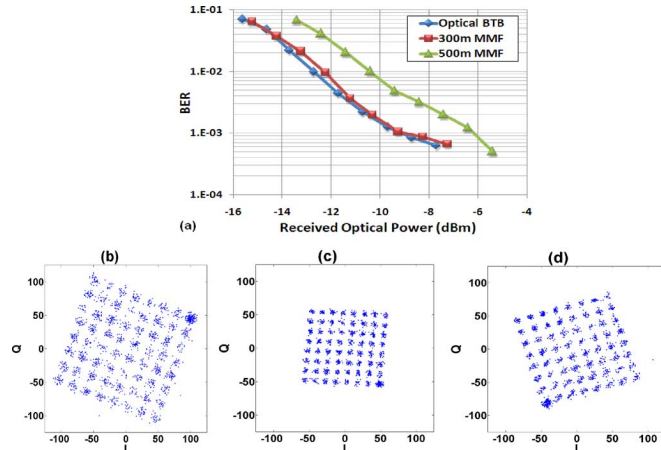Fig. 2. Transmitted and received subcarrier powers and system frequency response for the 500-m MMF system.

Fig. 3. (a) BER performance of real-time 11.25-Gb/s 64-QAM-encoded OOFDM signal transmission over 300- and 500-m MMF and optical back-to-back link configurations. (b)-(d) Received subcarrier constellations before channel equalization after 500-m MMF transmission. (a), (b) 1st Subcarrier. (c) 8th Subcarrier. (d) 15th Subcarrier.

transmitted subcarriers have equal powers in the transmitter, the received subcarrier power variation of ~ 11.5 dB is too large to produce an acceptable total channel BER.

To effectively compensate for the system frequency response roll-off effect, use is made of the variable power loading technique reported in [5]. The resulting optimum variable power loading profile across all the subcarriers prior to the IFFT in the transmitter is shown in Fig. 2, where the corresponding received subcarrier power levels recorded immediately after the FFT in the receiver are also plotted. The received subcarrier powers vary within a range as small as 5 dB and lead to an almost uniform error distribution across all the subcarriers. It should be noted that the optimum clipping level is also dependent upon variable power loading [5].

Making use of the variable power loading profile illustrated in Fig. 2, the measured BER performance is shown in Fig. 3(a) for three different cases: optical back-to-back, a 300 m MMF and a 500 m MMF. For the 500 m MMF link, a minimum BER of 4.5×10^{-4} is obtained, and the corresponding received constellations prior to channel estimation are plotted in Fig. 3(b–d) for the 1st, 8th and 15th subcarriers.

It can be seen in Fig. 3(a) that, for the 500 m MMF link, the minimum received optical power required for achieving a BER of 1×10^{-3} is approximately -6.3 dBm, implying that the optical power budget can be as high as 12 dB when a typical 6 dBm DFB laser is employed.

Fig. 3(a) also shows that, for the 300 m MMF, the measured power penalty at a total channel BER of 1×10^{-3} is negligible, suggesting that the adopted cyclic prefix is sufficiently long to completely compensate for the DMD effect associated with the link. However, when the transmission distance is increased to 500 m, a power penalty of approximately 3 dB occurs, which is mainly attributed to the effects of long transmission distance-induced large DMDs and modal noise. Our experimental investigations suggest that the modal noise effect contributes approximately 1 dB power penalty for the 500 m MMF, whilst for the 300 m MMF the modal noise effect is negligible.

It is also worth mentioning that our initial experimental research indicates that gain control can be used to compensate any drift in the received electrical signal level, and thus significantly minimize the modal noise effect.

IV. Conclusion

A record-high real-time end-to-end OOFDM transmission at 11.25 Gb/s over 500 m MMFs has been experimentally demonstrated, for the first time, in simple DML-based IMDD systems. Real-time experimental investigations are currently being undertaken to explore the potential of the OOFDM technique for upgrading legacy MMF-based LANs to > 20 Gb/s.

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Experimental demonstration and optimisation of a synchronous clock recovery technique for real-time end-to-end optical OFDM transmission at 11.25Gb/s over 25km SSMF

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Abstract: A simple, digital signal processing-free, low-cost and robust synchronous clocking technique is proposed and experimentally demonstrated, for the first time, in a 64-QAM-encoded, 11.25Gb/s over 25km SSMF, real-time end-to-end optical OFDM (OOFDM) system using directly modulated DFB laser-based intensity-modulation and direct-detection (IMDD). Detailed experimental investigations show that, in comparison with the common clock approach utilised in previous experimental demonstrations, the proposed clocking technique can be implemented to achieve no system BER performance degradation or optical power budget penalty and more importantly to improve system stability. As a viable synchronous clocking solution for real-time OOFDM transmission, this work is a vital step towards the realisation of practical OOFDM transmission systems and has particular significance for synchronisation of OOFDM multiple access-based passive optical networks where highly accurate synchronisation of all network elements is essential.

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1. Introduction

It is widely accepted that there is a need to drastically increase the transmission capacity of existing networks to support the rapidly emerging bandwidth-hungry internet services. In particular, access networks are the main network bottlenecks, consequently this is driving the rapidly growing roll out of fiber to the home (FTTH). At present, conventional optical transmission techniques can support high bandwidths needed in the near future, however advanced optical transmission techniques are essential to support the demand for ultra-high bandwidths further into the future. Optical orthogonal frequency division multiplexing (OOFDM) is widely recognised as a strong candidate for a cost-effective, "future-proof" optical transmission technology to enable next generation ultra-high-speed optical networks. Evidence of this is the large number of research groups world-wide undertaking OOFDM research activities. However, most research is based on non-real-time, off-line digital signal processing (DSP). To date, several research groups have demonstrated OOFDM transmission involving real-time DSP in either the transmitter [1,2] or receiver [3,4]. These experiments, however, do not completely eliminate off-line DSP for true end-to-end real-time OOFDM transmission.

To our knowledge, we are the first and only group that has demonstrated a series of end-to-end real-time OOFDM transmission experiments implemented with field programmable gate array (FPGA)-based DSP in both the transmitter and receiver [5]. Our key objectives so far have been to experimentally demonstrate that real-time, high-speed OOFDM transmission can be achieved over realistic transmission distances in both standard single-mode fibre (SSMF)-based access networks [5] and multi-mode fibre (MMF)-based local area networks [6], in a cost-effective manner, by utilising off-the-shelf, low-cost optical/electrical components. It has also been shown [5,6] that modern digital semiconductor electronics can perform the computationally intense algorithms, in particular, the fast Fourier transform (FFT) and inverse FFT (IFFT), in real-time with sufficient speed and accuracy required for end-to-end real-time OOFDM transmission, and also that intensity-modulation and direct-detection (IMDD) OOFDM systems can be implemented using low-cost directly-modulated DFB lasers (DMLs) [5,6], vertical cavity surface-emitting lasers (VCSELs) [7] and reflective semiconductor optical amplifiers (RSOAs) [8]. Furthermore, our experimental results have also shown that, in simple DML/VCSEL-based IMDD transmission systems, digital-to-analogue converters (DACs) and analogue-to-digital converters (ADCs) operating at sampling rates as low as 4GS/s can support signal bit rates as high as 11.25Gb/s over 25km SSMF [5,7] and 500m MMF [6].

The transmitter and receiver in our previously reported real-time end-to-end OOFDM systems both derived their required clock signals from a common reference clock, as do the OOFDM receiver experiments [3,4]. It is obvious that, in a practical system, the receiver must independently generate a suitable clock. Generally speaking, for any transmission system, there are two distinct receiver clock generation methods: asynchronous and synchronous. In an asynchronously clocked system, the receiver operates with an independent oscillator, and uses the received signal to accurately detect the offset between the transmitter and receiver

clocks, the offset effects are then compensated for in the receiver; while in a synchronously clocked system, the receiver extracts a synchronous clock signal from the received signal based on embedded timing information.

For asynchronously clocked OOFDM transmission, sampling clock offset (SCO) and symbol timing offset (STO) may occur, which, if not suitably compensated, degrade the system performance due to the ICI and ISI effects [9,10]. The necessary compensation of the SCO and STO effects inevitably requires additional DSP resources which add extra complexity to the receiver. In addition, depending on the transceiver implementation, individual SCO compensation may be needed for each subcarrier, therefore, DSP resources increase with the number of subcarriers. Real-time asynchronously clocked OOFDM transmission [10] has been experimentally demonstrated at 11.25Gb/s, which employs DSP to extract timing information directly from the OOFDM signal through detection of any drift in cyclic prefix position, OOFDM symbol realignment then compensates both the SCO and STO effects.

Synchronously clocked OOFDM is free from the SCO and STO effects, assuming fast tracking of any transmitter clock drift, sampling instance errors are only caused by residual jitter of the receiver's sampling clock. However, extracting timing information directly from the noise-like, analogue, high-speed OOFDM signal is challenging and also requires additional DSP functionality in the receiver.

In [11,12], a simple, DSP-free synchronous clocking technique has been proposed and experimentally demonstrated in a real-time end-to-end IMDD OOFDM system at 11.25Gb/s over 25km SSMF using a DML. In this paper, in-depth investigations of the DSP-free synchronous clocking technique are undertaken in the aforementioned transmission systems in terms of: a) identification of optimum operating conditions for maximisation of the system transmission performance, and b) examination of system performance robustness. It is shown that a high quality receiver clock can be recovered from the received optical signal, and more importantly, that there is no BER degradation or optical power budget penalty compared to the common clock approach. It is also shown that the synchronous clocking technique leads to a significant improvement in system stability.

The work reported here is a vital milestone towards the realisation of practical OOFDM systems. This work also has particular significance for synchronisation of OOFDM multiple access-based passive optical networks (OOFDMA-PONs). An example OOFDMA-PON is illustrated in Fig. 1(a). For operating the OOFDMA-PON, all network elements must be highly synchronised, this is because OOFDMA divides bandwidth between users using dimensions of both frequency and time [13]: subcarriers provide bandwidth partitioning in the frequency domain and timeslots provide bandwidth partitioning in the time domain. Dynamic bandwidth allocation (DBA) can therefore be performed with a high granularity as represented by the individual "data blocks" in Figs. 1(b,1c). In downstream transmission, the timing for all users can be synchronised due to the common optical line terminal (OLT). Whilst in upstream transmission, clock offset between different optical network units (ONUs) can result in offsets in both the frequency and time domains, thus causing the "data blocks" to merge in both dimensions, as shown in Fig. 1(c). The offsets in the frequency domain destroy orthogonality between subcarriers, resulting in inter-subcarrier leakage; the offsets in the time domain lead to severe merging of timeslots/frames if no mechanism is employed to maintain timeslot/frame alignment. Therefore, it can be far more practical to implement OOFDMA-PONs using synchronously clocked ONUs, because of the following two key reasons: firstly, subcarrier orthogonality is preserved in the upstream, secondly, any timeslot/frame drifts between ONUs are eliminated thus avoiding the need for additional DSP to track and readjust timeslot offsets.

OOFDMA-PONs in Fig. 1(a) can also potentially support multiple time-division-multiplexed (TDM) PON standards [13], this coexistence of different standards has the advantage that subscribers can be gradually migrated to the higher speed next generation PON

standards such as OOFDMA, without changes to the network infrastructure. Backwards compatibility of OOFDMA-PONs and its overlay with existing PON standards is only possible if the entire PON can be synchronised together with inter-timeslot allocation management. The OOFDM synchronisation technique presented in this paper therefore has great potential for drastically simplifying the implementation of OOFDMA-PONs.
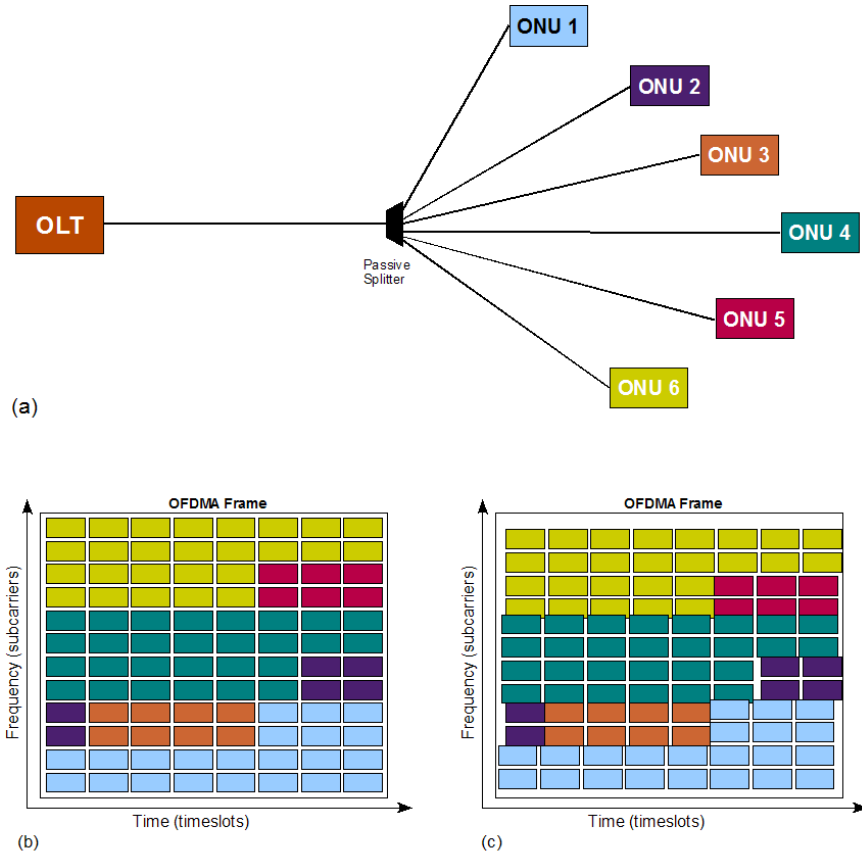

Fig. 1. (a) Example OOFDMA-PONs, (b) OOFDMA upstream frame with synchronously clocked ONUs, (c) OOFDMA upstream frame with asynchronously clocked ONUs without compensation (colours represent "data blocks" from individual ONUs).

2. Principle of synchronous OOFDM clocking technique

The proposed and implemented synchronous clocking technique [11,12], as illustrated in Fig. 2, overcomes the difficulty of extracting timing information directly from the OOFDM data signal by combining a dedicated electrical timing signal, here referred to as the synchronisation clock, S_{CLK}, with the generated electrical OFDM signal, S_{OOFDM}. In the OOFDM transmitter, S_{CLK} and S_{OOFDM} are summed together electrically to produce a combined signal S_{COMB}, which is utilised to directly modulate the intensity of an optical laser source. The synchronisation clock is a sine wave at a frequency outside the OFDM signal band. The transmitter requires at least two top level clock signals namely $C_{TXLOGIC}$ and C_{DAC}: $C_{TXLOGIC}$ clocks the transmitter's digital logic and C_{DAC} is used by the DAC to generate the sampling clock, either directly or indirectly. $C_{TXLOGIC}$, C_{DAC} and S_{CLK} are all generated from a common reference clock, C_{REF}, as all clocks must be synchronous.

In the transmitter, after being combined with an appropriate DC bias current, the S_{COMB} signal directly modulates the intensity of an optical laser source to generate an OOFDM signal

for transmission. The total bandwidth of the signal S_{COMB} is much lower than bandwidths of any optical filters or WDM multiplexers/demultiplexers in the optical signal path such that it can pass transparently through the system from transmitter to receiver. After transmission through the optical system, the received intensity-modulated OOFDM signal is directly detected by a photo-detector in the receiver to produce an electrical signal S'_{COMB}. This signal is then split to extract the received OFDM signal, S'_{OOFDM}, by low-pass filtering, and also to extract the received synchronisation clock, S'_{CLK}, by band-pass filtering. S'_{OOFDM} is appropriately amplified and digitised for subsequent DSP to recover the transmitted data following a procedure detailed in [5]. The received, jittered clock signal S'_{CLK} is pre-scaled to reduce its frequency before driving a phase locked loop (PLL) which generates a receiver clock, from which all required receiver clocks can be produced. The PLL can convert the received clock frequency and also provides a high level of jitter suppression such that stable, low jittered clocks are produced to drive the receiver's electronics. Similar to the transmitter, the receiver also requires two top level clocks $C_{RXLOGIC}$ and C_{ADC}: $C_{RXLOGIC}$ is the clock for the receiver's digital logic and C_{ADC} is the clock for the receiver's ADC. The ADC generates the sampling clock either directly or indirectly from C_{ADC}. It should be emphasized that all clocks in the transmitter and receiver, in particular the DAC and ADC sampling clocks, are synchronous and originate from C_{REF} in the transmitter, thus the SCO effect is negligible.
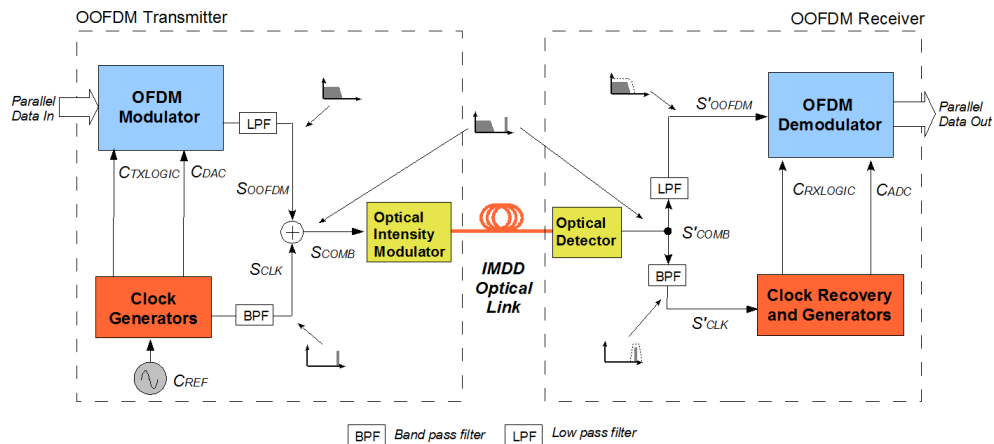

Fig. 2. Basic system configuration for synchronously clocked OOFDM system

The basic method of transmitting and recovering the synchronisation clock is relatively straightforward. However, applying it to a real-time OOFDM system provides an extremely effective, low complexity, low cost and robust clocking solution which avoids the need for any DSP for receiver clock generation. Although the basic clock transmission principle is relatively simple, the clock must be transmitted independently to the OFDM signal yet as the signals are transmitted simultaneously through the same optical system, careful system design is required to identify optimum operating conditions where the clock and data transmission functions can satisfactorily coexist.

It should be noted that the use of the proposed synchronous clocking technique for both upstream and downstream traffic in OOFDMA-PONs, does not require any additional clocks to be generated, as the additional transmitter and receiver can utilise the available clocks. The clock driving the digital logic can drive both the transmitter and receiver logic, which would most likely be in the same integrated circuit, likewise the DAC/ADC clock can be used to drive both DAC and ADC simultaneously.

2. Real-time OOFDM experimental system setup for synchronous clock recovery

Figure 3 shows the experimental setup for the synchronously clocked real-time OOFDM system. As implementation of the real-time OOFDM data generation/detection has been reported in detail in [5], this paper focuses particular attention on the implementation and optimisation of the synchronous clocking technique. In the FPGA-based real-time OOFDM transmitter and receiver, 64-QAM encoding/decoding is employed on all 15 subcarriers, giving a raw data rate of 11.25Gb/s. To achieve optimum system performance, the FPGA design uses the same channel estimation, adaptive power loading, live parameter control, symbol alignment and on-line performance analysis functions as described in [5]. Table 1 summarises all the key system parameters and Fig. 3 also indicates all RF amplifier gains and RF filter cut-off frequencies. In comparison to [5], in the transmitter an RF amplifier is introduced to increase the OFDM signal power from the DAC to compensate the coupler loss and, in combination with electrical attenuators, to maximise the adjustment range of the signal power. In the receiver an RF amplifier is also used before the splitter to compensate its loss. Compared to [12] a higher gain amplifier is used to amplify S'_{CLK}.

At the transmitter, a frequency synthesiser functions as the master clock source operating at 4GHz with an accuracy of $\leq$3ppm. This clock is also internally pre-scaled to provide a 100MHz clock for the transmitter FPGA ($C_{TXLOGIC}$) (100MHz is the OOFDM symbol rate). One 4GHz output from the frequency synthesiser is divided by 2, band-pass filtered and amplified to generate a 2GHz sine wave signal for the 4GS/s DAC (C_{DAC}). The DAC consists of four interleaved converters so the 2GHz clock is further subdivided to 1GHz internally in the DAC. A second 4GHz output is band-pass filtered and variably attenuated to provide the dedicated 4GHz synchronization clock signal (S_{CLK}). The amplitude of S_{CLK} can be adjusted directly with the synthesiser's output level adjustment and the variable electrical attenuator is also used to extend the adjustment range. The electrical OFDM signal from the DAC (S_{OOFDM}) is amplified, low-pass filtered and variably attenuated before combination with the synchronization clock via a resistive RF coupler. The signal from the coupler (S_{COMB}) is attenuated and combined via a bias-T with an optimised DC bias current to directly modulate a 10GHz, 1550nm DFB laser. After boosting the DFB output power with an EDFA and optical band-pass filtering to reduce ASE, the optical launch power is set at 6dBm. The 25km SSMF has an 18ps/nm/km chromatic dispersion parameter and a linear loss of 0.2dB/km at 1550 nm.

At the receiver a variable optical attenuator is used to control the received optical power prior to a 12.4GHz linear PIN detector. The electrically amplified output of the PIN (S'_{COMB}) is split by a 2-way resistive RF splitter. One output that feeds the OOFDM receiver is low-pass filtered to remove the clock signal and provide anti-aliasing filtering. Having been amplified and suitably attenuated, the signal (S'_{OOMDM}) is then fed to the differential input of the 4GS/s ADC via a balun. As the received optical power varies, S'_{OOMDM}'s electrical gain is also adjusted accordingly to optimise the signal amplitude at the ADC input. Automatic gain control (AGC) can of course be implemented by measuring the received signal amplitude, and controlling a variable gain amplifier (VGA). The second output is amplified by a high gain amplifier (30dB) and band-pass filtered to extract only the 4GHz synchronisation clock signal (S'_{CLK}). A pre-scaler reduces the clock frequency to 10MHz, which is then low-pass filtered and used as the external reference for a clock synthesizer generating the 2GHz clock for the receiver's ADC (C_{ADC}), this clock is also pre-scaled to generate the 100MHz receiver FPGA clock ($C_{RXLOGIC}$). In the present system setup, the clock synthesizer in the receiver effectively operates as a PLL, such clock synthesizer can, however, be easily replaced by a low-cost, fixed frequency PLL with a 1/20 prescaler.
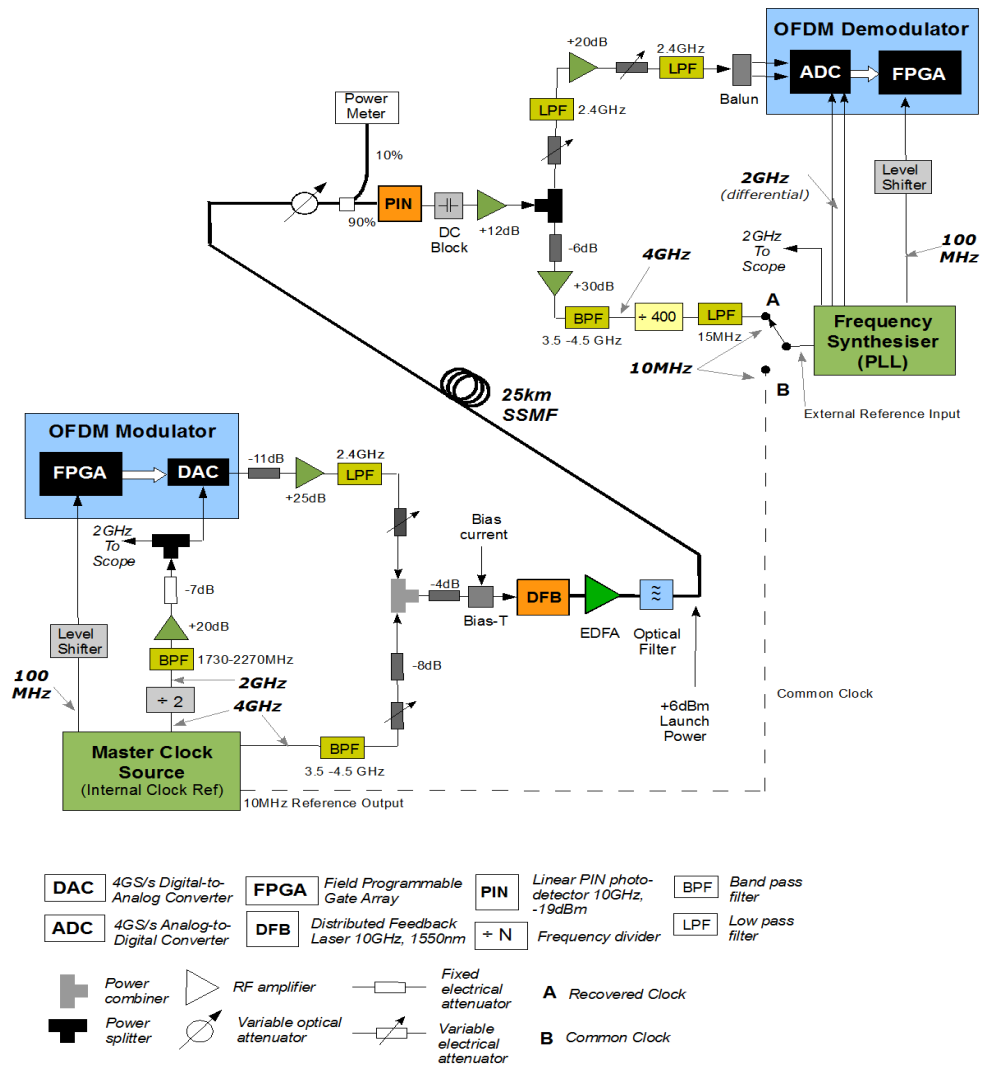
Fig. 3. Experimental system setup for real-time OOFDM transmission at 11.25Gb/s with synchronous clock recovery.

To configure the system to also operate with the common clock method as used in [5–7], the 10MHz reference output from the transmitter's clock synthesiser is directly connected to the external reference input of the receiver's frequency synthesiser. This is illustrated in Fig. 3 where the external reference input is connected to point A to use the recovered clock and to point B to use the common clock. Changing between the recovered clock and the common clock in this way enables a direct comparison of the two clocking methods under exactly the same system setup and operating conditions. The optimum signal clipping ratio and adaptive subcarrier power loading profile [5] are obtained for the 25km IMDD SSMF system using the common clock configuration and employed for all measurements. This ensures any performance variations observed are only due to the two different clocking methods.

Table 1. Transceiver and system parameters

Parameter	Value
Total number of IFFT/FFT points	32
Data-carrying subcarriers	15
n-th subcarrier frequency	$n \times 125$MHz
Modulation format on all subcarriers	64-QAM
DAC & ADC sample rate	4GS/s
DAC & ADC resolution	8 bits
Symbol rate	100MHz
Samples per symbol (IFFT)	32 samples (8ns)
Cyclic prefix	8 samples (2ns)
Total samples per symbol	40 samples (10ns)
Error count period	88,500 symbols (7965000bits)
Raw signal bit rate	11.25Gb/s
Net signal bit rate (cyclic prefix 25%)	9Gb/s
DFB laser wavelength	1550nm
DFB laser modulation bandwidth	10GHz
DFB laser bias current	40mA[a] (42mA max)
DFB laser driving voltage	655mVpp[a,b] (900mVpp max)
EDFA output power	10dBm
PIN detector bandwidth	12.4GHz
PIN detector sensitivity	−19dBm [c]
SSMF dispersion parameter at 1550nm	18ps/(nm·km)

[a] Optimised value
[b] Combined OFDM signal and clock signal
[c] Corresponding to 10 Gb/s non-return-to-zero data at a BER of 1.0×10^{-9}

3. Experimental results

3.1 Operation of synchronously clocked real-time OOFDM

The DML-modulated 11.25Gb/s OOFDM signals with the 4GHz synchronisation clock are transmitted simultaneously over an IMDD 25km SSMF system with successful clock and data recovery in the receiver. Figure 4 shows electrical signal waveforms at various points in the system subject to optimum operating conditions identified in Section 3.2. It should be noted that all peak-to-peak signal levels in Fig. 4 include ~20mVpp of internal oscilloscope noise. At the selected operating conditions, the RF signal powers at the bias-T input are approximately −16dBm for the synchronisation clock and −9.6dBm for the OFDM signal, the synchronisation clock power is therefore 6.4dB lower than the power of the OFDM signal. In the optical domain this corresponds to a power difference of 3.2dB. For the previously reported, un-optimised operating conditions [12], the employed synchronisation clock power is 4dB higher than the OFDM signal. Here the clock signal power is significantly reduced and is now lower than the OFDM signal power as oppose to higher.
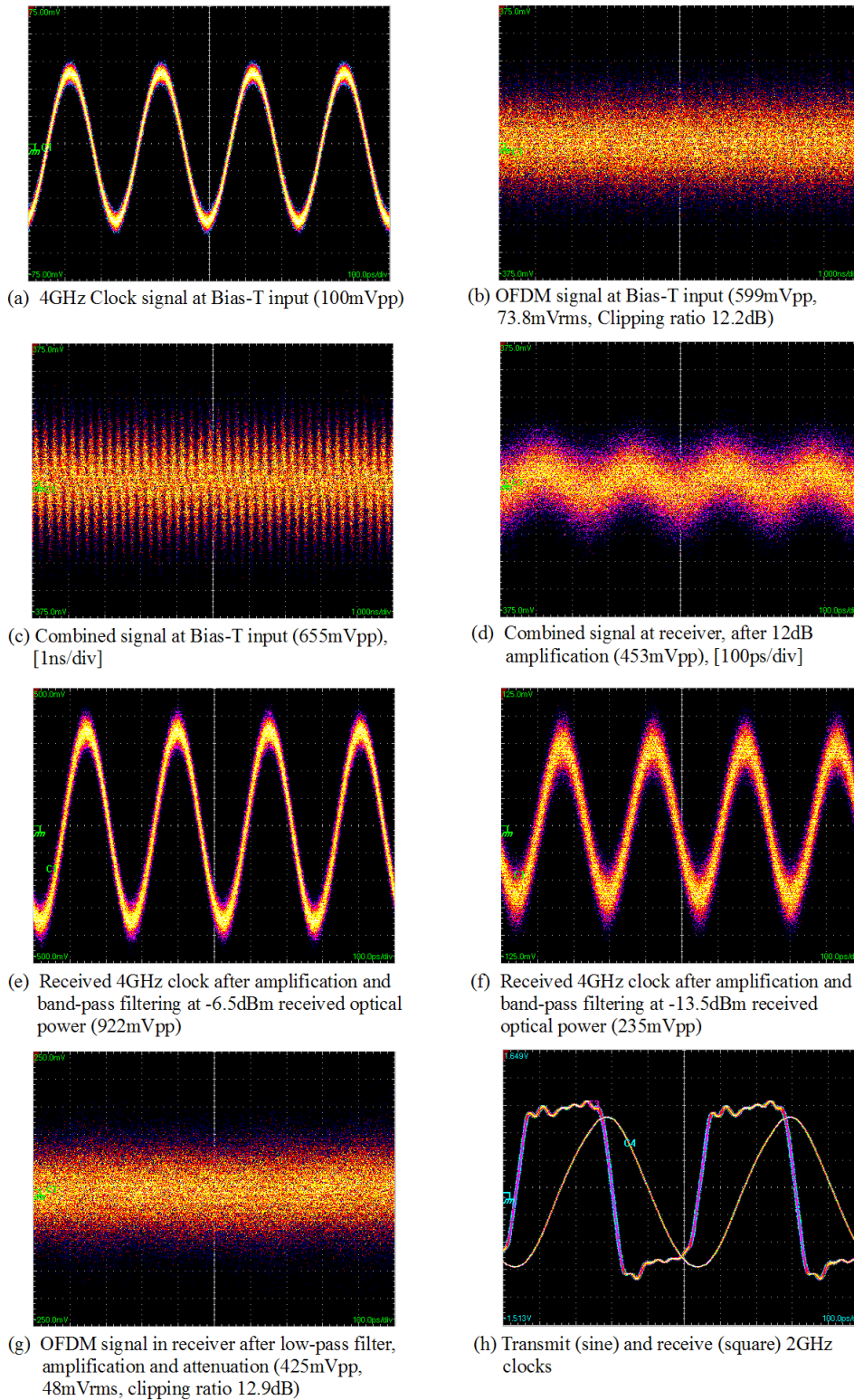
(a) 4GHz Clock signal at Bias-T input (100mVpp)

(b) OFDM signal at Bias-T input (599mVpp, 73.8mVrms, Clipping ratio 12.2dB)

(c) Combined signal at Bias-T input (655mVpp), [1ns/div]

(d) Combined signal at receiver, after 12dB amplification (453mVpp), [100ps/div]

(e) Received 4GHz clock after amplification and band-pass filtering at -6.5dBm received optical power (922mVpp)

(f) Received 4GHz clock after amplification and band-pass filtering at -13.5dBm received optical power (235mVpp)

(g) OFDM signal in receiver after low-pass filter, amplification and attenuation (425mVpp, 48mVrms, clipping ratio 12.9dB)

(h) Transmit (sine) and receive (square) 2GHz clocks

Fig. 4. Signal waveforms of the OFDM data signal, 4GHz synchronisation clock, combined signal and 2GHz system clocks measured in the transmitter and receiver.

Figure 5 shows the electrical spectra of both the transmitted signal S_{COMB} and received signal S'_{COMB} measured with the same resolution bandwidth (3MHz). The OFDM signal occupies the baseband frequency region of <2GHz, above which the residual OFDM signal image due to imperfect low-pass filtering in the transmitter is also observed. However, it is not necessary to insert a capacity-reducing guard band to permit the image signal to be completely removed by filtering. The synchronisation clock is clearly seen at 4GHz and it is evident that there is a frequency spacing of more than 1GHz below the clock to allow easy separation of the OFDM signal and the synchronisation signal by low order filters having a low pass-band width as wide as 1GHz. To reduce the total bandwidth of the signal and thus the bandwidths of required optical and electrical components, the frequency of S_{CLK} can be reduced, this, however, increases the requirements of the band-pass filter in terms of narrower pass-band width and out-of-band blocking. The low-pass filtering used to extract the OFDM signal would similarly require higher performance to ensure any of the synchronisation clock signal remaining after filtering does not generate a significant aliasing product in the OFDM signal region as a result of under-sampling. More importantly, as the frequency spacing between the synchronisation clock and the OFDM signal band reduces, a threshold may be reached where unwanted interferences occur between the synchronisation clock and the OFDM signal band. Future research work is planned to investigate the dependence of the system performance on synchronisation clock frequency.
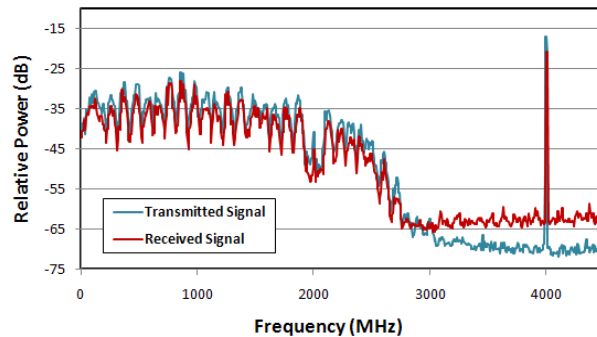

Fig. 5. Spectra of transmitted signal (at Bias-T input) and received signal (after first receiver RF amplifier)

3.2 Optimisation of synchronously clocked real-time OOFDM system

To examine if any BER performance degradation occurs due to the presence of the synchronisation clock signal, the optimum electrical signal levels of the synchronisation clock and OFDM signals are investigated. Firstly, irrespective of the system BER, the allowed values of the S_{OOFDM} signal level and the S_{CLK} signal level under which synchronisation can be maintained is determined. Synchronisation is defined as the state where the receiver's clock recovery circuit generates stable clocks locked to the transmitter's clocks. To detect whether or not the system is synchronised, the 2GHz DAC and ADC clocks are simultaneously fed to an oscilloscope from the test points indicated in Fig. 3, it is then possible to observe when the receiver clocks are stable and locked to the transmitter clock, as shown in Fig. 4(h).

Figure 6 plots both the maximum and minimum clock levels for synchronisation as the OFDM signal level is varied. Both signal levels are measured at the input to the bias-T (50Ω). The effect of laser bias current on the synchronisation range is also illustrated in Fig. 6. As expected, if the bias current is too low (<38.5mA) the clock and OFDM signal ranges over which synchronisation can be achieved are reduced; whilst for a bias current at 40mA a large synchronisation range is achieved. Further increasing the bias currents beyond 40mA (42mA maximum) only has the effect of allowing a small increase in the maximum clock level at

higher OFDM signal regions. At the 40mA bias current, the maximum permitted OFDM signal level to maintain synchronisation is approximately 600mVpp. It is worth pointing out that the DFB laser can be driven up to around 900mVpp.

To further explore the impact of the synchronisation clock on the system performance, for the cases of the synchronisation clock present and absent, the system BER is measured as the peak-to-peak (PTP) amplitude of the OFDM signal is varied for the system configuration using the common clock. The system set up and parameters considered are identical for both cases. The measured results are shown in Fig. 7. In obtaining Fig. 7, the synchronisation clock amplitude is selected as 100mVpp, as this value provides a low clock amplitude sufficient to maintain synchronisation with a small margin above the minimum required clock level. A 40mA bias current is also used, as this provides the maximum range for the OFDM signal level where synchronisation can be achieved. It should also be noted that the above-mentioned bias current setting is also determined by the DML used.
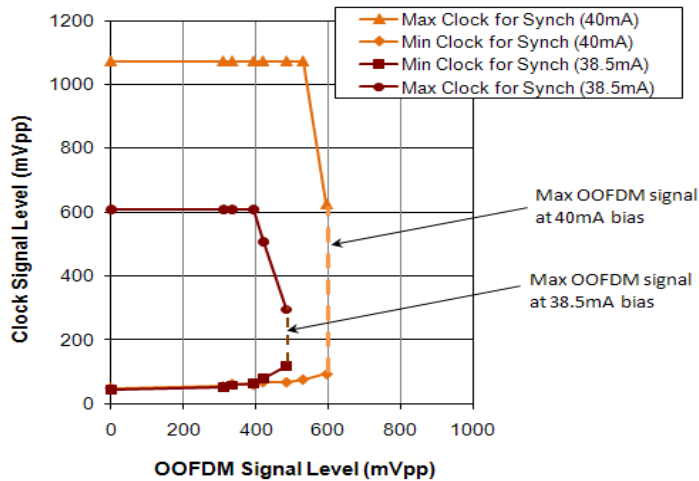

Fig. 6. Synchronisation region for varying OOFDM signal and clock levels

Figure 7 shows that the OFDM signal level has an exploitable operating region from approximately 530mVpp to 760mVpp where the OFDM signal power-dependent BER variation is negligible. More importantly, it is also shown that the presence of the synchronisation clock at the selected level has almost negligible impacts on the system BER performance within the aforementioned exploitable operating region. Therefore, if an OFDM signal level of 600mVpp is selected, this is both within the exploitable operating region and the synchronisation region, so even though the OFDM signal level must be limited to ~600mVpp to allow receiver synchronisation, this is still adequate to achieve optimum system performance.
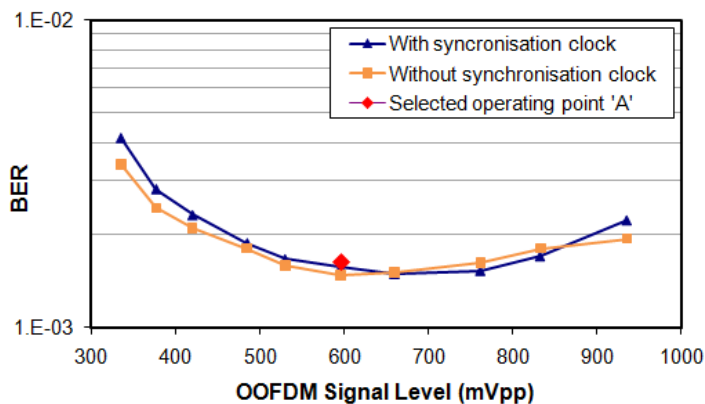
Fig. 7. BER variation with OOFDM electrical signal level (at bias-T input) with 40mA bias current, measured with and without the synchronisation clock present and operating with the common clock configuration.

In all experimental results presented below, the operating point (point A in Fig. 7) is selected, which corresponds to an OFDM signal level of 600mVpp, a synchronisation clock level of 100mVpp and a bias current of 40mA. This point allows operation with synchronous clock recovery in the receiver without any BER degradation compared to the minimum BER achieved with the common clock configuration. In Fig. 7, the occurrence of the minimum BERs for both cases considered is a direct result of the driving signal-induced variations in signal distortion/clipping and extinction ratio of the intensity modulated signals: A high OFDM signal level leads to a large OOFDM signal extinction ratio. This increases the effective signal-to-noise ratio (SNR) in the receiver, thus decreasing the BER; whereas a high OFDM signal level also causes increased signal waveform distortions and severe signal clipping, leading to an increase in BER. The co-existence of these opposing effects results in the trough shaped curve shown in Fig. 7. It is contrary to the expectation that when the synchronisation clock is introduced this would lead to a degradation in system performance due to the higher driving signal-induced signal distortion, which is not accompanied by an improvement in the effective extinction ratio of the OOFDM signal. An increase in the peak DFB driving voltage, however, only occurs when the positive (negative) clock signal peaks coincide with the OOFDM positive (negative) signal peaks, these new peaks have higher frequency content so any increase in distortion/clipping mainly occurs to the high frequency clock rather than the lower frequency OOFDM signal. The clock signal can therefore be introduced to increase the DFB driving voltage without degrading the BER performance.
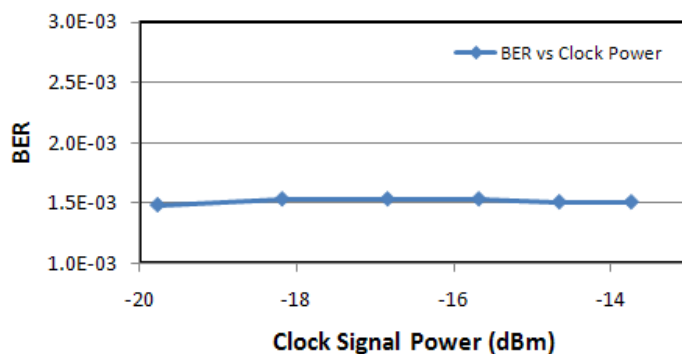

Fig. 8. BER variation with synchronisation clock power under optimum operating conditions.

Having discussed the OFDM signal voltage dependent system BER performance, Fig. 8 is plotted to investigate the influence of the synchronisation clock power level on the system BER performance. In obtaining Fig. 8, the transmission system is configured for synchronous clocking subject to the optimum OFDM signal voltage identified in Fig. 7. It can be seen in Fig. 8 that the clock signal power can be varied over a range of at least 6dB without effecting the system BER. Such a wide dynamic range implies that the system is very robust to variations in the clock signal power. It should also be noted that, to maintain synchronisation, the tested clock signal power region is limited to the maximum output adjustment range of the frequency synthesiser employed in the experiments, the dynamic clock range may therefore exceed 6dB.

3.3 Performance of synchronously clocked real-time OOFDM

For 11.25Gb/s over 25km SSMF OOFDM signal transmission in the DML-based IMDD system under the identified optimum operating conditions, the system BER performance as a function of received optical power is plotted in Fig. 9 for both the common clock configuration and the synchronous clock configuration. The results clearly show that the BER performance of these two cases are identical, implying that the synchronous clocking technique allows a high quality clock to be recovered in the receiver, and more importantly, that the technique does not result in any BER or optical power budget degradation. The high quality of the recovered clock can also be seen in Fig. 4(h), where the 2GHz clock in the receiver (C_{ADC}) with a peak-to-peak jitter as small as 10ps is clearly locked to the 2GHz clock in the transmitter (C_{DAC}). Furthermore, Fig. 10 presents comparisons of subcarrier constellations measured before equalisation in the receiver, between the common and recovered clock cases. The observed excellent resemblance between corresponding subcarrier constellations further verifies the high performance of the synchronous clocking technique.

The optical back-to-back BER performance is plotted in Fig. 9, which shows that there is an optical power penalty of <1dB at a widely adopted forward error correction (FEC) limit of 2.3×10^{-3}. In addition, the minimum BER achieved for both clocking methods is $\sim 1.5 \times 10^{-3}$, which is slightly higher than that obtained in [5]. Such a difference is due to the utilisation of extra electrical components including amplifiers, couplers and splitters, as illustrated in Fig. 3. These additional components give rise to increased noise and signal distortions. A main source of distortion is believed to originate from the RF component ports, which do not offer a sufficiently high and uniform return loss over the wide signal spectral range (0-4GHz).

Experimental measurements also indicate that the clock recovery can operate with a received optical power as low as −13.5dBm. This is also verified in Fig. 4(f), where the received 4GHz clock at a received optical power of −13.5dBm shows more jitter and noise compared to the received 4GHz clock at a received optical power of −6.5dBm, as presented in Fig. 4(e). The 7dB reduction in received optical power does not have an effect similar to a 14dB reduction in transmitter's electrical power, as such an electrical power reduction destroys the system synchronisation. This implies that the intensity-modulated optical power does not affect the performance of the proposed technique, further demonstrating the robustness of the synchronous clocking technique.

3.4 System performance stability

The system performance stability over time is examined for both the common clock and synchronous clock methods. It is known that the DFB laser wavelength may drift slowly with small changes in laser temperature. When the common clock configuration is used, a drift in laser wavelength results in a wavelength-dependent differential time delay between the clock signal and the received OFDM signal. As manual symbol alignment is used, the change in the differential time delay effectively shifts the symbol alignment in the receiver, thus leading to the BER degradation. This is the physical mechanism underpinning the BER evolutions shown in Fig. 11(a), where the first plot shows the BER increasing after initial symbol

alignment as the symbol alignment deteriorates; whilst the second plot shows the BER reducing as the symbol alignment improves. When the BER drifts it is always possible to restore the system operation to the minimum BER by only readjusting the symbol alignment.
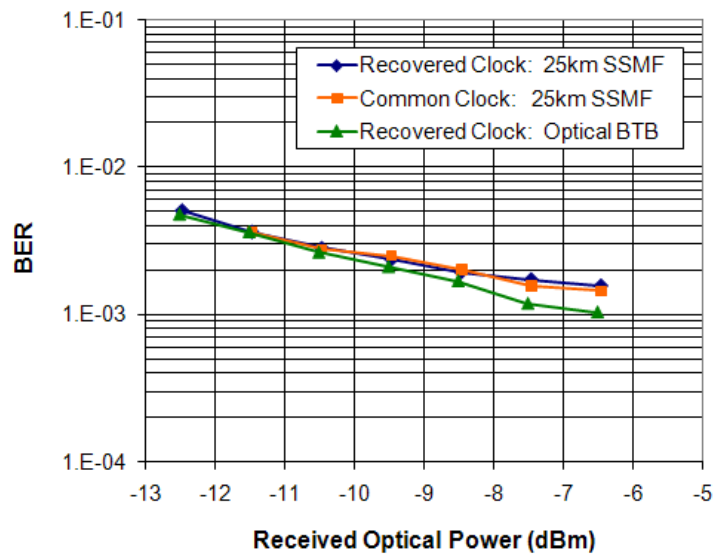

Fig. 9. BER performance of real-time 11.25Gb/s OOFDM with recovered clock and common clock for IMDD 25km SSMF and optical back-to-back performance with recovered clock.
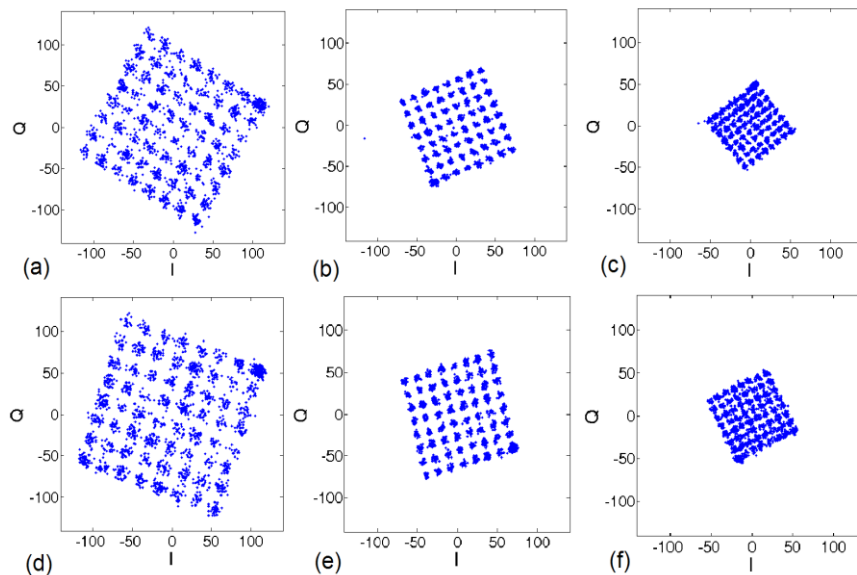

Fig. 10. Received 64-QAM subcarrier constellations before channel equalisation for 25km SSMF with common clock (a) 1st SC, (b) 8th SC, (c) 15th SC and recovered clock (d) 1st SC, (e) 8th SC, 15th SC
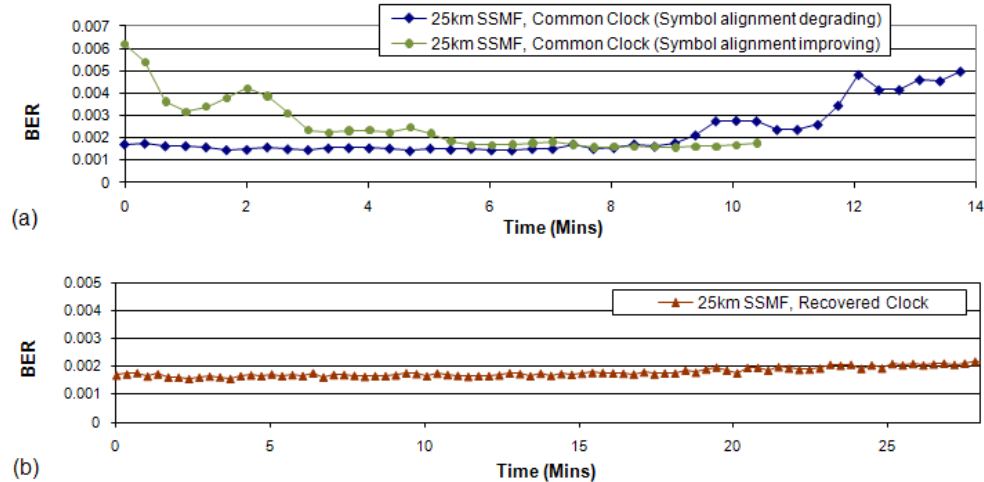
Fig. 11. BER performance stability for (a) common clock configuration and (b) synchronous clocking configuration.

In sharp contrast, when BER stability is observed with the synchronous clocking technique, it is seen to be significantly more stable as shown in Fig. 11(b). The BER can remain stable for over one hour before symbol realignment is needed. The improved stability is due to the fact that the clock signal is transmitted with the OOFDM signal, therefore any change in the signal propagation time due to the laser wavelength drift is experienced by both the OFDM signal and the clock, therefore no significant differential time shift is produced within the experimental measurement period to significantly degrade the symbol alignment and hence the BER. However, the DFB wavelength drift with small changes in laser temperature can still result in very small BER deteriorations over a long period of time, as observed in Fig. 11(b). This is mainly due to the wavelength dependent chromatic dispersion-induced differential time delay between the OFDM signal and the clock signal. This BER drift effect is now due to the small differential wavelength variation as opposed to the absolute wavelength change in the common clock case, thus dramatically reducing the impact on the BER drift.

4. Conclusions

Synchronous clock recovery has been proposed, experimentally demonstrated and optimised in a real-time end-to-end DML-based 11.25Gb/s OOFDM IMDD system. The technique offers a low-cost, low-complexity, DSP-fee, robust solution with no BER performance or optical power budget penalty and achieves improved BER stability. The work presented here is a vital step towards the realisation of practical OOFDM transmission systems. Furthermore this work is also important as it potentially offers a simple and highly effective solution for network synchronisation in OOFDMA PONs. Extensive investigations are currently being undertaken in our research group to implement the proposed synchronisation technique in OOFDMA PONs with practical optical power budgets.

Acknowledgments