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A roll-to-roll compatible vacuum-evaporation route to organic circuit production

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A Roll-to-roll Compatible Vacuum-evaporation Route to Organic Circuit Production

By

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Papers:

[1] D. M. Taylor, A. Williams, E. R. Patchett, G. Abbas, Z. Ding, H. Assender, J. J. Morrison, S. G. Yates, "Simulating the Electrical Characteristics of Organic TFTs Prepared by Vacuum Processing", *Journal of Display Technology*, **9**, 877-882, 2013

[2] E. R. Patchett, A. Williams, Z. Ding, G. A. W. Abbas, H. Assender, J. J. Morrison, S. G. Yates, D. M. Taylor, "A high-yield vacuum-evaporation-based R2R-compatible fabrication route for organic electronic circuits", *Organic Electronics*, **15**, 1493-1502, 2014

[3] G. A. Abbas, Z. Ding, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett, D. M. Taylor, "A High-Yielding Evaporation-Based Process for Organic Transistors Based on the Semiconductor DNTT" – (re-submitted)

[4] D. M. Taylor, E. R. Patchett, A. Williams, N. J. Neto, Z. Ding, H. Assender, J. J. Morrison, S. G. Yates, "Organic Digital Logic and Analog Circuits Fabricated in a Roll-to-Roll Compatible Vacuum Evaporation Process" – (submitted)

[5] Z. Ding, G. A. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett, D. M. Taylor, "Effect of oxygen, moisture and illumination on the stability of dinaptho[2,3-b:2',3'-f]thieno[3,2-b]thiophene OTFTs during operation and storage" – (In preparation)

Poster Presentations:

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Poster Presented: A Vacuum Approach to Roll-to-roll Production of Organic Electronics Giving 100% Yield

Abstract

The properties of organic electronics allow them to be processed at low temperatures onto flexible substrates, opening up a new and novel field of low-cost high throughput electronics. Up to date, research into the roll-to-roll printing of electronics has concentrated on the use of solution based methods for the deposition of material. That is, the use of solvents, which presents a number of problems. Here the methods used for the deposition of materials were compatible with vacuum deposition processes, avoiding the problems that are encountered with the use of solvents.

First transistors were fabricated using naphtho[2,3-b]naphtho[2′,3′:4,5]thieno[2,3-d]thiophene (DNTT) semiconductor on Si/SiO_2 substrates to determine if recrystallization alone was a suitable method for the purification of DNTT when compared to sublimation. It was found by transistor transfer measurements that although recrystallized DNTT gave a larger spread in mobilities than sublimated DNTT, it had a higher average saturation mobility, 0.54 cm^2/Vs compared to 0.36 cm^2/Vs.

Two transistor configurations were then investigated on poly(ethylene 2,6-naphthalate) (PEN) substrates with polystyrene (PS) dielectric and recrystallized DNTT semiconductor. The performance of top-gate-bottom-contact (TGBC) and bottom-gate-top-contact (BGTC) transistors was evaluated by output and transfer measurements. It was found that the mobilities of the BGTC transistors were significantly higher, an average of 1.01 cm^2/Vs in the linear regime and 0.97 cm^2/Vs in the saturation regime, than those of the TGBC transistors, ~0.05 cm^2/Vs in the linear regime and ~0.016 cm^2/Vs in the saturation regime. However, despite the high mobility the transistor yield was unacceptably low, at best ~ 65 %. Although the mobilities of the TGBC transistors were relatively low, it was still possible using that configuration to fabricate inverters that had a gain in excess of 1 for a number of rail voltages, (-60 V, -40 V, -20 V = V_{DD}).

BGTC Transistors were then fabricated on tri(propylene glycol) diacrylate (TPGDA) dielectric with recrystallized DNTT semiconductor. The average mobility in the saturation regime was found to be 0.44 cm^2/Vs, lower than for the PS dielectric transistors, and had a dependence on channel width, W, due to device design. However, the device yield was 89%, an improvement on the solution processed device yield. Although the device yield was good, the stability of the devices made it difficult to fabricate inverters with stable operation. Due to the device instability it was not feasible to fabricate more complicated devices.

By using a PS buffer layer to improve the surface of TPGDA, transistors with an average saturation mobility of 1.51 cm^2/Vs were fabricated with a yield of 90%. Here again the mobility was shown to be W dependent, although not to the same degree as for TPGDA/DNTT transistors. Transistors that had been stored under lab conditions for six months in the dark were shown to still have good mobility and stable device operation with no hysteresis. Using the same device configuration it was possible to fabricate working, stable inverters with high switching speeds with total rise and fall times of less than 1 ms. Ring oscillators were also fabricated with output frequencies in the low KHz range, in excess of previously published R2R printed ring oscillators. Functioning NAND and NOR gates were also fabricated with similar switching speeds as the inverters. Finally, a working fully-integrated NAND-based SR Flip-flop gate was also fabricated.

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Chapter 1

Introduction

1.1 Introduction

Electronic devices are undeniably an important part of modern day life. Over the last two decades the personal computer has become essential for work and for school, for adults and children alike. A significant proportion of the population would not walk out of the house without a phone in their pocket, and a number find it to be an indispensable tool. More recently such appliances have almost become fashion accessories with a number of modern devices such as tablets combining the features of several different appliances. Industry is currently trying to look at new areas where electronic technology can be adapted. An area that is generating considerable interest is foldable displays [1], with a number of prototypes having been produced. Another example is wearable electronics [2,3], where everyday clothes can harvest energy through the use of organic photovoltaics (OPVs) [4], and store that energy in batteries that are also a flexible woven part the clothing [5].

One of the drawbacks of current technology is the reliance on rigid silicon chips that are produced in batches at a high cost. It means that it can be prohibitively expensive to produce single-use disposable electronics. Products such as displays can only be produced on single pieces of glass at a time, this also limits display size and restricts the display to rigid applications. Concepts such as foldable displays and wearable electronics cannot be produced with such technology. There is a need for new technology where the microelectronics can be flexed without damaging their properties. This would allow such electronics to be produced in a roll-to-roll system, increasing throughput and reducing cost.

Organic semiconductors have lower processing temperatures than their inorganic counterparts. This allows them to be deposited onto flexible substrates that can pass through a roll-to-roll (R2R) system. Although organic semiconductor mobilities are comparatively much lower than the mobilities of inorganics, the idea is not to directly compete with inorganic electronics, but to open up the market for cheap and disposable electronics. Applications for such electronics could include smart

packaging, smart magazines, large area displays and RFID tags. Organic materials are already prevalent in commercial products, particularly display technology. Television and mobile phone displays have already been manufactured that feature organic light emitting diodes (OLEDs).

Currently research into the printing methods for depositing organic materials onto substrates rely heavily on the use of solvents. The solvent acts as a carrier, depositing the organic material onto the substrate as it evaporates away. However, this can lead to several problems that can result in processing bottlenecks and poor device properties.

1. Although the solvent evaporates to leave a film of material behind, a certain amount of that solvent will remain trapped within the deposited film. This makes it necessary to anneal the films to remove excess solvent, adding time and heating costs to the production process.
2. For a good dielectric to be formed it needs to be pinhole free. Evaporation of solvents can leave pinholes in the deposited films that annealing may not completely remove.
3. Solvents have to be carefully selected; when the same solvent is used for sequential layers the previously deposited layer will be removed or damaged. This makes it necessary to have orthogonal solvents. There is also the problem of some semiconductors being highly sensitive to solvents. Semiconductors can be damaged regardless of solubility in the solvent used.
4. Solvents tend to be harmful to the environment and can also lead to health and safety issues. Therefore waste solvent capture systems would be an additional but essential cost to a production system.

An alternative route to the R2R production of electronics would be a vacuum deposition approach. Metallisation of polyethylene terephthalate (PET) film is already a commercial process [6], and has been used to pattern antennas. It has also been shown that it is possible to pattern capacitors using the metallisation technique in combination with diffusion pump oil in a process similar to lift-off patterning [6]. Transparent barrier layers have also been deposited using the technique, showing that it may be possible to pattern dielectric layers in this way. Many small molecule semiconductors are already deposited under vacuum in laboratory conditions.

In the work to be reported here, R2R compatible vacuum deposition methods will be used to fabricate transistors, and further devices, to demonstrate the suitability of a vacuum 2R2 process as an alternative to conventional R2R printing techniques.

1.2 Thesis Outline

The theoretical background of the work is presented in Chapter 2, which also provides an introduction to how values such as carrier mobility and device capacitance were calculated. The current research in the area of R2R organic electronics is also reviewed.

The experimental methods are given in detail in Chapter 3, together with a list of the fabrication materials that are used – aluminium, gold, tri(propylene glycol) diacrylate (TPGDA), polystyrene (PS) and naphtho[2,3-b]naphtho[2′,3′:4,5]thieno[2,3-d]thiophene (DNTT).

Experimental results for transistors fabricated from different samples of DNTT on SiO_2 substrates are presented in Chapter 4. The results are used to determine whether recrystallization is a suitable purification method for DNTT when compared against the more conventional method of sublimation.

In Chapter 5 experimental results for DNTT transistors on a polystyrene dielectric are presented. Here also the characteristics of bottom-gate and top-gate transistors are investigated to determine the best configuration for transistor fabrication. The work here was also used to demonstrate the failing of solution processing in terms of device yield.

All-evaporated transistor experimental results are presented in Chapter 6. Here, for the first time in this work, only vacuum R2R techniques were used to fabricate transistors. This work was undertaken to demonstrate the high transistor yield of the fabrication processes used.

In Chapter 7, results are presented for transistors fabricated on a polystyrene (PS) buffered dielectric. It also contains experimental results for inverters and ring oscillators. Work here was undertaken to demonstrate the true capability of the vacuum R2R processes.

Experimental results for logic devices fabricated using the same techniques as for the transistors in Chapter 7 are presented in Chapter 8. This work was undertaken to further demonstrate the capability of the vacuum R2R compatible processes.

The conclusions from this work are presented in Chapter 9, together with ideas for further work in pursuit of an all-evaporated R2R system for the production of electronics.

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Chapter 2

Background Concepts and Literature Review

This chapter covers the background theory underpinning organic semiconductors, including bond hybridisation and band bending. A review of a small part of the large volume of literature on organic thin film transistors (OTFTs) is presented. The operation of the OTFT is explained, and the equations for device mobility presented. Transistor-based devices such as inverters, logic gates and ring oscillators are discussed, and their operation explained. Finally, printing techniques adapted for the R2R printing of organic electronic circuits are discussed, as well as the developments in R2R printing research.

2.1 Organic Semiconductors

2.1.1 Introduction

Semiconductors are materials whose conductivity lies between those of conductors and insulators. Their conductivity can be controlled by the application of external agents such as dopants, light or an electric field. Instead of having a continuous band where there are numerous energy states as in conductors, there are some energy levels that cannot be occupied. Instead energy levels exist in a density of states (DoS) for both the valence and conduction bands. Organic semiconductors are often described as having exponential or Gaussian DoS, in contrast to the parabolic DoS found in inorganic semiconductors such as silicon. Crystalline inorganic semiconductors display a gap between valence and conduction band energies. It is the magnitude of the band gap that differentiates a semiconductor from an insulator and determines the semiconductor properties. The band gap for a semiconductor can be anywhere from >0 eV up to ~ 4 eV.

Investigations into the conducting and semiconducting properties of organic materials were taking place as early as the 1950s and 1960s, of which references [1-4] are just some examples. Presently there are a multitude of different organic semiconductors that fit into one of four groups, polymers, oligomers, small molecules and small

molecule blends. To date however, an organic semiconductor with mobility matching the semiconducting properties of single crystal inorganic semiconductors is yet to be discovered. Although organic semiconductors cannot currently match the performance of inorganic single crystals, they can however, be processed at low temperatures allowing them to be deposited onto flexible plastic substrates. This opens up a novel field in electronics for cheap to produce and relatively robust electronic circuits.

2.1.2 Bond Hybridisation

For an element to be in its most stable state it requires a full outer valence shell of eight electrons, the Noble gas configuration. This can be achieved by the loss or gain of electrons to form ionic species, or by the sharing of electrons in a covelant bond. The electronic configuration of a carbon atom is $1s^2 2s^2 2p^2$. The $2s$ and $2p$ orbital electrons are valence electrons and take part in chemical bonding. A p orbital is divided into three separate orbitals, $2p_x$, $2p_y$ and $2p_z$, and each orbital can contain a pair of electrons. In its ground state carbon has four electrons occupying the valence orbitals. As $2s$ is lower in energy it is filled first with two electrons, then a single electron occupies each of the $2p_x$ and $2p_y$ orbitals and $2p_z$ is empty as shown in Figure 2.1.

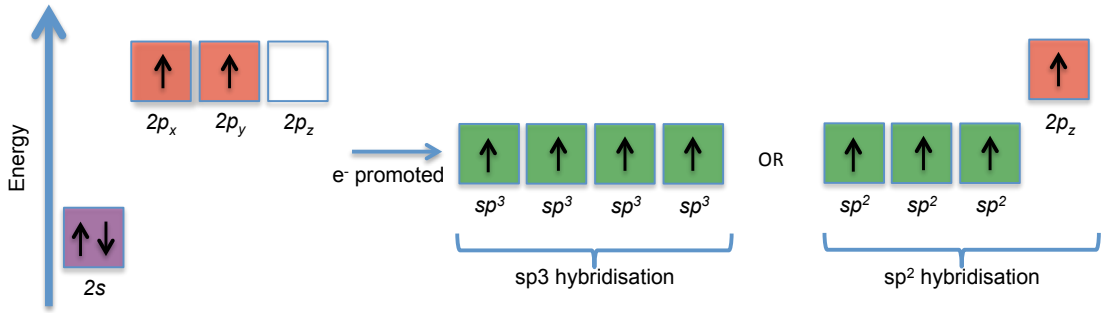


Figure 2.1 A simple representation of the energy differences between orbitals and the hybridized orbitals of sp^3 and sp^2. It is also possible to have sp^1 hybridization in the case of triple bonds. Adapted from [5].

An excitation of a single electron from the $2s$ orbital to the $2p_z$ orbital results in sp^3 hybridisation (1 s orbital and 3 p orbitals) i.e. four single electrons of equal energy available for covalent bonding. This occurs in molecules such as methane where the s orbitals of four hydrogen atoms overlap with the four hybridised sp^3 orbitals of a

carbon atom forming four σ bonds in a tetrahedral configuration completing the outer shell of the carbon and hydrogen atoms. In ethene the same process occurs, however the $2p_z$ orbital remains at a higher energy level compared to the *sp* hybridised orbitals, resulting in sp^2 hybridization as shown in Figure 2.1.

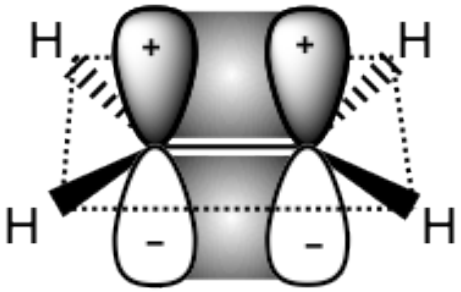


Figure 2.2 An ethene molecule showing the overlap of the p_z orbitals that form the π orbital. Adapted from [5]

In ethene three σ bonds are formed between the overlap of the sp^2 hybridised orbitals of the carbon atom with the *s* orbitals of two hydrogen atoms and an *sp* hybridized orbital of an adjacent carbon atom. All of the σ bonds lie in a single plane with all bond angles equal to 120^0, as can be seen in Figure 2.2. A fourth weaker bond, the π bond, is formed between the overlap of the $2p_z$ orbitals of the adjacent carbon atoms on a vertical axis to the plane of the σ bonds.

The π bond is split into a low energy in-phase π molecular orbital (bonding) and a high energy out-of-phase π* molecular orbital (anti-bonding) (Figure 2.3). Bonding orbitals are more stable, the electron density between adjacent atoms is higher and as the electron pair is shared the outer shell of each carbon atom is complete. For anti-bonding orbitals the opposite is true and can lead to repulsion between individual atoms.

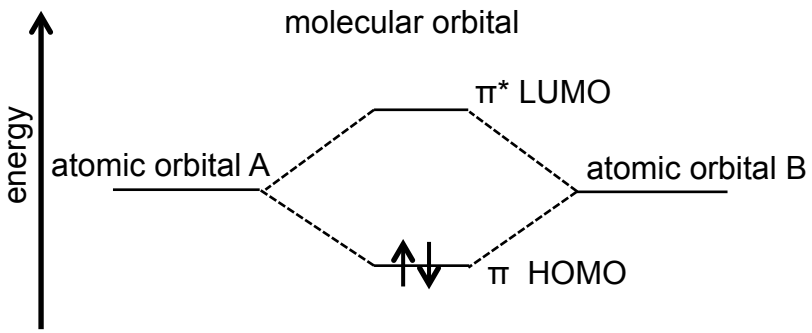


Figure 2.3 Energy levels split into a lower energy occupied HOMO level, and higher energy unoccupied LUMO level. Adapted from [5]

A conjugated system is recognised as a region of alternating single and double bonds between carbon atoms, which can also include lone pair electrons, leading to delocalisation of π electrons. When a molecule has bond conjugation, and there are numerous π bonds, there is an interaction between the $2p_z$ orbitals of all of the conjugated carbon molecules that is dependent on the phases of the *p* orbitals. Due to the number of combinations of bond phases the discrete energy levels observed in Figure 2.3 appear to become continuous and a band of states is formed. A band gap is formed between the highest occupied molecular orbital (HOMO) (the highest energy level of the valence band in inorganic semiconductors) and the lowest unoccupied molecular orbital (LUMO) (the lowest energy level of the conduction band). Between these two energy levels there are no allowed energy states, so there are two bands of states separated by a band gap similar to energy bands observed in inorganic semiconductors. However, the two energy bands are not continuous, and the energy levels occupy a Gaussian DoS.

Benzene is a cyclic molecule of six carbon atoms, each bonded to its neighbour by a single σ bond. In addition to the σ bond, each carbon has an un-hybridised $2p_z$ orbital perpendicular to the plane of the molecule containing a single electron. The overlap of the six $2p_z$ orbitals forms a delocalised electronic ring above and below the plane of the molecule. When all six $2p_z$ orbitals are in phase the bonding between each atom is of an equal length. Any out of phase $2p_z$ orbitals will cause anti-bonding interactions and increase the energy of the system. Multiple benzene rings in a single system increases the conjugation and the number of bonding/anti-bonding orbitals, in turn increasing the number of energy levels within a band of states due to the number of resulting bonding/anti-bonding combinations seen in many organic semiconductors.

2.1.3 Energy Bands and Band Bending

An intrinsic semiconductor (there are no dopants or defects) is described as having an intrinsic Fermi level, E_i, near to the centre of the forbidden energy gap. The position of the Fermi level relative to the conduction and valence bands can be altered by dopant atoms and determines whether the semiconductor is a p-type or an n-type semiconductor.

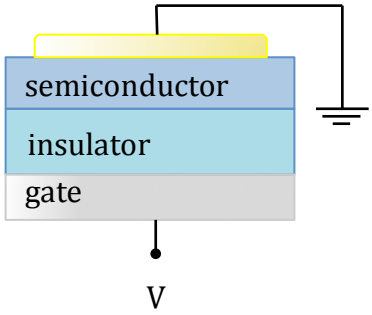


Figure 2.4 Schematic cross-section representation of an MIS capacitor.

As discussed above bond conjugation leads to a description of an organic semiconductor in terms of energy bands. Figure 2.5 shows the equilibrium band diagram of an ideal metal-insulator-semiconductor (MIS) structure based on a p-type semiconductor, with no applied voltage. (The schematic for such a device is shown in Figure 2.4.) This is recognised as the flatband condition, as there is no band-bending in the semiconductor.

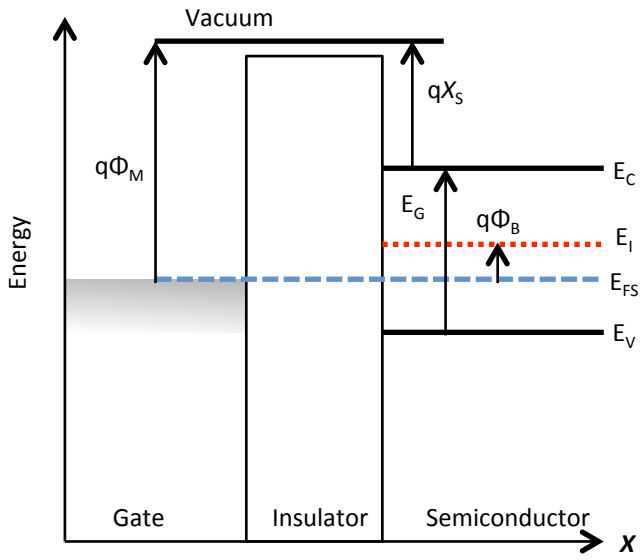


Figure 2.5 The energy levels under flatband conditions. Adapted from [6]

Under flatband conditions the materials are in thermal equilibrium, and the Fermi level (E_{FS}) of the semiconductor matches the work function (Φ_M) of the metal gate. The band gap that is formed between the valence electrons (E_V) (corresponding to the HOMO level) and the conduction electrons (E_C) (corresponding to the LUMO level) as described earlier in section 2.1.3, is shown here as E_G with q the absolute electron charge.

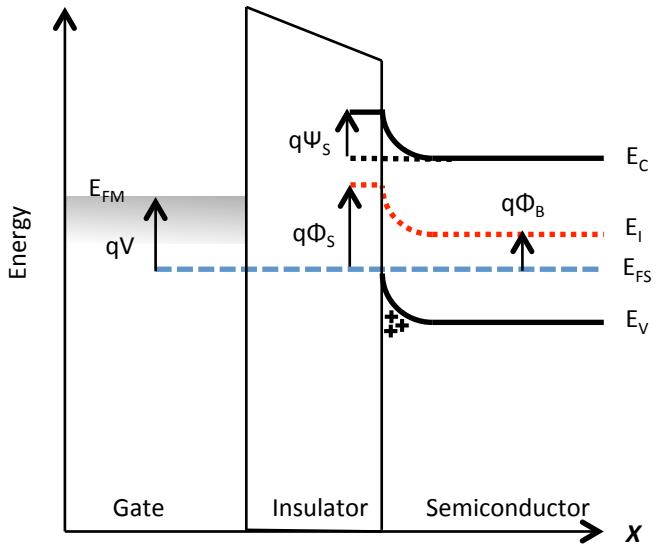


Figure 2.6 Band bending showing accumulation of charge carriers. Adapted from [6]

By applying a negative potential V to the gate (where E_{FM} is the Fermi level of the metal), the band edges at the semiconductor surface are bent upwards, bringing the valence band edge closer to the semiconductor Fermi level, E_{FS}, as shown in Figure 2.6.

As a result of the band bending there is an exponential accumulation of majority charge carriers (in the case of p-type semiconductors they are holes) at the surface. As a result, a conduction channel is formed at the insulator/semiconductor interface screening the bulk from the electric field generated by the gate. The distance x, perpendicular to the interface, that the band bending extends into the semiconductor bulk is dependent on the magnitude of the gate voltage. The more negative the voltage applied, the greater the degree of band bending. φ_S is the difference in potential energy between E_i and E_{FS} at the interface, and φ_B is the difference in the bulk semiconductor. ψ_S is a measure of the band bending, the potential difference of the surface with respect to the bulk, being the potential difference between φ_S and φ_B. Band bending extends perpendicularly from the interface into the bulk semiconductor with the potential $\psi_{(X)}$ at x given by

$$\psi(x) = \phi(x) - \phi_B \tag{2.1}$$

where $\varphi(x)$ is the difference in energy between E_i and E_{FS} at x. The number of majority charge carriers decreases exponentially from the interface. The hole concentration $p(x)$ at x is then given by

$$p(x) = N_A exp\left[-\frac{q\psi(x)}{kT}\right] \quad (2.2)$$

where N_A is the density of acceptors, k is Boltzmann's constant and T is the absolute temperature.

If a positive voltage is applied to the gate electrode then the band edges are bent downwards, increasing the energy difference between the valence band and E_{FS}. For a p-type semiconductor this causes a depletion of holes at the interface as seen in Figure 2.7.

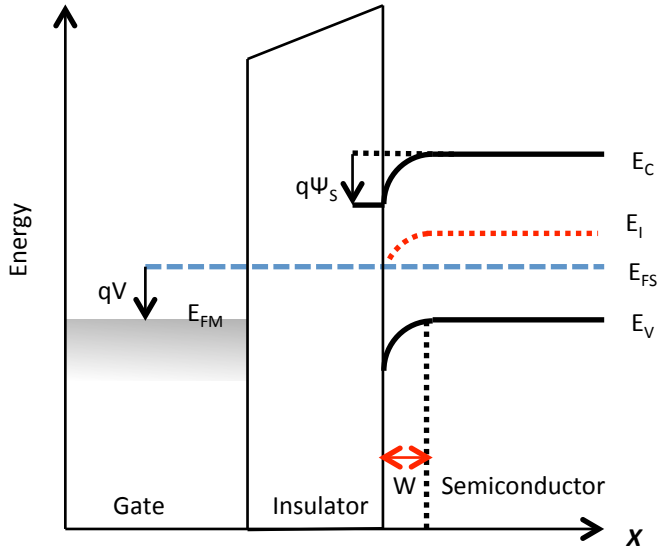


Figure 2.7 Band bending showing the creation of a depletion layer. Adapted from [6]

Now immobile negatively charged acceptor ions maintain charge neutrality at the interface. As the voltage on the gate becomes more positive the width W of the depletion region increases in order to maintain charge neutrality.

For sufficiently large applied voltages, band bending in *inorganic* semiconductors can be sufficient to cause a state of inversion. This does not commonly occur in organic semiconductors and is therefore not discussed here.

2.1.4 MIS Capacitors

A metal-insulator-semiconductor (MIS) capacitor is constructed from two parallel conductive plates separated by an insulating dielectric layer and a semiconductor layer, the schematic of which is shown in Figure 2.4. The state of the semiconductor/dielectric interface is determined by the voltage applied to the metal gate contact as detailed in the previous section. This also alters the capacitance of the

device. When the semiconductor is in accumulation it does not contribute to the capacitance. It simply provides carriers to charge the semiconductor/dielectric interface. When the semiconductor is in depletion then it acts as an additional capacitor in series with the capacitance of the dielectric layer, decreasing the total capacitance of the device.

By conducting capacitance vs voltage measurements (C-V) it is possible to observe the voltage at which the semiconductor changes its state from accumulation to depletion. For a p-type semiconductor when a sufficiently negative gate voltage is applied to the gate, then the semiconductor is in accumulation.

It will then transition to depletion as the applied voltage becomes more positive to a point where the layer is completely depleted of charge carriers usually at +ve voltages. This gives two relatively flat areas to a plot of C vs V where the low capacitance is the capacitance of the semiconductor and insulator in series, and the high capacitance is the capacitance of the insulator alone.

The response of the semiconductor can be measured also in capacitance vs frequency (C-*f*) measurements. When a negative voltage is applied to the gate of a capacitor with a p-type semiconductor layer during such a measurement, the charge carriers respond to the a.c. signal so that the measured capacitance is that of the insulator. As frequency increases generally fewer charge carriers will be able to respond, so that the semiconductor behaves more like an insulator. The measured capacitance will then decrease as the overall capacitance becomes that of the semiconductor and insulator in series. This is an example of the so-called Maxwell-Wagner effect.

In real MIS devices the insulator itself can also respond to the changing frequency. Polarisable molecules within the dielectric orientate within the field, and have an associated response time. There can also be migrating species such as H_2O trapped within the dielectric. The higher the frequency, the less time these molecules have to respond and orientate in the field, so the frequency response of the polarisable molecules can also be observed as a drop in the capacitance in a C-*f* measurement.

2.1.5 Role of Dopants

When dopants are introduced into the semiconductor they create energy states within the band gap of the semiconductor. For p-type semiconductors the dopants act as

electron acceptors. The energy required to promote electrons from the valence band to higher energy states is reduced. When this occurs holes are generated in the valence band that can contribute to conduction. This process is shown in Figure 2.8. Electrons in an adjacent state diffuse/tunnel into the hole state, resulting in the hole moving in the opposite direction.

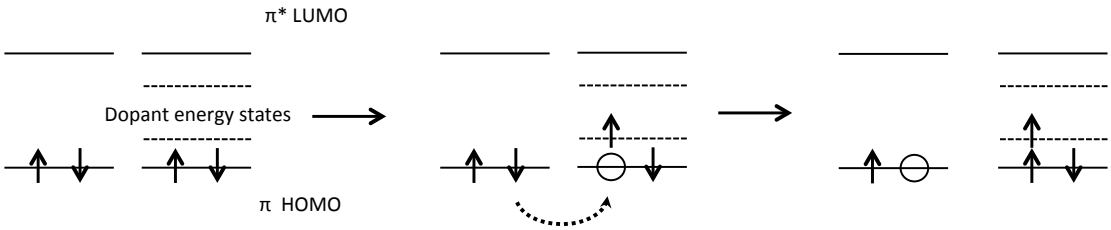


Figure 2.5 Doping of an organic semiconductor. Adapted from [7]

It is easy then to see how dopants can increase the number of charge carriers available. However, unlike inorganic semiconductors where doping is controlled, doping in organic semiconductors is difficult to manipulate and can lead to device instability.

2.1.6 Charge Trapping

A limitation on charge transport and device operation is charge trapping. Charge traps can also lead to device instability, and can be observed in the form of measurement hysteresis and threshold voltage shifting in OTFTs. Localized defects in crystal structure were studied in detail by Podzorov *et al*. [8]. Here deep traps in the form of crystal defects were created deliberately by changing the structure of a rubrene single crystal using x-rays. It was shown that deep traps only affect the threshold voltage, and were not detrimental to device mobility above the threshold voltage. It was shown in [9] that oxygen can act as a source of deep traps and that such traps do lead to a reduction in mobility for a corresponding gate voltage. It is discussed that the degradation mechanism is dominated by an oxygen related defect. This defect is likely to be pentacenequinone, a product of the oxidation of pentacene, which does not contribute to charge transport. So when exposed to oxygen it is likely that the pentacene is oxidised leading to a reduction in free charge carriers and, therefore, a reduction in mobility. The creation of charge traps due to oxygen exposure was also shown to occur in rubrene single crystals in [10]. Here again it was stated that the charge traps are likely due to the reaction of oxygen with the rubrene molecules.

Molecules that do not support charge transport will act as scattering centres around which free charges must be transported.

If charge trapping occurs at the surface of the dielectric, then it is easy to see how this can shift the threshold voltage. If holes are trapped at the surface, then they will repulse free holes from the interface. Thus, a more negative gate voltage is required to attract the same number of charge carriers as previously. If the traps fill gradually during a measurement of the transistor and do not de-trap then this will be observed as hysteresis, and there will be an obvious threshold voltage shift. Charge trapping should not therefore have a bearing on the maximum mobility if all the traps are filled, only the V_G to which the maximum mobility corresponds.

2.1.7 Charge Transport in Organic Semiconductors

We have seen how bands are formed in organic semiconductors, and how the energy of those bands near the interface can be manipulated. In this section, we will now consider how charge is transported in the semiconductor. Charge transport models have been largely based on inorganic semiconductors, where transport occurs in delocalized states. In those materials, the limitations to transport arise from phonons and impurities within the crystal lattice. However, due to the disorder in the crystal structure of organic semiconductors, and in some cases the amorphous nature of the material, conventional charge transport as observed in crystalline semiconductors cannot be used to explain the charge transport in organics. Instead charge transport occurs through phonon-assisted hopping between localised states. Therefore, in contrast to inorganic semiconductors, as temperature and hence lattice energy increases mobility increases, see for example Brown *et al*. in [11].

In the multiple trapping and release (MTR) model, charge carriers are transported through a narrow delocalised band under the influence of an applied electric field. As the charge carriers are transported they interact with lower lying localised energy levels that act as traps. The carriers are then thermally promoted back to the delocalised band, from which they will become trapped again.

The strong localisation of charge carriers associated with amorphous organic films was cited as the reason that the MTR theory could not apply. Instead Vissenberg and Matters proposed a model that charge transport is governed by hopping between localised states rather than by thermal activation of charge carriers from localised

states to a delocalised band [12]. Hopping is also referred to as thermally activated tunnelling between localised states, where a carrier can hop over a short distance with high activation energy or over a long distance with low activation energy.

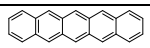
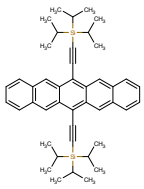
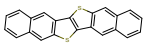
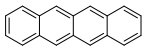
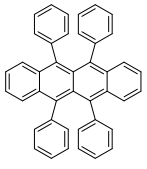
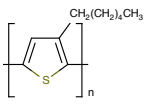
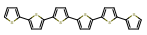
In organic transistors mobility dependence on gate voltage is explained by the increasing concentration of charge carries in the accumulation layer. Initially the lower energy states will be occupied, then higher energy states as V_G increases. The charge carriers occupying the higher energy states will have smaller activation energy to overcome to hop to a neighbouring site and will, as a result, have a higher mobility. This explains why mobility increases with increasing V_G.

True charge transport in organic semiconductors is likely to be a combination of the models detailed.

2.1.8 Organic Semiconductors

A number of different types of semiconductors have been studied. Polymers, oligomers, small molecules, blends and single crystals. All these semiconductor materials display bond conjugation to some degree, as described in section 2.1.3.

Table 2.1 The HOMO and LUMO levels of some common organic semiconductors

Semiconductor	Structure	HOMO (eV)	LUMO (eV)	Gap (eV)	Type	Ref
Pentacene		-4.96	-2.67	2.29	SM	[13]
TIPS-Pentacene		-5.08	-3.07	2.01	SM	[13]
DNTT		-5.19	-1.81	3.38	SM	[14]
Tetracene		-4.87	-2.09	2.78	SM	[15]
Rubrene		-4.69	-2.09	2.60	SM	[15]
P3HT		-5.20	-3.34	1.86	Polymer	[16]
EHP-PPV	-	-4.88	-2.60	2.28	Polymer	[17]
α-Sexithiophene		-5.48	-3.00	2.48	Oligomer	[18]

For polymers and oligomers the HOMO and LUMO energy levels can vary depending on the number of repeat units and side chains. This also means that the band gap can vary for the same material. For small molecules the HOMO and LUMO energy levels are fixed as there is no difference in the size of the molecule. Table 2.1 gives a brief overview of the HOMO and LUMO levels of some commonly used organic semiconductors. The semiconductors shown here typically display p-type behaviour. Therefore the energy level of the HOMO is important, as it is the energy band that holes will be injected into. All of the semiconductors have a band gap of less than 4 eV. Choosing a contact material is important, as if one is chosen to match the HOMO level then it is likely not to match the LUMO level. In terms of p-type semiconductors a contact material with workfunction, φ_M, matching the HOMO energy level is essential. Thus the Fermi level of gold, -5.53 eV, makes it a suitable contact material for a number of p-type semiconductors as can be seen in table 2.1.

2.2 Organic Thin Film Transistors

2.2.1 Introduction

Shockley, Bardeen and Brattain fabricated the first transistor in polycrystalline germanium at Bell Labs in 1947 [19]. By 1949 single-crystal material replaced polycrystalline and resulted in significantly improved transistor performance [20]. The first integrated circuit was demonstrated by Jack Kilby in 1958 based on bipolar transistors, with metal oxide semiconductor (MOS) transistors being developed during the 1960s [21-26]. Modern technology depends heavily on MOS transistor based integrated circuits, with some graphics cards composed of over 12 million transistors per mm^2.

The first organic thin film transistor (OTFT) was fabricated in 1987 [27] utilising a polythiophene semiconductor. Since then numerous organic materials have been used to fabricate transistors with varying degrees of success, the early development of which has been reviewed in detail by Dimitriakopoulos and Mascaro [28].

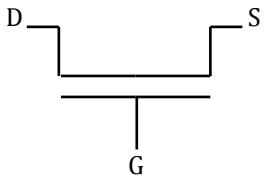


Figure 2.6 A circuit representation of a field effect transistor

Essentially, the OTFT is similar to the familiar MOS field effect transistor (MOSFET). Instead of a single plate in contact with the semiconductor there are two contacts. Figure 2.9 shows the circuit diagram of a simple three contact transistor. The gate (G) controls the conductivity of the semiconductor between the source (S) and drain (D) contacts. By applying a negative voltage to the gate of a p-type device, hole charge carriers accumulate at the interface of the dielectric/semiconductor. A conductive channel is formed at the interface between the source and drain electrodes, and when an electric field is applied between the source and drain, holes will be injected at S and withdrawn at D. In the case of p-type semiconductors charge transport occurs in the valence band that corresponds to the HOMO level. The φ_M of the contact needs to be as closely matched as possible to the HOMO level of the semiconductor, the greater the difference in the energy levels the higher the barrier to charge injection. If the energy barrier between the two materials is too large then no charge injection will occur. This is why selection of the contact material can be crucial. However, it is possible in some cases to modify the interface between the contact and the semiconductor to reduce the barrier and increase charge transfer [29-31].

2.2.2 The Gradual Channel Approximation and Mobility Equations

Although an OTFT operates in accumulation, the equations describing its operation are based on those initially derived for a MOSFET, which operates in inversion. In a p-channel OTFT, the device current is carried by mobile holes that have been accumulated at the semiconductor interface by the application of a negative gate voltage as shown in Figure 2.10. As the conducting channel of a transistor is only a few nanometres thick the potential in the vertical *y* direction is assumed constant.

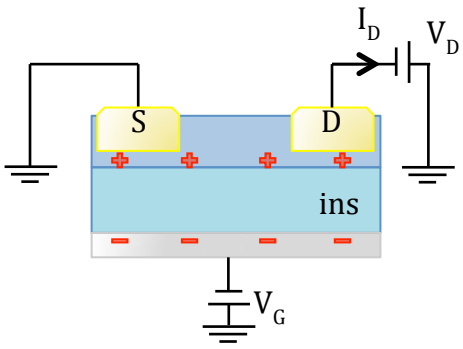


Figure 2.7 A schematic cross-section of an organic thin film transistor in accumulation, showing the formation of an accumulation channel between the source and drain electrodes.

By applying a negative voltage V_D at the drain holes flow from S to D giving rise to the device current I_D. If V_D = 0 V, then the charge density $Q(x)$ in the channel at a point x (from S towards D) is given by

$$Q(x) = C_i(V_G - V_T). \tag{2.3}$$

Here C_i is the capacitance per unit area and V_T is the threshold voltage. When a non zero V_D is applied to D the accumulation layer potential changes along the channel so that

$$Q(x) = C_i((V_G - V_T) - V(x)). \tag{2.4}$$

Changes in $Q(x)$ caused by changes in V_G (produces an electric field normal to the channel) can be treated independently of current flow induced by V_D (producing an electric field along the channel) this is the basis of the gradual channel approximation.

The current $I(x)$ at x is equal to the device current, I_D and given by

$$I_D = [-WC_i((V_G - V_T) - V(x))](\mu E) \tag{2.5}$$

where W is the width of the conducting channel. The electric field $E = -\frac{dV}{dx}$, so equation (2.5) can be re-written as

$$I_D = \mu C_i W((V_G - V_T) - V(x))\frac{dV}{dx}. \tag{2.6}$$

Integrating equation (2.4) from source to drain i.e.

$$\int_0^L I_D dx = \int_0^{V_D} \mu C_i W((V_G - V_T) - V(x))dV \tag{2.7}$$

where L is the channel length (distance between source and drain) then yields

$$I_D = \mu C_i \frac{W}{L}((V_G - V_T) - \frac{V_D}{2})V_D = \mu C_i \frac{W}{L}((V_G - V_T)V_D - \frac{V_D^2}{2}). \quad (2.8)$$

For $V_D << V_G$ the quadratic term in equation 2.8 can be ignored, leading to the equation describing the linear regime of the OTFT

$$I_D = \mu C_i \frac{W}{L}(V_G - V_T)V_D. \quad (2.9)$$

The ratio W/L is known as the aspect ratio of the device. It defines the geometry of the channel and can be used to control its trans-conductance $\frac{dI_D}{dV_G} = \frac{W}{L}\mu C_i V_D$. When $V_D \geq (V_G\text{-}V_T)$ the voltage drop across the insulator is insufficient to accumulate charge near the drain, and further increase in V_D does not result in an increase in I_D. This is where channel pinch off occurs and the current is said to enter saturation. In the saturation region it may be assumed that $V_D = (V_G - V_T)$, so that equation (2.8) reduces to

$$I_D = \mu C_I \frac{W}{2L}(V_G - V_T)^2. \quad (2.10)$$

As shown in Figure 2.11 there are four possible configurations for OTFTs, top-gate-top-contact (TGTC), top-gate-bottom-contact (TGBC), bottom-gate-top-contact (BGTC) and bottom-gate-bottom-contact (BGBC). There are advantages and disadvantages for all configurations depending on materials and processes.

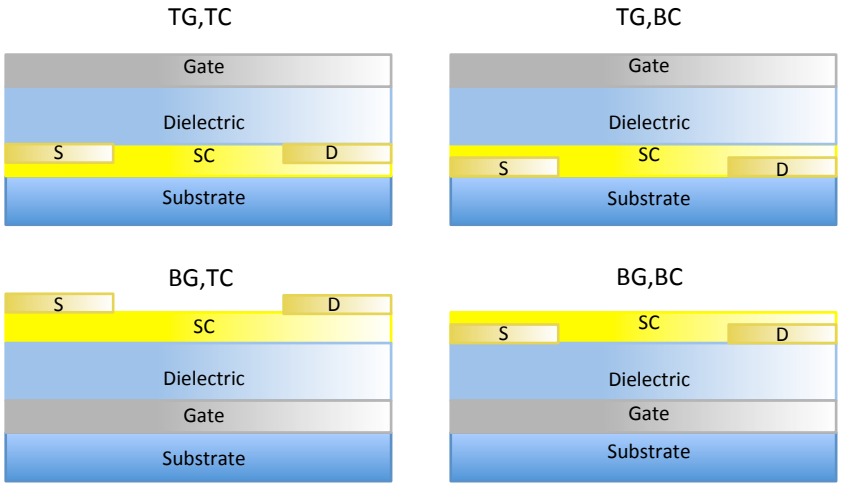


Figure 2.8 Schematic representations of the four basic configurations possible for organic thin film transistors.

One of the main differences in device performance comes from the location of the S and D electrodes in relation to the semiconductor/insulator surface. A configuration where the S and D surface are in direct contact with the dielectric (TGTC and BGBC)

reduces the area for charge injection. This increases contact resistance and reduces the effective mobility [32-34].

The difference in the performance of BG and TG transistors is dependent on the materials used for the dielectric and semiconductor. This is due to the roughness of the interface of the two materials being dependent on which is deposited first. Ideally the interface should be as smooth as possible, so if the semiconductor has a smoother surface than the dielectric it should be deposited first, so the device would be a TG transistor. However, there are other concerns. Many organic dielectrics require UV curing to form polymers. The UV curing process can be detrimental to the semiconductor layer, in such cases it is necessary to deposit the dielectric first. This restricts such dielectric/semiconductor combinations to the BG configuration.

2.2.3 Characterisation of OTFTs

The performance of a transistor is described by its output (I_D vs V_D) and transfer (I_D vs V_G) characteristics. Examples of such plots obtained in the present work are given in Figure 2.12.

In an ideal transistor, the output plots should all pass through the origin, displaying a V_G dependent linear region at low V_D and good saturation at high V_D as seen in Figure 2.12 (a). In some cases there will be an upward curve to the linear region indicating a diode-like contact resistance. If there is an ohmic contact resistance the linear region of the plots will appear to merge as V_G increases due to a limitation on charge injection, the saturation region then peeling off at higher I_D for increasing V_G.By plotting I_D vs V_G for the linear and $I_D^{1/2}$ vs V_G for the saturation regimes as in Figure 2.12 (b), V_T can be estimated from the intercepts of the tangents (dashed lines) of the respective slopes with the axis of V_G. If C_i, W and L are known then from these plots it is possible to extract the linear and saturation mobilities of the semiconductor using equations (2.9) and (2.10).

From Figure 2.12 (c) it is possible to determine the I_{ON}/I_{OFF} ratio; it is taken as the ratio of the on I_D to the off I_D, and is usually expressed in powers of 10. The subthreshold slope is the gradient of the slope immediately after the switch on voltage V_{ON}. The units are conventionally given as V per decade. The gate leakage current, I_G, also shown in Figure 2.12 (c) gives an indication as to what proportion of I_D is contributed by I_G and hence how good the dielectric is.

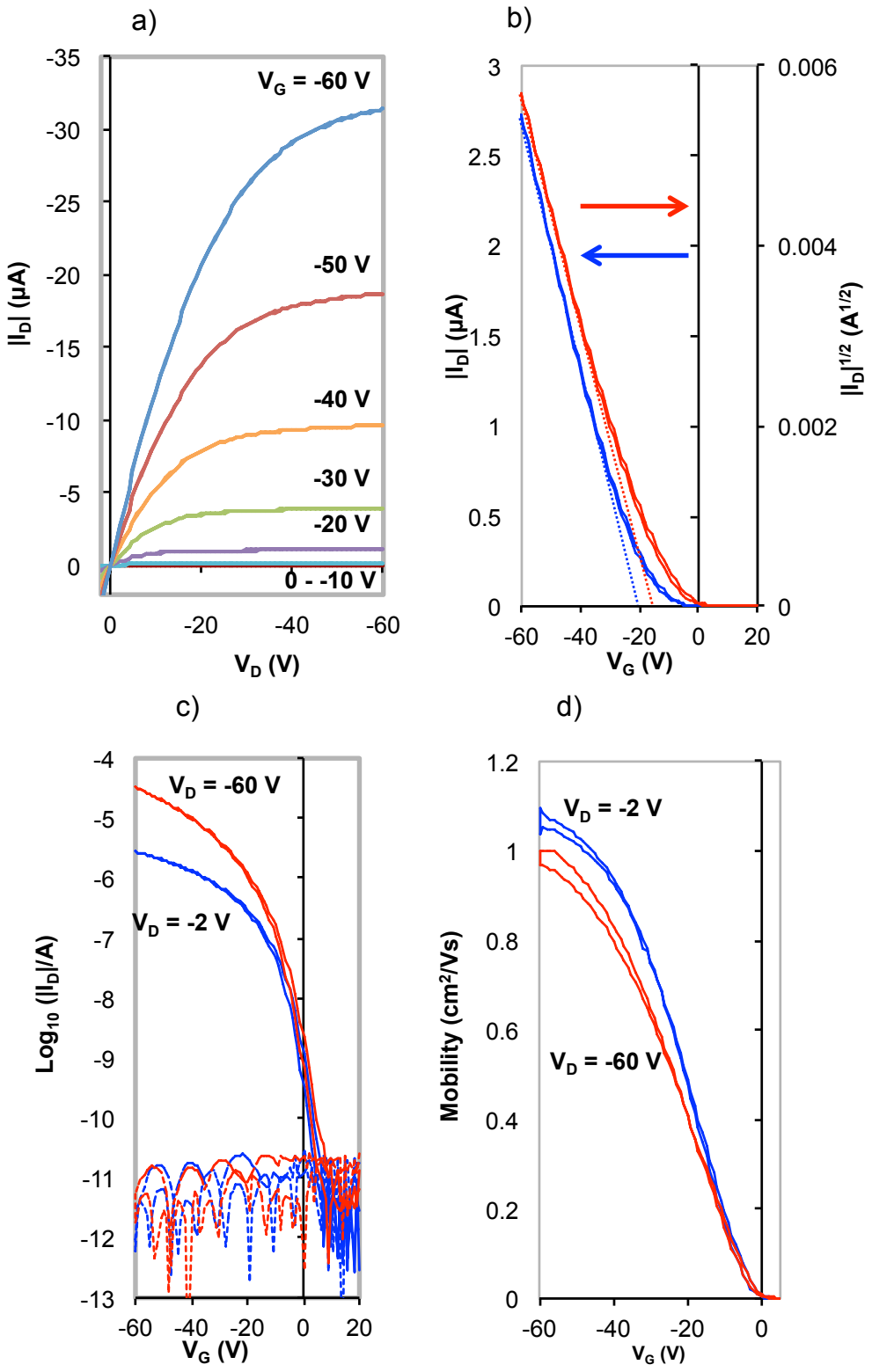


Figure 2.9 A typical set of transistor characteristics from which its performance may be assessed. (a) Output, (b) linear transfer characteristic, I_D vs V_G, (blue), and saturation transfer characteristic, $I_D^{1/2}$ vs V_G (red). (c) The transfer characteristics re-plotted in semi-log form together with the semi-log of the gate leakage current, I_G, vs V_G. (d) The gate dependent mobility.

The transfer plots shown in Figure 2.12 (b) are sometimes curved without a linear region due to a gate voltage dependent mobility, or due to contact resistance as demonstrated in [35].

The plots will have an upward curve if the mobility is gate voltage dependent, the current I_D increasing as more charge carriers are drawn to the surface by an increasing gate voltage filling more traps leading to more efficient charge transport. If charge injection is limited due to high contact resistance the plot of I_D vs V_G will have a reducing slope at higher currents. In such cases it is difficult to accurately estimate V_T and μ due to the curvature of the plots. It then becomes necessary to extract the mobility from a local slope method without the need to estimate V_T. In the linear region, then from equation 2.9

$$\mu_{lin} = \frac{dI_D}{dV_G}\frac{L}{WC_iV_D} \tag{2.11}$$

and in the saturation region from equation 2.10

$$\mu_{sat} = \left(\frac{\sqrt{dI_D}}{dV_G}\right)^2 \frac{2L}{WC_i}. \tag{2.12}$$

Figure 2.12 (d) shows μ_{lin} (blue) and μ_{sat} (red) plotted against V_G, here the mobility is shown to be gate voltage dependent by the fact that the mobility increases in both regimes with increasing V_G. From the plots it is possible to extract the maximum mobility from each regime.

2.2.4 OTFTs in Literature

The semiconducting layer of organic transistors can be fabricated using polymers, small molecules or blends. The main measure of transistor performance is its mobility, the velocity per unit electric field of free charge carriers through the semiconductor layer from source to drain. Table 2.2 shows an example of the mobility, V_T and I_{ON}/I_{OFF} ratio for various small molecule semiconductors along with the dielectric and substrate used.

As can be seen from the table single crystal transistors give the highest mobility transistors. However, these are difficult to process and take a long time to fabricate. They are also fragile rigid crystals going against the concept of materials suitable for flexible electronics. This means that such transistors are unsuitable for R2R printed electronics.

Table 2.2 A number of properties of a selection of OTFT devices. (*Denotes single crystal small molecule semiconductor). (n/m – property not mentioned in literature)

Semiconductor	Dielectric	Substrate	Mobility (cm^2/Vs)	V_T (V)	I_{ON}/I_{OFF}	Dep.	Ref
C_{10}-DNTT	200 nm SiO_2	n^+Si/SiO_2	7.6	n/m	$>10^8$	Ev.	[36]
DPh-DNTT	AlOx/C-14 SAM	Polyimide	2.4	-0.40	$>10^5$	Ev.	[37]
TIPS-Pen			>1		10^7	Sol.	[38]
C_{10}-DNTT	SiO_2	Si/SiO_2	6.0	0	10^6	Sol.	[39]
Pentacene	$Ba_{1.2}Ti_{0.8}O_3$	Glass	8.85	-1.89	10^3	Ev.	[40]
Pentacene	Tristratal SG silica	PET	6.3	-1.11	$>10^5$	Ev.	[41]
DNTT	SiO_2	Si/SiO_2	2.9	-11	10^7	Ev.	[14]
DNTT	AlOx/C-14 SAM	PEN	0.6	-	10^6	Ev.	[42]
Pentacene*	n/m	n/m	35	N/A	N/A	N/A	[43]
Pentacene*	Parylene	n/m	0.3	5	10^6	N/A	[44]
DNTT*	Cytop/SiO_2	Si/SiO_2	8.3	5	10^8	N/A	[45]
Rubrene*	Parylene	n/m	8.0	~0	$>10^4$	N/A	[46]
Rubrene*	Parylene	n/m	≤1.0	n/m	10^4	N/A	[47]
diF-TES ADT/PF-TAA	CYTOP	Glass	>5.0	-9.3	10^6	Sol.	[48]
TIPS/PαMS	SiO_2	Si/SiO_2	0.3	-1	$>10^5$	Sol.	[49]

Also evident from table 2.2 is the discrepancy in the mobility of single crystal transistors for the same materials, particularly for pentacene. However, it is difficult to make a direct comparison between [43] and [44] as the substrate and dielectric are not mentioned in [43], different measurement methods were used, and the methods for purifying the source material were different. The difference in the mobilities obtained for rubrene single crystal transistors is also significant, $1cm^2/Vs$ vs $8\ cm^2/Vs$ [46,47]. Here the work for both studies has been done by the same group using the same dielectric, namely parylene. The dramatic improvement was said to be due to optimisation of their crystal growth process. This shows what can be achieved by process optimisation. Additionally, in [46] a zero threshold operation is claimed, but there is no evidence for this in the results as only semi-log plots are shown. From the results it appears that the threshold voltage would be gate voltage dependent and becomes more positive with increasing V_G. So the claim of low trap states would be incorrect. This is an example of where a statement cannot be taken at face value and must be scrutinised. The mobility of $8\ cm^2/Vs$ does however appear to be reliable. This is because the crystals are said to be flat, this means that there are no

discrepancies when calculating the capacitance per unit area. Some single crystals can be round and the shape of the crystal is not taken into account when calculating the capacitance per unit area.

The mobilities in organic transistors typically tended to be less than 1 cm^2/Vs, with pentacene being the material of choice for the fabrication of transistors with mobilities exceeding 1 cm^2/Vs. Recently a lot of work has been done on functionalising existing semiconductors and also the development of blend materials. There are now numerous examples of transistors exceeding a mobility of $1cm^2/Vs$ as shown in table 2.2. Functionalised small molecules and blends tend to give better ordering leading to the higher mobilities [36, 39, 48]. In [36] is an example of work done with C_{10} functionalised DNTT where the mobility is over twice that of the highest mobility [14] realised using the parent molecule in non single crystal form. The semiconductor here is patterned within the edges of the source and drain contacts and so defines the channel width W. There should be no parasitic current contributing to I_D. The extracted mobility here therefore is reliable. However, in [39], the C_{10}-DNTT is deposited from a solution with the solvent tetralin, and is likely to cover the entire substrate. The channel is defined by a CYTOP coating that is deposited by using an ink-jet technique. However, this would not prevent parasitic currents travelling through the common semiconductor. This raises some doubt over the true mobility of such transistors. Also there is significant hysteresis in the measurements for the solution processed C_{10}-DNTT, compared to no hysteresis for the vacuum deposited C_{10}-DNTT.

The difference in the stability of the C_{10}-DNTT transistors of [36] and [39] is probably due to the use of solvent in [39]. The risk of using a solvent is that there may be contamination of the semiconductor layer by the carrier solvent if it does not fully evaporate post deposition.

One way to avoid the use of solvents is to solely use the method of vacuum deposition in the OTFT fabrication. These are usually small molecules that can easily evaporate and self orientate on the substrate surface. The advantage here is that only the semiconducting material is deposited onto the substrate, avoiding possible contamination of the film.

The most commonly used small molecule in transistor fabrication is pentacene, as it was shown early in the development of OTFTs to have a high mobility [50]. Unfortunately pentacene shows poor air stability, and OTFT performance begins to degrade within days of fabrication [51]. More recently an alternative evaporable small molecule naphtho[2,3-b]naphtho[2′,3′:4,5]thieno[2,3-d]thiophene (DNTT) was synthesised for the fabrication of OTFTs [14], showing mobilities close to those of pentacene. Unlike pentacene there is no central benzene ring that is vulnerable to oxidation, giving it greater stability in air as shown in the work of Zschieschang *et al*. [42]. It also has the potential to match and surpass the mobility of α-silicon.

Novel applications have already been demonstrated using DNTT transistors, such as organic light emitting diodes controlled by DNTT transistors [52], and the fabrication of DNTT transistors on banknotes [53]. As DNTT has been demonstrated to have high mobility and good air stability it became the material of choice for this work.

2.3 The Dielectric

2.3.1 Introduction

The conducting channel of an OTFT lies at its interface with a dielectric, and device performance critically depends on the nature of this interface. There are a number of properties to consider when selecting a dielectric.

If selecting a solution deposited dielectric (the most common option for OTFTs) the first issue to consider is to be certain that the solvent in the solution of the material being deposited, be it the insulator on to the semiconductor or vice versa, does not interact with the previously deposited layer. This can lead to layer interdiffusion, increased surface roughness and lower breakdown voltage properties for the dielectric. This can be mitigated by the selection of orthogonal solvents for sequential layers. However, the solvent may still contaminate the semiconducting layer or damage it, regardless of being orthogonal.

The evaporation of the solvent from the drying dielectric also poses a problem. As the solvent dries it may leave behind pin-holes in the dielectric. Pinholes provide breakdown paths within a transistor that could lead to circuit failure.

The roughness of a deposited film also determines the properties of the interface. The conducting channel is typically only a few nanometres thick, so if the surface roughness of a film is 50 nm then there will be physical barriers to charge transport. The importance of the topography of the interface was discussed in [54].

A high-dielectric constant (*k*) material becomes desirable over a low-*k* material for films of equal thickness, as this should increase carrier mobility. The high-*k* dielectric allows for a higher concentration of charge carriers compared to a low-*k* dielectric for the same V_G, allowing more traps to be filled and more efficient charge transport. However, some high-*k* dielectrics can be hygroscopic, drawing moisture from the air causing device instability. Low-*k* dielectrics tend not to be as susceptible to atmospheric contaminants, leading to greater device stability. Another problem associated with high-*k* dielectrics is their tendency to scatter energy states due to increased dipolar disorder at the interface [55]. Selecting a good dielectric is therefore a balance between these properties.

2.3.2 Common Dielectric Materials

The list of commonly used dielectrics in Table 2.3 is far from comprehensive but does give a brief overview of materials that are commonly used as dielectrics for organic semiconductors.

Table 2.3 A selection of dielectrics commonly used to fabricate OTFTs

Dielectric	Process	C_i (nF/cm^2)	*k*	d (μm)	Ref
PMMA	Spin-coat	-	2.6	0.7	[56]
PVP	Spin-coat	1.2	3.9	1-1.5	[57]
PVA	Spin-coat	1.8	8	1-1.5	[57]
SiO_2	Thermally Grown	34.5	3.9	0.1	[58]
AlOx	Sputter	54	6.5	0.1	[59]
AlOx/PVP	Sputter/spin-coat	31	-	0.145	[59]
Parylene	Reactor coating	-	2.6	0.2	[47]
AlOx/C-14 SAM	Evap/Plasma/Immersion	800	-	0.0053	[60]
Cytop	Spin-coat	2.7	2.1-2.2	0.7	[61]

It can be seen that the capacitance per unit area, C_i, dielectric constant, *k*, and film thickness d, vary widely, and the materials are not limited to organics. Reducing d and increasing *k* will increase C_i, theoretically leading to higher mobilities for the

semiconductors deposited on the films. However, reducing the thickness can also lead to higher gate current; the effects of higher *k* have already been discussed in section 2.3.1. One thing that is noticeable is that the organic dielectrics are deposited from solution. In the approach attempted in the present work, solvents are not needed as the focus is on an evaporable dielectric.

Thermal evaporation is a technique that has been frequently used for the deposition of organic semiconductors and metallic contacts over the past number of years. Our collaborators at Oxford University have also developed a system for the roll-to-roll vacuum deposition of a dielectric material tri(propylene glycol) diacrylate (TPGDA) [62, 63] for use in OTFTs. TPGDA has been shown to be a very uniform, smooth dielectric with no evidence for pinhole formation, with a root mean square (rms) roughness of less than 1 nm. Since no solvent is required, there are no drying or annealing times to factor in. It also means that there is no concern regarding the selection of orthogonal solvents. Each sequential layer is deposited directly onto the next without fear of interdiffusion. As will be shown, the insulator is of high integrity even at thicknesses down to ~400 nm. This gives TPGDA several advantages over conventional solution deposited dielectrics.

This allows the opportunity to realise fully R2R vacuum-deposited transistor circuits as an alternative route to the conventional R2R printing methods.

2.4 Organic Circuits

2.4.1 Introduction

Integrated circuits have become extremely important to the function of modern technology. Organic circuits are unlikely to replace crystalline inorganic semiconductor based circuits as the material of choice for fast, high density circuits, as even the best mobilities are orders of magnitude lower than their counterparts. The main application of organic integrated circuits will be in large-area, low-cost electronics. There are a number of steps to be completed on the way to achieving fully integrated circuits using vacuum deposited DNTT. First will be the transistor, which is the basic building block. The second will be the inverter, which will require two neighbouring transistors to be fabricated successfully. NOR and NAND gates are essentially inverters with an additional driver transistor, thus requiring three

neighbouring transistors to be fabricated successfully. A ring oscillator is a device consisting of an odd number of inverters, ranging from three upwards. A three stage ring oscillator would therefore require six neighbouring transistors to be fabricated successfully. As the circuits become more complicated and the numbers of transistors increase, device yield becomes an important issue.

2.4.2 Inverter

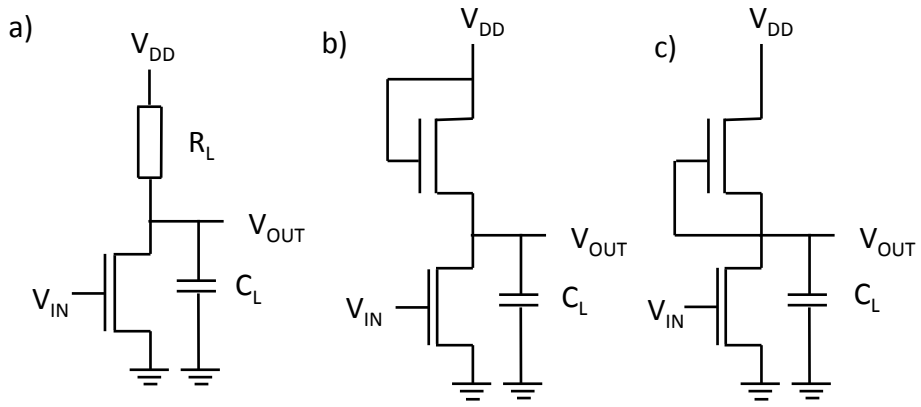


Figure 2.10 Three different circuits for an inverter with (a) resistor load (b) enhancement mode load transistor (c) depletion mode load transistor. Adapted from [64].

a) Resistive Load

The inverter in its simplest form is shown in Figure 2.13 (a). It consists of a load resistor, a driver transistor acting as a switch and an associated load capacitor C_L. The load capacitor is essentially formed by the gate of the subsequent transistor stage in a more complex circuit, e.g. a ring oscillator plus any parasitic capacitance. In the following description inverters powered from a voltage rail at V_{DD} and based on p-type OTFTs will be used to charge/discharge C_L.

When the input voltage switches from high (V_{IH}) to low (V_{IL}), the driver transistor switches off allowing C_L and hence the output voltage, V_{OUT}, to rise towards the rail voltage V_{DD}, rising from a low output voltage (V_{OL}) to a high output voltage (V_{OH}). During this period the current through R_L decreases, following the equation

$$I_L = \frac{V_{DD} - V_{OUT}}{R_L} \tag{2.13}$$

with the time dependence of V_{OUT} given by

$$V_{OUT} = \left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.14}$$

where τ is the charging time constant given by

$$\tau = C_L R_L. \tag{2.15}$$

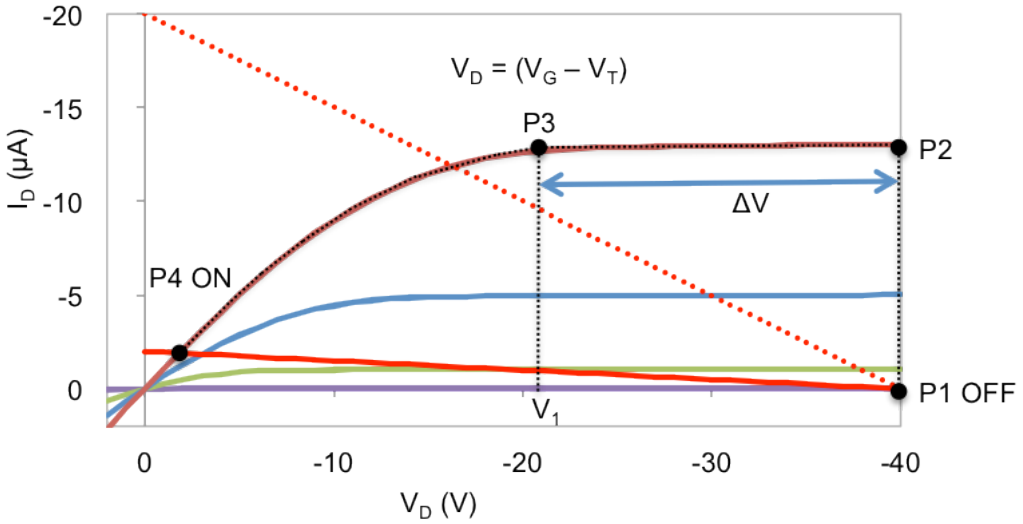


Figure 2.11 Two different load lines of a resistor load, the solid line is 10 x the resistance of the dashed red line. The load lines are plotted against the output characteristics of the driver. Adapted from [64]

After several time constants the circuit is close to steady state represented by the point P1 in Figure 2.14 where the load line representing R_L crosses the output characteristic corresponding to $V_G = 0$. When V_{IN} is then switched from V_{IL} to V_{IH} the transistor turns on, the operating point moves instantly to P2. Now the charge stored on C_L is discharged through the driver transistor at a rate determined initially by the saturation current for the given V_D and V_{IN}. The operating point now moves from P2 to P3 the time, t_s, taken being given by

$$t_s = \frac{C_L \Delta V}{I_D} = \frac{2C_L(V_{DD} - V_1)}{\beta(V_G - V_T)^2} \tag{2.16}$$

where $\beta = \frac{W\mu C_i}{L}$, and $\Delta V = V_{DD} - V_1$. As the inverter moves from P3 to P4, I_D falls as V_D decreases. However, the current discharged from C_L must be the same as I_D, so that

$$C_L \frac{dv(t)}{dt} = -\beta(V_G - V_T)v(t) + \frac{\beta}{2}v(t)^2. \tag{2.17}$$

Solving equation 2.17 for *v(t)* gives

$$v(t) = V_1 \frac{2exp^{(\frac{-t}{\tau})}}{1+exp^{(\frac{-t}{\tau})}} \quad (2.18)$$

where $\tau = C_L/g_m$, $g_m = -\beta(V_G-V_T)$ and $V_1 = (V_G-V_T)$. The switching time from V_1 to P4 of ΔV_{OUT} is ~ 2.7 τ, so that the total switching time is t_s + 2.7 τ. Conventionally the switching time of the inverter is taken as the time taken between 10 % and 90 % of ΔV_{OUT}.

The quiescent point, P4, may be deduced from the point at which the load line for R_L crosses the relevant output characteristic and occurs when the current through R_L is equal to the transistor current. The load line for a resistor with a resistance an order of magnitude less than that of the original resistor is shown as a dashed red line in Figure 2.14. This would shift the quiescent point and result in faster switching speeds but a smaller ΔV_{OUT}.

Resistor loads are not generally suited to integrated circuit technology typically the sheet resistance achievable is too low and they take up too much chip space. Consequently it is more common for inverter loads to combine the driver transistor with a load transistor operating in the enhancement mode (Figure 2.13 (b)) or in the depletion mode (Figure 2.13 (c)).

b) Enhancement mode load

An enhancement load inverter is shown in Figure 2.13 (b). Here the resistor of Figure 2.13 (a) is replaced by an enhancement mode load transistor. The gate of the transistor is connected directly to the rail voltage so that the transistor is always in the saturation regime.

The load line representing an enhancement mode transistor with the same transconductance g_m as the driver is shown in red in Figure 2.15. In this case charging and discharging of C_L will be rapid but the voltage swing will be low. If g_m (load) = 0.1 g_m (driver), achieved by reducing the aspect ratio W/L, of the load transistor, then I_L is reduced by a factor 10. As I_L is smaller, the V_D required for the corresponding I_D is reduced. This results in a larger V_{OUT} swing as represented by the dashed load line in Figure 2.15. There is a trade off, therefore, in that the smaller the load transistor the larger the V_{OUT} swing but the time taken to charge C_L is increased.

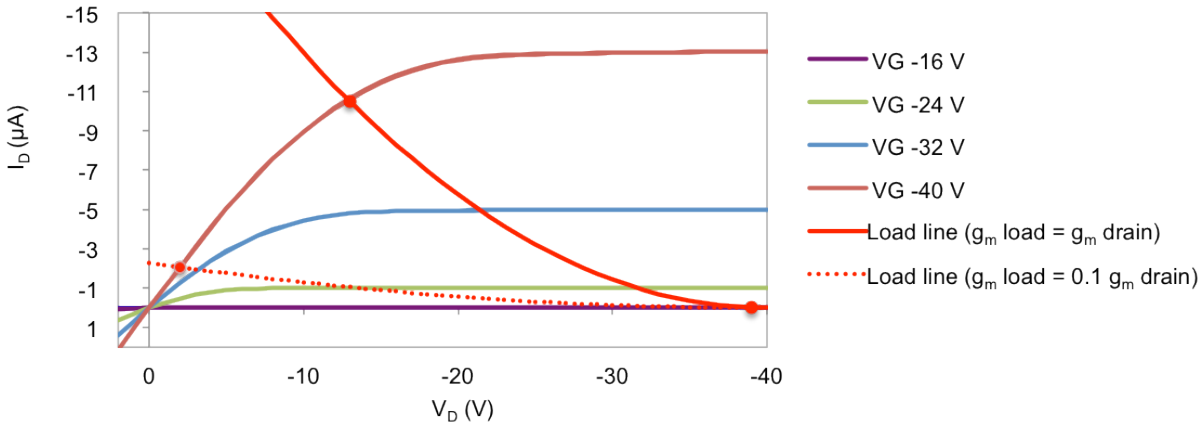


Figure 2.12 The load lines of two load transistors are plotted in red. In the solid plot the conductance ratio of load to driver transistor is 1:1 and for the dashed plot is 1:10. Both are plotted with the output of the driver transistor. Adapted from [64].

c) Depletion mode load

As with the enhancement load inverter, the depletion mode inverter has a load transistor rather than a resistor and is shown in Figure 2.13 (c). In this case, the gate of the load is connected directly to the inverter output. The operation of the device depends on the transistor being conductive at $V_G = 0$ V, so that V_T of the load device must be positive. Switching times of depletion mode devices tend to be quicker than those of enhancement mode load devices. This is due to a better balance between the charge and discharge times.

d) Noise Margin

The noise margin of an inverter can be found from the voltage transfer characteristic, such as that shown in Figure 2.16, and is a measure of inverter stability. When $V_{IN} = V_{OUT}$ this is said to be the trigger voltage, V_{TR}. V_{TR} is not a stable state and is within the transition region of the inverter.

Any fluctuation in V_{IN} will cause the circuit to switch to either V_{OH} or V_{OL}. Problems occur when a circuit is in one of the stable states and a fluctuation due to noise pushes V_{IN} past V_{TR} causing the circuit to switch to the opposite stable state. The noise margin that can be tolerated is the difference in voltage between the stable voltage points, V_{OH} and V_{OL} and the input voltages at which the gain ($\frac{dV_{OUT}}{dV_{IN}}$) exceeds 1.

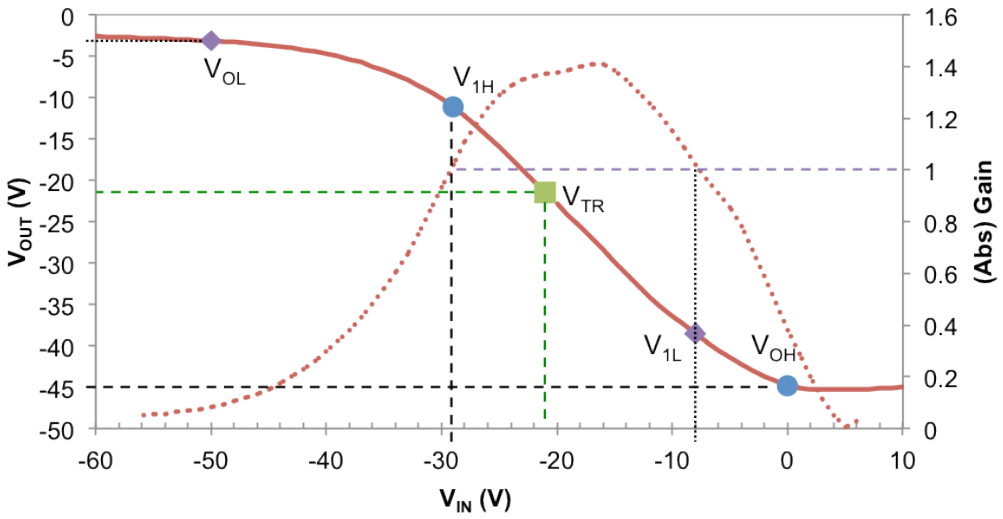


Figure 2.13 A voltage transfer plot showing V_{OUT} (solid line) vs V_{IN}. The gain, dV_{OUT}/V_{IN}, is shown as the dashed line. Adapted from [64].

When the output of one inverter forms the input of the next the importance of the noise margins becomes more apparent. If we consider V_{OH} to be the maximum output voltage, then this is the maximum V_{IH} for the next stage (blue circle Figure 2.16). V_{IH} must be higher than the high input voltage at which gain = 1 (V_{1H}, blue circle). Otherwise the input voltage would be within the transition region, and the output would be unstable.

It can be seen that there are two separate regions of noise tolerance. Ideally these should be of equal magnitude and the transition between them sharp with as large a step as possible. For the low noise margin (NM_L) this is the difference between V_{OL} and the low input voltage at which $\frac{dV_{OUT}}{dV_{IN}} = 1$ (V_{1L}). That is $V_{1L} - V_{OL} = NM_L$. For the high noise margin (NM_H) it is the difference between the high output voltage, V_{OH}, and the high input voltage at which $\frac{dV_{OUT}}{dV_{IN}} = 1$. So that $V_{OH} - V_{1H} = NM_H$.

2.4.3 Ring Oscillator

A ring oscillator is essentially a set of inverters where the output signal of one inverter becomes the input signal of the next inverter.

Figure 2.17 is an example of a three-stage ring oscillator. As can be seen it is three connected inverter stages with the output of the third stage fed back to the input of the first stage. When D1 is turned on the output of stage 1 becomes ~ 0 turning off D2 so that the output of stage 2 goes high turning on D3. This in turn causes V_{OUT} to

become ~ 0 which then turns off D1 causing all the inverters to change their state sequentially. These changes in state propagate continuously through the circuit giving rise to an oscillating output of frequency *f*. In [60] is an example of the MHz output frequencies that DNTT ring oscillators are capable of achieving.

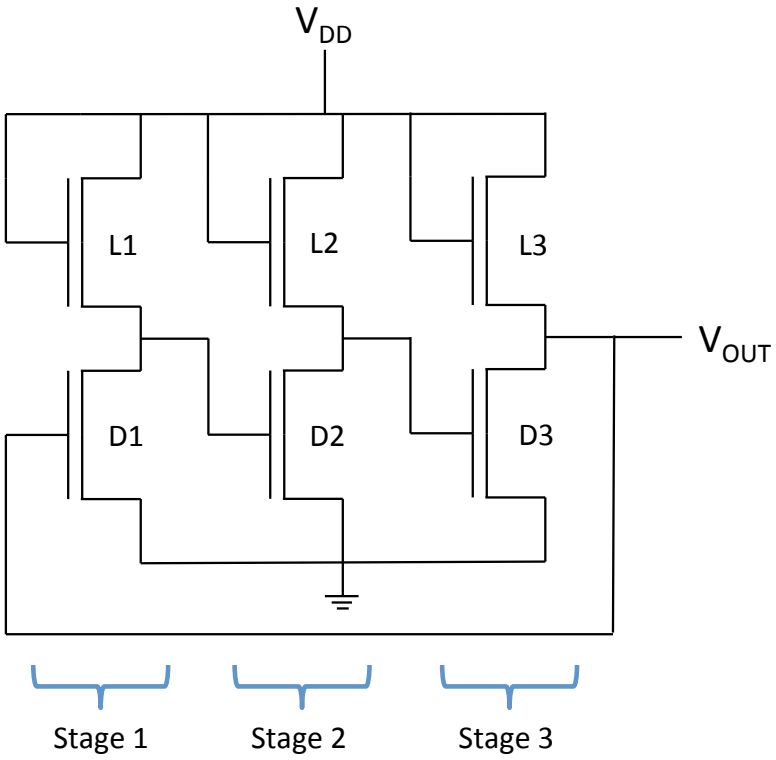


Figure 2.14 A schematic circuit diagram of a three stage ring oscillator. Adapted from [64].

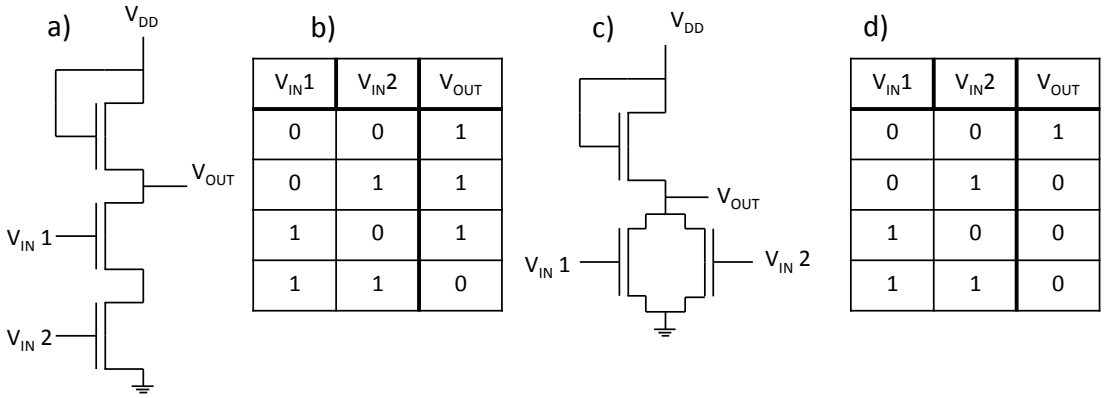
As was seen in section 2.3.2 there is a time delay associated with charging the gate of the following inverter stage. The initial switch-on of D1 will depend on the time it takes for the gate capacitance to charge through L3. There is also a time delay for D1 to discharge the capacitance of the gate of D2. The collective time taken for both charge and discharge to occur in known as the stage delay, t_d. For a complete oscillation cycle to occur each stage must change stage twice. Therefore the time taken for one complete oscillation, $t = \frac{1}{f}$, is the time taken for N stages to switch twice. So the average stage delay can be written as

$$t_d = \frac{1}{2fN}. \tag{2.18}$$

The maximum oscillation frequency of the ring oscillator is therefore dependent on the switching speed of the individual inverter stages. There are ways to increase this

frequency. The first is to reduce the number of stages, as each additional stage adds to the total stage delay. Secondly V_{DD} can be increased, but this also increases power consumption and puts additional bias stress on the transistors. Reducing the load capacitance of the individual stages would also speed up the output frequency, by reducing the charging time. Asymmetry in the rise and fall times means that devices are limited by one or the other, creating a bottleneck. By balancing the rise and fall times the bottleneck is avoided and the circuit switching should be faster.

2.4.4 NOR and NAND Gates



$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

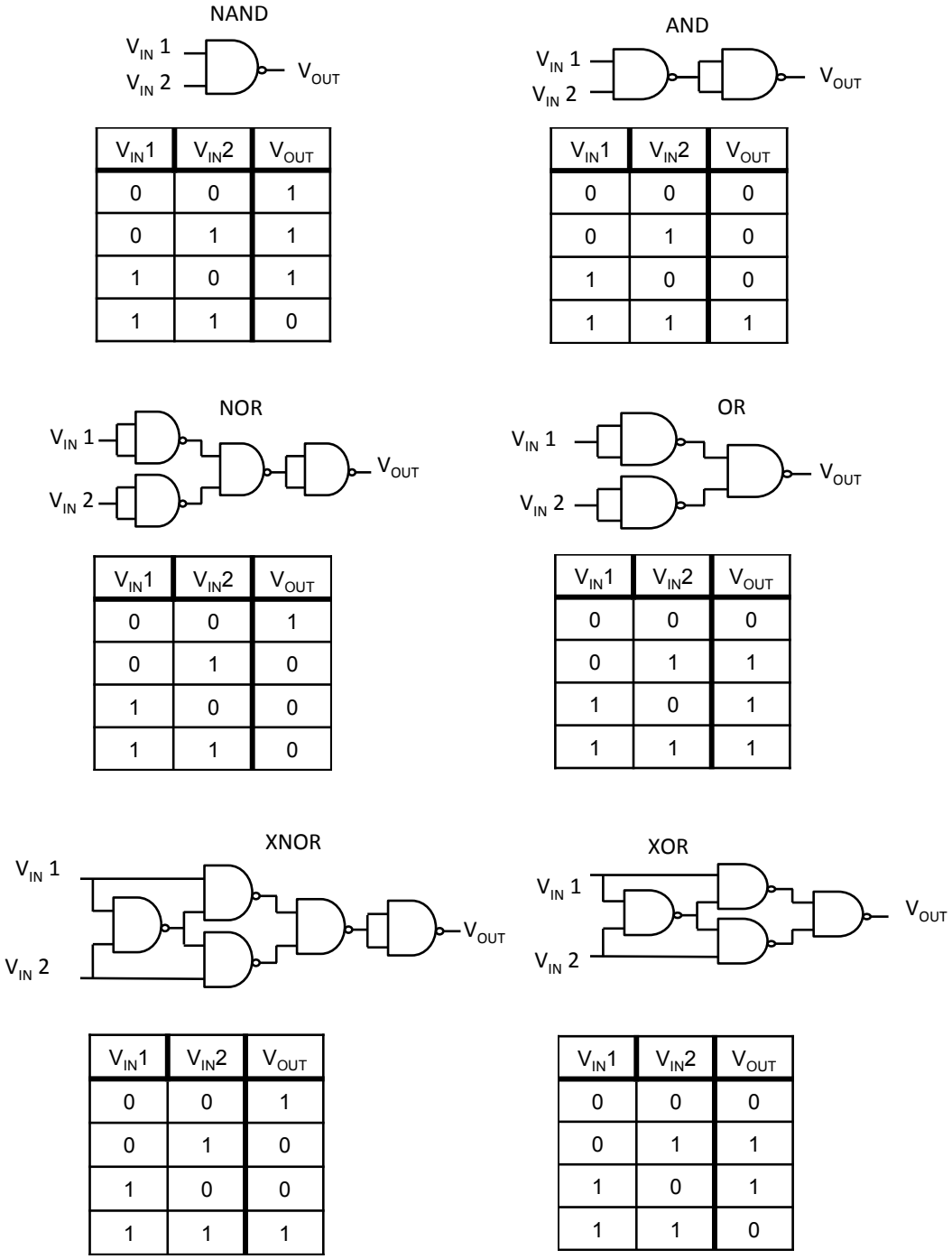
$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

Figure 2.15 (a) Circuit diagram of a NAND gate and (b) the NAND gate truth table. (c). The NOR gate circuit diagram and (d) the NOR gate truth table. Adapted from [64]

It is possible to add a second driver transistor to the inverter, thus enabling additional logic functions to be achieved. In the NAND gate (Figure 2.18 a)) the additional transistor is placed in series with the original driver transistor.

It is easy to see that for current to pass from V_{DD} to ground both inputs $V_{IN}1$ and $V_{IN}2$ must be set high (logic 1). So the output is only 0 when both inputs are 1, otherwise the output is 1 (Figure 2.18 (b)). The NOR gate differs from the NAND gate in that the second driver transistor is parallel to the first (Figure 2.18 (c)) rather than in series. Now if either input is 1, current can pass from V_{DD} to ground. Therefore the output is only 1 when both inputs are 0, otherwise it is 0 (Figure 2.18 (d)). By placing an inverter on the output of the two gates it is possible to achieve the inverse functions, AND for NAND and OR for NOR. In fact it is possible to achieve all logic functions with circuits consisting solely of NAND or NOR gates. Some examples of simple logic gates based only on NAND gates are given in Figure 2.19. The only

function not shown is the NOT gate which is simply an inverter function that can be achieved by connecting $V_{IN}1$ and $V_{IN}2$.



$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	0
0	1	0
1	0	0
1	1	1

$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	0
0	1	1
1	0	1
1	1	1

$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	1

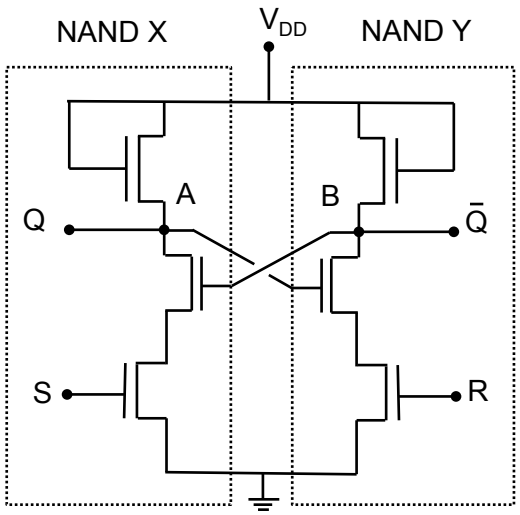
$V_{IN}1$	$V_{IN}2$	V_{OUT}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 2.16 Logic functions that can be completed using only NAND gates. Adapted from [64].

It becomes apparent that if NAND or NOR gates can be successfully fabricated it would be possible to start designing more complex circuits around them.

2.4.5 NAND SR Flip-Flop

Unlike the logic gates mentioned in section 2.3.4 the SR flip-flop shown in Figure 2.20 provides a basic memory function, as its previous state and its current input determine whether it changes state or not. This makes it possible for it to store one bit of data.



Set (S)	Reset(R)	Output (Q)
0	0	Invalid State
0	1	Q = 1
1	0	Q = 0
1	1	No Change

Figure 2.17 Circuit diagram for the SR NAND flip-flop gate, (b) SR NAND flip-flop truth table. Adapted from [64].

There are two inputs, S which sets the output Q, and R which resets Q. Q can be at either 0 or 1 depending on the set/reset conditions. If the logic gate is considered as two cross-coupled NAND gates it is readily seen that the output of NAND X is also one of the inputs of NAND Y. This allows feedback from one NAND to the other, and the state of one output becomes dependent on the state of the second output.

If we consider the circuit shown in Figure 2.20, and begin by setting S to 1 and R to 0, then NAND Y has one input at zero and $\bar{Q}$ = 1. The output of $\bar{Q}$ is fed back to NAND X through connection B, so now both of its inputs are 1, therefore Q = 0. If now R is set to 1, $\bar{Q}$ will remain at 1, as the input from A is 0. The circuit remains set at $\bar{Q}$ = 1 and Q = 0. If S is then set to 0 (R remaining at 1), then Q = 1, since at least one of its inputs is set to zero. Since Q = 1, then so is input A of NAND Y. For NAND Y both inputs are now 1, and the output $\bar{Q}$ = 0. Now if S it set to 1 it does not change the state of the logic gate as input B of NAND X is at 0, so Q will remain at 1 and $\bar{Q}$ at 0. This is the second set state. It can be seen that having both S and R inputs at 1, Q and $\bar{Q}$ will have an opposite state, 0,1 or 1,0 depending on the state of the S and R inputs

before being set to 1, 1. However, setting both S and R inputs to 0 zero must be avoided, as this sets both Q and $\bar{Q}$ to 1 that can cause the logic gate to lose the memory of the previous state and to become unstable.

2.5 R2R Printing

2.5.1 Introduction

Roll-to-Roll (R2R) printing is commonly used in newspaper and magazine printing, as well as packaging production. A roll of material is fed into a printer, and re-rolled at the exit at speeds of up to 250 m per minute. There is potential for using such a process for high-throughput large-area electronics. Conventional inorganic based electronics are crystalline and cannot be folded or bent, so cannot be used in an R2R process.

2.5.2 Printing Methods

A requirement of the R2R printing of transistors is that layers can be deposited sequentially in a 2D structure to a specific pattern. This can be achieved using any one of a number of processes. The methods of printing described below can be used as a stand-alone process, or in combination with others in a single R2R system.

a) Gravure Printing

Gravure printing is widely used for the high-volume printing of magazines. The image is etched into a metal cylinder. In operation the cylinder rotates through an ink bath (Figure 2.21), ink fills the recesses and after doctor blading is then transferred to the substrate by the surface tension of the ink. The recesses of the roller are continually refilled by passing through an ink bath, the doctor blade removing the excess ink. Low viscosity inks are used to prevent clogging of the roller during long-term operation.

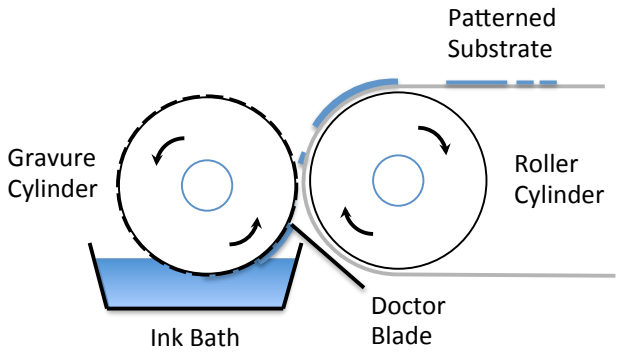


Figure 2.18 Schematic representation of the gravure printing process.

b) Flexographic Printing

In flexographic printing, ink is deposited onto an anilox roller from a fountain roller (Figure 2.22) that is partially submersed in an ink bath. The anilox roller has recesses that carry ink. A doctor blade removes excess ink from the roller leaving it coated to the required thickness. The ink is then transferred to a printing roller with a raised pattern, which is then pressed onto the substrate surface to create the required pattern.

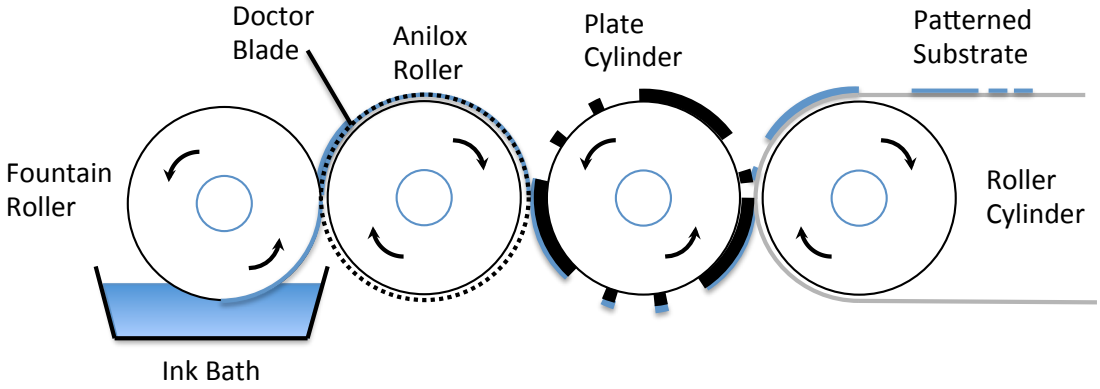


Figure 2.19 Schematic representation of the flexographic printing process.

c) Rotary Screen Printing

In screen printing ink is forced through a partially covered mesh by a squeegee. Ink passes through the patterned perforations in the mesh and deposits on to a substrate. This process is only suitable for viscous inks as thinner inks would flow through and underneath the mesh and not form the desired pattern. There are two methods of screen printing, flat bed and rotary screen printing. Flat bed screen printing is essentially a sheet to sheet process. In rotary screen printing the mesh and squeegee

are placed inside a roller as a substrate passes on the outside and is compatible with a R2R process as seen in Figure 2.23.

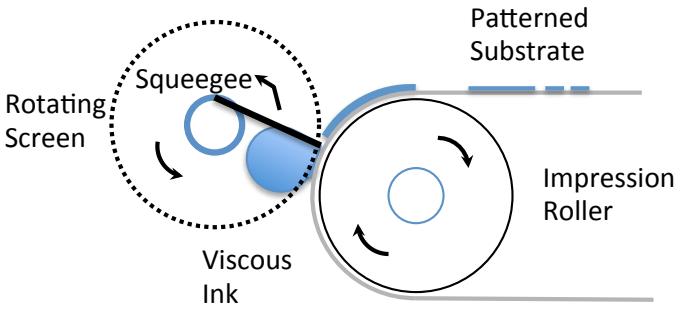


Figure 2.20 Schematic representation of the scree printing process.

d) Offset Printing

Here there are two sources (Figure 2.24). The first is either a water or oil based source that repels the ink from the second source. This generates a pattern on the printing plate cylinder, and only the ink is transferred to the offset cylinder. The ink is then transferred to the substrate in the desired pattern.

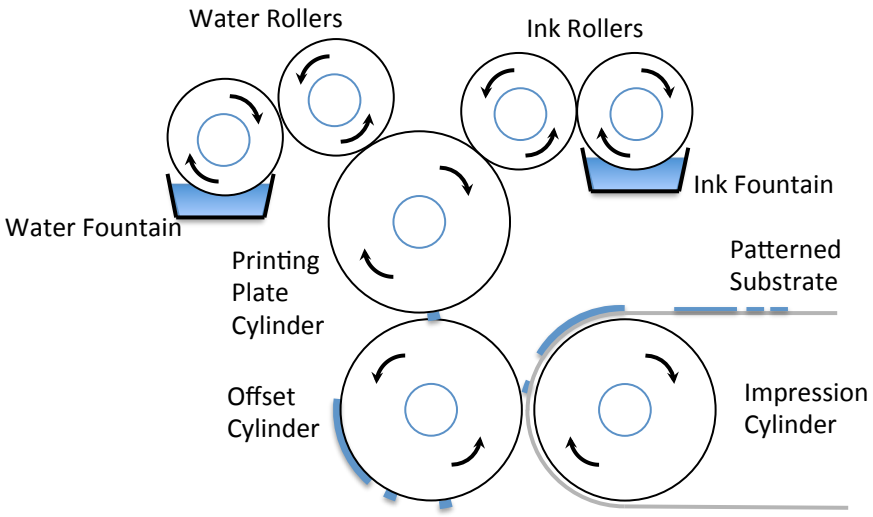


Figure 2. 21 Schematic representation of the offset printing process.

e) Inkjet Printing

The inkjet printing method is different to the other printing methods as there is no pre-patterned mask for ink transfer to the substrate. Instead ink is transferred to the surface through a piezoelectric controlled nozzle. Features are printed following a pixelated pattern, where a pixel will receive a droplet of ink or not to the desired pattern. This has advantages over the other methods as patterns can be changed easily

using a computer in contrast to the time and expense of producing the patterned cylinders/plates in the other systems.

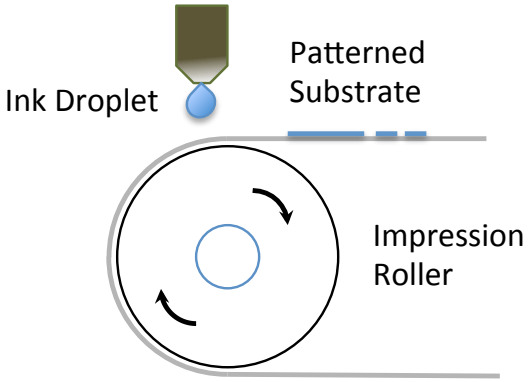


Figure 2.22 Schematic representation of the inkjet printing process.

One thing that connects all of the methods mentioned above is their use of inks, the material to be deposited suspended within a solvent. As layers are sequentially deposited, the solvents for the various layers must be orthogonal. Otherwise there is a possibility that the interdiffusion of layers will affect the device structure and its operation. There is also the issue of drying times. The solvent needs to be completely removed so that it does not affect device performance. The problems encountered concerning pinholes has been discussed earlier in section 2.3.1. Layer thickness is another problem. Due to the viscosity of the inks used, layers can be very thick, > 2 μm, and have a high degree of surface roughness that could hamper device performance. As an example, the dielectric layer thickness in [65] was 3 μm, with a surface roughness of 70 nm, thick films being required to avoid short circuits. There are also solvent drying times during which the solvent must evaporate, and annealing times to consider.

For the envisioned all-vacuum process a method of depositing a fine aluminium pattern has already been developed [66]. Here in a lift-off like process using gravure printing, diffusion pump oil is patterned onto the substrate then aluminium is evaporated onto the substrate. The heat of the aluminium is enough to evaporate the oil, so the area of the surface onto which the oil was originally deposited remains free of aluminium. It can easily be seen how this process could be developed for the patterning of transistor gates and with further development the source-drain contacts.

A significant challenge that arises from the high throughput speed is registration. The substrate will track from side-to-side resulting in layers becoming misaligned. Registration is, therefore, a major issue. If a substrate tracks by 1 mm, this is significantly grater than a channel length in the tens of μm range. Tolerance must be built in, therefore, in any circuit that is designed for a R2R process.

2.5.3 The Development of Organic Circuit Printing

In 2000 inkjet printing was proposed as a new method for printing low cost electronic circuits by Sirringhaus *et al*. [67] and was an important first step towards printed electronics. However, the semiconductor and dielectric layers were spin coated, only the SD and G contacts being ink jet printed using poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS). The substrate was also specially prepared for inkjet deposition to improve printing resolution. What was shown here was that it was possible to use a conventional printing process to pattern electrodes using organic materials. Carrier mobility in these devices was between 0.01 and 0.02 cm^2/Vs for poly(9,9-dioctylfluorene-co-bithiophene) (F8T2) semiconductor on poly-vinylphenol (PVP) dielectric, and inverters had a switching frequency in the hundreds of Hz range.

In the following year Kawase *et al*. [68] demonstrated that inkjet printing could be used to pattern vias by the selective deposition of the dielectric layer solvent. However, the semiconductor dielectric layer were still solution processed as in [59] the only real development being the ability to pattern interconnects.

In 2004 Knobloch *et al*. [69] had success in printing a ring oscillator with an output frequency of 0.86 Hz at V_{DD} = -90 V. Polyaniline (PANI) was doctor bladed onto a substrate and etched to form the SD electrodes. Poly (3-hexylthiophene) (P3HT) and poly(3, 3”-dihexyl-2, 2’:5’, 2”-therthio-phene) (PDHTT) were both used as the semiconducting layer, polymethylmethacrylate (PMMA) and poly(4-hydroxystyrene) were used for the dielectric layer; all were doctor bladed. The final gate contact was deposited by pad printing. Since no details of patterning of the semiconductor are supplied, it is assumed that it coats the entire surface. The significant step here is the working ring oscillator. Although the frequency is low, it was shown that printing techniques could be used to pattern it. The transistors displayed high gate leakage, as

can be seen in the transistor output characteristics; the plots do not pass through the origin.

Three years later in 2007 Hübler *et al*. [70] printed the PEDOT/PSS SD electrodes by using offset printing, followed by gravure printing of the F8T2 semiconductor layer and a low k butadiene-styrene-copolymer (BuS) dielectric. The OTFTs were finished using flexographic printing of a high k Luxprint dielectric and silver-ink gate electrodes. Although each step was performed separately, each was done at a speed of ~60 metres per minute, indicating the potential for high-speed production. Carrier mobility in the devices was low, ~ 1.3 x 10^{-3} cm^2/Vs, and a ring oscillator was shown to operate at a frequency of 4 Hz.

The following year, Tobjork *et al*. [71] also demonstrated a fully printed device. The gate electrode was inkjet printed silver ink, the P3HT semiconductor and PVP dielectric layers were printed by reverse gravure and the PEDOT/PSS SD contacts were inkjet printed. Once again the processes were undertaken in sequential steps rather than one continuous process. Transistors were successfully fabricated but the mobility was not given. Device performance was not improved, only a different method of reverse gravure utilised.

Two years later in 2010, a number of groups published papers based on printed transistors. Vornbrock *et al*. [72] used a combination of gravure printing for the silver gate electrodes, PVP dielectric and poly(2,5-bis(3-tetradecylthiophene-2-yl)thieno[3,2-b]thiophene) (pBTTT) semiconductor layers. Inkjet printing was used for the silver SD electrodes, the resulting devices giving a maximum hole mobility of 0.06 cm^2/Vs. However, this was once again a stepwise process and required annealing times in excess of five minutes between each deposition. The focus of the study was the development of patterning techniques rather than device performance.

The same year Hamsch *et al*. [73] reported on the complete gravure printing of more than 50,000 OTFTs of which 400 were tested giving ~75% yield. The gravure printing steps were performed at a web speed of 30 metres per minute. The average mobility was estimated to be ~ 5 x 10^{-4} cm^2/Vs, the highest being ~1.6 x 10^{-3} cm^2/Vs. A 5-stage ring oscillator was also fabricated that had an output frequency of 2.5 Hz, at -100 V V_{DD} with a 25 V swing. The frequency was lower than that reported two years previously.

Also in 2010 Voigt *et al*.[74] used gravure printing for the semiconductor, dielectric and gate contacts. The substrates used had pre-patterned SD contacts. The best mobilities were in the range of 0.02-0.10 cm^2/Vs. Once again this was not a continuous process, and each step was printed at a speed of 40 metres per minute.

Verilhac *et al*.[75] printed the semiconducting layer by two different methods, screen and gravure printing. The dielectric and gate contact layers were printed by inkjet. The SD contacts were patterned by photolithography or laser ablation, so the end product could not be called fully-printed The best mobility was found to be ~0.036 cm^2/Vs, and was measured on devices patterned by laser ablation of the SD contacts and screen printing of the semiconductor. Despite the low mobility they were able to successfully fabricate working ring oscillators. A 5-stage ring oscillator had an output frequency of 300 Hz, and a swing of 12 V with V_{DD} = 50 V.

In 2011 Heubler *et al*. [76] used the same printing process as noted in [70] using F8T2 semiconductor on PMMA dielectric to fabricate ring oscillators, using web speeds of between 30 and 60 metres per minute. The ring oscillator had an output frequency of 6 Hz with V_{DD} = -80 V. Although far lower than the 300 Hz achieved in [75], these were entirely printed devices and were a slight improvement on the 4 Hz output frequency achieved previously in 2008.

Chung *et al*. [77] used inkjet printing exclusively for the fabrication of all printed transistors. However this was once again a stepwise process, with 20 minutes required for sintering of the contacts. Even though extra measures were taken, the mobility was still relatively low at 0.02 cm^2/Vs, but comparable to other printing methods.

Noh *et al*. [65] used R2R gravure to print the silver gate electrode, dielectric and silver SD electrodes and roll-to-plate (R2P) gravure to print the single-walled carbon nanotube (SWNT) semiconductor layer. This was done at a web speed of 10 metres a minute for both processes. The maximum field effect mobility was 0.5 cm^2/Vs in saturation, a factor of 10 higher than most printing processes. The printing process was used to print a D-flip-flop device that showed a 23 ms fall time. However, a number of the layers required curing before the next layer could be deposited. Later in the same year the group used the process to successfully print a half adder circuit, with a device with a fall time of 53 ms [78]. In 2012, the group were able to reduce the variation in the electrical characteristics of individual components by using only

R2P printing methods, at an increased web speed of 18 metres per minute [79]. A full adder consisting of 27 individual TFTs was successfully printed. At the time it was the most complicated fully printed organic circuit reported.

Also in 2012 Hambsch *et al*. [80] compared the performance of unipolar and complementary logic gates. The transistors were printed by using gravure printing for the PEDOT/PSS SD contacts and TIPS-pentacene semiconductor layer, and using flexographic for the Cytop dielectric and PEDOT/PSS gate electrodes at a web speed of 30 metres per minute. An n-type small molecule was used for the complementary inverters. The p-type transistors had mobilities in the range of 0.01 to 0.02 cm^2/Vs, and the n-type were an order of magnitude lower at 2-4 x 10^{-3} cm^2/Vs. Enhancement load inverters were shown to have a total delay time of 87.6 ms, compared to 13.8 ms for the complimentary inverters. Complementary NAND gates were also printed with similar rise and fall times to the complementary inverter.

In 2013 Baeg *et al*.[81] reported on the inkjet printing of complementary logic gates. Photolithography was used for patterning the gold SD contacts and inkjet for the dodecylthiophene (PC12TV12T) semiconductor, poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE) PMMA blend dielectric and via connections. The hole and electron mobilities were found to be ~0.5 cm^2/Vs and NOR, NAND, OR and XOR gates were successfully fabricated. Later in the same year the group reported [82] on the fabrication of ring oscillators achieving an output frequency of 80 KHz at a V_{DD} of -30 V. However, the inkjet patterned semiconductor was annealed in an N_2 glove box for half an hour and after dielectric deposition the substrates were baked for a further two hours to remove residual solvent. There are doubts whether these results will translate well into a R2R system. It is not noted whether the frequency was achieved on PEN or on glass (both substrates were used).

Over a period of 14 years the development of large-area printing of electronics has been slow. Devices that have undergone printing-only processes have shown mobilities as high as 0.5 cm^2/Vs. Although a ring oscillator with an output frequency of 80KHz has been partially printed, there is a question whether this is at all transferrable to R2R due to the long curing times involved. The next highest frequency is 300 Hz, but once again this is from transistors that have photolithographically patterned SD contacts. The highest frequency of an all-printed device is a modest 6 Hz. The relatively low mobilities and low frequency devices

means that there is potential for improving device performance. A number of the reports above are R2R compatible, and are not considered true R2R due to the fact that the printing is done in stages rather than one continuous process. The hurdle many of these groups now face is to be able to fit the stages together to form one continuous process and addressing the issue of registration.

2.6 Summary and the Path Forward

This chapter has reviewed the concepts and literature relevant to the work reported in the following chapters.

Selection of an appropriate dielectric is key to the fabrication of OTFTs due to the fact that it determines the interface properties that are integral to device operation.

Following the description of an OTFT, the operation of an inverter was discussed and the measurements needed to evaluate its performance, namely its voltage transfer performance and dynamic response to a square wave input. An additional driver transistor either in parallel or in series with the original driver transistor of the inverter gives the NOR and NAND gate circuit respectively. The characteristics of both can be measured by using the same techniques as for the inverter. The output signal of a working gate will conform to a truth table based on the input signals of the respective devices.

The construction and operation of ring oscillators was then discussed. The ring oscillator is characterised by measuring the frequency of the output voltage, V_{OUT}.

There is a significant effort underway worldwide to print such circuits using techniques commonly used in industry. Techniques such as gravure, flexographic, screen and inkjet printing have all been used by research groups to fabricate transistors and other devices.

One avenue that has not been explored is the R2R vacuum production of large area electronics. We wish to explore the viability of such an approach as an alternative to conventional printing methods. The work proceeded in a series of steps leading towards the goal of fully integrated R2R electronics. First was the effort to achieve a high transistor yield that is required for the printing of integrated circuits. High yield alone is insufficient for good devices, and an average mobility of ~ 1cm^2/Vs had to be

realised. Once a high yield of transistors with good mobility can be achieved (>1 cm^2/Vs) it will be possible to fabricate integrated inverters. If it is possible to fabricate a high yield of inverters, then it should be possible to fabricate functioning ring oscillators that can produce a clock signal for a circuit. If a ring oscillator can be fabricated then more complex switching elements will be attempted, namely NOR and NAND logic gates. With these logic gates it is possible to achieve any logic function, making them an essential steppingstone towards realising fully integrated circuits. If by using the vacuum deposition technique it proves possible to fabricate such devices, then more complex devices will be designed and fabricated.

The purpose of the present work then is to demonstrate an alternative route for the R2R fabrication of electronics to the conventional methods dependent of solution-processed materials. Solution processing, although convenient, requires the use of solvents as a carrier material for the deposition of the desired materials. There are disadvantages for such processes. First is the introduction of a possible impurity in the crystal structure of the semiconductor and dielectric layers. This may lead to device instability. Evaporation of the solvent from the dielectric layer may leave pinholes in the surface that can lead to device failure. Solvents must be carefully selected in order to avoid damage and interdiffusion of previously deposited layers. There are also delays introduced by the use of solvents, as there is an associated drying time for the evaporation of the solvent from the transistor layers. Often an anneal is required for optimal device performance. Both of these will potentially slow down an R2R process using solution deposited materials.

By using vacuum deposition techniques the above problems are avoided. The semiconductor and dielectric layers can be deposited in their purest forms, free of contamination. There are no drying times, and no anneal is required. The speed of the process is limited by the deposition time of the materials.

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Chapter 3

Materials and Methods

3.1 Introduction

This chapter begins by providing details of the materials used in this work. The methods used for the deposition of those materials are then highlighted. The various device fabrication routes are discussed, detailing device configuration and deposition order. These range from transistors, through inverters, NOR/NAND gates and NOR/NAND SR Flip-flop, to five-stage and seven-stage ring oscillators. The masks that were designed and used for the deposition processes are shown, together with details of the devices that are patterned from the respective mask sets. Also provided here are details of the methods used for characterising deposited films and the electrical measurements made on the fabricated devices.

3.2 Materials

Naphtho[2,3-b]naphtho[2′,3′:4,5]thieno[2,3-d]thiophene (DNTT) semiconductor material was supplied as required by Dr. J. Morrison at Manchester University and stored in a glovebox under N_2 when not in use. The dielectric materials used were polystyrene (PS) (av MW – 350,000), tri(propylene glycol) diacrylate (TPGDA) and thermally grown silicon dioxide (SiO_2). PS was purchased from Sigma Aldrich, Si/SiO_2 wafers purchased from Active Business Company GmbH and TPGDA supplied deposited onto substrates pre-metallised at Bangor, by Mr Z. Ding at Oxford University. Solvents for cleaning, i.e. acetone, 2-propanol and methanol, were used as supplied and were of greater than 99.5 % purity. Solvents were purchased either from Sigma Aldrich or Stratlab Laboratory Supplies. Hexamethyldisilazane (HMDS) was purchased from Sigma Aldrich.

Devices were fabricated on the planarized side of 250 μm thick polyethylene naphthalate film (PEN, supplied by DuPont Tenjin) or silicon wafers with a 300 nm thick thermally grown oxide. The PEN substrate size varied depending on the mask set used. For mask sets 1 and 2 the PEN was cut into 2.5 cm x 2.5 cm squares. For

mask sets 3 – 5 PEN substrates were cut into larger 6.5 cm x 6.5 cm squares so that they could be clamped in place in the mask holder.

3.2.2 Synthesis of DNTT

DNTT was synthesised by Dr J. Morrison at Manchester University using the same route as publicised in [1].

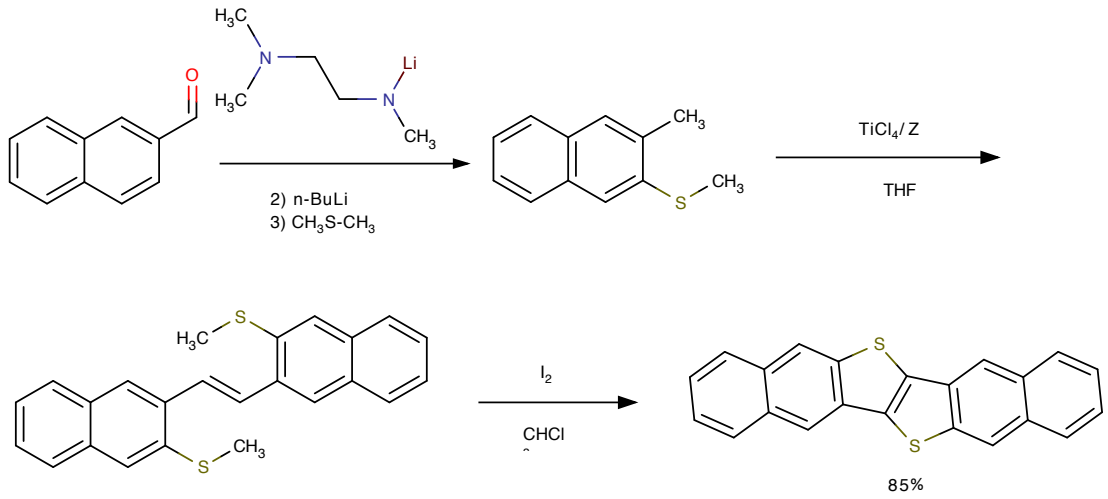

Figure 3.1 Synthesis of DNTT. (Adapted from [1])

The final step of purifying the DNTT can be undertaken by using either sublimation or recrystallization. For the work to be completed here samples of sublimated DNTT, sublimated recrystallized DNTT and recrystallized DNTT were supplied.

3.2.3 Preparation of TPGDA Dielectric

The process for the deposition of the TPGDA monomer (Figure 3.2) to form a polymer layer is described in detail in [2]. First the monomer in its liquid form is degassed and it is then turned into a molecular gas within an enclosure under controlled temperature conditions that prevent it from reforming a liquid and from polymerizing. The molecular gas is ejected from the chamber through a nozzle and condenses on contact with the substrate. Subsequently, the film is polymerized by either plasma or electron-beam curing to form a solid pinhole free film with a root mean square roughness of 5 Å [3].

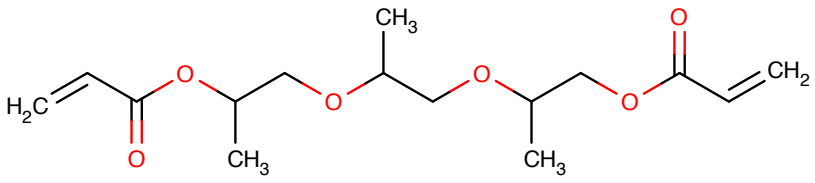

Figure 3.2 TPGDA monomer

This can be done at web speeds of 25 m min^{-1}, the thickness being controlled by the flow rate of the TPGDA monomer into the vaporising chamber.

3.3 Substrate Cleaning

Substrates were placed in a substrate holder and cleaned as follows:

10 minutes ultrasonication in Decon 90/DI water.

Rinsed in DI water for 15 minutes and dried in a stream of nitrogen

2 x 5 minutes ultrasonication in DI water

2 x 5 minutes ultrasonication in acetone

2 x 5 minutes ultrasonication in methanol

2 x 5 minutes ultrasonication in 2-propanol

Dried in a stream of nitrogen

The substrates were then transferred to a plasma etcher (Diener Electronic) and exposed to an oxygen plasma for 2 minutes to eliminate any remaining organic mater.

3.4 Fabrication Methods

The TPGDA substrates received from Oxford were processed entirely within a nitrogen glovebox (Glovebox Technologies Ltd.) which contained an inbuilt Glovebox Technologies spin-coater and integrated multi source evaporator (Mini Spectros, Kurt Lesker Ltd.).

DNTT was evaporated from a ceramic crucible at a rate of 0.4 $Å/s^{-1}$ and a pressure below 5 x 10^{-6} mbar, the thickness of the layer was measured by monitoring step height using atomic force microscopy (AFM). Gold and aluminium were evaporated at a rate of 1 $Å/s^{-1}$ and at a pressure below 5 x 10^{-6} mbar. Metallisation was also undertaken in an Edwards evaporator at a rate of 1 $Å/s^{-1}$ and a pressure below 8 x 10^{-6} mbar for chrome/gold deposition when fabricating bottom contact transistors patterned by photolithography.

3.5 Device Fabrication

3.5.1 Si/SiO_2/DNTT Transistor Fabrication

In the first set of experiments carried out, DNTT was deposited onto the oxidised Si wafers to form top-contact/bottom-gate transistors (Figure 3.3). The gate contact was made by scratching through the 300 nm thick SiO_2 layer to the underlying Si prior to substrate cleaning due to the amount of dust created.

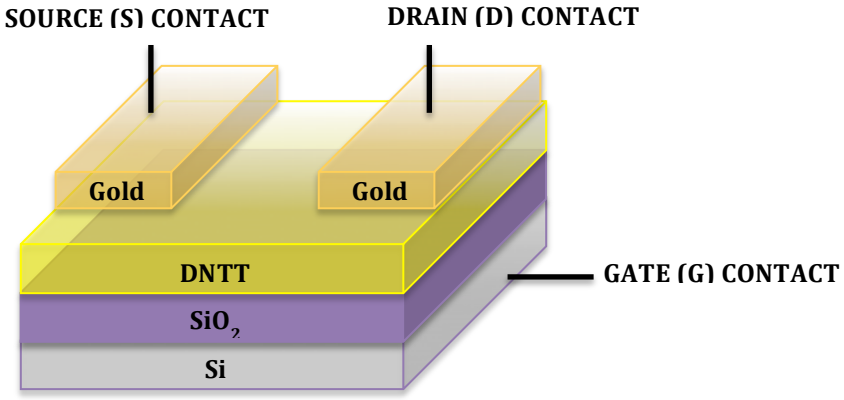

Figure 3.3 Schematic cross section of a transistor fabricated on a silicon substrate.

HMDS was pipetted onto the substrate and left to stand for 1 minute. It was then spin-coated at 1500 rpm for 1 minute after which the substrate was placed on a hot plate for 1 minute to dry off any remaining solvent. 70 nm DNTT was deposited through a shadow mask to define the semiconducting layer. 30 nm thick gold source and drain electrodes were deposited by thermal evaporation in vacuum through the source-drain shadow mask of Mask Set 1 (section 3.5.6, Figure 3.8 (a)) to yield devices with the schematic cross-section seen in Figure 3.3. Finally, a drop of silver paste was used to create a contact pad to the Si gate.

3.5.2 Bottom-Contact-Top-Gate PS/DNTT Device Fabrication

For bottom-contact devices (Figure 3.4) 5-nm chrome and 30-nm thick gold films were deposited by thermal evaporation in vacuum onto a PEN substrate. Source and drain contacts were patterned by photolithography and acid etching of the chrome/gold layer.

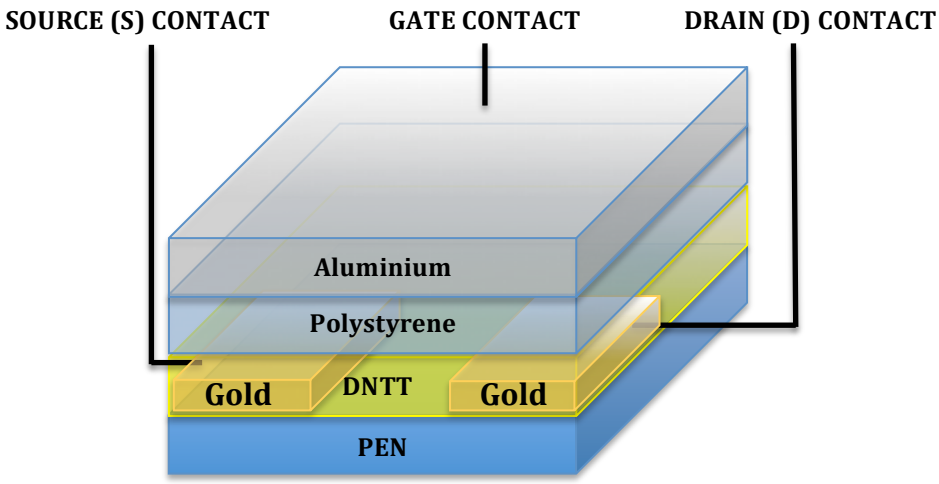

Figure 3.4 Schematic cross section of a top-gate bottom-contact PS/DNTT transistor fabricated on a PEN substrate.

A S-1818 photoresist layer was spun on at 1000 rpm and the substrate then placed on a hot plate for 1 minute. Subsequently the photoresist layer was exposed to UV light for 15 s (Electronic Visions Co EV420) through the source-drain photo mask of Mask Set 2 (section 3.5.6, Figure 3.8 (b)). A MF 319 photoresist developer was then used to remove the exposed photoresist. The exposed gold layer was removed by Aqua Regia, and the chrome removed by chrome etch. The remaining unexposed photoresist was removed using SVC 175 photoresist etch to leave the patterned gold contacts. The substrate was then transferred to the plasma etcher and exposed to an oxygen plasma for 2 minutes to eliminate any remaining organic mater. The remaining steps were completed in a glovebox under N_2 atmosphere. 70-nm thick DNTT was deposited by thermal evaporation through a shadow mask from Mask Set 2 to define the semiconducting layer. The dielectric layer was produced by spin coating a 10% wt solution of polystyrene in toluene at 1000 rpm for one minute. The substrate was then placed on a hot plate for 10 minutes at 100 ^{O}C to dry off any remaining solvent. The resulting dielectric layer was ~1.4 µm thick as determined by AFM measurements. Finally, 70 nm thick aluminium was deposited by thermal evaporation in vacuum through the gate shadow mask of Mask Set 2 to define the gate contact of the OFET and inverter devices, giving the schematic cross-section seen in Figure 3.4.

3.5.3 Top-Contact-Bottom-Gate PS/DNTT Device Fabrication

Mask Set 3 (Figure 3.9) was used for patterning an array of 90 x OTFTs and 5 x MIS capacitors. The deposited layers yielded devices with the schematic cross section

shown in Figure 3.5. All steps were completed within a glovebox under an N_2 atmosphere.

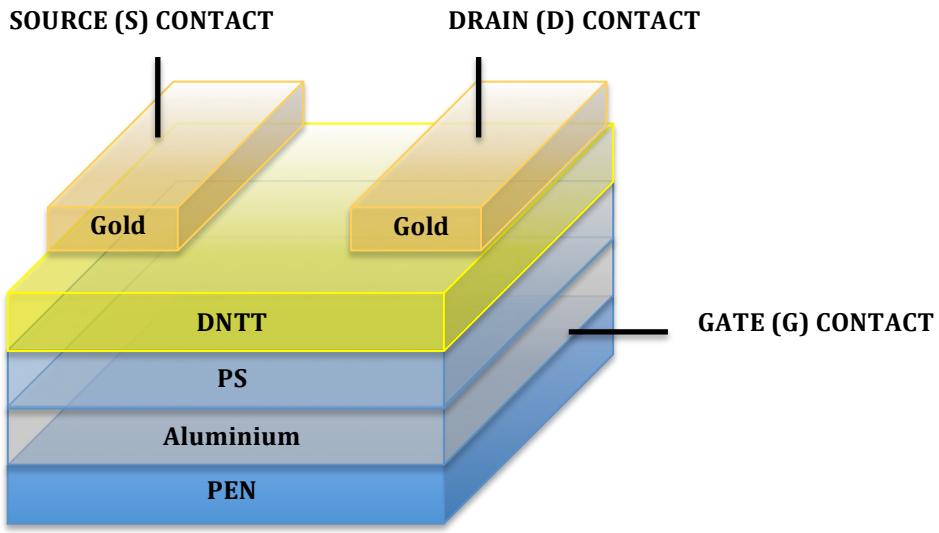

Figure 3.5 Schematic cross section of a bottom-gate top-contact PS/DNTT transistor fabricated on a PEN substrate.

For the bottom-gate top-contact PS/DNTT OTFTs, 70-nm thick aluminium was first deposited onto the PEN substrate by thermal evaporation through the gate shadow mask to define the gate electrodes. PS was spin coated from 9% wt/wt in toluene at 1000 rpm onto the metallized substrate to form a ~1 µm thick dielectric layer. The substrate was then placed on a hot plate for 10 minutes at 100 ^{O}C to dry off any remaining solvent. A 70-nm thick DNTT film was deposited onto the PS by thermal evaporation through a shadow mask to define the area of the semiconductor. Finally, 60-nm thick gold was deposited by thermal evaporation through the source-drain shadow mask to complete the devices.

3.5.4 TPGDA/DNTT Device Fabrication

Only bottom gate devices were used for fabricating devices utilising the TPGDA dielectric due to the UV curing process of the TPGDA being harmful to the DNTT layer. Mask Sets 1, 3 and 4 were used for fabricating TPGDA/DNTT devices with the schematic cross-section shown in Figure 3.6.

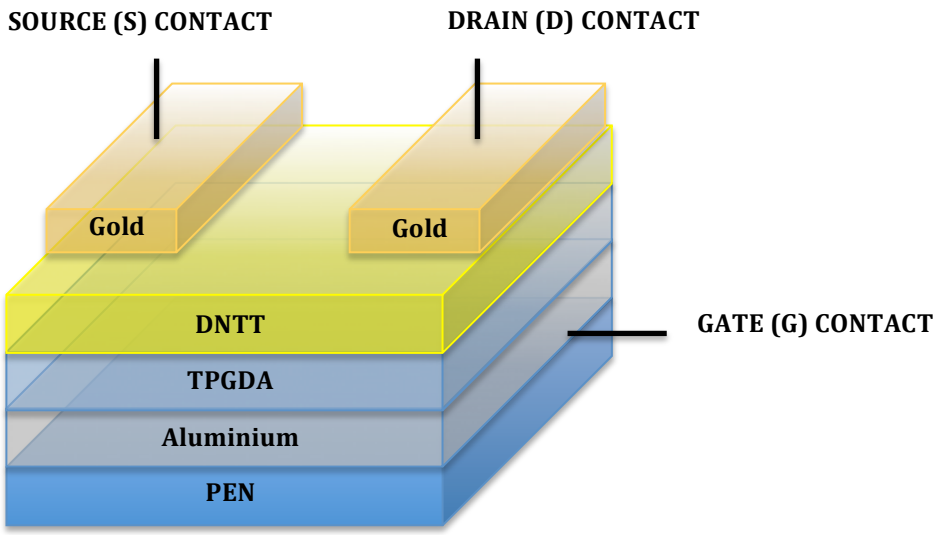

Figure 3.6 Schematic cross-section of a bottom-gate top-contact TPGDA/DNTT transistor fabricated on to a PEN substrate.

For the bottom-gate top-contact devices 70-nm thick aluminium was deposited onto a PEN substrate by thermal evaporation through a shadow mask to define the gate electrodes. The substrates were then dispatched to Oxford in sealed petri dishes where they were fixed onto the water-cooled drum of a web coater (Aerre Machines) and rotated at a linear speed of 25 m/min. Tri(propylene glycol) diacrylate (TPGDA) monomer vapour was directed onto the metallized substrate where it condensed forming a thin liquid layer of uniform thickness which immediately passed under a plasma source where it cross-linked to form an insulating layer [2,3]. The substrate passed under the TPGDA nozzle multiple times as the drum rotated, the number of rotations determining film thickness. Once returned to Bangor, 70-nm thick DNTT was deposited by thermal evaporation through a shadow mask to define the semiconducting channel. Finally, 60-nm thick gold was deposited by thermal evaporation in vacuum through a shadow mask to define the source and drain contacts of the OFET and inverter devices.

3.5.5 PS-TPGDA/DNTT Device Fabrication

Fabrication of the PS-TPGDA/DNTT devices followed the same procedures as described in section 3.5.4 except that an additional PS layer was spin-coated onto the TPGDA to form a buffer layer between the TPGDA and the DNTT, giving devices with the schematic cross-section shown in Figure 3.7.

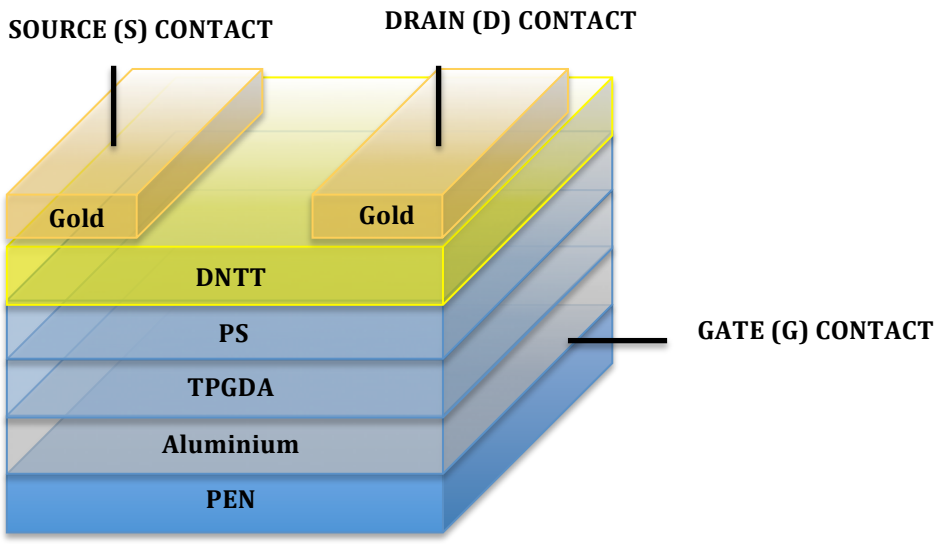

Figure 3.7 A cross section of a bottom-gate top-contact DNTT-PS/TPGDA transistor fabricated on to a PEN substrate.

Mask Sets 3-5 (section 3.5.6, Figures 3.9, 3.10 and 3.11) were used to pattern these devices. Once substrates were returned from Oxford the subsequent steps were conducted in a nitrogen glovebox to complete the processing. The PS was spin coated from 3% wt solution in toluene at 1000 rpm for 1 minute and the substrate then placed on a hot plate for ten minutes at 100 ^{0}C to remove any remaining solvent.

3.5.6 Mask Designs

Dr C. P. Watson designed Mask Sets 1 and 2 depicted in Figure 3.8. Mask Set 1 features three sets of transistors with the dimensions shown in Figure 3.8 (a) and a circular capacitor of diameter 4mm. Mask Set 2 features two sets of transistors, four interdigitated transistors connected to form a pair of inverters, and a ring guarded capacitor that can also be connected as a transistor. The device dimensions are given in Figure 3.8 (b).

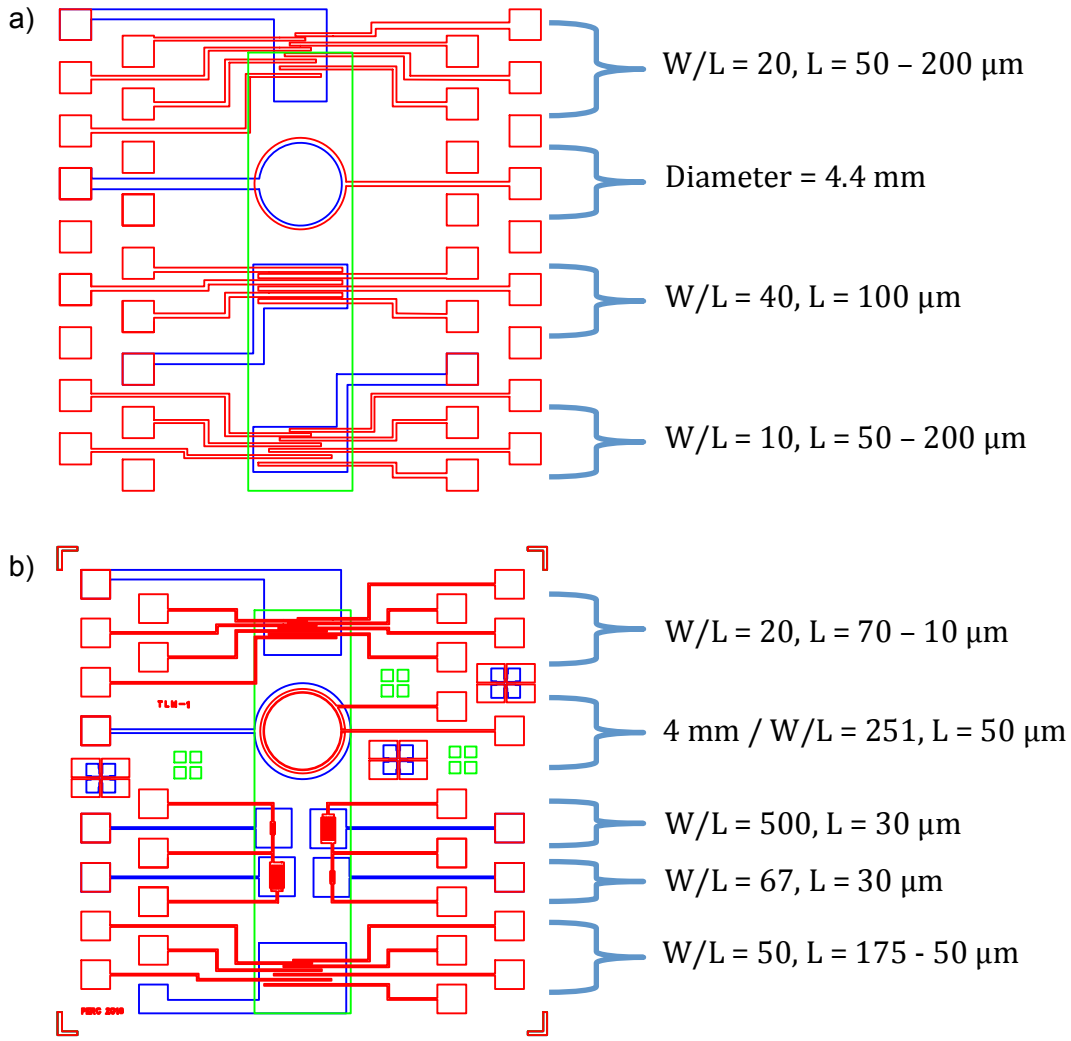

Figure 3.8 a) Mask Set 1 and b) Mask Set 2, SD contacts are depicted in red, G contacts in blue and semiconductor in green.

The author designed the following Mask Sets. Mask Set 3 (Figure 3.9) features 90 transistors, arranged in five rows of eighteen labelled A-E and numbered 01-18 from left to right. The channel length L for OTFTs in each row are as follows - 50 µm (A), 75 µm (B), 100 µm (C), 150 µm (D) and 200 µm (E). For devices numbered 01-09 W was fixed at 2 mm. For devices numbered 10-18 the W/L ratio was fixed at 20 so that W ranged from 0.5 mm (row A), to 4 mm (row E). The design makes it possible, therefore, to investigate the variation in mobility due to changes in the W/L ratio.

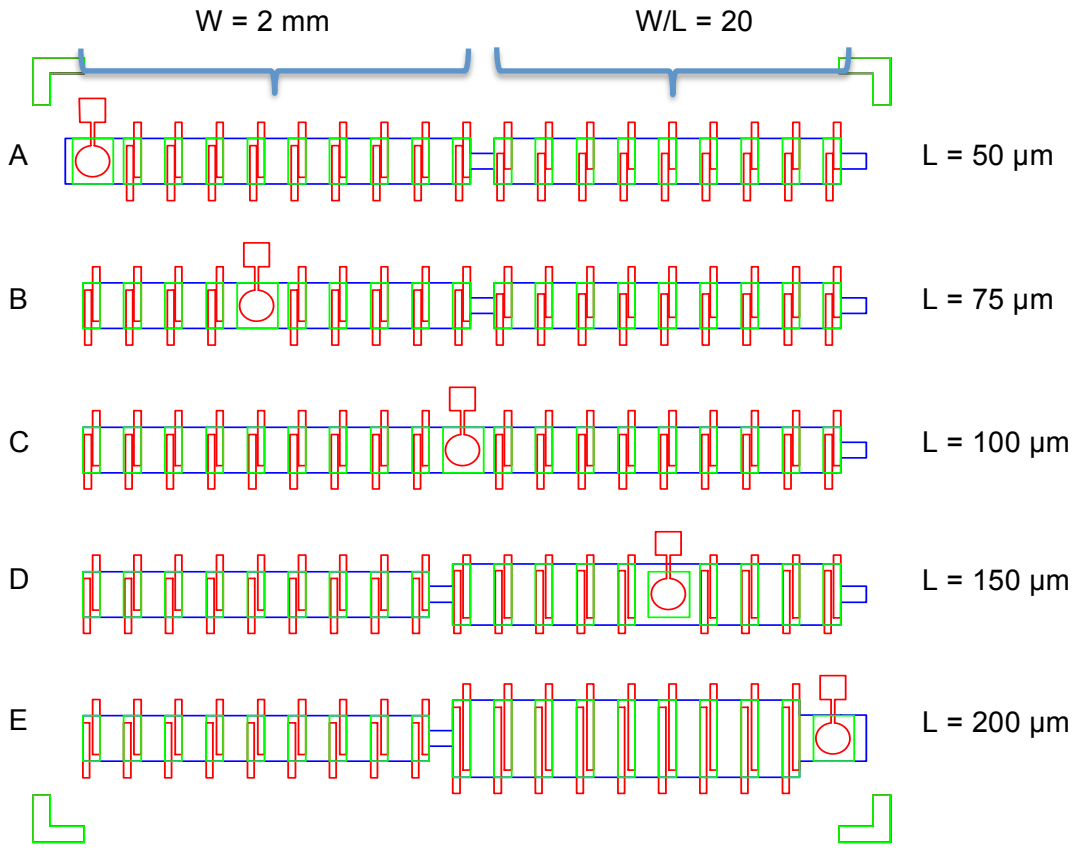

Figure 3.9 Mask Set 3, SD contacts are depicted in red, G contacts in blue and semiconductor in green. Five circular capacitors of 2mm diameter were used to determine the capacitance per unit area of the dielectric layer.

The mask also features five circular capacitors, diameter 2 mm, arranged diagonally across the substrate in order to determine the uniformity of the dielectric thickness and hence of C_i, the capacitance per unit area of the OTFTs. The mask was designed with the final R2R process in mind, i.e. incorporating significant overlap between layers to accommodate a large degree of registration error. The DNTT is over 100 µm wider than the channel L and also extends beyond the channel W. The gate width is also wider than the channel W by 0.45 mm at each end for the majority of the transistors.

Mask Set 4 (Figure 3.10) features 9 NAND gates and 9 NOR gates. The design is such that it also allows the characteristics of each transistor to be measured individually.

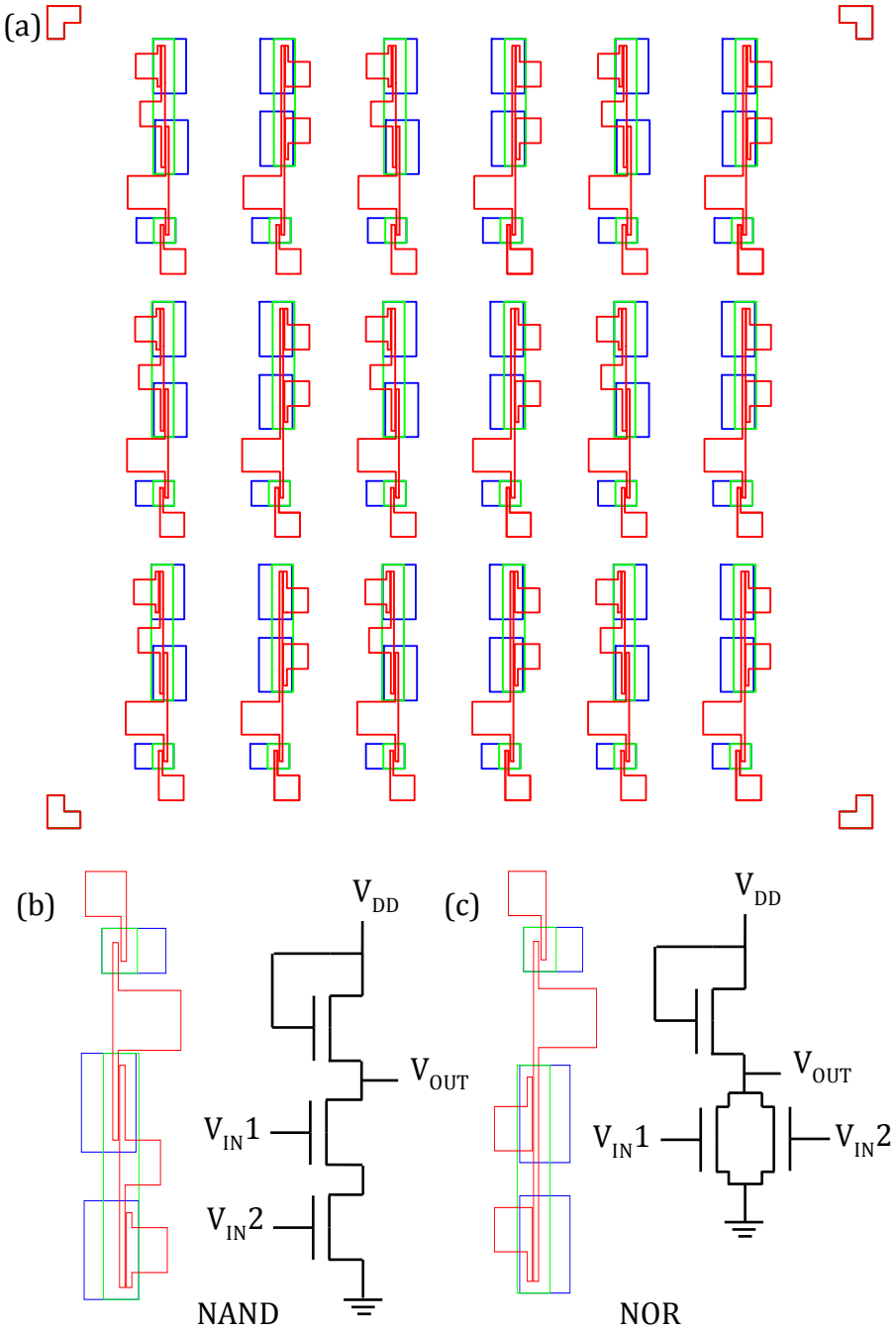

Figure 3.10 (a) Mask Set 4, consisting of 9 NAND and 9 NOR gates. SD contacts are depicted in red, G contacts in blue and semiconductor in green. The layout and circuit description of individual NAND (b) and NOR (c) gates.

In each gate the driver OTFT channel L = 50 µm and W = 2.5 mm. For the load OTFT L = 100 µm and W = 0.625 mm. This gives a conductance ratio of 8:1. This mask was also designed with the R2R process in mind, keeping to a simple bar design

for the electrodes rather than an interdigitated one and allowing ±100 μm for registration error.

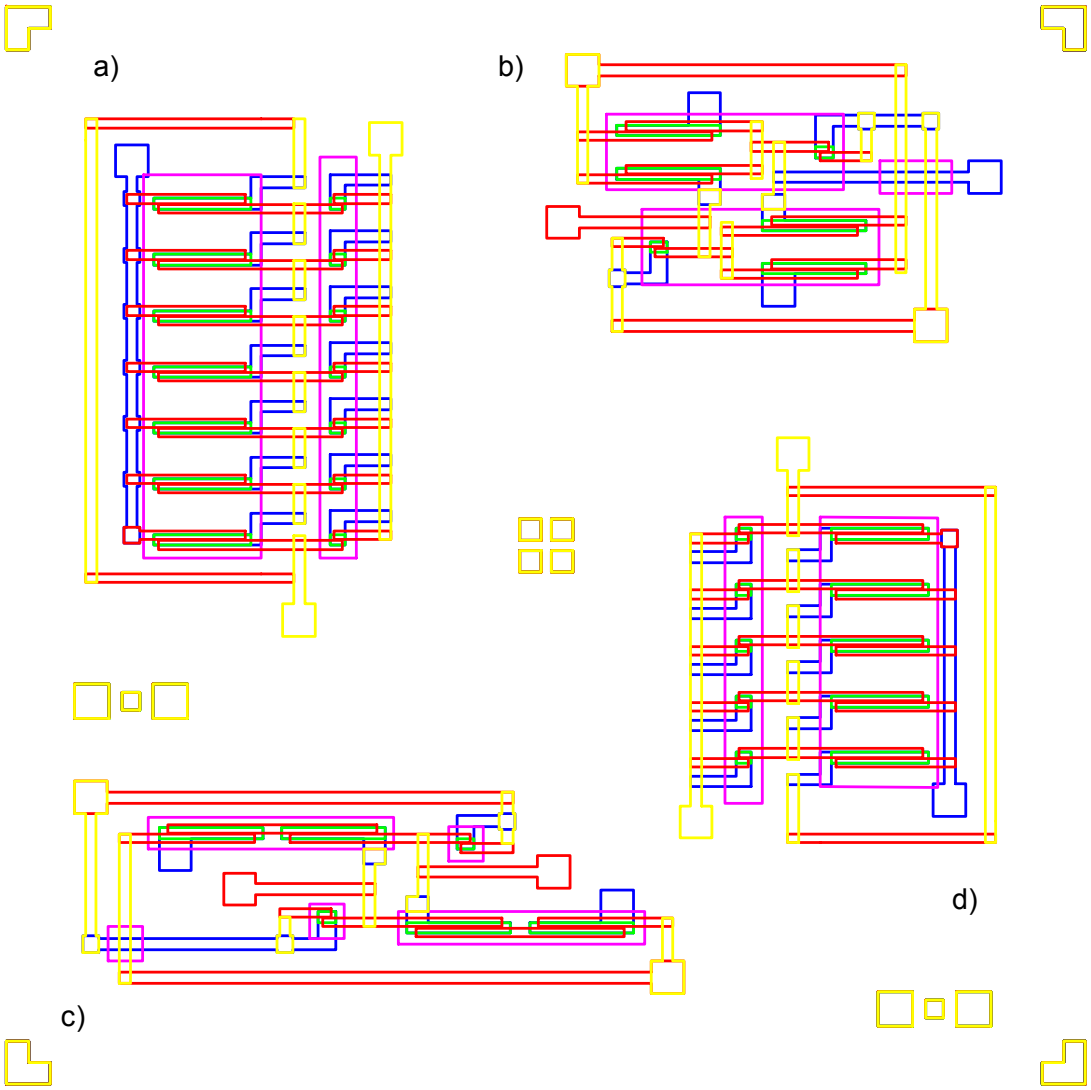

Figure 3.11 Mask Set 5. The first metallisation layer (interconnects) is depicted in yellow, the second metallisation layer (SD contacts) in red, G contacts in blue, dielectric apertures in pink and semiconductor in green. The design allows (a) 7-stage ring-oscillator, (b) NOR SR flip-flop, (c) NAND SR flip-flop and (d) 5-stage ring-oscillator circuits to be fabricated

Mask Set 5 (Figure 3.11) features one 7-stage (3.9 (a)) and one five-stage (3.9 (d)) ring oscillator. It also features one NAND SR flip-flop gate (3.9 (c))and one NOR SR flip-flop gates (3.9 (b)). The dimensions of each driver OTFT are L = 50 μm and W = 4 mm. For the load OTFT the dimensions are L = 50 μm and W = 0.4 mm. Although the trans-conductance ratio is increased to 10:1 compared with the devices in Mask Set 4, the output current of both the driver and load transistors here is higher.

3.6 Surface Characterisation

The surface topography and thicknesses of the dielectric, semiconductor and contact layers were investigated by atomic force microscopy (AFM) (DI, Nanoman V) operated by Dr Y. Hong. The thicknesses of the various films were determined by scribing the film with a specially made steel scribe to create a step. The heights of the steps were then measured using AFM. The topography of the deposited layers was imaged in tapping mode with the resulting image converted to a 3D image using Image SXM.

3.7 Transistor Characterisation

As organic molecules are photosensitive, device characteristics were obtained in a dark room.

Early measurements (chapters 4 and 5) were conducted using an in-house built probe station, consisting of three probes mounted on micromanipulators. Later measurements (chapters 5-8) were conducted using a (Sel-tek limited - Signatone 1160 Series) probe station mounted within an aluminium box to minimize the effects of electromagnetic interference when measuring low currents.

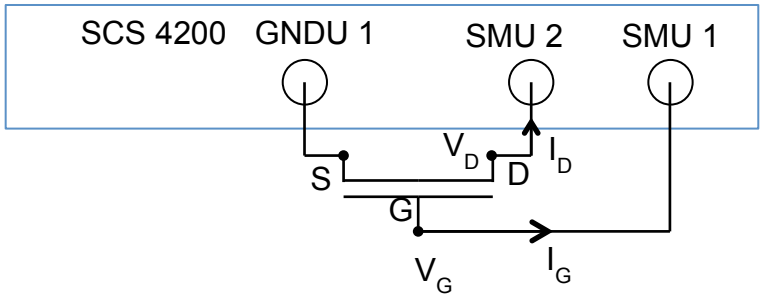

Figure 3.12 Schematic representation of the setup used for transistor characteristics measurements.

The Keithley SCS 4200 Semiconductor Characterisation System (Keithley Instruments Inc.) is connected to three probe tips mounted on micromanipulators. This allowed connections to be made to the source (S), drain (D) and gate (G) electrodes of the fabricated transistor that complete a circuit (Figure 3.12).

Transfer (I_D vs V_G) and output (I_D vs V_D) measurements were recorded as well as gate leakage currents. For the measurements, the source contact was grounded (Figure 3.12) with voltages V_D and V_G applied via the SCS 4200 to the drain and gate

respectively. Simultaneously the source-drain (I_D) and gate (I_G) currents were measured at the drain and gate contacts respectively. The measurements were conducted at room temperature in ambient air.

3.8 Circuit characterisation

3.8.1 Inverter Characterisation

The set-up used for characterising the inverter (Figure 3.13) was similar to the one for transistor measurements.

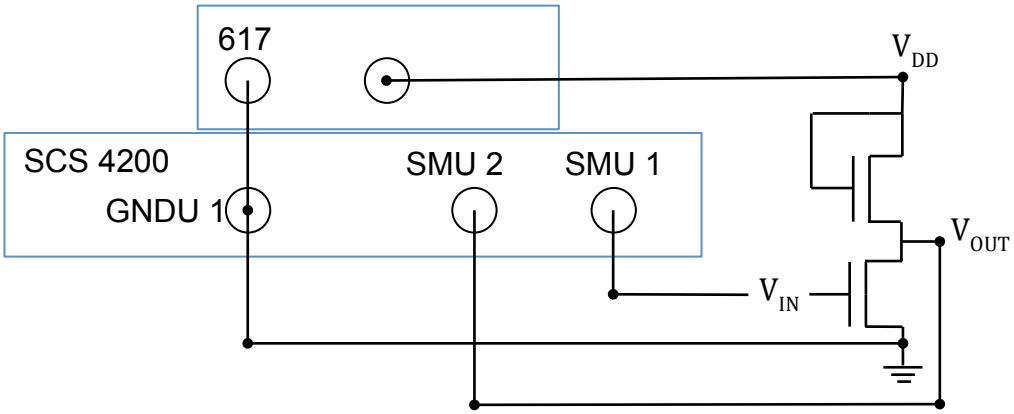

Figure 3.13 Schematic diagram of the circuit used to measure the static inverter performance.

However, in addition to the Keithley SCS 4200 connected to the source, drain and gate of the driver transistor contact to the inverter was completed with a fourth probe connected to a Keithley 617 to provide the rail voltage. A common ground was established between both instruments. For time response measurements, a test box was designed with external coax contacts connected to gold pins inside the box. Circuits were completed by using silver paste and gold wire between the test circuit contacts and gold pins. Initially the Keithley SCS 4200 was used to measure the dynamic response of inverter devices, and was usefull in showing that devices were operating as intended. However, it proved to be too slow for the response time measurement time scales. Later a digital storage oscilloscope (Agilent DSO-X 2014A) was used to measure the dynamic time response of the inverter by connecting it to the circuit output via a buffer amplifier to minimise loading effects. The time scale of the measurements of the output voltage varies dependent on device and input signal frequency, these will be given in the relevant chapters.

3.8.2 Ring Oscillator Characterisation

The ring oscillators were characterised using the circuit arrangement shown in Figure 3.14.

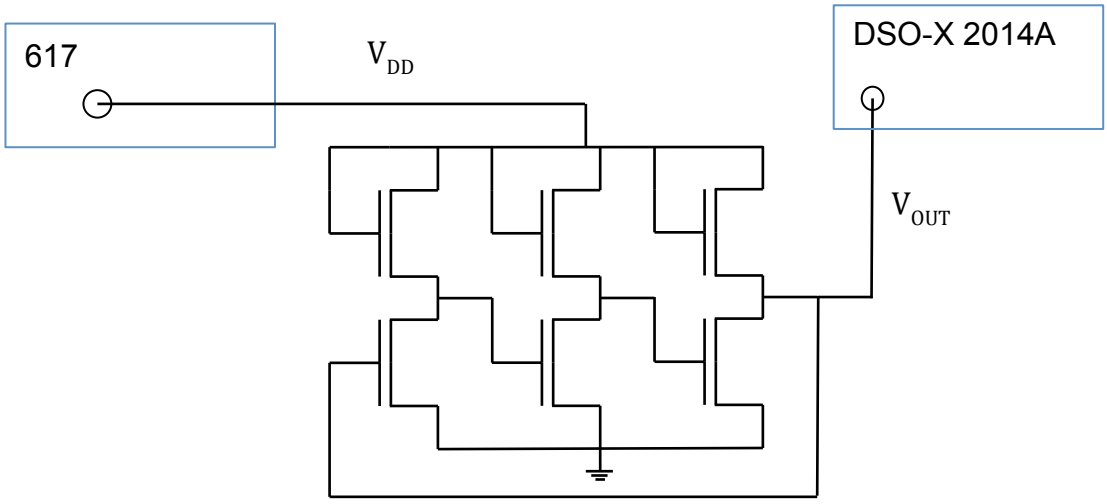

Figure 3.14 Schematic representation of the setup used to measure the output frequency of ring oscillators.

The Keithley 617 was again used as voltage supply unit for the V_{DD}. Time response was then measured using a digital storage oscilloscope (Agilent DSO-X 2014A), the signal passing through a buffer-amplifier to minimise oscilloscope loading on the ring oscillator. As with the inverters the ring oscillator was placed in the test box and contacts connected to pins using silver paste and gold wire.

3.8.3 Characterisation of NOR/NAND and SR Flip-flop

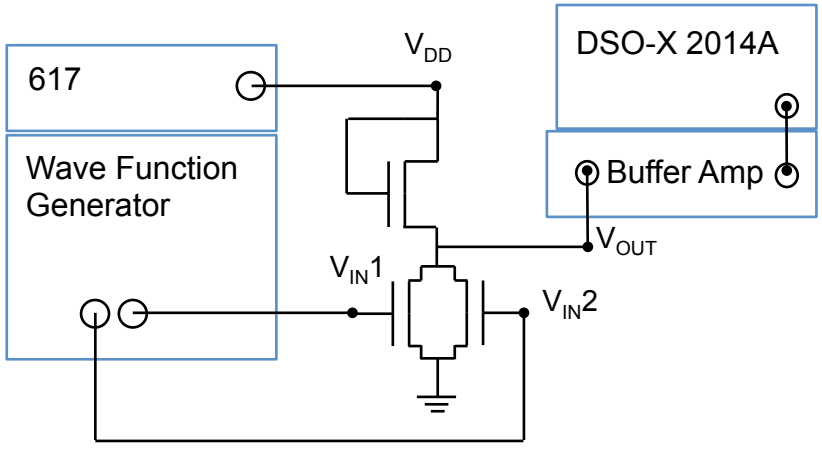

Figure 3.15 Schematic representation of the setup for the time response measurement of NOR devices.

The NOR/NAND and SR Flip-flop responses were investigated using the setup shown in Figure 3.15. The two input signals were supplied from a wave function generator (TTi TGA 1242 waveform generator) through amplifiers (Falco Systems DC-20KHz High Voltage Amplifier WMA-01) and the output signal measured using the digital oscilloscope (Agilent DSO-X 2014A) connected to the circuit via a buffer amplifier.

3.9 Capacitance Measurements

The capacitance of the dielectric layer was measured on an Agilent 4284A precision LCR meter (Agilent Technologies UK Ltd.). The set up is shown in Figure 3.16.

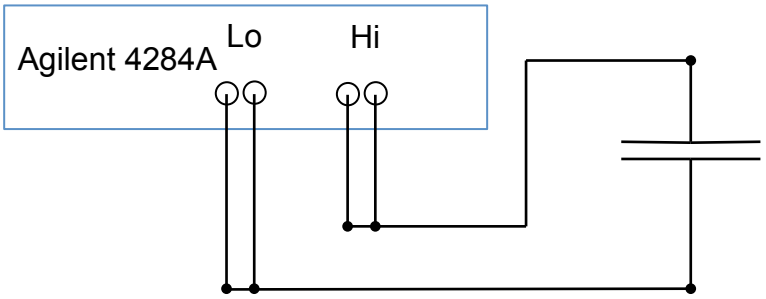

Figure 3.16 Schematic representation of the circuit connections from the Agilent 4284 to the capacitor

Prior to the measurement the excess semiconductor layer was carefully removed from around the capacitor electrode to limit any lateral conduction effects. Measurements were conducted in the dark at room temperature in atmospheric conditions.

3.10 Summary

The information in this chapter has detailed the materials used and from where they were obtained. The experimental methods and characterisation techniques have also been described, together with the mask designs for making transistor based devices. All of the above techniques and processes were used in obtaining the results described in the subsequent chapters.

3.11 References

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Chapter 4

SiO_2/DNTT Transistors

4.1 Introduction

Although not compatible with the philosophy of an all-vacuum process, the work described in this chapter was, nonetheless, important since it provided feedback on the best purification method for DNTT. There is a requirement to purify the material, as unreacted precursor material may be present, as well as unwanted isomers and reactants.

The synthetic route used by our Manchester University collaborators to prepare DNTT is described in section 3.2.2. In the case of small molecule organic semiconductors the two methods in general use for cleaning up the final product are sublimation and recrystallization. Sublimation is the process of heating the solid, turning it directly into a gas without entering the liquid phase, and then cooling to reform the solid. This is based on the idea that the contaminants do not sublimate, and that only a pure product is collected. To recrystallize a sample, the solid is dissolved in a solvent and is then displaced from the solvent by an additional reactant so that it drops out. The mixture is then filtered and the required sample crystallizes. The latter has the benefit of reducing the time to synthesise DNTT and can produce larger yields. On the other hand sublimation is regarded as having the advantage of yielding a purer product.

This chapter explores the effect of this final purification step on the performance of DNTT OTFTs, and whether using recrystallized DNTT has an adverse effect on transistor performance. If it does not, then it will be the favoured method for the purification of DNTT due to the higher yield, and therefore, reduced material waste.

Three purification methods were used (a) recrystallization, (b) sublimation and (c) sublimation followed by recrystallization. The three samples of DNTT are referred to as R-DNTT for recrystallized DNTT, S-DNTT for sublimated DNTT, and SR-DNTT for sublimated and recrystallized DNTT. The transistor performance of

each sample was used to determine which DNTT sample would be used for the remainder of the project work.

For each sample of DNTT, two substrates of 18 transistors were fabricated using mask set 1 (Figure 3.6 (a)). For comparison the transistors from the three samples of DNTT were fabricated on n++ doped Si/SiO_2 substrates diced from a single Si/SiO_2 wafer treated with hexamethyldisilazane (HMDS) self assembled monolayer (SAM). This minimised uncertainty arising in the extracted mobility due to variability in the dielectric.

4.2 Results

Figure 4.1 shows AFM images of the surface topography of S-DNTT, SR-DNTT and R-DNTT deposited onto Si/SiO_2 substrates. The images are representative of a 2 µm x 2 µm area within the channel region of the respective OTFT.

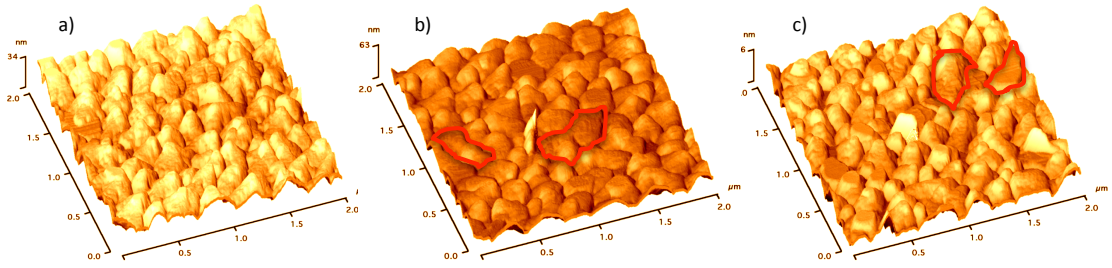

Figure 4.1 AFM images of the three samples of DNTT (a) S-DNTT, (b) SR-DNTT and (c) R-DNTT taken from within corresponding transistor channels. The large crystals found in R-DNTT and SR-DNTT are highlighted in red. (image area 2 µm x 2 µm)

The size scale of the DNTT grains is similar in all three cases (0.2-0.4 µm). However, in the SR-DNTT (b) and the R-DNTT (c) images there are a number of slightly larger crystals that are ~ 0.5 µm (such as those highlighted in red) that are absent in the S-DNTT image (a). Also the S-DNTT image shows a more uniform grain size structure, and a root mean square (RMS) surface roughness of 6.6 nm, compared to 7.5 nm for R-DNTT and 7.8 nm for SR DNTT.

Figure 4.2 shows a typical set of results obtained from a R-DNTT OTFT. Output characteristics (I_D vs V_D) are shown in (a) while in (b) transfer characteristics are shown for the linear regime (I_D vs V_G, V_D = -2 V) and in the saturation regime ($I_D^{1/2}$ vs V_G, V_D = -60 V). In (c) the transfer data is replotted in semi-log form. The inset in (c) shows the gate-voltage dependence of mobility in the two regimes, i.e.

μ_{lin} and μ_{sat} extracted using equations (2.11) and (2.12) respectively. In all measurements, the hysteresis was negligible.

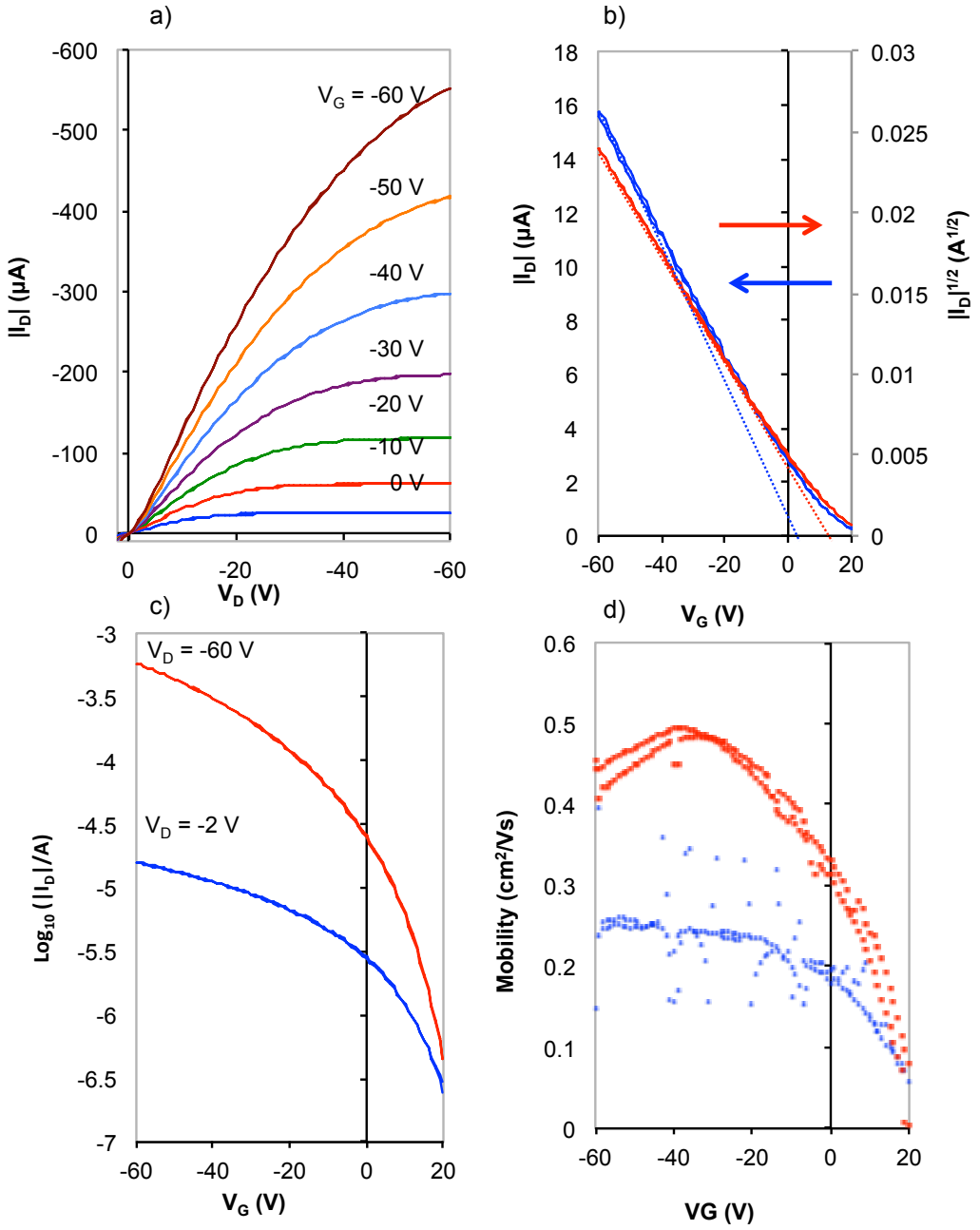

Figure 4.2 Results obtained from an R-DNTT transistor. W = 4 mm, L = 100 µm, C_i = 1.151 x 10^{-8} F/cm^2. (a) Output characteristics plotted from a V_G of 0V to -60 V in -10 V increments. (b) plots of I_D in the linear regime in blue (V_D = -2 V) and $I_D^{1/2}$ in the saturation regime in red(V_D = -60 V) vs V_G. (c) Semi-log plots of I_D vs V_G in the linear regime (blue) and saturation regime (red). The corresponding mobility plot for both regimes is inset.

Apart from the light curvature at the lowest values of V_D, probably arising from the presence of a small diode like contact resistance, the output characteristics

(Figure 4.2 (a)) show good transistor performance. The plot of I_D vs V_D for V_G = 0V shows a high current > -20 μA. This fits with the positive V_T and the transistor starting to conduct when V_G ~ 20 V (Figure 4.2 (b)).

The plots for I_D and $I_D^{1/2}$ vs V_G in the linear and saturation regimes respectively, show an upward curvature at low V_G, where I_D is gate voltage dependent. However, both do show a long linear region, the tangent to which (dashed lines) gives a V_T equal to 10 V in the linear regime and 16 V in saturation. As W, L, V_T and C_i are known it is possible to calculate the mobilities of the linear and saturation regimes using equations 2.9 and 2.10 respectively, yielding 0.24 cm^2/Vs for the linear regime and 0.44 cm^2/Vs for the saturation regime.

From Figure 4.2 (c) it is possible to see that in both the linear and saturation regimes, I_D is strongly dependent on V_G. The off currents are not observable as V_G is not set to a positive enough voltage to turn the device off, so the On/Off ratio is determined to be >100 in the linear regime and >1000 in the saturation regime. It can also be assumed that V_{ON} > 20 V. The subthreshold slope in the linear regime is 14.6 V per decade and 8.5 V per decade in the saturation regime.

The V_G dependent mobility is plotted for both regimes in the inset of Figure 4.2 (c). The maximum mobility calculated using equation 2.11 for the linear regime is 0.25 cm^2/Vs (ignoring the points due to noise). Equation 2.12 is used to calculate the saturation mobility for R-DNTT, from which the maximum mobility is 0.49 cm^2/Vs (inset of Figure 4.2 c)). Both the extracted maximum linear and maximum saturation mobilities calculated using equations 2.11 and 2.12 are similar to the mobilities extracted using equations 2.9 and 2.10.

In Figure 4.3 the results for the S-DNTT transistor are shown. Here again the output characteristics are shown in (a), the transfer characteristics in (b), and the replotted semi-log of the transfer characteristics in (c) with the gate dependent mobility in the inset. In the output characteristics (Figure 4.3 (a)), as with the R-DNTT, there appears to be a small diode-like contact resistance effect near the origin. Otherwise the characteristics show good transistor behaviour with good saturation in all plots except at V_G = -60 V. Hysteresis was negligible in all three plots except at the highest V_G in saturation (see Figure 4.3 (b)).

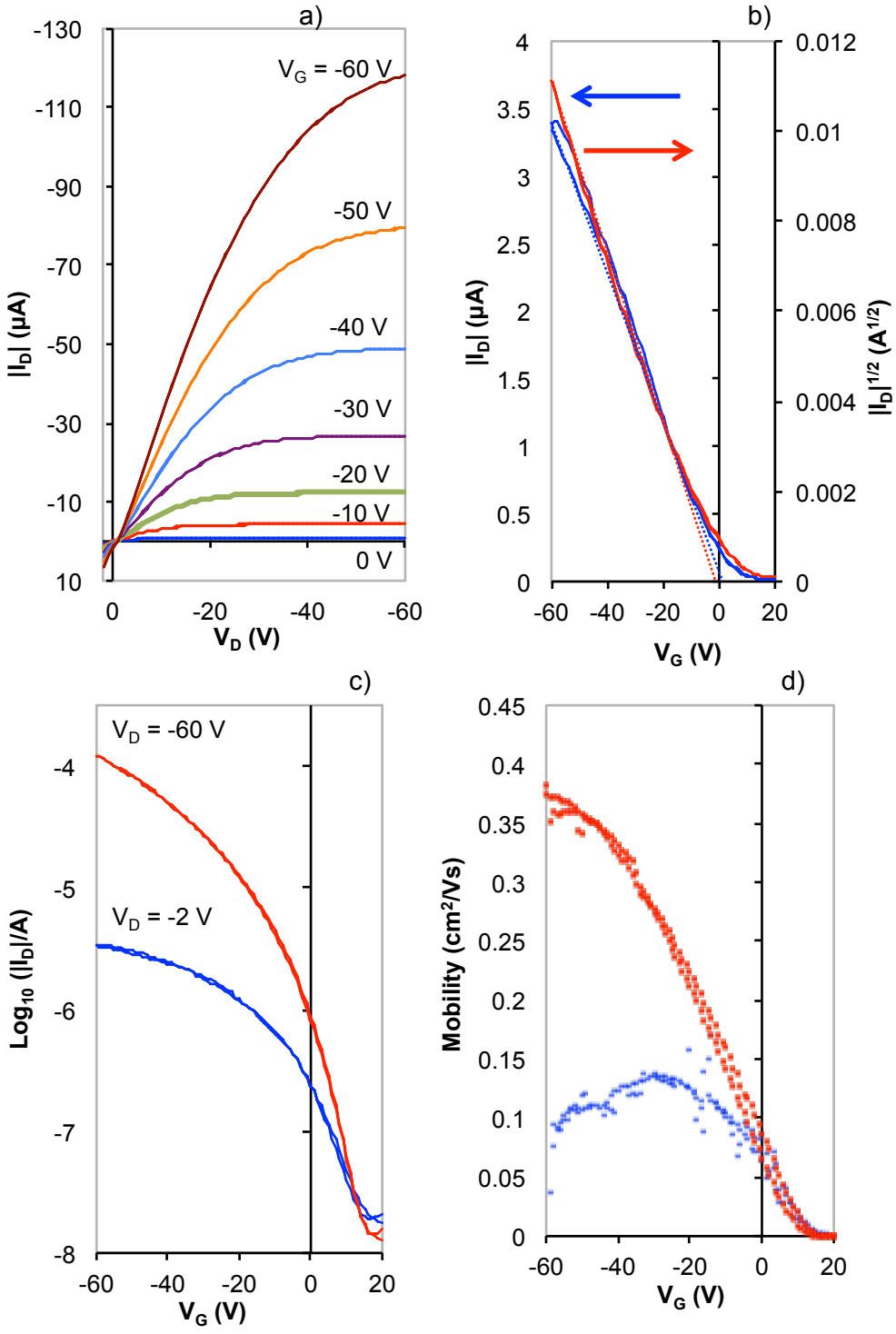

Figure 4.3 Results obtained from an S-DNTT transistor. W = 1.5 mm, L = 75 µm, C_I = 1.151 x 10^{-8} F/cm^2. (a) Output characteristics plotted from a V_G of 0V to -60 V in -10 V increments. (b) plots of I_D in the linear regime in blue (V_D = -2 V) and $I_D^{1/2}$ in the saturation regime in red(V_D = -60 V). (c) Semi-log plots of I_D vs V_G in the linear regime (blue) and saturation regime (red). The corresponding mobility plot for both regimes is inset.

Again it can be seen that there are curved and linear sections in the transfer plots in Figure 4.3 (b). From extrapolation of the linear sections of the plots, V_T is

shown to be 0 V in the linear regime and -2 V in the saturation regime, over ten volts difference in both regimes to the V_T of the R-DNTT.

Using equations 2.9 and 2.10 to calculate the mobility, solving for the respective slopes of the linear and saturation regimes, we obtain 0.13 cm^2/Vs in the linear regime, and 0.32 cm^2/Vs in the saturation regime.

Unlike the R-DNTT OTFT, the off current is observable in both the linear and saturation regimes and is below 50 nA in both cases. V_{ON} in the linear regime is at ~15 V, and in the saturation regime it is ~16 V. The I_{ON}/I_{OFF} ratio of the transistor in the linear regime is $\sim 10^2$ and in saturation is in the range of 10^4. The subthreshold slope is marginally steeper in the linear regime at 14 V per decade than for the R-DNTT, but is shallower in the saturation regime at 8.9 V per decade.

Again using the local slope to calculate mobility, plotted in the inset of Figure 4.3 (c), the maximum linear mobility is 0.14 cm^2/Vs (ignoring points due to noise) and the maximum mobility in the saturation regime is 0.36 cm^2/Vs. Once again both mobility calculations give similar results.

The third set of results shown in Figure 4.4 show SR-DNTT to have very similar characteristics to the R-DNTT sample. As with the other two samples hysteresis in the plots is negligible.

The incremental plots of I_D vs V_D show good transistor behaviour with good saturation except at V_G = -50 V and -60 V. Again the plot of I_D vs V_D in Figure 4.4 (a) shows a high current (> -10 μA) at V_G = 0V, similar to Figure 4.2 (a). As with the other two samples there appears to be a degree of diode like contact resistance at low values of V_D.

From the extrapolation of the linear section of the two plots in Figure 4.4 (b) V_T is estimated to be 9 V in the linear regime and 12 V in saturation, closer to the V_T values of R-DNTT than S-DNTT. The mobilities were extracted from the slope of the respective plots, and were 0.19 cm^2/Vs in the linear regime and 0.36 cm^2/Vs in saturation.

From the semi-log transfer plot, Figure 4.4 (c), we see that as with the R-DNTT sample, 20 V is not positive enough to switch off the transistor, so that the I_{ON}/I_{OFF} ratios can only be estimated to be > 100 in the linear regime, and > 1000 in the

saturation regime. The subthreshold slope is steeper in both regimes than for the other two samples, in the linear regime the subthreshold slope was 13.8 V per decade, and in the saturation regime it was 7.5 V per decade.

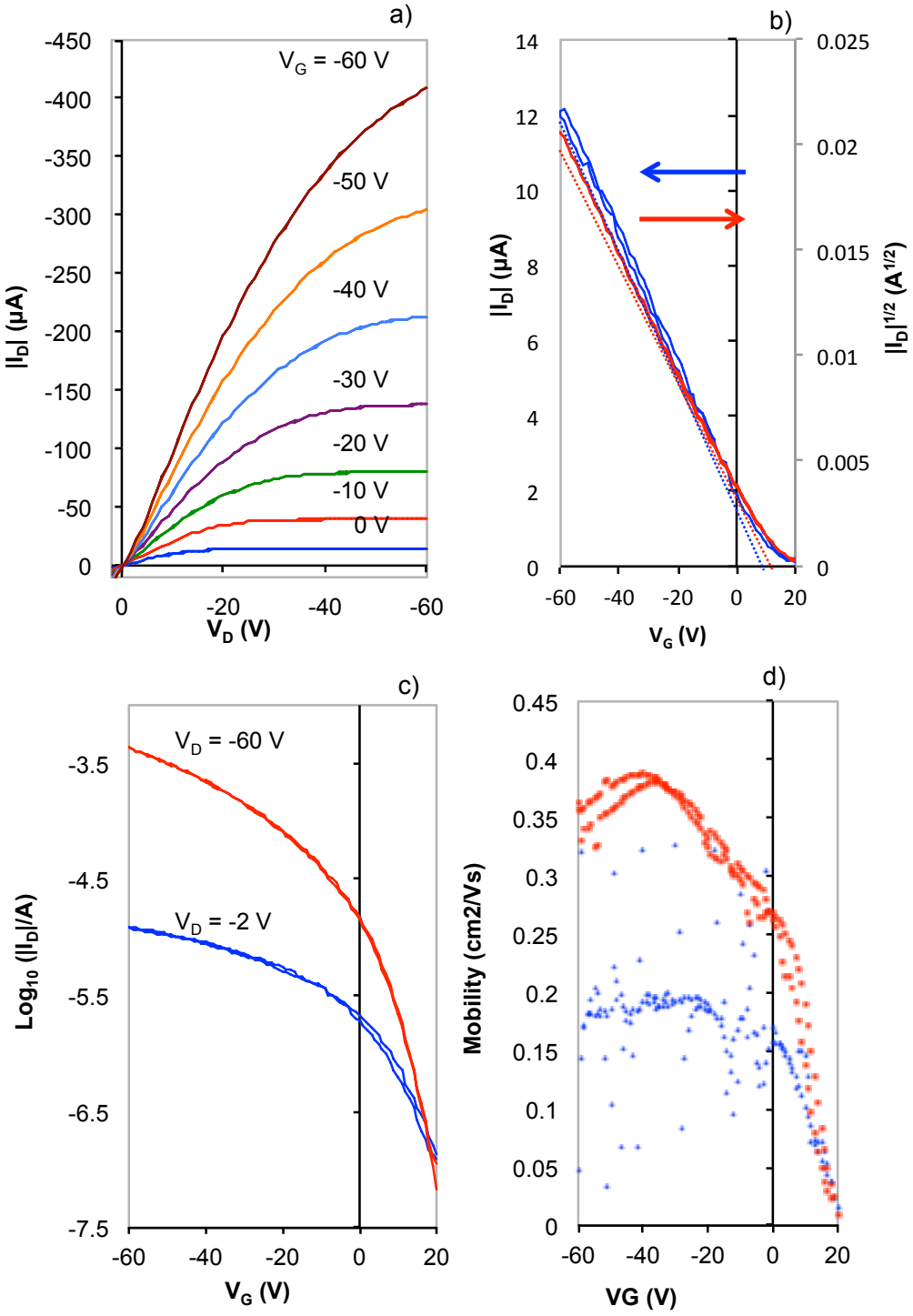

Figure 4.4 Results obtained from an SR-DNTT transistor. W = 4 mm, L = 100 µm, C_I = 1.151 x 10^{-8} F/cm^2. a) Output characteristics plotted from a V_G of 0V to -60 V in -10 V increments. b) plots of I_D in the linear regime in blue (V_D = -2 V) and $I_D^{1/2}$ in the saturation regime in red (V_D = -60 V). c) Semilog plots of I_D vs V_G in the linear regime (blue) and saturation regime (red). The corresponding mobility plot for both regimes is inset.

The gate voltage dependent mobility is shown in the inset of Figure 4.4 (c). Maximum linear mobility is calculated to be 0.20 cm^2/Vs (ignoring points due to noise) and in the saturation regime the maximum mobility is determined to be 0.38 cm^2/Vs. Saturation mobility increases from ~ 0 cm^2/Vs at V_G = 20 V up to 0.38 cm^2/Vs at V_G = -37 V, decreasing for more negative voltages, and is very similar to the corresponding plot for R-DNTT (inset of Figure 4.2 (c)).

Figure 4.5 shows for each sample of DNTT a histogram of the number of devices within a range of maximum saturation mobility in increments of $\Delta\mu$ = 0.09 cm^2/Vs.

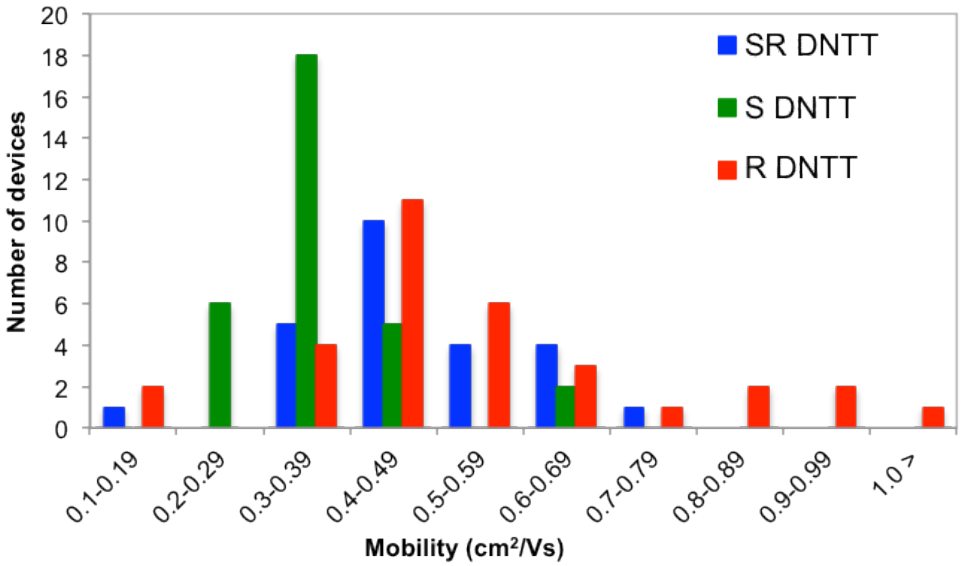

Figure 4.5 A histogram of the maximum saturation mobilities of all the transistors fabricated using the R-DNTT, S-DNTT and SR-DNTT samples.

There is a large spread in the mobility of transistors fabricated using R-DNTT and SR-DNTT. There is much less of a spread in the mobility of transistors fabricated using the S-DNTT sample. The histogram also shows that devices fabricated using the R-DNTT are capable of the highest mobilities.

Table 4.1 shows the number of working devices for each DNTT sample, the average maximum saturation mobility and median saturation mobility. From this it is seen that on average the R-DNTT has the highest mobility, followed by the RS-DNTT with the S-DNTT showing the lowest average mobility. However, the spread in saturation mobility values is lowest for the S-DNTT, showing mobilities between 0.2 cm^2/Vs and 0.69 cm^2/Vs, with the majority of the transistors having a mobility in the range 0.30-0.39 cm^2/Vs. The mobility spread for R-DNTT is from

0.1 cm^2/Vs to >1.0 cm^2/Vs. The spread in mobilities is also emphasised by the difference in the average and median mobilities.

Table 4.1 A table summarising the number of transistors characterised for each sample, together with the average saturation mobility and median saturation mobility.

	Sublimed	**Sublimed Recrystallized**	**Recrystallized**
Number of devices	31	25	32
Average mobility (cm^2/Vs)	0.36	0.47	0.54
Median Mobility (cm^2/Vs)	0.34	0.43	0.39
Standard Deviation	0.09	0.13	0.20
Average V_T (V)	-2	10	9.65
Median V_T (V)	-1.5	10	10
Standard Deviation	1.78	2.24	1.86

4.3 Discussion

It could be assumed that a combination of both the sublimation and recrystallization process would yield the best sample, but this appears to not be the case. The R-DNTT yields the transistors with the highest mobility, and the S-DNTT yields the transistors with the most consistent mobility with less spread in its mobility range. The SR-DNTT yields results lying between the other two samples. However, it is immediately evident that there are a number of similarities in the characteristics of the transistors fabricated using the R-DNTT and SR-DNTT samples. Although all three samples displayed a diode-like contact resistance at low V_D in the output characteristics, both the R-DNTT and SR-DNTT were conductive at $V_G = 0$ V. This was reflected in the positive V_T of both samples. For the S-DNTT sample V_T was close to 0 V in both linear and saturation regimes. Both the R-DNTT and SR-DNTT had a saturation mobility that initially increased with V_G, but then decreased at a V_G more negative than ~ -37 V. The V_G dependent saturation mobility of the S-DNTT transistor continued to increase with increasing V_G, showing no sign of decreasing at higher voltages. This would suggest that the recrystallization process has a large influence on how the material performs when used as the semiconductor. It also means that the choice is truly between S-DNTT and R-DNTT.

Average maximum mobility observed in saturation for the R-DNTT and the SR-DNTT are 0.54 and 0.47 cm^2/Vs respectively. The spread in values for both are large, ranging from 0.18 cm^2/Vs to 1.15 cm^2/Vs for R DNTT. In contrast 58 % of S DNTT transistors have a mobility value within the range of 0.30 – 0.39 cm^2/Vs. The average mobility is lower than both SR DNTT and R DNTT, but the values are spread over a smaller range. In all cases though, the values are significantly lower than the 3 cm^2/Vs quoted in the first report on DNTT OTFTs on SAM modified SiO_2 [1].

From Figure 4.1 SR-DNTT and R-DNTT samples have similar topography with larger crystals embedded in a background of smaller grains. In S-DNTT the grain size is similar to that of the background grains in SR-DNTT and R-DNTT but are more uniform in size, are flatter and with narrower intergrain spacing. The SR-DNTT and R-DNTT also have a very similar RMS surface roughness, again indicating that there is a similarity between the two samples when compared to the S-DNTT.

Mobility has previously been shown by Horowitz and Hajlaoui [2] to be grain size dependent in organic semiconductors. Mobility was shown to increase with an increasing grain size. This was explained by high conductivity within the crystal grains and low conductivity in the grain boundary area. According to Ding *et al*. [3] the correlation between large crystal size and high mobility alone is misleading, mobility is also dependent on the underlying dielectric layer for similar sized crystal grains. Although pentacene had a similar grain size on polystyrene (PS), poly (vinyl stearate) (PVS) and poly (methyl methacrylate) (PMMA), the mobility was similar on PS and PVS ~ 0.2 cm^2/Vs, but much lower for pentacene on PMMA ~ 0.05 cm^2/Vs. Variation in mobility due to differences in the dielectric layer was mitigated in the present work by fabricating all transistors on substrates diced from the same wafer, so in this case the crystal grain size is expected to be important.

Therefore, mobility is expected to be higher in the SR-DNTT and R-DNTT samples due to the larger average grain size, and therefore reduced number of grain boundaries. However, the grain sizes of the SR-DNTT and R-DNTT samples were not uniform, and the large crystals occurred randomly. This is reflected in the transistor results. SR-DNTT and R-DNTT that contain the large crystals have the

higher average mobility but with a grater spread in values. In S-DNTT average mobility and spread in values are lower which is consistent with a more uniform grain size.

4.4 Summary

OTFTs were fabricated on HMDS treated SiO_2 using DNTT purified in three different ways. For each set of materials, output and transfer characteristics were obtained in the dark under ambient conditions and values for hole mobility extracted in both the linear and saturation regimes. In all cases the characteristics were free of hysteresis but the mobility in saturation was significantly higher than in the linear regime.

The recrystallized DNTT was shown to have the highest average mobility, 0.54 cm^2/Vs compared to 0.47 and 0.36 cm^2/Vs for SR and S DNTT respectively. It also had the largest spread in mobility values 0.18 – 1.06 cm^2/Vs. AFM images showed the presence of large flat crystals in the R and SR DNTT which were not present in the S DNTT. The presence of these larger crystals was believed to be the cause of the increased mobility and large spread in mobility values.

The purpose of this investigation was to determine whether recrystallization could be used as the method of purification replacing the sublimation step without having an adverse impact on transistor performance. What has been shown here is that the average mobility for R-DNTT transistors was higher than that for S-DNTT transistors with the potential for achieving much higher values as evidenced by the histograms in Figure 4.5. The only disadvantage of using the R-DNTT sample is the spread in mobilities when compared to the S-DNTT sample. With these findings in mind, and the fact the recrystallization gave a much higher % yield of DNTT in a shorter time, it was decided to proceed using the R-DNTT for future device fabrication.

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Chapter 5

Polystyrene/DNTT Devices

5.1 Introduction

It is well known that transistor configuration has a direct impact on performance. In particular when source/drain electrodes are coplanar with the channel, Figures 2.8 (a) and (d), charge injection from the edge of the source can be inefficient leading to a high contact resistance and low effective mobility due to a reduced contact injection area [1, 2, 3]. In this chapter, therefore, using recrystallized DNTT as the semiconductor, the performance of top-gate bottom-contact (TGBC) and bottom-gate top-contact (BGTC) devices is evaluated, avoiding the coplanar configurations due to the associated high contact resistance.

For this study spin-coated polystyrene (PS) was used as the gate dielectric for several reasons.

(a) It is a widely used dielectric showing good performance with a range of organic semiconductors.
(b) It was readily available and avoided delays while waiting for TPGDA samples from Oxford.
(c) It can be used to fabricate both top-gate and bottom-gate OTFTs with DNTT as DNTT is not soluble in toluene the solvent used for spin-coating PS.

By concentrating on TGBC and BGTC the effect of differences in interface morphology and possibly chemistry, can be determined. In TGBC devices interface morphology will be determined by the DNTT film while in BGTC devices by the PS film.

5.2 The Semiconductor/Dielectric Interface

Figure 5.1 shows the surface topography of (a) DNTT and (b) PS on a PEN substrate. The surface of the DNTT (Figure 5.1 (a)) becomes the interface in a top gate device, and the surface of the PS (Figure 5.1 (b)) becomes the interface in a bottom gate device.

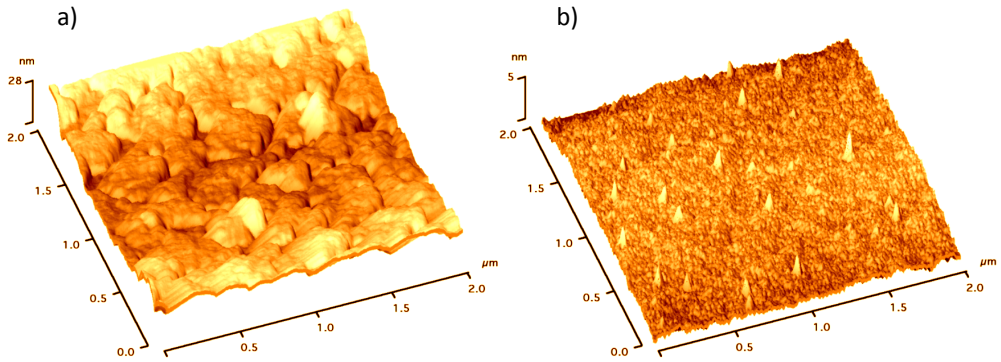

Figure 5.1 (a) A 2 x 2 μm AFM image of the DNTT surface on PEN substrate. (b) A 2 x 2 μm AFM image showing the surface of PS on PEN substrate.

The surface of the DNTT has an RMS surface roughness of 6.4 nm, over a 4 μm^2 area. There is a difference of 12 nm between the peaks and troughs of the crystal grains. In comparison RMS surface roughness of the PS is 0.69 nm over a 4 μm^2 area, ten times lower than the DNTT surface. There are some spikes of material protruding from the surface with a height of ~ 2 nm, but these cover very little of the overall surface area and are the only surface features visible.

5.3 Top-Gate-Bottom-Contact Polystyrene-DNTT Transistors

5.3.1 Results

Figure 5.2 shows the results obtained from a TGBC PS-DNTT transistor in which W = 15.9 mm and L = 30 μm. Output characteristics are given in Figure 5.2 (a). Transfer characteristics are plotted in (b) as I_D vs V_G in the linear regime (V_D = -2 V) and as $I_D^{1/2}$ vs V_G in the saturation regime (V_D = -30 V). Transfer characteristics are plotted in semi-log form in (c) and gate leakage current in both regimes is given by the dashed curves in the corresponding colour in Figure 5.2 (c). The gate dependent mobility in the linear regime and saturation regime is plotted in (d).

The output current quickly saturates for all gate voltages, although I_D continues to rise slowly in the saturation region.

There is a significant clockwise hysteresis in the transfer characteristics, the device showing poor stability in air (Figure 5.2 (b)).

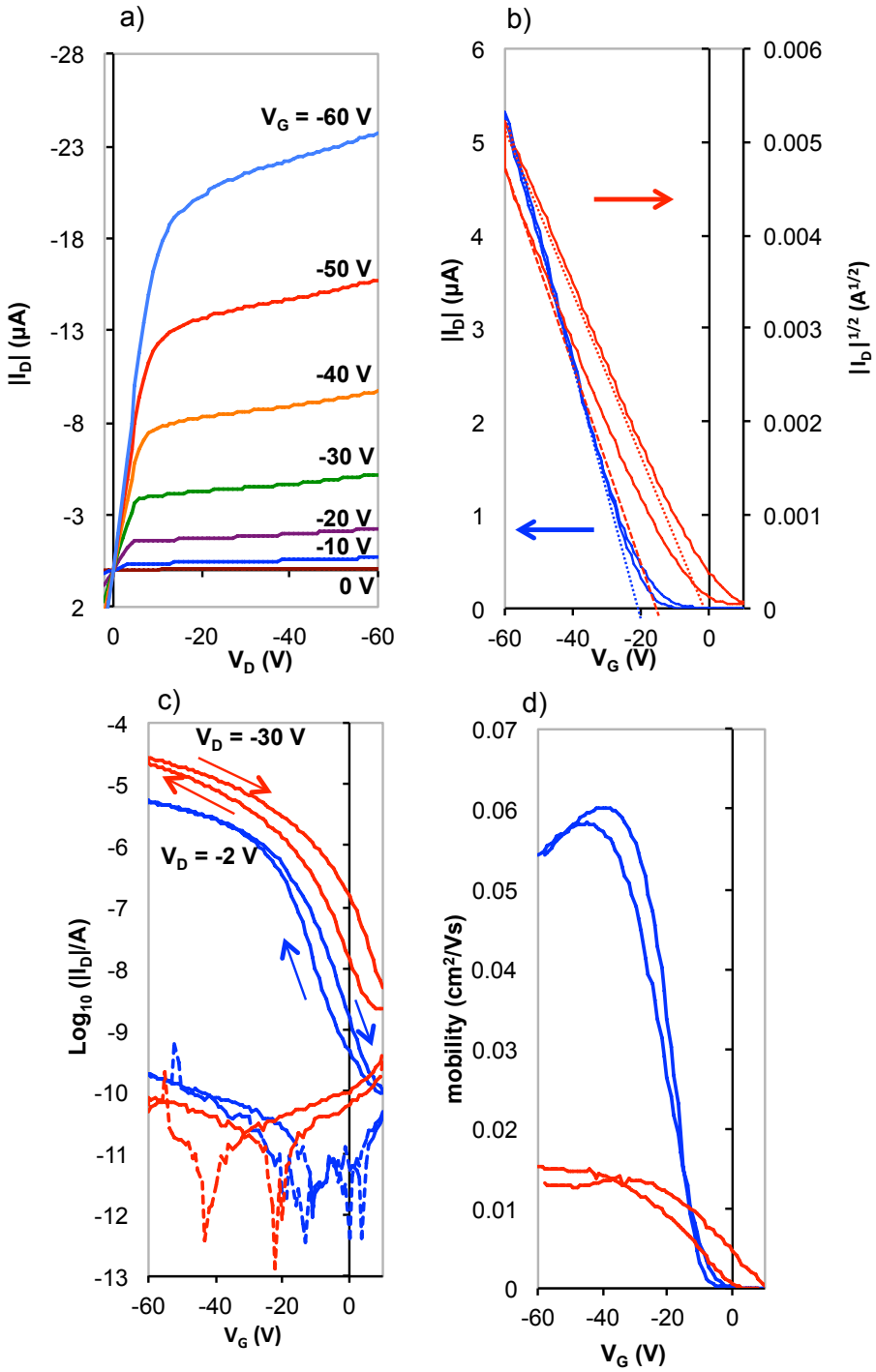

Figure 5.2 Results obtained from a TGBC DNTT-PS transistor. (a) Output characteristics for V_G in the range 0 to -60 V in -10 V increments. (b) Transfer plots for I_D in the linear regime and $I_D^{1/2}$ vs V_G in the saturation regime. (c) Transfer plots in the linear regime, V_D = -2 V (blue), and the corresponding I_G vs V_G plot (dashed blue line), in the saturation regime V_D = -30 V (red) and its corresponding I_G vs V_G plot (dashed red line). (d) μ_{lin} (blue) and μ_{sat} (red) extracted from the local slopes of the transfer plots using equations 2.10 and 2.11.

A V_T of -11 V is estimated for the saturation regime in the forward sweep by extrapolating the $I_D^{0.5}$ vs V_G plot, and is 0 V on the return sweep. Similarly for the linear regime the I_D plot in Figure 5.1 (b) is extrapolated to a V_T of -20 V. This shows that the V_T is shifting positively with each sweep in the saturation regime but is negligible in the linear regime. The linear mobility extracted from the slope of the corresponding plot in Figure 5.2 (b) is 0.058 cm^2/Vs, the saturation mobility extracted using the same method is 0.022 cm^2/Vs for the initial sweep and 0.016 cm^2/Vs for the return sweep.

From the semi-log plots in Figure 5.2 (c) it is possible to estimate the V_{ON} to be $\geq$ 10 V in the linear regime, and 5 V in the initial sweep in the saturation regime. The I_{ON}/I_{OFF} ratio in the linear regime is 10^4 and 10^3 in saturation. In the linear regime the subthreshold slope is 6.6 V per decade in the initial sweep and 7.0 V on the return. In the saturation regime it is 7.9 V per decade on the initial sweep and is 6.6 V per decade on the return sweep. The gate leakage current I_G is also shown in Figure 5.2 (c) for both regimes as dashed line plots and is found to be <120 pA over most of the V_G range.

Plots of the gate voltage dependent μ_{lin} and μ_{sat} extracted using equations 2.10 and 2.11 respectively are plotted as a function of V_G in Figure 5.1 (d). μ_{lin} rises to a significantly higher value than μ_{lsat}, reaching a maximum of 0.05 cm^2/Vs vs 0.016 cm^2/Vs, again indicating that there is a limitation on the saturation current.

5.4 Top Gate Polystyrene DNTT inverter

As described in section 3.5.6, Mask Set 2 (Figure 3.8) incorporated designs for two identical inverters. Figure 5.3 shows an expanded view of the inverter design. Inverters were fabricated to this design based on the top-gate PS-DNTT transistors process in which the source drain electrodes were patterned photolithographically.

In this case for D09 W/L = 1.8 mm/30 μm while for D10 W/L = 15.9 mm/30 μm. After characterising the transistors independently, transistor D09 was converted to an enhancement mode load by connecting pads G_2 and D_2 using silver paste after which the inverter performance was evaluated.

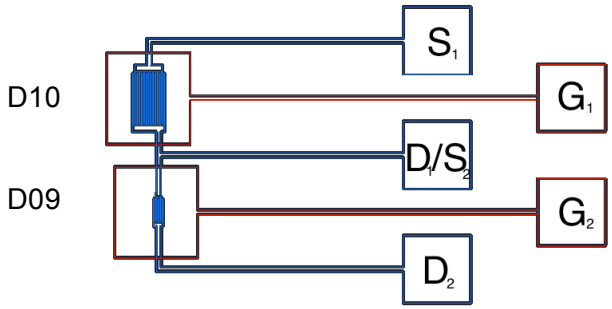

Figure 5.3 Expanded view of the inverter design in Mask Set 2 (Figure 3.8). By connecting G_2 and D_2, transistor PS-D09 becomes an enhancement mode load for the inverter.

5.4.1 Results

The semi-log transfer characteristics of the individual transistors are shown in Figure 5.4 (b). It is seen that the off currents are dependent on the applied drain voltage V_D. When V_D = -2V, I_{OFF} is probably < 100 pA but for V_D = -30 V is > 1 nA, suggesting the presence of a parasitic source-drain current. As a consequence the on/off ratio for PST-D09 was 10^3 and PSR-D10 was 10^4. The maximum values extracted from μ_{sat} in the two devices was 0.012 cm^2/Vs.

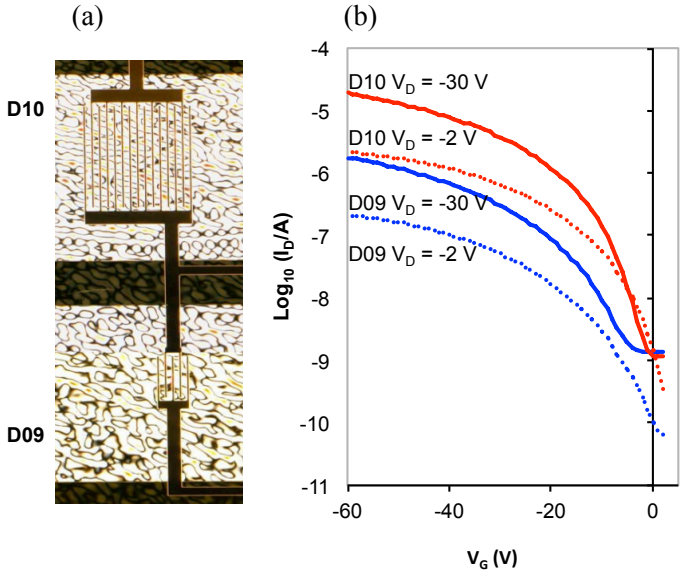

Figure 5.4 (a) Optical microscope image of transistors PST_D10 and PST_D09 obtained by illuminating through the transparent PEN substrate. The rough pattern is from residual gel pack adhesive used to hold the PEN substrate on a glass slide while processing. (b) Transfer characteristics for devices PST-D09 (blue curves) and PST-D10 (red curves) obtained in the linear regime (V_D = -2V, dashed curves) and in saturation (V_D = -60V, full curves).

After characterising the individual transistors they were connected together to form an enhancement load inverter. The voltage transfer characteristics of the inverter and its response to a square wave input signal are shown in Figure 5.5.

For the inverter transfer measurement V_{DD} was set to -60 V initially, then -40 V and finally -20 V. For each V_{DD}, V_G was swept from +30 V to -30 V. The gain ($=\frac{\Delta V_{OUT}}{\Delta V_{IN}}$) was calculated at each value of V_G and is also given in Figure 5.4 (a).

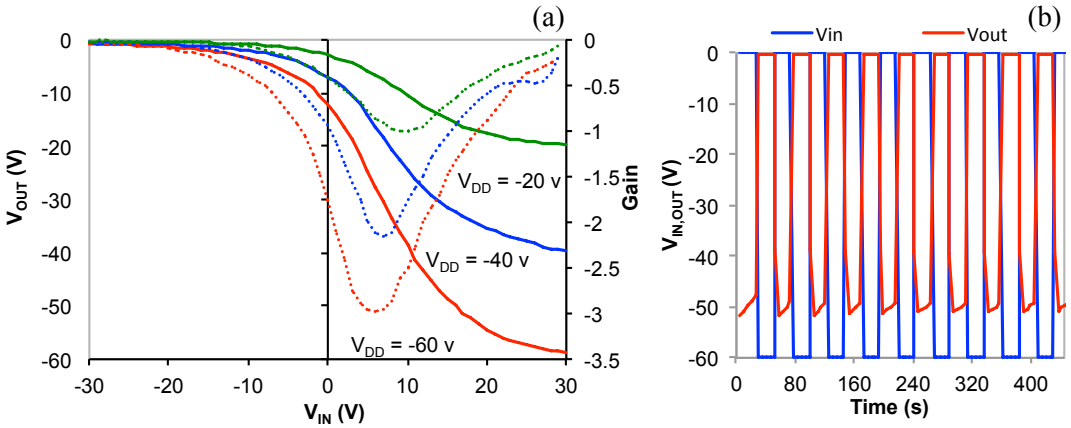

Figure 5.5 (a) The dynamic square wave response of the PS inverter at V_{DD} = -60 V. (b) The voltage transfer plots at V_{DD} voltages = -60 V (red), -40 V (blue) and -20 V (green). The corresponding gain plots are plotted with the same colours in dashed lines.

Of interest is the maximum gain which is 3 for V_{DD} = -60 V, 2.1 for V_{DD} = -40, and for V_{DD} = -20 V it is still greater than 1. This would make the inverter suitable for a ring oscillator circuit with a rail voltage of V_{DD} = -20 V. Based on Figure 5.4 (b) it would be expected that the transition point, V_{TR}, where V_{IN} = V_{OUT} for the inverter would be negative. For an inverter switching from 0 V to the rail voltage, as is conventional for a p-type semiconductor, the noise margins are very poor. Again this is evident from the position of the maximum gain peaks and V_{TR} that are at positive voltages.

The inverter response to a low frequency square wave was recorded and is given in Figure 5.5 (b). In this example, V_{DD} = -60 V and the input signal switched between 0 V and -60 V. The output signal clearly demonstrates inversion, switching from 0 V to around -50 V in antiphase to the input. However, during the period when the input is low at 0 V the output voltage drifts downwards when high by ~ 5 V.

5.5 Bottom-Gate-Top-Contact Polystyrene-DNTT Transistors

All steps in the fabrication of bottom-gate-top-contact PS-DNTT devices were identical to those used for the top-gate device except for the patterning of the gold source/drain electrodes. Defining these electrodes photolithographically would have exposed the DNTT layer to harsh chemical treatment during etching and exposure to UV light which would have been detrimental to its performance [4]. Therefore, the opportunity was taken to design a new mask set (Mask Set 3, Figure 3.9), for assessing transistor yield. The transistor yield was determined by only counting working transistors. For this project a working transistor was defined as one with an above average mobility, or no less than 90% of the average, and a gate current (I_G) of less than 10% of the maximum linear output current (I_{Dlin}).

5.5.1 Transistor Characteristics

90 transistors were fabricated using Mask Set 3, with a range of aspect ratios, to evaluate device yield. After fabrication, measurements were conducted under ambient dark conditions. For bottom gate PS dielectric OTFTs all 90 transistors on a single 50 mm x 50 mm substrate area were characterised. Out of the 90 measured transistors two were short circuit (to the gate) and 27 had high gate leakage, giving a yield of ~66%.

Hole mobility in saturation ranged from 0.74 cm^2/Vs up to 1.14 cm^2/Vs, with an average of 0.97 cm^2/Vs for all working OTFT devices on the substrate. V_T ranged from -5 V to -25 V, the average being -11 V.

Figure 5.6 (a) shows an example of the transfer characteristics of a group of nine adjacent common gate devices (PS_C10 – PS_C18) that have the same transistor dimensions. In one set of plots the devices were in the linear regime (V_D = -2V) and the other set the devices were in the saturation regime (V_D = -60V). The plots generally follow the same dependence on V_G, particularly at high gate voltages.

Many of the transistors have a high off current corresponding to the high gate leakage currents, I_G, of the same devices shown in Figure 5.6 (b). The gate leakage current, I_G, is generally ≤ 20 pA. A number of the other OTFTs (results not shown) displayed unacceptably high I_G, in excess of 10% of the maximum I_D. The transistors show

good uniformity in the output current in both regimes with negligible hysteresis. The On/Off ratios ranged from 10^1 to 10^6, 36 of the transistors having the I_{ON}/I_{OFF} ratio of 10^6. The low I_{ON}/I_{OFF} ratios were due to high off currents and also resulted in a shallower sub-threshold slope.

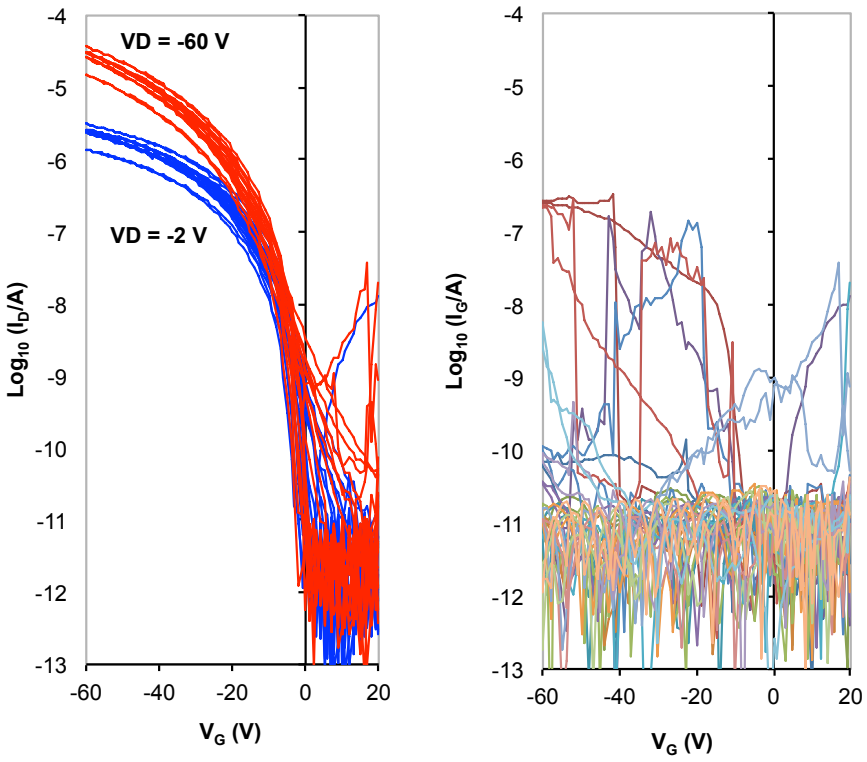

Figure 5.6 (a) Transfer plots in the linear (V_D = -2 V) and saturation (V_D = -60 V) regimes for devices C10- C18. (b) The gate leakage currents, I_G, for the same transistors.

Figure 5.7 shows an example of the output characteristics (a) and transfer ((b) and (c)) of a good PS dielectric OTFT PS_C08, W = 2mm, L = 100 μm (not featured in Figure 5.6). For this particular device the linear mobility is marginally higher than in saturation mobility. These results were typical of a working bottom gate OTFT on the PS dielectric.

All the output plots in Figure 5.7 (a) show negligible hysteresis and good saturation. High currents are observed for V_G more negative than -20 V (the V_T of the transistor), with little evidence for the presence of a contact resistance.

The transfer characteristics are shown in Figure 5.7 (b). The V_T for both regimes are taken from the extrapolation of the linear section of both plots. In the linear regime the V_T = -20 V, and in the saturation regime is -16 V. The slope of the plots is

determined using equations 2.9 and 2.10 to extract the mobility. μ_{lin} is calculated to be 0.98 cm^2/Vs and μ_{sat} is calculated to be 0.96 cm^2/Vs.

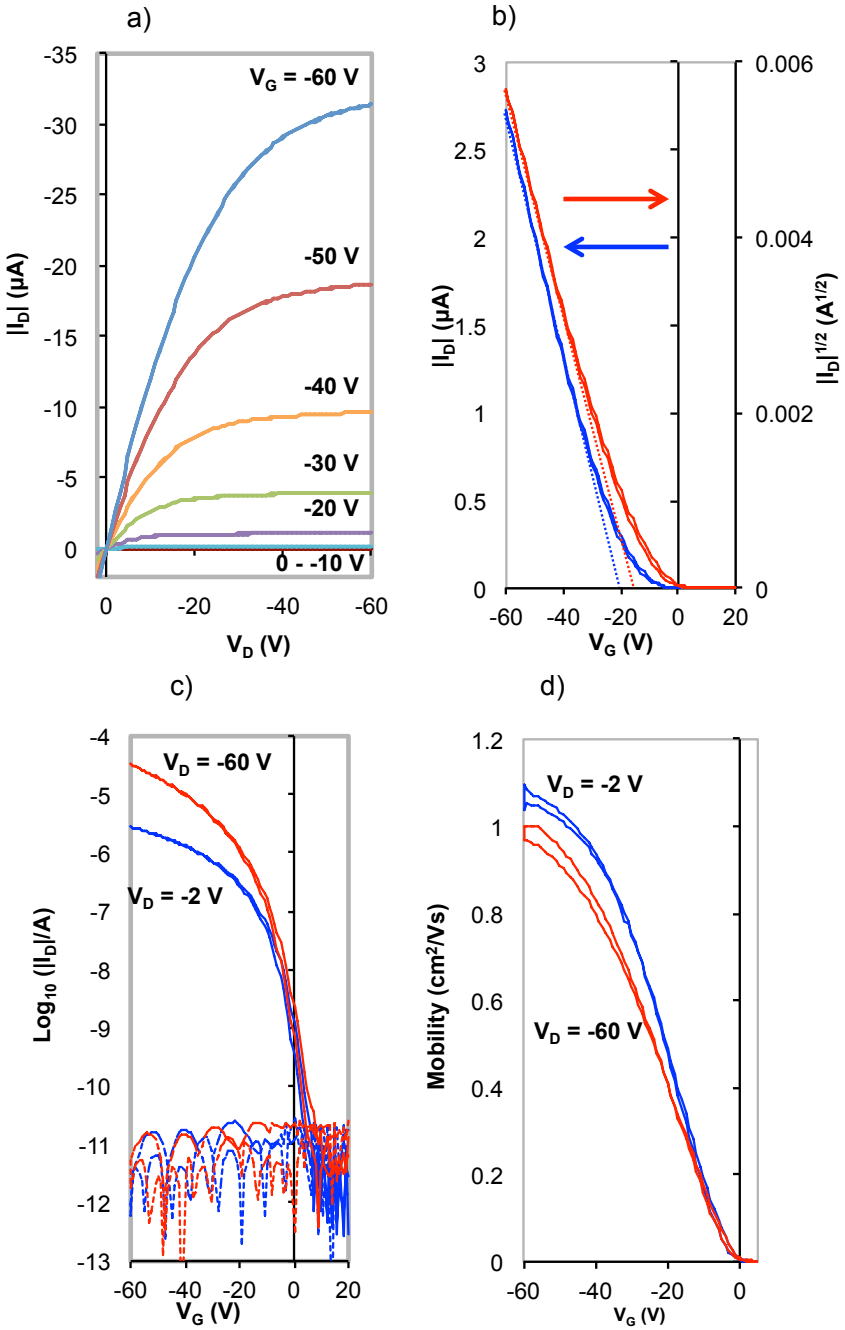

Figure 5.7 Results obtained from a BGTC DNTT-PS transistor PS_C08. (a) Output characteristics. (b) Transfer characteristics of the linear plotted as I_D vs V_G (V_D = -2 V, blue), and saturation plotted as $I_D^{1/2}$ vs V_G (V_D = -60 V, red) regimes. (c) The semilog plots of the saturation and linear plots along with the corresponding gate leakage currents plotted as dashed lines. (d) Linear (μ_{lin} blue) and saturation (μ_{sat} red) mobilities plotted as a function of V_G.

It can be seen from the semilog plot in Figure 5.7 (c) that hysteresis is low, and there is a good degree of overlap of the linear and saturation plots in the sub-threshold region. The subthreshold slope in the linear regime is 3.65 V per decade and in the saturation regime is 4.00 V per decade. The gate leakage current is shown in corresponding colours in dashed plots and are low, typically <50 pA, in both cases.

The gate voltage dependent mobility calculated using equations 2.11 and 2.12 is shown vs V_G in Figure 5.7 (d). The maximum values were 1.00 cm^2/Vs for saturation and 1.05 cm^2/Vs for linear. The two plots show similar dependence against V_G, and are similar to the mobilities extracted using equations 2.9 and 2.10.

The same method was used to calculate the maximum linear and saturation mobilities of each transistor on the substrate. The values are plotted against position on the substrate in Figure 5.8.

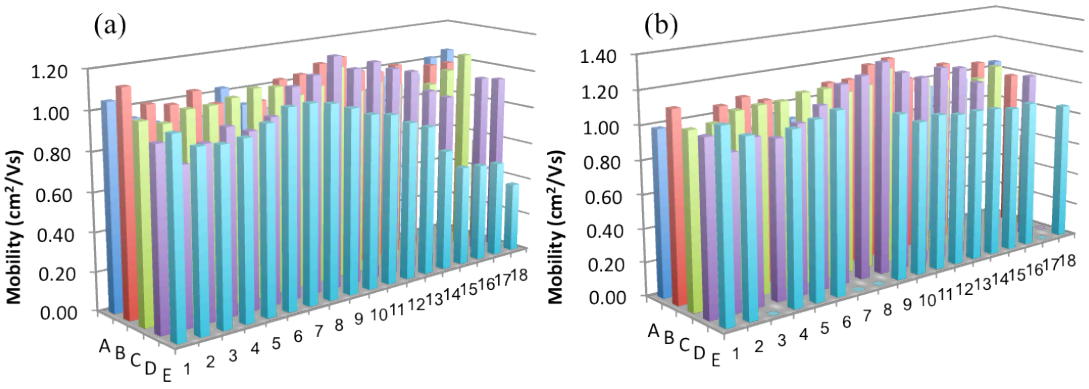

Figure 5.8 3-D plots of the maximum mobilities taken from the V_G dependent local slope plots (a) in the saturation regime and (b) in the linear regime. Results are arranged by their location on the substrate.

There appears to be a trend in devices E10-18, however this was isolated to a single group, and the pattern is not repeated elsewhere on the substrate. This could be due to a local variation in capacitance on that area of the substrate. There are no other obvious group trends observed in the 3-D plot of the PS-DNTT transistor mobilities in Figure 5.8. The maximum saturation mobilities and the maximum linear regime mobilities are closely matched with an average ~ 0.97 cm^2/Vs. Where there are spaces reveals where either the gate current, I_G, of the transistor was too high or where the transistors were short-circuit.

Table 5.1 summarises the average mobility for the ten sets of 9 devices on substrate PS1. There is one outlying group of devices, E10-19, where the saturation mobility falls far below the average. For all of the other groups the average mobility is close to 1 cm^2/Vs. This suggests that the mobility is independent of channel length and width, and, therefore, the aspect ratio.

Table 5.1 Average maximum mobilities for the 10 different groups of transistors on substrate PS1.

Row		A	B	C	D	E
L (μm)		50	75	100	150	200
W = 2 mm	01-09 Linear	0.93	1.12	1.10	1.07	1.06
	01-09 Saturation	0.94	1.05	1.02	0.98	0.96
W/L = 20	10-18 Linear	0.98	1.12	1.02	1.14	0.92
	10-18 Saturation	0.96	1.02	0.95	1.02	0.67

5.6 Discussion

Working bottom gate devices on PS show negligible hysteresis and good device stability. The average hole mobilities in saturation are close to 1 cm^2/Vs, and are higher than the mobility quoted in [5] for pentacene OTFTs on PS modified HfO_2. The average mobility of 1 cm^2/Vs is comparable to that of α–silicon.[6, 7, 8]. In comparison the results in Figure 5.2 shows that top gate PS dielectric devices have low mobility and poor stability. The surface of the deposited DNTT is rougher than the surface of PS. In the case of top-gate devices where the DNTT is deposited before the dielectric the interface between DNTT and PS was rougher than for a bottom gate device where the PS layer is deposited first. Charge transport is greatest within a few nanometres of the interface; if the interface is rough this produces physical barriers to charge transport, and reduces the mobility in top gate devices [9, 10, 11]. In this case, because there is a difference of 28 nm between the peaks and troughs of the DNTT it is easy to see why charge transport would be hindered, and how charge carriers can be scattered. In contrast the PS surface is very flat with few features that can provide obstacles to charge transport.

In addition the rougher DNTT surface in the top gate devices will probably have a higher density of charge traps at the interface due to crystal defects. Therefore, when the transistor is first switched on and V_G is swept from 10 V to -60 V traps will gradually fill as the current flows shifting V_T towards more +ve gate voltages. When the sweep is reversed from -60 V to 10 V, and no de-trapping occurs, the shift in V_T gives rise to hysteresis. The off current is increased and the sub-threshold region becomes shallower during the measurement. This shows that charge trapping at the interface is responsible for the V_T shift.

From the output characteristics of the BGTC transistor (Figure 5.2) it can be seen that there is some form of limitation on charge injection as each plots saturates with a very short shoulder region. This suggests that current crowding is occurring as V_G increases, and would explain the large difference between the linear and saturation mobilities observed in Figure 5.2 (d). This could be as a result of the rough interface, but could also be due the order the semiconductor and contact layers are deposited. The orientation of DNTT crystals deposited onto the PS dielectric will not be the same as DNTT crystals that are deposited directly onto gold. It may be that charge injection into the semiconductor is limited in the TGBC configuration due to a higher energy barrier as a result of the different orientation of the DNTT crystals. Although this energy barrier could be reduced by the use of a SAM such as pentafluorobenzene thiol (PFBT) [12] the roughness of the interface is prohibitive to making high mobility transistors.

The yield of 66% is lower than the 75% yield obtained by Hambsch *et al*.[13] for all printed transistors. A disadvantage of spin coating dielectric films is the formation of pinholes as solvent evaporates away and the film dries. The pinholes provide a path for the gate leakage current, I_G, potentially causing devices to become short circuited if the pinhole is present between the SD and G contacts. In good devices though the gate leakage current was low as in Figure 5.7 (c), resulting in high on/off ratio $>10^6$.

The inverter was shown to invert the input signal of 0 to -60 V, into an output from ~-59 V to ~-0.2 V, working well despite the low mobility of the constituent transistors. Unfortunately, due to the shifting V_T, the voltage transfer was asymmetric, having a very large high noise margin, and no low noise margin. The V_{OH} of the inverter during the square wave response measurement was shown to drift, the output voltage dropping as the input voltage was held low. This suggests that the V_T is shifting in the

load transistor (as the driver is off) negatively as the device is stressed, resulting in the observed drop in voltage. The device then recovers by the next switch, and the effect observed when stressing the device is short lived.

No inverters were fabricated in the bottom-gate configuration due to the low device yield. However, the high mobility and good transistor performance, particularly in comparison to the top-gate transistor, suggests that an inverter fabricated in such a configuration should work well.

5.7 Summary

18 TGBC transistors were fabricated using spin-coated PS dielectric on DNTT semiconductor, using mask set 2. Saturation mobility was calculated to be 0.016 cm^2/Vs in one of the few working devices, and was almost two orders of magnitude lower than for the BGTC transistors. This was ascribed to the rough semiconductor/dielectric interface of DNTT and PS in the top gate configuration.

An inverter, fabricated using TGBC OTFTs, was characterised and the inverter performance (transfer and gain) evaluated. The maximum gain of the inverter was found exceed 1 for all rail voltages higher than -20 V.

90 transistors with different aspect ratios were fabricated in a BGTC configuration using mask set 3 and their performance evaluated by measuring output and transfer characteristics. Transistor yield was found to be 66% with 27 devices having unacceptably high gate leakage current and two in which the gate was short-circuited. For the 61 working transistors the average maximum linear mobility was found to be 1.01 cm^2/Vs and saturation mobility was found to be 0.97 cm^2/Vs.

As a result of the study reported in this chapter it is clear that the BGTC design is far superior to the TGBC design, so long as the gate dielectric, in this case PS, has a far smoother surface than the DNTT. Owing to its method of deposition, the surface of TPGDA is very smooth, with an rms roughness of 5 Å [14]. When combined with other factors arising from a top gate design, i.e. possible damage to the DNTT during deposition and curing of TPGDA, the choice to fabricate devices exclusively in the BGTC configuration was easy to make.

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Chapter 6

TPGDA/DNTT Devices

6.1 Introduction

This chapter begins to address the main objective of the work – the characterisation of DNTT OTFTs fabricated entirely using vacuum evaporation methods compatible with R2R production. They key to the approach is the deposition and subsequent plasma polymerisation of tri(propylene glycol) diacrylate (TPGDA) as the gate dielectric (see section 3.2.3 for details of the process). The intention here was to fabricate a large number of transistors to ascertain the transistor yield and mobility. Once the yield and mobility are established it will be possible to optimise the processes to improve both quantities. Once the yield and mobility are sufficient it would be possible to begin fabricating more complex devices.

Based on the results of the previous two chapters the TFTs were fabricated using the R-DNTT sample, as it was shown to give the highest mobility. The bottom-gate-top-contact configuration was adopted as it avoids the rough interface associated with the DNTT top surface and, importantly, damage to the DNTT during the polymerisation of the TPGDA. Also there appeared to be no contact resistance issues in the characteristics of the BGTC configuration transistor (Figure 5.7), and was shown in the previous chapter to yield a higher mobility than the TGBC configuration.

Due to the TPGDA deposition process being solvent-less there is no requirement for an annealing or drying time. The absence of solvent should also significantly reduce the presence of pinholes in the dielectric that form when a solvent is evaporating. Eliminating pinholes was expected to increase transistor yield making it possible to progress with fabricating integrated multiple transistor circuits.

In this chapter, we initially characterise an array of 90 TPGDA DNTT transistors fabricated with Mask Set 3 to evaluate transistor performance. An array of transistors fabricated using Mask Set 1 was also tested once a week over a period of four weeks. The effect of atmospherically-induced performance degradation is investigated by characterising transistors initially in ambient conditions and then under vacuum. We attempt to replicate the improvement seen in device stability under vacuum by

applying an encapsulating layer as a final fabrication step. The characteristics of the encapsulated transistor are then compared to those of an un-encapsulated transistor. We also characterise the static and dynamic behaviour of an inverter fabricated from TPGDA DNTT transistors in air and then under vacuum.

6.2 TPGDA DNTT Transistors

6.2.1 Experimental Results

Devices were fabricated as described in section 3.5.4 and results obtained in ambient dark conditions using the setup as described in section 3.7. A 90-transistor array was fabricated using Mask Set 3. The only devices not characterised were A01-A09 that did not function due to a scratch in the SD contacts in the channel region of the devices. Consequently only 81 transistors on the 50 mm x 50 mm substrate were characterised. For the linear transfer characteristics V_D was held at -2 V and at -60 V for saturation as V_G was swept from 10 V to -60 V and back to 10 V.

Figure 6.1 shows an example of the linear and saturation transfer characteristics of a group of nine adjacent common gate devices (E10 – E18) that have the same transistor dimensions (L = 200 μm and W = 4 mm). There is a single device within this group of 9 where the gate current, I_G, has affected the measurement within the subthreshold slope (orange plot Figure 6.1). Apart from this single device, I_G remains low within this set i.e. < -1 nA, and this is true for more than 95% of the working devices on this substrate.

These observations are typical of the nine characterised groups of 9 transistors on substrate A1. The initial sweep from 10 V to -60 V shows a significant difference between devices in the subthreshold regions of both the linear and saturation regimes. There is an observable anticlockwise hysteresis in the linear regime that caused a negative shift in the turn on voltage so that there is a closer agreement in the subthreshold slopes of all devices in both regimes in the return sweep from -60 V to 10 V. Initially V_{ON} is between 7 V and -7 V, on the return sweep V_{OFF} varies from -7 V to 0 V. V_T from the initial sweep varies between -23 V and -25 V in the saturation regime for all but two of the devices where V_T = -16 V. The V_T shifts by ~ 2 V between the initial and return sweep. The saturation subthreshold slope is 6.7 V per decade for device E15 for the initial sweep, and 5.7 V per decade on the return sweep.

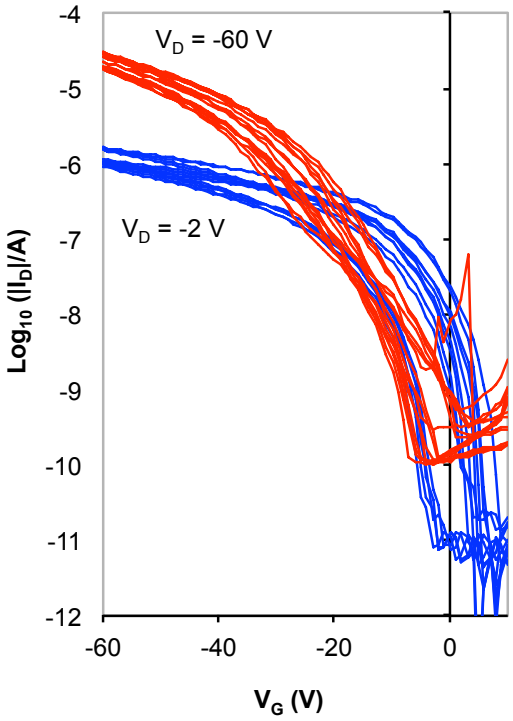

Figure 6.1 Semi-log transfer characteristics in linear (V_D = -2 V) and saturation (V_D = -60 V) regimes of devices fabricated on TPGDA (devices E_10 -E_18)

This was typical of these devices. In saturation the obvious hysteresis at higher V_G is clockwise, but within the subthreshold region the hysteresis switches to an anticlockwise direction. The linear and saturation plots are very similar to the results of Kim *et al*. [1] for pentacene transistors measured in ambient air on a cyanoethylated poly(vinyl alcohol) dielectric with a thickness of 400 nm.

Figure 6.2 shows the performance of DNTT transistor E06 on the TPGDA dielectric. It has the same channel length L as devices E10-E18 shown in Figure 6.1, but a shorter W = 2 mm. The output characteristics are shown in (a). The transfer characteristics are shown in (b): I_D vs V_G in the linear regime (V_D = -2 V) and as $I_D^{1/2}$ vs V_G in the saturation regime (V_D = -60 V). The transfer is re-plotted in (c) in semi-log form, together with the semi-log plot of the gate current, I_G. The gate-voltage-dependent mobility of transistor E06 is plotted against gate voltage in (d).

The output characteristics shown in Figure 6.2 (a) show poor saturation for all gate voltages, significant currents were only observed when $V_G \geq$ -40 V_G. A clear distinction between the linear region and saturation region is only observable for a

gate voltage V_G = -60 V. The characteristics also display anticlockwise hysteresis on the reverse slope.

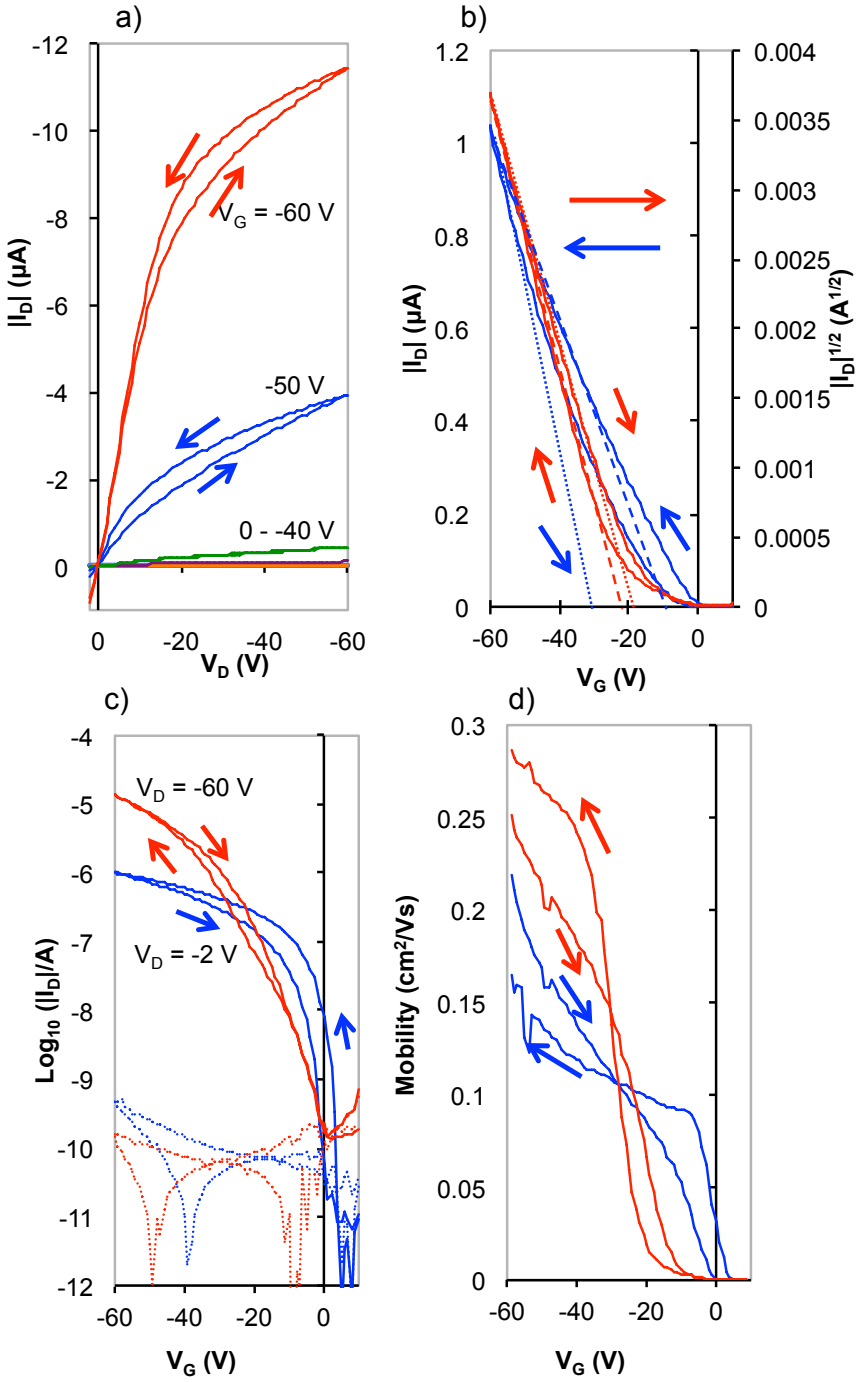

Figure 6.2 (a) Output characteristics of device E06. (b) Transfer characteristics in linear (blue) and saturation (red) regimes. The corresponding tangents from which V_T is estimated are also shown, long dashes for the forward sweep, and short dashes for the return sweep. (c) The semi-log plots of the device transfer characteristics with the corresponding leakage current shown in the same colour using dashed lines. (d) The gate voltage dependent mobility.

The extrapolated tangents of the maximum slopes of the plots of I_D vs V_G (linear) and $I_D^{1/2}$ vs V_G used to estimate the threshold voltage V_T are shown in Figure 6.2 (b). Due to the hysteresis in the measurement, two tangents are taken for each plot, one for the forward sweep (long dashes) and one for the reverse (short dashes). In the linear regime the threshold voltage shifts negatively from -10 V in the forward sweep to -30 V in the return sweep. In the saturation regime the threshold voltage shifts towards positive i.e. from -23 V for the initial sweep to -20 V in the reverse sweep. The mobilities extracted using equations 2.9 and 2.10 for linear and saturations regimes respectively were 0.22 cm^2/Vs and 0.24 cm^2/Vs.

The shape of the semi-log plots of I_D in the saturation and linear regimes in Figure 6.2 (c) closely match those seen in Figure 6.1 for devices E10-E18 and are typical results for a transistor on this substrate. In the linear regime the anticlockwise hysteresis is evident, while in the saturation regime the hysteresis direction is a little more complicated. The initial V_G sweep in the saturation regime has a "double hump" feature where the direction of hysteresis changes from anticlockwise to clockwise. The clockwise direction of the hysteresis is easy to see at high gate voltages, $V_G > -20$ V. However, the hysteresis appears to be anticlockwise at lower gate voltages but is more difficult to observe in this particular device. The corresponding gate current is low both in saturation and linear regimes, < 125 pA.

The subthreshold slope is 7.3 V per decade for the initial slope, and 6.6 V per decade for the return sweep in the saturation regime. There is very little overlap in the subthreshold regions of the linear and saturation regimes, with only the initial V_{OFF} of the linear and saturation slopes being a close match at ~ 0 V. V_{OFF} is the same as V_{ON} in saturation but there is a 4 V difference in the linear regime.

Equations 2.11 and 2.12 were used to calculate the V_G dependent mobility from the data in Figure 6.2 (b) and the results are shown in Figure 6.2 (d). In the linear regime the mobility is higher on the return sweep. This is opposite to the saturation regime where the mobility is highest in the initial sweep. The maximum mobility in Figure 6.2 (b) is 0.29 cm^2/Vs in saturation, and 0.22 cm^2/Vs in the linear regime showing good agreement with the mobilities extracted using equations 2.9 and 2.10.

Figure 6.3 shows the maximum mobilities for all 81 working devices in both linear (μ_{lin}) and saturation (μ_{sat}) regimes for substrate A1, extracted using equations 2.11 and 2.12 respectively.

For TPGDA the hole mobility in saturation ranged from 0.23 cm^2/Vs for device E12 up to 0.86 cm^2/Vs for device A15, with an average of 0.44 cm^2/Vs for all working OTFT devices on the substrate. In the linear regime the average mobility was lower at 0.35 cm^2/Vs, ranging from 0.11 cm^2/Vs for device E17 up to 0.72 cm^2/Vs for device A10. The I_{ON}/I_{OFF} ratios ranged from 10^4 to 10^5 in the saturation regime, the off currents were in a range between hundreds of pA and single nA. Two devices, A14 and B16 had mobilities far below counterpart devices of the same dimensions and were deemed not to be working and are not counted towards the yield. Thus of the original 90 devices 79 gave acceptable performance i.e. a yield of 88%.

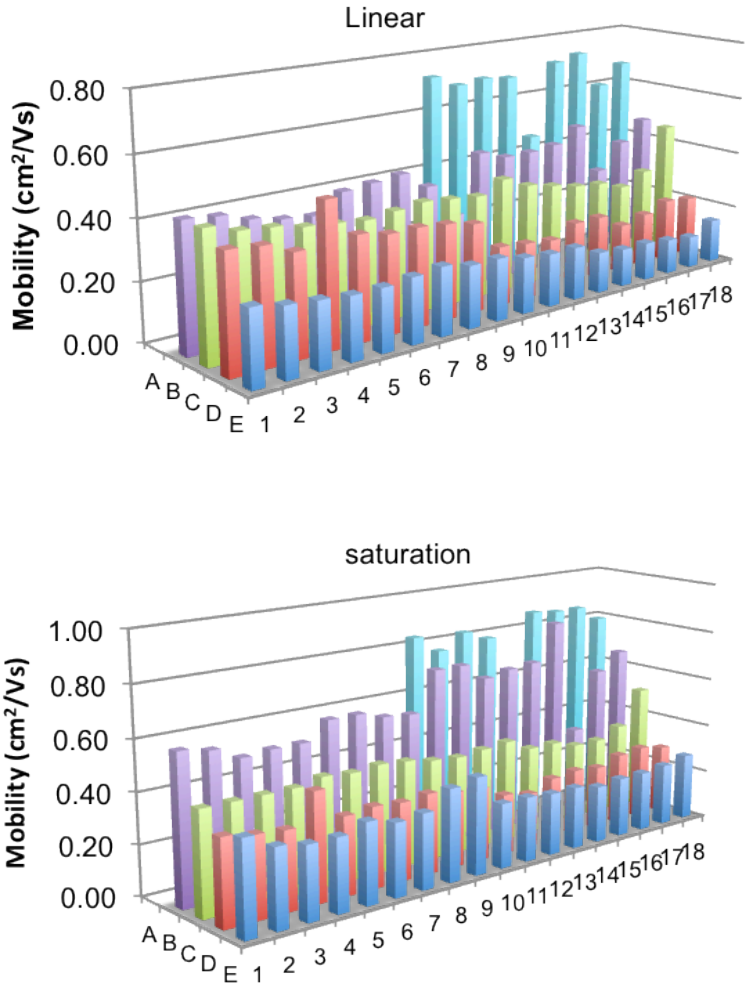

Figure 6.3 Maximum linear and saturation mobilities of all working devices in their relevant position on substrate A1

From Mask Set 3 (Figure 3.9) we can se that there are ten groups of different device dimensions. All devices numbered 01-09 have the same W, but L ranges from 50 μm for devices A to 200 μm for devices E. Devices numbered 10-18 have the same W/L ratio, but L is the same as for the devices numbered 01-09. From Figure 6.3 it is seen that there is a small random variation in mobilities within each group of 9 OTFTs. However, between rows there is a much larger systematic variation that is seen clearly in table 6.1. Here is given the average mobilities in the linear and saturation regimes for each group of 9 devices (excluding A01-A09, A14 and B16).

Table 6.1 The average extracted maximum mobility of each OTFT geometry for substrate A1.

		Average mobility (cm^2/Vs)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
W = 2 mm	01-09 Linear	-	0.40	0.38	0.36	0.22
	01-09 Saturation	-	0.56	0.42	0.33	0.33
W/L = 20	10-18 Linear	0.66	0.41	0.34	0.20	0.15
	10-18 Saturation	0.79	0.65	0.38	0.27	0.25

Using the same transistor designs the bottom-gate OTFTs based on the polystyrene gate dielectric showed no dependence on device geometry (table 5.1). Furthermore, μ_{sat} matched closely to μ_{lin}, but was slightly lower. This is in sharp contrast to the TPGDA case where (i) the extracted mobilities are much lower, (ii) μ_{sat} may be up to ~70% higher than μ_{lin} and (iii) μ_{lin} increases by a factor 4.4 and μ_{sat} by a factor 3.2 as the device dimensions shrink from W = 4 mm, L = 200 μm down to W = 1 mm, L = 50 μm.

6.2.2 Discussion

In terms of the R2R process device yield is good ~88%, higher than the 75% yield obtained in [2] for R2R compatible transistors. Of concern is that the average mobility for the devices on TPGDA, 0.44 cm^2/Vs, is less than half of the value that is being aimed for, 1 cm^2/Vs, that would make it comparable to α-silicon. In comparison the average mobility on PS dielectric was 0.97 cm^2/Vs, making it difficult to argue the case for TPGDA as a stand alone dielectric. There are two factors that could be responsible to the reduced mobility. One is that the crystal structure of DNTT on TPGDA is different to that on PS. Second, it may be due to the fact that TPGDA is a

high k dielectric. As discussed in Chapter 2, this would result in charge scattering due to the dipole moment. Despite this the average saturation mobility is still higher than most of the mobilities quoted for R2R compatible transistors [2]-[7].

There are two other areas of concern regarding the performance of the TPGDA/DNTT transistors that make it difficult to progress to patterning circuits using the current configuration.

The first problem encountered is the device instability, observed most notably in the measurement hysteresis. Device instability is observed in both Figures 6.1 and 6.2. The instability in the device is not restricted to within measurements, but characteristics also vary from one measurement to the next on the same device. For example, in Figure 6.2 (a) V_T was determined from the transfer measurement to be -23 V (-20V on the return sweep). The output characteristics should be showing significant current, therefore, at V_G = -30 V. However, even at V_G = -40 V the output current remains comparatively low. This shows that the V_T has shifted negatively between measuring the transfer and output characteristics.

Due to the opposing directions in the hysteresis of the linear and saturation regimes, along with the unconventional profile of the saturation subthreshold slope, a number of different contributing factors are believed to be responsible for the device instability. Both anticlockwise (linear regime) and clockwise (saturation regime) hysteresis was observed in the transfer characteristics in Figures 6.2 and 6.3. In DNTT devices based on SiO_2 and PS dielectrics, hysteresis was negligible. It could be concluded therefore that the hysteresis here must be associated with the TPGDA. However, it could also arise from the DNTT if its structure on TPGDA was very different to that on the other two dielectrics. For example, if there were more traps in the semiconductor as a result of a higher concentration of structural defects, hysteresis may well occur.

However, the instability is more likely to stem from the TPGDA dielectric itself. TPGDA monomer contains a number of oxygen functional groups, of which a number will be on the surface of the polymer. These can form hydrogen bonds to water molecules, and can act as charge trapping centres. Since the devices were tested in air without encapsulation, atmospheric contaminants such as water and oxygen would

have been absorbed at the interface giving rise to trapping centres as previously shown in [9] and [10].

According to [11] charge trapping and de-trapping at the semiconductor/dielectric interface are believed to be responsible for anticlockwise hysteresis. This, coupled with atmospheric contamination, could explain then the anticlockwise hysteresis in the linear regime. In this case, the trapping of holes at the interface causes the interface to become more positive, becoming repulsive to mobile holes. To maintain the source-drain current, I_D, a more negative V_G is required. This results in a negative threshold voltage shift. However, this is not observed for the saturation regime, where hysteresis is in the opposite direction.

Clockwise hysteresis is believed to be caused by the presence of polar groups and/or ionic species within the dielectric [12]. Due to the presence of oxygen in the structure of the polymer it is likely that water is trapped within the dielectric giving rise to both the polar groups and ionic species. As V_G is swept from 0 V to -60 V polar species within the dielectric will orientate in the electric field while ionic species will drift in the field. In both cases this creates a negative TPGDA surface that shifts V_T to more positive voltages. As V_G is swept back from -60 V to 0 V the polarised species should return to their original state, decreasing the negative charge at the TPGDA interface and turning the channel off. If the polar ionic species react slowly and take a longer time to return to their original state this will lead to a residual positive shift in V_T and higher I_D for a given V_G. This explains the clockwise hysteresis observed in the saturation regime in Figures 6.1 and 6.2 (c).

Such effects have been observed in OTFTs with relatively thick dielectric layers in which there are a number of chemical species that cause slow polarisation [12]. The TPGDA layer on substrate A1 was particularly thick > 1 μm. However, the “double hump” feature of the saturation transfer curve suggests that there is also some degree of interface charge trapping as described in a study by Scheinert *et al*. [13] where the effect of charge traps on the transistor transfer measurement are modelled. They proposed that acceptor-like interface traps cause no interference in the measurement above the threshold voltage, but do have an influence on the subthreshold characteristics. For the initial sweep the trapped interface states are completely occupied by electrons, and are below the Fermi level of the semiconductor. As the gate voltage becomes more negative the trap states recharge causing a dip in the

subthreshold slope. Further increase in the negativity of the gate voltage cause the traps to become neutral and thus have no further influence on the transfer curve. This would explain the two rises seen in the initial sweep of V_G. It is not described what would happen on the return sweep. In the present work the return sweep shows no such dip in the subthreshold slope.

Moisture has been proposed as the source of the hysteresis for pentacene transistors on polymer dielectrics [14][15]. In [14] the source of the hysteresis was determined to be the presence of moisture within the bulk of the dielectric itself, rather than moisture at the interface. However, according to the work of Noh *et al*. [14] annealing the dielectric completely removes the hysteresis. A precaution was taken here of heating the substrates for a period of 10 minutes at 110 ^{O}C prior to the evaporation of DNTT, all steps being taken within a N_2 glovebox. This would suggest that the source of the hysteresis in the present case is not moisture within the bulk of the TPGDA dielectric. However, as the device was tested in ambient conditions it is possible that moisture may have permeated into the dielectric.

The second problem encountered is the apparent geometry dependence of the mobility. This is in contrast to the results for DNTT transistors on PS dielectric in Chapter 5. It has previously been shown that mobility can depend on the channel length for devices with a channel length from 2 – 50 μm [8]. It was also shown in [8] that mobility was independent of channel length for devices of channel length 60 – 175 μm. Here, the shortest channel length is 50 μm, identical to the PS/DNTT transistors where no geometry dependence was observed. The average mobility of the L = 50 μm channel devices was three times that of devices of L = 200 μm. The geometry dependence should not be observed to the degree that it is here and is a concern.

For the row of devices C, there is no difference in geometry across the substrate. Therefore the mobility should be similar for the two blocks of devices 01-09 and 10-18. As can be seen from table 6.1 there is a slight decrease in the average maximum mobility from group 01-09 to the group of devices 10-18. This may suggest that mobilities for devices 01-09 could be higher in general, indicating a trend on the substrate that may be due to a reducing capacitance, or a decreasing channel L. This is also partly supported by Figure 6.3. For devices C01-C09 the extracted maximum mobilities are constant, but there is an observable decrease in the mobilities for

devices C10-C17, particularly in saturation. However, the same pattern is not observed for the other groups of nine devices elsewhere on the substrate.

As the W/L ratio increases from row E to row B (devices 01-09) the average mobility almost doubles (see Table 6.1). For rows E to A where the W/L ratio is constant the increase in mobility is even more marked: μ_{lin} increasing by a factor of 4 and μ_{sat} by a factor 3. In virtually all cases μ_{sat} exceeds μ_{lin}.

Of greater interest is the increasing overall trend in mobility from row E to row A. If device current, I_D, scaled linearly with W and L, then assuming C_i is identical for all devices, then all OTFTs in the array should have the same mobility. That they do not suggests either (a) non linear behaviour or (b) the presence of parasitic source-drain currents.

When the contact resistance is greater than the channel resistance, the device characteristics are expected to be limited by the contacts and not the charge carrier mobility [16] [17]. However, this is only expected for short channel length devices as described earlier [8]. The mobility here increases as the channel length decreases and this can be seen in Figure 6.3 for both linear and saturation mobilities. When the channel length is kept the same and W is the variable there is no difference in channel resistance per unit length so the mobilities of such transistors should be similar. However, it is possible to see in Figure 6.3 that when L is kept constant and W becomes the variable, the transistors that have the shortest W have the highest mobilities.

Since device dimensions are relatively large, it is unlikely that these devices should display non-linear behaviour. It is likely, therefore, to arise from the presence of parasitic currents. Below it is argued that although not a factor in the PS based devices, the TPGDA dielectric can give rise to significant parasitic source-drain currents flowing outside the main channel area as illustrated in Figure 6.4.

The source drain electrodes are in red, DNTT in green and the gate electrode in blue. The DNTT and gate electrode extend beyond the tips of the source-drain electrodes by a distance d_p. It is within this area of DNTT that a gate controlled parasitic source-drain current could flow.

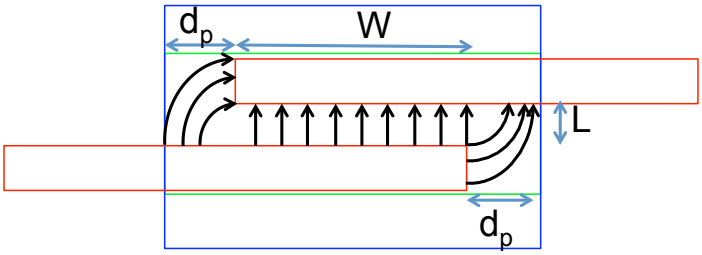

Figure 6.4 Magnified sections of Mask Set 3. It is possible to see how the SD contacts (red) and semiconductor (green) overlap the gate (blue) beyond the channel W of the transistors. The yellow highlighted areas show where charge can be injected into the semiconductor outside of the designed channel.

The distance, d_p, for the various groups of OTFTs is given in Table 6.2. For the majority of devices d_p = 0.45 mm but increases to 0.70 mm for devices B10-B18 and to 0.95 for devices A10-A18. This is summarised in table 6.2.

Table 6.2 The length d_p for each device geometry.

Row	A	B	C	D	E
L (µm)	50	75	100	150	200
Devices 01-09					
W (mm)	2	2	2	2	2
dp (mm)	0.45	0.45	0.45	0.45	0.45
Devices 10-18					
W (mm)	1	1.5	2	3	4
dp (mm)	0.95	0.70	0.45	0.45	0.45

Any of the DNTT semiconductor layer that overlays the gate when it is negatively biased will have a thin accumulation layer of charge carriers at the interface, regardless of being in the defined channel or not. When a potential difference is then applied between the source and drain, the source will inject charge into the accumulation layer along the entire length that is in contact with the DNTT that overlays the gate. As the DNTT becomes more conductive as V_G becomes more negative, it is possible to see in Figure 6.4 how charge can be transferred outside of the defined channel area as more holes accumulate at the surface. This is recognised as a parasitic current.

Assuming that the effect does extend to the edge of the gate/DNTT then of the ten different sizes of transistors in Mask Set 3 devices E 10–18 should be least affected by this parasitic current. These are the transistors where d_p is the smallest % of overall

channel width, W. It can be seen in Table 6.1 that this device geometry had the lowest average linear and saturation mobilities. The opposite is true for devices A, where the highest mobilities are observed, as these are the transistors where d_p forms the highest % of overall channel width. Therefore it can be concluded that the linear mobility of 0.15 cm^2/Vs and saturation mobility of 0.25 cm^2/Vs are probably closer to the true mobility of the TPGDA transistors.

This then raises another question, why is the geometry dependence not observed for the PS/DNTT devices when d_p is identical for both device arrays?

The difference in the dielectric constant of the two materials may be responsible for the geometry dependence. PS has a k of ~2.4, while the k of TPGDA is ~4-6. As discussed earlier in Chapter 2, a high k dielectric has a large dipole moment. Veres *et al*. [18] discussed the hypothesis that polar groups scatter states to create a more spread out DoS. This in part explains the reduced mobility. The proposed reasoning for the geometry dependence is due to the slow polarisation of ionic species in the dielectric layer. The "double hump" feature was deemed to be due to the slow polarisation of ionic species. From Figure 6.5 is it possible to see how as the ionic species align to the field they can attract more holes to the interface.

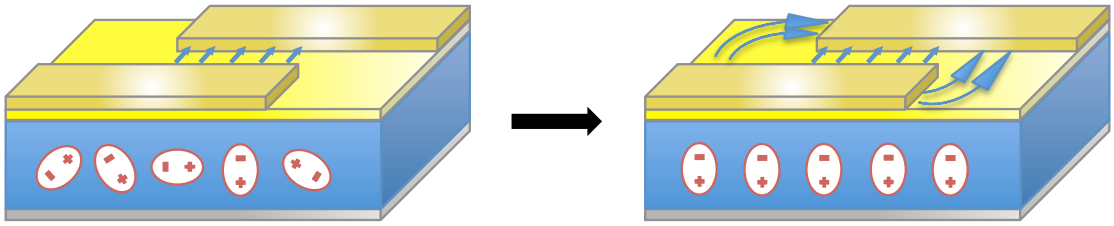

Figure 6.5 The ionic species respond slowly to the applied voltage, as they align the number of holes at the interface increases. Due to the effect of the ionic species the current can pass outside of the defined channel area.

Considering the Vissenberg and Matters model for charge transport [19], there are an increased number of states so mobility is increased. Due to the increase number of holes the current is able to pass outside of the channel, and is limited only by the area of the DNTT and gate overlap.

The intention here was to ascertain the yield and mobility, and to optimise the process to improve both. Although the yield is high, and there is a possibility of improving the mobility, the stability of the transistors during measurements makes progression to multiple transistor devices unproductive, as they would also be unstable during

operation. Now the focus shifted to stabilising the transistor performance of the TPGDA/DNTT transistors.

6.3 Environmental Stability of DNTT

6.3.1 Experimental Results

The stability of DNTT OTFTs has previously been demonstrated: good device performance being maintained over a number of months [20]. To confirm this for the TPGDA dielectric, 2x18 TPGDA/DNTT transistor arrays were fabricated on a 25 mm x 25 mm PEN substrate using mask set 1, as described in section 3.5.4. The transfer and output measurements were taken under ambient dark conditions on a weekly basis using the set-up described in section 3.5. Between measurements the devices were kept in a dark room in ambient air.

Only 29 transistors out of the 36 fabricated worked due to a misalignment of the shadow masks which prevented the semiconductor being deposited onto the channel for 7 of the transistors. The maximum saturation mobility was extracted from the characteristics and recorded for a period of 29 days (Figure 6.6). Initial mobility values ranged from 0.2 cm^2/Vs up to 0.8 cm^2/Vs. One device did break down but continued to work; it can be seen as the highest mobility on day one, but the lowest on day eight onward.

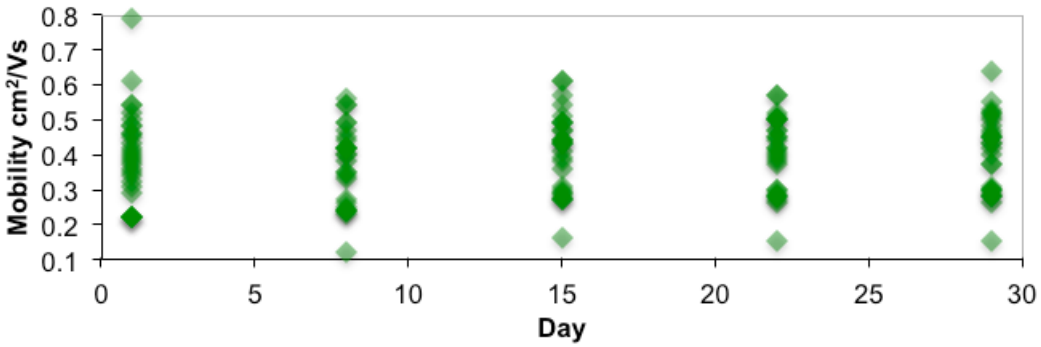

Figure 6.6 Calculated mobility of 29 transistors measured every seven days for a period of 29 days

It can be seen from Figure 6.6 that the maximum saturation mobility is steady over the 29 day period. However, during the same period, the threshold voltage, V_T, and V_{ON} shift positively for both the saturation and linear regimes by ~ 30 V. This also led to a drop in the I_{ON}/I_{OFF} current ratio, because of the increased I_{OFF}.

6.3.2 Discussion

The spread in mobility is significant, even if ignoring the mobility of 0.8 cm^2/Vs on the first day, the mobility of 0.6 cm^2/Vs is three times higher than the lowest mobility, ~ 0.2 cm^2/Vs. This is related to the findings of the previous section where parasitic currents give rise to apparently higher mobilities. However, as can be seen from Figure 6.6, saturation mobility is almost stable over a period of thirty days when kept in ambient dark conditions. The stability of the mobility agrees well with the work of Zschieschang *et al*. [20] where DNTT transistors were shown to have an almost constant mobility for over fifty days whilst they were kept in air. However, in the present case mobility for the group of transistors does vary slightly over the one month time period, probably due to different laboratory temperature and humidity at the time of measurement. This does suggest that any degradation of the DNTT, if there is any, is slow. Although mobility was relatively stable other device parameters were not, e.g. a large shift in V_T occurred. This reflects the instability seen in the OTFTs of the previous section. The next step was to establish what was causing the device instability.

6.4 Transistors In Vacuum

Earlier in this chapter it was suggested that atmospheric contaminants i.e. H_2O and O_2, were partially responsible for the hysteresis observed in the characteristics of the TPGDA OTFTs in Figures 6.1 and 6.2. In order to establish the effect of atmospheric dopants on the performance of the TPGDA/DNTT OTFTs, a comparison was performed between device performance in atmosphere and under vacuum. By measuring the characteristics under vacuum it should be possible to observe the OTFT performance in the absence of atmospheric dopants such as H_2O and O_2. This will aid in understanding the role of such dopants in the device instability.

6.4.1 Results

Transistor D12 was removed from an OTFT array on substrate A3 that was from the same TPGDA batch as substrate A1. For the pre and post vacuum measurements the results were obtained using a similar setup as described in section 3.7 and conducted in ambient dark conditions. The vacuum measurements were conducted under a pressure of 10^{-5} Torr in the dark. Instead of contacts being completed with probe tips

the transistor was mounted in an Oxford Instruments cryostat with contacts being completed using gold wire and silver paste. The transfer characteristics were obtained with V_D = -2 V in the linear regime and at -60 V for saturation. V_G was swept from 20 V to -60 V and back to 20 V. C_i of the TPGDA insulator was measured to be 5.84 nF/cm^2. Measurements were made initially with the device in ambient conditions in the dark, followed by repeated transfer and output measurements in vacuum at 10^{-5} Torr, and finally transfer and output measurements immediately after the device was returned to ambient conditions.

Figures 6.7 (a), (e) and (i) show the transitions in performance from ambient, to vacuum and back to ambient of the transistor output characteristics I_D vs V_D. The transfer characteristics are shown in (b), (f) and (j) for the linear regime, I_D vs V_G (blue), and for the saturation regime, $I_D^{1/2}$ vs V_G (red). The transfer characteristics are re-plotted as semi-log plots in (c), (g) and (k). The gate dependent mobility for linear, μ_{lin}, and saturation, μ_{sat}, is shown in (d), (h) and (l) vs V_G.

From Figures 6.7 (a) to (e) it is possible to see that, initially in ambient conditions, the hysteresis is evident. When the same device is operated under vacuum the hysteresis becomes negligible, and I_D is reduced for equivalent gate voltages. When the device is retuned to ambient conditions in (i), the hysteresis returns and I_D once again increases.

The reduction in I_D under vacuum and recovery in air subsequently is also seen in the transfer characteristics (Figures 6.2 (b), (f) and (j)).

For the transfer characteristic initially measured in ambient condition V_T is initially -16 V for the forward sweep, and -4 V for the return sweep in the saturation regime. In the linear regime the shift is from -4 V to -20 V. In the transfer characteristics taken under vacuum (Figure 6.7 (f)), there is still some hysteresis present in the linear regime at the higher V_G values. The V_T shifts positively from the ambient values in saturation and is stable at -8 V, and in the linear regime it also shifts positively to -10 V. When the measurement is made in ambient conditions after being in vacuum (Figure 6.7 (j)) hysteresis is once again evident. The V_T for the saturation plot shifts negatively from the vacuum vale and is stable at -16 V. There is hysteresis in the linear plot, shifts from -28 V to -18 V in the return sweep.

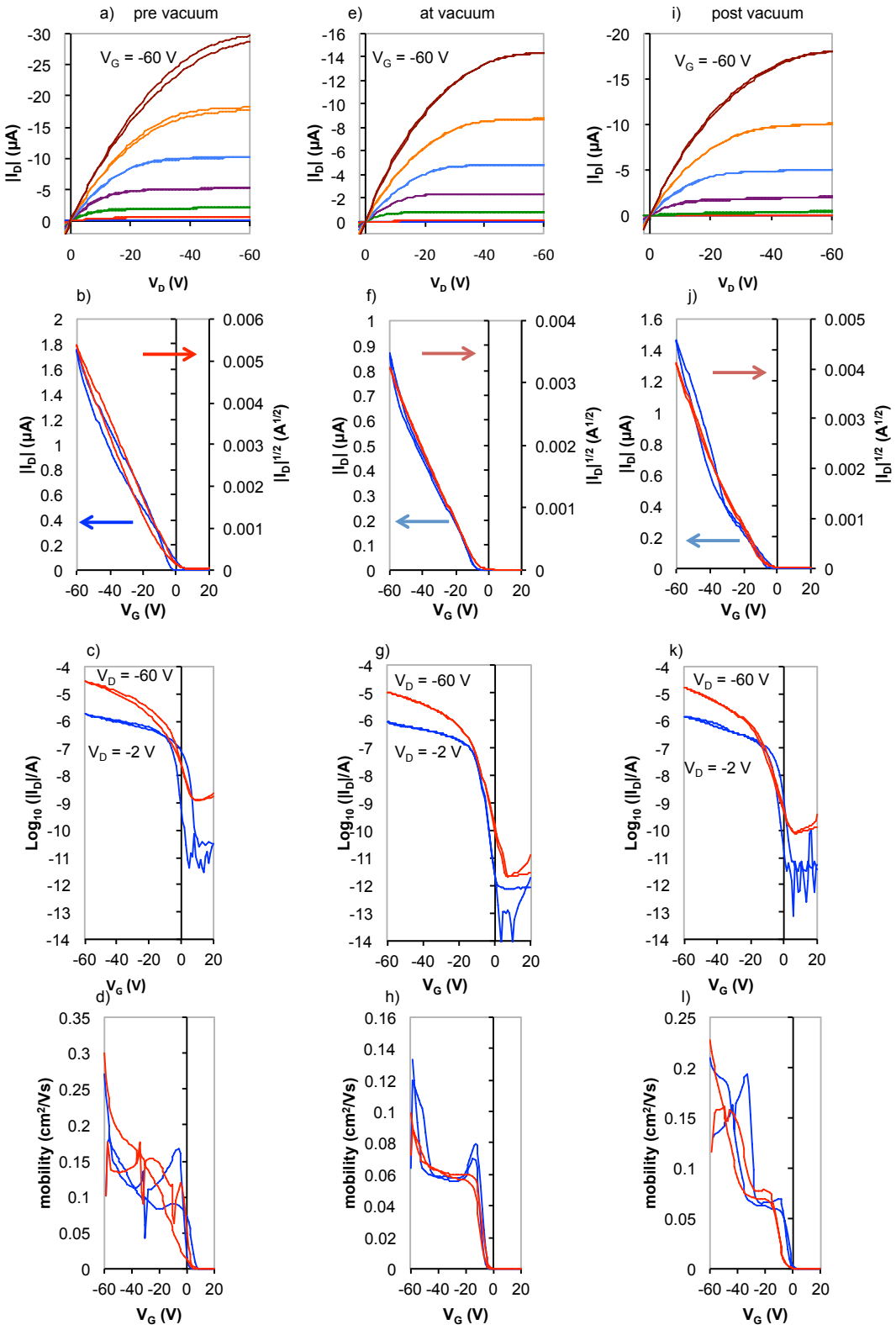

Figure 6.7 Characteristics in linear and saturation regimes of device D12 (a), (b), (c), (d) in ambient pre-vacuum measurement, (e), (f), (g), (h) under vacuum (10^{-5} Torr), and (i), (j), (k), (l) in ambient post vacuum. The output characteristics are shown in (a), (e), (i). The transfer plots are shown in (b), (f), (j) as I_D vs V_G for the linear regime (blue), and $I_D^{1/2}$ vs V_G in the saturation regime (red). The corresponding semi-log transfer plots are shown in (c), (g), (k). The gate voltage dependent linear and saturation mobilities are shown in (d), (h), (l).

The re-plotted transfer characteristics in the form of semi-log plots are shown in Figures 6.7 (c), (g) and (k). Initially in (c) the I_{ON}/I_{OFF} ratio in the linear regime is 10^4, and 10^4 in the saturation regime. The subthreshold slope of the saturation regime is 5.7 V per decade for the initial sweep, and 6.7 V per decade on the return sweep. Under vacuum in (g) the I_{ON}/I_{OFF} ratio increases in the linear regime to 5 x 10^5, and in the saturation regime it increases to 5 x 10^6. This is despite a reduction in I_D, and is due to a reduction in the off current for both saturation and linear regimes, decreasing to a few pA even in the saturation regime. The subthreshold slope was also steeper at 3.9 V per decade in both directions in the saturation regime.

When the device was once again measured in ambient (Figure 6.7 (k)) the saturation off-current increased from a few pA to a few hundred pA, and the off current in the linear regime was an order of magnitude greater than when measured under vacuum. The on/off ratio was reduced to 10^5 and the subthreshold slope in the saturation regime was 6.9 V per decade and 6.5 V per decade for the forward and return sweeps respectively. The I_{ON}/I_{OFF} current ratio was also reduced for the linear regime to 10^5.

Mobilities were extracted using equations 2.10 and 2.11 giving the plots seen in Figure 6.7 (d), (h) and (l) for the gate dependent mobility. The maximum mobility was taken from each plot and were μ_{lin} = 0.36 cm^2/Vs and μ_{sat} = 0.44 cm^2/Vs in the pre-vacuum measurement. Under vacuum, the mobility was reduced, μ_{lin} and μ_{sat} were 0.16 cm^2/Vs and 0.14 cm^2/Vs respectively and significantly lower, therefore, than the pre-vacuum values. Finally the device was returned to ambient conditions in the dark and the measurements immediately repeated. The μ_{lin} and μ_{sat} increased from the vacuum values to 0.26 cm^2/Vs and 0.29 cm^2/Vs respectively, similar to values given earlier in the chapter, i.e. returning partially towards the pre-vacuum values.

6.4.2 Discussion

Pre-vacuum, the transistor is shown to have a performance similar to the devices on substrate A1. Under vacuum, atmospheric species that contaminate the semiconductor-dielectric interface are removed. The removal of these contaminating species eliminated hysteresis and reduced the off current in both saturation and linear regimes. When the device was measured under vacuum the only property not to improve was the mobility.

Thus it may be concluded that atmospheric contaminants were responsible for the hysteresis observed earlier in this chapter. As stated earlier in the chapter the slow polarisation could be due to absorbed water molecules responding slowly to the applied field, causing the clockwise hysteresis observed in the saturation regime.

The reduction in mobility from 0.44 cm^2/Vs in ambient to 0.14 cm^2/Vs in vacuum suggests that there is atmospheric doping of the semiconductor. The reduction in mobility is a result of the removal of doping molecules. This is further supported by the increase in mobility immediately post vacuum, from 0.14 cm^2/Vs to 0.29 cm^2/Vs. Oxygen doping of *p*-type semiconductors by electron transfer from the semiconductor to oxygen has previously been studied [21] and shown to lead to higher mobilities. The doping molecules could also act as charge acceptors in the dielectric.

If TPGDA functional groups were the sole origin of the hysteresis then it would also be observed when the device was operating in vacuum. The functional groups are part of the dielectric structure and cannot be removed by being in vacuum. However, the same functional groups will attract molecules such as O_2 and H_2O when in atmospheric conditions. This is an observation made by Zan and Hsu [22] for pentacene transistors on PVP and PVP-PMMA dielectrics. They reasoned that the reduction in mobility was due to a reduction in the number of hydroxyl groups reacting with water. The hydroxyl groups on the surface of the dielectric become O^-, therefore attracting more hole charge carriers to the surface increasing the extracted mobility. It may be argued that the perceived increase in mobility may be a result of an O^- surface shifting the V_T positively as the transistor is easier to switch on. However, V_T for the initial sweep appears to be the same for their encapsulated and unencapsulated transistors on PVP. If the mobility is increased by the presence of O^- ions at the interface then this could also be true of the TPGDA and would explain the reduced mobility under vacuum. This may also be a possible explanation for the parasitic current observed on TPGDA and not on PS, the O^- ions at the surface facilitating the parasitic current.

Oxygen doping of DNTT in air could also be lowering the resistance between the SD contacts and the accumulation channel. When the atmospheric dopants are removed the series resistance increases, reducing the potential along the channel, resulting in a lower than expected I_D and a reduction in the extracted mobility.

An increase in source and drain series resistance for transistors measured in vacuum was shown to occur by Taylor *et al*. [23] using OTFT parameter extraction software to simulate the characteristics of devices measured in air and under vacuum. To obtain good fits with the air data, it was necessary to set to zero the resistances R_S and R_D associated, respectively, with the source and drain contacts. Under vacuum, for buffered TPGDA transistors, good fits could only be obtained with $R_S = 7.39 \times 10^4\ \Omega$ and $R_D = 8.66 \times 10^4\ \Omega$.

One study concluded that oxygen doping of pentacene resulting in an increase in SD current was photo-induced, occurring mainly in the presence of light [24]. This in particular is strange, as it would be expected that oxygen in the presence of light would oxidise pentacene and reduce mobility. In the present case the semiconductor was DNTT, a more stable material, and the devices were tested in the dark. This suggests that oxygen doping of DNTT does not require exposure to light. The recovery in mobility in the DNTT OTFTs occurred immediately on exposure to atmosphere, while still in the dark. Photo-induced doping could not be responsible for the increased mobility observed here.

Atmospheric contaminants would be removed from the TPGDA prior to DNTT deposition that was deposited at a pressure at a minimum of 6×10^{-6} mBar. Therefore, any contamination of the deposited layers takes place after removal of the substrate from the glove box. It may therefore be possible to prevent the contamination of the semiconductor layer by encapsulating the surface of the completed transistors prior to removal from the glovebox.

6.5 Encapsulated Transistors

Encapsulation has previously been shown to improve device stability [25][22], acting as a barrier to atmospheric contaminants. To test the efficacy of encapsulating devices to minimise atmospheric effects, sets of OTFTs (Mask Set 4 Figure 3.8) were fabricated on two different substrates as described in section 3.5.3. One of these sets was encapsulated by spin-coating at 1000 rpm for 1 minute inside a N_2 glovebox a layer of PS from a 9% wt solution in toluene over the newly fabricated devices. If there are H_2O molecules trapped in the dielectric layer during the fabrication process then hysteresis should still be observed after encapsulation. The encapsulation would

serve to trap any contaminants present in the same way that it acts as a barrier to external contaminants. If the contaminants are removed as expected prior to the deposition of the DNTT then the encapsulation should prevent hysteresis in the measurement and yield transistor characteristics similar to those observed under vacuum.

6.5.1 Results and Discussion

Example results from devices of identical geometry from each substrate are shown in Figure 6.8 (a), (b) and (c) for the encapsulated device and (d), (e) and (f) for the unencapsulated device. The capacitance per unit area, C_i, for these was devices was 5.54 nF/cm^2.

For the transfer characteristics V_D was held at -1 V and -40 V respectively for measurements in the linear and saturation regimes, while V_G was swept from 20 V to -40 V and back again. The first sweep is shown in red while the second sweep performed immediately afterwards is shown in blue.

The output characteristics of the unencapsulated and encapsulated devise are shown in Figures 6.7 (a) and (d) respectively. The transfer characteristics of both transistors are plotted in (b) and (e) as I_D vs V_G in the linear regime, and $I_D^{1/2}$ vs V_G in the saturation regime. The tangents used to determine the V_T are not shown as the plots would be difficult to see. Both transfer plots are re-plotted in (c) and (f) in semilog form for the linear and saturation regimes.

Figures 6.7 (a) and (d) show the output characteristics of the unencapsulated and encapsulated device respectively. Both have a very similar profile, in that the drain current continues to increase substantially in saturation. However there are slight differences. The drain currents of the unencapsulated transistor are higher than for the drain currents of the encapsulated transistor at a corresponding V_G. There is also hysteresis in the plots of I_D vs V_D of the unencapsulated transistor, but not in the encapsulated transistor.

The transfer plots for the unencapsulated and encapsulated transistors are shown in Figures 6.7 (b) and (e) respectively. The dashed plots represent the linear regime, I_D vs V_G, red for the initial sweep and blue for the second. The solid plots represent measurements in the saturation regime, $I_D^{1/2}$ vs V_G, red for the initial sweep and blue

for the second. For the transfer characteristics of the unencapsulated device seen in (b) the hysteresis is significant.

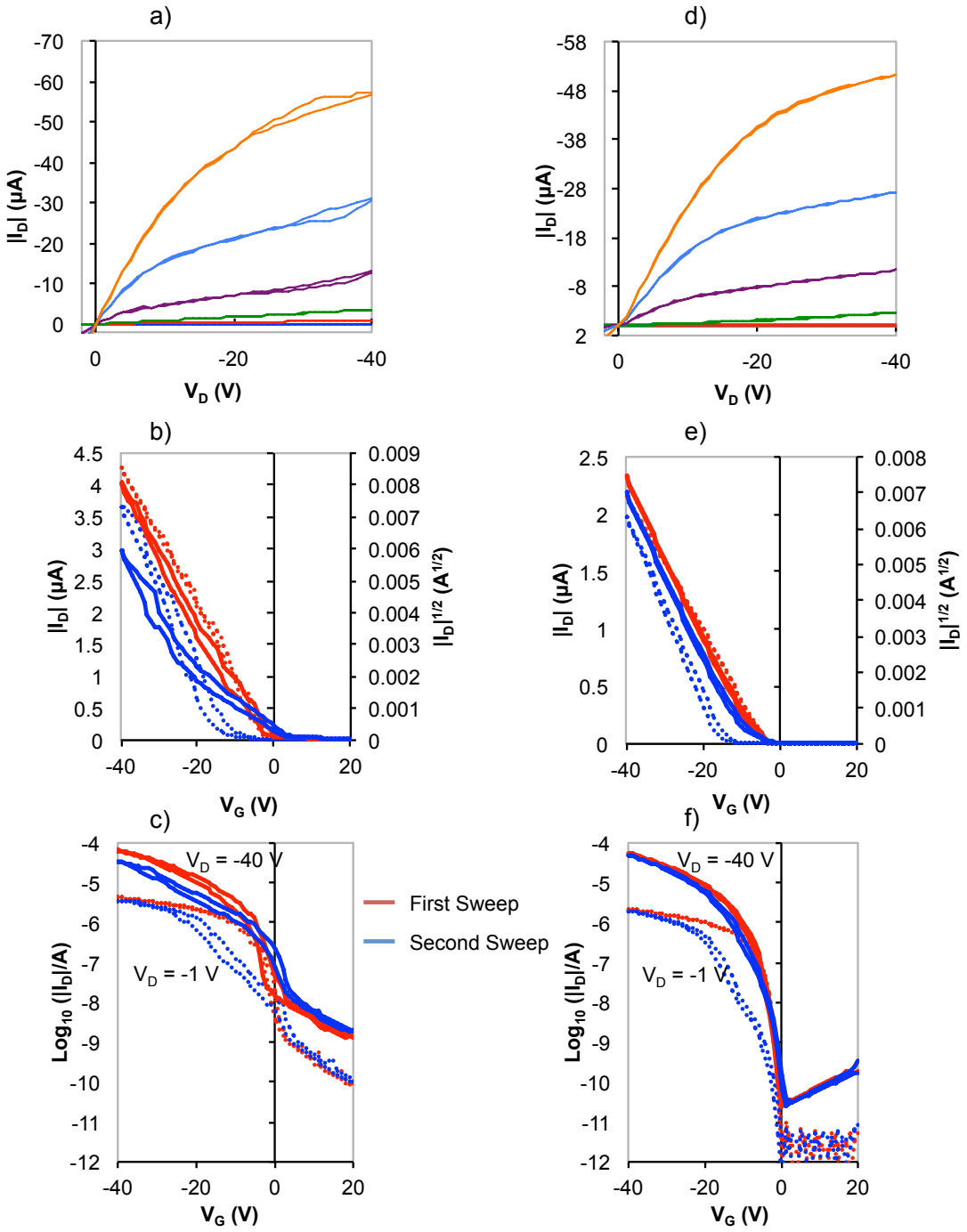

Figure 6.8 The output characteristics of the un-encapsulated transistor are shown in (a) and of the encapsulated transistor in (d). Sequentially measured transfer characteristics in linear (blue plots) and saturation regimes (red plots) of (b) the un-encapsulated transistor and (e) the encapsulated transistor. The semi-log plot of the transfer measurements are shown in (c) for the unencapsulated transistor, and in (f) for the encapsulated transistor.

V_T in both the linear and saturation regimes shifts negatively between measurements, the peak saturation drain current reduces significantly from -65 μA to -36 μA, a difference of 29 μA. In contrast, the transfer characteristics of the encapsulated transistor shown in (e) displays hysteresis only in the second sweep, and it is much less significant than that observed for the unencapsulated device.

The saturation regime is particularly stable, and only a small V_T shift is observed, the reduction in the peak saturation current is much less, from -56 μA to -49 μA, the difference here is only 7 μA. However, the V_T shift in the linear regime of the encapsulated transistor is almost identical to the V_T shift in the linear regime of the unencapsulated transistor. This shows that even though it is encapsulated it is not entirely stable. This is probably due to a slow permeation of atmospheric dopants through the encapsulant. As shown earlier, PS layers are prone to pin-holes which are routes for contamination of the semiconductor and the underlying dielectric.

The subthreshold slopes of the initial sweeps of the linear and saturation semi-log plots are 3.6 and 3.8 V per decade respectively for the unencapsulated transistor (Figure 6.8 (c)). The subthreshold slopes increase to 5.9 and 4.9 V per decade for the linear and saturation regimes respectively on the second sweep. The encapsulated transistor performs better. The subthreshold slopes in the initial sweep were 3.0 and 2.6 V per decade for the linear and saturation regimes as seen in (f) becoming 3.4 and 2.6 V per decade for the linear and saturation regimes respectively.

It can be seen from Figures 6.7 (c) and (d) the off current of the unencapsulated transistor is ~ 100 times larger than that of the encapsulated transistor. The encapsulated transistor displays an off current that is close to that of the transistor in vacuum, the same observations were made by Abbas *et al*. in [25] for pentacene transistors. The unencapsulated transistor has an I_{ON}/I_{OFF} ratio of 10^3 in the linear regime and $>10^3$ in the saturation regime. For the encapsulated transistor the I_{ON}/I_{OFF} ratio in the linear regime is 10^5, and in the saturation regime is 10^6, again showing the advantage of encapsulation. The lower off-current of the encapsulated transistor suggests a link between doping and higher bulk currents in the unencapsulated transistor. This once again echoes work done in [22]

The gate dependent mobility was extracted using equation 2.10 for the linear regime, and equation 2.11 for the saturation regime. The maximum mobility in the linear

regime for the unencapsulated transistor was 0.46 cm^2/Vs, and for the saturation regime was 0.60 cm^2/Vs. In comparison the maximum mobility extracted for the encapsulated transistor was lower in both the linear regime, 0.22 cm^2/Vs, and in the saturation regime, 0.38 cm^2/Vs. The higher mobility observed for the unencapsulated transistor was as expected. As seen in the previous section, atmospheric doping increases mobility and the un-encapsulated device will be more prone to such doping.

It can be concluded that encapsulation does slow down the permeation of the transistor layer by atmospheric contaminants. The reduced off-currents and increased stability of the encapsulated transistor also shows that any contamination of the TPGDA during transportation is removed during the remainder of the device fabrication. Unfortunately what is shown here is the unsuitability of TPGDA as a stand alone dielectric for the fabrication of organic circuits, as even encapsulation does not appear to entirely stabilise the device. Although the device yield is good, the transistor operation is not stable, even with encapsulation. Inverters were fabricated to demonstrate why the instability of the TPGDA/DNTT transistors were unsuitable for circuit fabrication.

6.6 TPGDA/DNTT Inverter

6.6.1 Experimental Results

The experimental set up was as described in section 3.8.1. The dimensions for the top contact inverter are different to those for the bottom contact inverter due to the difficulty in patterning small feature sizes using shadow masks. For the driver W = 2.5 mm, and L = 50 μm. For the load W = 625 μm and L = 100 μm giving a driver/load conductance ratio of 8:1.

Under ambient conditions, V_{DD} was set to -60 V, -40 V, -20 V and V_{IN} was swept from 0 V to -60 V as V_{OUT} was measured. With V_{DD} = -60 V the gain reached a maximum of 3.2, Figure 6.9 (a), but for V_{DD} = -20 V the gain reached only 0.7. Figure 6.9 (a) also shows the square-wave input response of inverter n3_1_2 to a signal alternating between 0 V and -60 V (V_{DD} = -60 V).

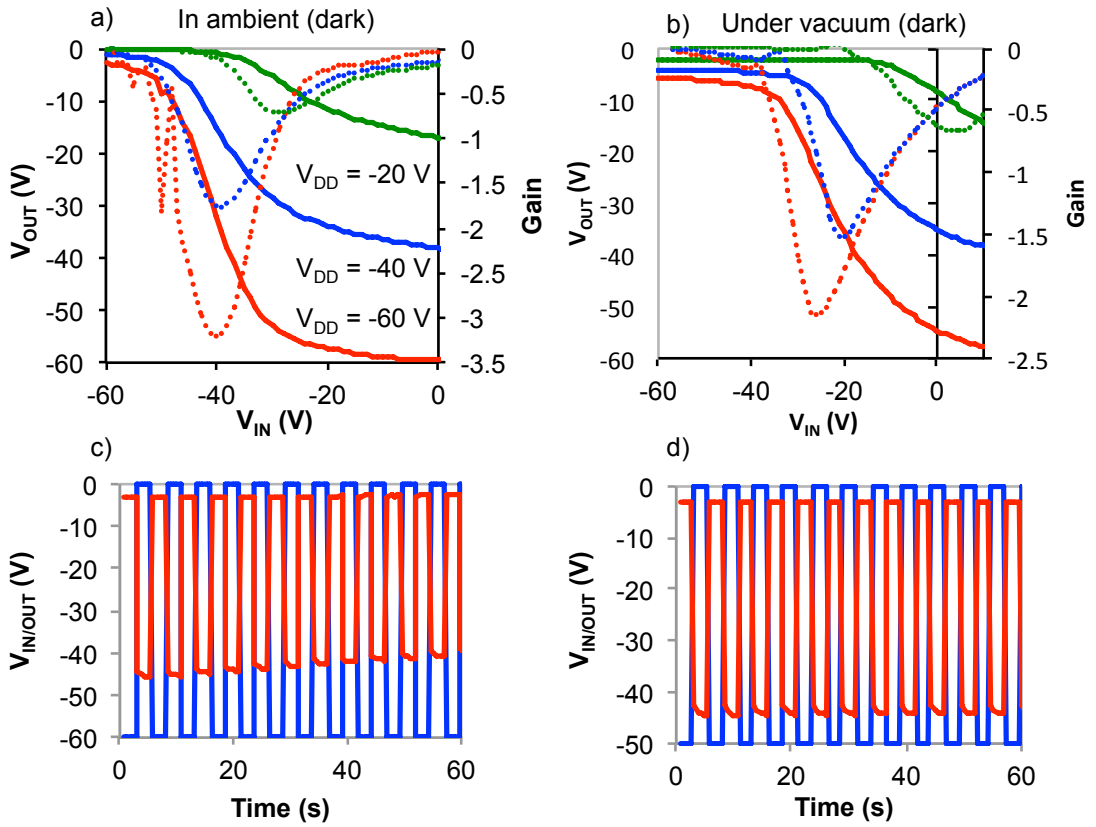

Figure 6.9 Voltage transfer plots (solid curves) and gain (dashed curves) of DNTT/TPGDA inverter in (a) ambient dark and (b) under vacuum (10^{-5} Torr). Response V_{OUT} of DNTT/TPGDA inverter (c) in ambient dark and (d) under vacuum (10^{-5} Torr) to an input square wave, V_{IN} (blue).

The input signal is inverted, but with each subsequent switch V_{OUT} reduces. The V_{OUT} swing was initially 41.7 V, but fell to 36.4 V after 60 seconds. When the same device was measured in vacuum the maximum gain for V_{DD} = -60 V was 2.2, but at -20 V again decreased to 0.7. The transition region shifted positively for all rail voltages from the values obtained when measured in ambient conditions. In vacuum there was no observable shift in V_{OUT} the swing being 41.1 V for the duration of the measurement, for a input square wave of 50 V amplitude.

6.6.2 Discussion

The square wave response of the inverter demonstrates why the TPGDA/DNTT transistors are unsuitable for organic circuit fabrication. The output response to V_{IN} under ambient conditions shows a reduction in V_{OUT} with each switch from V_{OL} to V_{OH}. This points towards a possible V_T shift in the load transistor towards negative, and its ability to "pull up" reduces with each successive switch. The shift appears to

occur due to atmospheric contamination of the interface, as the reduction in V_{OUT} is not observed when the measurement is conducted in vacuum. Even with a reduced rail and input voltages for the inverter tested under vacuum, the output swing is only 1 V less than the initial switch when tested at higher voltages in ambient conditions. It is concluded therefore that TPGDA is unsuitable as a stand-alone dielectric for organic transistor fabrication.

6.7 Summary

90 transistors were fabricated using DNTT as the semiconductor and with a TPGDA dielectric in a bottom-gate-top-contact configuration using Mask Set 3. 81 functioning transistors were characterised by transfer and output measurements. The transistors gave a range of mobility values from 0.23 cm^2/Vs to 0.86 cm^2/Vs in saturation, μ_{sat}, and 0.11 cm^2/Vs to 0.72 cm^2/Vs in the linear regime, μ_{lin}. All transistors displayed both clockwise (saturation regime) and anticlockwise (linear regime) hysteresis. The mobility values were shown to be overestimated due to parasitic currents arising from overlap of the semiconductor and gate electrodes outside of the channel area.

The stability of DNTT was evaluated over a period of 29 days, the output and transfer characteristics being measured once a week. The results show that the extracted mobility, μ_{sat}, is relatively stable throughout the period. The slow, cyclical changes that occur are attributed to differences in room temperature at the time of the measurements.

A transistor of the same BGTC configuration was characterised in ambient conditions, then under vacuum and again in ambient conditions. Hysteresis and mobility were shown to decrease under vacuum. There are two possible explanations for these observations. Firstly, the direct effect of O_2 on the hole mobility in the channel is reversed during vacuum measurements. Secondly, O_2 doping of the bulk DNTT reduces the series resistance between the contacts and the channel. Removal of the dopants in vacuum would increase the series resistance, thus reducing the actual potential available for charge accumulation in the channel.

Two transistors were then fabricated with the same configuration, one being encapsulated. The encapsulation was shown to improve device stability but only

partially eradicated device instability in ambient, probably due to the existence of pinholes in the encapsulating PS layer.

Inverters were fabricated from TPGDA/DNTT OTFTs using Mask Set 4. The inverter transfer and square wave responses were measured in ambient conditions and under vacuum. The device was shown to be unstable in ambient by the reduction in the output swing, but performed well in vacuum with a stable output swing.

PS could be deemed to be a more suitable dielectric than TPGDA, but it is not processible in an all-evaporated system and does not give the yield of transistors that TPGDA does. However, TPGDA as a single layer dielectric is not suitable for the R2R printing of electronics. Devices are not stable in air, the mobility values are too low, and there is little reproducibility of results between batches of substrates. Modifying the surface of the TPGDA so that it is hydrophobic may stabilise device performance without compromising device yield.

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Chapter 7

PS-TPGDA/DNTT Transistors and Ring Oscillators

7.1 Introduction

In Chapter 6 it was shown that TPGDA was unsuitable as a stand-alone dielectric for transistor fabrication due to device instability. However, transistors were fabricated at high yield, >90 %, with gate currents remaining low in all devices. In chapter 5 we showed that PS was unreliable as a stand-alone dielectric due to a lower device yield <70%, that would be unsuitable for more complicated device fabrication. When the PS transistors worked (low I_G) they were shown to have good saturation and linear mobilities of ~1 cm^2/Vs. PS has previously been shown to passivate polar dielectric surfaces [1]. This was also shown to work for transistors on TPGDA by Ding *et al*. [2]. This made it possible to combine the advantages of both materials. Although PS cannot be deposited in a vacuum based system it was used to demonstrate what was achievable by passivating the surface of the high yield TPGDA. It also separates the DNTT from direct contact with the oxygen molecules of the TPGDA polymer layer. The combined thickness of the two layers (TPGDA ~ 500 nm and PS ~ 300 nm) was ~ 800 nm, similar to the thickness of the dielectrics of the previous transistors.

In this chapter we will demonstrate that it was possible to fabricate transistors with a mobility of ~1 cm^2/Vs to a high yield by combining the properties of the PS layer with those of TPGDA layers in a bilayer gate dielectric. The same device configuration was then used to fabricate inverters, and due to the high device yield, fully integrated ring oscillators.

7.2 PS-TPGDA/DNTT Transistors

7.2.1 Results

The fabrication process for the passivation of the TPGDA layer with PS is described in section 3.3.4, the transistors being completed with a DNTT dielectric. Results were

obtained using the setup described in section 3.4 and conducted in ambient dark conditions.

Due to the reported short lifetimes of OTFTs [3, 4, 5] it is usually desirable to test transistors immediately after fabrication. It had been apparent from the immediate testing of DNTT transistors on both the PS and TPGDA dielectrics upon removal from the glovebox that initially the devices appeared not to work or to work poorly. The same was true for devices on PS-TPGDA dielectric. It was observed that devices improved gradually, taking over 48 hours to stabilise. Figure 7.1 shows a sequence of transfer plots obtained in saturation and plotted in semi-log form together with the corresponding I_G measured on a single transistor over a period of 47 hours. The gate current, I_G, was below 500 pA for all measurements. When the device was tested immediately after fabrication the transfer characteristics (I_D vs V_G) were poor (the 0 H plot in Figure 7.1), I_D reached ~100 nA.

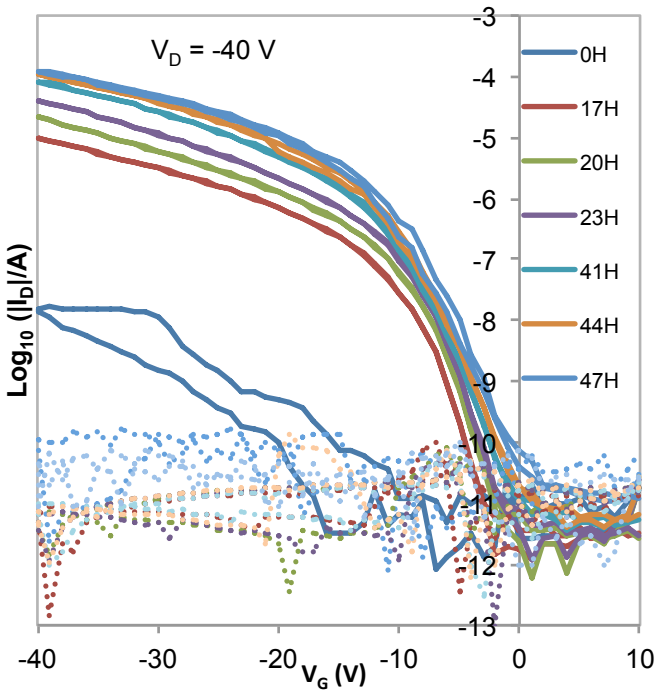

Figure 7.1 Semi-log transfer of a PS-TPGDA/DNTT transistor in saturation at different time intervals over a 48 hour period.

The measurement was noisy, there was a large degree of hysteresis and no discernable subthreshold region. It therefore appears at first that the transistor does not work. After 17 hours the device had improved dramatically and the hysteresis became

negligible. After 40 hours the device began to stabilise and any further improvement in device performance was minimal.

Figure 7.2 (a) shows an example of the linear and saturation transfer characteristics, plotted in semi-log form, of a group of nine adjacent common gate devices (D10–D18) that have the same transistor dimensions. The corresponding gate currents, I_G, are shown in Figure 7.2 (b).

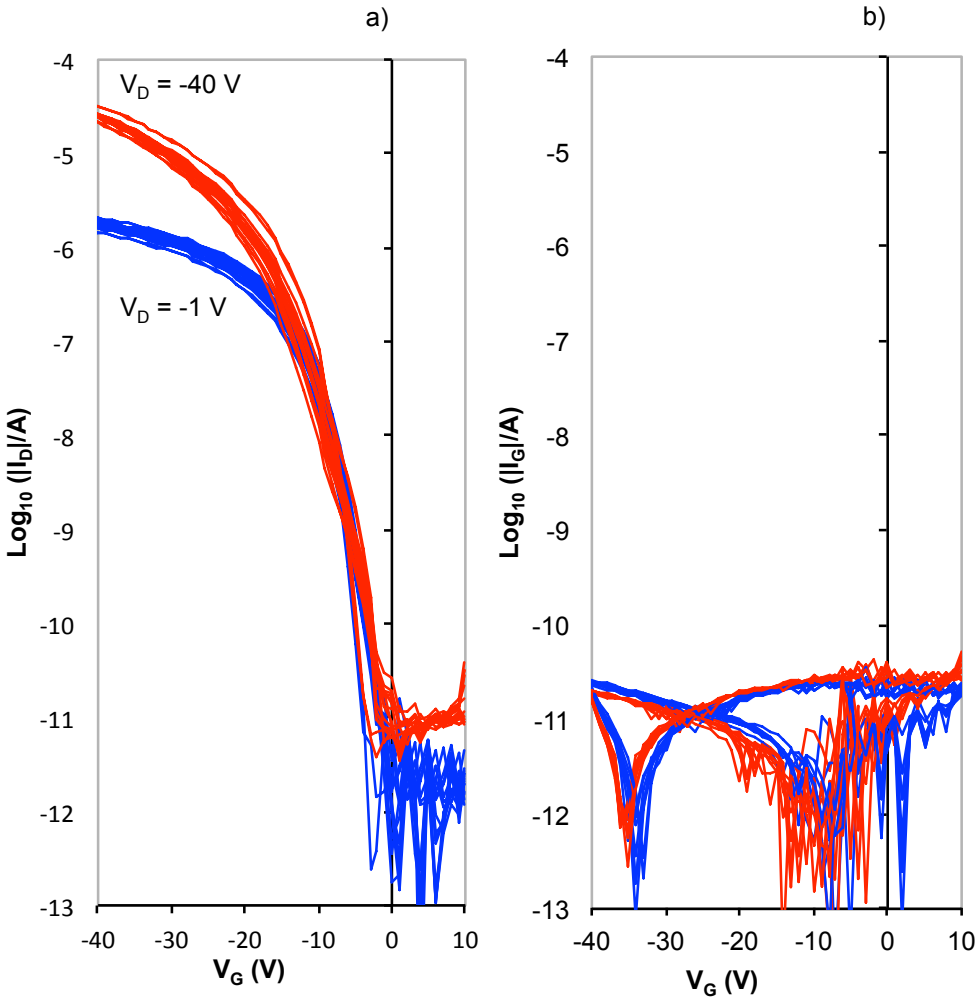

Figure 7.2 (a) Semi-log transfer characteristics in linear and saturation regimes of devices fabricated on PS-TPGDA (D10 -D18). (b) The corresponding gate leakage current, I_G, of both the linear and saturation regimes.

The observations for this group was typical of the various device geometries on the PS-TPGDA dielectric. The initial and return sweeps show good alignment of the linear and saturation regimes in the subthreshold regions. V_{ON} is between 0 V and -3 V, with negligible difference on the return sweep for all transistors in both regimes. V_T varies between -12 V and -15 V for all of the devices with no significant V_T shift

between the forward and reverse sweeps. The I_{ON}/I_{OFF} ratio is $>10^6$ in the saturation regime for all transistors and $>10^5$ in the linear regime. All of the devices within this group show a low gate current (Figure 7.2 (b)) I_G remains below 100 pA for all devices in both the saturation and linear regimes.

Figure 7.3 shows the transfer and output characteristics of transistor D10 that also features in Figure 7.2. The results are typical for a transistor on substrate APS1. The output characteristics are shown in Figure 7.3 (a), where I_D is plotted vs V_D for various gate voltages. The plots show good transistor behaviour with well defined linear and saturation regions and no hysteresis.

Figure 7.3 (b) shows the transfer characteristics of the linear regime, μ_{lin}, plotted as I_D vs V_G, and of the saturation regime, μ_{sat}, plotted as $I_D^{1/2}$ vs V_G. The transfer characteristic is re-plotted in Figure 7.3 (c) in semi-log form, along with the corresponding gate current, I_G, for both regimes. Figure 7.3 (d) shows the gate dependent mobility for both the linear and saturation regimes.

Hysteresis is also negligible in the transfer characteristics. V_T is -15 V for both the initial and return sweeps, as shown by the intercept of the dashed lines with the x-axis. The linear and saturation mobilities were extracted using equations 2.9 and 2.10 respectively. The mobility extracted for the linear region was 0.97 cm^2/Vs and in saturation was 1.15 cm^2/Vs.

The saturation curve again shows a hint of the "double hump" feature in the forward sweep that was seen in the TPGDA transistors in chapter 6. The saturation curve initially closely follows the linear curve, but becomes shallower at V_G = -6 V before becoming steeper and surpassing the linear curve at V_G = -12 V. Therefore, for V_G between -6 V and -12 V I_D at V_D = -40 V is lower than for V_D = -1 V. The gate current is low for both the saturation and linear regimes,< 70 μA. The subthreshold slope is 2.9 V per decade for the initial slope, and 3.01 V per decade for the return sweep in saturation. $V_{ON} = V_{OFF}$ = -1 V for both saturation and linear regimes.

The gate dependent mobilities were extracted using equation 2.11 for the linear regime, and equation 2.12 for the saturation regime and plotted against V_G as shown in Figure 7.3 (d). The maximum extracted mobilities were 1.39 cm^2/Vs in the saturation and 0.95 cm^2/Vs in the linear regimes.

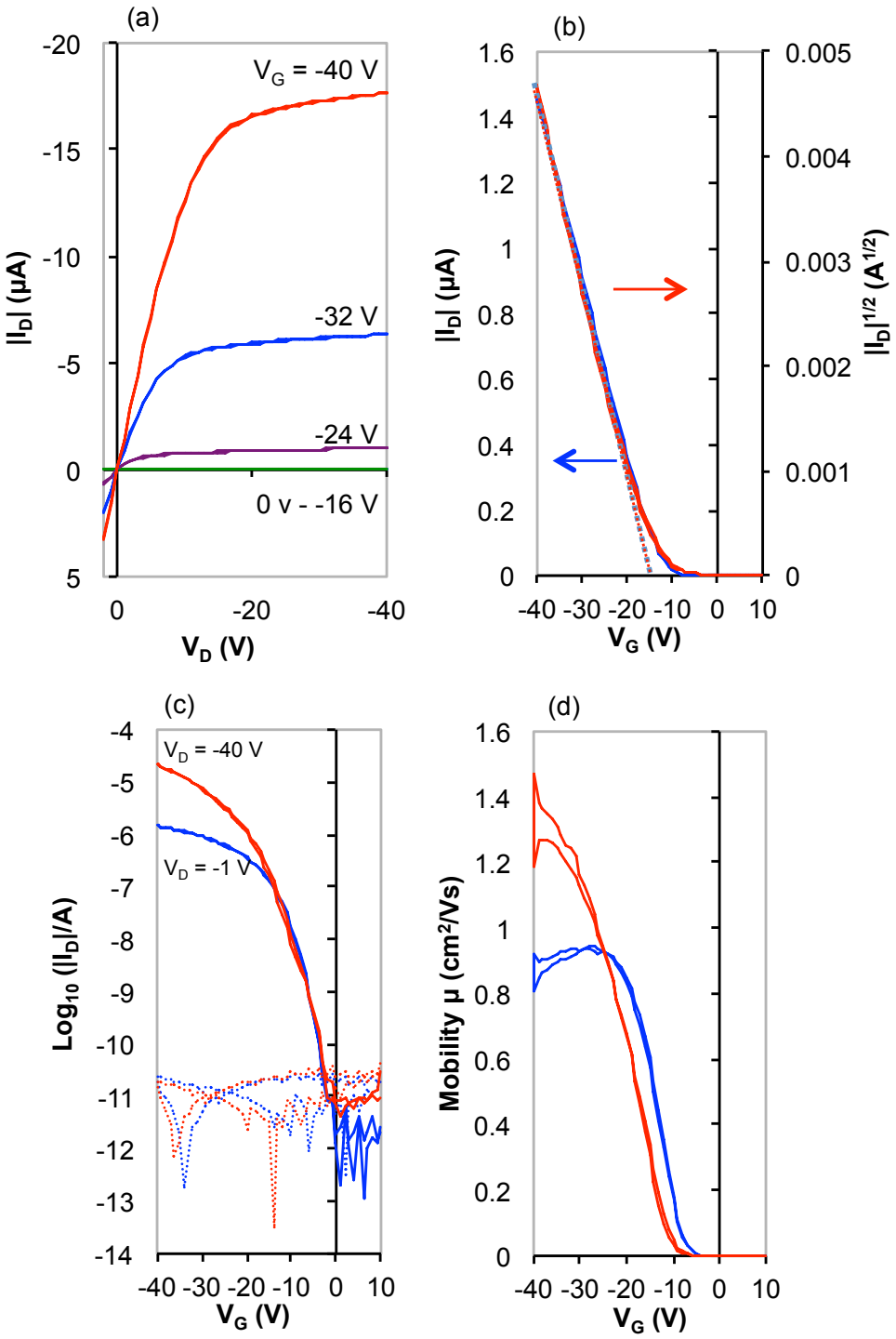

Figure 7.3 (a) Output characteristics of transistor D10 for a range of gate voltages (V_G = 0 to -40 V). (b) Transfer characteristics in linear, I_D vs V_G (blue), and saturation $I_D^{1/2}$ vs V_G (red), regimes. The corresponding tangents from which V_T is estimated are shown by the dashed lines. (c) The semi-log plots of the device transfer characteristic with the corresponding leakage current shown in the same colour as the dashed line. (d) The gate voltage dependent mobility in both the linear (blue) and saturation (red) regimes.

The same measurements were performed for each working device on the substrate. For this substrate the only devices found to be faulty were E01-E09. This was due to a fold in the substrate surface obstructing the deposition of PS for these devices. The remaining 81 transistors on a 50 mm x 50 mm substrate were characterised. C_i of the PS-TPGDA was measured to be 3.29 nF/cm^2. The maximum mobility was extracted for all transistors in both the linear and saturation regimes. The results are shown in Figure 7.4.

For PS-TPGDA the hole mobility in saturation ranged from 0.86 cm^2/Vs (C09) up to 2.14 cm^2/Vs (A17), with an average of 1.51 cm^2/Vs for all working OTFT devices on the substrate. In the linear regime the average mobility was lower at 1.16 cm^2/Vs, ranging from 0.52 cm^2/Vs (C09) up to 1.58 cm^2/Vs (A17).

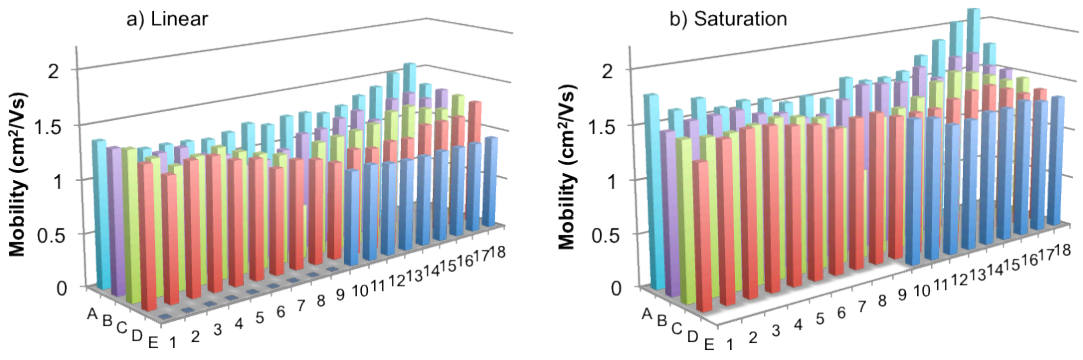

Figure 7.4 Maximum linear and saturation mobilities of all working devices in their relevant position on the substrate.

The I_{ON}/I_{OFF} ratios were mostly $>10^6$, only in row A were lower values observed, five devices at 10^4 and two devices at 10^5. As the W/L ratio decreases from row A to row D (devices E01-E09 were damaged) devices there is a small decrease in device mobility in both the saturation and linear regimes. The mobility ALSO decreases in devices A to E in the group where W is constant. It is the same pattern as was observed for transistors on the TPGDA dielectric. Device C09 had a linear and saturation mobility significantly lower than the other transistors on the substrate, therefore although the device is working it is regarded as a failed device. This gives 80 transistors out of 90 working as expected and a yield of ~ 89 % (~ 98 % for tested transistors).

7.2.2 Transistor Characterisation After Six Months in Air

The end product of an R2R printing process is envisioned to be disposable low cost electronics. However, due to the reactive nature of organic materials such products may be expected to have a limited shelf life. Due to this, confirming good transistor operation over an extended period of time becomes important.

To test the stabilities of the PS-TPGDA devices the substrate was stored in an unsealed petri dish under lab conditions (room temperature and humidity) and kept in the dark. After six months a number of the transistors were re-characterised. Figure 7.5 shows the resulting transfer characteristics for transistors E10-E18.

It is clear from Figure 7.5 (a) that the V_T has shifted positively over time. Only one device, E18, stands apart from the other transistors with a V_T of -10 V. The range of V_T values has also reduced to a 1 V difference for the majority of the devices, with good agreement between the saturation and linear regimes.

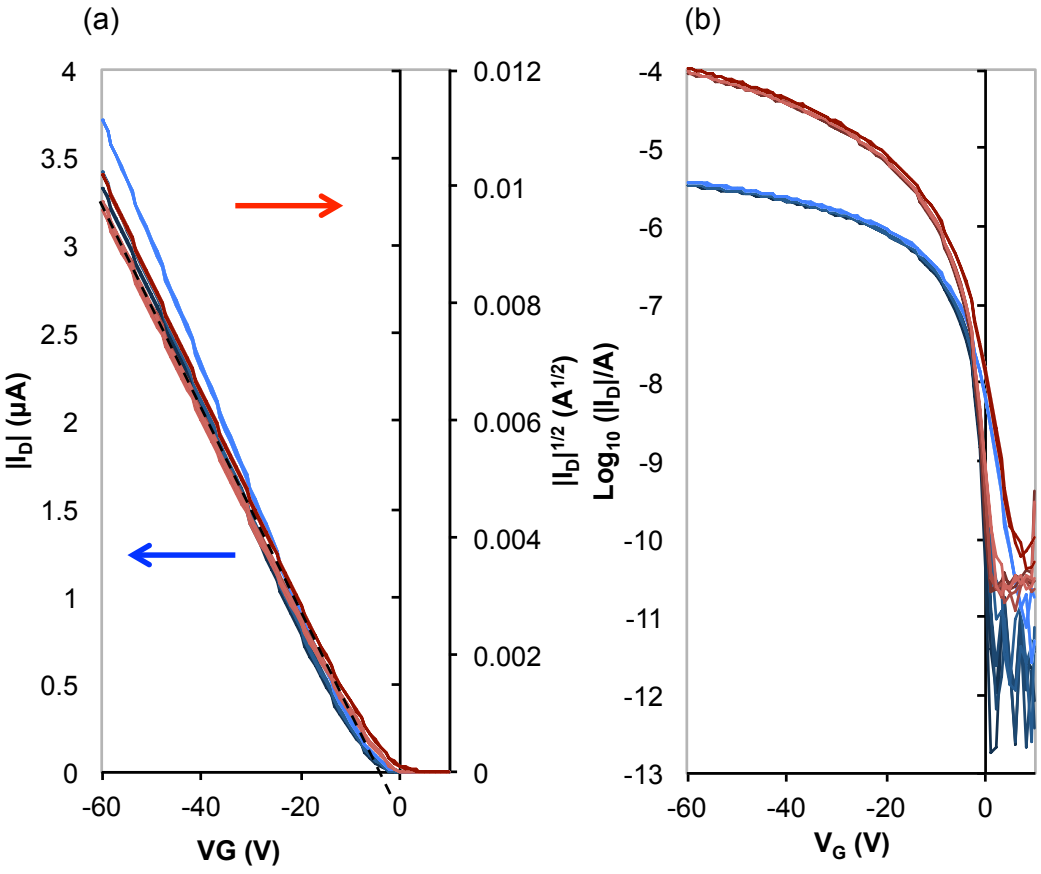

Figure 7.5 (a) Transfer characteristics of devices E10-E18 in the linear regime, I_D vs V_G (blue plots), an in the saturation regime, $I_D^{1/2}$ vs V_G (red plots). (b) Transfer characteristics of devices E10-E18 re-plotted in semi-log form for both the linear regime (blue plots) and saturation regime (red plots).

The close agreement in the two regimes is also seen in the subthreshold slopes seen in Figure 7.5 (b). The characteristics of each device here are almost identical. The agreement in device performance is closer than six months previously as seen for devices D10-D18 (Figure 7.2 (a)).

However, the mobility is now significantly lower, ~ 1 cm^2/Vs, than was initially extracted, indicating perhaps some device degradation.

To assess the stability of the aged transistors a transfer sweep in both the linear and saturation regimes was performed sequentially 20 times. The results are shown in Figure 7.6 (a).

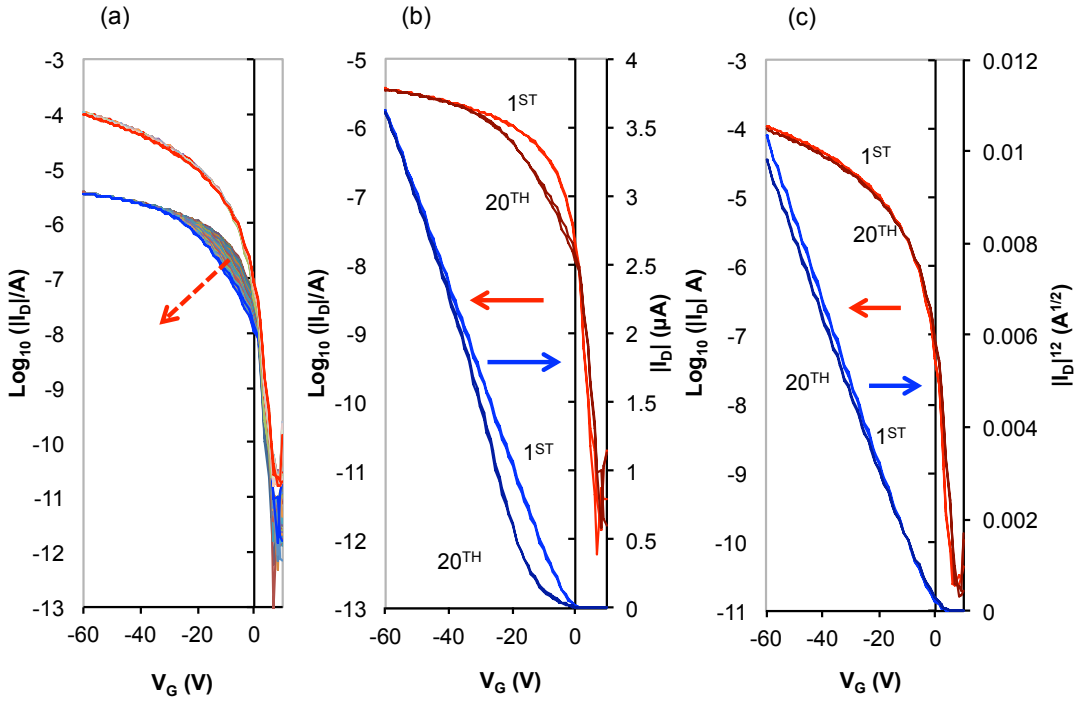

Figure 7.6 (a) 20 cycled sweeps of the transfer characteristic plotted in semi-log form for both the linear an saturation regime. A feature is observed in the linear regime that is not seen in the saturation regime, the effect getting larger with each sweep as shown by the red dashed arrow. (b) The linear transfer plots (I_D vs V_G) for the first (light blue) and twentieth (dark blue) cycles, the corresponding semi-log plots are also shown. (c) The corresponding saturation plots.

On the first sweep, the linear plot (Figure 7.9 (b)) is as expected, a straight line above V_T and ~ 0 below V_T. At low and high voltages the successive sweeps match well. However, on each successive sweep the linear plot departs from the ideal in the

middle of the sweep range. The saturation regime does not display this local shift. However, the V_T does shift marginally to positive values with each successive sweep.

The first and twentieth linear transfer plots, I_D vs V_G (light blue and dark blue), and corresponding semi-log plots are shown in Figure 7.6 (b). It is clear that between 0 and -40 V for the twentieth sweep that the plot diverges from the behaviour described by equation 2.9. Interestingly there is no hysteresis, so the anomaly appears to be V_G dependent as well as V_D dependent (the feature is not observed in the saturation regime).

Such characteristics were also observed for the encapsulated TPGDA/DNTT transistor (Figure 6.8 (f)), where there was a shift within a particular range of V_G for the linear regime while the saturation regime remained stable. Even after six months, however, transistors formed on PS-TPGDA are still more stable than those fabricated on a single layer of TPGDA.

7.2.3 A Closer Look At Parasitic Currents

Although not as marked as for the TPGDA-based transistors, nevertheless, there is a clear trend of increasing mobility with reducing channel width W for the PS-TPGDA devices. In this section, the possible reason for this is investigated.

Figure 7.7 shows the average mobilities of the ten different geometry groups of nine transistors patterned using Mask Set 3 for DNTT OTFTs on three different dielectrics, (a) PS, (b) TPGDA and (c) TPGDA/PS plotted as a function of the channel width, W.

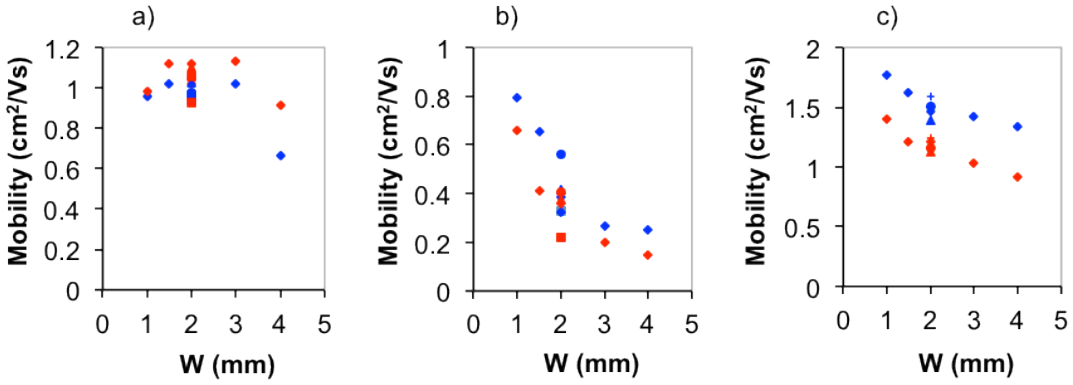

Figure 7.7 The average mobility of the ten groups of 9 transistors vs channel width for (a) polystyrene, (b) TPGDA and (c) TPGDA-PS dielectrics. Saturation mobilities are shown in blue, linear mobilities in red.

In Figure 7.7 (a) the PS transistors show no dependence of mobility on the channel length L or on the channel width, W. The linear mobility is slightly higher than the corresponding saturation mobility but both are ~ 1.0 cm^2 in all cases except for L = 200 μm and W = 4 mm which appears to be an anomalous result. In contrast the mobility in TPGDA transistors in Figure 7.7 (b) show a strong dependence on W, the mobility increasing markedly from W = 4 mm to W = 1 mm. Here, the saturation mobility is always higher than the linear mobility. There is a ~ 350% increase in the saturation mobility from devices E to A. Figure 7.7 (c) shows the average mobilities of the 9 different groups of transistors on the combined TPGDA-PS dielectric. As with the TPGDA dielectric there is an obvious trend, an increase in mobility with decreasing W. Also, here again the saturation mobility is always higher than the corresponding linear mobility. However, the dependence on W does not seem as strong as it does for the transistors on TPGDA. The % increase in device mobility from devices E to A is much lower than for the TPGDA transistors ~ 32%.

It is clear therefore that the mobility may be overestimated in the smaller devices and a parasitic source-drain current is the likely cause as demonstrated in Chapter 6 section 2.2. Such parasitic currents are difficult to demonstrate using the TPGDA dielectric transistors due to device instability between sequential measurements. The PS-TPGDA devices were stable, allowing a better opportunity to confirm the presence of such a current. Device A11 (W = 1mm, L = 50 μm), was chosen as it was determined to be one of the devices where parasitic current would have the most influence. After checking that the device operated normally, the conducting channel was removed by scraping away the semiconductor as shown in Figure 7.8 so that only a parasitic current could be responsible for any observed device current. This leaves only the areas described as d_p in Chapter 6.

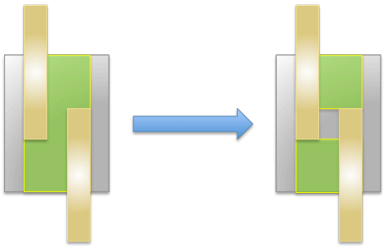

Figure 7.8 A schematic showing the channel area removed so that any measured I_D can only be due to a parasitic current

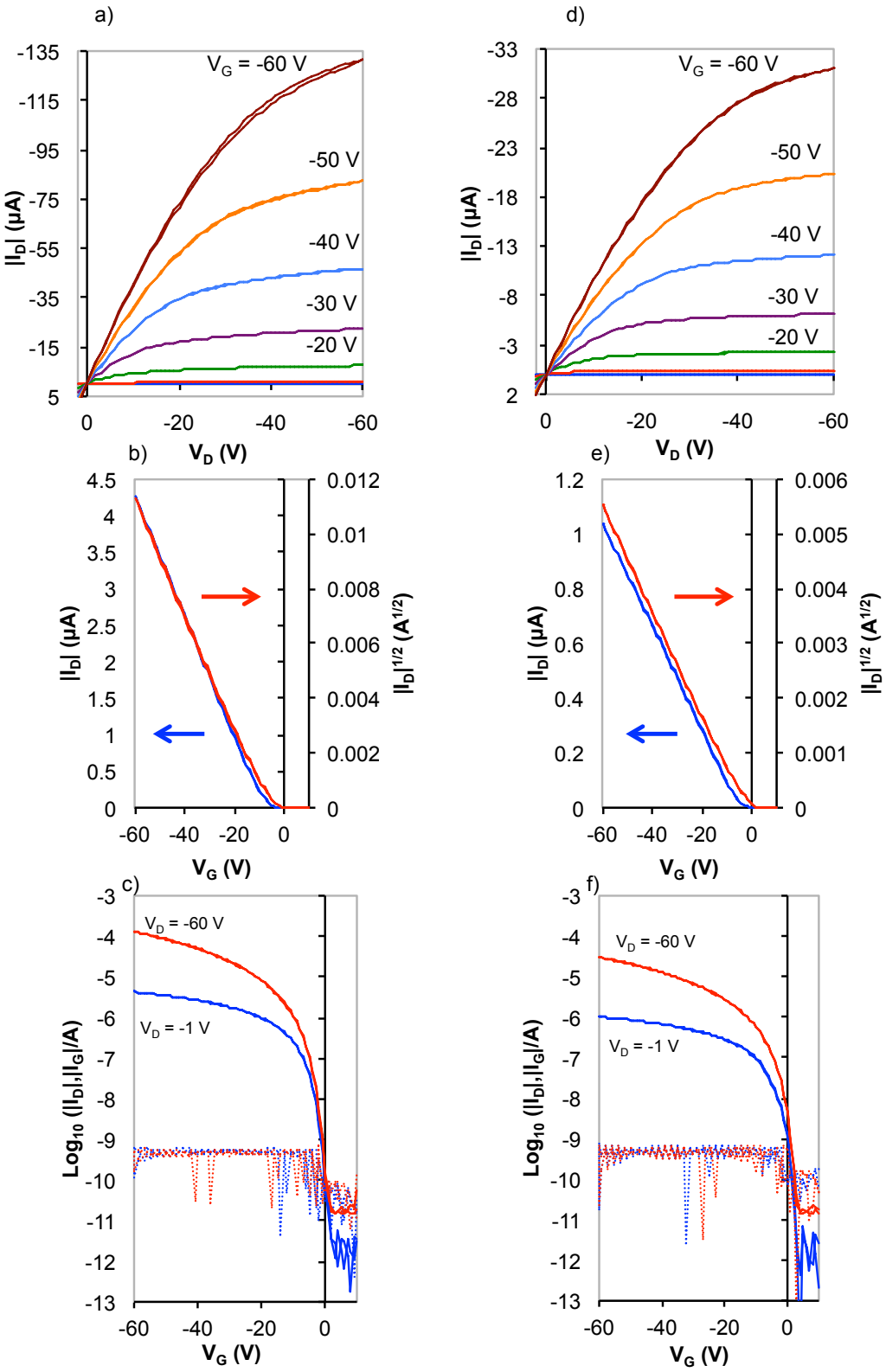

Figure 7.9 The output current of transistor A11 (a) before and (d) after the channel is removed. The transfer characteristics are shown in the linear regime (V_D = -1 V, blue) and saturation regime (V_D = -60 V, red) (b) before and (e) after removing the conducting channel. The transfer characteristics are re-plotted in semi-log form in (c) and (f) corresponding to (b) and (e) respectively.

Output and transfer characteristics were measured immediately before and immediately after removing the semiconductor layer from the channel. The results are shown in Figure 7.9. The output characteristics are in Figures 7.9 (a) and (d) for the before and after measurements respectively. The corresponding transfer plots are shown in Figures 7.9 (b) and (e), and are re-plotted in semi-log form in (c) and (f).

Although these measurements were carried out some six months after the original measurements on device A11, the device performance is very similar. Interestingly after removing DNTT from the channel region the device still shows transfer-like characteristics.

Figures 7.9 (a) and (d) both show that the device exhibits typical transistor output behaviour and good saturation with no evidence of contact effects. There is some hysteresis in Figure 7.9 (a), however, it is negligible. For V_G = -60 V, and prior to removing the channel, the transistor has a maximum drain current, I_D, of ~ 130 μA. After removing the channel the maximum drain current reduced to ~ 31 μA at V_G = -60 V. The parasitic current in this case must, therefore, have contributed ~ 24% to the drain current observed in Figure 7.9 (a). This is close to accounting for the increase in mobility between devices E and A.

The transfer plots confirm that the parasitic current is ~ 25% of the current initially observed prior to the removal of the channel.

From the semi-log plots shown in Figures 7.9 (c) and (f) it is seen that even though the drain current has been reduced by removing the channel, the gate current, I_G remains the same and is low in both devices. It is also possible to see that the off currents in both the linear and saturation regimes are not affected by the removal of the semiconducting channel.

7.2.4 Discussion

The gradual improvement in transistor performance in the first two days after fabrication has also been observed in pentacene devices [6]. There the effect was attributed to the relaxation of the crystal structure following the pressure change upon removing the devices from the vacuum deposition chamber into the atmosphere. A second possible reason is that atmospheric oxygen diffuses into the DNTT as was shown for poly(3-hexyl thiophene) in [7]. Oxygen is known to act as a p-type dopant

in many organic semiconductors, thus increasing the hole concentration [8]. This could have two consequences; (a) increasing the conductivity of the bulk DNTT between the contacts and the channel and (b) directly increasing mobility. A correlation has been shown between increased mobility and increasing dopant concentration [9].

Devices fabricated on TPGDA were shown to be sensitive to atmospheric moisture, which led to device instability and hysteresis effects. The lack of hysteresis in the PS-TPGDA and PS dielectric transistors suggests that the interaction between the TPGDA surface and atmospheric moisture is prevented from occurring by the PS buffer layer due to the hydrophobic nature of PS.

90 transistors were fabricated of which 81 gave good performance, i.e. a transistor yield of 90%. This would have been higher but for the defect in the PEN substrate. Not only was the transistor yield high, so was the device mobility, averaging ~ 1.51 cm^2/Vs for the substrate. Even assuming that there is an overestimation of the mobility and that it is probably closer to 1 cm^2/Vs, this is still comparable to α–silicon. However, it is lower than many recently quoted mobilities for other organic transistors [10-13], including for other DNTT transistors [14], but is higher than mobilities quoted for other R2R compatible processes [15-21]. The requirement for a transistor mobility exceeding 1 cm^2/Vs for the fabrication of RFIDs, sensors and displays was said to be difficult to achieve [22]. Here, only a single transistor fails that target (in the saturation regime) out of the 81 that were characterised. This shows that a vacuum based R2R process can be viable in fabricating a large quantity of transistors with a good mobility.

There is a hint in the saturation semi-log plot of the "double hump" observed in the TPGDA transistors. However, there is no hysteresis or shifts in V_T. This suggests that the TPGDA has an effect on the semiconductor that is not an interface interaction. An explanation for this could be that the dipole moment of the TPGDA is having an effect through the PS layer. However, this has not been observed in similar work done by Ding *et al*. [2] for thinner buffer layers. This suggests that the TPGDA film has significant variation quality between batches. Although the difference in device performance may also be due to the long exposure of the TPGDA films to the atmosphere during transportation between Oxford and Bangor. However, as stated earlier any contaminants should be removed from the 10 minute heating of the

substrate inside the N_2 glovebox prior to commencing fabrication. If the 10 minutes is not long enough to remove all of the water then the deposition of the PS layer will trap any water present in the film. This would then have implications on device performance.

However, device stability due to the PS layer is emphasised by the excellent performance of the devices measured six months after fabrication. The characteristics of individual devices are closely matched, possibly in better agreement after the six month period than when initially measured 48 hours after fabrication. There was no hysteresis in the device characteristics, and the stability of the devices was demonstrated in the saturation regime with only a small shift in V_T over 20 cycles. A possible explanation for the disappearance of the "double hump" feature is that the trapped contaminants have been slowly removed over time resulting in more closely matched transistor performance.

However, there was an anomaly in the linear transfer regime that became more prominent with each successive sweep. When considering equation 2.9,

$$I_D = \mu C_i \frac{W}{L}(V_G - V_T)V_D$$

it can be seen that there are two independent variables here that can result in the change in I_D, namely μ and V_T. The divergence from the linear dependence is probably caused by a change in V_T at low V_G that becomes more pronounced as the number of cycles increases. This shift was also observed by Ding *et al*. [23], however this was observed in saturation. Indoor relative humidity in the UK is between 30 % and 80 %, therefore the humidity could be affecting the results in the present study. However, why it is not observed for saturation can at present not be explained.

Even though the transistor characteristics of the PS-TPGDA dielectric transistors were shown to be as stable (no hysteresis) with similar characteristics to the BGTC PS dielectric devices, the mobility showed a dependence on both the channel W and L, although to a lesser degree than for the TPGDA dielectric devices.

The increasing mobility with decreasing channel W relationship was attributed to parasitic source-drain currents flowing through the DNTT outside of the channel area. That the effect is reduced in the PS-TPGDA dielectric transistors compared to the TPGDA devices suggests that it is related to a bulk phenomenon in the TPGDA and

not simply the presence of O^- ions at the interface. The bulk phenomenon is probably the slow polarisation of ionic species within the TPGDA layer as described in Chapter 6. Here, the effect was screened to some degree by the PS layer, while the effect of the dipolar disorder at the interface was completely negated. This then leads to the higher mobilities that were observed.

These parasitic currents need to be taken into account when designing transistors for a R2R printed circuit. They cannot be entirely avoided due to registration issues. Substrates travelling at several metres per minute will inevitably not align perfectly the entire way through a printing system. The substrate travel needs to be compensated for in device design. This will mean that there will be an overlap of SD contacts, DNTT and gate contact outside the channel area. The semiconductor area could be used to define the channel width, but this would require longer contacts that take up more space on the substrate for an equivalent output and is not feasible therefore for a production process where registration is an issue. When designing circuits it is important to be aware that parasitics could lead to large overestimations of the transistor mobility.

This is particularly true of common gate devices where the semiconductor is spin coated. Even if contacts are designed so that there is no overlap, a parasitic current may still be present at the tips of the contact.

Of note here is that high yield and high mobility transistors have been realised. Not only this, but the transistors are also stable with negligible hysteresis. Thus the target of the previous chapter was achieved. This is particularly important as it makes progression to more complex circuit elements possible. The next step is to fabricate two transistor inverters.

7.3 TPGDA/PS DNTT Inverters

With a high yield of good transistors now guaranteed, the programme proceeded to the next step, i.e. fabricating inverters that consist of two transistors - a driver transistor and a load transistor. Although inverters had been fabricated previously in this work, there were issues with device stability. Due to the stable device operation of the PS-TPGDA/DNTT transistors in air without encapsulation, and the uniform performance of geometrically identical transistors, it was believed that it would be

possible to fabricate air stable inverters. Using Mask Set 4 (Figure 3.10), 27 testable inverters were fabricated on PEN substrates.

7.3.1 Experimental Results

There were some restrictions on the inverter design. First, the devices were unipolar, so the inverter had to be an enhancement load or depletion mode device. As the V_T of our transistors was highly negative (-15 V), they would be non-conducting in the depletion mode load and require a separate gate bias supply to operate correctly. Therefore, the inverters had to be enhancement load devices as shown in Figure 2.13 (b).

Figure 7.10 shows the voltage transfer and corresponding gain plots for a range of V_{DD} from -20 to -60 V, for a unipolar PS-TPGDA/DNTT enhancement load inverter that has a conductance ratio of 10:1. The measurements were recorded using an Agilent DSO-X-2014A oscilloscope. The driver has the dimensions L = 50 µm and W = 4 mm, and the load has the dimensions L = 50 µm and W = 0.4 mm.

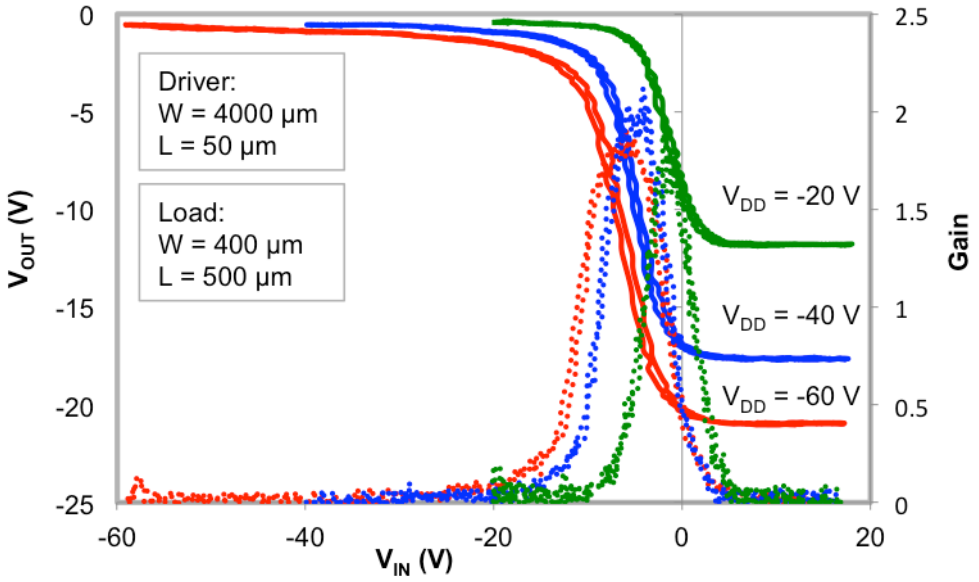

Figure 7.10 Inverter transfer and gain at a range of rail voltages, -20 – 60 V V_{DD}. V_{IN} sweep rate = 1 V/ms.

The maximum gain, found at the point where the voltage transfer slope is steepest was 1.88 at V_{DD} = -60 V, 2.1 AT V_{DD} = -40 V and 1.71 at V_{DD} = -20 V. The voltage swing was relatively poor at all rail voltages, at -60 V V_{DD} it is 20.4 V, at -40 V V_{DD} it is 17.1 V and at -20 V V_{DD} it is 11.4 V. Regardless of the poor V_{OUT} swing, the

transition region between the two points at which the gain = 1 (V_{1L} and V_{1H}) was sharp. There is an asymmetry in the device performance, with V_{TR} more positive than the ideal values, and a significant difference in the high and low noise margins. Of note is the low noise margin at V_{DD} = -20 V. Here, the low output voltage (V_{OL}) is higher than the input voltage at which the inverter enters the transition region.

Table 7.1 Key inverter characteristics at various V_{DD} voltages.

V_{DD} (V)	NM_L (V)	NM_H (V)	Gain	V_{TR} (V)	ΔV_{OUT} (V)
-60	1.4	10.0	1.9	-8.0	20.4
-40	1.1	8.6	2.1	-6.5	17.2
-20	-	5.8	1.8	-3.3	11.4

Figure 7.11 (a) shows the dynamic response to a 100 Hz square wave input oscillating between 0 and -40 V, with V_{DD} = -40 V, of an inverter with a driver to load conductance ratio of 8:1. Inverter (a) has a driver with the dimensions L = 50 µm and W = 2.5 mm, while the load has the dimensions of L = 100 µm and W = 0.625 mm. In Figure 7.11 (b) is shown the square wave response of the inverter in Figure 7.10 to the same signal at the same rail voltage.

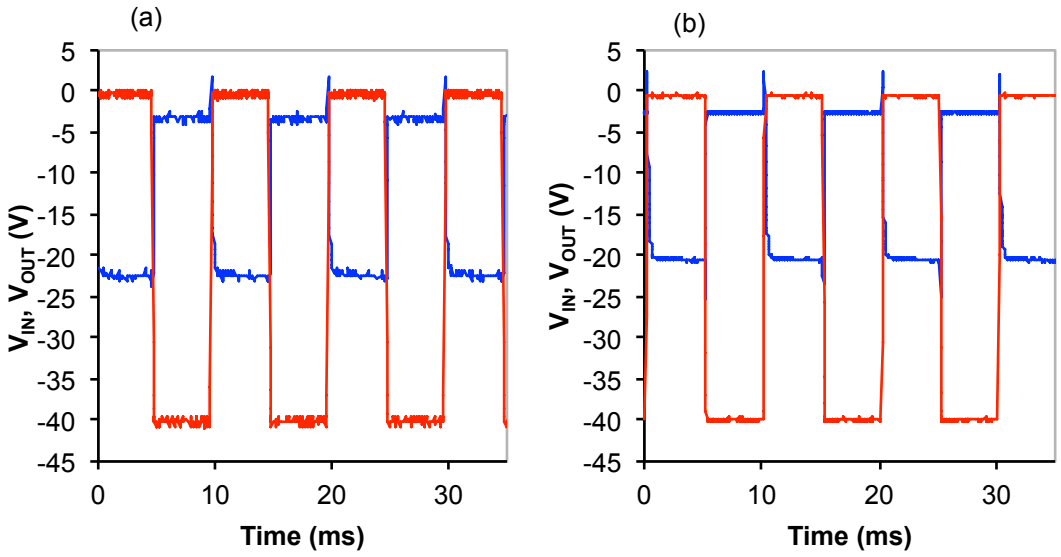

Figure 7.11 Square wave responses (blue) of two different inverters to a 100 Hz input frequency (red) at V_{DD} = 40 V. Conductance ratios of driver to load transistors are (a) 8:1 and (b) 10:1.

The spikes observed when the output signal switches are capacitive in nature and can be ignored. The output signal was stable, without the drop in V_{OH} that was observed for the TPGDA inverter. However, the output swing, ΔV_{OUT}, is less than half the input voltage swing, V_{IN}. ΔV_{OUT} in (a) is 19.3 V, and in (b) it is 17.7 V. Also there was a slight drift in V_{OH} while V_{IN} was held low.

Figures 7.12 (a) and (b) give expanded views of the time response for Figures 7.11 (a) and (b) respectively. It is clear from Figure 7.12 that the rise and fall times are different. Figure 7.12 (a) shows a rise time of ~275 µs, and a fall time of ~75 µs, giving a total delay time of ~350 µs. Figure 7.10 (b) shows a rise time of 250 µs, and a fall time of ~72 µs, and has a total delay time of ~322 µs.

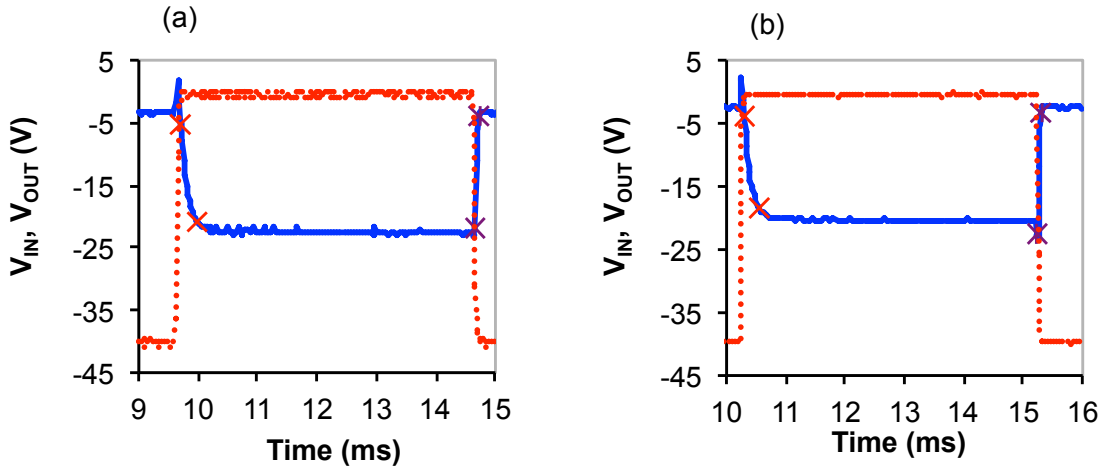

Figure 7.12 Time response (blue) of the inverters to an input signal (red) at a frequency of 100 Hz. The rise time, t_r is measured between the red crossess, and the fall time, t_f, is measure between the purple crosses. Conductance ratios of driver to load transistors are (a) 8:1 and (b) 10:1.

The rise time suggests that the inverters should be able to respond to signal frequencies in excess of 1 KHz. This is confirmed in Figure 7.13 where the time response of the same inverters to an input signal of 1 KHz (V_{DD} = -40 V) are shown.

At this higher frequency ΔV_{OUT} is reduced to 17 .8 V for inverter (a) and to 16.0 V for inverter (b). For both inverters the magnitude of ΔV_{OUT} remained constant for each switching event.

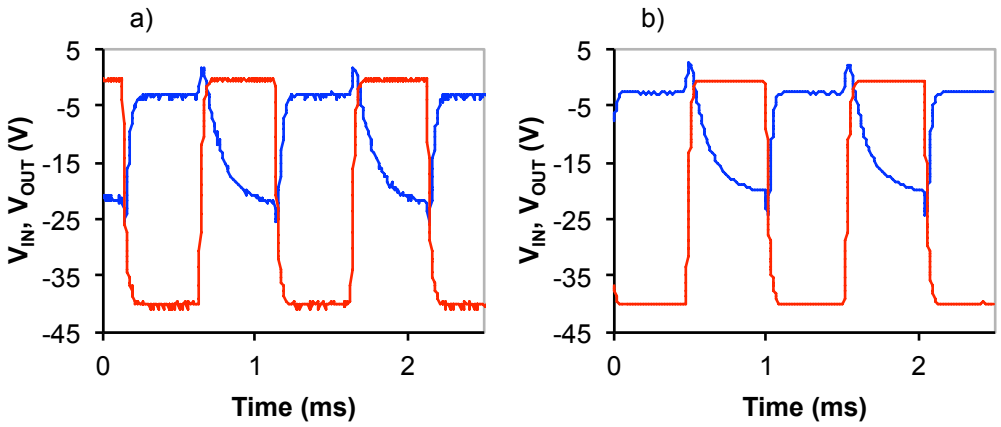

Figure 7.13 Square wave response (blue) of inverters with two different conductance ratios to a 1 KHz input signal (red) at V_{DD} = 40 V. Conductance ratios of driver to load transistors are (a) 8:1 and (b) 10:1.

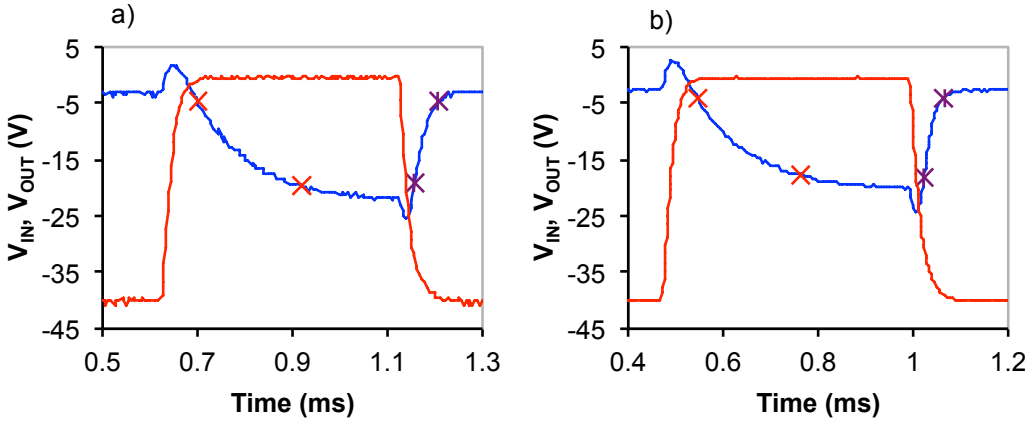

Figure 7.14 Time response (ble) of the inverters to an input signal (red) at a frequency of 1 KHz. The rise time, t_r is measured between the red crossess, and the fall time, t_f, is measure between the purple crosses. Conductance ratios of driver to load transistors are (a) 8:1 and (b) 10:1.

The rise and fall time of inverters (a) and (b) in response to a 1 KHz signal were deduced from the expanded plots in Figure 7.14. The rise time, t_r, for (a) is ~258 µs, and the fall time, t_f, is ~50 µs. The t_r and t_f for inverter (b) are ~250 µs and ~41 µs respectively. One thing that may affect the result here is the rise and fall time of the input signal. It is clearly evident at this time scale that the input signal does not switch immediately from high to low and that there is a slight time delay involved adding to the overall response time of the inverter.

7.3.2 Discussion

The inverter was shown to work well, with very little hysteresis and good gain for each of the rail voltages. However, ΔV_{OUT} is particularly low, less than 50% of V_{IN} at V_{DD} = -60 V and -40 V. V_{TR} is more positive than the ideal for each rail voltage ($V_{DD}/2$) showing asymmetry in device performance. The asymmetry is also reflected in the noise margins. NM_L is a concern here being less than 2 V. This becomes a problem when connecting two inverters together, where the output of the first circuit becomes the input signal of the second circuit. The minimum V_{OUT} is the low input voltage (V_{IL}) for the next stage. As NM_L is measured to be less than 2 V for each rail voltage this means that an increase of 2 V to V_{IL} will cause a device to become unstable. This is because the voltage would fall within the transition range of the inverter. NM_H is considerably larger than NM_L for each rail voltage, meaning that the device is more likely to be stable when the input is low.

When dynamic measurements are taken there are no signs of the device being unstable at either low or high input voltages. The dynamic measurements were undertaken to evaluate differences in inverter geometry. Inverter (a) has a conductance ratio of 8:1 (driver to load), and inverter (b) has a conductance ratio of 10:1. Inverter (a) is expected to have a faster switching speed, while inverter (b) is expected to have a larger ΔV_{OUT}. However, by fabricating inverter (b) with transistors with larger aspect ratios the loss of switching speeds appears to have been mitigated.

The inverter performances here were an obvious improvement on the TPGDA/DNTT inverter of the previous chapter. This shows the differences that having stable transistor performance makes. It also shows the ability to not only fabricate multiple working transistors, but multiple working inverters.

7.4 PS-TPGDA/DNTT Ring Oscillator

Having shown that it was possible to fabricate working inverters, the next step was to fabricate a working ring oscillator circuit that can be used for generating a clock signal in digital circuits. The key here is the high device yield and stability of the PS-TPGDA/DNTT configuration. If the device yield was low, there would be a high probability of one of the constituent transistors of the ring oscillators not working, causing the entire device to fail. If the individual device performance was unstable

then this would be observed in the output frequency of the ring oscillator as fluctuations in the clock frequency.

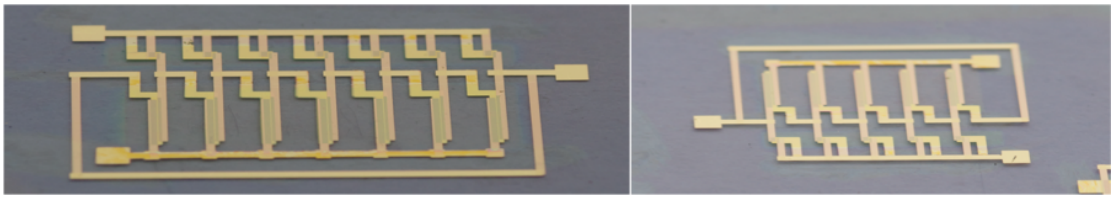

Figure 7. 15 Photographic images of the seven and five stage ring oscillator circuits.

7.4.1 Results and Discussion

Due to the success of fabricating a number of working inverters and achieving high yield of devices a new mask set was designed (Mask Set 5, Figure 3.9) to fabricate integrated ring oscillators and SR gates.

Vias were patterned in the TPGDA using a shadow mask to define the deposition pattern. To make vias in the PS layer it was necessary to use a toluene soaked cocktail stick to remove the PS layer from the contacts before the final metallisation layer. The first integrated ring oscillator successfully fabricated and tested was a seven-stage ring oscillator, consisting of 14 transistors.

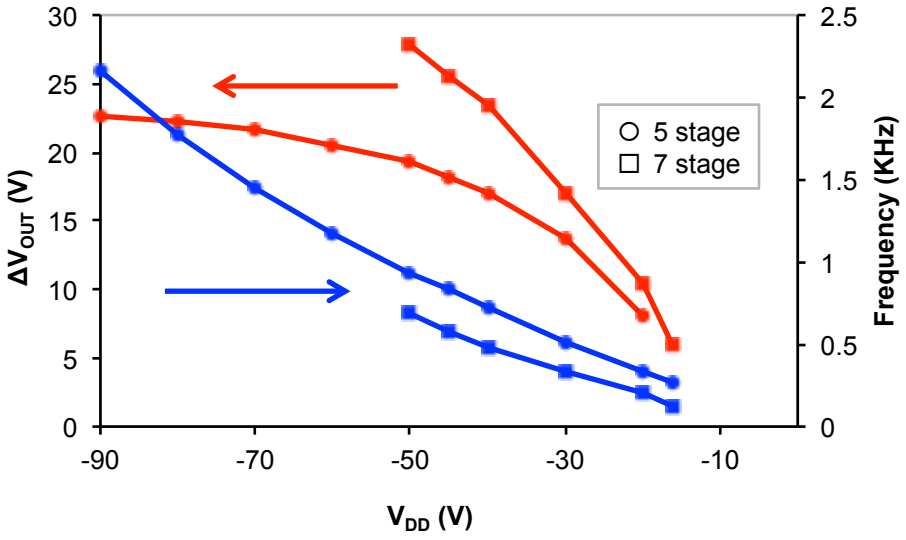

Figure 7.16 ΔV_{OUT} (red) of a seven stage (square points) and five stage ring oscillator (circle points) are shown together with the output frequency (blue) at various rail voltages.

The first measurements were conducted ~ 21 hours after fabrication and removal from the N_2 glove box. The output frequency and ΔV_{OUT} were measured on an oscilloscope

via a buffer amplifier. Figure 7.16 shows the output frequency and ΔV_{OUT} vs V_{DD} for the seven-stage ring oscillator (shown with circular points) in blue and red respectively.

The seven-stage ring oscillator began to oscillate at V_{DD} = -14 V, with a frequency of 123 Hz with ΔV_{OUT} = 5.9 V. At lower V_{DD} the device performance was sporadic and unstable. Both the output frequency and ΔV_{OUT} increased non-linearly with V_{DD} up to V_{DD} = -50 V, when the output frequency reached 685 Hz with ΔV_{OUT} = 27.8 V. At V_{DD} = -60 V the buffer amplifier interfered with the output signal, the output voltage of the ring oscillator exceeding the buffer range (+30 V to -30 V). The seven stage ring oscillator gave an output frequency that was ~ twice as fast as published so far using R2R printing techniques [24], and far higher than others [15, 16, 25, 26].

Also shown in Figure 7.16 is the output frequency and ΔV_{OUT} of a five stage ring oscillator vs V_{DD} (circular data points) plotted in blue and red respectively. By the time the five-stage ring oscillator was tested, it had been stored in a petri dish under lab conditions (dark, room temperature) for one month. It showed a similar performance to the seven-stage ring oscillator. Its output frequency was slightly higher, but with a smaller ΔV_{OUT} for corresponding V_{DD} values. Also, at this point the buffer amplifier had been modified so that its voltage range was 0 to -60 V, making it possible to use more negative V_{DD} voltages, V_{DD} up to -90 V. The output frequencies of ~1.2 KHz were four times faster at V_{DD} = -60 V than the previously highest published frequency for R2R compatible techniques. As shown in Figure 7.17 at V_{DD} = -90 V, the output frequency was 2.16 KHz with ΔV_{OUT} = 22.7 V. This reduced to an output frequency of 1.18 KHz with ΔV_{OUT} = 20.5 V at V_{DD} = -60 V. The lowest V_{DD} at which the ring oscillator was stable was -16 V, having an output frequency of 269 Hz.

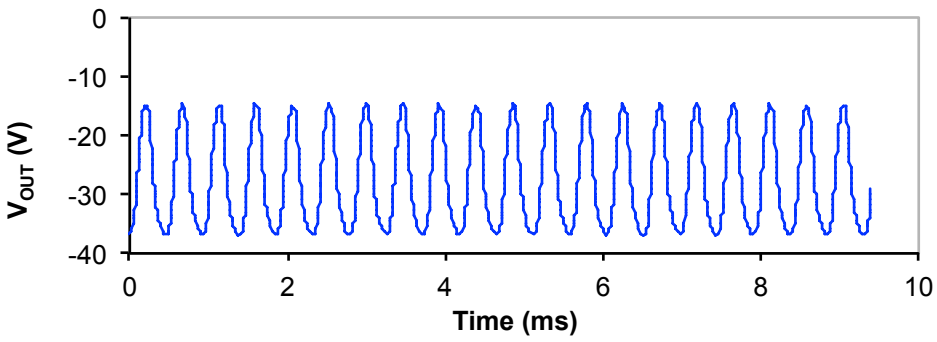

Figure 7. 17 Output frequency of the five stage ring oscillator at V_{DD} = -90 V.

As shown earlier in this chapter, the transistor performance improved over a 48 hour period, and this was also true of the seven-stage ring oscillator. Some 20 hours after the final fabrication step the ring oscillator was tested with V_{DD} = -60 V without using the buffer amplifier. The output frequency was measured to be 1.29 KHz and ΔV_{OUT} = 17.3 V. The increase in the output frequency was attributed to the device improvement over time, and the decrease in ΔV_{OUT} down to the loading effect of the oscilloscope connected directly to the output.

The following day the same ring oscillator was continuously operated at V_{DD} = -60 V for a period of eight hours, beginning from 40 hours after fabrication and removal from the N_2 glovebox. Figure 7.18 shows the output frequency and ΔV_{OUT} of the oscillator over the eight hour period.

The output frequency increased steadily up to 44 hours after fabrication, before decreasing slightly over the remaining four hours, varying from 1.29 KHz up to 1.42 KHz. However, ΔV_{OUT} decreased markedly during the first hour before stabilising, decreasing from 23.3 V at 40 hours, to 9.7 V at 48 hours.

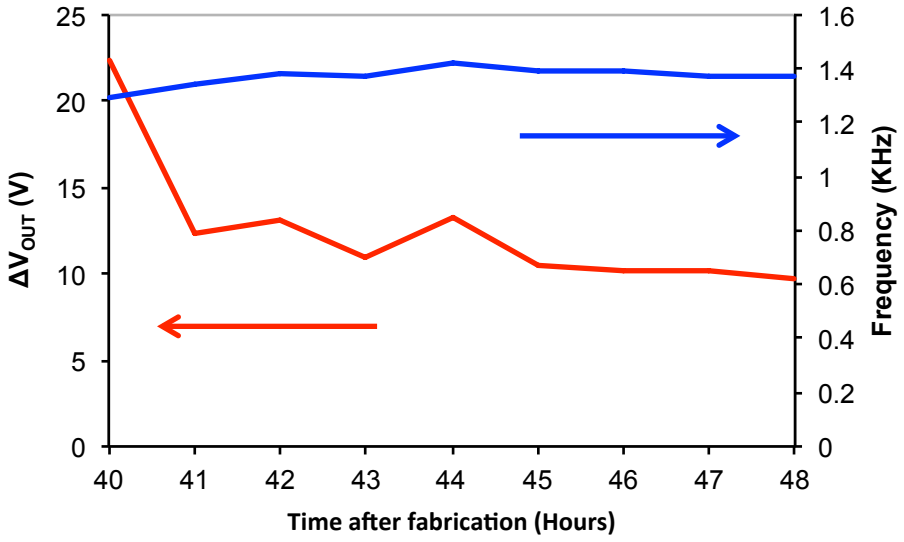

Figure 7.18 ΔV_{OUT} (red) of a seven stage ring oscillator is shown together with the output frequency (blue) over an 8 hour period of continious operation at a V_{DD} = -60 V.

For each oscillation each transistor must switch twice. Assuming the oscillation frequency of 1.3 KHz, over an eight hour period each transistor has completed a minimum of 1,248,000 switches.

The same ring oscillator was also monitored over a 31 day period (non-continuous operation) at V_{DD} = -60 V. The device was operated for an hour on each day that it was tested before the measurement was taken. (On some days the device was operated for longer periods of time, however the measurements shown were taken after the first hour of operation). Figure 7.18 shows the output frequency and ΔV_{OUT} of the seven-stage ring oscillator over the 31 day period.

Both the output frequency and ΔV_{OUT} decreased during the 31 days. However, the output frequency, after falling to ~ 0.5 KHz after ~ 500 hours, remained at that frequency for the remainder of the measurement. Although ΔV_{OUT} increased initially from 17 V to 28 V, this can be attributed to the improvement in individual transistor performance over the initial 48 hour period. ΔV_{OUT} decreased from a maximum of 28 V down to 6.2 V over the measurement period.

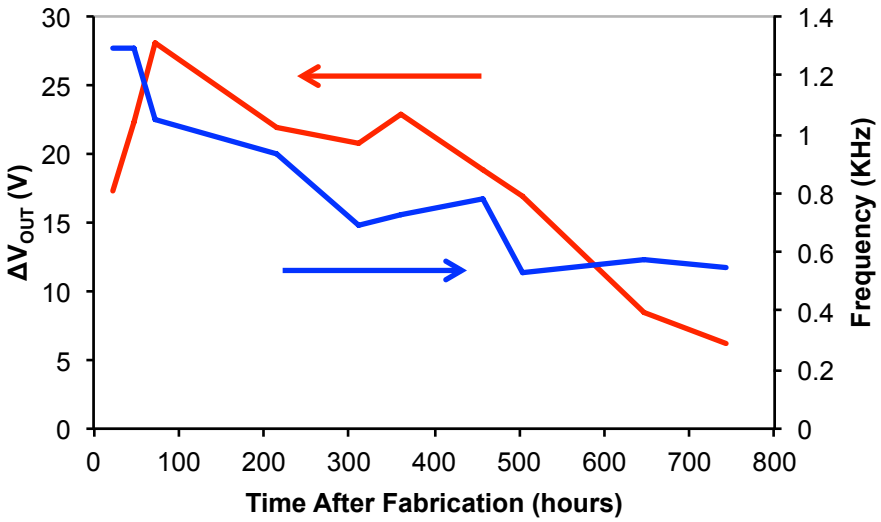

Figure 7.19 The ΔV_{OUT} (red) of a seven stage ring oscillator is shown along with the output frequency (blue) over a 30 day period.

The output frequencies of these ROs are not as high as published elsewhere for organic ROs [27], as they were fabricated using R2R compatible methods. The frequencies here are also much lower than the 80 KHz achieved by Baeg *et al*. [28] where it is claimed that the transistors are high speed printed. However, the SD contacts were patterned by photolithography, a time consuming and batch process. In addition the inkjet patterned semiconductor had to be annealed for 30 minutes in an N_2 glovebox (1 hour for PEN substrates). Also the dielectric was spin coated and annealed for 2 hours inside a N_2 glovebox. It would appear that these processes are a

long way from being applied to a true high speed printing process. Therefore, these ring oscillators appear to have the highest oscillation frequency of R2R compatible devices.

7.5 Summary

The performance of PS-TPGDA/DNTT transistors was shown to improve gradually over a 48 hour period before stabilising. After stabilising, the devices showed very little hysteresis, and little variability in devices of identical geometry. The transistors were shown to have a good mobility, > 1 cm^2/Vs, suitable for fabricating multiple transistor devices. This was enhanced further by the high device yield (>89%).

The transistors were shown to be stable even after six months in air, with good agreement between devices of identical geometry. There was no hysteresis, however, an unusual feature appeared in the linear transfer plot determined to be caused by a variation in V_T related to a bulk property of TPGDA.

As with the TPGDA transistors, PS-TPGDA transistors were shown to have a W dependent mobility. This was determined to be due to parasitic currents existing at the edges of the S and D contacts. This was confirmed by removing the conducting channel of a transistor. Upon re-measuring, a significant current still flowed between source and drain.

Inverters based on enhancement load transistors showed an asymmetrical performance with relatively poor low noise margin. The asymmetry is expected for unipolar enhancement mode devices. The switching delay for these inverters was shown to be less than 1 ms. This compared well with other R2R patterned inverters reported in the literature.

Following the successful characterisation of a number of individual inverters, integrated ROs were characterised. These were shown to have output frequencies in the low KHz range, to our knowledge, outperforming any R2R printed ROs currently published.

These are very encouraging results in terms of R2R compatible devices, being comparable or better in terms of mobility and switching speeds. Having shown that it

was possible to fabricate inverters and ring oscillators the next step was to fabricate logic gates.

7.6 References

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Chapter 8

Logic Gates

8.1 Introduction

In the previous chapter, it was shown that PS-buffered TPGDA provides the basis for a good fabrication method for the production of transistors with a high mobility of ~1 cm^2/Vs in high yields. It was also shown that these transistors can be used to fabricate inverters and multiple transistor ring oscillators. This chapter will focus on the fabrication of NAND and NOR logic gates and their application in an SR Flip-flop device. NAND and NOR gates are examples of digital logic circuits that have fewer transistors than a ring oscillator but show a progression in complexity from the inverter device. Both the NAND and NOR gates are designed to provide electronic representations of digital logic functions described by truth tables. They are the next step on from inverters and ring oscillators in realising more complex digital circuits in a R2R process. This is an important step because all logic gate functions can be implemented using only NOR or NAND gates as was shown in section 2.4.4 Figure 2.19. Successful fabrication of such gates would further strengthen the case for vacuum deposition as an alternative method to conventional printing techniques for R2R production of flexible electronics.

Here then, we apply the high-yield process for DNTT/PS-TPGDA transistors to the fabrication of NOR and NAND gates. First we look at the voltage transfer characteristics of an inverter in the NOR gate, before proceeding to investigate the dynamic switching response time of the NOR gate. We then repeat the process to evaluate the NAND gate. Finally we investigate the dynamic properties of a NAND-based SR Flip-flop.

8.2 NOR and NAND Logic Gates

8.2.1 NOR Gate Results

NOR gates were fabricated using the stable configuration of DNTT on PS-TPGDA dielectric using Mask Set 4 (Figure 3.10 (a)). For both driver OTFTs W = 2.5 mm and L = 50 μm. For the enhancement mode load OTFT W = 625 μm and L = 100 μm. The

NOR circuit is shown in Figure 8.1 (a), along with the mask pattern in (b) from Mask Set 4.

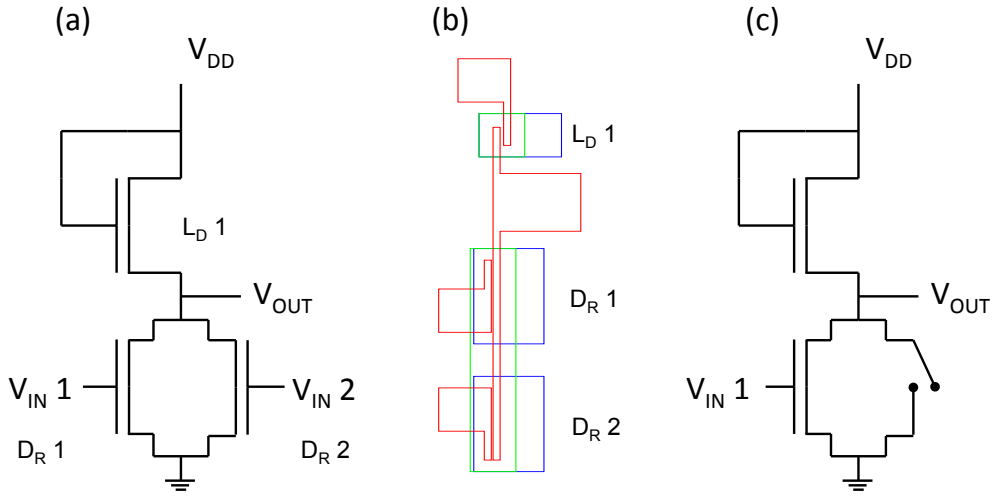

Figure 8.1 (a) Shows the NOR circuit as designed and (b) the overlaid mask patterns for the circuit. (c) Shows how the inverter voltage transfer of the NOR gate was measured.

The voltage transfer measurement was taken with driver 1 acting as the sole driver transistor, driver 2 was switched off for the duration of the measurement, similar to an open switch, as shown in Figure 8.1 (c). Figure 8.2 shows the resulting voltage transfer response of the inverter as V_{IN} is swept from 10 V to -60 V.

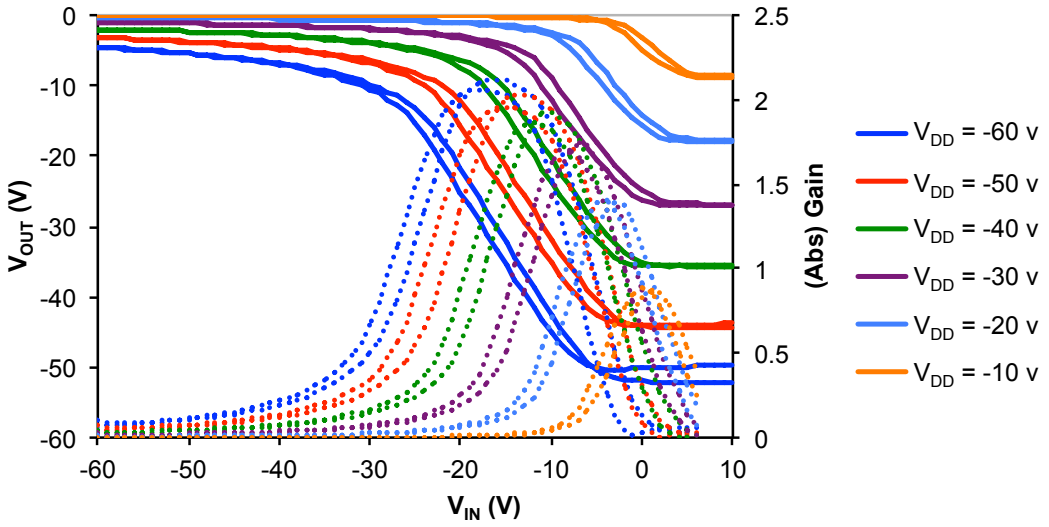

Figure 8.2 The voltage transfer characteristics of a NOR inverter at various rail voltages V_{DD} together with the corresponding gain shown as a dashed plots.

When V_{IN} = 10 V, the driver transistor (dr1) is off and the output is high, V_{OUT} at V_{IN} = 0 V is taken as V_{OH}. As V_{IN} becomes progressively more negative dr1 switches on and

begins to conduct and V_{OUT} begins to drop, entering the steep transition region. On exiting the transition region the plots become relatively flat again, corresponding to the driver transistor being fully on. The difference between the minimum and maximum of the output voltage in response to an input voltage that is swept from +10 V to -60 V shown in Figure 8.2 is larger than the ΔV_{OUT} quoted in table 8.1.

In table 8.1 ΔV_{OUT} has been calculated as the difference between V_{OH} when V_{IN} = 0 V and V_{OL} when $V_{IN} = V_{DD}$ as this better reflects the switching between V_{IL} and V_{IH} of an inverter. This was also done when calculating the noise margins. So, for the rail voltages where V_{DD} < -60 V, the ΔV_{OUT} is smaller than shown in the voltage transfer measurement.

Table 8.1 A table summarising some of the key properties of the NOR inverter.

V_{DD} (V)	N_{ML} (V)	N_{MH} (V)	Gain	V_{TR} (V)	ΔV_{OUT} (V)
-60	3.5	24.0	2.12	-21.75	48.70
-50	2.2	19.0	2.03	-18.50	40.8
-40	1.1	15.7	1.92	-14.50	32.7
-30	0	13.1	1.74	-10.50	23.0
-20	0	7.8	1.41	-7.50	12.8
-10	-	-	0.87	-2.25	4.5

The points of the slope of V_{OUT} that are > 1 are within the transition region of the inverter and are not stable. As the load transistor current saturates the transfer enters another flat region where the gain is low, V_{OUT} at $V_{IN} = V_{DD}$ is taken as V_{OL}. All plots are asymmetric when considering V_{IL} = 0 V and $V_{IH} = V_{DD}$ for each plot. This is emphasised by the fact that V_{TR} for each plot is more positive than $V_{DD}/2$, (ideally $V_{TR} = V_{DD}/2$). The asymmetry is easy to see in the noise margins for each rail voltage (shown in table 8.1) where the NM_H is large for all rail voltages, and short to non-existent for NM_L. The clockwise hysteresis seen in the transition region does not appear to be rail voltage dependent as each plot displays the same degree of hysteresis. The hysteresis probably arises from a slow shift in V_T during the measurement due to stress on the two transistors. As the rail voltage becomes more negative the gain increases as the transition region of each plot becomes steeper. For rail voltages V_{DD} ranging from -20 V to -60 V the gain exceeds 1 (summarised in table 8.1), peaking at 2.1 at V_{DD} = -60 V.

Preliminary dynamic inverter measurements were taken by switching $V_{IN}1$ as $V_{IN}2$ was grounded (V_{IL}), and with $V_{IN}2$ held at -60 V (V_{IH}) using the Keithley 4200 SCS as the input signal source. When considering Figure 8.1 (c), this is equivalent to stepping $V_{IN}1$ between 0 V and -60 V when the switch is open, and repeating the step with the switch closed. The NOR gate response is shown in Figure 8.3

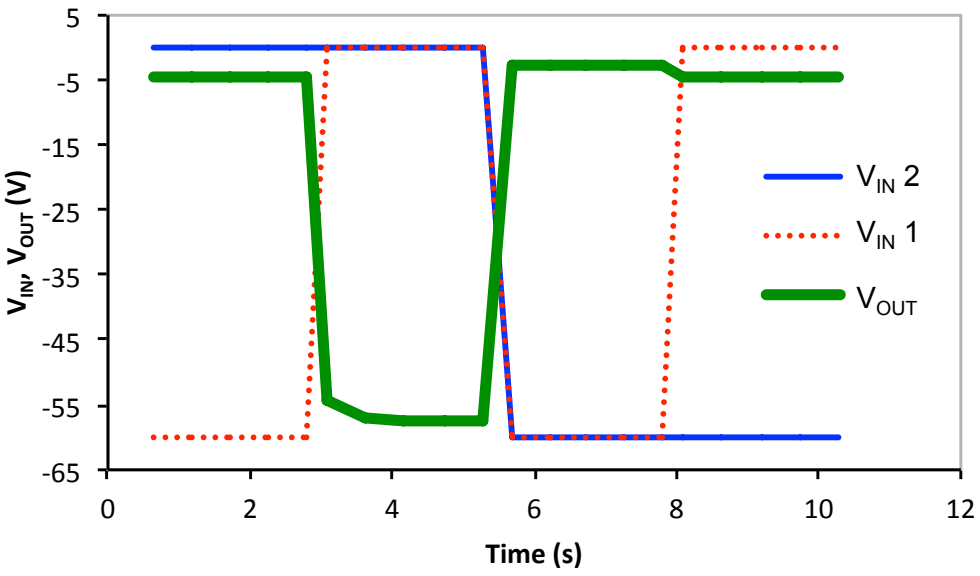

Figure 8.3 Output response (V_{OUT}, green) of a NOR gate to two input signals $V_{IN}1$ (red) and $V_{IN}2$ (blue)

The result shows a good NOR gate response corresponding to the NOR truth table (Figure 2.18 (d)) in Chapter 2. When $V_{IN}1$ is high (red line) and $V_{IN}2$ is low (blue line) V_{OUT} = -4.7 V (low). When $V_{IN}1$ switches to low, both inputs are now low and V_{OUT} switches to -57.6 V (high). $V_{IN}2$ was then held at -60 V and the switch in $V_{IN}1$ was repeated. When both inputs are high V_{OUT} goes to -2.6 V (low). When $V_{IN}1$ subsequently switches to low there is a minor rise in V_{OUT} to -4.4 V however it still remains low. There is a good voltage swing of 52.9 V for the rise, and a larger swing of 55 V for the fall. However, this could be reversed depending on the order of the switching of V_{IN}.

The response time of the Keithley SCS 4200 was not fast enough to determine the true switching speed of the NOR gate, and was only suitable for seeing if the device responded according to the relevant truth table. It was also only possible to supply one input signal, meaning a new set up was required to provide two input signals and a better response time.

The dynamic square wave response of the NOR gate was then measured using the Agilent DS0-X-2014A and buffer amplifier, the two input signals supplied from a TTi TGA 1242 waveform generator through an amplifier (Falco Systems DC-20KHz High Voltage Amplifier WMA-01).

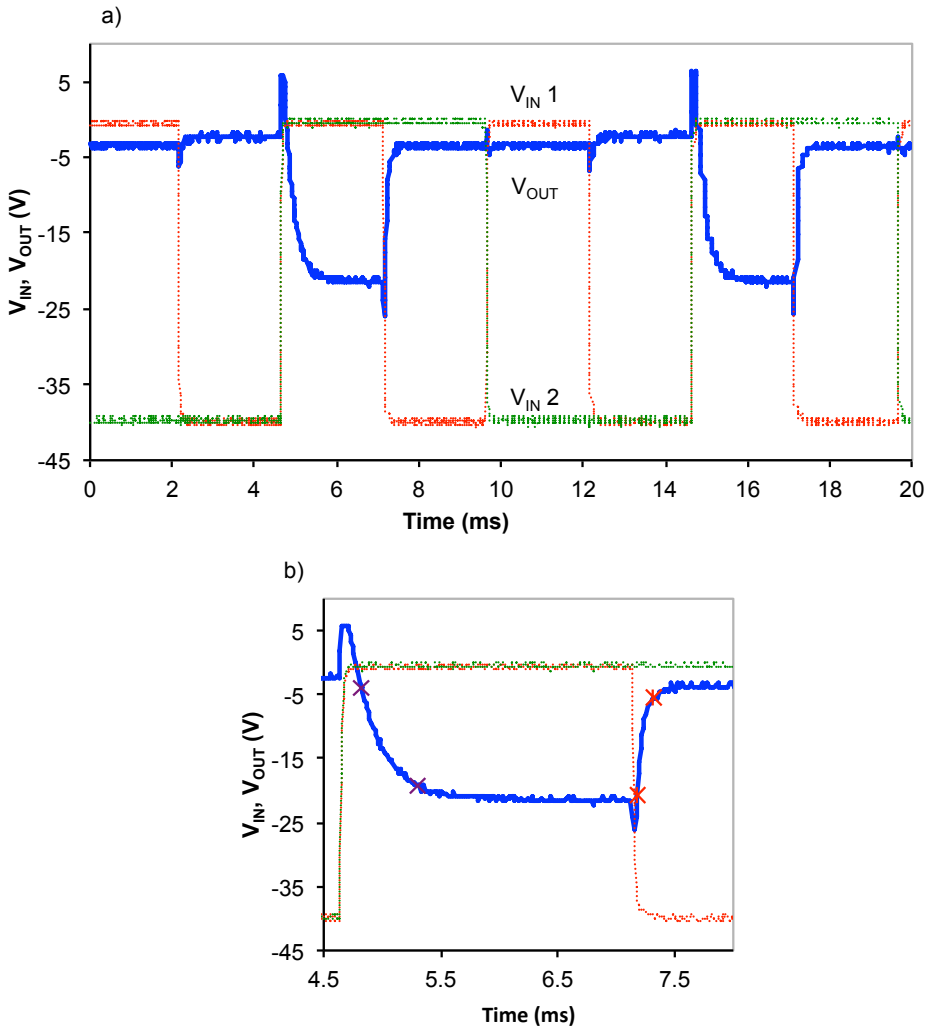

Figure 8.4 a) Output response (V_{OUT}) of a NOR gate to two input signals switching between ground and -40 V at frequencies of 200 Hz (red line) and 100 Hz (green line). b) Expanded section showing the rise and fall times of the NOR switch, the crosses mark the points corresponding to 10% and 90% of the voltage swing of V_{OUT}.

Shown in Figure 8.4 is the dynamic output response (V_{OUT}) of NOR logic gate NOR1 to two square wave input signals, $V_{IN}2$ at 100 Hz and $V_{IN}1$ at 200 Hz, switching from 0 V to -40 V and with V_{DD} = -40 V. The observed spikes are capacitive breakthrough and can be ignored. Vo_H for this device is -20.9 V, i.e. when V_{OUT} is at its maximum negative voltage. Vo_L has two values ~ -2.3 V when both $V_{IN}1$ and $V_{IN}2$ are high and ~

-3.9 V when either $V_{IN}1$ or $V_{IN}2$ is high and correspond to when V_{OUT} is at a minimum negative value. The output voltage swing, ΔV_{OUT}, between V_{OL} and V_{OH} is 18.6 V. From V_{OH} to V_{OL}, ΔV_{OUT} is 17 V. In both cases, this is less than half of the input voltage swing.

Figure 8.4 (b) shows a section of V_{OUT} on an expanded timescale from which it is seen that the time taken to go from low to high takes ~ 1 ms, while the reverse transition is much faster. Defining the transition times as the time taken to switch between 10% and 90% of ΔV_{OUT}, then the rise time, t_r, is ~ 480 µs, and the fall time, t_f, is ~140 µs. The measurement times are marked by crosses on the signals in Figure 8.4 (b) – t_r, purple crosses; t_f, red crosses. As V_{OUT} raises the delay between $0.5\Delta V_{IN}$ and $0.5\Delta V_{OUT}$ is ~ 310 µs. The delay as V_{OUT} falls between $0.5\Delta V_{IN}$ and $0.5\Delta V_{OUT}$ is ~70 µs.

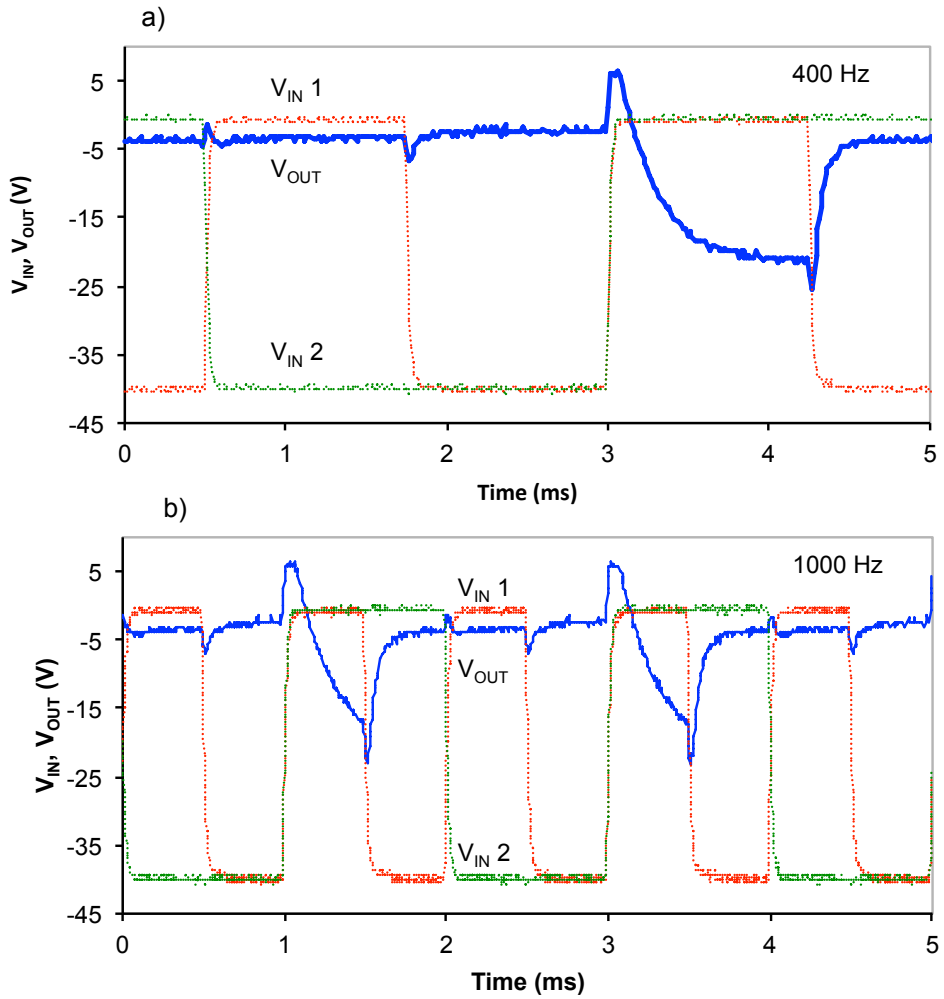

Figure 8.5 a) Shows the dynamic NOR gate response to two input signals switching at frequencies of 400 Hz (red line) and 200 Hz (green line). b) Shows the response of the same NOR gate to a higher frequency input signals of 1 KHz (red line) and 500 Hz (green line).

The responses of the NOR gate to increasingly faster input signals are shown in Figure 8.5. At 400 Hz the device still responded well, reaching a stable voltage of -20.7 V. However, at 1000 Hz the rise time is too long for the output to reach a steady state. V_{OUT} only reaches -17.4 V before it switches back to low. However, the high and low voltages are still easily distinguished.

8.2.2 NAND Gate Results

NAND gates were fabricated on the same substrate as the NOR gates. The circuit is shown in Figure 8.6 (a) and the mask layout is shown in Figure 8.6 (b). The dimensions of the driver and load OTFTs were identical to those used in the NOR gates. Initially the drain of OTFT 2 was grounded so that the response of the inverter formed by OTFT 1 and the enhancement load OTFT could be determined as shown in the circuit diagram in Figure 8.6 (c).

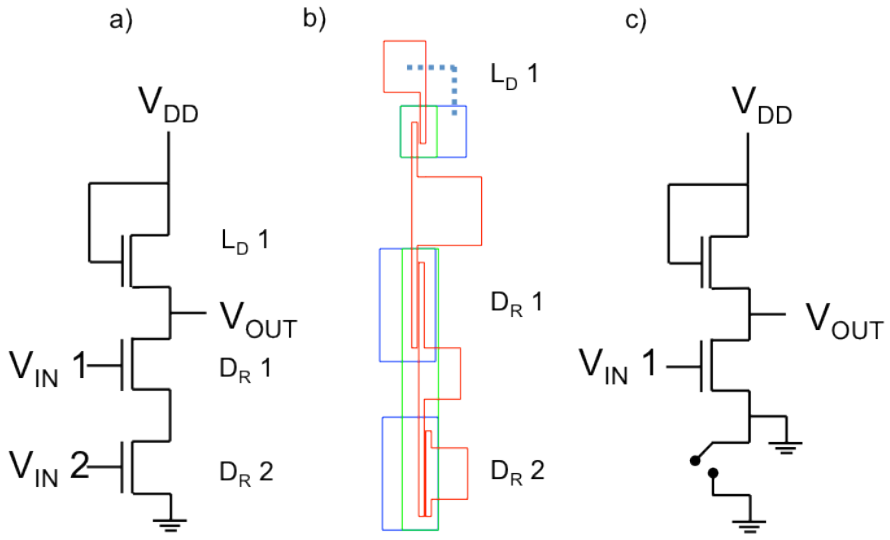

Figure 8. 6 (a) Shows the NAND circuit and (b) the overlaid mask patterns for the circuit. (c) Shows a representation of the circuit for measuring the inverter voltage transfer of the NAND gate.

The voltage transfer characteristic is shown in Figure 8.7. In this measurement $V_{IN}1$ was swept from +10 V to -60 V, and back again. The rail voltage V_{DD} was stepped from -10 V to -60 V in -10 V increments.

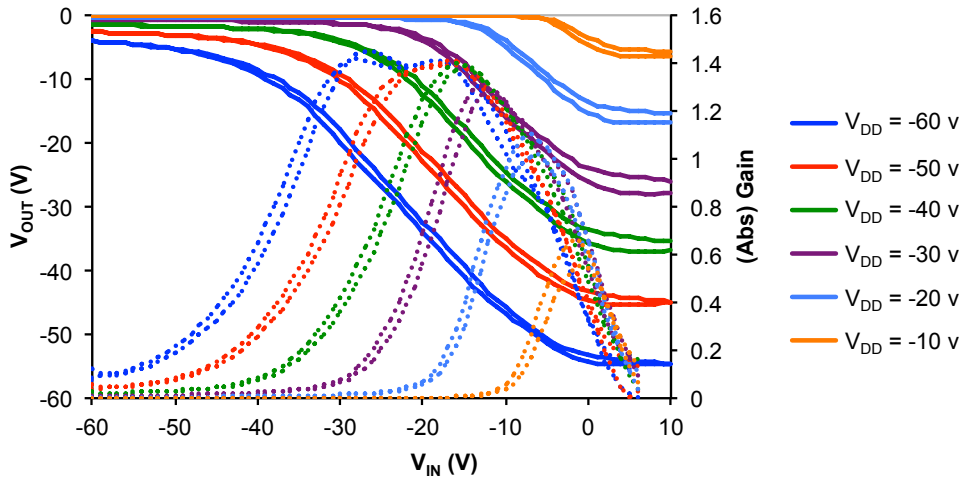

Figure 8.7 The voltage transfer characteristics of a NAND inverter at various rail voltages V_{DD} together with the corresponding gain shown as a dashed plots.

The voltage transfer plots here are closer to being symmetrical than they were for the NOR gate. This is also reflected in the noise margins shown in table 8.2, where there is a closer match between the low noise margin (NM_L) and high noise margin (NM_H) than in table 8.1. There is hysteresis between the forward and reverse sweeps in the transfer and V_{OH} region, but once again this is not rail voltage dependent.

Table 8.2 Here a number of the key properties of the NAND inverter are summarised.

V_{DD} (V)	N_{ML} (V)	N_{MH} (V)	Gain	V_{TR} (V)	ΔV_{OUT} (V)
-60	5.9	18.4	1.45	-25.75	50.5
-50	4.9	16.2	1.41	-21.25	41.6
-40	5.0	13.8	1.40	-16.75	33.4
-30	3.7	9.6	1.30	-12.5	24.7
-20	3.4	7.2	1.10	-7.6	14.6
-10	-	-	0.66	-2.5	5.1

Although $V_{TR} \neq V_{DD}/2$, it is, nevertheless, $\sim \Delta V_{OUT}/2$. The gain does not vary much, 1.4-1.45, for the rail voltages -60 V, -50 V and -40 V, but decreases to 0.66 for a rail voltage of -10 V. Of note here is the double peak of the gain at a rail voltage of -60 V, one at -28 V and the other at -17 V. For all rail voltages V_{OL} is less than -5 V. The voltage swing is calculated in the same way as for the NOR gate, and is shown for each rail voltage in table 8.2. ΔV_{OUT} is above 80% of ΔV_{IN} for rail voltages between -60 V and -30 V, but drops to 73% for a V_{DD} = -20 V and to 51% for V_{DD} = -10 V. With the

drain of driver 2 still grounded, preliminary measurements were undertaken using the Keithly 4200 SCS, the results are shown in Figure 8.8.

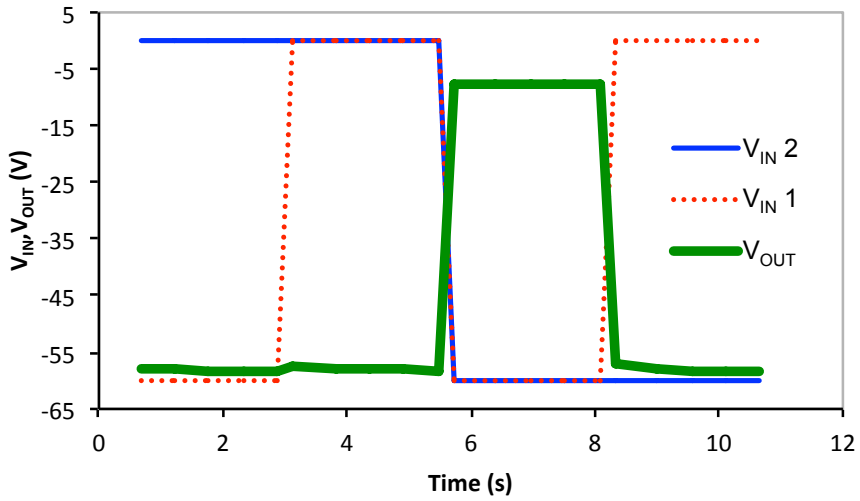

Figure 8.8 Output response (V_{OUT}, green) of a NAND gate to two input signals $V_{IN}1$ (red) and $V_{IN}2$ (blue)

As for the NOR gate, $V_{IN}1$ was switched with driver 2 initially off, and then with driver 2 on. The circuit is shown in Figure 8.6 (c), when driver 2 is off (on) the switch can be considered to be open (closed).

The preliminary measurement of the NAND gate showed a good NAND response that corresponds with the truth table in section 2.4.4 of Chapter 2 (Figure 2.18 (b)). Initially when $V_{IN}1$ is high and $V_{IN}2$ is low, V_{OUT} is high at a value of -58.2 V. As $V_{IN}1$ switches to low it pulls down V_{OUT} a small amount but V_{OUT} recovers to back to -58.2 V when both inputs are low. When both inputs switch to high, V_{OUT} becomes low at a value of -7.7 V. As $V_{IN}1$ switches back to high, so does V_{OUT} to a value of -58.5 V. The voltage swing is 50.5 V for the fall, and a swing of 50.8 V for the rise.

As for the NOR gate previously, to determine the response speed of the circuit higher frequency input square waves were used and the output signal measured on an Agilent DSO-X-2014A connected to the output of the NAND via a buffer amplifier.

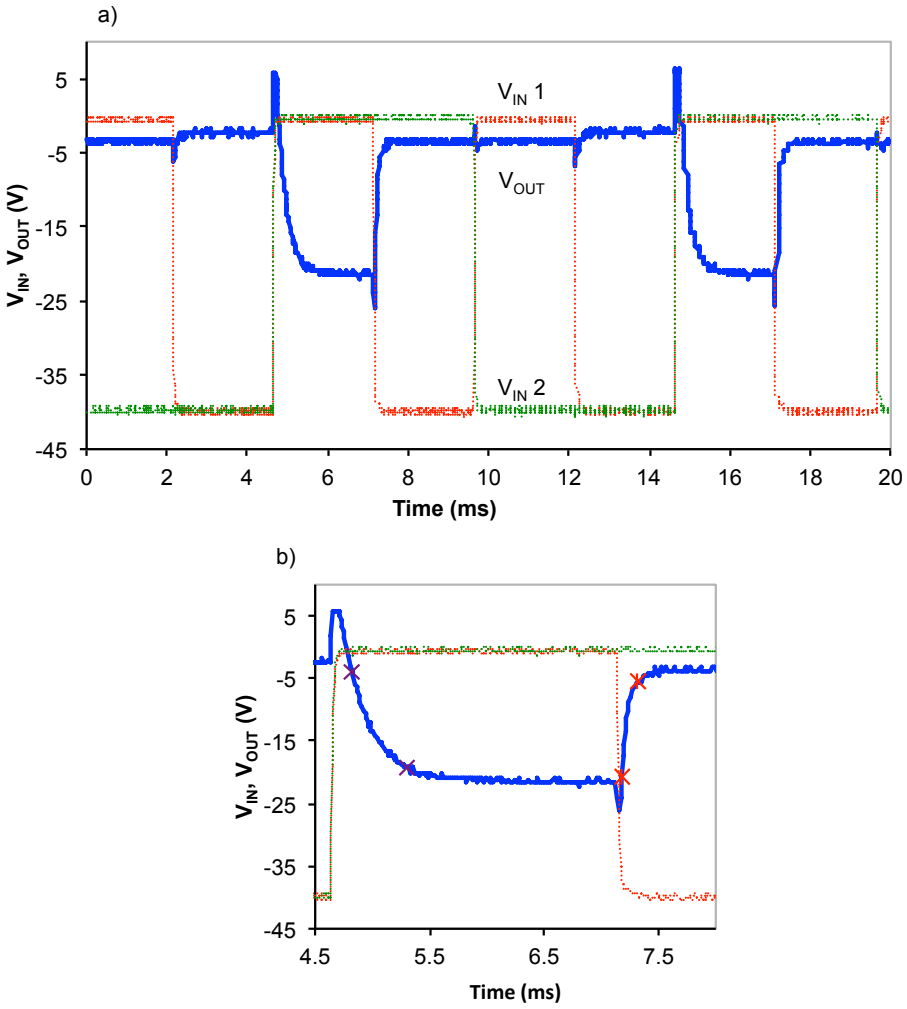

Figure 8.9 a) Output response (V_{OUT}) of a NAND gate to two input signals switching between ground and -40 V at frequencies of 200 Hz (red line) and 100 Hz (green line). b) Expanded section showing the rise and fall times of the NAND switch, the crosses mark the points corresponding to 10% and 90% of the voltage swing of V_{OUT}.

Shown in Figure 8.9 (a) is the output response, V_{OUT}, of the NAND logic gate NAND1 to two input signals, one at 100 Hz and the other at 200 Hz, switching from 0 V to -40 V. Again the observed spikes are capacitive breakthrough and can be ignored.

Initially $V_{IN}1$ is 0 V and V_{IN} 2 is 0 V, V_{OUT} is at a stable voltage of -21.6 V, corresponding to V_{OH}. When V_{IN} 1 switches to -40, V_{OUT} remains at -21.6 V maintaining the output at V_{OH}. As V_{IN} 1 switches to 0 V and V_{IN} 2 switches to -40 V V_{OUT} does spike and drop a little but recovers and remains stable at -21.6 V. Only when both inputs are high at -40 V is V_{OUT} low at -5.5 V. This gives a ΔV_{OUT} of 16.1 V.

Figure 8.9 (b) is an expansion of the switch on and switch off sections of the output of APS4_NAND1. t_f is estimated to be ~150 µs, and t_r is estimated to be ~300 µs. As V_{OUT} falls the propagation delay between $0.5\Delta V_{IN}$ and $0.5\Delta V_{OUT}$ is ~ 235 µs. Similarly as V_{OUT} rises the propagation delay between $0.5\Delta V_{IN}$ and $0.5\Delta V_{OUT}$ is ~73 µs.

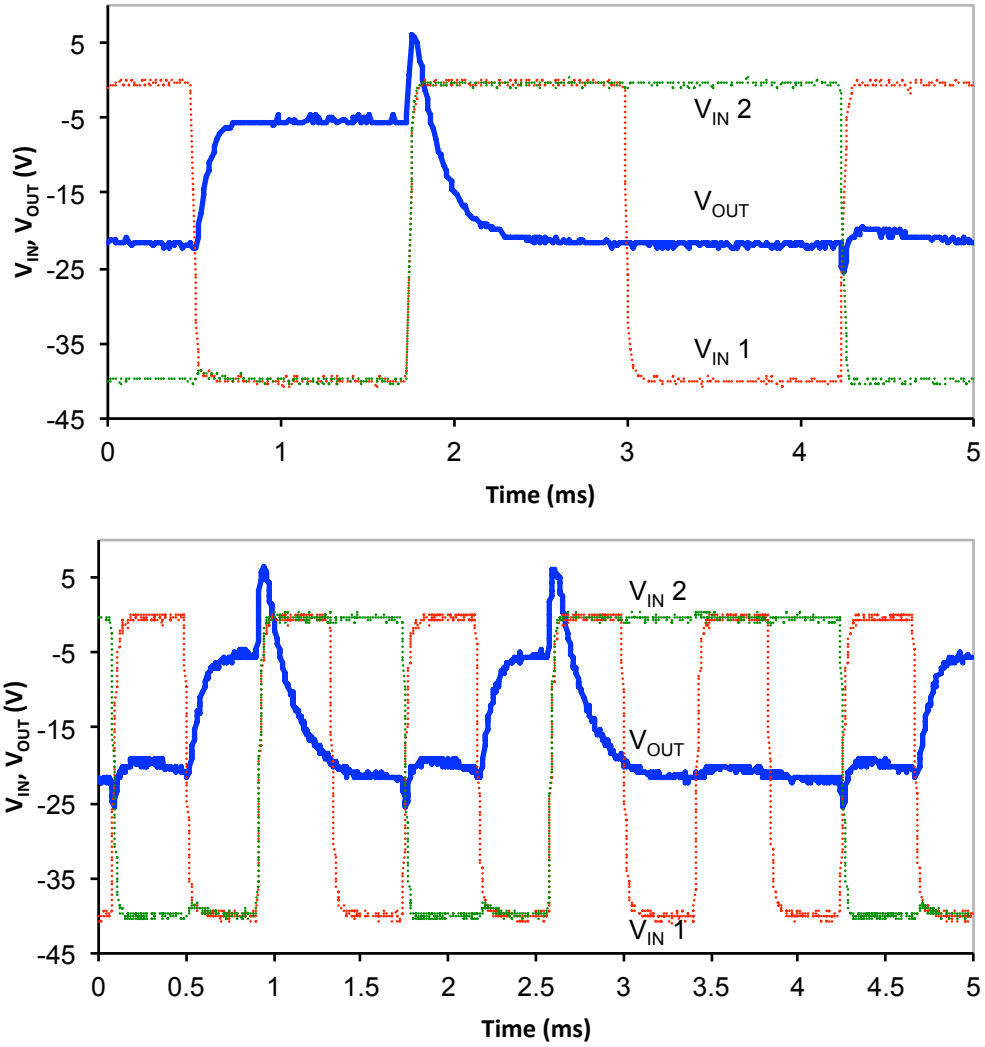

Figure 8.10 a) Shows the dynamic NAND gate response to two input signals switching at frequencies of 400 Hz (red line) and 200 Hz (green line). b) Shows the response of the same NAND gate to a higher frequency input signals of 1200 KHz (red line) and 500 Hz (green line).

Figure 8.10 shows the NAND response at higher signal frequencies, namely, 400 Hz and 1200 Hz. At 400 Hz the NAND reaches a high of -21.6 V, the same high value as when the signal was 200 Hz. At 1200 Hz the NAND reaches a high of -21.6 V once

again. However, it only reaches -19.3 V at the point that $V_{IN}1$ switches back to high from where both inputs are low, in the same state at 400 Hz it reached -21.6 V.

8.2.3 Discussion

To date, 20 NOR gates and 21 NAND gates out of a possible 62 have been tested and all worked successfully as expected from the high transistor yield reported in Chapter 7.

When connected as simple two-transistor inverters both the NOR and the NAND structures showed very similar behaviour (Figures 8.2 and 8.7). This is expected since transistor dimensions were the same in both cases. Both show a good ΔV_{OUT} in excess of 80% of ΔV_{IN} (where $\Delta V_{IN} = V_{DD}$ to 0 V).

However, there are also differences in the device performance. The gain in Figure 8.2 peaks at 2.12 for a rail voltage of -60 V, while in Figure 8.7 the maximum gain at the corresponding rail voltage is 1.45. The same is seen when comparing each rail voltage in tables 8.1 and 8.2. The gain is higher for the NOR inverter. This is a result of the transition region being shorter and sharper in the NOR inverter than in the NAND inverter. However, the NAND transistor has a more symmetrical transfer plot than that of the NOR transistor, this has a bearing on the high and low noise margins. The NM_L is a particular concern for the NOR inverter, as this would suggest that the device may become unstable when V_{IN} is high, particularly where V_{IN} is the output of a preceding inverter. The noise margins of the NAND transistor exceed 10% of the V_{DD} for both the high and low margins, and would therefore be expected to be stable. Both plots have similarities to the plot observed by Hambsch *et al*. [1] for a diode-type inverters in enhancement. The asymmetry they observed is similar to that seen in Figure 8.2, while the value for the gain is similar to that in Figure 8.7.

In the preliminary dynamic measurements using the Keithley 4200 SCS both logic gates showed good NOR/NAND operation with $\Delta V_{OUT} > 50$ V for $V_{IN} = -60$ V and $V_{DD} = -60$.

When the same gates were measured at higher frequencies, however, the voltage swing on the oscilloscope through a buffer amplifier was much less. Now ΔV_{OUT} was ~ 20 V for $V_{IN} = -40$ V and $V_{DD} = -40$ V. The device rise and fall times were < 1 ms and the output signal was observed to saturate and become stable. However, this is a very short

time scale compared to the measurements undertaken on the Keithley 4200 SCS, the reduced swing is probably a result of the faster measurement stressing the device much less. The load transistor is responsible for pulling the output signal to the rail voltage. Under stress the V_T for these transistors shifts positively, resulting in a higher current for the equivalent V_G. In terms of the output, this would make it appear that the load transistor has a stronger pull-up for slower measurements. This could be observed in future by slowing down the input signal from the wave function generator gradually to a frequency approaching that of the Keithley 4200 measurements.

The dip in the output voltage signal of the NAND when it is high, seen at ~14 ms in Figure 8.9 (a) and at ~4.2 ms in Figure 8.10 (a), is due to the two driver transistors being on at the same time. As $V_{IN}1$ switches to low and $V_{IN}2$ switches to high, there is a point when the input voltage for both transistors is sufficiently high to turn on both driver transistors that are in series, completing the circuit. The output signal is otherwise very stable.

The total delay time for the NOR gate was shown to be ~620 μs, for the NAND it was even shorter at ~450 μs. Unfortunately the rise and fall times are asymmetric. Balancing these values out would allow the devices to respond to a higher frequency input. They are currently limited by their rise times, 480 μs and 300 μs for the NOR and the NAND respectively. This was expected, the load capacitance associated with the buffer amplifier and connected cables, is charged by the relatively small load transistor but discharged by the larger driver transistor. This rise and fall times are significantly faster (30 x) than those achieved by Hambsch *et al.* [1]. Although total rise and fall time are not specified they are in the ms range, and were said to be similar to the times they had measured for their complimentary inverters that had a total delay time of 13.8 ms.

8.3 NAND SR Flip-flop

8.3.1 NAND SR Flip-flop Experimental Results

Having successfully fabricated the NOR and NAND gates and in a final exemplification of the fabrication process, a SR Flip-flop was fabricated and tested. A SR Flip-flop is a basic memory unit that has a set (S) and reset (R) function, and is readily fabricated from two cross-coupled NAND gates.

A NAND SR Flip-flop was fabricated using Mask Set 5 (Figure 3.11) to give the circuit seen in chapter 2, section (Figure 2.20), a photograph of which is shown in Figure 8.11. This was a fully integrated device, the vias were patterned by shadow masking the substrate during the deposition of TPGDA. There was some feathering of the TPGDA underneath the shadow mask, but sufficient tolerance was allowed in the design to account for this. However, as the PS layer was spin-coated this covered the entire substrate, consequently, it was necessary to create vias using toluene-soaked cocktail sticks to remove the PS from the contacts.

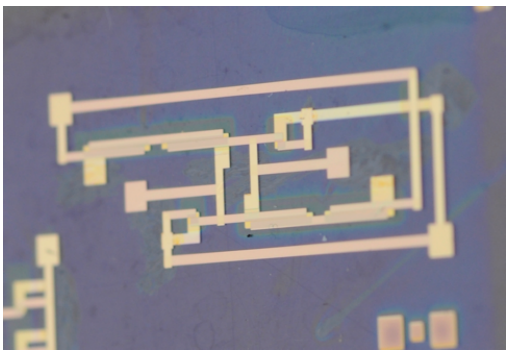

Figure 8.11 Photographic image of the NAND SR flip-flop

In the NAND-based SR flip-flop, when S and R = 0, then $Q = \bar{Q} = 1$. In this case, according to the logic this is an invalid state which can lead to the device becoming unstable and should be avoided.

As only one buffer amplifier was available only one output could be measured at a time. As one output was measured the other output was left floating. The results were then overlaid to give Figure 8.12.

(For this description the reader is referred back to Figure 2.20). We start by describing the plot of Figure 8.12 from ~10 ms, where initially both outputs are high. As 10 ms is approached R remains low and S switches to high. At this point, for NAND Y input R is low, and as it is a NAND gate, a single low input means that the output, $\bar{Q}$, must be high. For NAND X, input B = $\bar{Q}$ and is high, input S is also high, therefore the output Q must be low. At ~ 15 ms input R switches to high, and input S switches to low. As S is low, Q as the output of NAND X must be high, which now results in both inputs for NAND Y becoming high, so that $\bar{Q}$ is low. At ~ 20 ms only input S switches to high, and there is no state change. Input B = $\bar{Q}$, and $\bar{Q}$ remains low, so at least one input of NAND X is low, so that Q remains high. At ~ 25 ms both inputs become low. This is

the invalid state. It is recognised as such because it causes $Q = \bar{Q}$. This is because both NAND gates now have at least one low input that means that the output of both must be high. The cycle is then repeated.

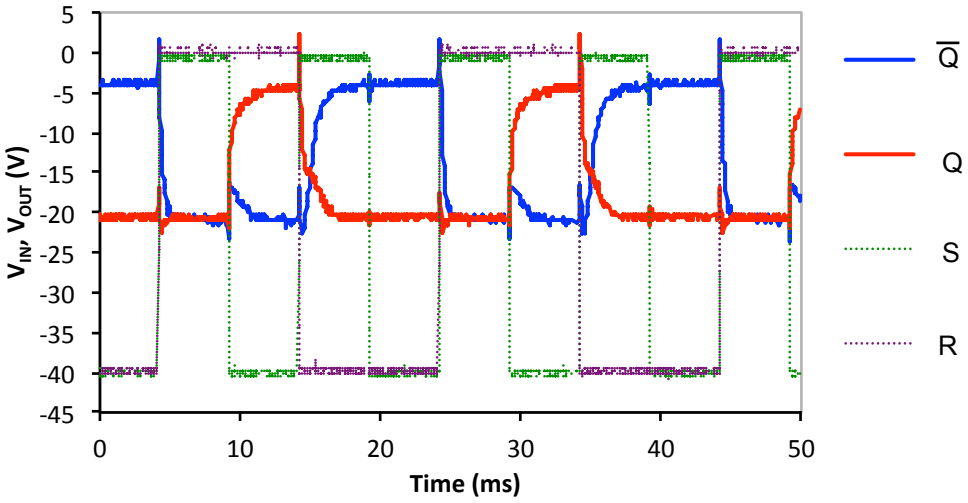

Figure 8.12 The two inputs, S (green) and R (purple), are shown with the two output signals, Q (red) and $\bar{Q}$ (blue) of the SR flip-flop against time.

It can be seen from Figure 8.12 that the two outputs obey the truth table for the NAND SR flip-flop, shown in Figure 2.2 (b). Q and $\bar{Q}$ remain opposite except for the invalid S=R state. It is also one of the most complicated devices fabricated using R2R compatible processes, and takes this work further than a number of previous studies [2]-[7], falling only behind Noh *et al.* [8][9] in the number of integrated transistors forming the circuit.

8.4 Summary

NOR and NAND logic gates were fabricated using DNTT semiconductor on a PS/TPGDA dielectric with a bottom-gate top-contact configuration. The static voltage transfer characterised was measured for inverters from both types of gate and showed a good V_{OUT} swing. Subsequently the dynamic square wave response of each gate was then measured at different frequencies. Both the NOR and the NAND gates showed a reduced V_{OUT} swing at high speeds, both being less than 25 V for rail voltages V_{DD} = -40 V. The NOR gate showed a good response at input frequencies of 200 Hz and 400 Hz. At an input frequency of 1000 Hz, the NOR response was not fast enough to fully switch the input to the maximum high. The NOR t_r was ~480 µs, and t_f was 140 µs. The NAND gate also showed a good response at input signal frequencies of 200 Hz

and 400 Hz. In contrast to the NOR gate the NAND showed a good response at an input frequency of 1200 Hz. This showed that the NOR and NAND gates were responding faster than previously published R2R compatible logic gates.

A NAND SR flip-flop was fabricated using the same bottom-gate-top-contact configuration. The dynamic properties were assessed by applying two square wave inputs to the S and R contacts and measuring the two output signals sequentially at Q and $\bar{Q}$. The two outputs showed the expected response, fitting the corresponding NAND SR flip-flop truth table.

The NAND SR flip-flop is so far the most complex device fabricated and successfully tested using R2R compatible vacuum evaporation techniques. This holds promise in developing the process towards complete circuit production.

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Chapter 9

Conclusions And Further Work

9.1 Conclusions

The aim of this thesis was to demonstrate the suitability of vacuum deposition as a method for the roll-to-roll (R2R) printing of electronic devices.

Initial work was undertaken to determine which method of purifying DNTT gave the best transistor results. Transistors were fabricated on Si/SiO_2 substrates using recrystallized, sublimated, and sublimated recrystallized DNTT semiconductor samples. The transistor performance was evaluated by comparing the transfer and output characteristics of the three samples. It was shown that the recrystallized DNTT yielded higher mobilities on average than the other two samples, up to 1.15 cm^2/Vs, although there was a larger spread in the extracted mobilities. It was therefore decided to proceed with using the recrystallized DNTT for the remaining organic thin film transistor (OTFT) devices.

Work was undertaken to assess the best approach to device configuration by fabricating top gate and bottom gate transistors using polystyrene as the gate dielectric. The top-gate transistors were shown to have poor mobility, typically less than 0.1 cm^2/Vs in both the linear and saturation regimes. In addition the device stability was poor, showing large hysteresis. This was determined to be due to the roughness of the DNTT/PS interface that was determined by the surface topography of DNTT. The DNTT had a root mean square (rms) surface roughness of 6.4 nm, an obvious obstruction in a conducting channel that is usually formed within ~ 5 nm of the interface. In contrast the roughness of the interface of the bottom-gate devices was dependent on the surface topography of the PS layer that was shown to have an rms roughness of 0.69 nm. The bottom gate devices also showed much higher mobility. The average of the extracted maximum linear mobility was 1.01 cm^2/Vs, and the average of the extracted maximum saturation mobility was 0.97 cm^2/Vs. However, although the configuration was shown to give a high mobility transistor with good stability the device yield was low <66%. This was due to pinholes that are a common problem in solution-processed dielectrics.

Based on the findings of the previous two chapters, the all-evaporated, BGTC transistors were fabricated using TPGDA as the dielectric and recrystallised DNTT as the semiconductor. The extracted maximum saturation mobility showed a strong dependence on the channel width and on average, ~ 0.4 cm^2/Vs, was less than half the mobility extracted from the PS dielectric transistors. The low mobility is due to the polar nature of the TPGDA which has previously been shown to reduce mobility due to its effect on the DNTT crystal structure. The instability in the performance of the TPGDA transistors was shown to be due to the presence of water and oxygen at the dielectric/semiconductor interface. However, the transistor yield was much higher at ~89% an important factor for the fabrication of integrated circuits. This is because the failure of a single transistor to function results in the failure of the entire circuit. It was determined that if the surface could be modified so that the influence of TPGDA polar groups and water/oxygen contaminants could be reduced, the device performance would be improved and device yield kept high.

The surface of the TPGDA was modified by a PS buffer layer. This combined the hydrophobic surface of the PS with the pinhole free bulk of TPGDA. Although some channel width dependence was still evident from the extracted mobility; the dependence was significantly reduced compared with the stand-alone TPGDA dielectric. The PS-TPGDA/DNTT transistors also showed high mobility, the average of the extracted maximum mobility in saturation was 1.51 cm^2/Vs for 81 transistors. This was over twice the highest mobility previously obtained in literature for R2R compatible transistors. Not only did the transistors show good mobility, they also demonstrated stable operation with negligible hysteresis. The yield for the devices was also impressive, ~90%. The transistors that did not work failed due to defects in the substrate impairing the patterning of the transistors, not due to the failure of the deposited materials.

After six months in air nine transistors of identical geometry showed near identical device performance with no measurement hysteresis. This showed that organic devices can be kept in air and maintain good device operation over a number of months even without encapsulation Device operation was also shown to be stable over twenty cycles in the saturation regime. However, in the linear regime there was an anomaly that became progressively more apparent with each cycle.

The PS-TPGDA/DNTT configuration was used to fabricate inverters with two

different driver-to-load conductance ratios, 10:1 and 8:1. By increasing the size of the load inverter in the 10:1 ratio inverter it was shown that switching speed was not reduced due to the increased power of the load transistor. Both inverters responded to square wave input signals with frequencies up to and exceeding 1 KHz, the total switching time being less than 0.5 ms. The output voltage swing, ΔV_{OUT}, was stable, with no reduction or shift over time. This showed that the process could be used to fabricate working logic gates with an enhancement mode load.

Following the successfully fabrication of inverters, 5- and 7-stage ring oscillators (RO) were fabricated and tested. Both ROs were shown to begin to operate at ~ V_{DD} = -16 V. Both ring oscillators were shown to have output frequencies in excess of 1 KHz. This was higher than previously published output frequencies for R2R compatible ROs. In the case of the five-stage RO, it was shown to have a maximum output frequency of 2.16 KHz at V_{DD} = -90 V. Also, they are the first ROs to be fabricated using vacuum deposition methods for both the semiconductor and the dielectric. This was even more significant as the RO had been stored under lab conditions in the dark for over month prior to testing. The seven-stage RO was demonstrated to operate with a relatively stable output frequency over an eight hour period. However, there was a significant drop in ΔV_{OUT} (~50 %) in the same time period. The output frequency of the seven-stage RO was also measured over one month from the time of fabrication. The output frequency was shown to reduce from ~1.2 KHz down to ~0.5 KHz, over the initial 19 days, stabilising at 0.5 KHz for the remainder of the measurement. This coincided with a significant reduction in ΔV_{OUT} from ~27 V down to ~6 V.

Functioning NOR and NAND gates were also fabricated, and shown to respond to input signals with frequencies up to 1 KHz. The outputs of the respective gates were shown to fit with the corresponding truth tables. In addition a fully integrated NAND-based SR flip-flop (six transistors) was also fabricated, and fitted its corresponding truth table showing good device operation. Such logic gates have not before been fabricated using vacuum deposition methods.

The results presented in this work demonstrate the suitability of a vacuum-based approach for the R2R production of flexible electronics. This was demonstrated not only in the performance of the newly fabricated transistors but also in the performance of the transistors and devices over a significant time period. Although

not an entirely vacuum-based process (as the PS buffer layer was spin-coated) it does demonstrate that this is a good alternative approach in comparison to conventional solution processed printing methods.

9.2 Further Work

The results of this study open up a number of avenues for further work. The first area of interest would be to look at other buffer layers that are evaporable to replace the solution processed PS layer. This would make the process all-evaporated, making it possible to transfer the entire process to an R2R system. An example would be the thermal evaporation (at room temperature) of n-octylphosphonic acid (C_8PA) as a buffer layer [1]. A drawback of this method is the requirement to anneal the C_8PA film for 210 minutes to get the best results. Another option would be to replace TPGDA completely, and opt for another evaporable dielectric. Parylene polymers can be one option, as they are already used in deposition processes for dielectrics.

Concerning materials, it would be wise to look at other semiconductors, and observe how the performance compares to DNTT. One good candidate would be C_{10}-DNTT, as it has previously been shown to have a higher mobility than the non-functionalised DNTT. As it has the same structure as DNTT, it has the same resistance to oxidation. It also has two aryl branches extending from the ends of the molecule which aid the alignment of the molecules within the crystal structure which is believed to be the reason for the improved mobility. It can also be evaporated like conventional DNTT.

Another option would be to investigate N-type semiconductors. If a high yield of good mobility N-type transistors could be fabricated in the same way as for DNTT, the same steps could be used to develop complementary inverters. Although it would be an additional printing step, complementary inverters have been shown previously to have a higher gain and faster switching speeds.

Further work needs to be undertaken in developing circuits and improving the transistor yield as close as possible to 100%. Gradually increasing the number of components, as has already been done, here would be the best way forward. Following that next step here would be to fabricate circuits for frequency division. The final step to progress from individual devices would be to fabricate a complete circuit.

Most important of all is the ability to transfer the deposition methods to a complete R2R system from the current batch production processes. This would be a process similar to that shown in Figure 9.1. Ideally this could be done at a high throughput speed. This is also where device yield becomes most important. It would need to be consistently close to 100% so that circuit failure is kept to a minimum.

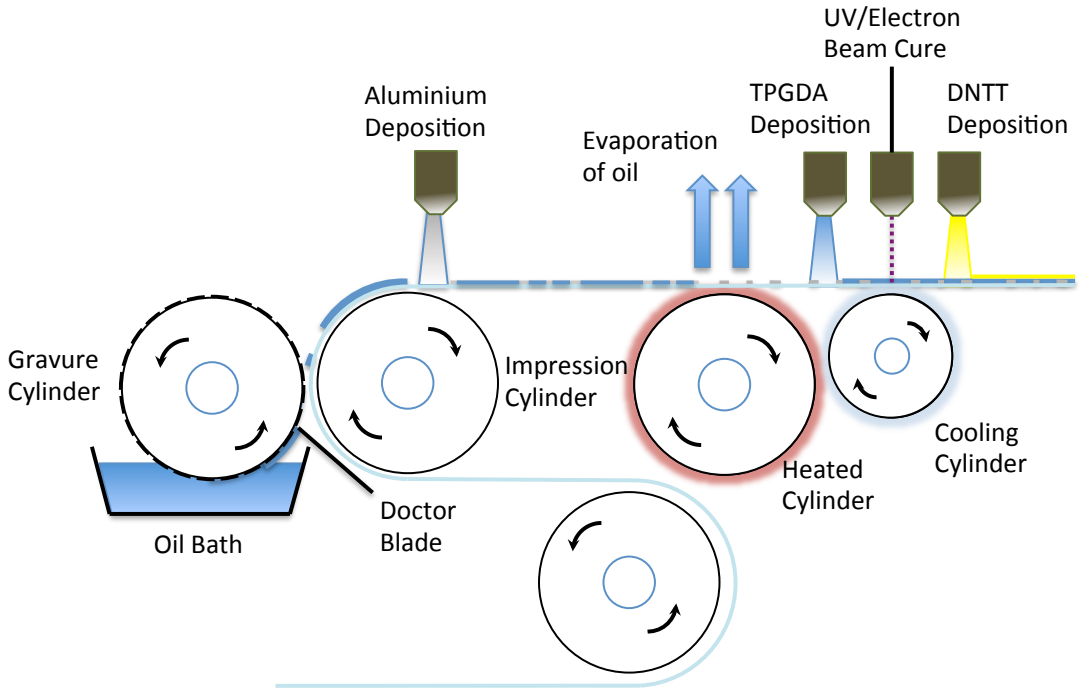

Figure 9.1 A possible process for the printing of flexible circuits

One problem that will be faced is the speed of the deposition of the semiconductor. Currently the ideal vacuum deposition of small molecules is at a rate of 0.4 Å per second. So a 50 nm thick film would take ~ 20-21 minutes to deposit. Clearly, this would be difficult to apply to a high speed R2R process. One way around this problem would be to have multiple deposition sources building up the thickness of the DNTT in sequential layers. From previous work undertaken it was found that there was no difference in transistor performance where the semiconducting layer was deposited in sequential layers compared to a layer of equal thickness deposited in a single step. An alternative process would be organic vapour jet printing, where the semiconductor is deposited in vapour form from an inert carrier gas. This has already been demonstrated by Abbas *et al*. for DNTT at a web speed of 0.02 m/min^{-1}. The first DNTT transistors fabricated using this method had a mobility of 0.5 cm^2/Vs without optimisation. Optimisation of the process could allow the fabrication of higher mobility transistors that are suitable for circuit fabrication. Although the web

speed of the OVJP process is still slow to be considered for the high speed R2R production of electronics.

As can be seen there is still much work to be done to adapt the processes to a fully R2R system, however, current work is encouraging and gives confidence to the idea that such a system would work.

9.3 References

[1] S. Gupta, H. Gleskova, "Dry growth of n-octylphosphonic acid monolayer for low-voltage organic thin-film transistors", *Organic Electronics*, **14**, 354-361, 2013

[2] G. A. Abbas, Z. Ding, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett, D. M. Taylor, "A High-Yielding Evaporation-Based Process for Organic Transistors Based on the Semiconductor DNTT" – Submitted