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Advanced study of pentacene-based organic memory structures

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Advanced Study of Pentacene-Based Organic Memory Structures

By

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in the

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School of Electronic Engineering

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Abstract

A systematic approach has been used to optimise the fabrication process of pentacene-based nonvolatile organic thin film memory transistors (OTFMTs) operating at low programming voltages. In the first part of this work, reliable, reproducible and hysteresis free organic metal-insulator-semiconductor (OMIS) devices and organic thin film transistors (OTFTs) were fabricated and characterised. All devices were based on poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP) as the organic insulators. The second part of this work focused on optimising the evaporation parameters to fabricate high-performance pentacene-based devices. About 50 *nm* thickness of pentacene film with a deposition rate of 0.03 $nm\ s^{-1}$ on ~ 300 *nm* of PMMA was found to produce large, uniform and condense grains leading to high quality devices. OTFTs with high mobility of 1.32 $cm^2\ V^{-1}\ s^{-1}$, on/off current ratio of 10^6, and negligible hysteresis and leakage current were demonstrated. The effect of the environment on the OTFTs obehaviour was also investigated. The bias stress effect was also investigated in terms of threshold voltage shift ΔV_T at various conditions and times. The results show ΔV_T increases with the increase of stress voltage. A negligible hysteresis is evident between the forward and reverse direction of the transfer characteristics and the shape of the transfer characteristics does not change with the bias stress.

Floating gate memory structures with thin layer of gold, gold nanoparticles (AuNPs) and single walled carbon nanotubes (SWCNTs) were fabricated and characterised during this investigation. Hysteresis in memory structures was a clear indication of the memory effect and charge storage in these devices. Also, the hysteresis was centred close to 0 *V* for SWCNTs-based structures, which indicate that a low operation voltage is needed to charge the devices. A memory window of about 40 *V* was observed for AuNPs-based memory devices based on PVP; while the memory windows for devices based on PMMA with thin layer of Au and AuNPs floating gates were 22 *V* and 32 *V*, respectively.

The electrical properties of the OTFMTs were improved by the use of the Au nanoparticles as the floating gate compared with that of an Au thin film. Using appropriate negative or positive voltages, the floating gate was charged and discharged, resulting in a clear shift in the threshold voltage of the memory transistors. Negative and positive pulses of 1 *V* resulted in clear write and erase states, respectively. Additionally, these organic memory transistors exhibited rather high carrier mobility of about $\mu = 0.319\ cm^2\ V^1\ s^{-1}$. Furthermore the data retention and endurance measurements confirmed the non-volatile memory properties of the memory devices fabricated in this study.

Dedicated to my parents and my husband, my daughter and son, my brothers and sisters.

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Chapter 1

Introduction

1.1 Introduction

During the last few years, the performance of electronic devices and circuits that based on organic compounds witnessed significant development. In addition to other properties characterise organic materials compared with inorganic materials such as low-temperature processing and low-cost manufacture, the ability to deposit these materials from solution provides the basis for applications requiring mechanical flexibility, and large-area coverage. Among the most important organic electronic devices that attracted a lot of attention from researchers are organic thin-film transistors (OTFTs) [1], organic memory devices [2], organic solar cells [3], and sensors [4]. Furthermore, in the field of organic light emitting diodes (OLEDs), the use of organic materials became of more interest in display panels' applications for different devices such as mobile phones and televisions.

One of the main advantages in organic materials is the possibility to change many of the electronic and chemical properties of polymers and small molecule materials by chemical modification. The morphology of thin films based on such materials can also be controlled using chemical modification. For example, the energy band gap in materials used in OLEDs can be adjusted to certain wavelengths of light [5].

Although in inorganic-based devices silicon is used significantly in early work as the base of the device structure beside the silicon dioxide (SiO_2) as the insulator, some organic small molecules, such as pentacene, produced rather good organic transistors.

These kind of devices resulted in field effect mobilities of about 3 cm^2/Vs [6], higher than recorded mobility for hydrogenated amorphous silicon (a-Si:H); about 1 cm^2/Vs [7]. The conduction in these OTFTs based on p-type organic semiconductors was obtained in accumulation, where only holes have the ability to conduct. Philips researchers in 1995 have succeeded in integrating OTFTs into electronic circuits, bringing to light the ability of such devices to perform logic functions, by building ring oscillators and logic gates [8]. This step was then followed soon by logic gates and inverters based on p-type organic semiconductors [9, 10]. Similar success demonstrated in transistor devices based on n-type organic semiconductors based on Buckminsterfullerene (C_{60}) as the active layer [11].

Designing of more complex circuits was successfully initiated by Crone et al. [12, 13]. As example for such devices are shift registers with 864 transistors [13] and decoders with operating voltages up to 100 *V* [12]. Recently, Klauk et al. were able to fabricate inverters operate at low applied voltages of 1.5 to 3 *V* [14]. These state of the art circuits based on NAND gates and ring oscillators with two different semiconductors; pentacene (p-channel device) and hexadecafluorocopperphthalocyanine (F_{16}CuPC, n-channel device) as the active layers as well as self-assembled monolayer (SAM) act as the gate dielectric.

It is important to mention the importance of bias stressing in OTFTs (which is studied in this thesis with different conditions), as it has critical effect on practical circuit applications. Bias-stressing is the shift of the current–voltage (*I–V*) characteristics with the application of continued voltages [15–17]. Structural disorder, at the semiconductor/dielectric interface or in the bulk of the semiconductor, as well as existed impurities act as traps leading to changes in threshold voltage [18]. In the "on state" of OTFTs devices, bias stress cause to some of the majority carriers becoming trapped in semiconductor/dielectric interface, so no longer contribute to the device conductivity. However, in the "off state" the bias stress results in minority carrier been trapped at the interface [19].

Recently, considerable interest has been focused on the development of new types of organic memory devices that can combine the properties of high speed, high density, and low power and cost with nonvolatility. Organic memory devices based on bistable switching [20], charge storage in MIS [21], and organic thin film memory transistors

(OTFMTs) [22–24] have been widely reported. The subject of memory devices is the main field of this thesis and will be reviewed in some details in Section 1.4 of this chapter.

1.2 Historical background

Historically, the beginning of organic electronics started with the identifying of organic semiconductors in the late 1940s [25]. Research on the electrical behaviour of organic materials were accumulated in the 1960s [26], while the discovery of photoconductive organic materials were in the 1970s, and late in that decade the conductive polymers were discovered [25]. The new impulse to the activity in the field of organic electronics was emerged after work in semiconductors and photoemission polymers established in the 1980s [27], for example, work on organic field-effect transistors (OFETs) [28], organic photovoltaic cells (OPVCs) [29], and organic light-emitting diodes (OLEDs) [30, 31]. The initial organic devices were based on either conjugated polymers such as polythiophene (PT) [28] and poly(p-phenylenevinylene) (PPV) [31] as the active layer in OFETs, or small organic molecules, such as, 8-hydroxyquinoline aluminium (Alq_3) as the emitting layer in OLEDs [30].

In the year 2000 the Nobel Prize in chemistry was awarded to Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa for the development of highly-conductive organic polymers (iodine-doped polyacetylene), which is discovered in 1977 [32]. Since that date (2000s), the performance of organic electronic devices has continuously improved; the power conversion efficiencies of OPVCs have reached over 5 % [33], OLEDs have now been launched onto the display market, and the performance of organic thin-film transistors (OTFTs) now competes with amorphous silicon TFTs, as shown in Figure 1.1 [34].

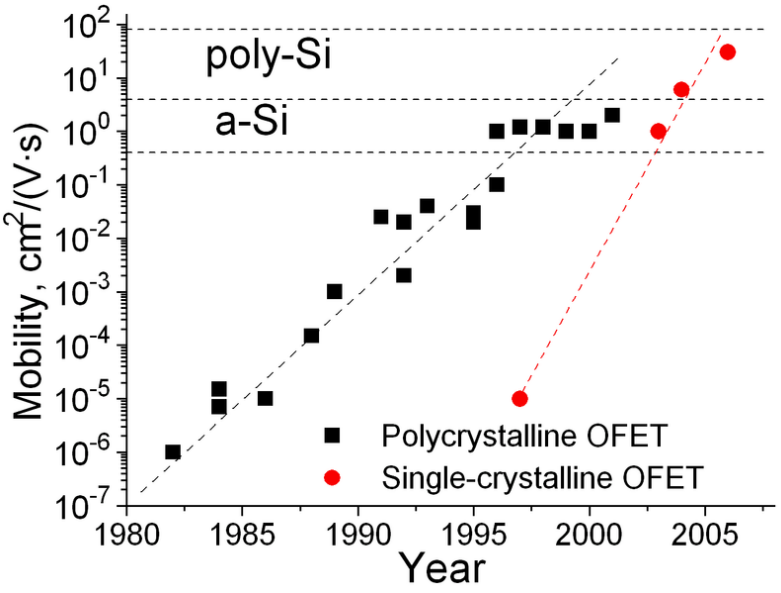

Figure 1.1: *Evolution of carrier mobility in organic field-effect transistor (OFET) [34].*

1.3 Organic electronic applications

Organic electronics has attracted considerable applications owing to their process ability advantages; they can be used for existing applications requiring mechanical flexibility, large-area coverage, low cost, and low-temperature processing. Figure 1.2 shows a number of application fields that can benefit from the ingenuity of organic electronics technology.

The applications of organic electronics include broad range of products and technologies, for example: sensors, active-matrix (AM), flat panel displays (FPDs) based on liquid crystal pixels, low-end smart cards, organic light emitting diodes, electronic ink, electronic identification tags, and perhaps all-flexible electronics. In this section we will review some of these applications.

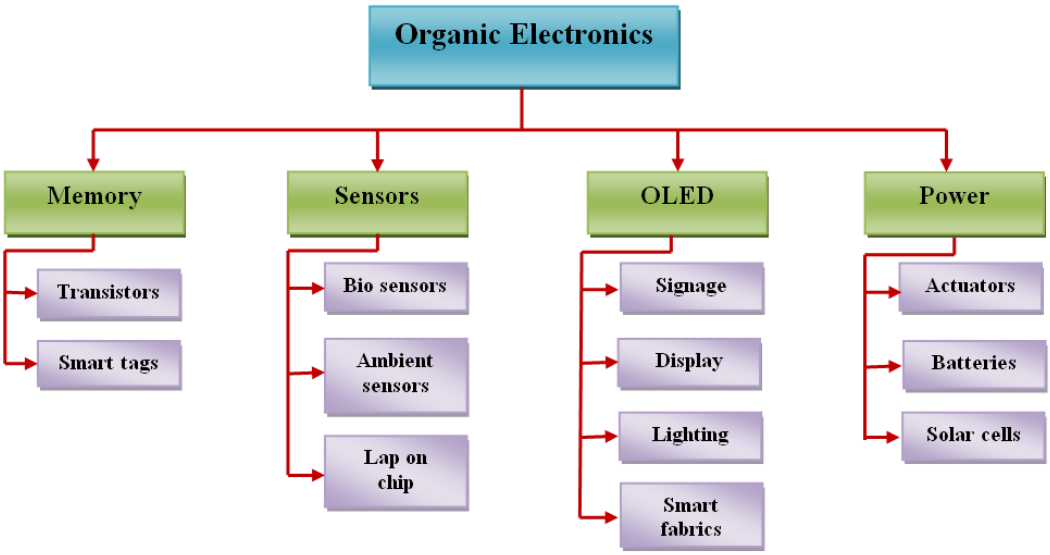

Figure 1.2: *A typical applications of organic electronic technology.*

Organic-based sensors used for environmental monitoring, home security, food safety and medical diagnostics have been intensely studied [35]. Organic sensors can be fabricated on flexible substrates with large-area coverage at room temperature using low-cost processes. Organic semiconductor materials have the possibility to lead to the manufacturing of sensors with selectivity and high sensitivity, where the important property for sensors is the ability to covalently attach biologically relevant moieties to organic semiconductor molecules [35].

In the field of flat panel displays, OTFTs are playing a key role in nowadays technology. In most applications the backplanes of AM OLED and AM liquid crystal displays (LCDs) are based on TFTs comprising low temperature poly silicon (LTPS) or hydrogenated amorphous silicon (a-Si:H) as the active layer. However, several advantages that OTFTs are possess such as: large-area coverage, low-cost manufacture and flexibility, make OTFTs a promising candidate for these backplanes. For example, it is impossible to make AM LCDs based on a-Si:H TFTs on a plastic substrate because of the high processing temperature needed for a-Si:H deposition.

In the year 2000, Philips Research [36] reported the first AM display based on organic semiconductors, while the electrophoretic flexible display using a backplane based on

OTFTs was shown in 2001 by Rogers et al. [37]. Hong et al. in 2005 [38] have reported high resolution for AM LCDs and the possibility to produce OTFT-based backplane with reasonably large size.

The performance of organic semiconductor technology has became sufficient to develop low-end smart cards and electronic identification tags applications that require low-cost circuits and modest speeds such as an integrated radio frequency identification (RFID) tag (operates at high-frequency, 13.56 MHz), intelligent electronic tickets, product packaging, card games and many other applications. Organic RFID tags can be produced with low cost and more flexible than those based on silicon by using solution processing and made of plastics. Pentacene based RFID circuits was demonstrated in 2003 by Baude et al. [39]. Following this in 2005, an organic RFID tag using novel pentacene and oligothiophene precursors was described by Subramanian et al [40]. Blache et al. reported the first working 4 bit transponder operating at a frequency of 13.56 MHz based on organic complementary metal-oxide-semiconductor (CMOS) in 2009 [41].

1.4 Memory devices

Memory device is a device that can preserve the information or data for later retrieval. Memory devices can be classified into two main types: volatile and non-volatile. Volatile memory devices lose the stored data as soon as the device is turned off and it need constant power to stay viable. There are mainly two types of volatile memory technology: Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM), the difference between them is the lifetime of the data they store. SRAM can keep the data reserved as long as the power is supplied but DRAM device can keep the data for a very short time, even when the power is turned on as DRAM is based on charge storage in a capacitor. DRAMs and SRAMs are extensively used in PCs mainly because DRAM's attributes of high density and low cost, and SRAM's attributes of high speed. On the other hand, non-volatile memory devices (NVMs) do not lose the data when the power supply is removed. NVM devices mainly consist of four types: flash memory, Ferroelectric Random Access Memory (FeRAM), Magnetic

Random Access Memory (MRAM) and phase change memory (PCM). The classification of memory devices technology is shown in Figure 1.3.

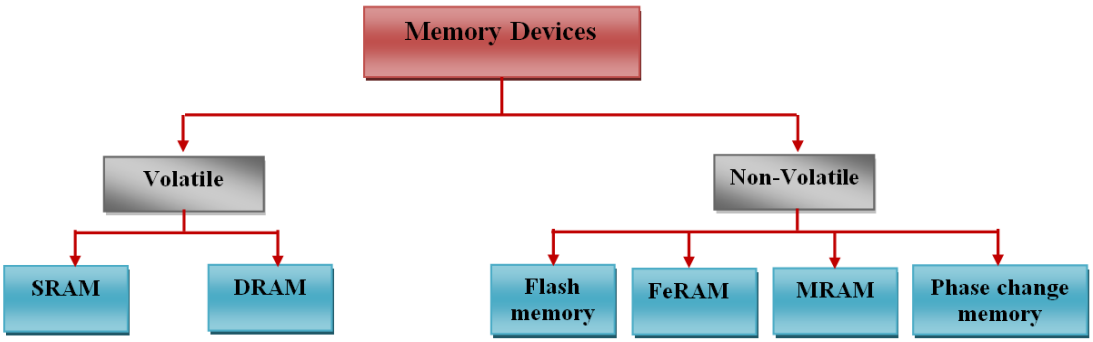

Figure 1.3: *A classification of memory devices technologies*.

Flash memory is the most suitable structure choice for non-volatile memory applications, since one cell consists of only one transistor. The data can be stored in a floating gate and defines the state of the memory by changing the threshold voltage of the transistor.

FeRAM is a non-volatile memory, in which a ferroelectric layer is used to store the data. Generally, there are two types of FeRAM technologies; ferroelectric field-effect transistor (FeFET) and capacitor-type. FeFET technology is a single element device uses a thin ferroelectric film as the gate dielectric in a FET [42]. Constructively, the second type, a capacitor-type, is similar to DRAM but to achieve a non-volatility property it uses a ferroelectric layer instead of the dielectric layer in DRAM for storing data.

The principle of the MRAM technology is based on storing the data as magnetic storage elements in micro-size cells not stored as current flows or electric charge. This technology needs a transistor and a magnetic tunnel junction [43], where it uses electron spin to store data (based on Spintronics).

PCM cell consists of a bipolar junction transistor and one resistor, the stored data in this non-volatile memory technology is based on the use of reversible phase change in

materials. Depending on applying suitable heat pulses, the PCM materials can be switched quickly back and forth between crystalline and amorphous [44]. PCM was used in optical information technologies (CD-ROM, DVD and so on), and it is expected to be a promising non-volatile memory.
In the following section, we will limit the memory devices review to the non-volatile floating gate memory device which is related to this study.

1.4.1 Floating gate memory device

In widespread, the flash memory technology is built on floating gate concept. Memory operation can be achieved by charging nanoparticles, nanowires, or nanocrystals integrated into the insulating layer [21, 22]. A floating gate memory is a field-effect transistor or metal insulator semiconductor (MIS) structures with two gate electrodes, in addition to the control gate; it has a floating gate embedded in the gate dielectric.
MIS capacitors provide the foundation base for various types of electronic devices from thin-film transistors to charge-coupled devices and memory structures. The simplicity of MIS structure made it a strong tool widely used for the analysis of the interfaces and electrical properties of MIS-based system. This is similar to metal oxide semiconductor (MOS) capacitors used as analytical tools for the improvement and understanding of silicon based devices. Understanding the physics of MIS capacitors was basically used to improve the inorganic-based devices. Organic MIS structures are in fact characterised by their capacitance-voltage (C-V) characteristics which exhibit three distinct regions: accumulation, depletion and deep depletion (inversion in inorganic MOS). Memory devices based on MIS structures consist of charge traps added inside the insulator of the structure, the charge traps behave as the floating gate. The addition of the floating gate results in a clear shift in the C-V characteristics and hysteresis in the double-sweep C-V curve. The hysteresis may lead to the definition of two stable capacitance states which may be controlled and read by an external bias stimulus and thus exhibiting the expected memory behaviour.

As for organic thin film memory transistors (OTFMs) when a large enough program voltage is applied between the control gate and the source contact, electronic charge

can be brought onto the floating gate by quantum tunnelling or thermal emission [45]. Charging the floating gate changes the transistor's threshold voltage, as the charge on the floating gate partially screens the electric field between the control gate and the semiconductor. The threshold voltage shift can be detected by measuring the drain current at a certain gate–source voltage [28]. As the floating gate is completely isolated by the dielectric layer, charges stored on the floating gate remain there without the need for any applied voltage (non-volatile memory). To erase the memory, a voltage of opposite polarity should be applied to discharge the floating gate [45].

1.5 Outline of the Thesis

The main theme of this thesis is investigation of pentacene-based organic memory devices. During this work, four different structures of organic electronic devices are fabricated and characterised: OMIS capacitors, OMIS memory structure, OTFTs, and OTFMTs. Different materials have been used in this thesis such as poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP) used as the gate dielectric, gold (Au) and Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS), used as contacts, thin layer of gold, gold nanoparticles (AuNPs) and single walled carbon nanotubes (SWCNTs) were used as floating gates. The behaviour of floating gate memory devices is based on the presence of hysteresis in the *C-V* and *I-V* characteristics of OMIS and OTFMTs, respectively. Therefore, the first objective of this work was to provide high performance, hysteresis-free devices that can be used as the control structures. This is an important step to ensure that memory behaviour is actually due to the presence of floating gate rather than trapped charges in the semiconductor/insulator interface. In addition, obtaining non-volatile OTFMTs operating at low programming voltages with long retention time is also investigated.

In Chapter 1, a general introduction to organic electronics is reviewed. The historical background and various applications of organic electronics are briefly given. A brief background of the memory devices is reviewed.

Introductions to organic semiconductors and dielectric materials as well as charge transport mechanisms in organic semiconductors are reviewed in Chapter 2. This

chapter also provides theoretical aspects relevant to the main theme of the thesis such as the electrical characterisation of MIS capacitors, TFTs and memory devices.

Chapter 3 provides information about the materials, experimental details and the techniques employed throughout this study.

Chapter 4 is the first results chapter, presents the fabrication and characterisation of OMIS capacitors and memory devices using different materials for gate electrode, gate dielectric and floating gates. This chapter also focused on the effect of surface morphology on device characteristics in order to establish optimal evaporation parameters for the evaporation of pentacene film.

In Chapter 5, the results are split into two parts, first part presents the result of pentacene-based OTFTs with two different types of organic gate dielectrics; PMMA and PVP. The influence of environment on device operation is also presented in this section. The second part focuse on the effect of bias stress on OTFTs with different conditions in order to measure the endurance properties of these devices.

The main objective of this study is presented in Chapter 6. This chapter presents the fabrication and characterisation of four types of pentacene based floating gate memory devices. Two different types of organic gate dielectrics are used; PMMA and PVP. Three different types of floating gates were incorporated: a thin film of gold, a layer of self-assembled metallic gold nanoparticles (AuNPs), and five layers of the Layer-by-Layer (LbL) single-walled carbon nanotubes (SWCNTs). Detailed programming and erasing procedures are also presented in this Chapter.

Finally, Chapter 7 provides the main conclusions derived from this work, together with possible further work.

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Chapter 2

Devices Theory of Organic Electronic

2.1 Introduction

In the last three decades, research in the field of organic electronics evolved rapidly with a large number of applications accompanied by the great potential to achieve industrial and commercial success. Research in this area includes to large extent multiple disciplines, for example; applied physics, industrial chemistry, electronic engineering, materials science and other areas. Pentacene-based organic devices have been strongly developed because of their lower cost, small weight, and higher integration density, for potential use in various applications such as organic displays, integrated circuit (IC), and flexible displays. Good device performance of organic metal-insulator-semiconductor (OMIS) capacitor, organic thin film transistor (OTFT) and organic thin film memory transistor (OTFMT) are useful tools to achieve these applications in the near future. All these three kinds of organic devices are achieved in this study with different materials.

This chapter reviews the theory, characterisation, and basic concepts relating to OMIS, OTFTs and OTFMTs to provide a foundation for the discussion of the results presented in Chapters 4, 5, and 6. An introduction to the main components of organic devices, the semiconductors and insulators, is provided in sections 2.2, 2.3 and 2.4. Charge transport mechanisms in organic semiconductors and metal-semiconductor interface are also reviewed in these sections. Metal-insulator-semiconductor structure is discussed in section 2.5, followed by the thin film transistor structure in section 2.6.

Finally the principles underlying the operation of memory devices are discussed in section 2.7 with special attention paid to the floating gate memory devices.

2.2 Organic semiconductors

In recent years organic semiconductor materials have attracted the attention of industrial and academic researchers alike due to the range of applications these materials can have. In particular, different organic semiconductors have been used as the active layer in organic thin film transistors (OTFTs) [1-3], organic light emitting diodes (OLEDs) [4, 5], organic photovoltaic (OPVs) [6] and organic memories [7-9]. These materials are including molecular crystals that can be formed by thermal evaporation, and conductive polymers that can be deposited by inkjet printing and spin-coating.

2.2.1 Charge transport in organic semiconductors

Organic semiconductors are hydrocarbon molecules based on carbon atoms which have six electrons with $1s^2 2s^2 2p^2$ electron configuration. The closest electrons to the nucleus, which have the lower potential energy, are held in the *1s* orbital, while the valence electrons responsible for forming various compounds by bounding with other elements are resided in the *2s* and *2p* orbits. Charge transport in organic semiconductors based on the capability of the charge carriers (electrons or holes) to pass between molecules. During the bonding process of organic materials, such as ethylene (C_2H_4) it is more favourable for the two electrons in *2s* to promote an electron to the *2p* orbital so that the electron configuration becomes $1s^2 2s^1 2px^1 2py^1 2pz^1$. As the hybridisation takes place, two types of bonds are created: single bonds between carbon-hydrogen atoms and carbon-carbon atoms called sigma (σ) bonds (possess highly localised electrons), and weakly couples pi (π) bonds that possess delocalised electrons, as shown in Figure 2.1.

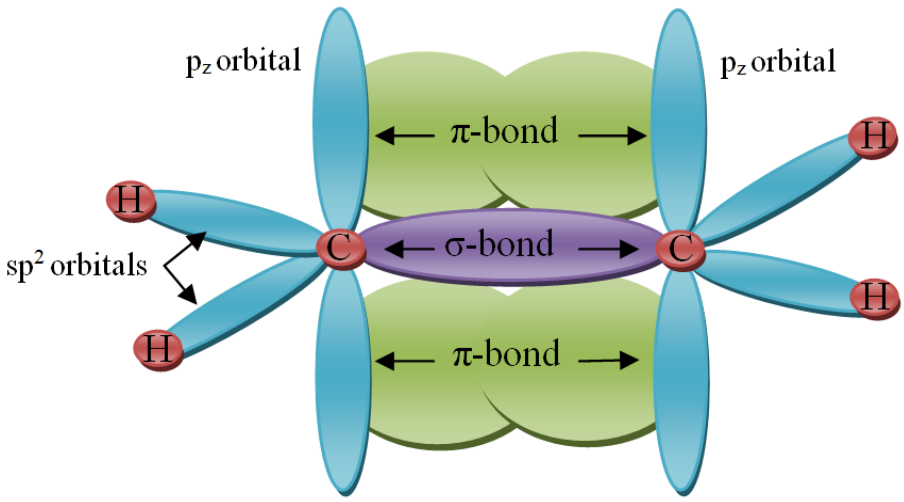

Figure 2.1: *diagram of the bonds and orbital for two sp^2-hybridised carbon atoms.*

In organic semiconductors, the interaction between neighbouring molecules results in the formation of energy bands as the discrete energy levels of the π electrons split to as many discrete bonding π and anti-bonding π^* states. At lower energy states, π electrons are located in the π band and the π^* band is empty [10]. The π and π^* bands are similar to the valence and conduction bands in inorganic semiconductors, respectively. The highest bonding energy level in organic semiconductors band structure is called Highest Occupied Molecular Orbital (HOMO), and lowest anti-bonding energy level is called Lowest Unoccupied Molecular Orbital (LUMO). The energy levels HOMO and LUMO are similar to the E_V and E_C in the inorganic semiconductors band structures, respectively [10]. The energy difference between the HOMO and LUMO represent the energy band gap (E_g) in inorganic semiconductors. A schematic diagram of the energy band structure for organic semiconductor is presented in Figure 2.2. Figure 2.2 shows the molecular orbital with electronic order for the ground state (S_0), first excited state (S_1) and first triplet excited state (T_1).

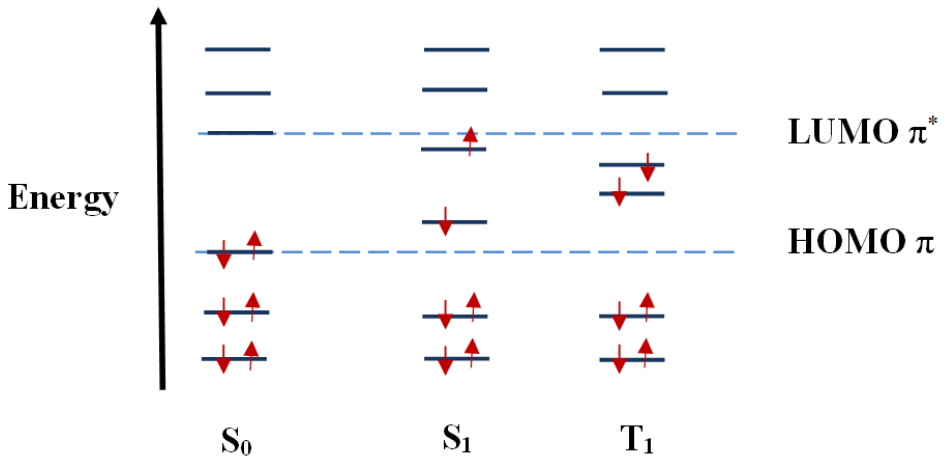

Figure 2.2*: Molecular orbital diagrams corresponding to the electronic ground and excited states in organic semiconductors.*

Two electrons of antiparallel spin are saturating the HOMO of the molecule in the ground state. However, the LUMO band remains empty until a state of agitation occurs. To initiate conduction in organic materials, an additional electron must be introduces to the LUMO band or (and) an electron removed from the HOMO band [11]. When excitation takes place, an electron moves from the HOMO to the LUMO, where the additional or missing electron in the anti-bonding or bonding orbital, respectively, are compatible with the nature of the excited state. One of the main processes to achieve conduction in such materials is the injection or extraction at electrodes. Due to the weak intermolecular bonds, delocalisation of charges is limited to few close molecules leading to low charge mobility in such materials [10]. Carrier mobility is referring to the moving of electrons or holes in the case of the availability of similar energy levels under the effect of electric field or temperature [12].

In conventional semiconductors such as silicon, doping with a few parts per million of donor or accepter impurities produces localised energy states in the band gap close to the conduction and valence bands, respectively. Due to the low purity in organic semiconductors this kind of doping is not practical. Therefore, p-type organic semiconductors have energy alignment with the electrode that is better facilitate the

injection of hole, while n-type semiconductors have alignment for the injection of electrons.

2.2.2 Small molecular organic semiconductors

Small molecules have an advantage of more fluid control of charge transport by modification of different molecular parameters. For instance, capability of these molecules to pack into well-organized polycrystalline films leads to higher mobility compared to polymeric semiconductors [13]. Small-molecule materials can be classified as heterocyclic oligomers, linear, and two-dimensional fused ring compounds. Pentacene, phthalocyanines (Pcs), and oligothiophenes (nT) (n indicate to the number of thiophene units) are the most representative p-type organic semiconductor materials based on small molecules. The chemical structures of these three examples are shown in Figure 2.3.

Pentacene is known to have the highest field-effect mobility among organic semiconductor materials, which makes it a promising candidate for preparation of p-type OTFTs based on small molecules [14]. This high mobility is outcome of considerable orbital overlap from edge-to-face interactions among the molecules in pentacene crystal lattice [2]. The pentacene molecule is a polycyclic aromatic hydrocarbon consisting of five aligned condensed benzene rings, as shown in Figure 2.3(a), and it called oligoacenes or linear acenes.

Oligothiophenes and their functional derivatives are also one of the important small molecule p-type semiconductor materials, which are used in a number of high-technology applications such as OFETs, OLEDs, and OPVs [5, 6, 15]. The ability of oligothiophenes to functionalize and to form well-ordered polycrystalline films in a herringbone arranging allows for the refine of their electronic properties [15]. Oligothiophenes used in OTFTs are either non-substituted, or substituted at both ends by a linear alkyl group (Figure 2.3(b)).

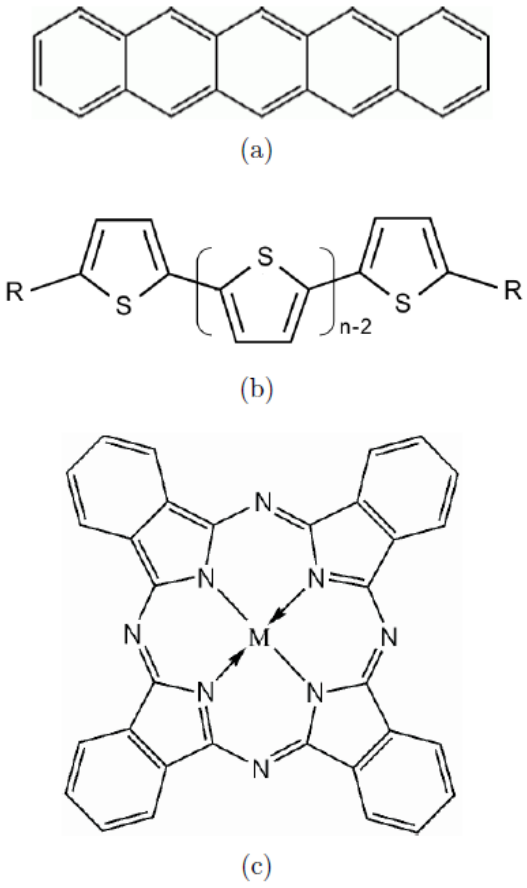

Figure 2.3: *Chemical structure of (a) pentacene, (b) oligothiophenes and (c) metal phthalocyanine (Pc) [14].*

Other small molecule p-type organic semiconductors are phthalocyanines (Pc), which considered to be one of the first reported families of small molecule. The structure of the phthalocyanine molecule has a molecular cage, into which different metals can be introduced. Figure 2.3(c) shows the chemical structure of metal Pc where the central hydrogen atom is changed to the metal atom (M = H_2). Many Pc compounds are substituted with electron withdrawing groups at their periphery, for example hexadecafluoro-substituted copper Pc (R = F, M = Cu) [15]. Furthermore, these compounds can be sublimed but do not melt, and most of them are thermally very stable [16].

2.2.3 Polymeric semiconductors

The first discovery of conductive polymers, doped with iodine, was by Shirakawa et al. in 1977 [17]. As shown in Figure 1.1 (in Chapter 1), the magnitude of the field-effect mobility in small molecules is one order higher than those of the polymers. This can be explained by the fact that thermally evaporated small molecules materials provide better ordering of crystalline structures than solution-processed polymers [14].

Polythiophenes (PTs) is one of the most commonly used materials for most work dealing with polymer-based OTFTs [18]. Various derivatives have combined their excellent electronic and optical properties with solution processability and perfect chemical stability [19]. It is well known that the good structural ordering of the chains at the polymer-insulator interface lead to improved performance of polymer-based OTFTs [20]. The alkyl derivatives can be integrated into a PT-based polymer chain with three different arrangement: head-to-tail (h–t), head-to-head (h–h) and tail-to-tail (t–t) [16]. Figure 2.4 shows different couplings of pairs of poly(3-alkylthiophene) (P_3AT) monomers, which has the highest carrier mobility, up to 0.1 $cm^2\ V^{-1}\ s^{-1}$ with the head-to-tail arrangement [18]. A polymer with one of these linkages (h-t or h-h or t-t) is referred to as regionregular in PT, while with a mixture of linkages is referred to as regionrandom [16].

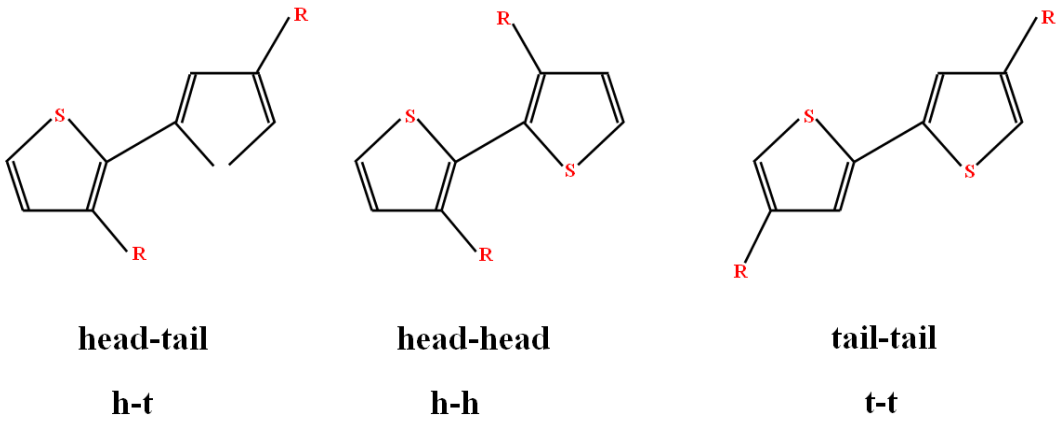

Figure 2.4: *Chemical structure of poly(3-alkylthiophene) (P3AT) with different couplings of pairs of monomers.*

2.3 Gate dielectrics

The interface between the active layer and gate dielectric is an important factor in determining the performance of organic electronic devices, especially for OTFTs. This importance lies in the control of the charge carriers that flow through the interface. Consequently, the interest in the improvement of suitable dielectric materials is an essential element in developing organic electronic devices. Practically, the operating voltage of the device is determined directly by the permittivity constant and the film thickness of the gate dielectric. The dielectric film roughness is another important factor, which determines the mechanical and chemical properties of the insulator-semiconductor interface, which have large influence on the mobility of OTFTs. Besides these factors, the deposition process and the ease of processing and preparing the insulating layer also important in decision-taking. The insulating materials can be classified as: organic (polymeric), inorganic (conventional), multilayer, nanocomposite and ultra-thin self-assembled monolayers (SAMs) materials. As all insulating materials that are used in this study are organic type materials, we will focus here on this class of materials.

There is a large number of inorganic dielectric materials have been studied and investigated over the past few decades, some of these materials and the most important properties that characterise these materials are listed in Table 2.1. For example, silicon dioxide (SiO_2) which has thermodynamic stability and large band gap (8.9 eV) [16], as well as high dielectric constant, made it as excellent dielectric layer. On the other hand the thermally grown property of silicon dioxide made it not suitable with flexible substrates as expected in organic electronics. Other examples for inorganic dielectric materials are tantalum oxide (Ta_2O_5) and titanium dioxide (TiO_2). Both these materials characterised with high dielectric constants as shown in Table 2.1.

Self-assembled monolayer (SAM) dielectric films which usually used as surface treatments are considered one of the promising dielectrics for organic electronics such as for low-voltage OTFTs due to their dense packaging and the short chain length [21].

Table 2.1: *Overview of inorganic dielectric materials [22].*

Material	Preparation method	Dielectric constant
SiO_2	Thermally grown	3.9
Al_2O_3	Sputtered	~5.1
Al_2O_3	Anodised	~4.2
TiO_2	Anodised	21
SiN_x	CVD	6~7
Ba(ZrTi)O	RF sputtered	17.3
Ba(SrTi)O	RF sputtered	16
Ta_2O_5	Sputtered	25

Multilayers insulating films are another type of dielectric layers composed of inorganic or organic insulating materials. They have been used to modify the surface of dielectric materials, where the roughness of the dielectric surface and the growth of the crystalline grains of the semiconductor can be improved by the addition of a layer of these materials. Examples of such additives are alkyl phosphonic acid monolayers on alumina [23], octadecyl-trichlorosilane (OTS) on silicon oxide [24], and octadecyl-trimethoxysilane (OTMS) on ziconium oxide dielectrics [25]. It has been reported that the field-effect mobility of OTFTs could be improved when polymers such as poly(α-methylstyrene) [26] or polystyrene [27] are added on the oxide layer.

Nanocomposites are another dielectric materials generated by blending of polymeric and ceramic materials, in order to modify the permittivity of organic insulators. For example, the permittivity of the traditional insulator Poly(vinyl phenol) (PVP) can be increased from 4 to 5.4 (at 1 MHz) for 7 % nanoparticles content of TiO_2 [28]. It is also important to mention at this point that the permittivity of organic insulators is frequency dependent.

2.3.1 Polymer dielectrics

Polymers are one of the major types of organic materials, generality of dielectric nature. Polymers can be formed to thin films by spin-coating, inkjet-printing or dip-coating. There are several polymers that have superior insulating characteristics with neglected leakage currents. Examples for such polymers are poly(methyl methacrylate) (PMMA), polystyrene (PS), poly(vinyl phenol) (PVP), poly(vinyl alcohol) (PVA), cyanoethylpullulan (CYEPL), parylene C and benzocyclobutene (BCB), as shown in Table 2.2.

Table 2.2: *Overview of the organic dielectric materials measured at 10 kHz [16].*

Material	Preparation method	Dielectric constant
Poly(methyl methacrylate)	Spin-coated	3.5
Polystyrene	Spin-coated	2.6
Poly(vinyl phenol)	Spin-coated	6.4
Poly(vinyl alcohol)	Spin-coated	10
Cyanoethylpullulan	Spin-coated	12
Parylene C	Vapour deposited	3.1
Benzocyclobutene	Spin-coated	2.65

One of the first common polymers used as insulating layers in organic electronics are PMMA and PS. Also, other polymer dielectric materials such as PVP and PVA are used in the fabrication of organic devices. Moreover, the durability of these insulators can be enhanced by cross-linking, using chemical agents such as hexamethylene tetraamine or melamine-co-formaldehyde. In general, dielectric materials exhibit low capacitance and accordingly the organic transistors based on these materials operate at relatively high voltages [14]. However, several research based on OTFTs with siloxane cross-linked ultra-thin polymeric films reported the improved characteristics of low leakage currents, insolubility and high capacitance [29-32].

2.4 Metal-semiconductor interface

The resistance that of two connected metals is as low as that have assumed for metal-semiconductor contacts. The characteristics of the interface between metal and semiconductor are responsible for determining the nature of the contact between them either as Ohmic or a blocking (rectifying) contact. The Fermi energy level of the semiconductor (E_{Fs}) and the work function of the metal (ϕ_m) are the factors that identifies whether that contact is Ohmic or rectifying. To produce an Ohmic contact, the Fermi level for a p-type semiconductor, situated near the valence band (E_v), should be equal or less than ϕ_m, in other words $\phi_m \geq E_{Fs}$, as shown in Figure 2.5. In contrast to the p-type semiconductors, an n-type semiconductors should have a Fermi level higher than ϕ_m, [33].

Figure 2.5 shows the energy band diagram of a metal with a work function (ϕ_m), and a p-type semiconductor with a work function (ϕ_s), (a) before contact and (b) directly after contact to produce an Ohmic contact. When the two materials brought into contact (Figure 2.5(b)), and to achieve the thermal equilibrium, the Fermi levels aligned with a small downward band bending in the semiconductor band structure. Electrons can flow from the semiconductor into the metal, leaving behind more holes in the interface; whereas electrons in the metal have the ability to move into the empty states in the semiconductor [34].

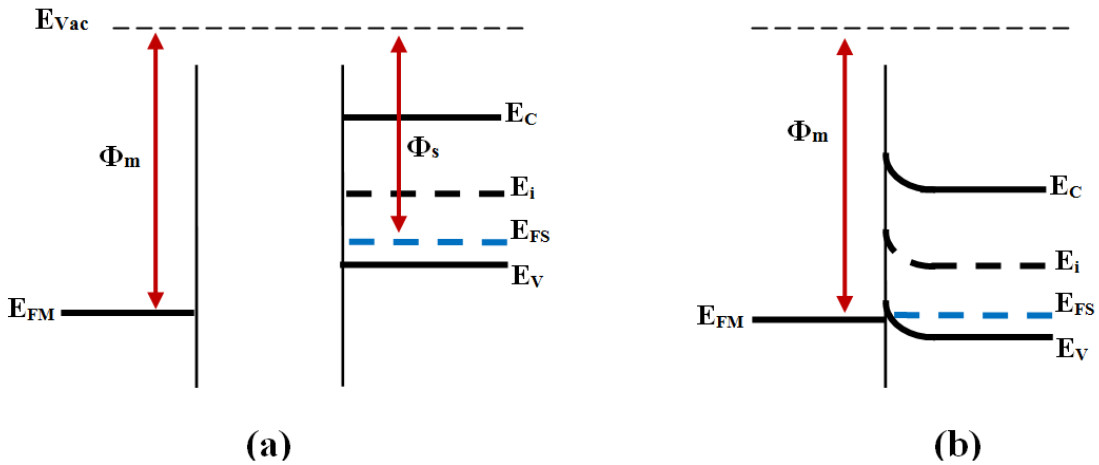

Figure 2.5: *Ohmic contact formation between a metal and a p-type semiconductor (a) before and (b) they are brought into contact.*

2.5 Metal-insulator-semiconductor (MIS) devices

The metal-insulator-semiconductor (MIS) structure plays an important role in the further understanding of the interface properties between semiconductor and insulating layers. The semiconductor/insulator interface is considered to be one of the main parameters for identifying stability and reliability of many organic electronic devices. MIS capacitor is simple device structure widely used as the bases for the fabrication of several electronic devices such as TFTs and memory structures.

2.5.1 MIS capacitor structure

The MIS capacitor structure (Figure 2.6) is formed from layers of insulating and semiconducting materials separates two conducting electrodes. The gate electrode is the bottom conducting electrode, which is metallic, where the gate bias voltage is applied. An insulating layer is set above the metal gate and separates it from a thin layer of semiconducting material where connectivity is determined by the population of electric charges in this layer. The top electrode to the back of the semiconductor is made from a metal, the charge carriers that injected into the semiconductor from this electrode provides an Ohmic contact to the semiconducting layer.

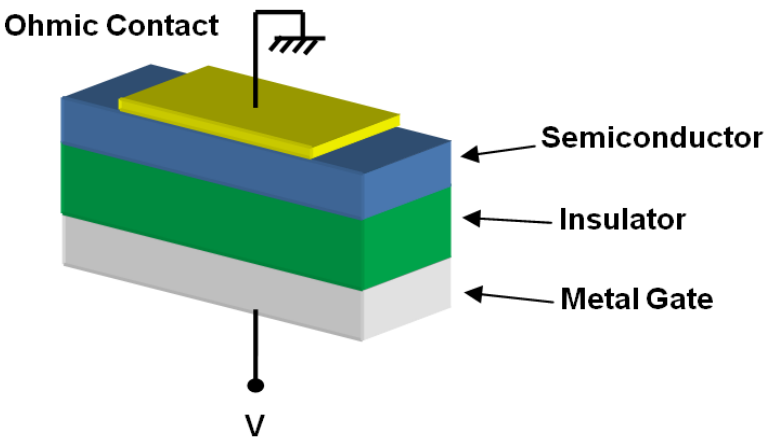

Figure 2.6: *Schematic diagram of an MIS structure*.

2.5.1.1 MIS capacitor energy band structure

In solid-state physics of semiconductors, energy band diagram is a description of the state of the electron in terms of energy owned. Valence energy band (E_V), there is not potentially electrical conductivity where the electrons are restricted into the atomic structure of the material. Conduction energy band (E_C), electrons are available to make an electrical current where the electrons are free and can move. The highest energy level that electrons populated at a temperature of absolute zero is a Fermi energy level (E_F). Electrons that have energy greater than E_F, can participate in the connectivity, while electrons with less energy are restricted to the crystal structure. In the metals, the valence energy band is overlapping with the conduction band, whilst there is a small energy band gap (E_g) separates E_V from E_C in the semiconductors. For the insulating materials, E_g is large, therefore, electrons cannot leave the valence energy band to enter the conduction energy band.

In order to understand the behaviour of MIS structure, we must characterize the four modes of operation of an ideal MIS capacitor. Depending on the magnitude and polarity of the applied voltage to the gate electrode one of these modes will occur: flatband, accumulation, depletion and inversion mode, which will be explained in the following sections.

2.5.1.1.1 Flatband mode

Figure 2.7 shows the energy band diagram for an ideal MIS capacitor at flatband conditions of p-type semiconductor. Flat band conditions occurs, for an ideal MIS capacitor, when there is no applied gate voltage (V = 0), i.e. no charge is existent on the semiconductor; therefore the energy bands are flat. This condition occurs at 0 V if no interface traps in the insulator, and the resistance in the insulator is almost infinite [34]. Also, the work function of the metal gate electrode is equal to the work function of the semiconductor. In other words, the flatband exists when the difference in the work function between the gate metal and the semiconductor equals the applied gate voltage.

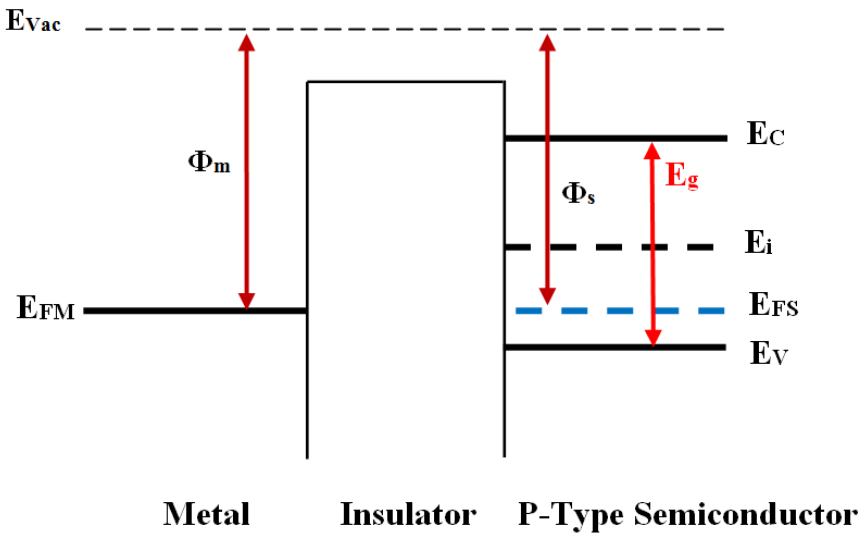

Figure 2.7: *Energy band diagram of an ideal p-type-based MIS capacitor at flatband condition.*

In practical MIS structures, it is very difficult to find a semiconductor and a metal with exactly the same value of work function, also, organic insulating materials would have some kind of defects resulted in shifting the flatband condition to a non-zero value. In a non-ideal MIS capacitor (practical) this shift will occur as a shift in the experimental capacitance-voltage plot (*C*-*V*) along the voltage axis due to the present of charges, Q_i, in the insulator. This shifting is expressed by a non-zero flatband voltage (V_{FB}). For example, if a negative voltage is applied to a p-type MIS device, V_{FB} shifts to higher positive bias. Therefore, the polarity of charges in the insulator can be decided from the direction of the shift of the *C*-*V* curve. The expression for the total shift in flatband voltage can be given as follows [35],

$$V_{FB} = \phi_{ms} - \frac{Q_i}{C_i}, \tag{2.1}$$

where ϕ_{ms} is the work function difference between the gate metal and the semiconductor, and C_i is the insulator capacitance per unit area.

2.5.1.1.2 Accumulation mode

Figure 2.8 shows the energy band diagrams of an ideal p-type MIS capacitor biased in accumulation, which occurs when a negative voltage ($V < 0$) is applied to the metal gate. The Fermi level of the gate electrode is raised to a higher position by an amount equal to the applied negative voltage. Due to the applied negative voltage, an electric field is built across the insulator and the free electrons in the gate electrode drifts toward the interface with the insulator, creating a negatively charged region in the interface. To maintain the equilibrium condition, an equal positively charged region is created in the semiconductor/insulator interface. The valance band edge, $E_{V,}$ in the semiconductor bend upward in the interface region with the insulator as shown in Figure 2.8. This shift in E_V makes the valence band edge move closer to the Fermi level at the insulator interface; leads to an accumulation of holes (majority carriers) near the interface surface. The accumulation of carriers depends on the band-bending of the edges, where this bending is increasing with high applied voltages [34].

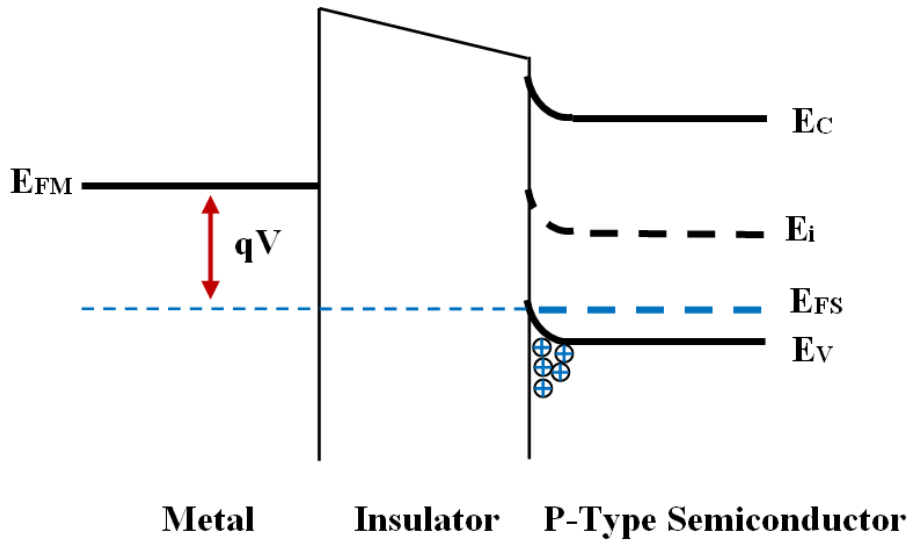

Figure 2.8: *Energy band diagram of an ideal p-type-based MIS capacitor in accumulation mode.*

2.5.1.1.3 Depletion mode

The depletion mode (Figure 2.9) occurs when a small positive voltage ($V > 0$) is applied to the gate electrode; creating an electric field that displace free electrons from the metal/insulator interface towards the bulk of the metal. As a result metal ions are formed in the metal/insulator interface, giving rise to a positively charged region. To maintain the equilibrium condition, an equal negatively charged region is created in the semiconductor/insulator interface. Hence, the valance band bends downward, moving away from the Fermi level in the interface region. The electric field repels any holes at the semiconductor/insulator interface towards the bulk of the semiconductor and then reduces the concentration of majority carriers near the interface. Therefore, surface depletion is formed when the positive gate voltage repelled the holes in the semiconductor, and this lead to create negatively charged ions in the semiconductor surface. The depletion layer width, *w*, further increases with increasing gate bias voltage.

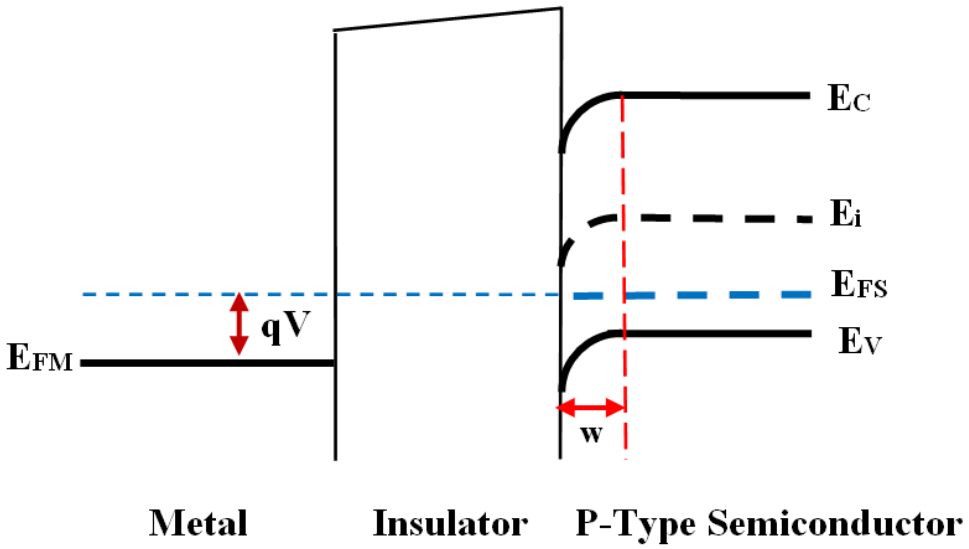

Figure 2.9: *Energy band diagram of an ideal p-type-based MIS capacitor in depletion mode.*

It is important to know the surface charge per unit area (Q_S) in this region, which is given by [35];

$$Q_S = -qN_a w, \tag{2.2}$$

where N_a is the doping concentration, and q is the elementary charge. The electric field in the semiconductor layer (E_S) is

$$E_S = \frac{qN_a w}{\varepsilon_s}, \tag{2.3}$$

where ε_s is the absolute permittivity of the semiconductor. The potential at the semiconductor surface, ψ_S, which is resulted from integrating the electric field, can give by;

$$\psi_s = \frac{qN_a w^2}{2\varepsilon_s}, \tag{2.4}$$

The applied voltage V is applied at both the semiconductor and insulator, i.e.

$$V = V_I + \psi_s \tag{2.5}$$

where V_I is the voltage across the insulator,

$$V_I = \frac{Q_S}{C_i} \tag{2.6}$$

where C_i is the capacitance per unit area of the insulator. As a result, the expression for the depletion width can be obtained from combining the Equations 2.4, 2.5 and 2.6, whose solution is

$$w = -\frac{\varepsilon_s}{C_i} + \sqrt{\frac{\varepsilon_s^2}{C_i^2} - \frac{2\varepsilon_s V}{qN_a}}. \tag{2.7}$$

2.5.1.1.4 Inversion mode

As the gate positive charge increases ($V >> 0$), the potential in the semiconductor increases, then the bands bend more downward to the extent that the intrinsic Fermi level, E_i, penetrates the Fermi level, E_{FS}, as shown in Figure 2.10. In this mode, the semiconductor surface exhibits n-type conduction as more electrons (minority carriers) emerge at the surface and become greater than that of holes in the bulk; therefore, a so-called inversion layer is formed.

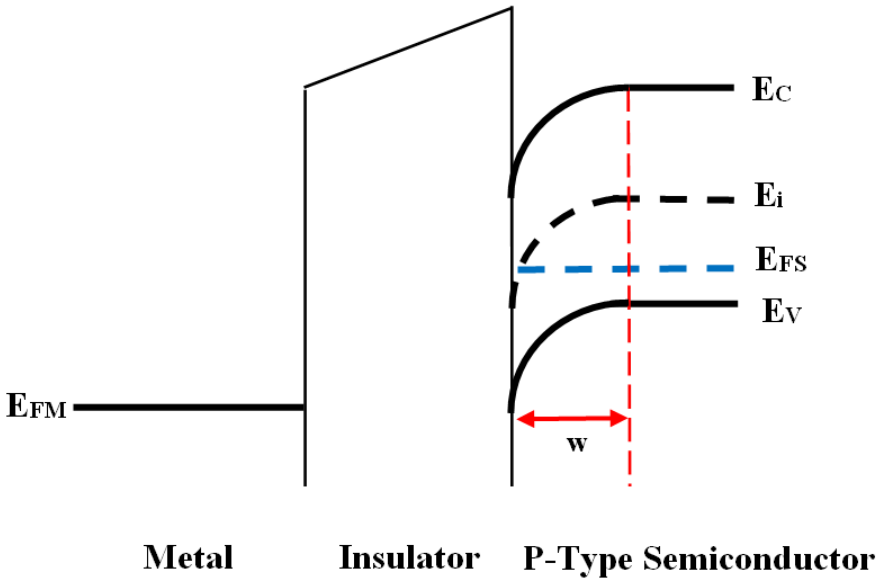

Figure 2.10*: Energy band diagram of an ideal p-type-based MIS capacitor in inversion mode.*

2.5.1.2 Ideal MIS capacitance-voltage characteristics

In the case of an alternating current (AC) voltage of angular frequency $\omega = 2\pi f$ (where f is the frequency) is imposed on the gate of an MIS device, the band-bending will vary with time as it pursues the applied AC voltage. To maintain balance of the charges on the gate, this is done by outflow the charges in and out of the semiconductor surface. As discussed in Section 2.5.1.1 for the effects of an applied bias voltage on MIS

capacitor, it is expected that the capacitance of the MIS structure to change depending on the applied voltage; leads to the accumulation, depletion and inversion regions as shown in Figure 2.11.

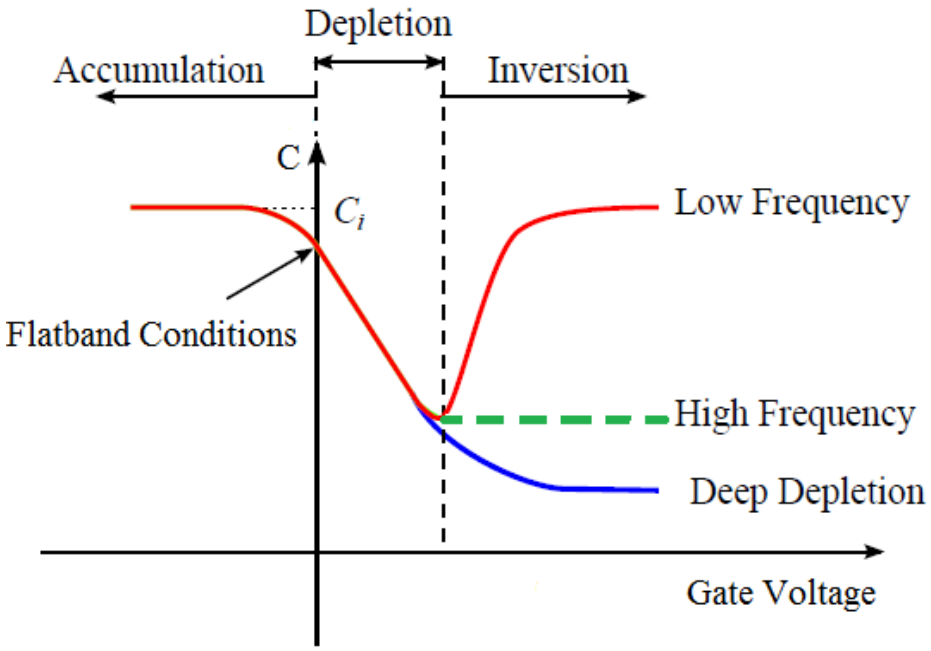

Figure 2.11: *Capacitance–voltage (C-V) response of an ideal MIS capacitor based on a p-type semiconductor at low frequencies (red solid line), at high frequencies (green dashed line), and deep depletion (blue solid line).*

In the accumulation region, the concentration of majority carriers (holes) at the surface exists within a very thin layer, leading to a large differential in the capacitance of the semiconductor (C_s). At low frequencies the majority carrier at the interface is able to follow the AC voltage so the measured capacitance (C_m) is equal to that of the insulator (C_i), $C_m = C_i$, then C_m can be given by

$$C_m = \frac{A\varepsilon_0\varepsilon_{Ins}}{d_{Ins}} \tag{2.8}$$

where A is the area of the top electrode, ε_0 is the permittivity of free space, ε_{Ins} and d_{Ins} are the absolute permittivity and thickness of the insulator, respectively.

When the gate voltage is reached to more positive voltages in the depletion region, the density of holes at the surface are reduces, the value of the device capacitance decreases. As the gate voltage becomes higher, a depletion layer of ionized acceptors is formed due to the repelling of the holes from the surface, and the MIS capacitance is called the depletion capacitance (C_d). The total measured capacitance, C_m, at the end of the depletion region reduces to the series sum of insulator capacitance C_i and the depletion capacitance C_d, and given by:

$$\frac{1}{C_m} = \frac{1}{C_i} + \frac{1}{C_d} \tag{2.9}$$

The value of C_d decreases when the depletion layer width increases, and reach a minimum at the full depletion layer width.

For the inversion region, depending on the modulation of the frequency, the charge carriers at the interface of semiconductor-insulator can lead to two different regimes as shown in Figure 2.11. At low enough frequency (< 100 Hz), the majority carriers can follow the AC signal. Therefore, the differential capacitance of this regime increases with bias and ultimately the measured capacitance is equal to the insulator capacitance, i.e. $C_m \approx C_i$ (red solid line in Figure 2.11). At high frequencies, charge carriers cannot follow the AC signal, but that those at the edge of the depletion region can do so. Consequently the measured capacitance remains at its minimum value and equal to the series sum of C_i and C_d (green dashed line in Figure 2.11). In the case of organic semiconductors, response time of charge carriers is very slow to keep track of the changes in the gate voltage, the depletion region capacitance continues, pending it fills the semiconductor bulk, and now the deep depletion is achieved (blue solid line in Figure 2.11).

2.5.2 Doping density

The doping density of organic semiconducting material represents the number of free majority charge carriers existent in the semiconductor bulk. The doping density *($N_a(w)$)* can be obtained using Mott-Schottky analysis from the inverse of the slope of *$1/C_m^2$* versus gate voltage, V_G, in depletion region, as follow [36]

$$N_a(w) = -2[q\varepsilon_s \frac{d}{dV_G}\left(\frac{1}{C_m}\right)^2]^{-1} \quad (2.10)$$

where *w* is the depletion layer width. The positive slope of the plot denotes that the dopants are acceptors; while the negative slope denotes that they are donors. If the distribution of dopants is uniform, a straight line with slope proportional to doping density is the result.

2.5.3 Equivalent circuits of MIS capacitor

Equivalent circuits facilitate a way to model the conduction of MIS capacitors. The majority carriers have the ability to follow the AC voltage signal, this happen when the period of the applied AC voltage is much longer than the dielectric relaxation time of the semiconductor (τ_D); i.e. $1/\omega >> \tau_D$. When the frequency of the AC signal become high, the majority carriers cannot respond, and the thermal equilibrium is not preserved leading to an energy loss. This loss is characterised as resistive element where it is modelled by an *R-C* time constant. The equivalent circuit for the MIS capacitor device in accumulation region is shown in Figure 2.12 where the bulk semiconductor resistance R_B is in parallel with the bulk capacitance C_B [37].

The circuit relaxation time (τ_R) of the MIS capacitor in accumulation can be described by [37],

$$\tau_R = R_B\,(C_I + C_B), \quad (2.11)$$

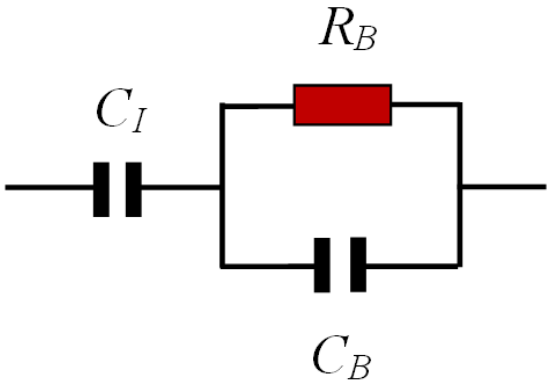

Figure 2.12: *Equivalent circuit for an ideal MIS capacitor in accumulation region.*

and the relaxation frequency in this region is [38],

$$f_R = \frac{1}{2\pi R_B\,(C_I + C_B)} \tag{2.12}$$

In the case of the MIS capacitor is biased into depletion region, the equivalent circuit (Figure 2.13) must include the depletion capacitance C_D which is associated with the depletion layer width, w, and can be calculated by

$$C_D = \frac{\varepsilon_S A}{w} \tag{2.13}$$

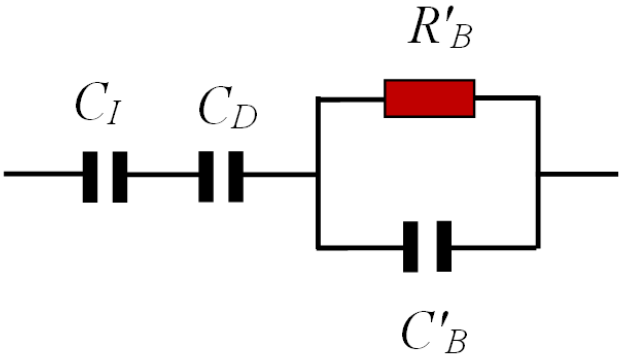

Figure 2.13: *Equivalent circuit for an ideal MIS capacitor in depletion region.*

The relaxation frequency in this region is now give by

$$f_R = \frac{1}{2\pi R'_B\,(C'_I + C'_B)}\,. \tag{2.14}$$

where C_I has been substituted by the series sum (C'_I) of C_I and C_D, and R_B and C_B substituted with R'_B and C'_B respectively.

The relaxation frequency value between that in accumulation and full depletion regions will be increase as result of grow the depletion region, therefore, [38]

$$\frac{1}{2\pi R_B\,(C_I + C_B)} < f_R < \frac{1}{2\pi R'_B C'_B} = \frac{1}{2\pi\tau_D} \tag{2.15}$$

where $\tau_D = \rho_S\varepsilon_S$ is the relaxation time of the undepleted semiconductor, ρ_S is the semiconductor resistivity.

2.6 Organic thin film transistor (OTFT) device

For more than a decade, organic thin-film transistors (OTFTs) occupied a large place in the areas of electronic applications on account of the applications in low cost and flexible electronics, alternative of silicon-based electronics [21, 39-42]. The first concept of a TFT was reported by Weimer in 1962 [43] and this guided to the first a-Si:H TFT by Le Comber in 1979 [44]. The first reports on OTFTs appeared twenty years later [45-47]. The main difference between the metal-oxide-semiconductor-field-effect-transistor (MOSFET) and the OTFT is that the channel is formed in MOSFET by the inversion of charge carriers close to the insulator-semiconductor interface. For OTFTs based on a p-type semiconductor, applied positive voltage to the gate electrode lead to depletion layer of charge carriers and operate the device in depletion mode, this caused to high channel resistance (off-state). On the other hand, applied negative voltage to the gate electrode lead to a large concentration of charge carriers and operate the device in accumulation mode, this caused to low channel resistance (on-state).

2.6.1 Device Structures of OTFTs

The common configurations of OTFTs are shown in Figure 2.14. These configurations are possible depend on the order of the gate electrode and source/drain (*S/D*) electrodes are formed at bottom or top of the structure, as well as present of the semiconductor and dielectric layers between them. The dielectric layer must separate the gate electrode from the semiconductor. The four configurations of OTFTs are: two of them are bottom-gate (BG) configurations, this can be achieved in two ways; referred to as bottom-gate, top-contact (BG-TC) (Figure 2.14(a)), and bottom-gate, bottom-contact (BG-BC) (Figure 2.14(b)) configurations. The other two architectures of OTFTs are top-gate (TG) which also can be achieved in two ways; top-gate, bottom-contact (TG-BC) (Figure 2.14(c)), and top-gate, top-contact (TG-TC) (Figure 2.14(d)) configurations. The nature of the contact between the source/drain electrodes and the semiconductor must be Ohmic to allow the charge carriers to inject and retrieve.

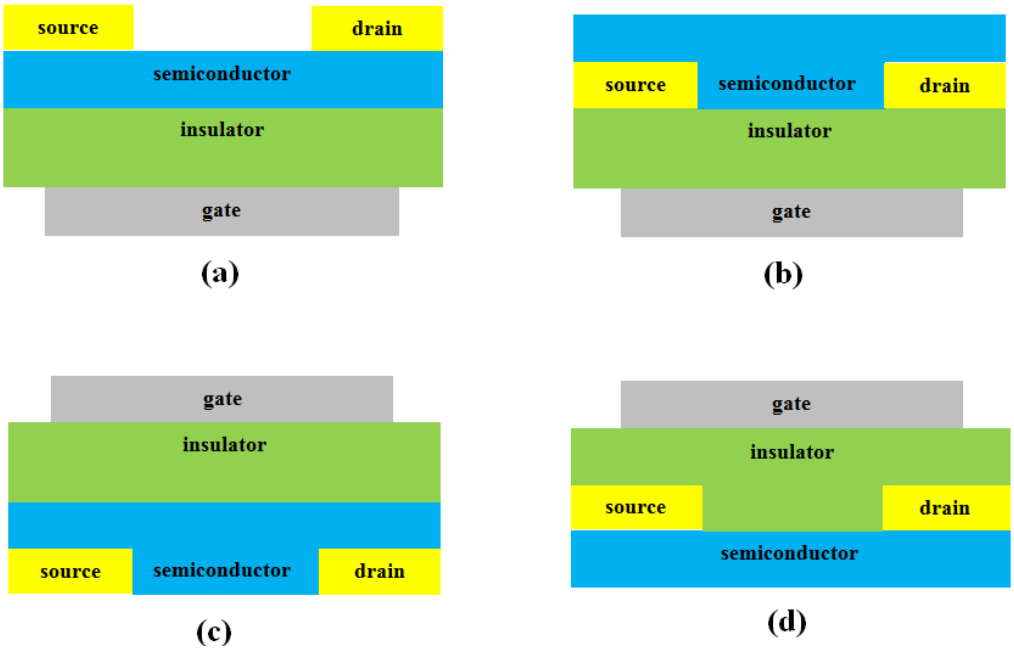

Figure 2.14: *Schematic diagrams of OTFTs configurations with (a) bottom-gate, top-contact (BG-TC), (b) bottom-gate, bottom-contact (BG-BC), (c) top-gate, bottom-contact (TG-BC) and (d) top-gate, top-contact (TG-TC).*

Each of these configurations has its advantages and drawbacks. In the BG configurations, the photolithographic methods can be used to pattern the S/D electrodes of BG-BC configuration as the semiconductor is deposited on the top. However, it has been reported a better device performance for BG-TC than in the BG-BC because of the lower contact resistance in the TC configuration [21] due to increase of contact area between the metal and the semiconductor. For TG configurations, as justification of the relatively 'fragile' properties of the semiconductor layer, the deposition process of the dielectric layer on the semiconductor in the TG-BC configuration is much harder than the other way in TG-TC configuration. However, the dielectric layer in this configuration is not only works as the gate insulator but as well offers a passivation layer for the semiconductor.

The configuration of bottom-gate and top-contact of OTFT is used in our study; this structure is similar to that of the MIS capacitor described in previous section. The gate electrode was first deposited onto the substrate, followed by the dielectric layer separated the gate from the semiconductor, the source and drain contacts are then deposited onto the semiconductor. The basic configuration of such OTFT device is shown in Figure 2.15, where there are three terminal devices for operation; the gate, source and drain. The control process of the flow of current between the source and drain contacts are achieved by applying a direct current (DC) voltage to the gate electrode. There is uncovered semiconductor distance separated the source from the drain known as the channel, where the length of this channel is L and the width is W, as shown in Figure 2.15.

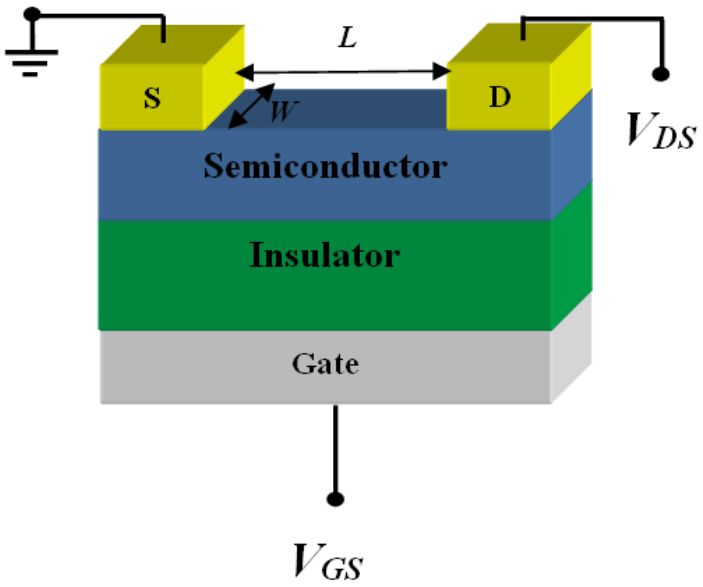

Figure 2.15: *Structure of bottom-gate, top-contact thin-film transistor TFT.*

2.6.2 Electrical characteristics of OTFTs

In the OTFT based on p-type semiconductor, the gate-source voltage (V_{GS}) controls the conductivity of the transistor channel by modulating the accumulation layer of holes. When a negative voltage is applied to the gate, this modulation of the accumulation layer results in the curves of drain-source current (I_{DS}) versus drain-source voltage (V_{DS}), as shown in Figure 2.16.

Figure 2.16 shows the output characteristics of a p-type transistor, where the I_{DS} values changing as a function of the V_{DS} for different applied values of V_{GS}. For the linear region of device operation, at low V_{DS} ($V_{DS} < V_{GS}$), the drain source current, I_{DS}, initially increases proportionally with V_{DS}, i.e. the $I_{DS(lin)}$ is related to the V_{DS} (as $V_T >> V_{DS}$) by [48];

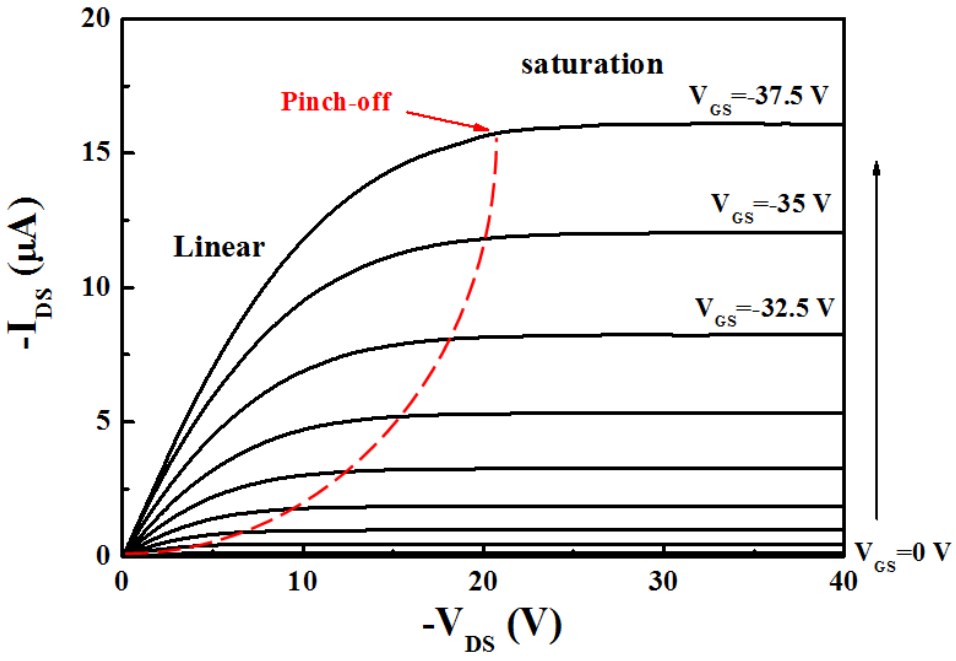

Figure 2.16: *Output characteristics for a typical OTFT based on a p-type semiconductor. The dashed line indicates where the channel of the OTFT becomes pinched-off.*

$$I_{DS(lin)} = \frac{WC_i}{L}\mu[V_{GS} - V_T]V_{DS} \qquad (2.16)$$

where C_i is the insulator capacitance per unit area, μ is the field-effect mobility, and V_T is the threshold voltage, which is defined as the value of the gate source voltage that required for the transistor to switched on, i.e. when a conductive channel forms at the semiconductor surface [49]. In an ideal transistor, the V_T equals 0 V, but because of the presence of dopants or traps it can differ from this ideal value.

In the saturation region, at high V_{DS} values ($V_{DS} > V_{GS} - V_T$), the conductive channel becomes 'pinched-off' as the drain-source current saturates, where I_{DS} is independent

of V_{DS}, as shown in Figure 2.16. The saturated drain-source current, $I_{DS(sat)}$, is represented by [48]

$$I_{DS(sat)} = \frac{WC_i}{2L}\mu(V_{GS} - V_T)^2 \tag{2.17}$$

The field-effect mobility of an OTFT in the linear regime, μ_{lin}, is typically calculated from the transconductance, $\boldsymbol{g_m}$, which gives from the derivative of Equation 2.16 [48];

$$\boldsymbol{g_m = \left[\frac{\delta I_{DS}}{\delta V_{GS}}\right]_{V_{DS=const.}} = \frac{WC_i}{L}\mu_{lin}V_{DS}} \tag{2.18}$$

The field-effect mobility in the saturation regime, μ_{sat}, can be estimated from rewriting Equation 2.17 as

$$\boldsymbol{\frac{(I_{DS})^{1/2}}{V_{GS} - V_T} = \left(\frac{WC_i\mu_{sat}}{2L}\right)^{1/2}} \tag{2.19}$$

Therefore, the value of μ_{sat} can be estimated from the slope of the plot of $(I_{DS(sat)})^{1/2}$ versus V_{GS} (black curve in Figure 2.17) known as the transfer characteristics. The device threshold voltage can be determined from the intercept on the voltage axis of this plot, as shown in Figure 2.17 (the red colour). In addition, from Figure (2.17), the plot of $I_{DS(sat)}$ on a logarithmic scale versus V_{GS} (blue curve) can be used to evaluate the ratio between the on-current and off-current (on/off current ratio, green colour in Figure 2.17), which is denote for the switching performance of the TFT. The other parameter is the subthreshold slope values (purple colour in Figure 2.17), which is indicating how fast the I_{DS} ramps up with the increase of V_{GS}.

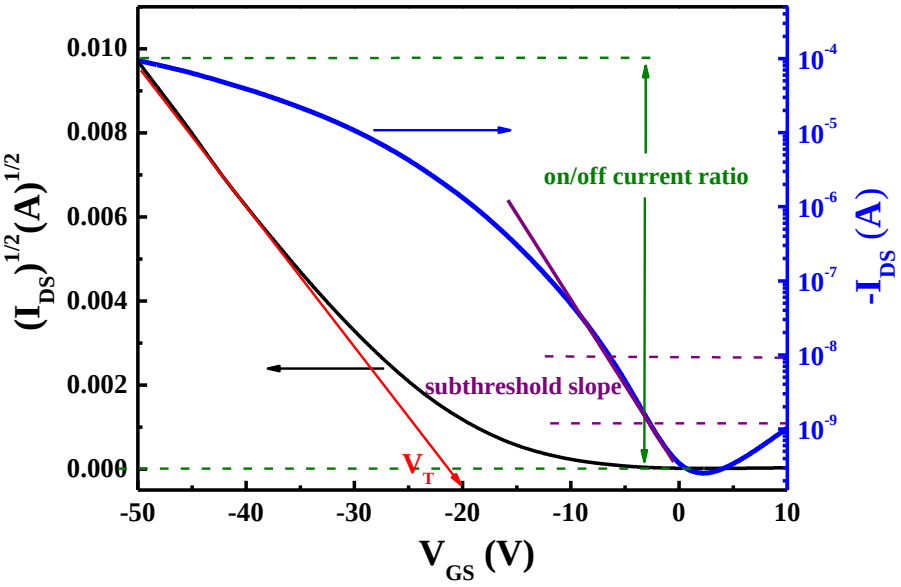

Figure 2.17: *Transfer characteristics for a typical OTFT based on a p-type semiconductor in the form of $I_{DS}^{1/2}$ (in the left axis) and I_{DS} on a logarithmic scale (in the right axis) versus V_{GS}.*

2.7 Organic non-volatile memory devices

In recent years, organic non-volatile memory (ONVM) devices became the main drive towards future flexible, light-weight, and low-cost electronics [50-52]. As example for such NVM devices are flash memories, optical disks, and floppy disks devices. ONVM devices based on OMIS and OTFT structures with floating gate are one of the key components to achieve those features due to their data storage and capability to integrate data processing. Particularly, nano-floating gate memories based on transistor structure proved to have fast switching speed, large memory window, and long retention time [53-60].

NVM consists of two main categories: (a) floating gate memory, which is differs from the conventional devices (such as MIS and TFTs) by adding thin layer of nanoparicles within the device insulator, and (b) charge-trapping, where there is extra memory stack between the original dielectric and the metal gate. The later type hold for all integrated devices, i.e. transistors, capacitors, resistors, and inductors. In this section we will give

an overview on ONVM and specifically on floating gate memories based on MIS capacitor and TFT structures.

2.7.1 Floating gate memories

It is worth mentioning that more than 90% of NVM production is based on floating gate principle [61]. Figure 2.18 shows the basic structure for nonvolatile floating gate memory based on structures of (a) metal-insulator-semiconductor (MIS), and (b) thin-film transistor. These devices are modified MIS and TFTs, where the new structures have a semi-permanent charge storage as an internal gate which is called a 'floating gate', as shown in Figure 2.18. Therefore, the internal gate acts as a memory cell, where the data stored in the form of accumulated electric charges dependence on the voltage that applied to the external gate. The external gate is the element which controls the flow the charge carriers to or from of the floating gate.

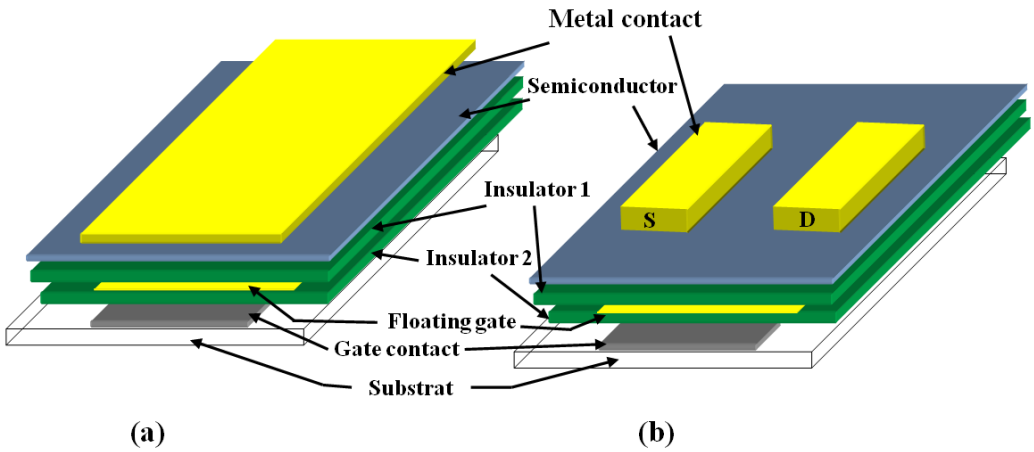

Figure 2.18: *Basic floating gate memory devices based on (a) MIS, (b) TFT devices.*

ONVM devices based on OTFTs are especially attractive to organic electronics, due to the possibility to read without destruction of their memory state ("non-destructive read-out"). Furthermore, they can be fabricated in the same production line as OTFTs

in any integrated circuit. In addition, integration with OTFTs settles the issue of the sneak current, which happens mostly in a passive crossbar array of memory elements [53, 62]. In the floating gate memory based on TFTs, the charges are stored in a metal layer which is completely surrounded by insulating layer. When a sufficient gate voltage, V_G, is applied, charges are injected into the floating gate from the transistor channel, lead to a shift in the threshold voltage, V_T. On the other hand, the discharge of the stored charges in the floating gate occurs when a reverse polarity V_G is applied [63].

The first nonvolatile floating gate memory device was introduced in 1967 by Kahng and Sze [64]. This memory device was based on an n-type semiconductor of metal oxide semiconductor field effect transistor (MOSFET). The energy band diagram of this memory device is shown in Figure 2.19; there are two insulators: insulator 1 (I_1) and 2 (I_2), I_1 with thickness of d_1 separating the semiconductor and the floating metal gate (FG), I_2 with thickness of d_2 between the FG and the external metal gate (G). When a positive gate voltage, $V_G > 0$, is applied to the external metal gate, an electric field, E, is developed in both insulators (Figure 2.19 (a)). In this case, the device is in accumulation mode, where the conduction band in the semiconductor bends downward and lets electrons to be moved through I_1 into the FG. Generally, the current through the insulators is mightily dependent on the electric field, and is more probably to be commanded by Fowler-Nordheim tunnelling. Now, by application of Gauss's law [65],

$$\varepsilon_1 E_1 = \varepsilon_2 E_2 + Q \tag{2.20}$$

and

$$V_G = V_1 + V_2 = d_1 E_1 + d_2 E_2 \tag{2.21}$$

where ε_1 and ε_2 are the absolute permittivities of insulator 1 and 2, E_1 and E_2 are the electric fields across these two insulators, and Q is the stored charge in the floating gate (write step). V_1 and V_2 are the voltages that formed across the two insulators. By solving the equations 2.20 and 2.21, we can satisfy the relation for the electric field across one of the insulators; for example, the E_1 in I_1 is given by:

$$E_1 = \frac{V_G}{d_1 + d_2\left({}^{\varepsilon_1}/_{\varepsilon_2}\right)} + \frac{Q}{\varepsilon_1 + \varepsilon_2\left({}^{d_1}/_{d_2}\right)}. \qquad (2.22)$$

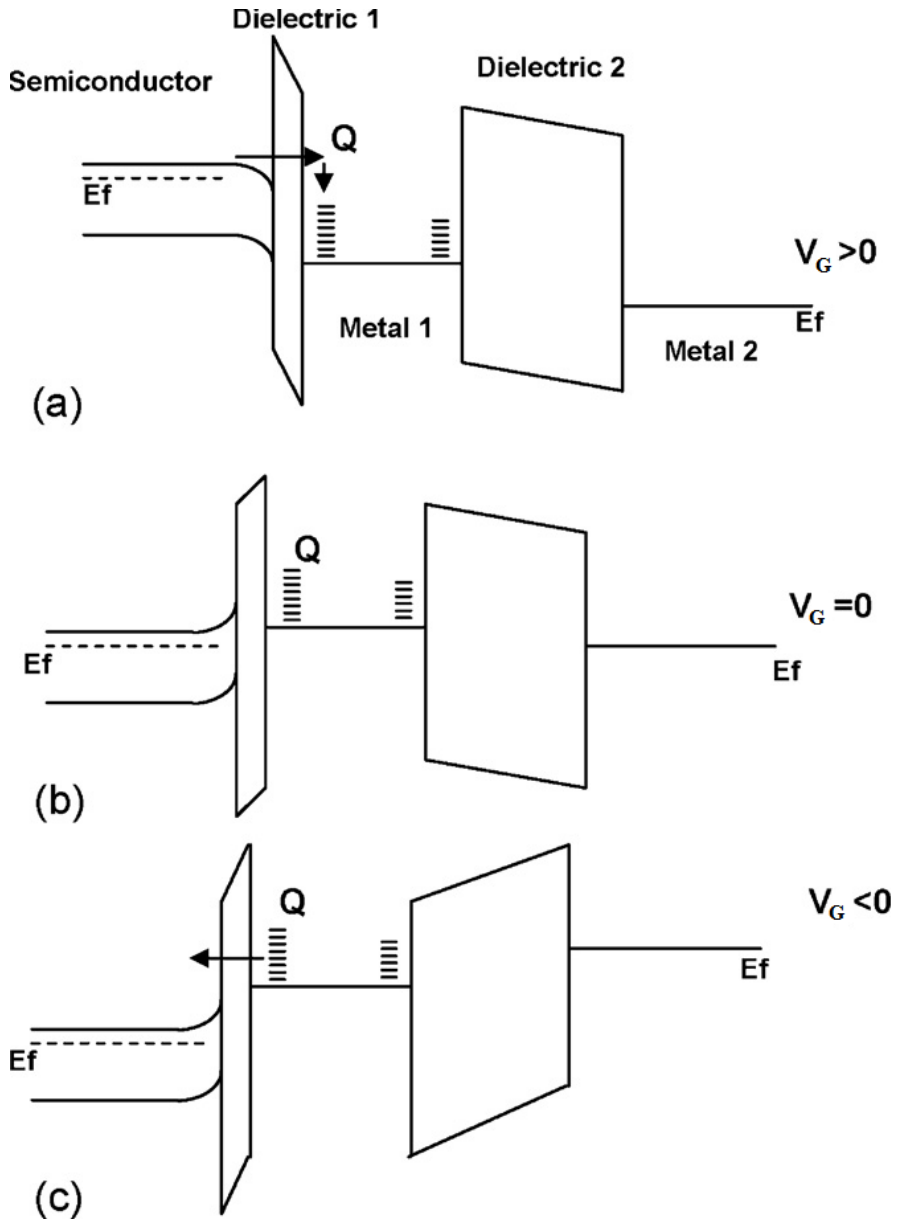

Figure 2.19: *Energy band structures of floating gate-based memory device under different gate voltages (a) $V_G > 0$, (b) $V_G = 0$, and (c) $V_G < 0$ [65].*

Pending the process of the application of V_G, the charge on the floating gate varies with time, as long as the currents in the two insulators are different, so it can give [61],

$$Q(t) = \int_0^t [J_1(E_1) - J_2(E_2)]dt \tag{2.23}$$

where *Q(t)* is the stored charge as a function of time *t*, J_1 and J_2 are the current densities in the two insulators. If the charge transport through the insulator is by Fowler–Nordheim tunnelling, the *J* is given as:

$$J = C_1 E^2 exp\left(-\frac{E_0}{E}\right) \tag{2.24}$$

where C_1 and E_0 are constants [64].

From this point, the current density can be used to calculate the stored charge *Q*. After time *t*, when the external voltage, V_G, is removed (Figure 2.19 (b)), assuming that $d_2 >> d_1$, *Q* leads to a shift in the threshold voltage by an amount ΔV_T which is given by [61];

$$\Delta V_T = -\frac{d_2 Q}{\varepsilon_2}. \tag{2.25}$$

By applying a negative V_G ($V_G < 0$, as shown in Figure 2.19 (c)), the erase step will happen, where the stored electrons in the floating gate will be discharged. For high enough negative V_G, surplus electrons can be removed from the floating gate leaving it with a positive charge.

2.7.2 Characterisation of floating gate memory devices

2.7.2.1 Write/Erase processes

Among the qualities that should characterise memory cells is that can store the information autonomously of the external conditions and can changed from one state to the other (from “programmed, 0” to “erased, 1”), provided that the conductivity of

the device can be changed in a non-destructive manner [61]. In other words; the magnitude of change in threshold voltage, V_T, from a high to low state, i.e. from programme "0" to erase "1" state, depends on the amount of stored or removed charges in or from the floating gate, respectively [61]. This for the floating gate memories based on n-type channel semiconductor, while in p-type channel the reverse is happens.

The write and erase processes for a floating gate memory device can be presented by plotting the transfer characteristics of the transistor; the drain-source current (I_{DS}) versus of gate-source voltage (V_{GS}) at constant drain-source voltage (V_{DS}) as shown in Figure 2.20; for (a) p-type, and (b) n-type channel semiconductor. It is clear from Figure 2.20 that the threshold voltage, V_T, is shifted from the initial device state to the charged floating gate state. The shift in V_T represents the memory window, which signifies the ability of memory devices to storage charges. Within this window, there are two different states of current; a high current ($I_{DS} >> 1$) and a low current ($I_{DS} = 0$), representing the logic data "1" for write and "0" for erase of the p-type channel *FG* memory [53] (Figure 2.20(a)), respectively. The situation is reversed for the n-type channel *FG* memory as shown in Figure 2.20(b). The "read" process is proceeded by applying a V_G that is between the values of programmed and erased V_T and valuing the current flowing through the device [61].

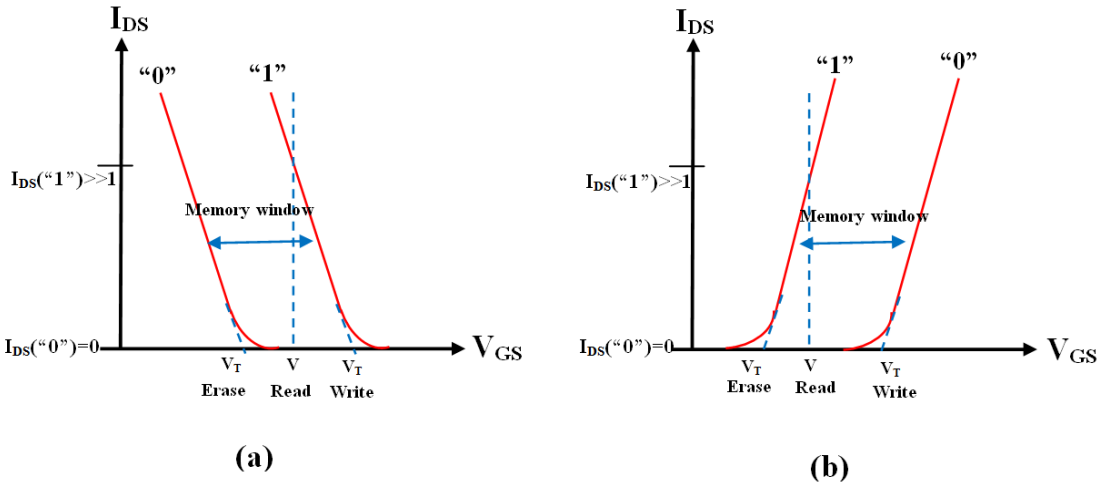

Figure 2.20: *The write and erase operations for a floating gate memory device based on TFTs, (a) for a p-type, and (b) for an n-type channel semiconductor (adapted from Heremans [53]).*

For the floating gate memory devices based on MIS capacitor structure, the shifting of V_T manifests itself as a shift in the flatband voltage (V_{FB}) of the capacitance-voltage (C-V) characteristics. The shift in V_{FB} depends on the polarity of the charges, positive (Q_p) or negative charges (Q_n), that existing in the *FG*. Figure 2.21 shows the shift in *C-V* plot for a p-type *FG* memory based on MIS structure at high frequency when (a) holes and (b) electrons are accumulated in the *FG*.

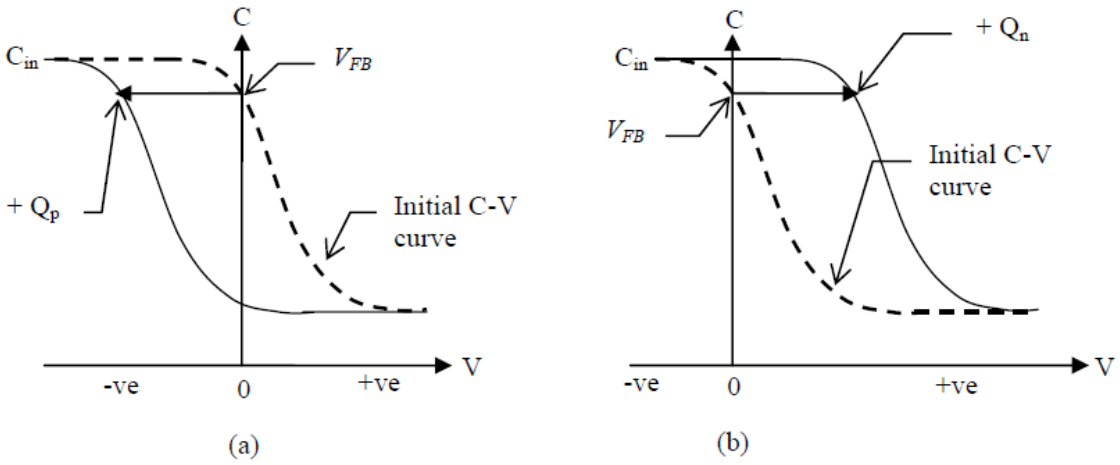

Figure 2.21: *Typical C-V characteristics of MIS-based memory structure with (a) positive charge, Q_p, and (b) negative charge Q_n in the floating gate (adapted from Sze [65]).*

2.7.2.2 Retention properties

Retention is a time value that a non-volatile memory cell can save the charge in the floating gate whether it is powered or not. The stored charge in the floating gate of memories may leak away through the external gate or through the insulator because of the gate defects and mobile ions [66]. Various mechanisms for charge loss have been described [66-68], such as charge loss due to electron detrapping, or due to thermionic emission, or due to contamination. On the other hand, there are different methods to

improve the retention features of memory cells, for example, the improvements of the quality of the gate and dielectric materials [68].

Retention can be measured by estimating the time it takes to unload the information stored in floating gate. As the charge loss is occur, the threshold voltage of the memory cell will be shift depending on the following equation [67],

$$dQ_{FG} = C_{FG}\, dV_T \tag{2.26}$$

Where dQ_{FG} is the charge loss of the floating gate, C_{FG} is the capacitance of floating gate, and dV_T is the floating gate threshold voltage shift.

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Chapter 3

Materials and Experimental Techniques

3.1 Introduction

This chapter includes an overview of the materials and experimental techniques used during this research. The nature of the materials and the required properties of the device determined the choice of process used in the work. For instance, thermal evaporation was used for the deposition of small molecules films, whilst the technique of spin-coating, in most cases, was used for the deposition of polymer materials. To minimise atmospheric contamination, the fabrication of all devices were conducted in a class 1000 clean room (no more than 1000 particles $\geq 0.5\ \mu m$ per cubic foot of air).

Although the research in this thesis involves the fabrication of different types of devices with different materials, i.e. metal-insulator-semiconductor (MIS) capacitors, MIS memory devices, thin film transistors (TFTs) and thin film memory transistors (TFMTs), most of the experimental techniques were similar. In this chapter, Section 3.2 describes all the materials used in this research. The main techniques of film deposition that have been used are explained in Section 3.3. The description of the general experimental details for the fabrication of devices can be found in Section 3.4, including the preparation of polymers and gold nanoparticles (AuNPs) solutions. However, the detailed experimental techniques for fabrication of any device will be described in the main section about that device. The atomic force microscopy (AFM) used to describe the morphology surfaces of films are found in Section 3.5. Finally, the electrical characteristics measurements setups are summarised in Section 3.6.

3.2 Materials

The following materials were purchased from Sigma Aldrich: 3-aminopropyl-trimethoxysilane (APTMS), NaBH4 (99.99%), HAuCl4.3H2O (99.9%), sodium citrate, PMMA (molecular weight 93,000), and pentacene.

3.2.1 Pentacene

The organic semiconductor material selected for this study is pentacene. Pentacene is one of the polycyclic aromatic hydrocarbons consists of five linearly benzene rings. This compound is sensitive to oxidation and slowly degrades when exposed to air and light [1, 2]. The principal molecular structure of pentacene is shown in Figure 3.1.

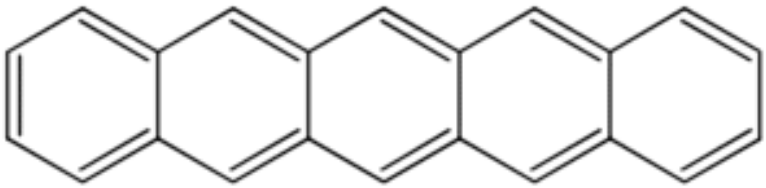

Figure 3.1: *Structure of a pentacene molecule.*

Pentacene is a p-type small molecule organic semiconductor with high electrical conductivity of about 0.1 ohm-cm under high pressure, at room temperature. However, it has insulating properties under ambient pressure [3]. Interest in pentacene increased when the successful performance of OTFT devices was reported in 1990s [4, 5]. That initiated a considerable potential for the use of pentacene as the active layer in TFTs for a variety of electronic circuits. Since then, pentacene has become one of the main materials studied intensively and widely as a promising material with high field-effect mobility. A mobility of 0.002 $cm^2\ V^{-1}\ s^{-1}$ for pentacene-based TFTs fabricated on a doped silicon substrate was reported by Horowitz *et al* in 1991 [6]. Scientists in the chemistry side of engineering have modified the structure of pentacene and produced advanced organic semiconductors based on pentacene and that improved the mobility of TFTs dramatically to more than 1 $cm^2\ V^{-1}\ s^{-1}$ in 1996–1997 [7–10]. Then the

mobility of pentacene TFTs gradually increased to 3.0 in 2002 [11], 3.3 in 2003 [12] and 5.5 $cm^2 V^{-1} s^{-1}$ in 2006 [13], which exceeds that of amorphous silicon. It has been shown that the high performance of TFT devices is attributed to the structural perfection on pentacene film: increased intermolecular packing, morphology surface and the properties of the interface between the gate dielectric and pentacene layer [14-16]. Thus, the factors responsible for high performance of the transistor device will be reported in this thesis.

3.2.2 Poly (methyl methacrylate) (PMMA)

One of the most common plastic materials in organic electronics is Poly (methyl methacrylate) PMMA, which was the first polymer to be used in 1933 as the gate dielectric by the German chemist Otto Röhm [17]. There are many features that have made PMMA a potential candidate as the dielectric layer in OTFTs, especially the high resistivity (more than 2×10^{15} $\Omega\ cm$) and low dielectric constant (approximately 3) [18, 19]. In addition, PMMA contains hydrophobic methyl radical group, which is very important as on inhibitor of moisture [20].

PMMA is formed by polymerization of fine droplets of methyl methacrylate (MMA) in water under the influence of free-radical initiators, so PMMA is the synthetic polymer of MMA [19]. The molecular structure of PMMA is shown in Figure 3.2. In this study, PMMA was the main organic insulator used as the gate dielectric layer in MIS, TFTs and memory structures.

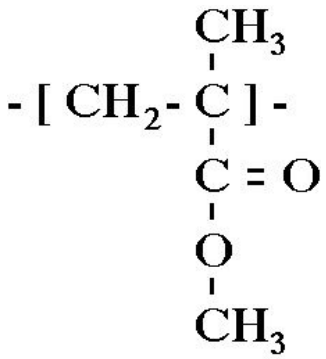

Figure 3.2: *Molecular structure of Poly(methyl methacrylate) (PMMA).*

3.2.3 Poly(vinyl phenol) (PVP)

The polymer Poly(vinyl phenol) (PVP) is available in several viscosity grades as a powder or liquid. These viscosity grades (low or high molecular weight), and the fact that it easily dissolves in aqueous and organic solvent, gives PVP great flexibility. This polymer is widely used as a dielectric layer deposited on organic semiconductors. In addition, the robustness of this polymer can be enhanced by cross-linking, using chemical materials like hexamethylene tetraamine or melamine-co-formaldehyde. The molecular structure of PVP is shown in Figure 3.3.

High capacitance and low leakage currents are the results of using PVP as the gate insulator in OTFT devices [21-24]. Furthermore, the low surface energy of PVP made it one of the most suitable candidates as a dielectric layer for the growth of pentacene film. This is because the morphology of the pentacene surface is dependent on the surface energy of the film it deposited on [11, 25]. Because of those encouraging properties of PVP, this organic polymer was one of the insulating materials chosen to fabricate different devices in this study.

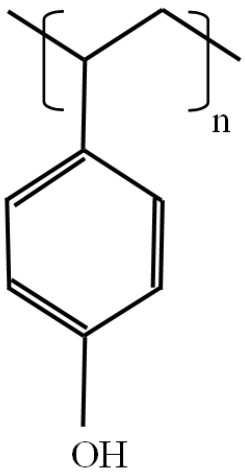

Figure 3.3: *Molecular structure of Poly(vinyl phenol) (PVP).*

3.2.4 Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS)

Besides gold being used as the metal contact in this study, another conducting material, Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) or PEDOT:PSS, was used, too. PEDOT:PSS is a single component polymer consisting of two ionomers as shown in Figure 3.4. First component of that mixture, PEDOT, is a polymer based on polythiophene carrying positive charges. The other component, PSS, is a polymer made up of sodium polystyrene sulfonate with negative charge [26, 27].

PEDOT: PSS is a conducting polymer which has high electrical conductivity reaching to 500 S/cm. It is used in OTFTs and organic light-emitting diode devices [28, 29]. Furthermore, PEDOT: PSS has good chemical and thermal stability [30, 31].

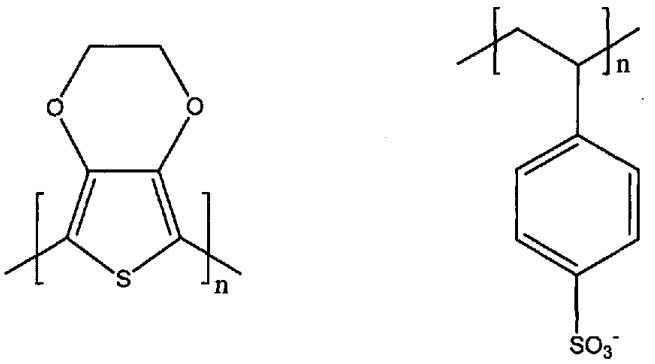

Figure 3.4: *Molecular structure of PEDOT: PSS.*

3.2.5 Gold nanoparticles (AuNPs)

Gold nanoparticles, are defined as sub-micrometer-sized particles of gold dispersed in a fluid, usually water. These special gold nanoparticles are known since ancient times [32]. In 1850s, scientists had focused their full attention on these nanoparticles to

understand the reasons of their extraordinary properties, e.g. electronic, optical, low toxicity, and molecular-recognition properties. Such properties allow for the gold nanoparticles to be attractive in a range of applications, including nanotechnology, electronics, and materials science [32].

Usually, a synthetic method for creating AuNPs are achieved by treating hydrogen tetrachloroaurate ($HAuCl_4$) with citric acid in boiling water, where the solution is rapidly stirred while a reducing agent (citric acid) is added; this causes Au^{3+} ions to be reduced to neutral gold atoms. Next, the solution becomes supersaturated as the result of more of these gold atoms form, and gold gradually starts to precipitate in the form of sub-nanometre particles [32-34]. The important factor in the production of AuNPs is the stirrer process of the AuNPs solution should be vigorously enough for the fairly uniform in size these particles [34].

The deposition methods of gold nanoparticles are dependent on application. Generally, there are two main approaches have been used for depositing nanoparticles. The first approach is top-down via deposition of sputtered or evaporated metal from vacuum to a polymer matrix [35], or to a substrate [36, 37]. Bottom-up was the second approach of nanoparticles deposition via self-assembly [38, 39], "soft" lithography stamping [40], sol-gel coating [41, 42], or adsorption of nanoparticles onto oppositely charged substrates [43, 44].

In our study, the main method of nanoparticles deposition, self-assembly, have been used for the deposition AuNPs as floating gates for OMIS and OTFT based memory structures. The method of deposition of AuNPs that used in this study, in addition to the preparation method will explain later in detail.

3.2.6 Single walled carbon nanotubes (SWCNTs)

Carbon nanotubes (CNTs) are graphite crystals with a cylindrical nanostructure. They were discovered in 1991 by Iijima of NEC Corporation [45]. Monolayer or multilayer flakes of graphite are components of CNTs, where according to a certain spiral angle these components surround the centre shaft in the cylindrical tube [46, 47]. This rolling angle and the radius of carbon molecules determine the nanotube properties; for instance, whether the individual nanotube is a semiconductor or of a metallic nature

[46-49]. Carbon nanotubes are classified as single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs) as shown in Figure 3.5.

Single-walled carbon nanotubes are considered as rolled-up into a one-atom-thick layer of graphite along a chiral vector in the cylindrical form, while Multi-walled carbon nanotubes consist of multiple rolled layers of graphene. The diameter of SWCNTs is about one nanometer and many millions of times longer in length [47]. The way the SWCNT is wrapped is determined by its chiral vector C_h [47];

$$C_h = na_1 + ma_2 \qquad (3.1)$$

where the indices chiral n and m are the number of unit vectors (a_1 and a_2) in the honeycomb structure of the graphene sheet along two directions. If $m = 0$, the nanotube is referred to as a zigzag nanotube as in Figure 3.6. If $n = m$, the nanotube is called an armchair nanotube. Any other vector leading to a tube is called a chiral [46-48].

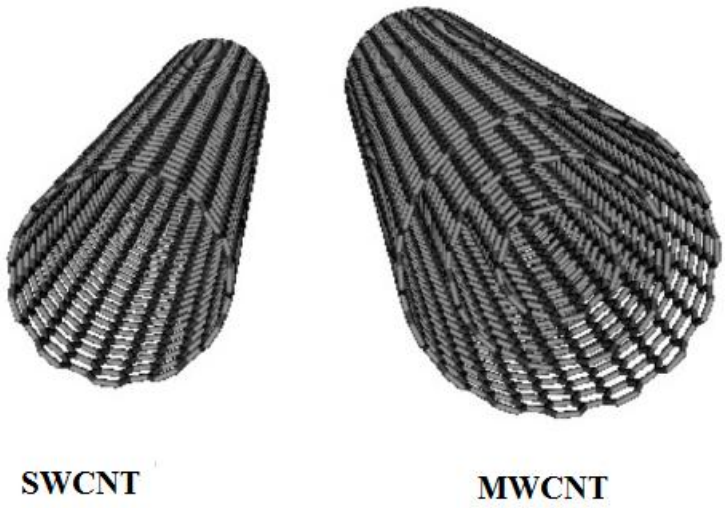

Figure 3.5: *Molecular structure of a SWCNT and a MWCNT [47].*

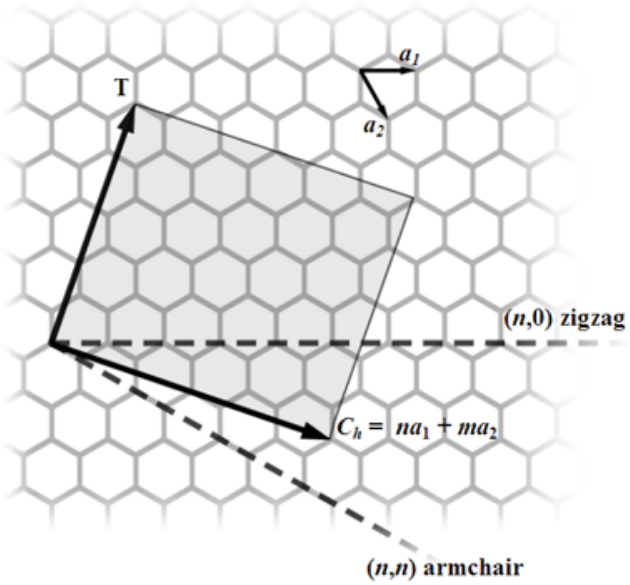

Figure 3.6: *The (n, m) nanotube naming scheme of a chiral vector (C_h) in the honeycomb graphene sheet of SWCNT. T denotes the tube axis, and a_1 and a_2 are the unit vectors of graphene in real space [49].*

One of the important applications of SWCNTs was in the improvement of the first intermolecular ordering of thin film transistors, where, in 2001; the logic gate using SWCNT TFTs was made [49].

3.3 Experimental techniques

3.3.1 Thermal evaporation

The physical vapour depositions of metal (Al gate and Au contacts in our fabrication) and organic materials (pentacene) were conducted by thermal evaporation using a Kurt. J. Lesker mini-spectros system as shown in Figure 3.7. The electrical energy in this technique was used to heat a filament and that led to heating a deposition material

to evaporation point. This vapour material condensed in the form of a thin film on the cold substrate surface, while a shadow mask was used to create a pattern of the thin film. Very high levels of vacuum, about 10^{-4} Torr, were required in this process to allow for a long mean free path to reduce film impurities. However, low pressures were usually used, about 1 x 10^{-7} Torr, to prevent reaction between the vaporized materials and the atmosphere. The depositing of two organic sources at the same time was possible in the Kurt. J. Lesker spectres with two individual sensors. Therefore, it was easy to monitor the evaporation rates of these two sources. Furthermore, in this technique, the film thickness was monitored by quartz crystal sensor (QCS) [50] and the processes of film deposition were controlled by the Sigma software.

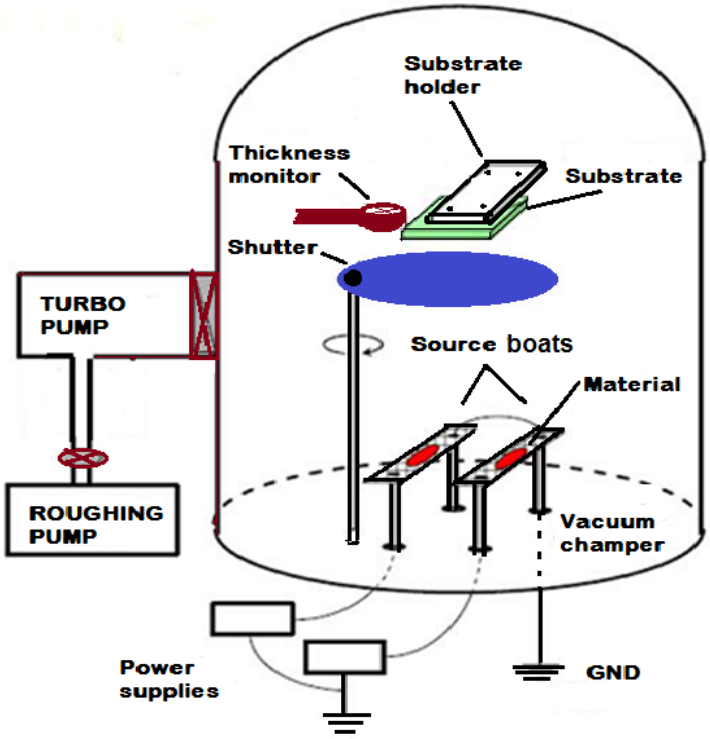

Figure 3.7: *Schematic diagram of a Kurt Lesker mini-spectros system.*

3.3.2 Spin coating

The spin coating technique has been used for deposition of thin films for several decades. This technique can be used for all kinds of solutions (generally polymers) on flat substrates, e.g. silicon wafers or glass slides. Usually the process involves applying a small amount of solution into the centre of the substrate, which is held by a vacuum chuck during the coating process. Then the substrate starts to rotate at a fixed speed, typically about several thousand rpm. The solution is applied continuously and spreads outwards as the substrate is rotating. The coating process is shown in Figure 3.8. Equation 3.2 shows the theoretical model for the spin coating process;

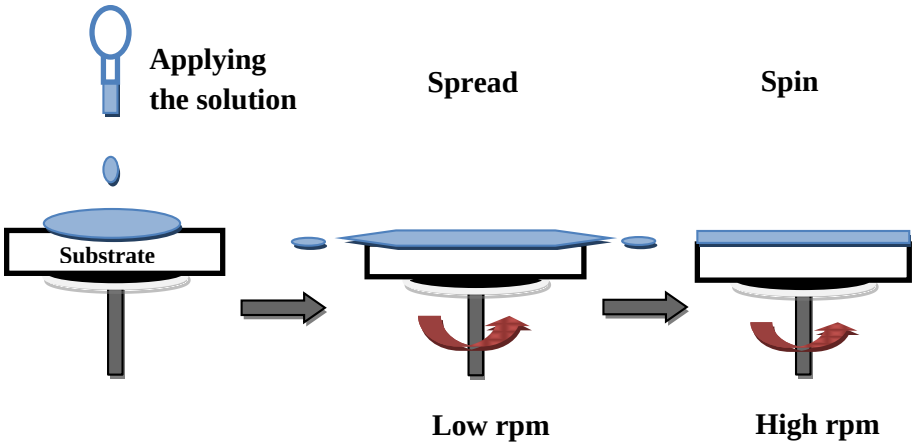

Figure 3.8: *Schematic diagram of spin coating process.*

$$d = \left(\frac{\eta}{4\pi\rho\omega^2}\right)^{\frac{1}{2}}\left(\frac{1}{t}\right)^{\frac{1}{2}} \qquad (3.2)$$

where d is the thickness of the spun film, η is the viscosity coefficient of the solution and ρ is its density with the angular velocity of the spinning ω at the spinning time t [51]. It is useful to say that the final film thickness depends on a variety of factors, such as the drying rate (temperature per minute), viscosity, surface tension,

concentration of solids, etc. Furthermore, the choice of the speed plays a major role in determining the film thickness.

3.3.3 Self-Assembly

Self-assembly is defined as the spontaneous organization of molecules into ordered structures by the interactions. These interactions are responsible for the formation of monolayers on a prepared substrate after they have been immersed into a solution of surface-active material [52]. As a deeper explanation of this process, the self-assembly monolayers (SAMs) are created by a head group, tail and functional group molecules, as shown in Figure 3.9. This process is driven by strong interactions between the substrate and the head group of the self-assembling molecule, followed by a slow organization of tail group molecules. The result is a chemical bond between the specific surface site and the head group for building the nanostructure [53].

The SAMs processes are often allowed to form for a time period from minutes to 72 hours at room temperature. The structure of SAMs and its other properties, such as conductance, chemical functionality, surface charge and magnetic properties, are commonly defined using scanning probe microscopy techniques (SEM) and atomic force microscopy (AFM) [54].

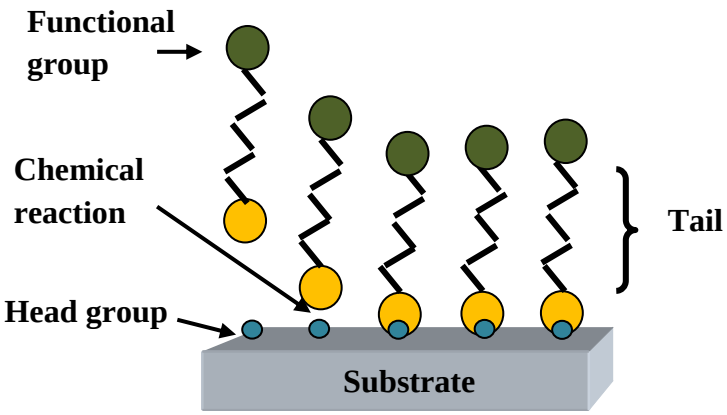

Figure 3.9: *Representation of a Self- assembly monolayer (SAM) structure.*

3.3.4 Layer-by-layer deposition

The Layer-by-Layer (LbL) deposition method is the most versatile thin film fabrication technique today. The films are formed by depositing positively and negatively charged layers of materials, successively, on the surface charge after the adsorption of each layer [55]. This process is performed by consecutive dipping of a charged substrate (for example, silicon, glass and plastics) in inversely charged polyanion and polycation solutions to form an assortment of species one monolayer at a time [43]. This deposition method is simple, cheap and it has several advantages, such as charge-charge interaction between substrate and monolayers to create multiple layers held together by electrostatic forces.

There are a variety of materials that can be used for layer-by-layer deposition, such as nanoparticles, ceramics, biological molecules and metals. Furthermore, the high degree of control over thickness is another important feature of LbL. Each layer of linear growth of the films contribute a known increase in thickness to form a number of bilayers [57].

There are many applications for the LbL deposition method in biomedicine, corrosion control, and many more [55-57]. The use of cationic and anionic nanotubes surfactants makes it possible to be used for the preparation of thin films [55]. For our study this technique was used for the deposition of SWCNT films as floating gates in organic memory devices.

3.4 Experimental details

3.4.1 Substrate preparation

Two sizes of glass substrates were used for fabricating devices during this study. The first size was 12 *mm* x 12 *mm* square, using two different shadow masks A and B, as shown in Figure 3.10. Each of these substrate slides had four devices. The second size used was 25 *mm* x 25 *mm* square, with six devices on shadow mask C, as shown in Figure 3.10. An EC-400 dicer (MTI Corporation) was used to cut the substrate slides into these sizes.

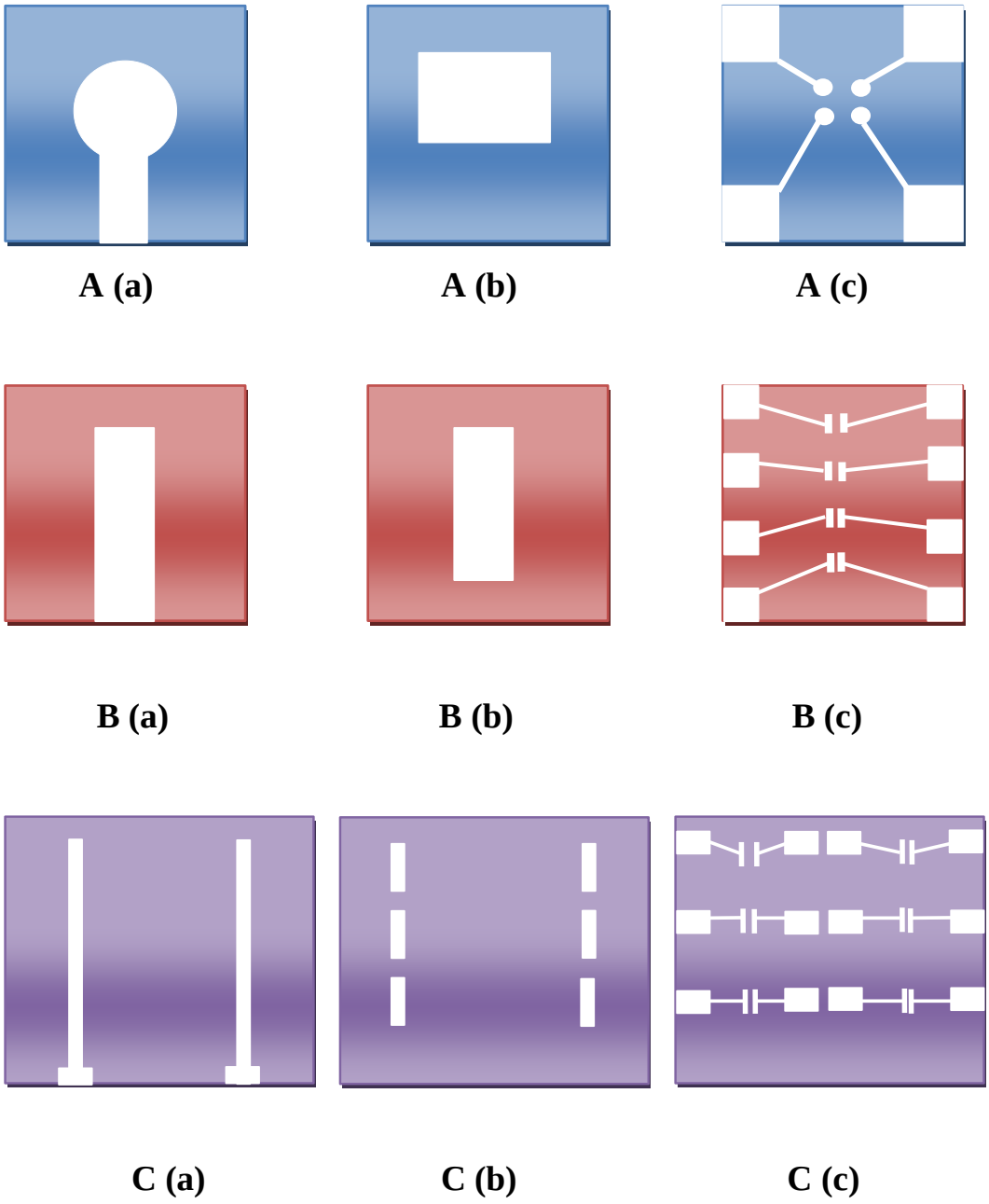

Figure 3.10: *The three types of shadow mask A, B and C for (a) gate contacts, (b) semiconductor layer, A (c) the MIS contact and B (c), C (c) source/drain contacts.*

First, substrates were cleaned by hand with hot water to remove any contamination caused by using the dicer. Then, they were cleaned with Decon 90 and rinsed in De-Ionised (DI) water. For further cleaning, the steps below were followed (Table 3.1) after the substrates were placed on a glass holder.

Table 3.1: *Cleaning process of glass substrates.*

Stage	Number of Times	Solution	Detail
1	1	2% Decon 90 in DI water	Ultrasonicate for 5 mins at 40 °C
2	2	DI water	Ultrasonicate for 5 mins at 40 °C
3	2	Acetone	Ultrasonicate for 3 mins at 40 °C
4	2	Methanol	Ultrasonicate for 3 mins at 40 °C
5	2	2-Propanol	Boiling for 3 mins
6	1	-	O_2 Plasma for 5 mins

3.4.2 Film deposition

3.4.2.1 Metal gate evaporation

An aluminium bottom gate electrode was deposited by thermal evaporation at room temperature, using Kurt. J. Lesker evaporation system, explained in Section 3.3.1. To maintain cleanliness of the substrates, immediately after the cleaning process, all slides were placed into the substrate holder of the chamber. 50-70 *nm* thickness of aluminium film was deposited through a shadow mask (Figure 3.10 (a)) onto the clean glass substrates at a rate of 0.1 $nm\ s^{-1}$. After this stage of the fabrication, the substrates were ready for deposition of the second film, which was the insulating layer.

3.4.2.2 Spin coating of the insulator

In this study, the spin coating process, described in Section 3.3.2, was used to deposit the gate dielectric layers of poly(methyl methacrylate) (PMMA) and Poly(vinyl phenol) (PVP). The EMS spin coater model 4000 was used in this process. 10% (wt) concentrations of PMMA/Anisole solution were prepared at least 48 hours (on the stirrer) in advance of the film deposition process. However, 24 hours was enough to desolve 25% (wt) concentration of PVP/2-propanol solution before film deposition. For dropping the solution (PMMA or PVP) onto the substrate, a disposable glass pipette was used for both materials.

To form the PMMA film, the first spin speed was 500 *rpm* for 10 seconds. This speed was to ensure the solution was spread on the substrate. Then a higher spin speed of 3000-5000 *rpm* for 50 seconds, was used to control the film thickness. Immediately after spin-coating, the substrates were cured at 120 °C on a hot plate for one hour. The same spin speeds and time conditions of PMMA film deposition were used to form PVP film. For the curing process, 60-80 °C was used to bake spun PVP film for 10 minutes. Finally, the substrates were kept under vacuum after the films were examined with an optical microscope to make sure there are no pin holes or any contamination.

3.4.2.3 Floating gates deposition

Thin layer of gold, gold nanoparticles (AuNPs) and single walled carbon nanotubes (SWCNTs) were used as floating gates to fabricate two different types of memory devices, MIS and transistor memory structures. The only difference in fabrication of these memory devices from MIS capacitor or transistor devices was the deposition of a floating gate material sandwiched between two insulating (PMMA or PVP) films.

(a) Gold nanoparticles preparation and deposition

The first kind of floating gate used in this study was formed by evaporating a 10 *nm* thin film of gold layer as a sandwich between two layers of insulators.

However, the method of self-assembled monolayers was used for the deposition of a second kind of floating gat, gold nanoparticle. All laboratory tools, i.e. glassware, syringe, tweezers, and any others which were used in the processes of preparation or deposition of AuNPs solution, were deep cleaned with acetone, 2-propanol and methanol solvents as well as Decon90 and DI Water. The process of preparing AuNPs solution involved adding 1 *ml* of 1% aqueous solution of gold chloride ($HAuCl_4.3H_2O$) to 100 *ml* of deionised water under vigorous stirring. Then, 1 *ml* of 1% aqueous sodium citrate was added after 1 minute. This was followed by adding 1 *ml* of 0.075% sodium borohydride ($NaBH_4$) in 1% sodium citrate 1 minute later. The next step was to stir the solution for a further 5 minutes and finally the solution was stored in the refrigerator at 4 °C. Figure 3.11 shows the AuNPs preparation steps.

To deposit the Au nanoparticles, 3-aminopropyltriethoxysilane (APTES, $C_6H_{17}NO_3Si$) was used as seed layer. In the first stage of deposition, the glass substrates were placed in a diluted solution of APTMS (1 *ml* of APTMS in 10 *ml* methanol) for 2-3 hours for devices based on PMMA and PVP respectively. Then, the substrates were rinsed thoroughly with methanol, and immersed in the Au nanoparticles solution for 15 minutes and rinsed with water.

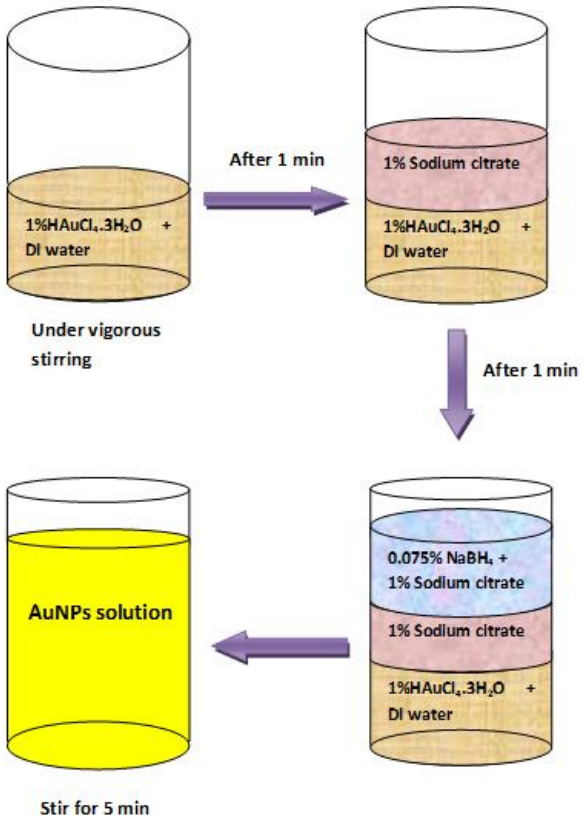

Figure 3.11: *Preparation steps of gold nanoparticles (AuNPs) solution.*

(b) SWCNTs deposition

The third type of floating gates used in this study, is three and five layers of single walled carbon nanotubes (SWCNTs). The preparation and deposition of SWCNTs were performed in collaboration with the School of Engineering at Durham University. Single walled carbon nanotubes were purchased from Carbon Nanotechnologies Inc. Before their integration into the memory devices, SWCNTs were purified until the metal content was below 5 wt %. In the purification process of the nanotubes, SWCNTs were subjected to a thermal oxidation for 90 min at 300 $^{\circ}$C, followed by stirring in a concentrated HCl bath overnight, before finally rinsing the nanotubes with deionized water until the pH of the solution is to that of deionized water and drying overnight at 120 °C. The SWCNTs were then subjected to a chemical cutting process using mild sonication in a mixture of H_2SO_4 and HNO_3 (in the ratio 1:1) for 3 h at 120

°C. The SWCNTs were separated by centrifugation and washed several times with deionized water and dried for 18 h. The cut SWCNTs were filtered using the 0.2 μm pore size polycarbonate membranes. At the end of the procedure SWCNTs of 200 nm or shorter were produced.

SWCNTs were deposited using layer-by-layer (LbL) technique which is a deposition technique based on a charge reversal to build up bi-layer assemblies of oppositely charged (functionalized) molecules utilizing electrostatic attraction, as explained in Section 3.3.4. The details of this technique and various film architectures built using SWCNTs are reported in our study [58] and elsewhere [59, 60]. Briefly, the deposition began by functionalizing the substrate by seeds layers, which facilitates the adhesion of SWCNTs onto the substrate. This was performed by the alternate immersion of the substrate in aqueous Poly(ethyleneimine) (PEI) (Mw=25000) (cationic, pH = 8.5) and Poly(acrylicacid) (PAA) (Mw=4000000) (anionic, pH = 6.5) solutions, for 15 min each. The substrate was then repeatedly immersed in PEI solution for 15 min then SWCNTs solution (anionic, functionalized SWCNTs dispersed in Sodium dodecyl sulphate (SDS) solution) for 30 min. After each immersion, the substrate was rinsed with deionized water and dried with nitrogen. The final SWCNTs matrix consisted of three SWCNTs - PEI bilayers. A schematic diagram of the LbL deposition is presented in Figure 3.12.

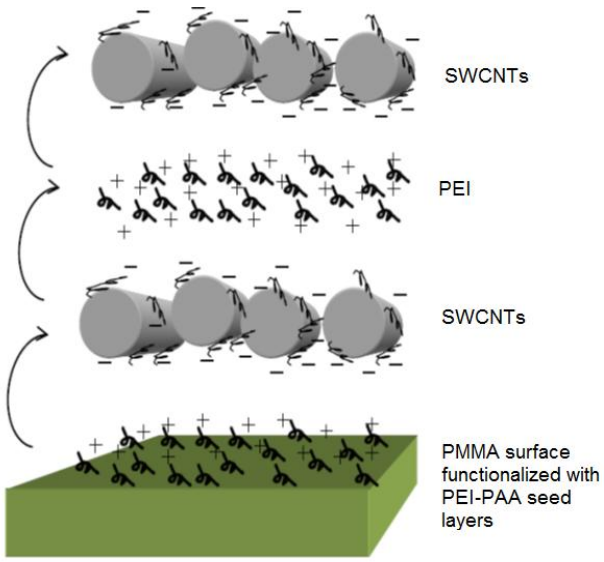

Figure 3.12: *A schematic diagram of the layer-by-layer SWCNTs deposition technique.*

3.4.2.4 Organic semiconductor evaporation

Pentacene was the organic semiconductor material used in this study as an active layer for all fabricated devices. Pentacene film formed on top of the dielectric layer through a shadow mask as shown in Figure 3.10 (b). Kurt. j. Lesker deposition system described in Section 3.3.1 was used for the deposition of the organic thin film. Although attempts were made with different evaporation rates (0.05, 0.03, 0.01 and 0.0015 *nm* s^{-1}) to deposit to 50 *nm* thickness of pentacene, the deposition rate of 0.03 *nm* s^{-1} was chosen as optimal. This choice depended on topographical images of the film surface which were taken by Atomic Force Microscope (AFM) technique. The performances of the devices were strongly associated with the surface morphology of pentacene, and the later mightily affected by the deposition rates.

3.4.2.5 Evaporation of metal contacts

Gold electrodes were deposited on the top of pentacene layer through a shadow mask shown in Figure 3.10 (c). The deposition thickness of the gold electrodes was 50-70 *nm*, with evaporation rate of 0.1 *nm* s^{-1} using the Kurt. J. Lesker deposition system. For TFTs and TFMTs, the source and drain were formed through the shadow mask shown in Figure 3.10 B (c) and C (c), with various channel lengths and widths. However, for the MIS capacitor structures the gold top-contacts were achieved without defining the source and drain, as shown in A (c) of Figure 3.10.

3.4.3 Thin film characterization

Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a high-resolution scanning probe microscopic technique used to help researchers to observe the surface morphology of thin films. In 1985, Binnig, Quate and Gerber were able to develop the atomic force microscope technique [61] in order to enable the study of materials and obtain images of a sample surface at a very high resolution. This technique has been used to analyze van der

Waals forces, lateral friction forces, repulsive forces and magnetic forces [62-63]. In this study, digital instrument nanoscope AFM was used to analyse the surface properties of pentacene and AuNPs thin films.

The images in this technique are obtained by scanning a sharp probe across the sample surface while the interactions of the sample and the tip are analyzed [62]. Usually the scanning process is achieved by placing the sharp tip of a microscopic cantilever close to the surface of the sample. There is an attractive force from the surface applied to the tip through the moving of the tip along the different features on the sample surface. The distance between the surface and tip is adjusted to keep the deflection of the cantilever constant, while the extremely small deflections of the cantilever will cause the cantilever to bend upwards. This bending is then measured by a laser spot reflected to the sensor. Subsequently an image of the surface can be recreated with resolution on the atomic level under ideal conditions based on the information collected by the sensor [63].

According to the interaction of the sample surface and the tip, AFM can be classified as contact or noncontact mode. Figure 3.13 shows the principle of atomic force microscopy in contact mode, where the tip has touched the sample surface. On the other hand, in the noncontact force mode the tip stays quite close to sample and does not touch it. The tip is vibrated, which these vibrations are closely related to the distance between the sample and the tip, a detection system with a laser measures the vibration and provides an electrical signal according to this tip-sample spacing [64].

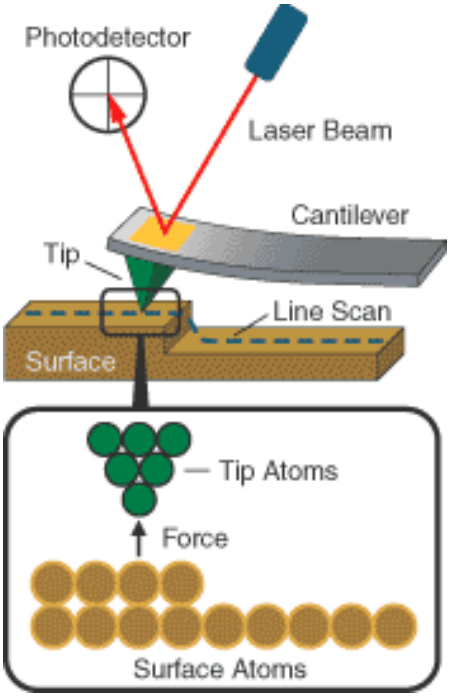

Figure 3.13: *Schematic diagram of atomic force microscopy (AFM) system [63].*

3.4.4 Electrical characterisation

3.4.4.1 AC measurements

Double sweep AC electrical characterisation in terms of capacitance–voltage (*C–V*) and capacitance-frequency (*C–f*) were performed for the MIS capacitors and memory devices at room temperature (21 ± 2 ◦C) using LCR bridge (HP4192). *C–V* measurements were achieved within the range of ± 40 *V* applied to the gate electrode with 1- 2 *V* steps at fixed frequencies within the range of 20 *Hz* to 1 *MHz*. As for the *C–f* measurements, the frequency sweep from 20 *Hz* to 1 MHz was performed at a fixed voltage using a signal of 1 *V*.

3.4.4.2 DC measurements

Double sweep current-voltage (*I-V*) characteristics of the TFTs and TFMTs were performed for both output and transfer characteristics at room temperature, using

Keithley 4140B picoammeter. A schematic diagram of the experimental setup is shown in Figure 3.14. The output characteristics were measured when applying a DC voltage to the gate electrode, and then the drain-source current (I_{DS}) was measured as a function of drain-source voltage (V_{DS}) at different gate voltages. For transfer characteristics, DC voltage was applied to the drain, and I_{DS} was measured as a function of gate-source voltage (V_{GS}) at constant V_{DS}. Figure 3.15 shows the sample holder used in this study for the electrical characterisations.

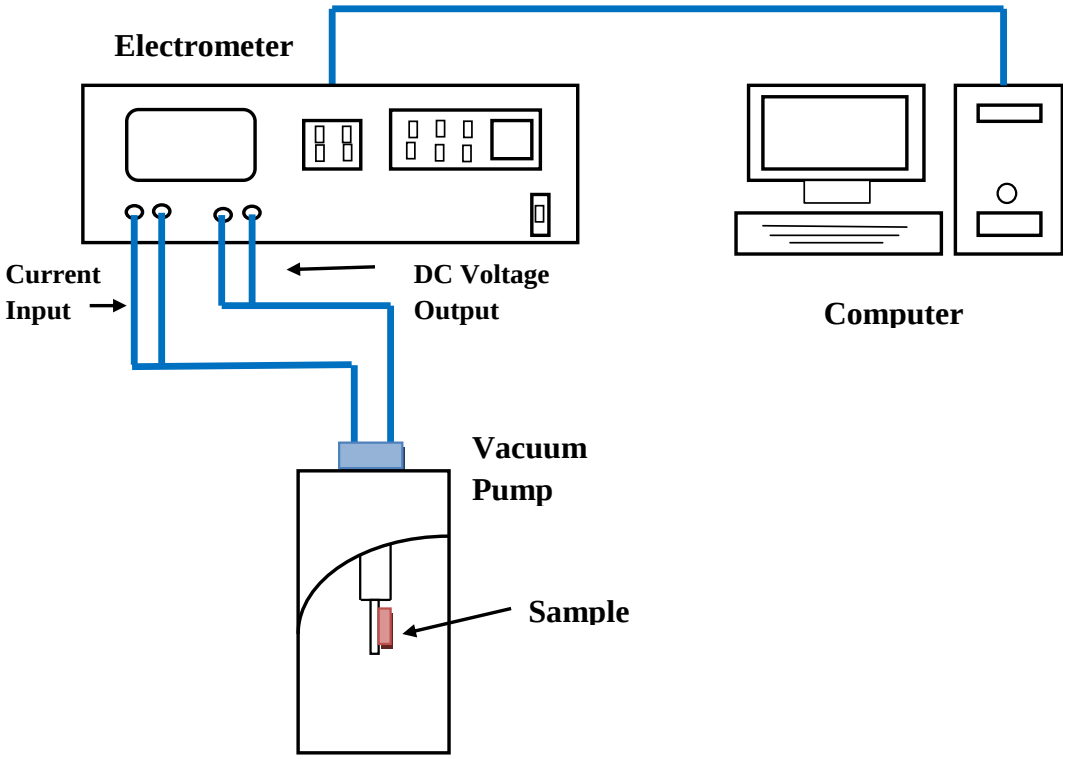

Figure 3.14: *Schematic diagram of experimental setup for electrical characterisation.*

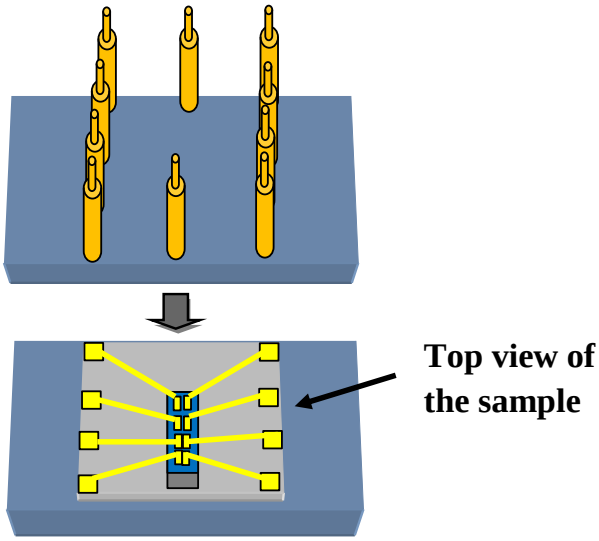

Figure 3.15: *The sample holder used for device measurements and the top view of the sample.*

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Chapter 4

Organic Metal-Insulator-Semiconductor (OMIS) Devices

4.1 Introduction

In this chapter, two types of organic metal-insulator-semiconductor (OMIS) devices are investigated. The first type of structures is OMIS capacitors, using different organic materials as insulators and different Ohmic contacts. These materials are poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP), used as the gate dielectric materials, gold (Au) and Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS), used as contact materials. OMIS memory devices is the second type of structures studied in this chapter, with four types of device, also depending on the materials that have been used. Gold thin layer, gold nanoparticles (AuNPs) and single walled carbon nanotubes (SWCNTs) were used as floating gates, and PMMA or PVP as the insulator. The experimental details, surface morphology and electrical characteristics of each of these seven devices are presented and discussed in this chapter.

4.2 Organic metal-insulator-semiconductor capacitor devices

4.2.1 PMMA-based OMIS devices

4.2.1.1 Fabrication process

Fabrication of OMIS capacitor devices with the structure of Al/PMMA/pentacene/Au (as shown in Figure 4.1) was started by thermal evaporation of 50 *nm* layer of Al through a shadow mask (Figure 3.10 A (a)) on a cleaned glass substrate to represent the gate electrode. A 300 *nm* thick insulating layer was deposited by spin coating of 10% (wt) anisole solution of PMMA with spin speed of 5000 *rpm* on top of the gate electrode and curing at 120°C for 1 hour. Pentacene was thermally evaporated through a shadow mask (Figure 3.10 A (b)) as the organic semiconductor to a thickness of 50 *nm* at a deposition rate of 0.03 *nm* s^{-1}. After seven days of the pentacene evaporation, a 50 *nm* layer of Au was deposited through a shadow mask (Figure 3.10 A (c)) by thermal evaporation. All films preparation and materials evaporation technique were discussed in chapter 3.

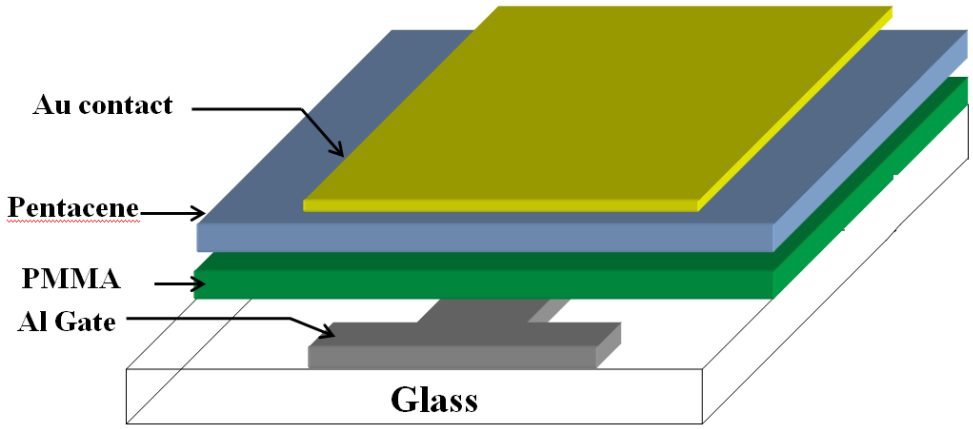


Figure 4.1: *Schematic diagram of PMMA-based OMIS capacitor structure*.

4.2.1.2 Surface morphology

Studying the surface morphology for the semiconducting layer in OMIS structures proved to be very important to enhance device characteristics. Atomic Force Microscopy (AFM) is used to examine the pentacene surface and study PMMA/pentacene interface with respect to fabrication parameters [1-3].

To achieve the optimal parameters for the evaporation of pentacene on top of PMMA layer, pentacene thin films were evaporated at different evaporation conditions (deposition rates and film thicknesses). Firstly, the thickness of pentacene and PMMA layers were fixed at 50 and 150 *nm*, respectively. The PMMA solution concentration and spin coating speed were 5% (wt) and 3000 *rpm*, respectively. Different deposition rates of pentacene film evaporation were used, i.e. 0.05, 0.03, 0.01 and 0.0015 *nm* s^{-1}. Figure 4.2 shows the AFM images of pentacene surface evaporated at different evaporation rates on 150 *nm* PMMA layer. Due to the irregular grain shape of pentacene, we defined average grain size as: X = area/number of grains and the average roughness, *Ra*.

As shown in Figure 4.2 (a), the AFM image for evaporated 50 nm thickness of pentacene layer on PMMA at a rate of 0.05 *nm* s^{-1} exhibits small and nodular grains with average size of 0.15 μm^2, and average roughness of 2.81 *nm*. This image shows that the boundaries between the grains are not connected. It is also clear from this figure that there are no visible crystalline structures in the pentacene film. Therefore, it is very difficult for the pentacene layer to act as a semiconductor under this evaporation rate. The film morphology of pentacene layer at evaporation rate of 0.03 *nm* s^{-1} shows a typical AFM image of good semiconducting layer with connected and large grains, of about 1.2 μm^2 in size, with a roughness of 4.29 *nm*, as shown in Figure 4.2 (b).

Figure 4.2 (c) and (d) show AFM images of the grown 50 *nm* thickness of pentacene film on 150 *nm* PMMA layer at lower evaporation rates, (c) at 0.01 *nm* s^{-1} and (d) at 0.0015 *nm* s^{-1}. It is clear from the image in Figure 4.2 (c) that the evaporation at 0.01 *nm* s^{-1} rates led to a good pentacene surface morphology with a roughness of 3.63 *nm*, and the grains were connected similar to those of the deposition rate of 0.03 nm s^{-1}. However, the grains were smaller in size and less dendritic.

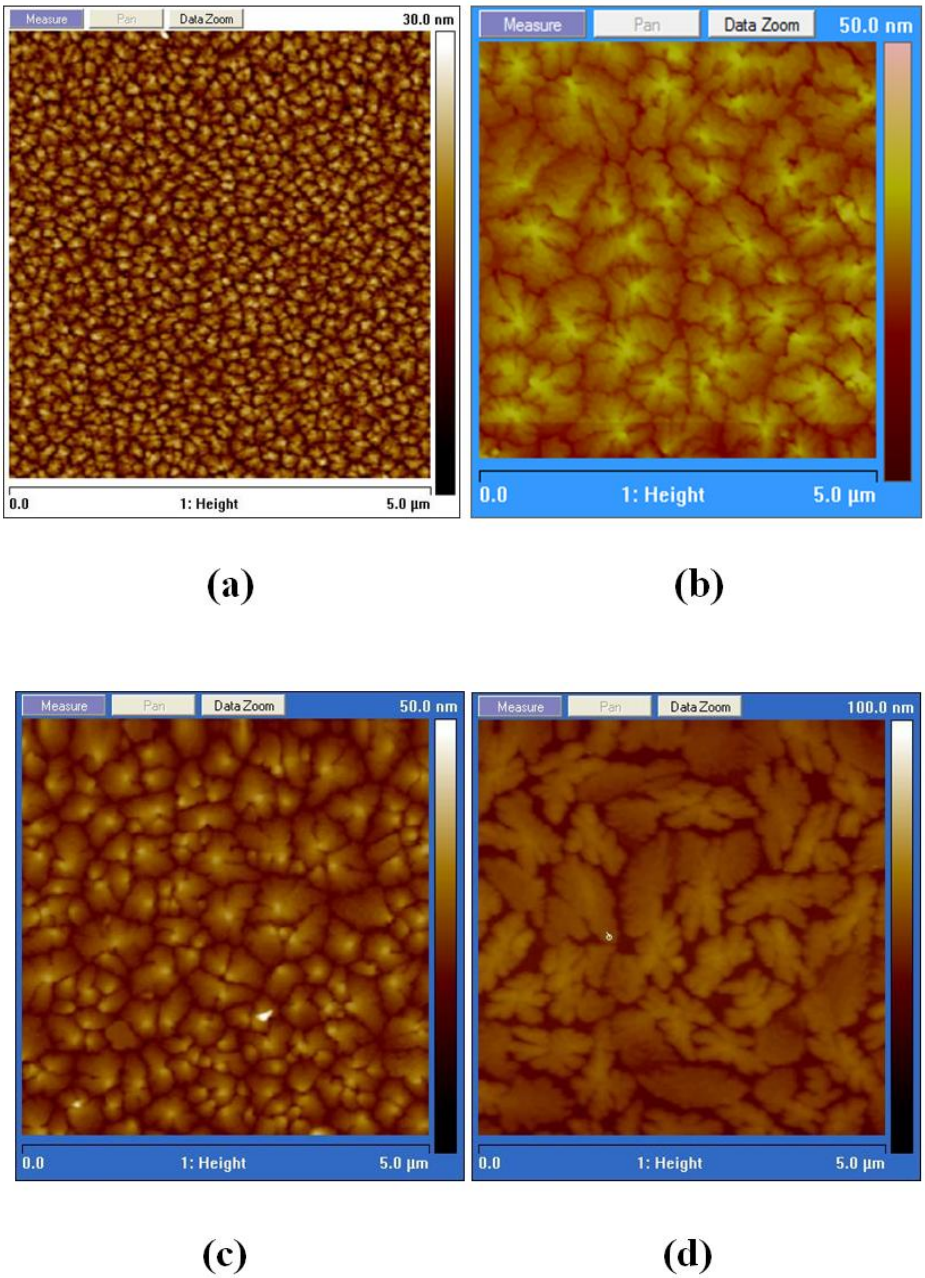


Figure 4.2: *AFM images of 50 nm pentacene film deposited on 150 nm PMMA at rates of (a) 0.05 nm s^{-1} (b) 0.03 nm s^{-1} (c) 0.01 nm s^{-1} and (d) 0.0015 nm s^{-1}.*

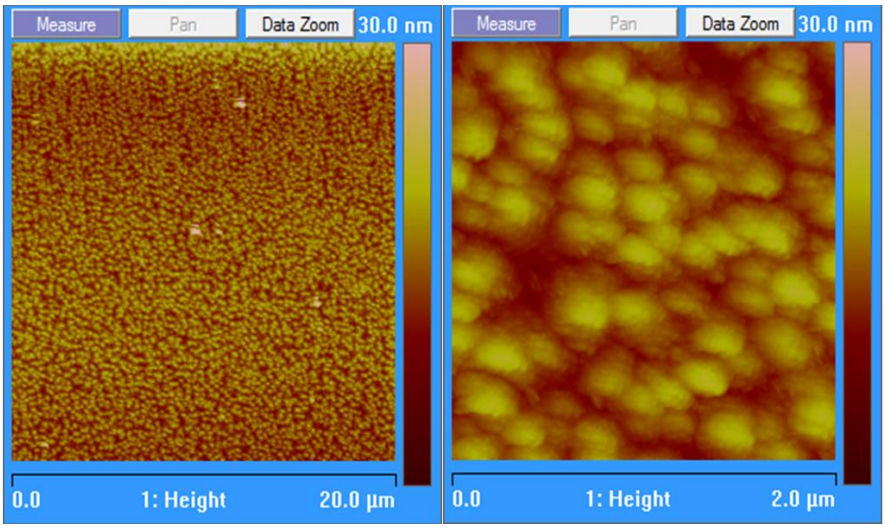
The slow evaporation of pentacene thin layer at 0.0015 μm^2 rate resulted in a well-formed, condensed and large dendritic grains of pentacene, as shown in Figure 4.2 (d). The only setback of this process is the evaporation time, as it required about 7 hours of

evaporation to reach 50 *nm* thickness of pentacene. The surface roughness of the evaporation at this very slow rate was measured at about 5.53 *nm*, and the typical size of pentacene grains was 1.17 μm^2.

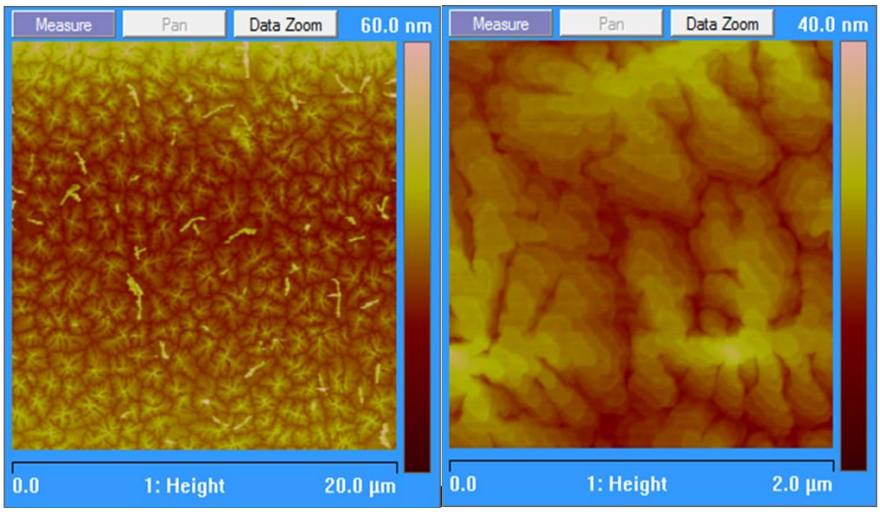
As a result, poor surface morphology, poor grains connections, and smaller grains, produced when high speed evaporation rate (0.05 $nm\ s^{-1}$) was used; and consequently, the pentacene layer show poor conductivity. In contrast, efficient films of pentacene were obtained by evaporation at moderate (0.03 and 0.01 $nm\ s^{-1}$) to low (0.0015 $nm\ s^{-1}$) rates. The optimum morphology surface, with bigger crystalline and connected grains was achieved using 0.03 $nm\ s^{-1}$ evaporation rate.

Since there is a strong dependence on the interface between the pentacene and PMMA, another parameter was investigated that may affect the quality of the pentacene film; this was the thickness of the PMMA layer. For that reason, the evaporation of 50 *nm* pentacene films was deposited at 0.03 $nm\ s^{-1}$ rate on two different thicknesses of PMMA layers, 50 and 300 *nm*. The PMMA solution concentrations were 3% (wt), 10% (wt), and spin coating speeds were 3000, 5000 *rpm* for 50 and 300 *nm* thickness, respectively.

Figure 4.3 shows the AFM images of evaporated pentacene films at a rate of 0.03 $nm\ s^{-1}$ grown on (a) 50 *nm* and (b) 300 *nm* thickness of PMMA. As the same pentacene deposition process and thickness were used, the difference in pentacene morphology is clearly due to the difference in the PMMA thickness. The dendritic type growth can be observed for pentacene deposited on 300 *nm* PMMA film, with large grain sizes of about 1.54 μm^2 in average, as shown in Figure 4.3 (b). In contrast, much smaller grains, about 0.044 μm^2, were observed when pentacene was deposited on a thinner layer of PMMA, as shown in Figure 4.3 (a), resulted in dramatic changes in the pentacene morphology; as grains were almost completely separate from each other. Figures 4.2 and 4.3 show few defects observed on the film surfaces, due to transferring the device outside the clean room environment.



(a)



(b)

Figure 4.3: *AFM images of 50 nm pentacene films deposited at rate of 0.03 nm s^{-1} on (a) 50 nm and (b) 300 nm thickness of PMMA.*

Summaries of morphology surface properties of 50 *nm* pentacene films formed on PMMA layer with different parameters (deposition rates and insulator thicknesses) are shown in Table 4.1.

Table 4.1: *The effect of pentacene evaporation rates and insulator thickness on pentacene surface morphology.*

PMMA Thickness (*nm*)	Deposition Rates ($nm\ s^{-1}$)	Average Roughness (*nm*)	Average Grain Size (μm^2)
150	0.05	2.81	0.15
150	0.03	4.29	1.2
150	0.01	3.63	1.0
150	0.0015	5.53	1.17
50	0.03	2.22	0.044
300	0.03	3.06	1.54

It is clear from Table 4.1 and the AFM images in Figures 4.2 and 4.3 that the optimum rate for deposition of pentacene film was 0.03 $nm\ s^{-1}$, and the optimal thickness of PMMA dielectric layer was 300 *nm*.

The thickness of PMMA was a function of spinning speed and solution concentration. At higher PMMA concentrations (> 15 % (wt)); the film thickness was inversely proportional to the spinning speed. On the other hand, for lower PMMA concentrations (< 3 % (wt)), the thickness of deposited film was nearly constant, and did not change with the spinning speed. These results are in full agreement with the findings of Y. Yun et al [4]. As PMMA is a porous polymer material, the low solubility and small thickness of PMMA will produce pin holes. To decrease the number of pin holes, it is necessary to increase PMMA thickness by increasing the concentrations. At the same time, it is necessary to increase the spinning speed to produce smooth and uniform PMMA thin films. A relatively smooth surface, uniform and pinhole-free film, is evident for the PMMA at a thickness of about 300 *nm*. Therefore, all MIS and

transistor structures investigated in this study were produced with PMMA layers of 300 *nm* thickness and 0.03 *nm* s^{-1} evaporation rates for pentacene layers.

4.2.1.3 Electrical characterisation

Typical capacitance, per unit area, and loss (G/ω) versus voltage (solid blue line) curves of Al/PMMA/pentacene/Au MIS capacitor structure are shown in Figure 4.4 measured at (a) 2 *kHz* and (b) 100 *kHz*. The device area was 8.5 x 10^{-3} cm^2. Double voltage sweep corresponding to a range of ±12 *V* was applied at a scan rate of 0.5 *V/s*. The voltage scan was always started from the accumulation region and swept toward the inversion region (although the opposite scan direction did not significantly alter the device behaviour). The capacitance-voltage (*C*–*V*) characteristic reveals the usual accumulation–depletion–inversion behaviour of an MIS structure, with a flat-band voltage (V_{FB}) of -2.5 and -3 *V* for measurements at 2 and 100 *kHz* respectively. This shift away from the 0 *V* originated probably from charge trap sites present in the interfaces between the insulating and the active layers [5, 6]. Also, these figures show a transition from accumulation (negative gate voltage applied to Al) to depletion (at applied positive gate voltage) occurring between about -2.8 *V* to 4 *V*, and about -3.3 *V* to 3.5 *V*, for the devices at 2 *kHz* and 100 *kHz*, respectively; i.e., the slope of the curve in the depletion region was shorter in 2 *kHz*. This may suggest that a lower interface state density exists at PMMA/pentacene interface at lower frequencies.

The measured value of the accumulation capacitance for the device at 100 *kHz* was 70.53 *pF*, from which the thickness of the layers was estimated to be about 320 *nm* for PMMA, and the pentacene film thickness, i.e. the maximum width of depletion region measured from the depletion capacitance (C_D = 354 *pF*), was estimated to be ~ 63 *nm* (using the dielectric constant, ε, of ~ 3 for PMMA [7, 8] and also ~ 3 for pentacene [9, 10] at 100 *kHz*). The difference in the calculated and expected thickness of the PMMA and pentacene layers is believed to be due to the lack of uniformity in the spin-coated thin PMMA layer and thermal evaporation of pentacene film and/or the actual values of relative permittivity for both materials.

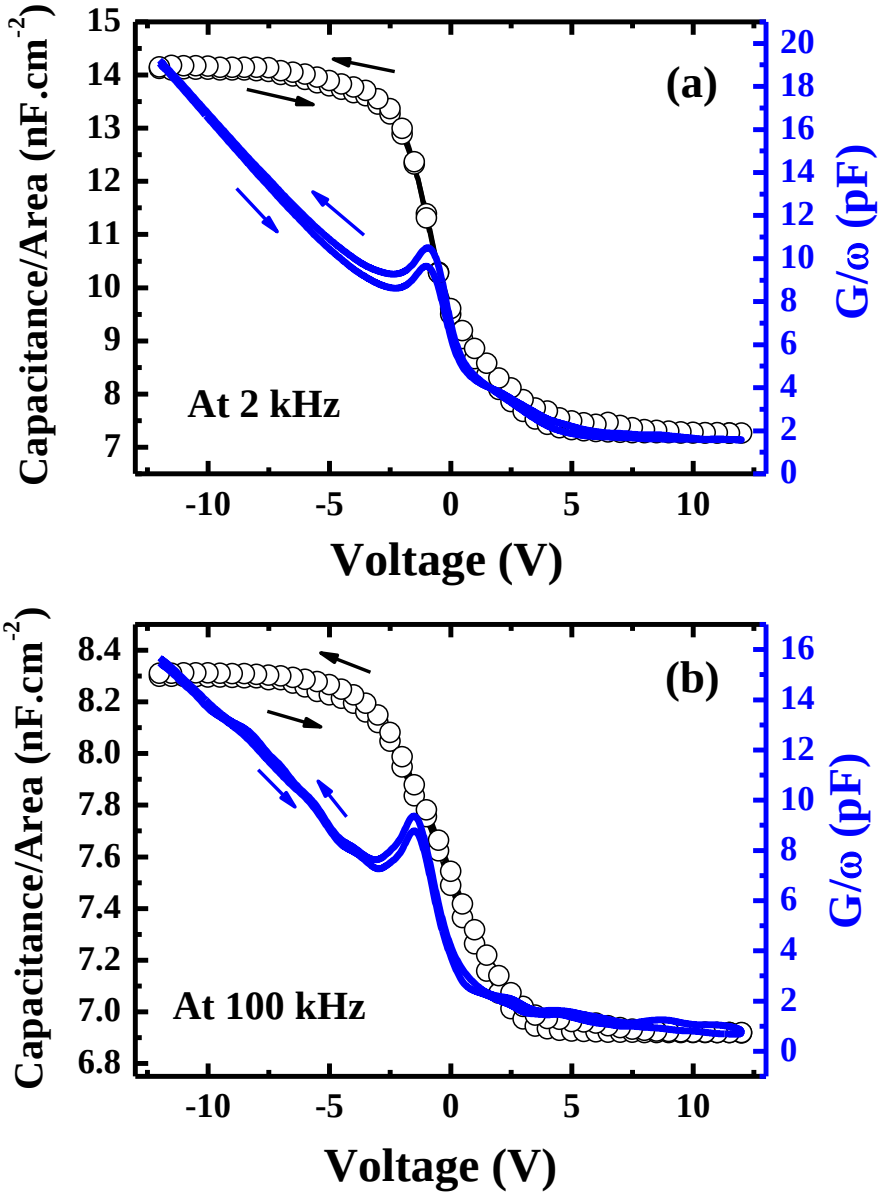


Figure 4.4: *C-V (open circle and line) and G/ω-V (blue solid line) characteristics for Al/PMMA/pentacene/Au structure with the bias swept from -12 V to 12 V and back to -12 V, at frequencies of (a) 2 kHz and (b) 100 kHz.*

Negligible hysteresis was evident in the voltage sweep at both frequencies. This result means there is almost no defects in the interface between the insulator and semiconductor or within the insulating layer [11], and the hysteresis was independent of the applied frequency [12].

We can calculate the doping concentration (N_a) for the pentacene layer using the calculated insulator thickness (d_{Ins}) and the flat-band capacitance (C_{FB}) (which is represents 85% of the normalized *C–V* curve) by using [13]:

$$C_{FB} = A \frac{\varepsilon_{Ins}}{d_{Ins} + \frac{\varepsilon_{Ins}}{\varepsilon_s}\sqrt{\frac{KT}{e}\frac{\varepsilon_s}{eN_a}}} \qquad (4.1)$$

Where *K* is the Boltzmann constant, *T* is the temperature (300 *K*), e is the electric charge, *A* is the device area and ε_{Ins} and ε_s are the permittivity of the insulator and the semiconductor, respectively. With the capacitance at the flat–band voltage is about 114.33 *pF* for measurements at 2 *kHz*, the doping concentrations (which determine the material's carrier concentration) were estimated to be 1.3 x 10^{17} cm^{-3}, in good agreement with reported values in literature [14, 15].

The loss (G/ω) versus voltage curves are also presented in Figure 4.4, where a single peak was observed in two directions and at the two different measurement frequencies, indicating a very small number of electrons trapped which increases the density of interface states [16]. Although the peaks occurred at these frequencies in the same site; in the depletion region at about -1 *V*, the height and width of the loss peak showed a slight increase in the reverse sweep, which means the trapped electrons, had increased the density of interface states.

The *C-V* characteristics of the device with forward and reverse direction of another device at different voltage sweeps, ± 10, ± 20 and ± 30 *V*, are shown in Figure 4.5. These data were measured at 100 *kHz* at a scan rate of 1 *V/s*. Negligible hysteresis was also evident at these voltage sweeps indicating there is almost no traps been generated at high voltages.

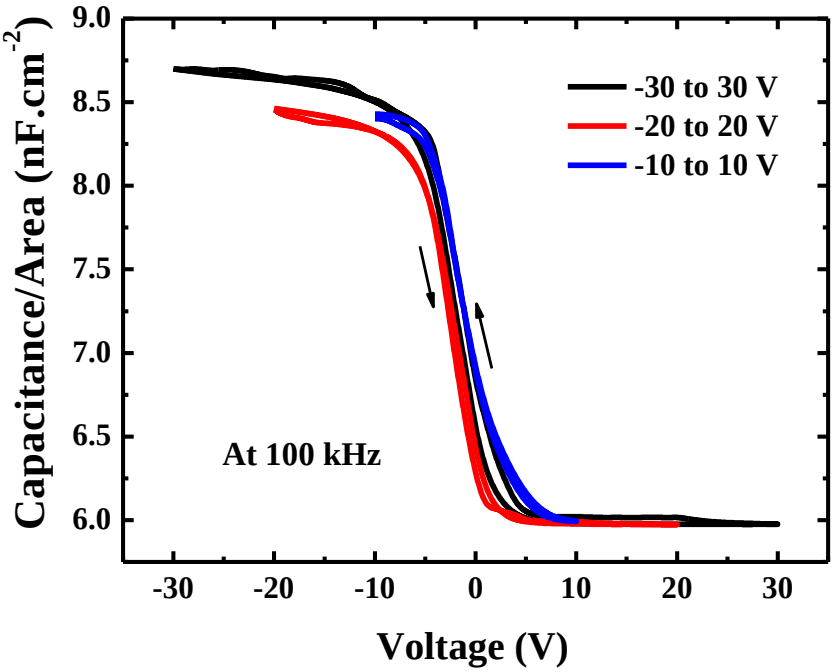


Figure 4.5: *Capacitance per unit area versus voltage at 100 kHz for Al/PMMA/pentacene/Au structure at different voltage sweeps.*

Furthermore, for all these voltage sweeps in Figure 4.5, the *C–V* curves reveal the usual accumulation-depletion-inversion characteristics of an MIS structure based on p-type semiconductor, with the nearly fixed value of flat-band voltage, approximately -5 *V*. The semiconductor reached full depletion at gate voltage ≥ 3 *V* for all these voltage sweeps with the minimum value of measured capacitance $C_M \sim 51.3\ pF$.

The frequency dependence of capacitance (*C–f*) curves of the same device at various voltage biases from -12 *V* to + 12 *V*, step 1 *V*, are shown in Figure 4.6. A gradual decrease in the measured capacitance with the increase in frequency is clearly seen in Figure 4.6. This result is in agreement with the values extracted from the *C-V* curves in Figure 4.4. At low frequency, the majority carriers can follow the AC signal and then lead to excess of the capacitance; leading to a high value of capacitance [17]. Additionally, in this figure, the capacitance shows strong frequency dependence and tends to decrease more when the positive voltage increased further. Furthermore, it is

clearly seen in Figure 4.6 that the capacitance values are not only frequency dependent but are also voltage dependent. These capacitance values show further increase towards higher negative voltages; from gate bias voltage of 2 *V* towards negative bias of -12 *V* steps 1 *V*. Also it can be seen that at gate bias voltage > 2 *V* (towards positive bias), the capacitance is weakly dependent on frequency. This behaviour can be explained by the detrapping phenomena at interface states acting as recombination/generation centres [18].

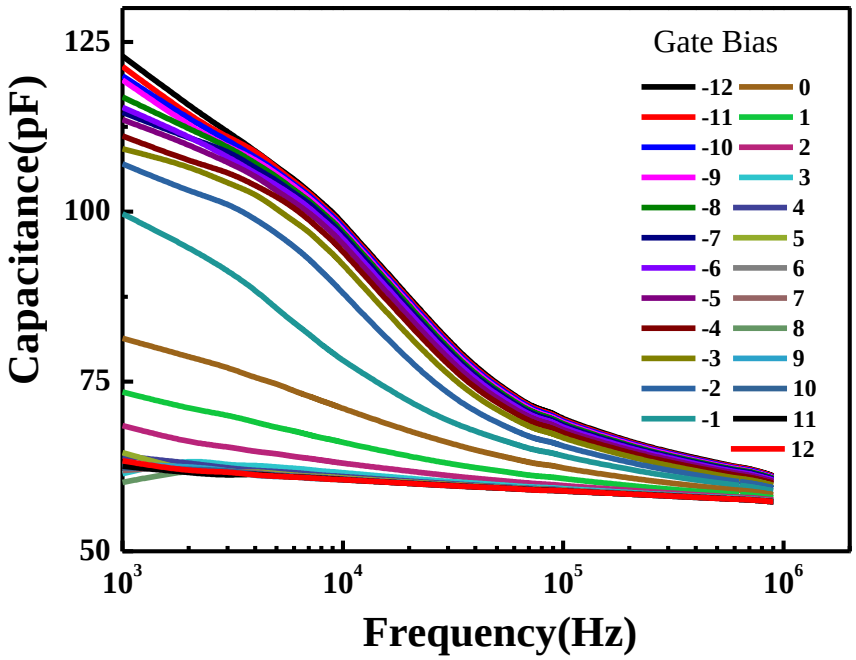


Figure 4.6: *Capacitance versus frequency (C-f) characteristics of Al/PMMA/pentacene/Au structure at different bias voltages.*

4.2.2 PMMA-based OMIS devices with PEDOT:PSS as the top contact

This section describes the electrical characterisation of Al/PMMA/pentacene/PEDOT:PSS capacitors. All fabrication conditions and experimental steps were the same as the previous MIS capacitor device (shown in Section 4.2.1.1). The

difference between the two structures is that PEDOT:PSS was used as the top contact instead of gold, and the PEDOT:PSS was patterned using a pen to the area of 0.12 cm^2.

4.2.2.1 Electrical characterisation

The *C-V* (capacitance per unit area), and *G/ω-V* characteristics of the MIS capacitor based on PEDOT:PSS as the top contact, are shown in Figure 4.7. The measurements were made with double voltage sweep of ± 20 *V* to a scan rate of 1 *V/s* at 2 *kHz*. The *C-V* curve reveals the accumulation-depletion-inversion characteristics with a flat–band voltage of approximately -2 *V*. The transition from accumulation to depletion occurred between -3 *V* and 12 *V*; this means that the slope of the curve in the depletion region was longer than that in the MIS capacitor device with Au as the top contact. More importantly, the characteristics show negligible (almost no) hysteresis in *C-V* behaviour indicating no traps in the insulator/semiconductor interface.

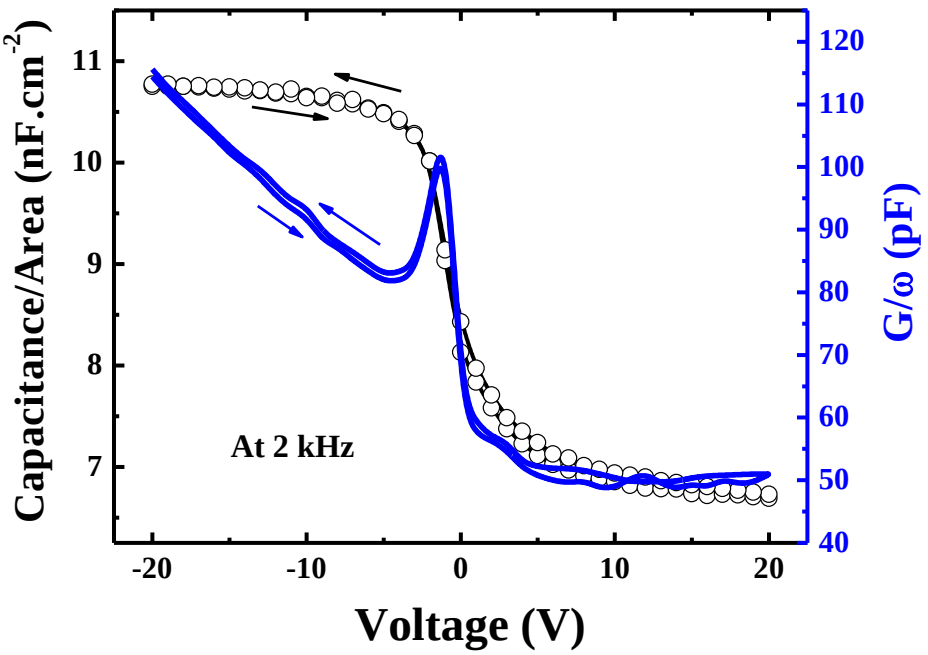


Figure 4.7: *C-V (open circle and line) and G/ω-V (blue solid line) curves for Al/PMMA/pentacene/PEDOT:PSS structure with bias swept from -20 V to 20 V and back to -20 V.*

This device was fabricated under the same conditions as the MIS capacitor based on Au as the top contact, and was characterised at 2 *kHz*. The capacitance per unit area in this device was smaller, with a higher peak loss. Higher loss indicates that trapped electrons had increased the density of interface states interacting with the majority carriers. In addition, it is clearly observed that the loss peak occurred in the depletion region in the *C-V* curve, as in the previous device, indicating the presence of interface states. The flat–band capacitance (C_{FB}) was estimated to be 1214 *pF* at 2 *kHz*, and therefore, the doping concentration N_a was estimated to be 0.8 x 10^{17} cm^{-3}.

Figure 4.8 shows the capacitance per unit area versus voltage of this device at different voltage sweeps (± 2, ±5, ± 8, ± 10, ± 12, ± 15 and ± 20 *V*) at 2 *kHz*. It is interesting to see that the device transition from the accumulation region to inversion through the depletion region at all these voltage sweeps is nearly in the same line, and at constant flat–band voltage of -2 *V*; there is no shift in the measurements of capacitance values (just a slight shift at bias from 0 to 5 *V*); this means that perhaps there are no charge trap sites present in the interfaces between the PMMA layer and the pentacene layer.

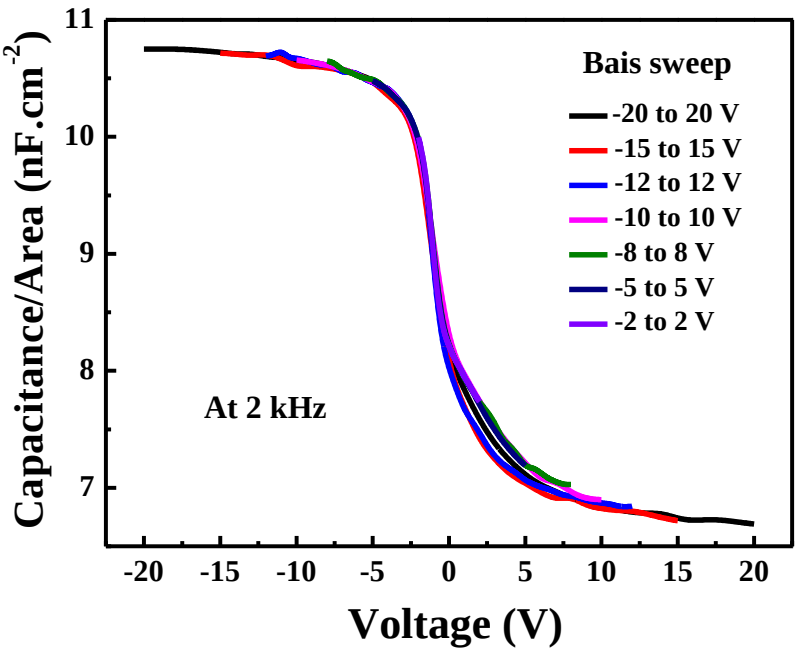


Figure 4.8: *Capacitance per unit area versus voltage for Al/PMMA/pentacene/PEDOT:PSS structure with various bias sweeps measured at 2 kHz.*

The capacitance measured in accumulation ~ 1293 *pF*, and the thickness of the insulating layer was estimated to be in the region of 296 *nm*. The device approached full depletion at biases ≥ 15 *V*.

4.2.3 OMIS capacitor with PVP as insulator

The experimental details, surface morphology of pentacene and Poly(vinyl phenol) (PVP) layers, and the electrical characterisation, are reviewed in this suction for Al/PVP/pentacene/Au structure.

4.2.3.1 Fabrication process

An aluminium strip gate was thermally evaporated on a glass substrate through a shadow mask (Figure 3.10 C (a)) to a thickness of 70 *nm*. 50% (wt) of PVP solution in isopropanol (IPA) was spin coated to a thickness of about 350 *nm* at 5000 *rpm*. The spun PVP film was then baked at 80 °C for 10 min to form a uniform layer. Pentacene was thermally evaporated through the shadow mask (Figure 3.10 C (b)) at 0.03 $nm\ s^{-1}$ to a thickness of ~ 50 *nm*. Finally, after seven days of the pentacene evaporation, 60 *nm* gold contacts were thermally evaporated through a shadow mask (Figure 3.10 C (c)). The area of the top Au electrode was 6.5 x 10^{-3} cm^2. The schematic diagram of this MIS capacitor structure is similar to that of the structure in Figure 4.1 with PVP as the insulating layer instead of PMMA.

4.2.3.2 Surface Morphology

The surface morphology for PVP and pentacene are depicted in Figure 4.9. The smooth surface and harmonic growth of PVP layer on Al gate is shown in Figure 4.9 (a), and the 3D surface grown at the same area scan size is shown in (b). The clear polycrystalline structures of pentacene deposited on PVP are also presented in this figure, with area scan sizes of (c) 5 μm, and (d) 2 μm. The grain size of pentacene was about 1.46 μm^2.

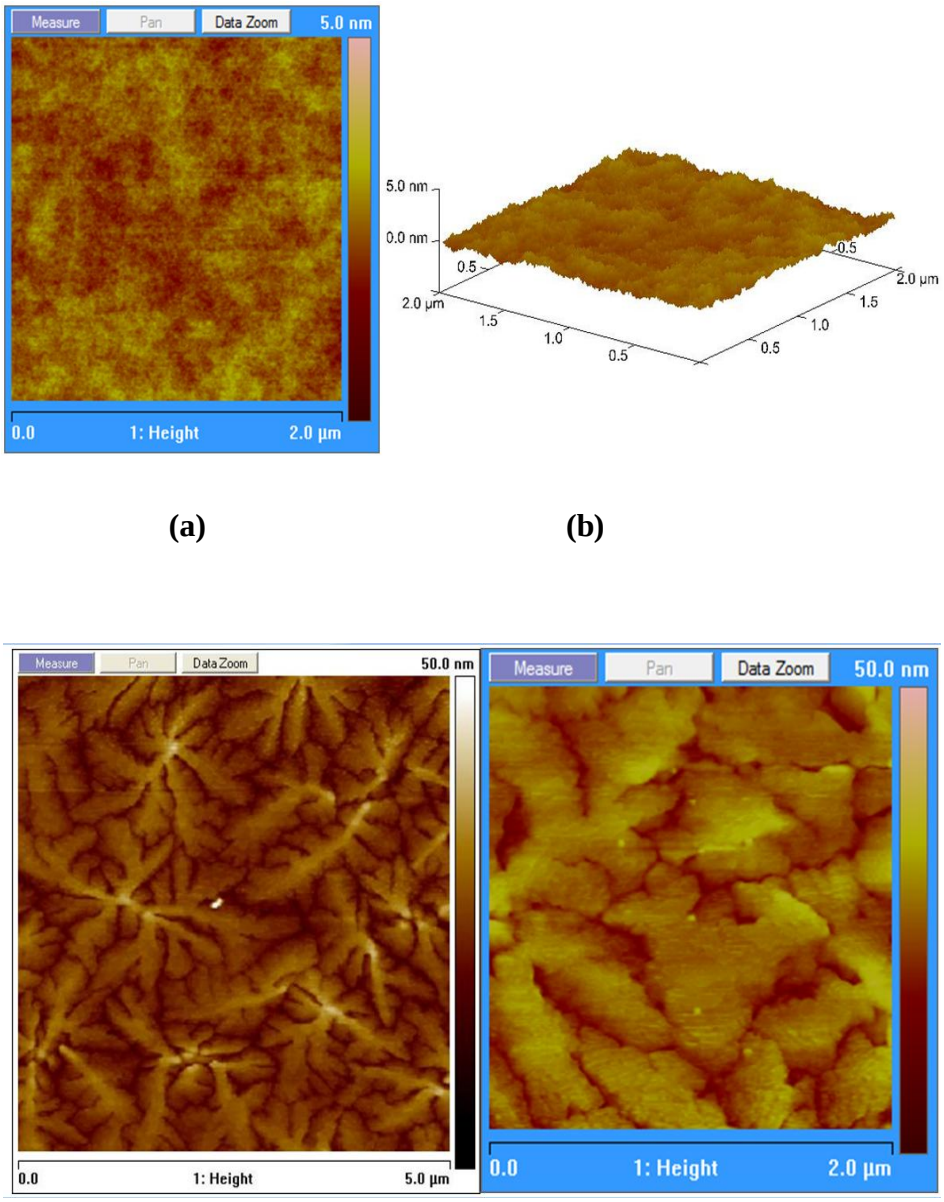


Figure 4.9: *AFM images of (a) PVP layer on Al gate layer with area scan size 2 µm, (b) 3D surface plot for PVP on Al, and deposited pentacene film on PVP with scan area size of (c) 5 µm and (d) 2 µm.*

4.2.3.3 Electrical characterisation

Double voltage sweeps of ± 40 *V* at a voltage scan rate of 2 $V\ s^{-1}$ were conducted for this structure at 100 *kHz* and 1 *MHz* as shown in Figure 4.10. As the gate bias swept from negative to positive voltages, the device transitioned from accumulation to depletion and deep depletion behaviour typically seen in p-type MIS capacitors. The flat–band voltage was about -16 *V*; there was no effect of the measurement frequency on the value of flat–band voltage in this device.

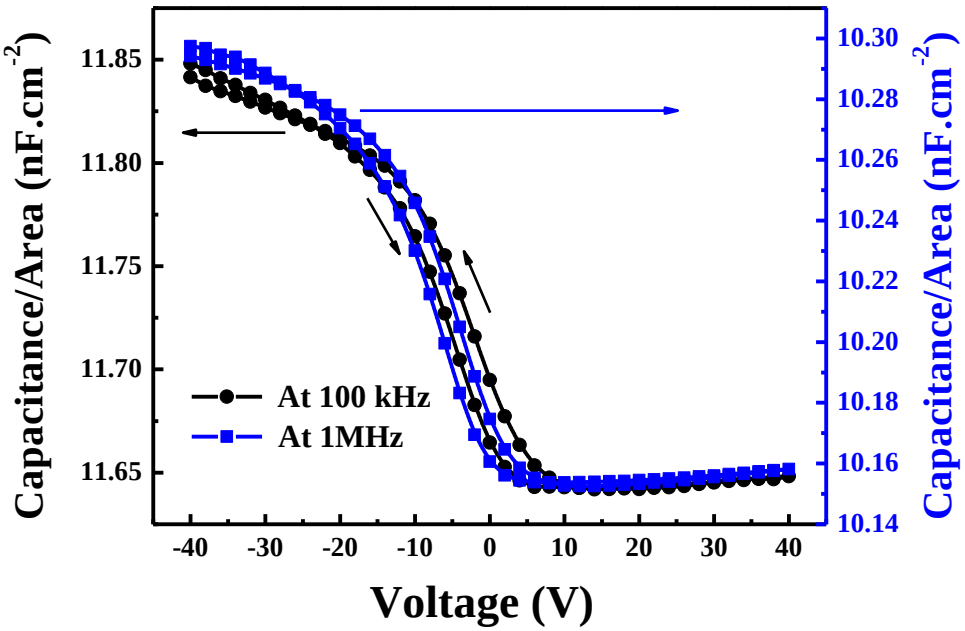


Figure 4.10: *C-V characteristic curves of double voltage sweep ± 40 V for Al/PVP/pentacene/Au structure at frequencies of 100 kHz and 1 MHz.*

Furthermore, the slope lines of the curves in the depletion region occurred between about -20 and 5 *V*, which indicates that a higher interface state density may exist at PVP/pentacene interface compared to that of PMMA/pentacene interface. At the two different frequency measurements, negligible hysteresis was evident at the voltage sweep rate of ± 40 *V*. The capacitance in accumulation for this device was 66.8 at 1 *MHz* and the thickness of the insulator was estimated to be about~ 345 *nm* (ε_{Ins} ~ 4 at *1 MHz* [19]). For the two frequency measurements, full semiconductor depletion was at biases ≥ 5 *V*.

The doping concentration (N_a) of pentacene is nearly the same value as for the PMMA-based devices, 1.3 x 10^{17} cm^{-3}. This means the pentacene's carrier concentrations were almost constant for both devices.

4.3 Organic metal-insulator-semiconductor memory devices

The experimental details and electrical characteristics for four types of OMIS memory devices are presented in this section. Thin layer of gold, gold nanoparticles (AuNPs) and single-walled carbon nanotubes (SWCNTs) were used as floating gates and PMMA or PVP as insulating layers.

4.3.1 OMIS memory devices with PMMA as insulator and thin layer of Au as floating gate

4.3.1.1 Fabrication process

The structure of the Al/PMMA/Au/PMMA/pentacene/Au MIS memory device is shown in Figure 4.11. The device was fabricated by thermally evaporating 50 *nm* thickness of an Al gate electrode through a shadow mask (Figure 3.10 B (a)) onto a clean glass substrate. A 300 *nm* thick insulating layer was formed by spin coating of PMMA on top of the gate electrode and curing at 120°C for 1 hour. The floating gate was formed by evaporating about 10 *nm* thick gold layer. Prior to deposition of pentacene, another thin film of PMMA was deposited onto the floating gate. Pentacene was thermally evaporated at a pressure of 7.5 x 10^{-7} mbar, at a rate of 0.03 *nm* s^{-1}, through a shadow mask (Figure 3.10 B (b)) to a thickness of 50 *nm*. Following deposition of pentacene, top contacts were defined by thermal evaporation of 50 *nm* of Au through a shadow mask (Figure 3.10 B (c)) after about seven days of the pentacene evaporation.

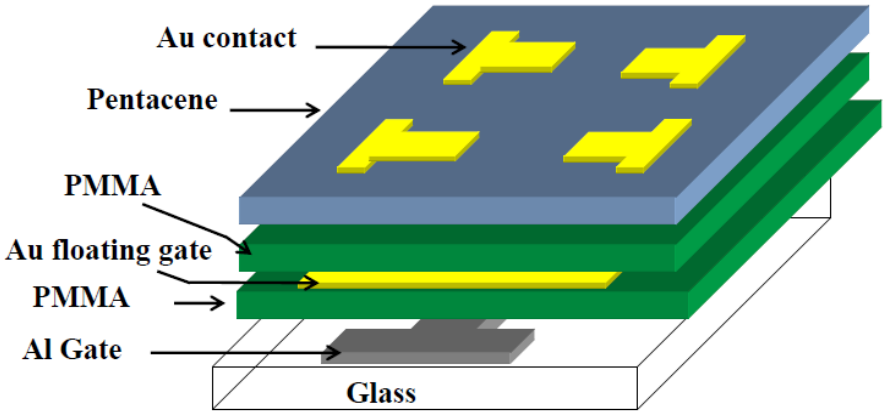


Figure 4.11: *Schematic diagram of Al/PMMA/Au/PMMA/pentacene/Au memory structure.*

4.3.1.2 Electrical characterisation

Figure 4.12 shows the *C–V* characteristics of the MIS memory (black solid line) and control (blue solid line) devices, with and without Au thin layer, respectively. The reference structure was Al/PMMA/pentacene/Au for the control device (without floating gate). All the measurements reported in this section were performed at 1 *MHz* and at a voltage scan rate of 100 $m\ V\ s^{-1}$; the area of the top Au electrode was 9 x 10^{-3} cm^2. In each measurement, the scan started from accumulation voltage and swept toward deep depletion and back to accumulation. The *C–V* curve for the control device reveals the typical accumulation–depletion–inversion characteristics of an MIS structure based on p-type semiconductor, with a flat–band voltage of about -8 *V*, and the semiconductor becomes fully depleted at about 5 *V* as the measured capacitance remains constant at voltages above 5 *V*. A negligible (almost no) hysteresis is evident in the voltage sweep rate used for the control device.

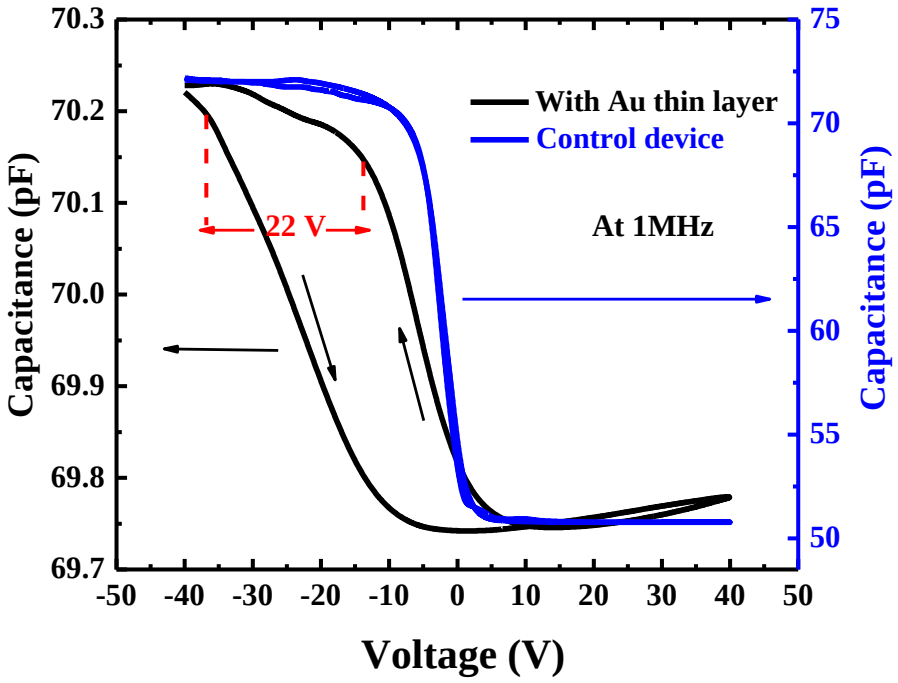


Figure 4.12: *C–V characteristics at 1MHz for the MIS memory (black solid line) and control (blue solid line) structures.*

The addition of a thin layer of Au between two layers of insulators to form Al/PMMA/Au/PMMA/pentacene/Au structure produced very small change in the flat–band voltage, as shown in Figure 4.12. Furthermore, on reversing the direction of the voltage scan, significant hysteresis was evident in the *C–V* curve with a large memory window (ΔV) of about 22 *V*. This was attributed to the presence of the Au thin layer and was almost certainly the result of charging and discharging. These results are consistent with our recent studies [20, 21] and with Mabrook et al.; *C-V* studies of P3HT/PSQ devices [22], in which hysteresis in the *C-V* curves was attributed to the presence of an Au floating gate embedded within the insulating layer. The anticlockwise hysteresis after sweeping the accumulation region suggests that the charging and discharging of interface traps (floating gate) is located close to, or at, the PMMA/pentacene interface [4, 23]. We believe that, in accumulation, when a negative bias is applied to the metal gate electrode, holes are injected from the pentacene surface into the floating gate, charging up the Au layer. An increased negative voltage

needs to be applied to the Au electrode to produce inversion of the pentacene surface (the *C-V* curve is shifted towards more negative voltages).

The effect voltage sweeps on the memory window (ΔV) of this device is shown in Figure 4.13. The memory window (shift in the flat–band voltage) increased linearly as the voltage sweep range increased, which is expected memory behaviour, and ΔV of about 7 *V* is achieved at sweep range ± 10 *V* and 22 *V* at ± 40 *V* sweep voltage. This is indicative that the charges stored in the memory device increased as the applied voltage increased.

From the value of capacitance *C* and conductance *G* in accumulation (*G* was 4.3 *S*), the parameters of the equivalent circuit in the accumulation region, which can be represented by a series of insulator capacitance C_I and series resistance R_S (representing the resistance of pentacene film and the contact resistance), were calculated by:

$$R_s = \frac{G}{G^2 + w^2 C^2}\ ,\ C_I = C\left(1 + \frac{G^2}{w^2 C^2}\right) \qquad (4.2)$$

We found that C_I = 70.24 *pF* and R_S = 23 *Ω*. The amount of charges stored (*Q*) in the gold thin layer for this memory device can be estimated from C_i (accumulation capacitance per unit area) and the flat–band voltage shift ΔV_{FB} using $Q = C_i\ \Delta V_{FB}$. From the accumulation capacitance in Figure 4.12, the calculated value of C_i is 7.8 x 10^{-9} *F* cm^{-2}; the number of charge carriers stored is approximately 1.07 x 10^{12} cm^{-2} for the sweep range ±40 *V*.

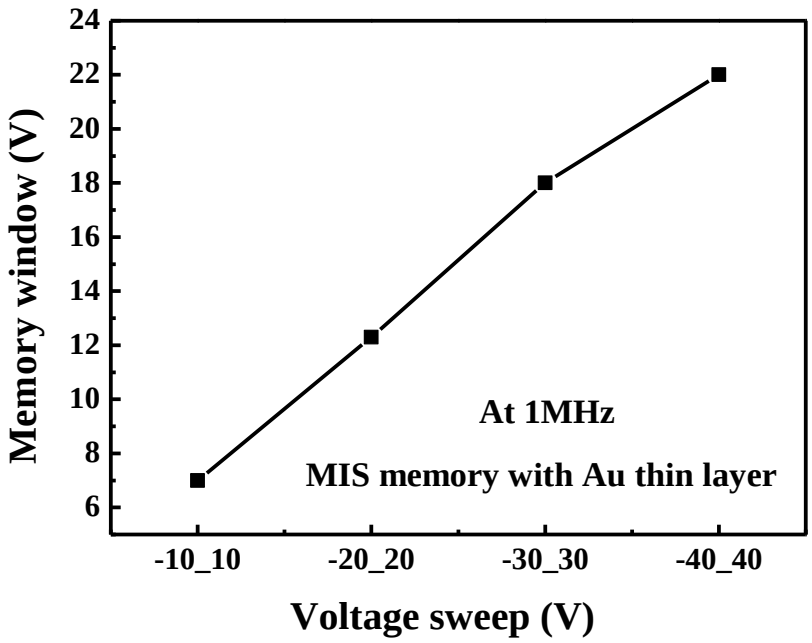


Figure 4.13: *The memory window (flat–band voltage shift) versus the voltage sweep range for MIS memory device with Au thin layer floating gate.*

4.3.2 MIS memory devices with PMMA as insulator and AuNPs as floating gate

In this device structure, a discrete floating gate consisting of gold nanoparticles (AuNPs) became a substitute for the Au thin film floating gate. The memory characteristics of the MIS device, with AuNPs as floating gate are examined in this section.

4.3.2.1 Fabrication process

The structure of MIS memory device based on AuNPs as the floating gate between two layers of PMMA is similar to that of Figure 4.11. The device was fabricated under the same fabrication conditions and experimental steps as those used for fabricating the MIS memory device in Figure 4.11, with AuNPs used as the floating gate instead of the gold layer. The AuNPs were deposited using the self-assembly technique described

in Section 3.3.3. The materials used and detailed deposition process is explained in Section 3.4.2.3 (a). Control device (without AuNPs) was also fabricated for comparison and to show the effects of the floating gate in the MIS memory device. It was the same control device as for the OMIS memory device based on Au thin layer, as both devices were fabricated at the same time.

4.3.2.2 Electrical characterisation

The C-V characteristics of the memory device (black solid line), after the addition of AuNPs within the insulating stack to form an Al/PMMA/AuNPs/PMMA/pentacene/Au structure, and the control device (blue solid line), are shown in Figure 4.14. As shown in Figure 4.14, the AuNPs floating gate layer produced a significant change in the flat–band voltage. Furthermore, on reversing the direction of the voltage scan, clear hysteresis was observed. The clockwise direction of the hysteresis, with a shift of the flat–band voltage to a less negative voltage, indicates that electrons originating from the Al gate become trapped on the floating gate. In this case, in accumulation, the electrons are injected from the Al electrode to the Au nanoparticles, which later become negatively charged. The opposite effect occurs in inversion, and electrons are transferred to the Al electrode from the nanoparticles. This behaviour is in good agreement with other researchers [23, 24]. The hysteresis in the *C–V* curve shows a memory window ΔV of about 32 *V* (larger than the hysteresis reported for Au thin layer device). On the other hand, the lack of hysteresis with the control devices strongly indicates that charge storage in the Au or AuNPs layers is responsible for the hysteresis effects.

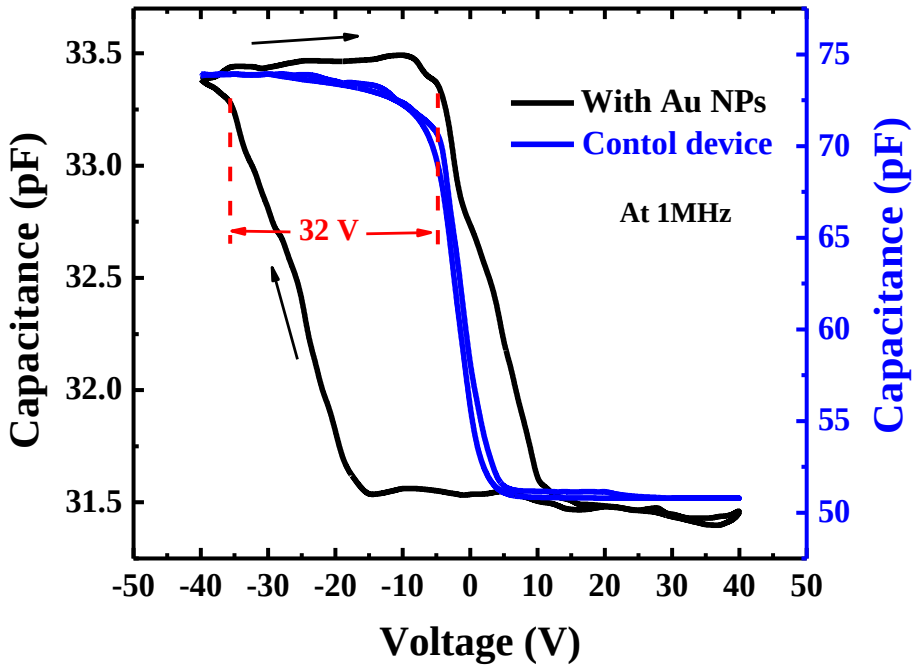


Figure 4.14: *C–V characteristics at 1MHz for the MIS memory (black solid line) and control (blue solid line) structure devices (with and without AuNPs floating gate).*

Figure 4.15 shows the linear increase of ΔV in this memory device as the voltage sweep range increased, which resulted from the increase of charges stored as the applied voltage increased. ΔV of about 16 V at ± 10 V was reached, and about 32 V at ± 40 V sweep voltage.

The calculated values for the insulator capacitance C_I and series resistance R_S were 33.4 pF and 12.5 Ω, respectively, where the conductance G was 8.01 S. The thicknesses of the insulator and semiconductor layers were estimated to be about 620 and 43 nm, respectively. The decrease in capacitance of the memory device as compared to the control devices was perhaps due to the additional material being added to the device such as the second layer of PMMA and AuNPs (floating gate). In practical, the structure cannot be treated as simply as the equivalent circuit of the control device [25]. However, the accumulation capacitance value indicates almost direct relationship between the capacitance and the thickness of the PMMA layers (two

layers of 300 *nm* each for the memory device). This also indicates that the presence of AuNPs did not change the PMMA dielectric properties such as permittivity. The number of charge carriers stored in the Au nanoparticles *Q* was approximately 0.74 x 10^{12} cm^{-2}.

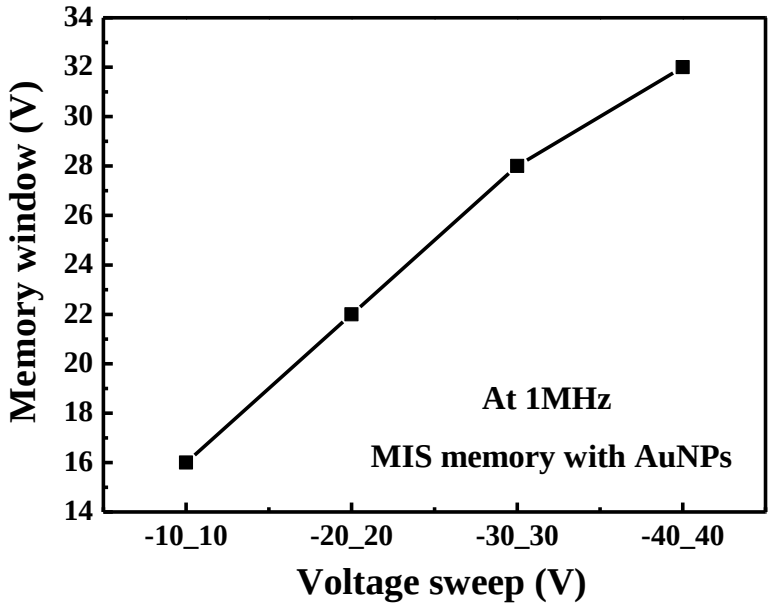


Figure 4.15: *The memory window versus voltage sweep range for MIS memory device with AuNPs floating gate.*

4.3.3 OMIS memory devices with PMMA as insulator and SWCNTs as floating gate

Single walled carbon nanotubes (SWCNTs) have extraordinary properties, including high thermal conductivity [26, 27], low electrical resistance [28, 29] and high mechanical strength [30, 31]. SWCNTs have been explored world-widely as one of the most promising candidates for next-generation nanoelectronic devices [32, 33]. The performance of non-volatile memory effects of single walled carbon nanotube-based MIS structure is reported in this section.

4.3.3.1 Fabrication process

The structure of MIS memory device based on SWCNTs as a floating gate, Al/PMMA/SWCNTs/PMMA/pentacene/Au, is similar to that of Figure 4.11 with SWCNTs used as the floating gate instead of the gold layer. The fabrication method and conditions that were described in Section 4.3.1.1 were also applied to the fabrication of this device. A floating gate between two layers of PMMA was deposited using layer-by-layer (LbL) technique, which is a deposition technique based on a charge reversal to build up bi-layer assemblies of oppositely charged molecules. Details of this technique were reported in Section 3.3.4. The materials used and the deposition process is explained in details in section 3.4.2.3(b). The control device without SWCNTs was also fabricated.

4.3.3.2 Electrical characterisation

The *C-V* characteristics for SWCNTs-based MIS memory structure, and the control device (without SWCNTs), are shown in Figure 4.16. All the measurements reported in this work were performed at 100 *kHz* and at a voltage scan rate of 2 $V\,s^{-1}$. In each measurement, the double scan was started from a negative gate voltage and swept towards inversion region and then back to negative voltages. The *C–V* curve for the control device (blue solid line in Figure 4.16) with a reference structure of Al/PMMA/pentacene/Au reveals the typical characteristics of an MIS structure based on a p-type semiconductor, with a flat–band voltage of about -8 *V* and full semiconductor depletion at about 1 *V*. Negligible hysteresis is evident at the double voltage sweep rate used for the control device. The measured value of the accumulation capacitance for the reference device was 72 *pF*. This was consistent with the insulator thickness ~ 330 *nm* and the device area 9 x 10^{-3} cm^{-2}.

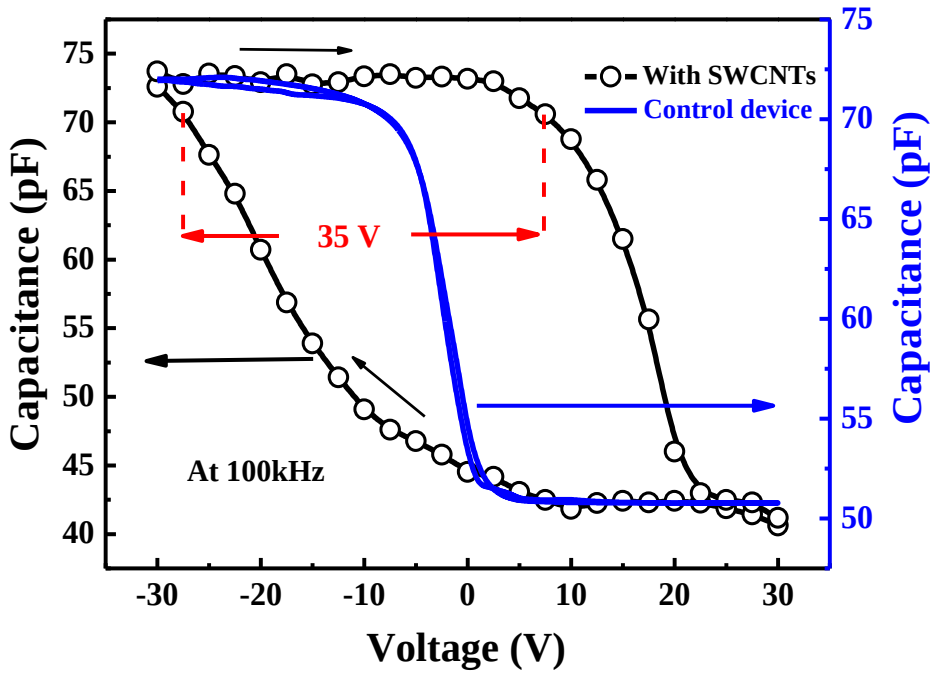


Figure 4.16: *C–V characteristics at 100 kHz for the SWCNTs-based MIS memory (open circle and line) and control (blue solid line) devices.*

On the other hand, the additional layers of SWCNTs within the insulating stack to form an Al/PMMA/SWCNTs/PMMMA/pentacene/Au structure produced a very noticeable change in the flat–band voltage. Furthermore, on reversing the direction of the voltage scan, significant hysteresis and shift in the flat–band voltage were observed in the *C–V* curve with a large memory window $\Delta V \sim 35$ *V*, which is indicative of the charge storage in the SWCNT layers, larger than memory devices based on Au thin layer and with AuNP devices. These results are consistent with our recent *C-V* studies [20, 21, 25, 34] and Mabrook et al.'s *C-V* studies [22, 35].

Although the operating voltage of ± 30 *V* for the MIS memory device based on SWCNTs was lower (which is favourable to organic memory applications) than for the devices based on Au thin layer and Au nanoparticles, the shift in flat–band voltage was larger. The clockwise hysteresis after sweeping the accumulation was associated with electrons charging of floating gate or polarization of the insulator. Furthermore, it is

clearly seen in Figure 4.16 that the hysteresis centred on approximately 0 *V*, which indicates that the devices may operate at lower voltages.

As shown in Figure 4.17, the memory window in the MIS memory device based on SWCNT floating gate increased as the voltage sweep range increased from ± 10 *V* to ± 30 *V* sweep voltage. This was as the expected memory behaviour, where the charges stored increase as the applied voltage is increased. However, when the voltage sweep reached ± 40 *V*, the memory window slightly decreased due to the polarisation effect from the SWCNTs stack.

The amount of charge stored in the carbon nanotubes *Q* can be estimated depending on the C_i, which gives a value of 8.2×10^{-9} $F\ cm^{-2}$, and the ΔV_{FB} was 35 *V*; the maximum number of charge carriers stored is approximately 1.7×10^{12} cm^{-2}. It is clear that although the hysteresis produced in the SWCNTs device was larger than the hysteresis of devices with Au thin layer and AuNPs, all have similar memory capacity.

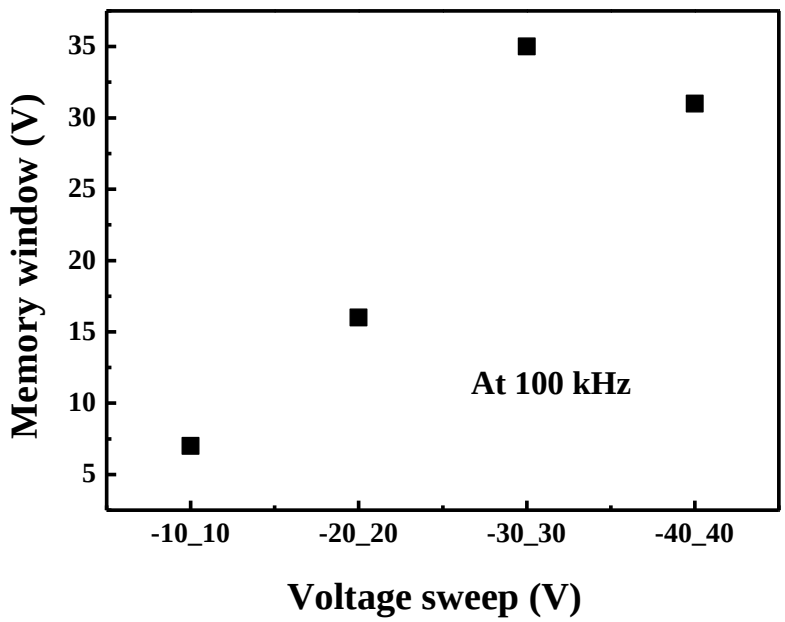


Figure 4.17: *The memory window (flat–band voltage shift) versus voltage sweep range for SWCNT-based MIS memory devices.*

4.3.4 OMIS Memory devices with PVP as insulator and AuNPs as floating gate

4.3.4.1 Fabrication process

The schematic diagram for the structure of Al/PVP/AuNPs/PVP/pentacene/Au MIS memory device is shown in Figure 4.18. This device was fabricated by thermally evaporating 70 *nm* thickness of an Al gate electrode through a shadow mask (Figure 3.10 C (a)) onto a clean glass substrate. 25% (wt) of PVP solution in isopropanol (IPA) was spin coated on top of the gate electrode to a thickness of about 250 *nm* at 3000 *rpm*. The spun PVP layer was then baked at 80 °C for 10 min to form a uniform layer. The floating gate, AuNPS, was deposited using the self-assembly methods described in Section 3.4.2.3. Prior to deposition of a pentacene semiconducting layer, another thin film of PVP was deposited onto the floating gate. Pentacene was thermally evaporated at a rate of 0.03 $nm\ s^{-1}$, through a shadow mask (Figure 3.10 C (b)) to a thickness of ~ 50 *nm*. Following the deposition of pentacene, the contact was defined by thermal evaporation of ~ 50 *nm* of Au through a shadow mask (Figure 3.10 C (c)) after about seven days of the pentacene evaporation.

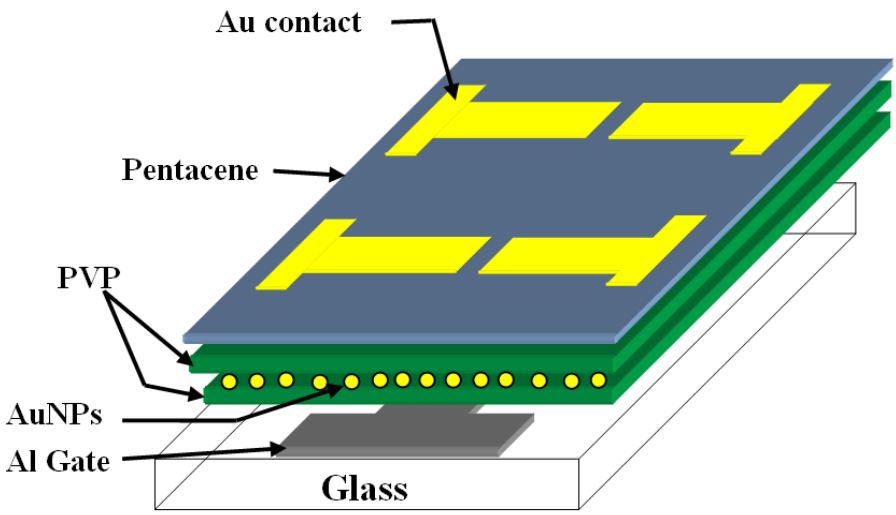


Figure 4.18: *Schematic diagram of Al/PVP/AuNPs/PVP/pentacene/Au MIS memory structure.*

4.3.4.2 Electrical characterisation

Figure 4.19 shows the *C-V* characteristics for the control and memory devices using double voltage sweep of ± 20 *V* and ± 40 *V* with 1 $V\ s^{-1}$ scan rate (starting from accumulation to deep depletion and back to accumulation) at (a) 100 *kHz* and (b) 1 *MHz*. The *C-V* characteristics of the control device were the same as for the device shown in Section 4.2.3.3. The area of this memory device was different from that of the last three MIS memory devices; it was 6.5 x $10^{-3}\ cm^2$.

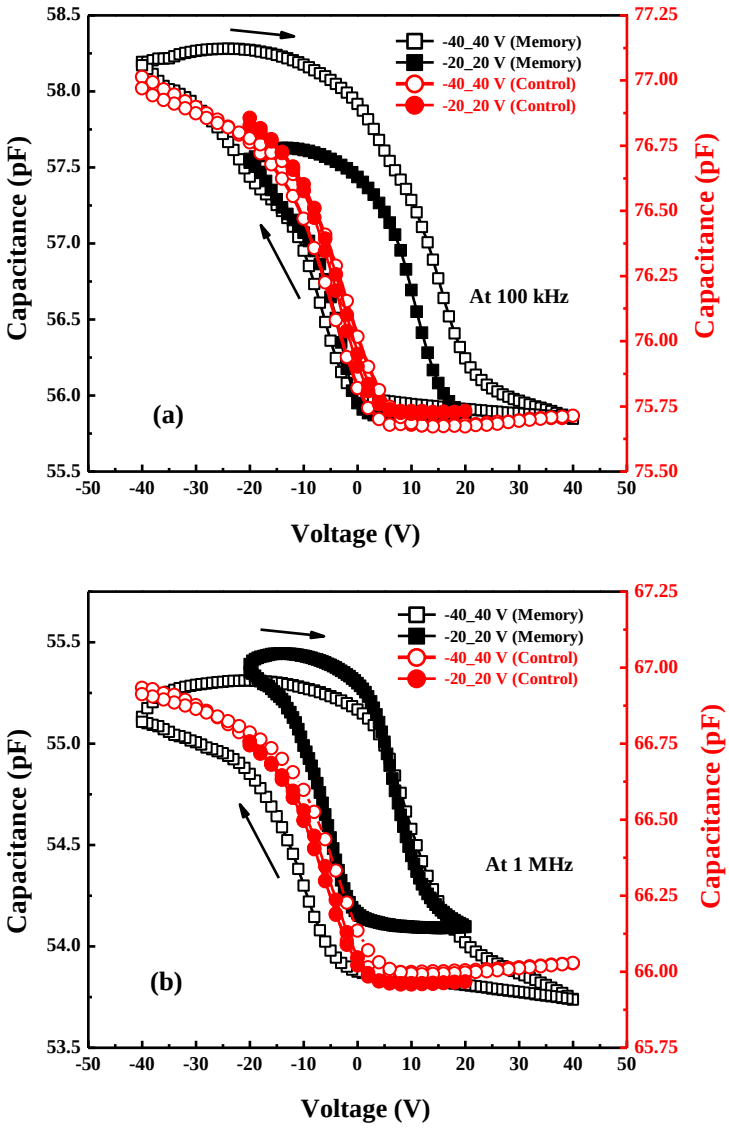


Figure 4.19: *C-V characteristic curves of double voltage sweep ± 20 V and ± 40 V for Al/PVP/AuNPs/PVP/Pentacene/Au MIS memory structures.*

The memory device with Al/PVP/AuNPs/PVP/pentacene/Au structure exhibited clear hysteresis in its *C-V* characteristics compared to the control devices, as shown in Figure 4.19. The flat–band voltage shifted to a more positive value after applying accumulation voltages, resulting in a clockwise hysteresis as electrons originating from the Al gate become trapped in the AuNPs layer. The hysteresis in the *C–V* curve at 100 *kHz* showed a memory window ΔV of about 19 and 40 *V* for voltage sweep ± 20 *V* and ± 40 *V*, respectively (increase of charges stored as the applied voltage was increased). Also, when the frequency was increased to 1 *MHz*, there was not much deference in the ΔV values; as they were about 18 and 38 *V* at voltage sweeps ± 20 *V* and ± 40 *V*, respectively. Generally, these values of hysteresis window were larger than the hysteresis reported for devices based on another floating gates, Au thin layer and SWCNTs. On the other hand, when the values of ΔV were compared with the memory device which had the same floating gate material (AuNPs) but with different dielectric layers (PMMA instead of PVP), a very small difference was found, thus strongly indicating that charge storage in the AuNPs layer was responsible for the hysteresis effects.

Furthermore, like the behaviour in the AuNPs-based memory devices based on PMMA, the values of capacitance of this memory device was less than of the control device (as depicted in Figure 4.19). Another important feature was that the hysteresis curves (except for *C-V* curve with ± 20 *V* at 1 *MHz* frequency) were cantered close to 0 *V*, which is an important advantage for the memory devices, as it indicates that the devices may operate at lower voltages. The calculated values for the insulator capacitance C_I was 58.27 *pF* for voltage sweep ± 40 *V*, at 100 *kHz*. Moreover, the average value of the series resistance R_S is about 12 Ω. The thicknesses of the insulator and semiconductor layers were estimated to be about 495 and 40 *nm*, respectively. The thickness of the insulator layer was almost doubled due to the second PVP layer deposited on top of the AuNPs film to complete their confinement. This also indicates, and in a similar fashion as for the devices in Section 4.3.2.2, that the presence of AuNPs did not change the PVP dielectric properties such as permittivity. The amount of charge stored *Q* in the gold nanoparticles can be estimated depending on the C_i, which give a value of 8.9×10^{-9}, 8.5×10^{-9} *F* cm^{-2}, and the ΔV_{FB} was ~ 18.5, 39 *V* for ± 20, ± 40 *V*

sweep range, respectively. The number of charge carriers stored was estimated to be approximately 1.2×10^{12} and 1.7×10^{12} cm^{-2}. It is clear that although the hysteresis produced in the AuNPs device based on PVP insulator layers is larger than the hysteresis of other devices (Au thin layer, SWCNTs and AuNPs based on PMMA as the insulator), the memory capacity is almost similar.

4.4 Summary

Fabrications and characterisation of different pentacene-based organic metal-insulator-semiconductor (OMIS) capacitor and memory structures have been examined. The topographies of the organic thin films have been presented to establish the required evaporation parameters that lead to fabricate high-performance pentacene-based devices. AFM images were used to extract the surface morphology of the deposited pentacene film as a function of PMMA and PVP for different thicknesses. Deposition of 50 nm thicknesses of pentacene film with a deposition rate of 0.03 nm s^{-1} on 300 nm of PMMA, or on 350 nm of PVP dielectric layers, was found to produce a large, uniform and condense grains of pentacene.

Fabrications and characterisation of three different types of OMIS capacitors, using different organic insulators and contact materials were investigated. The *C-V*, *G/ω-V* and *C-f* plots were obtained for the OMIS devices, and all devices exhibited the classical p-type-based MIS behaviour with a transition from accumulation to depletion regions. All the MIS devices exhibited negligible hysteresis in the C-V characteristics. The doping concentration N_a for the Al/PMMA/pentacene/Au MIS capacitor device is larger than for the MIS capacitor device with PEDOT:PSS as the top contact; this means that an increase in conductivity in this device is due to the higher concentration of carriers available for conduction.

The fabrication and characterisation of PMMA or PVP-based organic flash memory devices with MIS structure using a thin film of Au layer, Au nanoparticles and single walled carbon nanotubes as a floating gate, has been demonstrated. The AuNPs were deposited using a self-assembly deposition method, where layer-by-layer deposition technique was used for deposition of SWCNTs. Negligible hysteresis was exhibited for control devices without floating gate, while memory devices exhibited clear hysteresis;

this was indicative of the memory effect and charge storage in the memory devices. The clockwise hysteresis in the memory devices (except for the Au thin film-based memories) was attributed to the charging and discharging of the electrons from the aluminium gate. Also the hysteresis was centred close to 0 V (in particular when SWCNTs are used as floating gate), which means that a lower operation voltage could be used to charge the memory. A higher applied sweep voltage leads to a wider hysteresis and larger memory window. A memory window of about 40 V was achieved at a ± 40 V sweep range for the AuNPs floating gate memory devices based on PVP. Whereas, at the same voltage sweep, the memory windows for devices based on PMMA with Au thin layer and AuNP floating gates were 22 V and 32 V, respectively. The memory window reached 35 V at ± 30 V sweep range for the SWCNTs-based memory devices. However, all tested devices show a memory capacity in the range of 10^{12} cm^{-2}. Table 4.2 summarise the electronic properties of the memory devices.

Table 4.2: *The electrical parameters of the OMIS memory devices.*

Structure	Memory window (*V*)	Voltage sweep (*V*)	*Q* (cm^{-2})
Thin Au layer/PMMA	22	± 40	1.07 x 10^{12}
AuNPs/PMMA	32	± 40	0.7 x 10^{12}
SWCNTs/PMMA	35	± 30	1.8 x 10^{12}
AuNPs/PVP	40	± 40	1.7 x 10^{12}

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Chapter 5

Organic Thin Film Transistor (OTFTs)

5.1 Introduction

Recently, pentacene-based organic thin film transistors (OTFTs) have attracted much interest for large area electronics applications; this is due to its high performance which is comparable or even better than amorphous Si TFTs [1]. This is the reason that led us to choose pentacene as the active layer for OTFTs. The fabrication and characterisation of bottom-gate, top-contacts pentacene-based (OTFTs) are investigated in this chapter. The bottom gate has mostly been used for most OTFTs because of the difficulty to deposit a gate dielectric onto the pentacene layer [2].

Two types of organic gate dielectric materials have been used in this study. These materials are poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP). OTFTs were stored under vacuum at room temperature in between measurements to reduce the effects of atmospheric degradation. Some devices were measured in air in order to investigate the effect of the environment on the device operation conditions.

Stability of OTFTs was investigated as devices were retested after two months of fabrication, as well as after one year. As for repeatability, the fabrication process was repeated several times. The influence of scaling of the channel length and width and the effect of voltage applied on the transistor characteristics are also studied in this chapter.

On the other hand to measure the endurance properties of these OTFTs, we applied bias stress on the devices after more than one year of fabrication. This process has

three stages; applied constant gate bias at different stress times, applied different gate bias stress at constant stress time and applied constant gate bias at constant stress time with different drain bias stresses. The experimental details and electrical characteristics of these devices are presented and discussed in this chapter. All measurements were performed at room temperature and voltage scanned in forward and reverse directions in order to investigate the presence of hysteresis.

5.2 PMMA-based OTFTs

5.2.1 Device fabrication

The fabrication of OTFT devices with the structure of Al/PMMA/pentacene/Au (as shown in Figure 5.1) was achieved by thermal evaporation of 50 *nm* layer of Al through a shadow mask (Figure 3.10 B (a)) on glass substrate as the gate electrode. A 300 *nm* thick insulating layer was deposited by spin coating of 10% (wt) anisole solution of PMMA with spin speed of 5000 *rpm* on top of the gate electrode, and then cured at 120°C for 1 hour. Pentacene was thermally evaporated through a shadow mask (Figure 3.10 B (b)), as the organic semiconductor, to a thickness of 50 *nm* at a deposition rate of 0.03 $nm\ s^{-1}$. Then after 7 days, a 50 *nm* layer of Au was deposited through a shadow mask (Figure 3.10 B (c)) by thermal evaporation as source and drain top contacts. All film preparation and materials evaporation techniques were discussed in chapter 3.

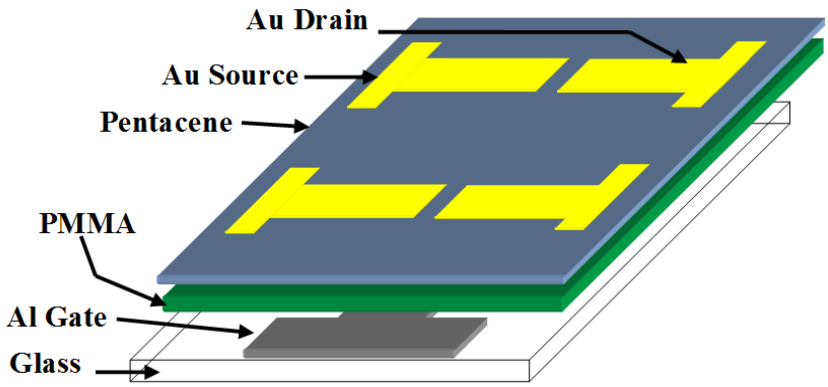
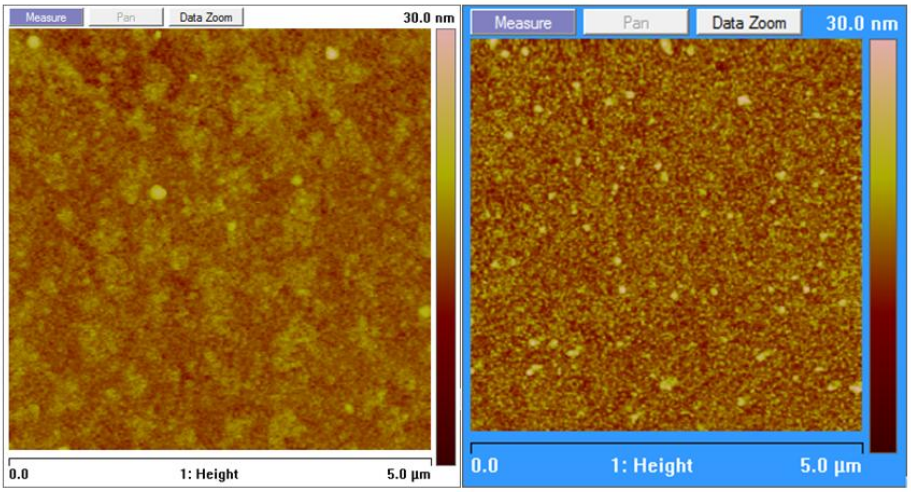


Figure 5.1: *Schematic diagram of PMMA-based OTFT structure.*

5.2.2 Device optimisation

To optimise the fabrication process, source and drain Au contacts were evaporated directly after the evaporation of pentacene for some OTFTs, while other devices left under vacuum for 2, 3, 5, 7, and 9 days before the evaporation of Au electrodes. Results show that pentacene films left to stabiles for seven days resulted in much improved transistors behaviours. Atomic force microscopy (AFM) images were used during this investigation to extract the morphology of the deposited Au electrodes for both sets of devices. The surface morphology of 50 *nm* gold contacts grown on 50 *nm* pentacene film varied significantly for the two fabrication processes, as shown in Figure 5.2, where (a) Au electrodes evaporated after seven days and (b) directly after the evaporation of pentacene. Uniform, crack-free and pinhole-free film was observed when the gold contacts were deposited after seven days, as shown in Figure 5.2(a). In contrast, surface defects were observed when Au electrodes deposited directly after the evaporation of pentacene, as shown in Figure 5.2(b). As the same pentacene deposition process and thickness were used for both sets of devices, the difference in Au morphology is attributed to the time used to allow pentacene to stabilise before the evaporation of Au electrodes.



(a) **(b)**

Figure 5.2: *AFM images of 50 nm gold contacts grown on 50 nm pentacene, (a) deposited after 7 days of the deposition of pentacene, and (b) directly evaporated after the evaporation of pentacene.*

The impact of pentacene stability and the period pentacene stored before gold contacts deposition is also clear in the electrical characterisation of OTFTs. Figure 5.3 shows the electrical characteristics for both set of devices. Figure 5.3 (a) and (b) represent the output and transfer characteristics, respectively, of the optimised OTFTs, where Au contacts deposited after seven days of the deposition of pentacene. Figure 5.3 (c) and (d) shows the output and transfer characteristics, respectively, for OTFTs, where Au contacts are deposited directly after the formation of pentacene.

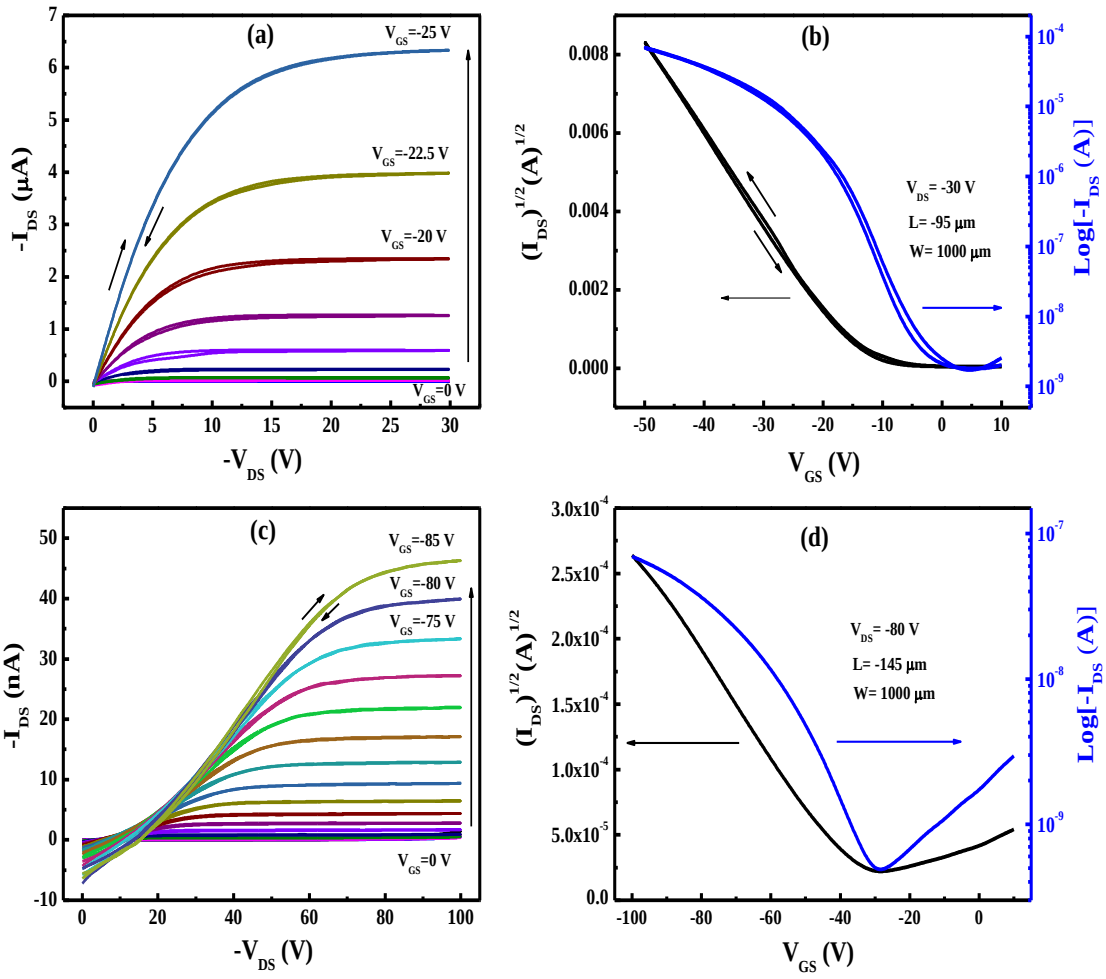


Figure 5.3: *The output and transfer characteristics of PMMA- based OTFTs, (a) and (b) for optimized devices and, (c) and (d) for devices with Au contacts evaporated directly after the evaporation of pentacene.*

It is clear from Figure 5.3 (a) and (b) optimised devices show higher current and mobility as well as negligible gate leakage current, while devices with Au contacts evaporated directly after the deposition of pentacene show large leakage current, low mobility and very high operating voltage. As a result of the above characterisations, all the devices in this work were fabricated so that source and drain Au contacts were evaporated seven days after the evaporation of pentacene.

5.2.3 Electrical characterisation of OTFTs

To explain the structure of the slides, Figure 5.4 shows the top view of slide (slide 2 (s2) for example) with four devices (d1, d2, d3 and d4) having four different channel lengths L= 50, 100, 150 and 200 μm, respectively, and with a channel width W = 1000 μm for all devices. The area of the top Au electrode was 9×10^{-3} cm^2. In practical, the actual channel lengths were slightly different from the above lengths due to the evaporation alignments of Au electrodes, therefore actual lengths were estimated from the optical microscopic images taken after the evaporation of source and drain. The field-effect mobility of TFTs shows higher calculated values if the channel length increased, this proportional relation is predicted by Equation 2.17, where drain-source current I_{DS} vary with width/length ratio (W/L).

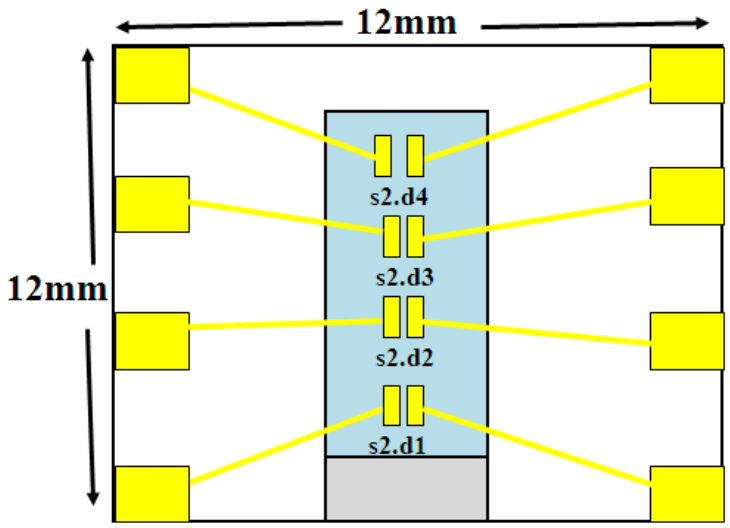


Figure 5.4: *Top view of the slide samples OTFT devices.*

Figure 5.5 shows typical (a) output and (b) transfer characteristics of the fabricated OTFTs with Al/PMMA/pentacene/Au device structure. The plot of output characteristics, Figure 5.5(a), represents a typical dependence of drain–source current (I_{DS}) on the drain–source voltage (V_{DS}) of p-type OTFTs with respect to gate bias from 0 to -40 *V* with steps of 2.5 *V*. While the transfer characteristic, Figure 5.5(b), represents the dependence of I_{DS} on gate–source voltage (V_{GS}) for V_{DS} = -30 *V*.

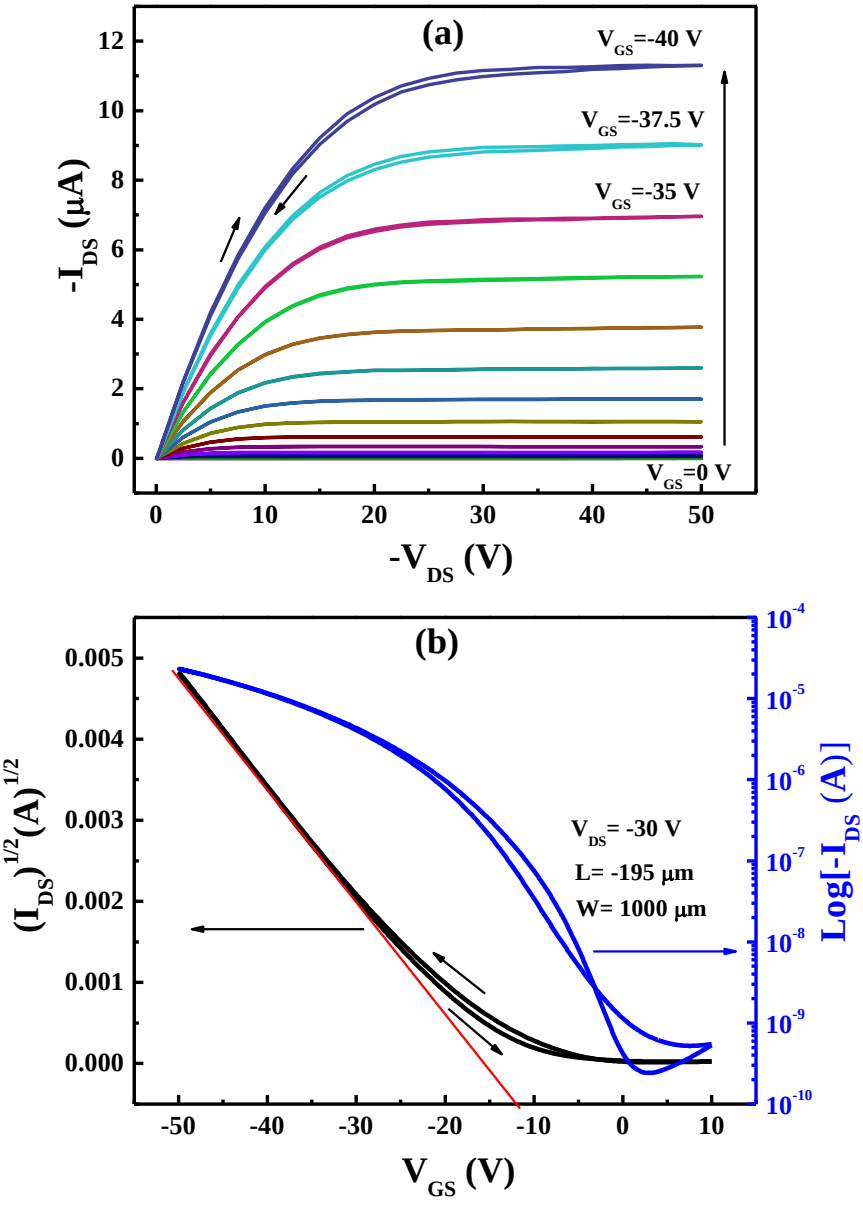


Figure 5.5: *Electrical characteristics of OTFT. (a) The output characteristics with respect to the gate bias from 0 to −40 V with steps of −2.5 V and (b) transfer characteristics at V_{DS} = -30 V.*

Plots in Figure 5.5(b) are given in the form of both $(I_{DS})^{1/2}$ versus V_{GS} and $log(I_{DS})$ versus V_{GS}. The channel length (L) and width (W) for this device are 195 and 1000 μm respectively. These characteristics were performed directly after fabrication (fresh device). For all characteristics, voltage sweep in both directions (for example V_{DS} from 0 to 50 V and back to 0 V for the output characteristics in Figure 5.5(a)) conducted to explore the presence of hysteresis in these devices. It is important to note that the device in Figure 5.5, shows negligible (or no) hysteresis in the output and transfer characteristics.

The field-effect mobility, μ, of the devices can be estimated from Equation (2.17) [3-5],

$$I_{DS} = \frac{\mu W C_i}{2L}(V_{GS} - V_T)^2$$

where C_i is the insulator capacitance per unit area (Equation (2.8)) and V_T is the threshold voltage. The threshold voltage represents the value of V_{GS} at which the transistor is turned on and can be determined from the intercept of the plot of $(I_{DS})^{1/2}$ versus V_{GS}, as shown in Figure 5.5 (b) (red line). The calculated value of μ in the saturation region for this OTFT is 0.825 $cm^2 V^{-1} s^{-1}$, with a threshold voltage of -13 V, and on/off current ratio of 1.06 x 10^5. The calculated parameters of this device are applied in Equation (2.17) in order to insure that the calculated values are in agreement with the practical measurements. Using a dielectric constant, ε_{Ins}, of ~ 2.6 for PMMA [6], the calculated current I_{DS} is found to be 2.3 μA for V_{DS} = -30 V and V_{GS} = -27.5 V (for example).This value of current is very close to the practical value of I_{DS} for the output or transfer characteristics in Figure 5.5. This indicates that the calculated parameters are accurate with a small error margin of less than 5%. This relatively high μ can be attributed to the surface morphology of pentacene film as evidenced by the AFM images in Figure 4.3 (B), in Chapter 4. The large crystalline pentacene grains which are accompanied with decrease in the density of grain boundaries, and thus a decrease in the density of trap-sites, results in enhanced mobility [7].

Table 5.1 summarizes an example of the electrical parameters of OTFTs devices fabricated on the same substrate in a structure similar to the structure in Figure 5.4. As shown in this table, for the devices that stored under vacuum between measurements

(S1), the average values of mobility μ = 1.09 $cm^2 V^{-1} s^{-1}$, the on/off current ratio is 2.75 × 10^5 and the threshold voltage V_T = -14 *V*. However, for the devices that exposed to air during measurements, they operate at higher gate-source voltages (V_{GS} = -70 to -100 *V*, and V_{DS} = -50 to -60 *V*) as shown in table 5.1 (S2 in blue colour rows).

Table 5.1: *The electrical parameters for set of OTFTs measured directly after fabrication.*

Slide No.	Device No.	μ ($cm^2/V.s$)	On/off current ratio	V_T (V)	L(μm)	V_{DS} (V)	V_{GS} (V)
S1	d1	1.28	4.1 x 10^5	-16	58	-30	-50
S1	d2	1.32	3.17 x 10^5	-14	98	-25	-50
S1	d3	0.94	2.7 x 10^5	-13	165	-30	-50
S1	d4	0.825	1.06 x 10^5	-13	195	-30	-50
S2	d2	0.36	2.26 x 10^4	-24	95	-60	-100
S2	d3	0.29	3.6 x 10^4	-18	113	-50	-100
S2	d4	0.61	1.0 x 10^2	-16	137	-60	-70

In these devices, the average values of μ decreased to about 0.42 $cm^2 V^{-1} s^{-1}$, while the on/off current ratio decreased about one order of magnitude (1.9 × 10^4) although there is considerably increase in V_T to the average of -19.3 *V*. These changes indicate clearly the effect of environment on device operation, and the devices are within practical limits of absorption of impurities from the ambient environment such as moisture, light exposure, and air.

As for the calculated values of V_T, the theoretical dependence of the thin film transistor parameters on V_T is quite complex. Assuming there is no difference in work function between the semiconductor and the gate metal, V_T can be estimated by [8].

$$V_T = \mu \left| \frac{Q_S}{C_i} \right| \tag{5.1}$$

where Q_S is the effective total charge (which may be positive or negative) per unit area at the dielectric-semiconductor interface at zero gate voltage and C_i has already been defined. The number of mobile and fixed charges at the interface state charge and dielectric layer will be contributing to make up the charge Q_S. The increase of V_T for the devices stored in air may be related the presence of positive fixed charges in the dielectric layer and from C_i at the flat-band voltage which is equivalent to the metal-insulator-semiconductor capacitors. These charges resulted from the absorption of impurities from the ambient environment.

To further study the stability of the fabricated devices, OFETs in Table 5.1 were characterised again after two months of fabrication. All OTFTs were stored under vacuum at all time. Table 5.2 shows the characteristics of the same OTFTs in Table 5.1 measured after two months of fabrication.

Table 5.2: *The electrical parameters for the set of OTFTs measured after two months of fabrication.*

Slide No.	Device No.	μ ($cm^2/V.s$)	On/off current ratio	V_T (V)	$L(\mu m)$	V_{DS} (V)	V_{GS} (V)
S1	d1	1.13	3.8×10^4	-8	58	-25	-50
S1	d2	1.28	4.1×10^4	-10	98	-30	-50
S1	d3	0.56	4.15×10^4	-8	165	-25	-50
S1	d4	0.858	3.11×10^6	-8	195	-40	-50
S2	d2	0.27	1.54×10^4	-18	95	-50	-100
S2	d3	0.24	1.63×10^5	-20	113	-40	-100
S2	d4	0.41	1.93×10^5	-22	137	-60	-100

Generally, there is slight decrease for the average value of mobility (0.96 $cm^2\ V^{-1}\ s^{-1}$), threshold voltage (-8.5 *V*), and the on/off current ratio changed slightly to about 8.07×10^5 for devices stored and measured under vacuum. It is important to note that all devices are in good working conditions and show very small degradation in electrical

properties. Similar effects are shown for devices stored under vacuum and measured in air (blue colour rows in Table 5.2) as the mobility decrease slightly.

Figure 5.6 shows an example of the output and transfer characteristics of OTFT (sample S1-d2), which has the highest mobility in our study; (a) and (b) measurements made just after the fabrication, and (c) and (d) after two months of fabrication.

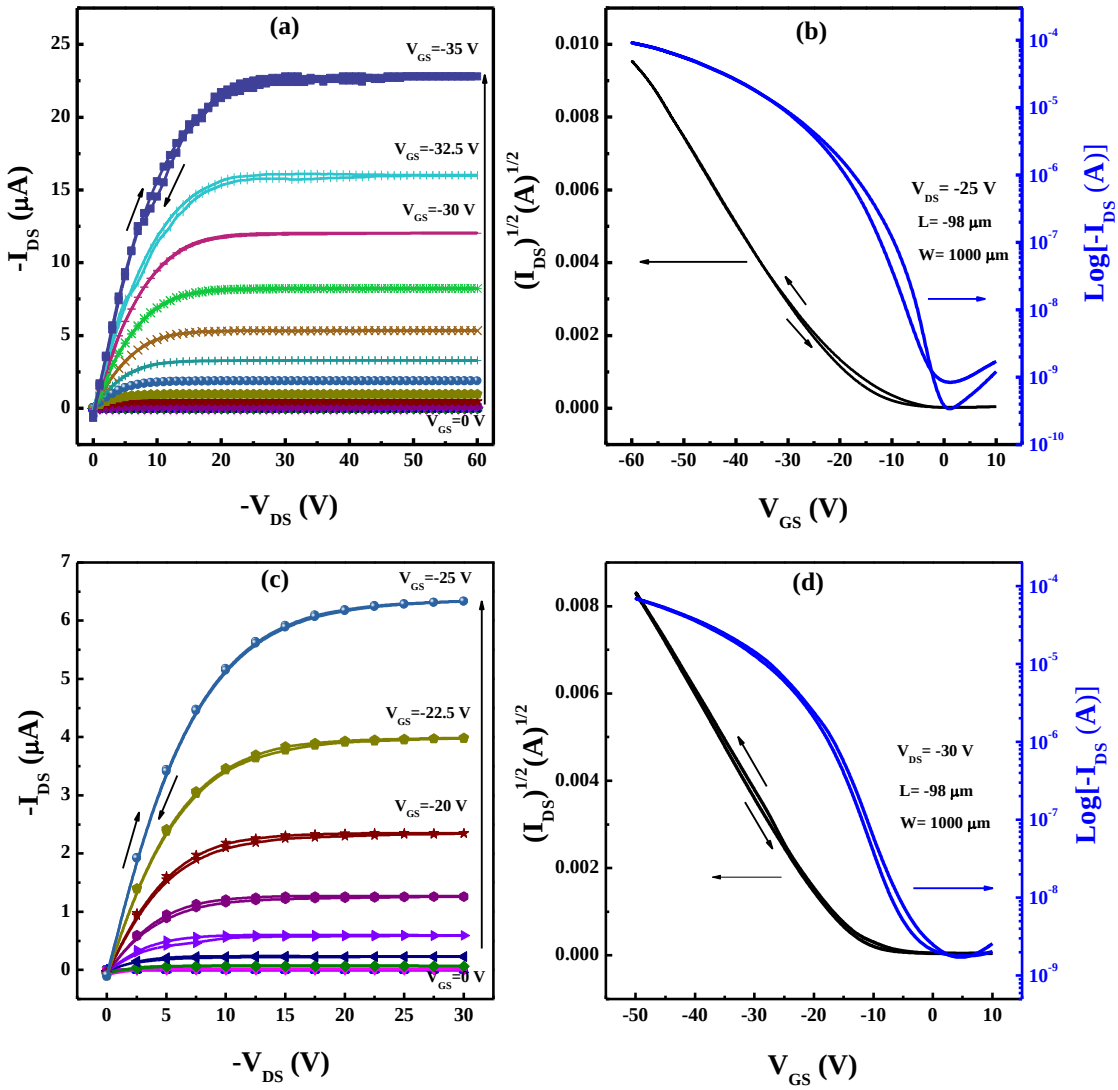


Figure 5.6: *The output and transfer characteristics of OTFT measured (a) and (b) just after fabrication, (c) and (d) after two months of fabrication.*

The test conditions maintained the same for all devices, the gate bias for the output characteristics start from 0 to -35 *V* with steps of 2.5 *V* for the fresh device and from 0 to -25 *V* with steps of 2.5 *V* after two months of fabrication. The channel length and width are 98, 1000 μm, respectively. As shown in tables 5.1 and 5.2, there is a slight decrease of mobility of this device from 1.32 to 1.28 $cm^2\ V^{-1}\ s^{-1}$, and the threshold voltage shifted from -14 to -10 *V*, the on/off current ratio decreased one order of magnitude.

Negligible hysteresis is observed in both output and transfer characteristics for the device. The calculated parameters of this device are applied in Equation (2.17), and the calculated current I_{DS} is found to be 13.5 μA at V_{DS} = -25 *V* and V_{GS} = -30 *V* for fresh device and I_{DS} = 1.2 μA at V_{DS} = -30 *V* and V_{GS} = -17.5 *V* for the device measured after two months. These values of current are very close to the practical values of I_{DS} for the output and transfer characteristics in Figure 5.6 for both measurements.

Figure 5.7 shows another example of OFTT performance at high operating voltages of fresh and after two months of fabrication devices, respectively. Figure 5.7 (a) and (b) are the characteristics of OTFT measured directly after fabrication, (c) and (d) are behaviour of the device after two months of fabrication. The channel length and width are 95, 1000 μm, respectively. The device is working at high voltages after two months of fabrication with the same test conditions. The field-effect mobility of the device in saturation region and threshold voltage show a slight decrease from 0.36 to 0.27 $cm^2\ V^{-1}\ s^{-1}$ and from -24 to -18 *V*, respectively. A small negligible hysteresis is observed when the direction of voltage scan is reversed in transfer characteristic of the device after two months (Figure 5.7(b)). This may be related to a relatively small number of defects in the device due to the surrounding environment.

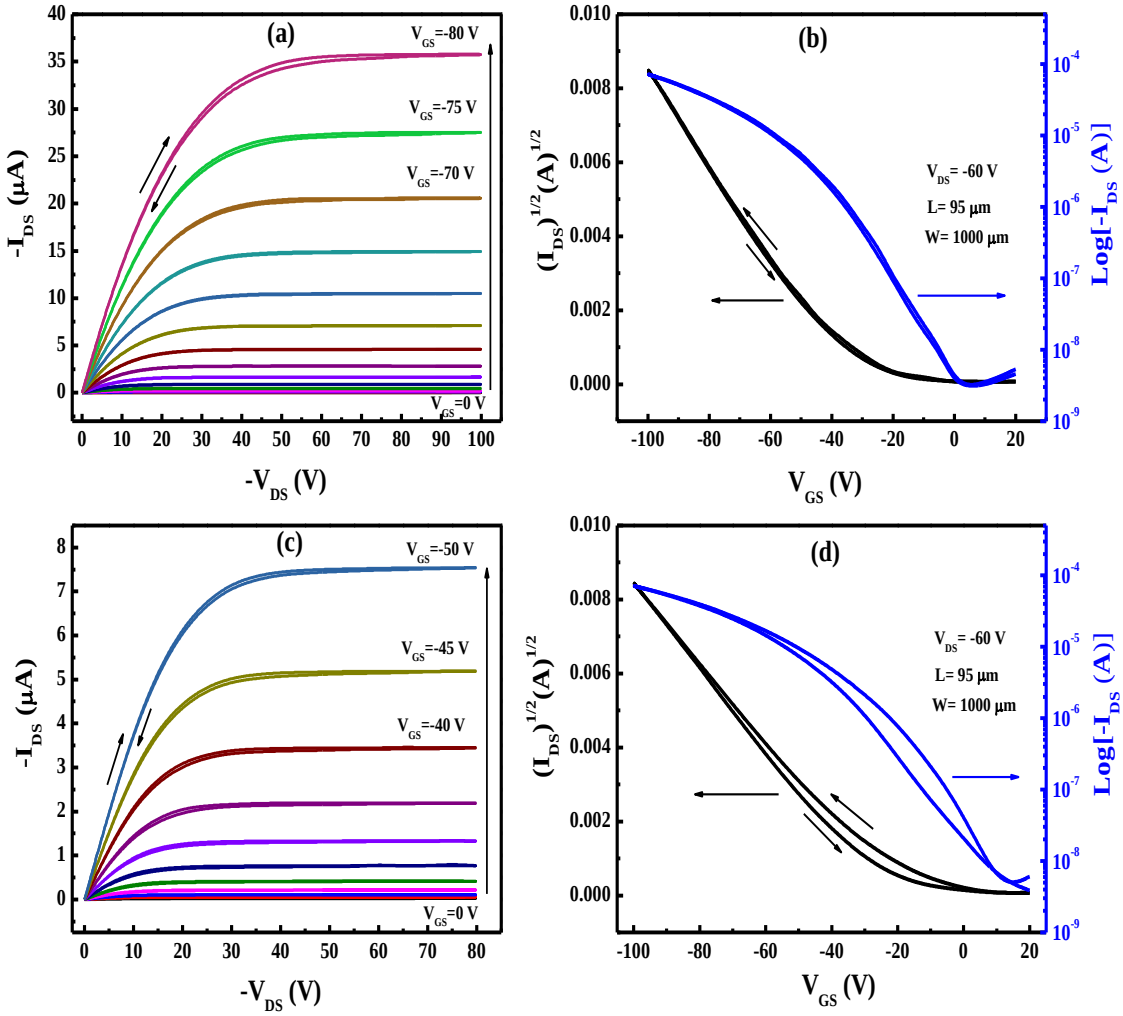


Figure 5.7: *The output and transfer characteristics of an OTFT operated at high voltages. (a) and (b) measured directly after fabrication, (c) and (d) measured after two months of fabrication.*

Some OFETs were also tested after one year of the fabrication. Figure 5.8 shows the (a) output and (b) the transfer characteristics for the device S1-d4 measured after one year of the fabrication, where the output and transfer characteristics for the fresh device are shown in Figure 5.5.

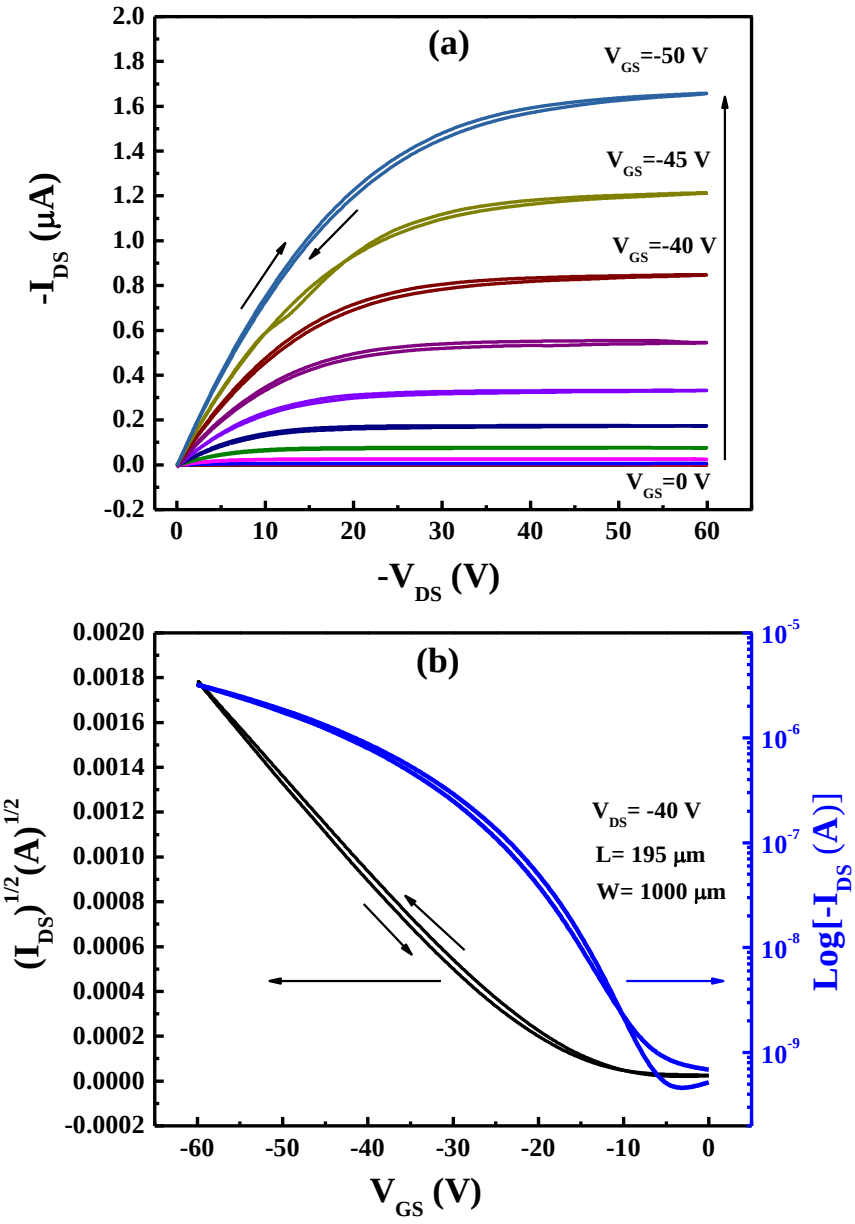


Figure 5.8: *OFET characteristics measured after one year of fabrication. (a) The output characteristics with respect to the gate bias from 0 to −50 V with steps of −5 V and (b) transfer characteristics for device S1-d4 in Table 5.1.*

It is clear that after one year of fabrication, the OTFT device is operating with rather good performance; it exhibits typical p-type FET behaviour, negligible hysteresis is observed for both the output and the transfer characteristics and also no significant drain off-set current exists in this device. However, the calculated value of μ decreased

to 0.102 $cm^2\ V^{-1}\ s^{-1}$ and the on/off current ratio decreased to 7.06×10^3, while the threshold voltage V_T = -16 *V*.

5.3 Repeatability study of OTFTs fabrication

In order to study the repeatability of the fabrication processes of OTFTs, similar process repeated to produce similar devices as in Table 5.1. Similar fabrication conditions were used with the same thickness layers. Table 5.3 shows a set of fabricated devices. Although the channel lengths should have similar values as in Table 5.1, but due to the typical mask alignments problem in the deposition of Au electrodes, shorter channel lengths are evident in Table 5.3. This problem is expected as all fabricated devices show different actual channel length and the optical microscopic estimation is required. High mobility values are obtained in these samples, as μ reached as high as 1.24 $cm^2\ V^{-1}\ s^{-1}$. It is clear from Table 5.3 the electrical parameters calculated for these newly fabricated devices are very similar to the calculated values for the set of devices in Table 5.1.

Table 5.3: *The electrical parameters for a new set of OTFTs (second fabrication).*

Slide No.	Device No.	μ ($cm^2/V.s$)	On/off current ratio	V_T (V)	$L(\mu m)$	V_{DS} (V)	V_{GS} (V)
S3	d1	0.85	5.1×10^3	-4	40	-30	-40
S3	d2	0.98	1.6×10^4	-5	80	-40	-50
S3	d3	1.12	1.7×10^4	-9	135	-40	-50
S4	d1	1.15	1.07×10^3	-10	35	-40	-45
S4	d2	1.24	1.4×10^4	-7	65	-40	-47.5

Figure 5.9 shows examples of the output and the transfer characteristics for OTFTs from the second fabrication. Figure 5.9 (a) and (b) show the characteristics for the device S3-d3 in Table 5.3, while the characteristics for device S4-d2 are shown in

Figure 5.9 (c), (d). These two devices were fabricated on different substrates to show reproducibility. Relatively high carrier mobility between 0.85 and 1.24 $cm^2\ V^{-1}\ s^{-1}$ achieved for OTFTs in Table 5.3, which can be considered among the highest mobility values that are reported for pentacene-based OTFTs. As previously explained, there is close relationship between the improved μ and the crystal grain of the pentacene. It has been reported that reducing the number of crystalline grains per unit area is necessary to achieve high mobility in OTFTs devices [9], where grain boundaries scatter the carriers, leading in lower mobility [10]. The high grain size of the pentacene film can be attributed to the prior purification of the pentacene material and to adjusting the deposition parameters and modification of the dielectric surface by chemically processing the gate insulator [9, 11].

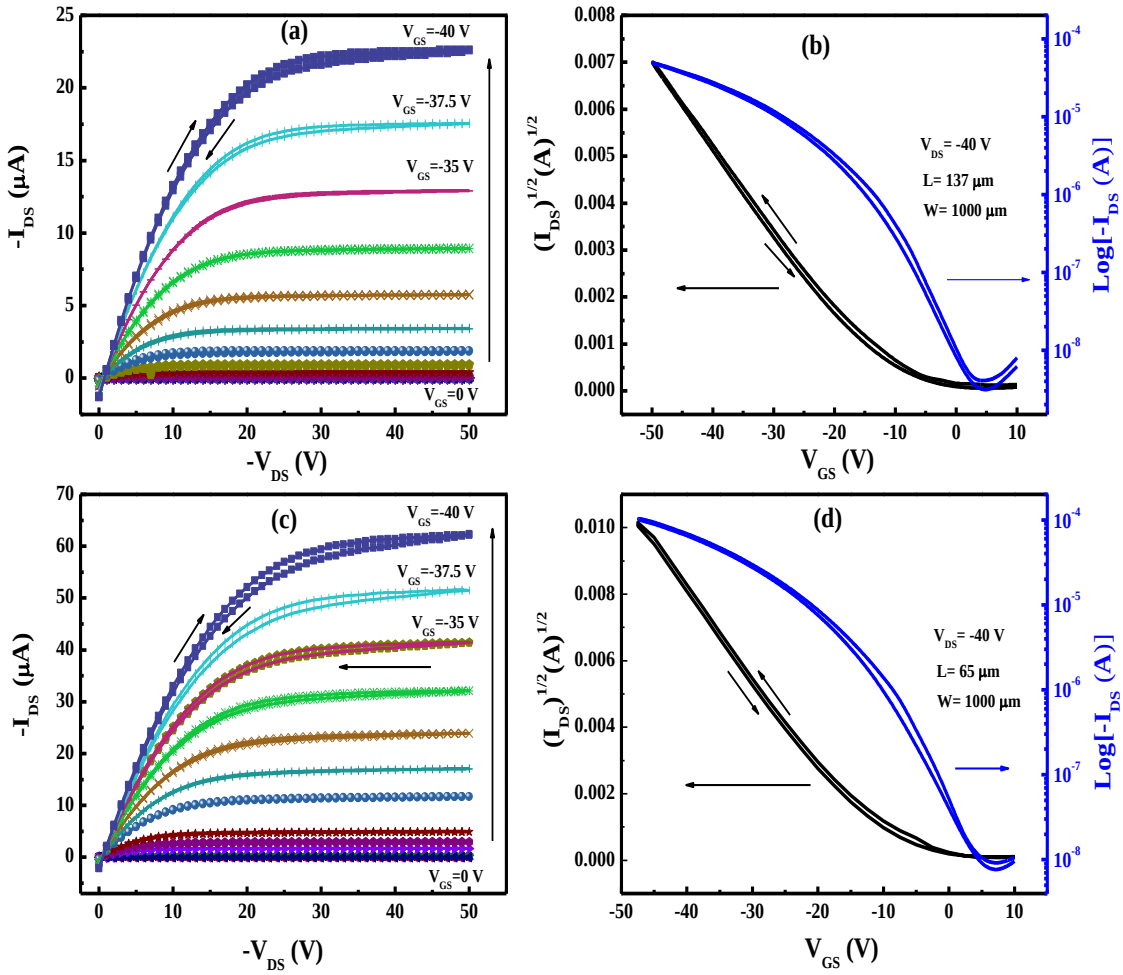


Figure 5.9: *The output and transfer characteristics of OTFTs. (a) and (b) for device S3-d3 and (c) and (d) for device S4-d2.*

From to the results of this investigation, OTFTs exhibited almost no hysteresis in both characteristics as the forward and reverse scans produced almost superimposed characteristics. The recorded output characteristics confirmed that each of these devices exhibited typical p-type filed effect transistor (FET) behaviour i.e. for a negative V_{GS} larger than the V_T, the current increased linearly at low V_{DS} values, suggesting an efficient hole injection from the pentacene/Au contacts [12] as well as good saturation region at high V_{DS} when $V_{DS} \geq V_{GS}$ - V_T due to the pinch-off of the channel. As can be observed from Tables 5.1-3, high drain currents are measured for OTFTs for both set of devices that were stored under vacuum or those exposed to air during the measurements. Also it is clear that no significant drain off-set current exists amongst these devices, indicating a low gate current [13] and hence good gate dielectric behaviour [14].

The calculated values of the field-effect mobility, on/off current ratio and threshold voltage for these particular devices compare very favourably with published data for pentacene/PMMA-based OTFTs [4, 15–18]. For example, Yun et al. [4] reported μ = 0.33 $cm^2 V^{-1} s^{-1}$ and V_T = -4 *V*, Chung-Ming et al. [18] have measured μ = 0.31 $cm^2 V^{-1} s^{-1}$ and V_T = -16.8 *V*, Huang et al. [17] reported μ = 0.24 $cm^2 V^{-1} s^{-1}$ and V_T = -6.3 *V*, Li et al. [16] give μ = 0.5 $cm^2 V^{-1} s^{-1}$ and V_T = -1.5 *V*, and Singh and Mazhari [15] have measured μ = 0.22 $cm^2 V^{-1} s^{-1}$ and V_T = -10.42 *V*. The mobility values of 0.33 and 0.31 $cm^2 V^{-1} s^{-1}$ at the gate voltage of -30 and -50 *V* that where obtained by Yun et al. [4] and Chung-Ming et al. [18] fit well with the values that are calculated for samples operated at higher V_{GS} (-100 V) and the measurements are performed in air.

5.4 PVP-based OTFTs

5.4.1 Device fabrication

OTFT devices were fabricated with Al/PVP/pentacene/Au structures. An aluminium gate was thermally evaporated on a glass substrate through a shadow mask (Figure 3.10 C (a)) to a thickness of 70 *nm*. 50% (wt) of PVP solution in isopropanol (IPA) was spin coated to a thickness of about 350 *nm* at 5000 *rpm*. The spun PVP layer was then baked at 80 °C for 10 min to form the thin film. Pentacene was thermally

evaporated through the shadow mask (Figure 3.10 C (b)) at a rate of 0.03 $nm\ s^{-1}$ to a thickness of ~ 50 *nm*. Finally, after seven days, source and drain top gold contacts were thermally evaporated to 60 *nm* thickness through a shadow mask (Figure 3.10 C (c)). The devices were stored under vacuum at room temperature in between measurements to reduce the effects of atmospheric degradation. The OTFT structure for these devices is identical to the structure shown in Figure 5.1 with PVP as the insulating layer instead of PMMA.

5.4.2 Electrical characterisation

Figure 5.10 shows the plots of the (a) output and (b) transfer characteristics of PVP-based OTFT with channel width (W) = 3000 μm, channel length (L) = 197 μm. In each measurement, forward and reverse voltage scans are performed. The output characteristic exhibits linear behaviour at low V_{DS}, and the saturation behaviour in this device is observed at high V_{DS} and low V_{GS} values (V_{GS} from 0 to ~ -30 *V*, as shown in Figure 5.10(a)). Figure 5.10(b) shows the transfer characteristic of the device, measured at V_{DS} = -50 *V*. The plots are given in the form of both $(I_{DS})^{1/2}$ and $log(I_{DS})$ as a function of V_{GS}. Negligible hysteresis is evident on reversing the bias scan direction; this may be related to a relatively clean interface between the PVP and the pentacene. Clockwise direction is evident in this hysteresis, which is a result of a slow polarization in the organic gate insulator [19]. The field-effect mobility, on/off current ratio and threshold voltage for this device were 0.65 $cm^2\ V^{-1}\ s^{-1}$, 2.66 × 10^2 and -7 *V* respectively.

Reference to the parameters from this device, it can be found that the magnitude of the field-effect mobility and on/off current ratio produced by the PMMA-based OTFT was significantly better than that of a similar OTFT with PVP at the same gate-source voltage V_{GS} range. This is supported by the morphology study explained in Chapter 4 as pentacene films evaporated on PMMA show greater crystalline grains than the one grown on PVP (as shown in Figure 4.9(c) and (d)).

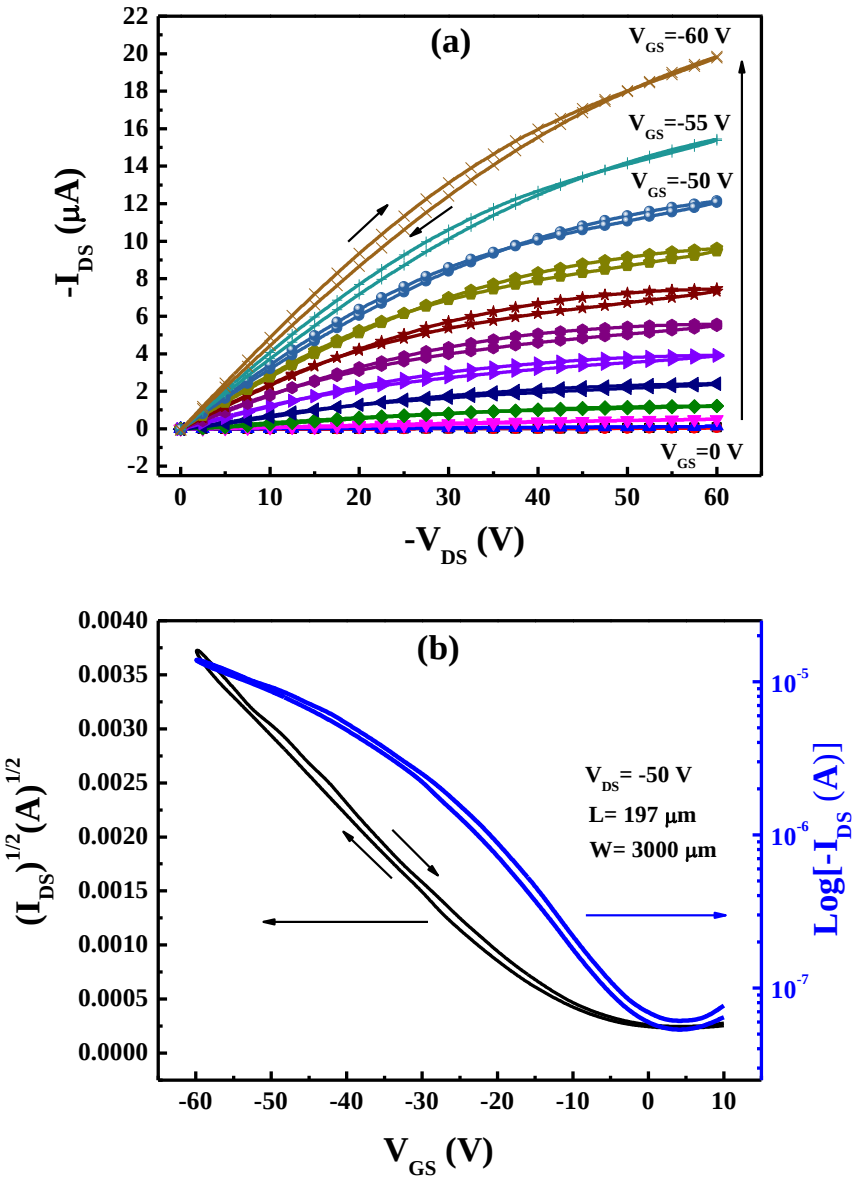


Figure 5.10: *(a) The output characteristic of PVP-based OTFT (b) The transfer characteristics of the OTFT.*

In addition, from Figure 5.10, it is clearly seen that I_{DS} for this device did not really reached the saturation at high V_{GS} voltages compared to that observed in the OTFTs devices with PMMA. The hysteresis that occurs in PVP-based device (as shown in Figure 5.10(b)) is another factor to consider compared to PMMA-based devices when it comes to the fabrication of organic memory devices. In fact for almost all PMMA-based devices output and transfer characteristics show no hysteresis. This is an

important factor in this research as the objective is to fabricate organic memory devices as will be discussed in the next chapter. U. Zschieschang et al. [20] and S. C. Lim et al. [21] reported similar hysteresis behaviour appears in PVP-based OTFTs. Therefore, for organic memory transistors PMMA is the main insulator used in this work.

5.5 Bias stress effect in pentacene-based OTFTs with PMMA as insulator

The effect of bias stress in pentacene-based organic thin film transistors with PMMA used as insulator for different stress conditions is investigated in this section. Understanding the bias stress effect is important for practical circuit applications. The change over time for the threshold voltage of the transistor is a result of creating carrier channel in a field-effect transistor due to applying gate-source voltage. Such change is termed the "bias-stress effect". Applying a positive gate-source voltage to the n-channel transistor causes its threshold voltage to shift towards more positive values, while a negative gate-source voltage applied to a p-channel transistor produced a negative threshold voltage shift. The bias stress effect is attributed to the trapping of channel carriers, these trap states located in the gate dielectric, or at the semiconductor/dielectric interface [22, 23].

It is well-known that applying bias stress on OTFTs leads to change of the output current with time, and under continuous application of gate bias, devices will show instability [24, 25]. In the attempt to extend the devices lifetime, maintain stability and to measure the endurance properties of OTFTs after one year of fabrication, the effect of applied bias stress on some devices with different conditions are investigated in the following section.

5.5.1 Initial test

Prior to the measurements of the gate bias stress tests; the initial transfer characteristic is measured for PMMA-based OTFTs. The bias stresses are applied to device S1-d4 in

Table 5.1 after one year of fabrication. The term "initial device" will be used to describe the devices before the bias stress test. The current–voltage (*I*–*V*) characteristic of the fresh device (Al/PMMA/pentacene/Au) just after fabrication was shown in Figure 5.3. The calculated value for field-effect mobility of the fresh device was 0.825 $cm^2\ V^{-1}\ s^{-1}$, the threshold voltage was -13 *V*, and the on/off current ratio was 1.06 x 10^5. The output and transfer characteristics of the initial device are shown in Figure 5.8. The calculated value of μ was 0.102 $cm^2\ V^{-1}\ s^{-1}$, the on/off current ratio value was 7.06×10^3 and the threshold voltage was -15 *V* for the initial device. The channel width (*W*) and length (*L*) were 1000 and 195 μm, respectively. The bias stress test were measured using a Keithley 4140B picoammeter at room temperature (21 ± 2 ◦C). The mechanism of bias stress process is performed in three stages: first constant negative gate bias was applied at different stress time, then different bias stress were applied at constant stress time and finally constant negative gate bias at constant stress time was applied with different drain source voltages.

5.5.2 Gate bias-stress of -40 *V* at various stress time

To analyse the effects of bias stress on OTFTs, a bias gate stress was applied for a set of time, and after each stress time the transfer characteristics were measured. During bias stress, a constant gate source voltage of -40 *V* was applied at a constant drain-source voltage of 0 *V*. The test was repeated for a set time of 10, 100, 1000, 4000 and 8000 *s*.

Figure 5.11 shows the transfer characteristics of OTFT before and after a stress voltage applied to the gate (V_{GS}). Figures 5.11 (a) and (b) for $(I_{DS})^{1/2}$ versus V_{GS}, (c) and (d) for $Log(-I_{DS})$ versus V_{GS}. Plots (b) and (d) represent the enlarged plots of the same data in (a) and (c) in one direction sweep. The transfer characteristic for the initial device was represented by black solid line, where $t = 0$.

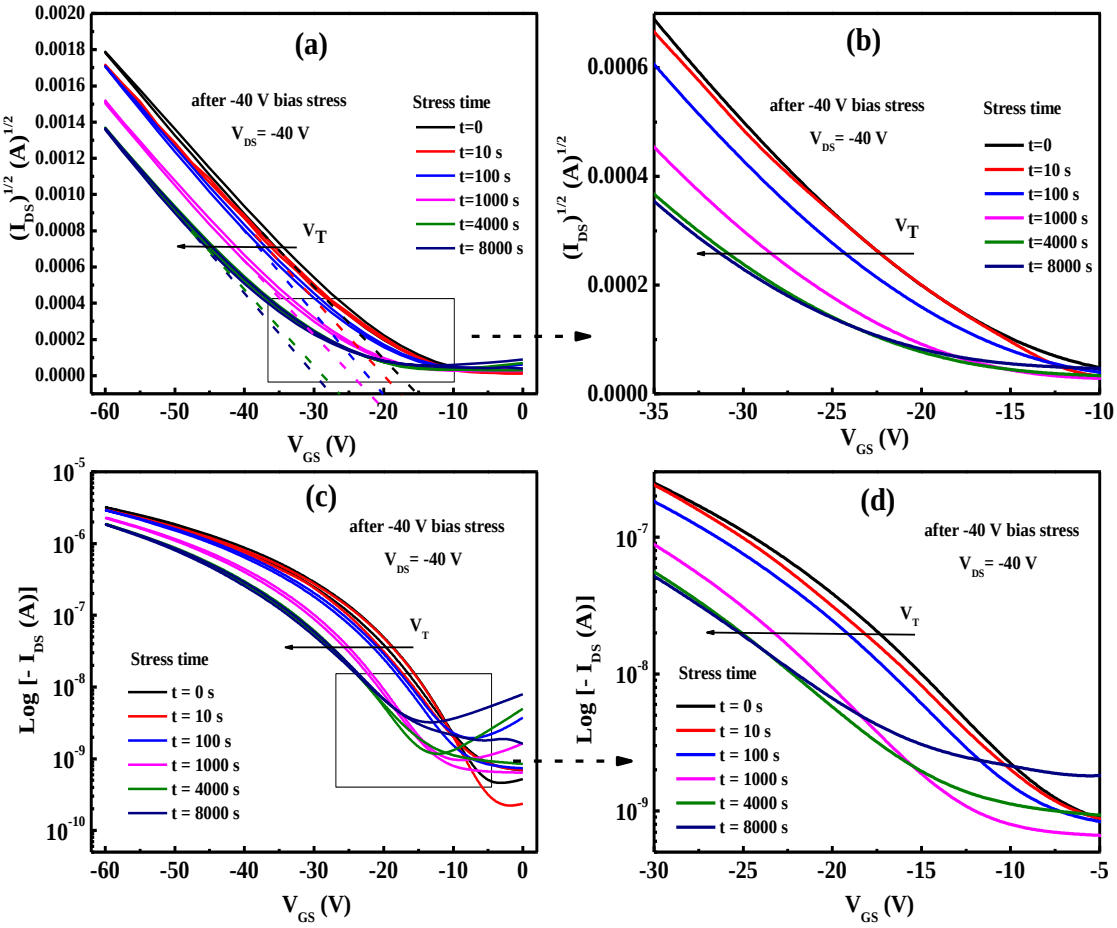


Figure 5.11: *Transfer characteristics after bias stress at V_{GS} = -40 V at different stress time (t). (a) and (b) for $(I_{DS})^{1/2}$ versus V_{GS}, (c) and (d) for Log(-I_{DS}) versus V_{GS}. (b) and (d) for the enlarged plots of the same data.*

The effect of increasing bias stress time is evident by shifting the threshold voltage V_T of the original transfer characteristics of the device in the negative V_{GS} direction. A large threshold voltage shift is clearly observed at stress voltage of -40 V for over 100 s. It is important to notice that there is a negligible hysteresis for the forward and reverse directions of the transfer characteristics, even for the bias stress of 8000 s. Furthermore, the shape of the transfer characteristics did not change with continuation of the stress time.

To describe the bias-stress effect, ΔV_T is commonly used for defining the magnitude of the shift V_T of the transfer characteristics after bias stress [22, 26, 27]. Theoretically,

under constant V_{GS} and V_{DS}, the time-dependence of bias stress-induced threshold voltage shift is typically described by a stretched exponential function [28-30]:

$$\Delta V_T(t) = [V_T(\infty) - V_T(0)]\left[1 - e^{-\left(\frac{t}{\tau}\right)\beta}\right] \quad (5.2)$$

Where $V_T(\infty)$ is the threshold voltage in the equilibrium state $(t \rightarrow \infty)$, $V_T(0)$ is the threshold voltage in the initial state, τ is the time constant, and β is the stretching parameter ($0 < \beta \leq 1$). For times beyond the time constant τ, the exponential response is fast, and this response become slower for times up to the time constant τ. The long time for bias-stress effect to settle indicates a slow trapping rate for the carriers located in the gate dielectric near the semiconductor/dielectric interface as suggested by Ryu at el. [22] and Libsch and Kanicki for a-Si:H TFTs [31] or trapped in the semiconductor [32].

Figure 5.12 shows the threshold voltage shift ΔV_T and saturation field-effect mobility μ of the tested OTFT as a function of stress time at a constant V_{GS}. During the continuous stress time the mobility decreased from 0.102 to 0.085 $cm^2\ V^{-1}\ s^{-1}$, and the threshold voltage shift in this device shows stretched-exponential time dependence. This is in agreement with the finding by other research groups [30, 31] as they found that stress voltages may result in a small decrease in mobility. We believe that the mobility degradation is not very significant compared to the degradation resulted from environment as shown in previous sections as well as the reported findings by [32, 33].

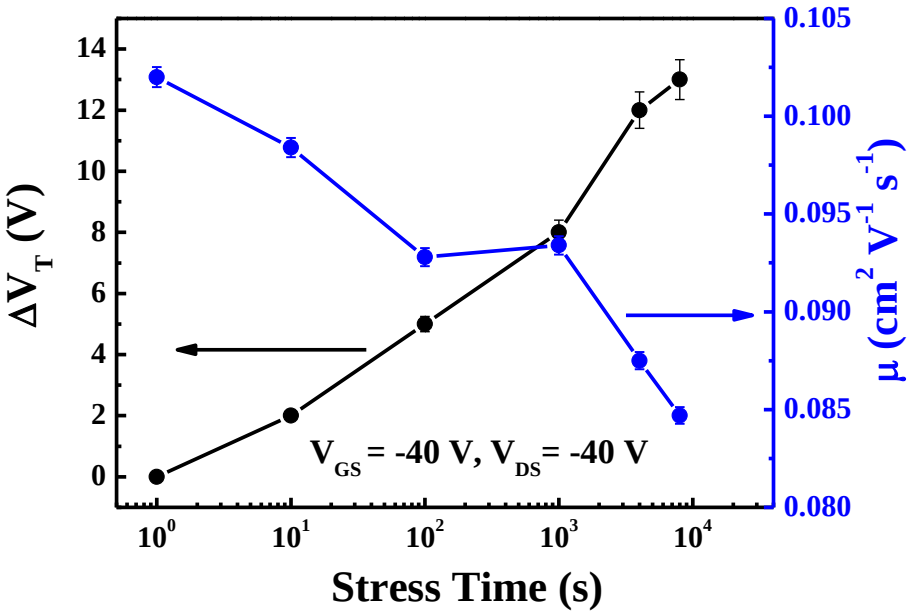


Figure 5.12: *The threshold voltage shift ΔV_T and saturation field-effect mobility μ versus stress time at V_{GS} = -40 V.*

5.5.3 Various gate bias-stress at 1000 s stress time

In this section, the measurements were taken for various stress V_{GS} conditions. During bias stress, a constant stress time of 1000 s is used for several gate bias-stresses (V_{GS} = -20, -30, -40, and -50 *V*), and after each bias stress the transfer characteristics were measured at V_{DS} = -40 *V*. The transfer characteristics are shown in Figure 5.13. The transfer characteristic for the initial device, without the effect of the bias stress is represented by black solid line. The threshold voltage shift was found to increase with increasing the gate-source voltage; the largest threshold voltage shift we have measured is 13 *V* (V_T = -28 *V* at a bias stress of -50 *V*). A similar behaviour of negligible hysteresis is evident between the forward and reverse direction of the transfer characteristics, and the shape of the transfer characteristics did not change.

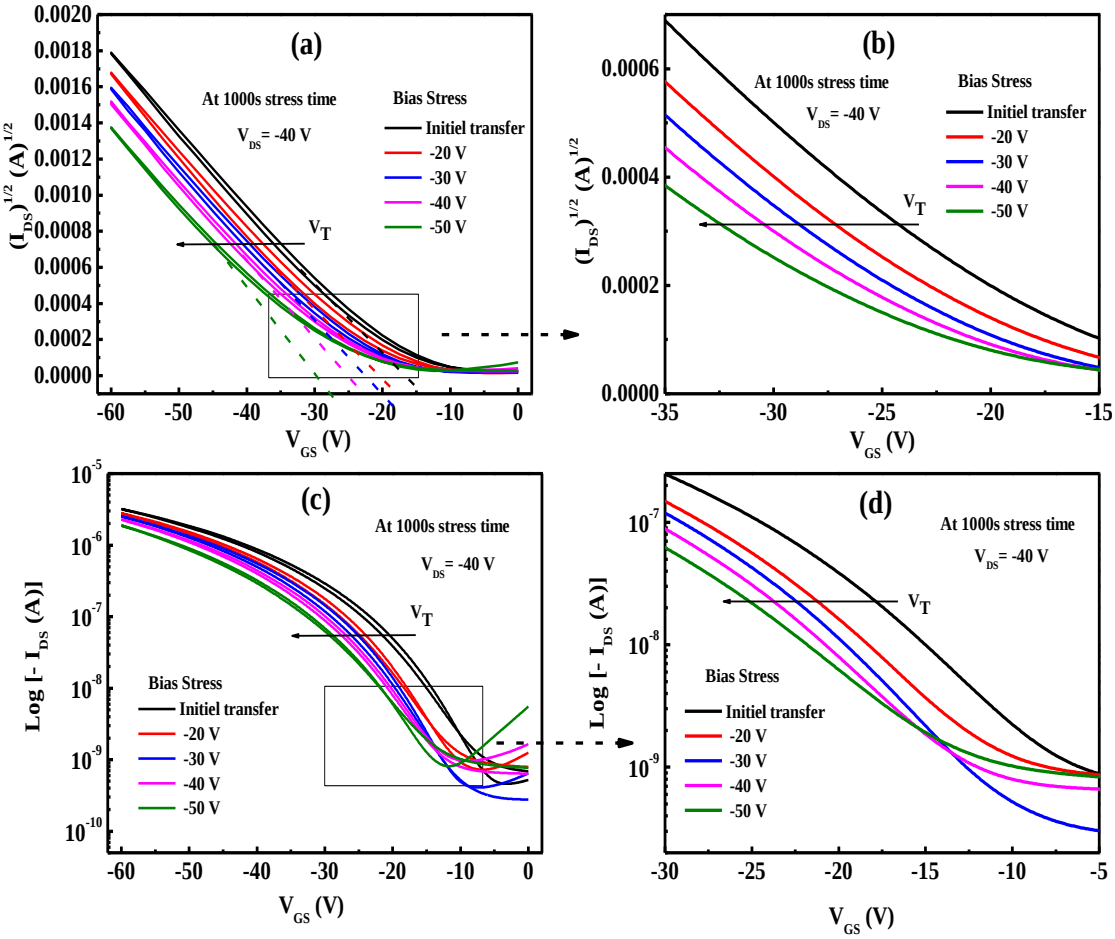


Figure 5.13: *Transfer characteristics as a function of gate bias stress at stress time t = 1000 s. (b) and (d) represent enlarged plots of (a) and (c) respectively.*

It is well documented in most reported OFETs, applying continuous gate bias stress results in several changes such as (i) the channel current decreases as a result of the shift in the threshold voltage [33, 34], (ii) reduction in charge carrier mobility, (iii) increase in the channel OFF current and/or (iv) clear hysteresis appear in the output and transfer characteristics [34]. First, second and third changes are in line with present results, as shown in Figure 5.13(a) and (b), the slope at the linear transfer curves decreased as the negative gate bias stress is continuously applied. This indicates that the current level decreased, not only from the shift of V_T, but also from the decreased μ (as will be presented later in Figure 5.14). On the other hand, devices show negligible hysteresis after all the stress voltages up to the last gate bias stress. This is again a very important behaviour for these devices, as it indicates that hysteresis in memory

transistors (covered in the next chapter) is a memory effect, and stress voltage have almost no influence on memory devices. This also reflects the high performance of present devices.

Figure 5.14 shows the threshold voltage shift ΔV_T and saturation field-effect mobility μ of the OTFTs as a function of gate bias stress at a constant stress time. As shown in Figure 5.14, the small decrease in mobility values (from 0.102 to 0.085 $cm^2\ V^{-1}\ s^{-1}$, comparable to those measured at stress time) are observed after the negative gate bias stress is applied. Several groups reported that deep traps with long discharge time would have effect on the mobility. Such traps have been observed in pentacene-based OTFTs [35-37].

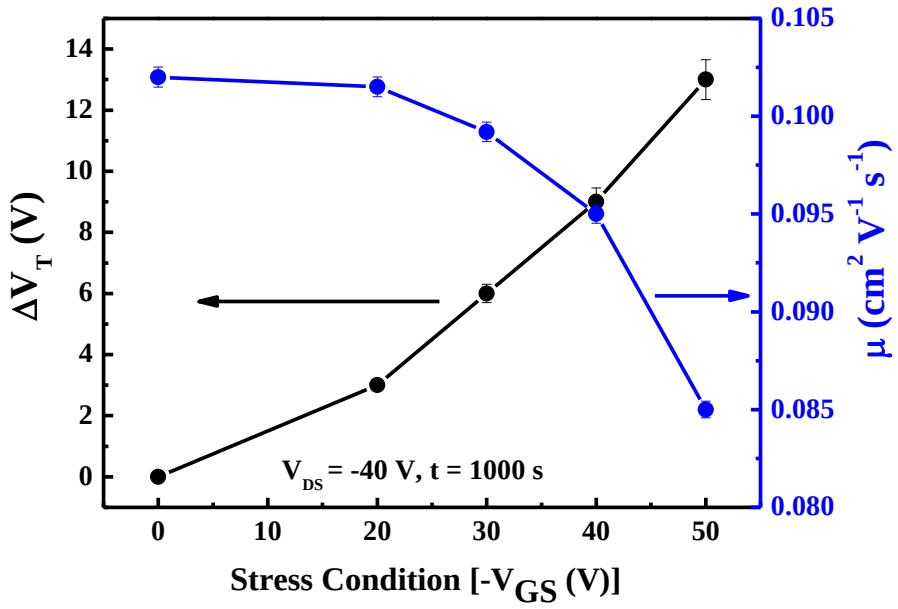


Figure 5.14: *Threshold voltage shift ΔV_T and saturation field-effect mobility μ versus gate bias stress at t = 1000 s.*

5.5.4 Various drain bias stress voltages at constants gate bias stress and stress time

To evaluate the dependence of ΔV_T on V_{DS} bias stress we performed the test at a constant V_{GS} = -40 *V* and a stress time of 1000 *s* for various V_{DS} (V_{DS} = 0, -5, -10, -15, -

20, -25, and -30 *V*). Figure 5.15 shows the effects of drain stress on transfer characteristics, the transfer characteristic for the initial device is represented by black solid line. Negligible hysteresis is evident between the forward and reverse direction of the transfer characteristics device without any change in the shape of transfer characteristics.

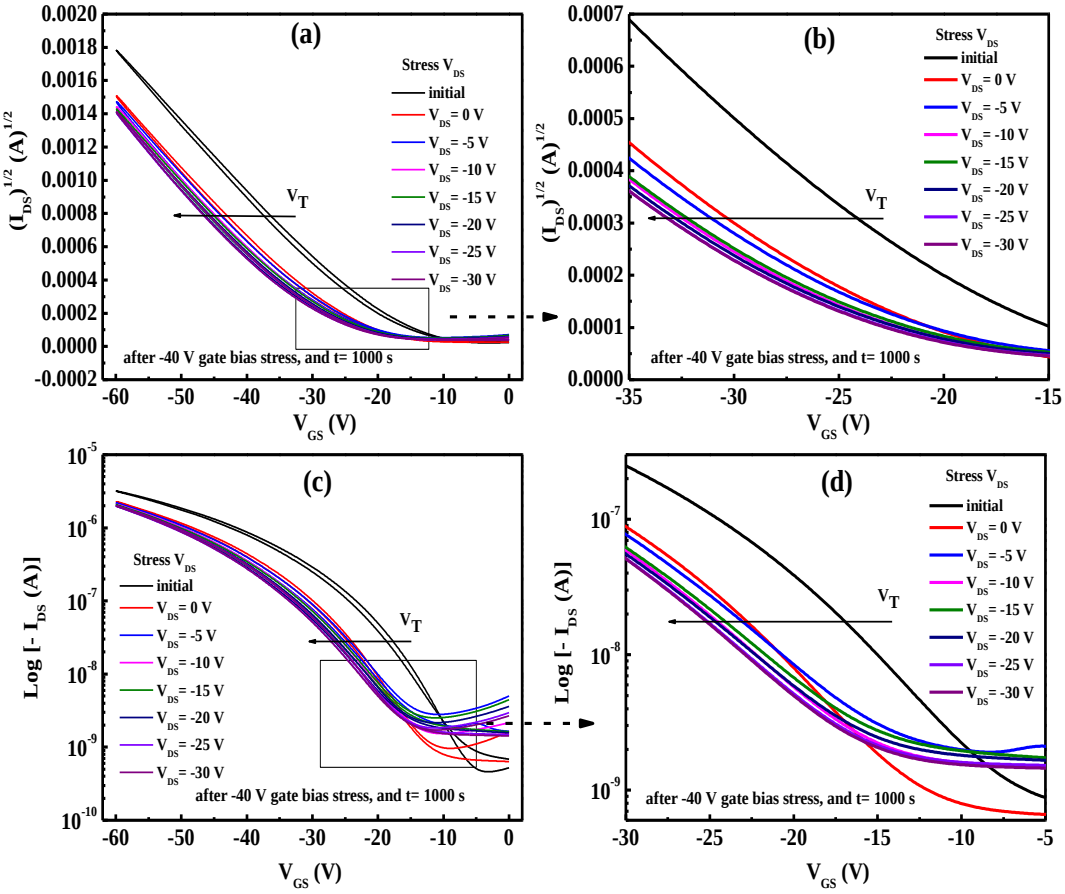


Figure 5.15: *Transfer characteristics after varying stress drain-sours voltages at V_{GS} = -40 V and t = 1000 s. (b) and (d) represent the enlarged plots of (a) and (c).*

The dependence of ΔV_T on the drain bias stress is shown in Figure 5.16; the drain bias stress increased from 0 *V* to -30 *V*, the resulting ΔV_T increased accordingly. It is notable that from Figures 5.15 and 5.16, the shifts of threshold voltage during drain

bias stress are slow compared to the shifts due to gate bias stress (Figure 5.14). How fast the V_T shifts during bias stress depends on the applied drain-source and gate-source voltages. High V_{GS} induces large density of charge carriers (positive charges) in the channel which increase the number of trapped carriers [37]. The trapped charge carriers will result in a large shift in V_T and increase ΔV_T. This is clearly evident in Figure 5. 14 when V_{DS} is equal to zero or at low values of V_{DS} stress voltages. When V_{DS} is increased, slower change in ΔV_T is observed in Figure 5.14. The reason for this kind of behaviour can be attributed to the release of trapped carriers as a result of the lateral electric field along the channel created by the drain-source voltage [37]. Also, larger V_{DS} induce electric field that counteracts the electric field induced by V_{GS} voltage in the area close to the drain electrode. Consequently, the trapped carrier density near the drain contact is reduced and the change in ΔV_T is also reduced. This is also supported by the fact that larger changes in ΔV_T observed in Figure 5.14 as $V_{DS} = 0$.

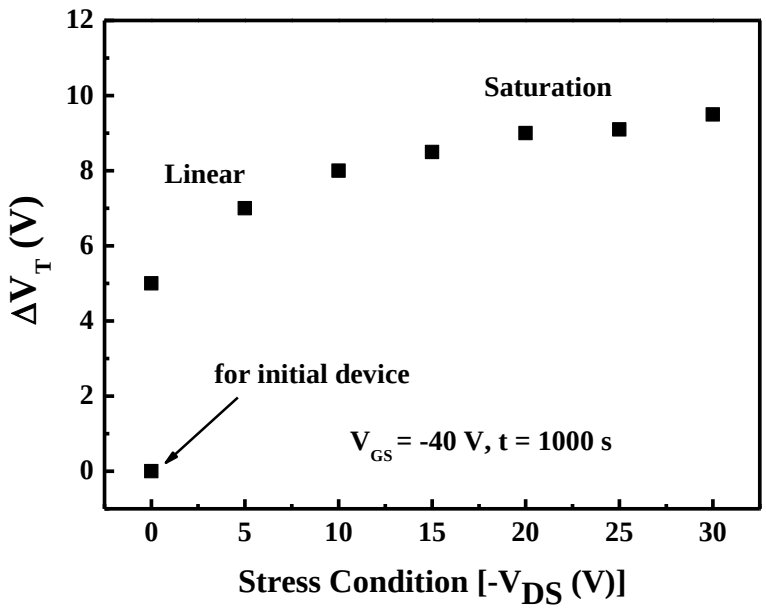


Figure 5.16: *Threshold voltage shift ΔV_T versus drain-sours stress voltage at V_{GS} = -40 V and t = 1000 s.*

It is worth mentioning that in most cases, it is possible to cancel these stress voltage effect by grounding the gate electrode and the threshold voltage is shifted back toward its initial value.

5.6 Summary

Fabrication and characterization of pentacene-based top contact organic thin film transistors (OTFTs) with PMMA and PVP as the dielectric layer have been investigated in this chapter. This study gave clear experimental evidence that the quality of pentacene film grown on the PMMA gives much improved transistor behaviour than that of a similar film grown on PVP. This indicates that PMMA is a very promising candidate for use as an insulating layer in pentacene-based organic electronic devices. Particularly, PMMA-based OTFTs exhibited good electrical properties and relatively high mobility values, of about 1.32 $cm^2\ V^{-1}\ s^{-1}$. All the devices exhibited typical p-type transistor behaviour. Holes accumulate at the pentacene surface when a large negative voltage is applied to the gate, and a high source-drain voltage results in saturation of I_{DS} as the conductive channel becomes pinched off. In each measurement, both forward and reverse scans were shown. Furthermore, transistors exhibit on/off current ratio between 10^3 and 10^6, with threshold voltage of about < -16 V and without leakage current.

One of the major achievements in this chapter is the fact that almost all OTFTs studied in this investigation produced hysteresis-free behaviour in the output and transfer characteristics. This indicates that all devices are traps and defects free that give this research an important characteristic. Without this behaviour it would be impossible to move to the fabrication of memory devices.

The effect of the environment on the device operation is also presented in this chapter. Devices were stored under vacuum at room temperature in between measurements, while some devices were in air during the measurements. Devices were retested after two months of fabrication, and some devices are retested after one year of fabrication. The results show more than 90% of the devices are operational with reasonable characteristics and good conditions. The electrical parameters of these devices showed a slow decrease in mobility after one year of fabrication. The fabrication of such

devices was repeated several times to ensure reproducibility as this is a critical point in this research when a control transistor is required in the fabrication of memory transistors (explained in the next chapter).

The second part of this chapter was to measure the endurance properties of OTFT devices. This process had three stages; applied constant gate bias at different stress time, applied different gate bias stress at constant stress time and applied constant gate bias at constant stress time with different drain bias stress. The bias stress effect has been observed in terms of threshold voltage shift ΔV_T and mobility. The ΔV_T have been measured for various conditions and times, and it has been found that ΔV_T obviously increases with the increase of the stress voltage. Also and significantly, negligible hysteresis is evident between the forward and reverse sweeps of the transfer characteristics and the shape of the transfer characteristics did not change with bias stress. The effects of stress voltage were found to be more effective in gate voltage stress rather than drain voltage stress. To clear stress voltage effects, gate electrode was connected to ground for few second.

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Chapter 6

Organic Thin Film Memory Transistors (OTFMTs)

6.1 Introduction

The fabrication and electrical behaviour of organic memory devices based on pentacene thin film transistor (TFT) structures using poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP) as gate dielectrics is studied . Four types of memory stacks were used during this investigation, three structures based on PMMA while PVP was used in the fourth structure. In the structures using PMMA, three different types of floating gates were used: a thin film of gold, a layer of self-assembled metallic gold nanoparticles (AuNPs), and five layers single-walled carbon nanotubes (SWCNT). While in the structure using PVP, a layer of self-assembled AuNPs was used as the floating gate. The experimental details and electrical characteristics of these devices are presented and discussed in this chapter. The detailed programming and erasing procedures are presented too.

6.2 PMMA-based OTFMTs, with thin layer of gold and AuNPs as floating gates

In this section, we study the properties of pentacene-based organic thin film memory transistors (OTFMTs) using PMMA as the insulator. The charge storage elements investigated in this Section are thermally evaporated thin film of gold and a layer of

self-assembled metallic gold nanoparticles (AuNPs). We have explained previously that this particular organic semiconductor/insulator (pentacene/PMMA) combination leads to good transistor devices with negligible hysteresis in the output and transfer characteristics (Chapter 5). The programming/erasing states at low voltages are reported, which represent a key issue for the fabrication of organic thin film memory transistors.

6.2.1 OTFMT fabrication

Devices depicted in Figure 6.1 were fabricated by thermally evaporating Al bottom gate electrode (50 *nm* thickness) through a shadow mask (Figure 3.10 B (a)) onto a clean glass substrate. A 300 *nm* thick insulating layer was formed by spin coating anisole solution of PMMA on top of the gate electrode and curing at 120 °C for 1 hour. Two organic devices were fabricated with different floating gates. The floating gate for "device A" was formed by evaporating a 10 *nm* thick gold layer, while a monolayer of self-assembled AuNPs was used as the floating gate for "device B". The preparation of the AuNP solution and the deposition method are described in Section 3.4.2.3(a). Before the deposition of pentacene, another thin film of PMMA was deposited onto the floating gate. Pentacene was thermally evaporated at a pressure of 7.5×10^{-7} *mbar* and at a rate of 0.03 $nm\ s^{-1}$ through a shadow mask (Figure 3.10 B (b)) to a thickness of 50 *nm*. Following the deposition of pentacene, source and drain contacts were defined by thermal evaporation of 50 *nm* of Au through a shadow mask (Figure 3.10 B (c)). All thermal evaporation processes were performed in glovebox (nitrogen purged). Control devices without the floating gate were also fabricated.

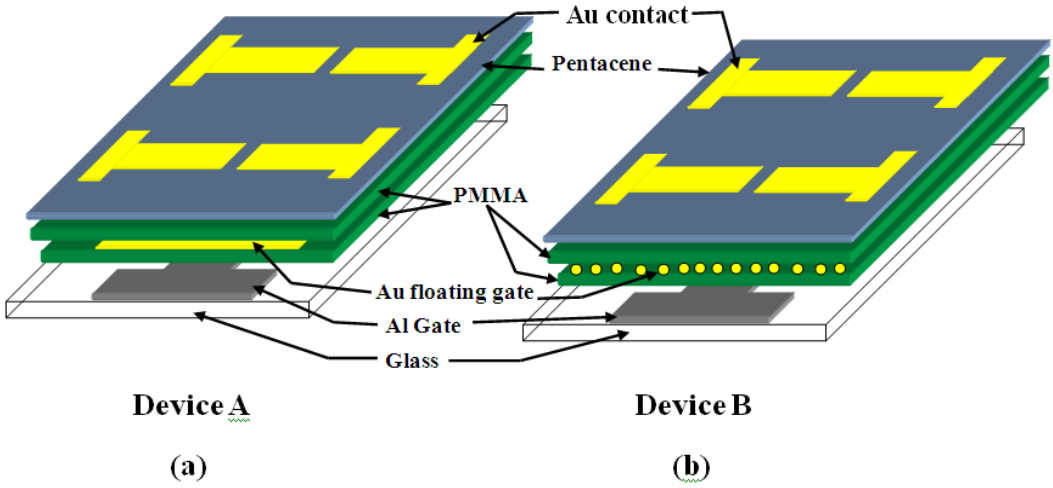

Figure 6.1*: Schematic diagrams of PMMA-based OTFMTs (a) with thin layer of gold (device A) and (b) gold nanoparticles (device B) as memory stack.*

Double sweep current–voltage *(I–V)* characteristics of the transistors were recorded at room temperature (21 ± 2 °C) using a Keithley 4140B picoammeter. More details of the measurement setup and device holders are discussed in Chapter 3.

6.2.2 OTFMTs characterisations

As shown in Figure 4.3 in chapter 4, the surface morphology of 50 *nm* pentacene film varied significantly as the thickness of PMMA, insulating layer, is changed.

The uniform adsorption of gold nanoparticles was confirmed using AFM images as shown in Figure 6.2. The average diameter of the synthesized AuNP was 56.01 ± 3.5 *nm*. The uniform adsorption of AuNPs in the whole area of the device on 300 *nm* of PMMA insulator layer was also observed. The thickness of the AuNPs film was estimated to be in the range of 20-30 nm, with few bundles of 40 nm thicknesses (shiny areas in Fig. 6.2).

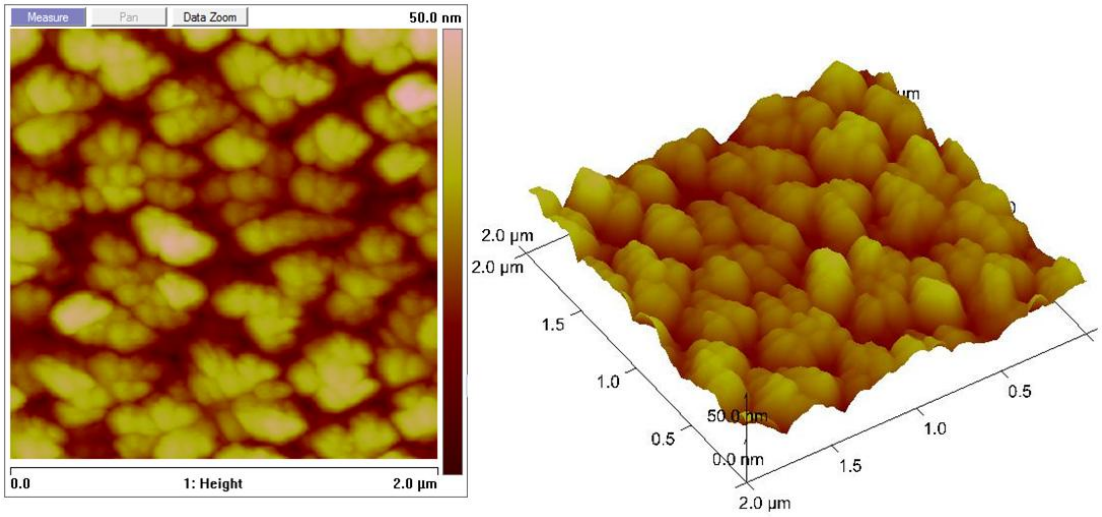

Figure 6.2: *AFM images of the self-assembled AuNPs deposited on 300 nm PMMA.*

Figure 6.3 (a) shows the output characteristics of the fabricated OTFT. The structure of the OTFT is Al/PMMA/pentacene/Au, which is used as the control device. The only difference compared to the memory devices is the absence of the thin gold or AuNP trapping layers in the gate dielectric layer. Otherwise, all of the device structures and the processing conditions are kept the same. Figure 6.3 (a) shows the typical output characteristics of p-type OTFT devices with respect to the gate voltage from 0 to -50 *V* with steps of 5 *V*. The transfer characteristic of the organic transistor is shown in Figure 6.3 (b) for V_{DS} = -50 *V*. The OTFT device exhibited almost no hysteresis in both characteristics. The calculated threshold voltage from the transfer characteristic is estimated to be -16 *V*.

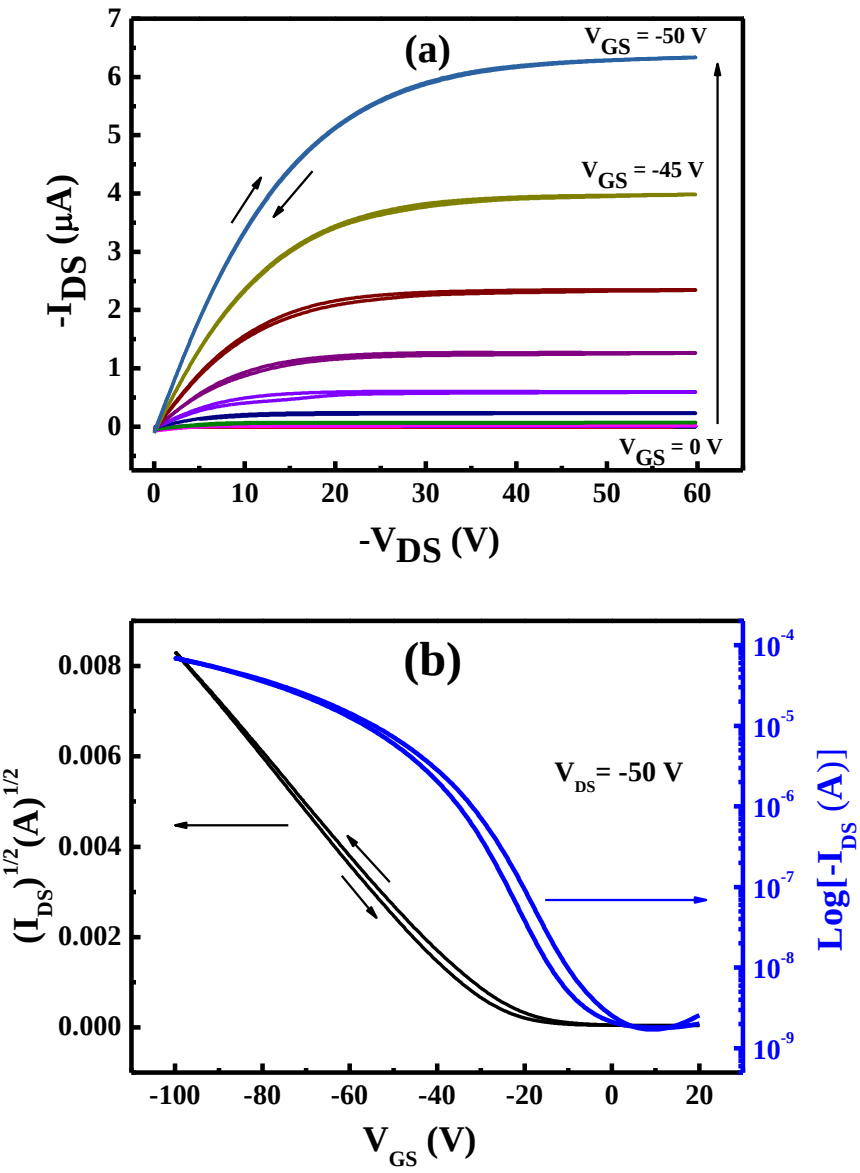

Figure 6.3: *(a) Output characteristics and (b) transfer characteristics of the OTFT fabricated as the control device.*

The transistor behaviour of the memory devices was investigated by measuring the output and transfer characteristics of the OTFMT at room temperature. Figures 6.4 and 6.5 show the characteristics of OTFMTs for devices A and B, respectively, as well as the OTFT control devices associated with each memory structure. Both forward and reverse scans are shown in each measurement, at a voltage scan rate of 1 $V\ s^{-1}$. The output characteristics of the memory and control devices exhibited good linear behaviour at low V_{DS} values as well as good saturation region at high V_{DS} (Figures

6.4(a) and 6.5(a)). The transfer characteristics of the memory device (initial curve) were also obtained before programming pulses (write/erase operation) were applied, as shown in Figures 6.4(b) and 6.5(b).

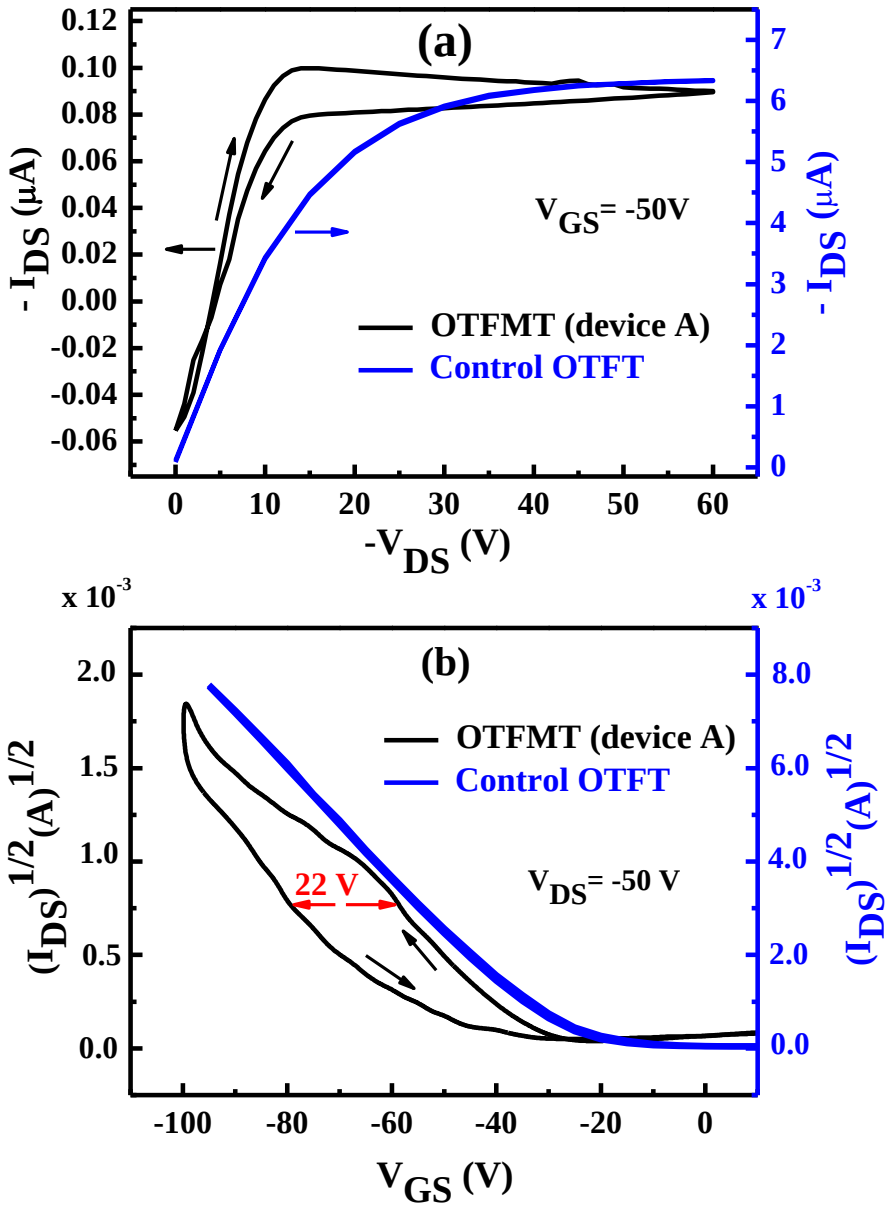

Figure 6.4: *(a) Output and (b) transfer characteristics of OTFMT of device A with and without the floating gate, thin layer of gold.*

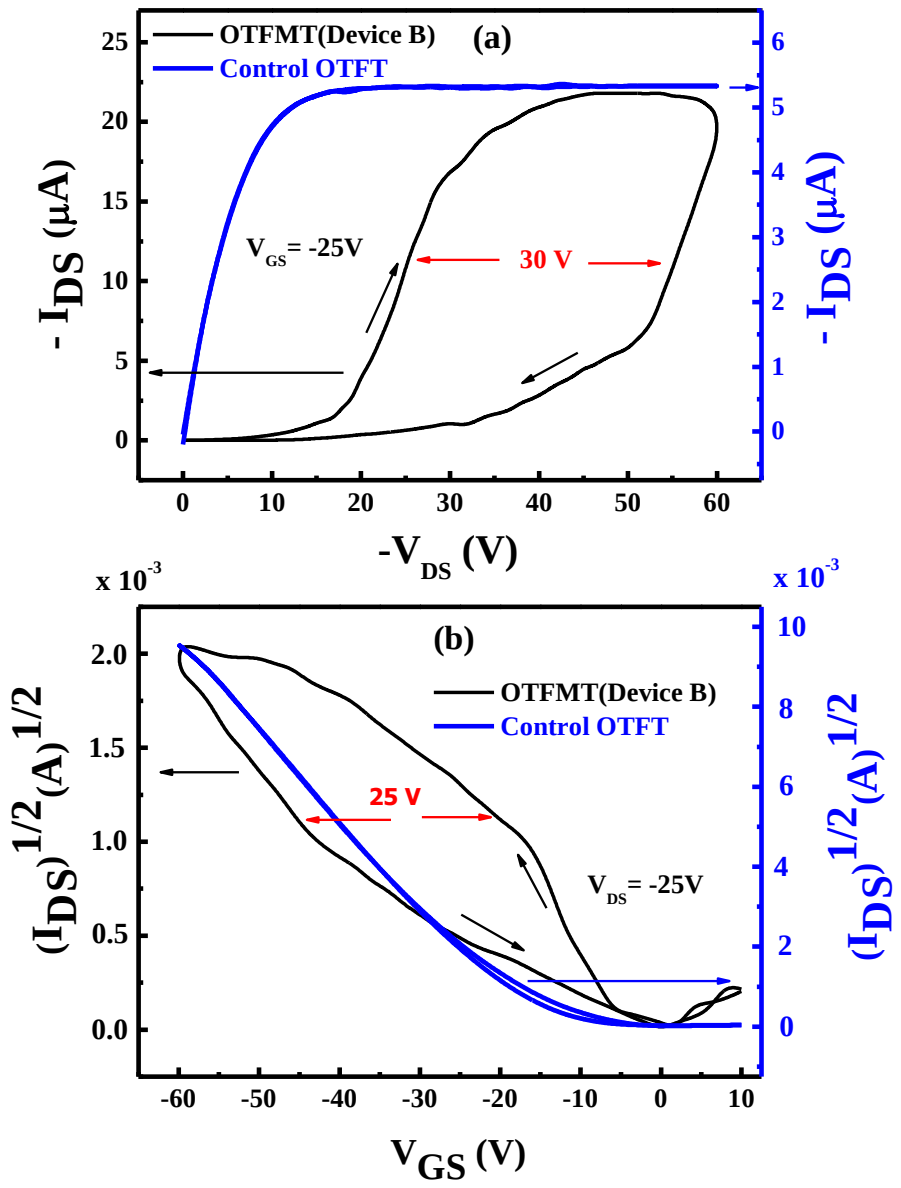

Figure 6.5: *(a) Output and (b) transfer characteristics of the OTFMT of device B with and without the floating gate, AuNPs.*

The V_{GS} values for the output characteristics were at -50 V for device A with channel length L = 140 μm and -25 V for device B with L = 195 μm, with channel width W = 1000 μm for both devices. For the transfer characteristics, the V_{DS} values were set at -50 V for device A and -25 V for device B. The field-effect mobility μ of the devices are calculated using equation (2.17).

Table 6.1 summarizes the electrical parameters for devices A and B, where the threshold voltages were measured for both forward and reverse directions (V_{TF} and V_{TR}, respectively). According to these results, the Au nanoparticle-based OTFMT structure (device B) produces an improved memory transistor performance than Au thin layer-based OTFMT structure (device A). It is also important to notice that device B operates at lower V_{DS} and V_{GS} (-25 *V*) values. On the other hand, it is very clear from Figures 6.4 and 6.5 that the addition of the Au floating gate produces a clear hysteresis in the transfer characteristics of the transistor; similar behaviour was observed for the output characteristics. It is almost certainly the result of charging and discharging with the applied voltages.

Table 6.1: *Electrical parameters of devices A and B.*

Structure	Mobility (cm^2/Vs)	Threshold voltage (*V*)		On/Off ratio	Memory window (*V*)	Charge capacity, *Q* (cm^{-2})
		V_{TF}	V_{TR}			
Device A	0.04	-20	-42	2.3×10^3	22	2.63×10^{12}
Device B	0.18	15	-10	0.3×10^3	25	1.19×10^{12}

It is important to note that there is almost no hysteresis in the control transistor as the forward and reverse scans produced superimposed characteristics. The counterclockwise direction of the hysteresis in the transfer characteristics indicates a clear hole charging, and the floating gate can become charged from the semiconductor surface. This is in agreement with our *C–V* characteristics of the MIS structures, as shown in Figure 4.12. When a high enough negative voltage is applied to the gate electrode, holes are injected from the semiconducting layer into the Au floating gate (through the top insulating layer), charging up the Au floating gate and programming the memory device. On the other hand, when a high enough positive voltage is applied to the gate electrode, holes are ejected from the floating gate through the pentacene layer (erase process).

In order to study the repeatability of the fabrication processes of OTFMTs, similar process repeated to produce memory transistors similar to the devices in Figures 6.4 and 6.5. Similar fabrication conditions used with the same thickness layers. Figure 6.6 show another examples of the output and the transfer characteristics for OTFMTs based on Au thin layer and AuNPs as the memory stacks. Similar hysteresis behaviours are clear for both devices due to charging and discharging of floating gates.

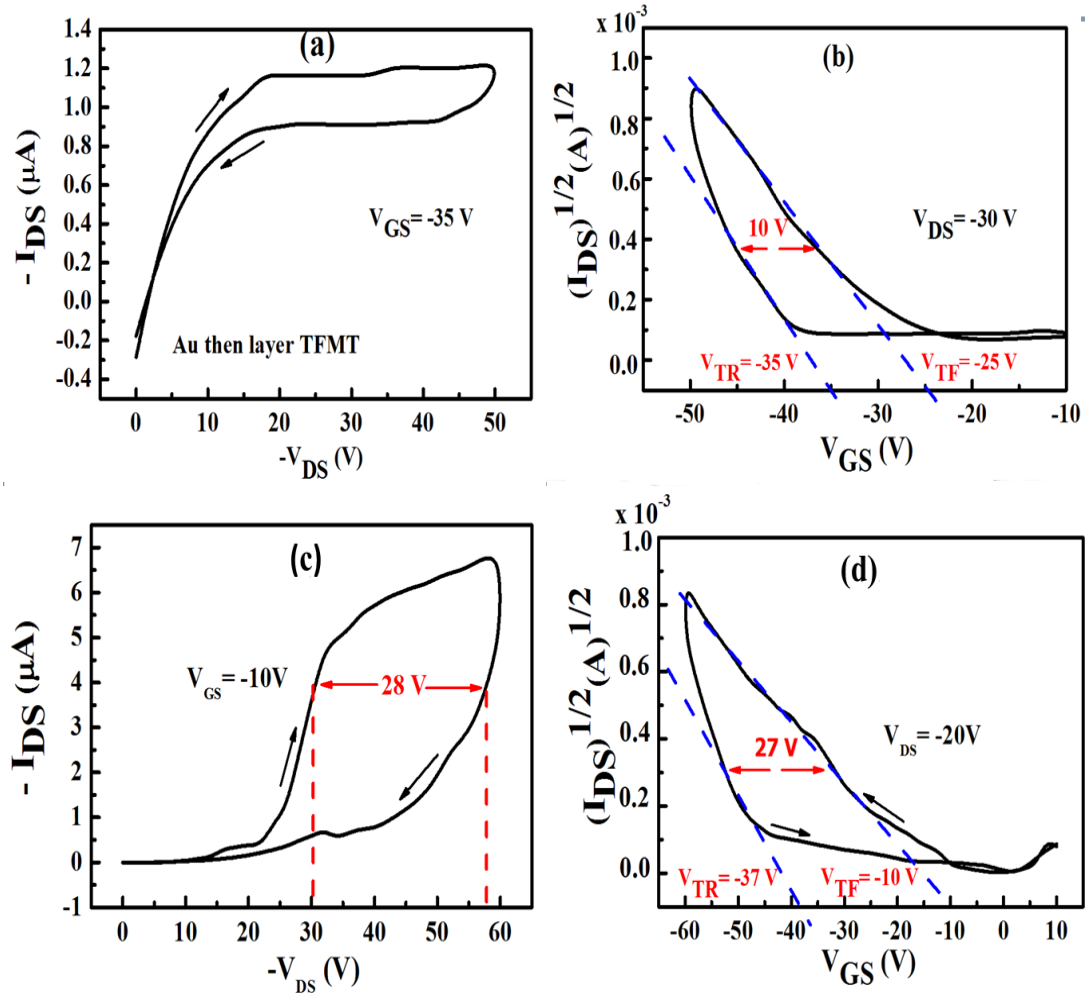

Figure 6.6: *Output and transfer characteristics for another OTFMTs based on (a) and (b) thin film of gold (Device A) and (c) and (d) AuNPs (Device B) as floating gates.*

To test the memory behaviour of the OTFMTs, successive positive and negative voltage pulses were applied on the gate electrode with V_{DS} maintained at 0 *V*. The magnitude of the voltage pulse was increased for each step, but the pulse duration was kept constant at 2 *s*. At each stage, and after the application of the voltage pulse, the transfer characteristics of the device were measured to calculate the shift in the threshold voltage compared to the unstressed device. Figure 6.7 shows the effect of negative and positive pulses applied to the gate electrode for Device A.

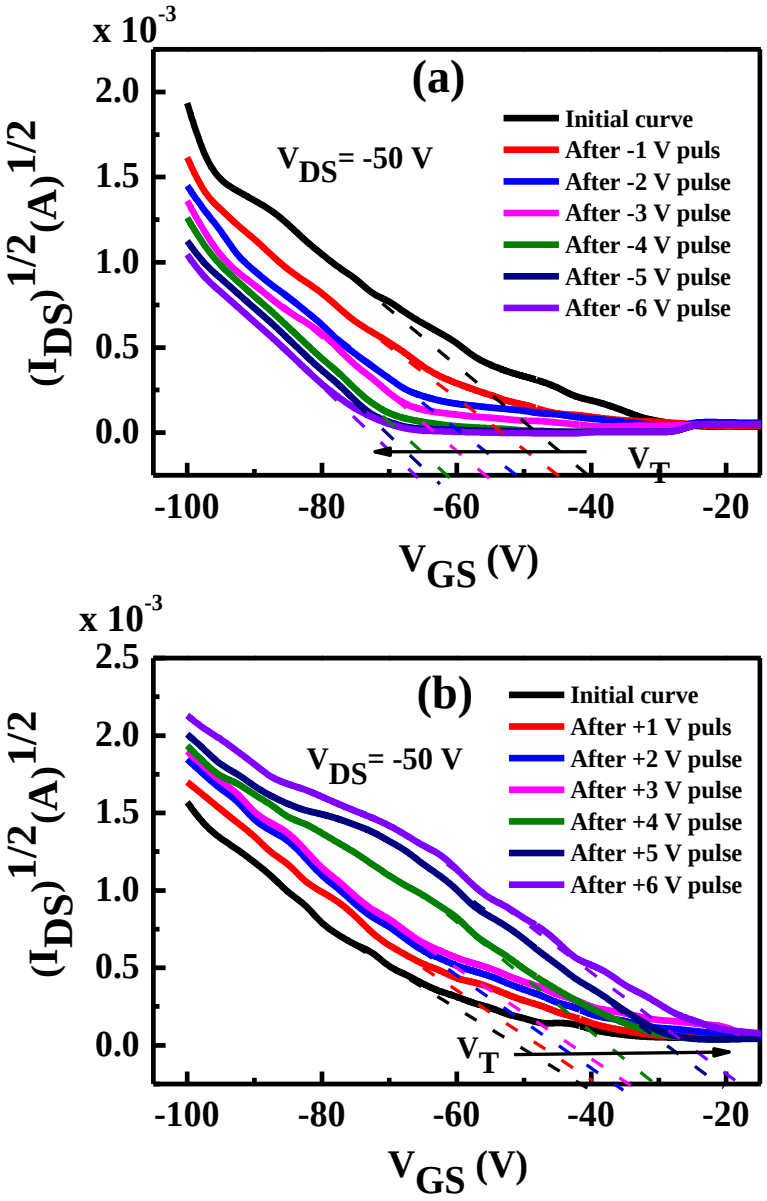

Figure 6.7: *The effect of (a) negative and (b) positive pulses on transfer characteristics of Device A.*

A clear shift to higher negative threshold voltages is observed for the application of negative pulses (write state) as shown in Figure 6.7(a), whereas, positive shifts of threshold voltages is observed due to the application of positive pulses (erase) as shown in Figure 6.7(b). These shifts are clearly presented in Figure 6.8 for pulses of -3 V and +3 V for write and erase states, respectively, of Device A. Similar behaviours are also observed for the programming of Device B as shown in Figures 6.9 and 6.10. Both devices shown repeatable and reproducible memory effects as measurements were conducted on several devices based on the same structures as devices A and B.

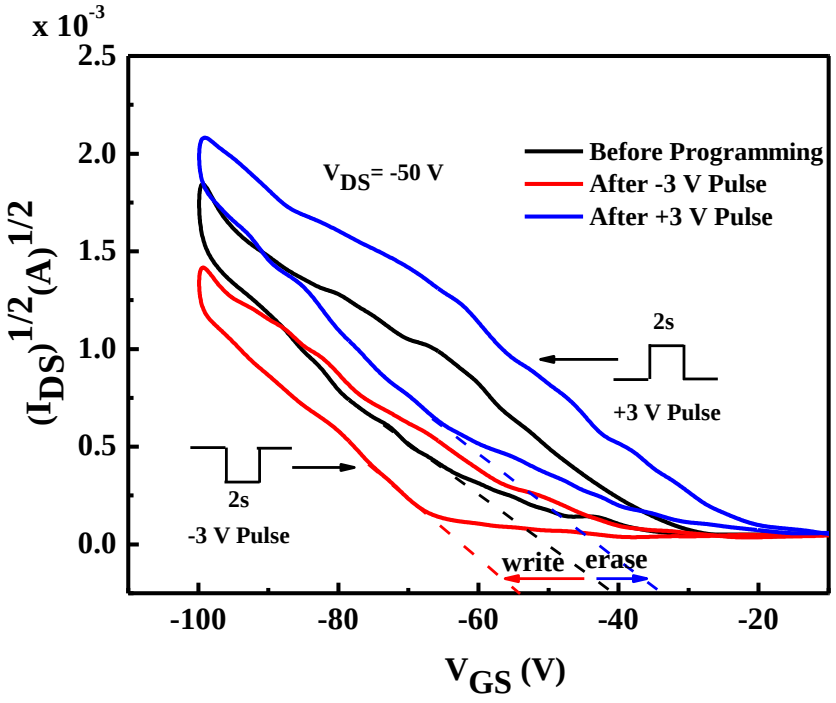

Figure 6.8: *Transfer characteristics of the OTFMT of Device A after the application of positive and negative pulses of 3 V for 2 s.*

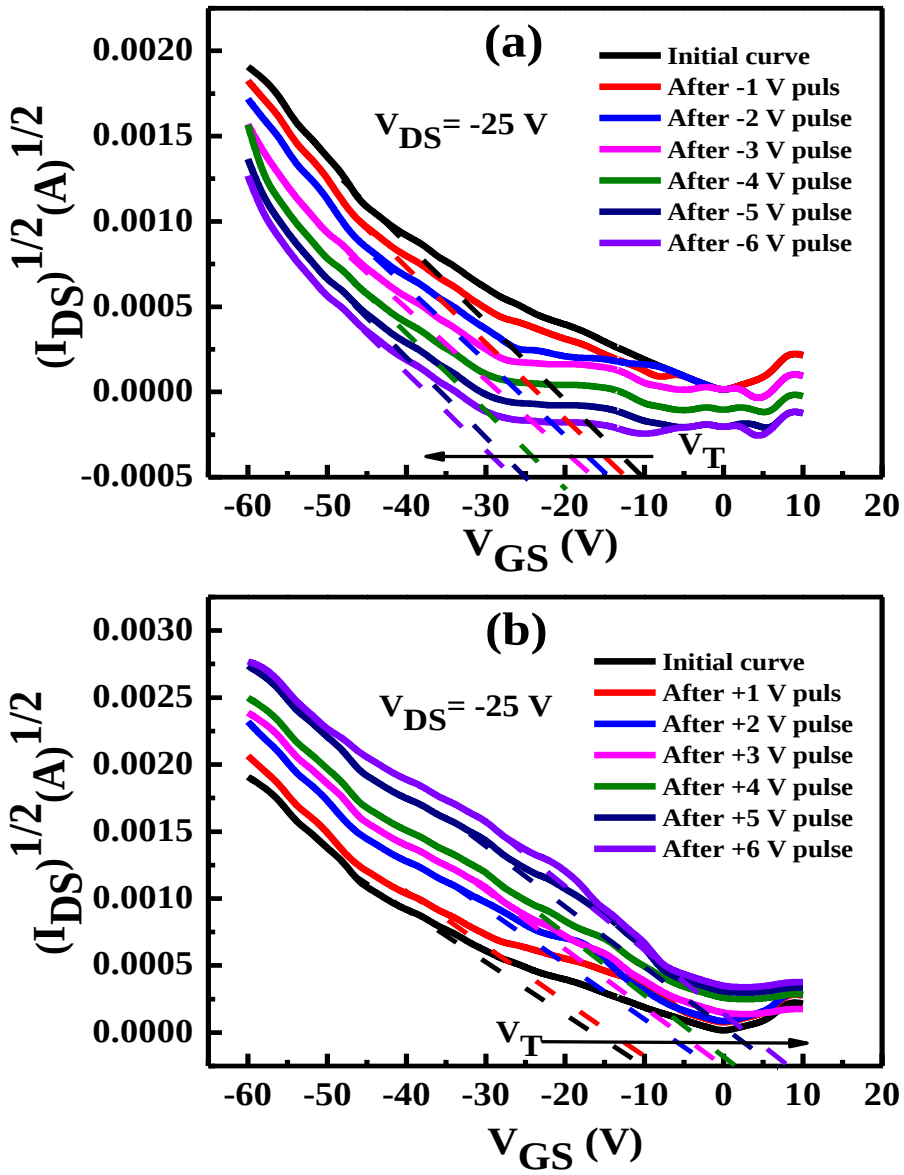

Figure 6.9: *The effect of (a) negative and (b) positive pulses on transfer characteristics of Device B.*

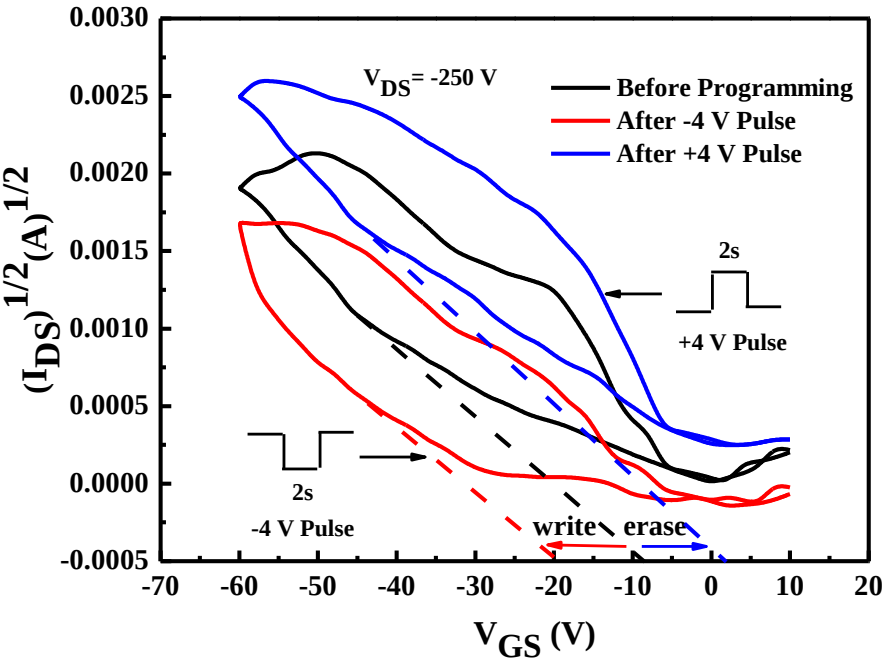

Figure 6.10: *Transfer characteristics of the OTFMT of Device B after the application of positive and negative pulses of 4 V for 2 s.*

Figure 6.11(a) shows the dependence of threshold voltage shift on the height of the applied voltage pulses for both Devices A and B. The devices in Figure 6.11(a) exhibit a clear memory window for voltage pulses over 1 *V*. Figure 6.11(b) shows the effect of programming pulses on the value I_{DS} when a voltage was applied to the gate electrode. The write state was achieve by a voltage pulse of -5 *V* for 2 *s* while for the erase state a voltage pulse of 5 *V* was used with the same period of time. When a gate voltage of 10 *V* was applied, it was possible to distinguish if the devices were in the write or erase states from the value of the drain-source current, evident from Figure 6.11(b).

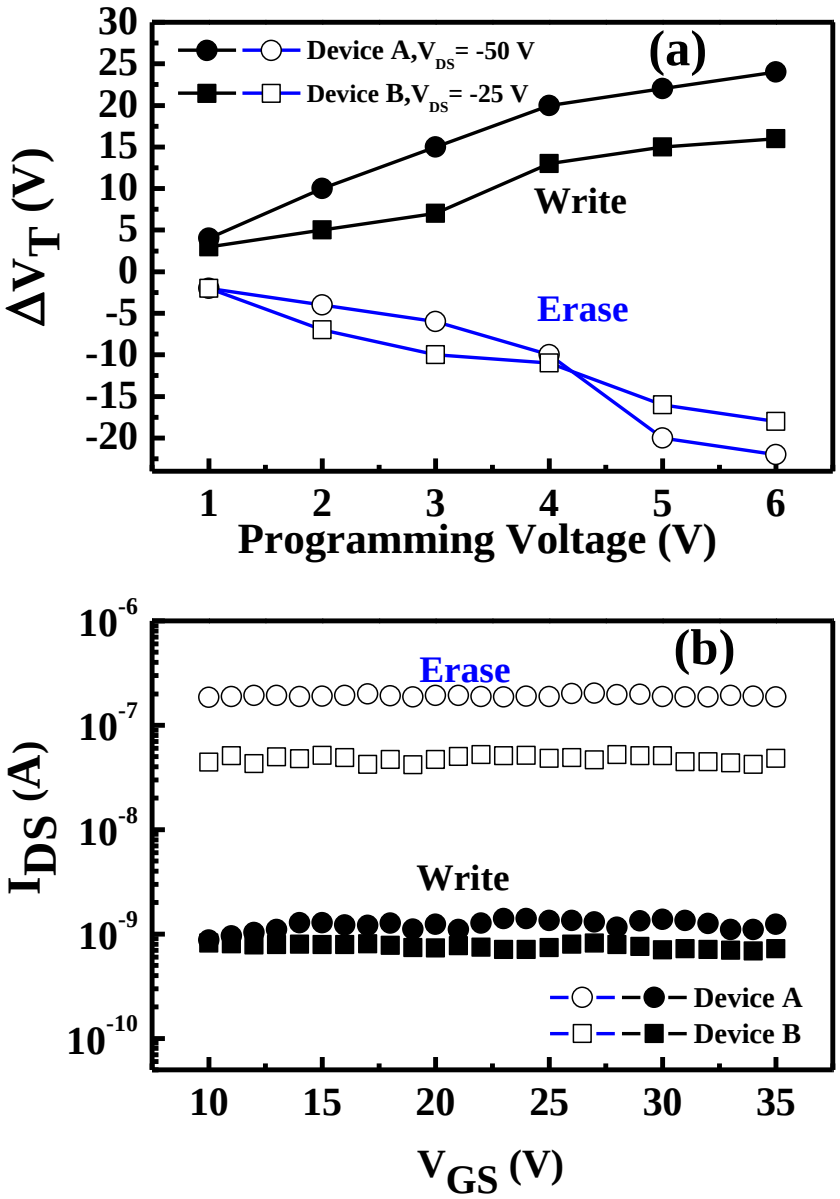

Figure 6.11*: Programming characteristics of OTFMT. (a) The effect of the programming voltage (2 s pulses) on the threshold voltage shift, ΔV_T. (b) Write and erase processes by applying a negative and positive pulse voltage, respectively.*

The nonvolatile behaviour of the OTFMTs was also investigated by monitoring I_{DS} after the application of voltage pulses for write and erase states. I_{DS} was periodically measured at regular time intervals with a fixed reading voltage of 10 *V*. Figure 6.12

shows the data retention capability as a function of time for devices A and B in the write/erase states under ambient condition at room temperature. In fact, the memory behaviour was retained for more than 12 months in the case of OTFMTs stored under vacuum.

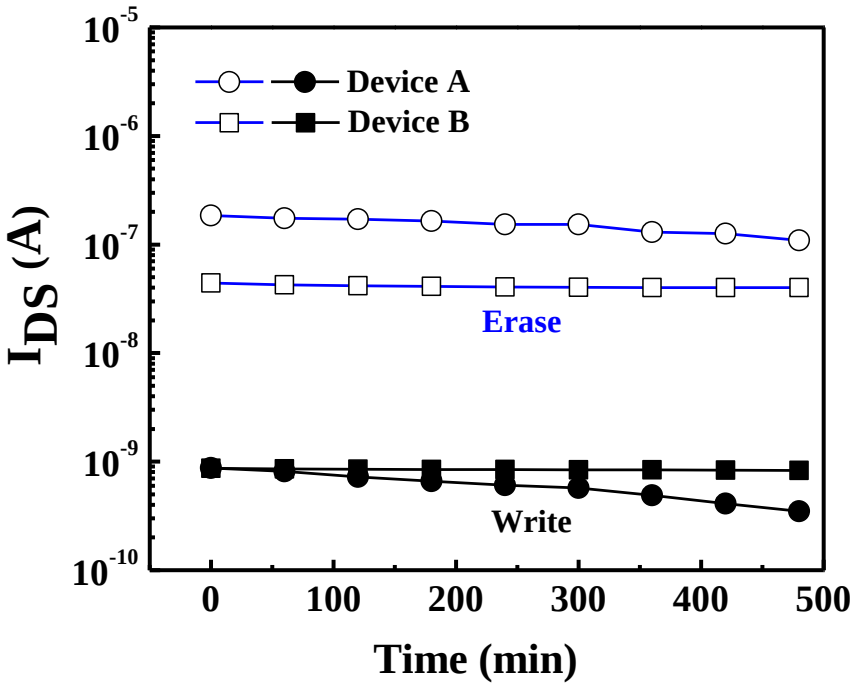

Figure 6.12*: Charge retention characteristics of the OTFMTs Devices A and B.*

When negative pulses (2 *s* pulses for devices A and B) are applied to the gate electrode (write state), it is believed that holes are transferred from the channel to the floating gate through the pentacene semiconductor. This charging process generates an internal electric field with a direction opposite to that of the applied negative voltage. As a result, a higher negative gate voltage is required to turn on the transistor, leading to a shift in the threshold voltage to a more negative value compared to the unstressed device. Correspondingly, when a positive pulse is applied to the gate electrode (erase state), holes stored in the floating gate are ejected into the transistor channel. A smaller negative gate voltage is then needed to turn on the transistor. This behaviour is evident

in Figure 6.11(a) as the shift in threshold voltage increases with increase in the applied voltage pulses. The characteristics in Figure 6.11(a) exhibit a clear memory window for voltage pulses as low as 1 *V* only.

The amount of charge stored in the floating gate Q can be estimated from $Q = C_i \Delta V_T$ [1–3] where C_i was measured using a simple pentacene/PMMA MIS structure. This gives a value of 7.8×10^{-9} and 3.7×10^{-9} F cm^{-2} for devices A and B, respectively; thus, the number of charge carriers stored is approximately 1.07×10^{12} and 0.7×10^{12} cm^{-2}, respectively, at a programming voltage of 6 *V*.

Figure 6.13 represent the relative energy diagrams for the materials used in the fabrication of the device depicted in Figure 6.1, where the work functions for Al and Au are 4.3 and 5.1 *eV* respectively. The highest-occupied molecular orbital (HOMO) and the lowest-unoccupied molecular orbital (LUMO) levels of pentacene are -5 and -3 *eV* respectively, while the energy band gap of PMMA is 5.7 *eV* [1]. The charging process shown in Figure 6.13 where under a negative bias applied to the gate electrode, holes emitted from the highest-occupied molecular orbital (HOMO) level are injected through the PMMA and captured by the Au floating gate. The presence of holes in the insulating stack of the transistor leads to higher negative voltage required to activate the transistor (higher negative threshold voltage). Based on the experimental results and the energy band diagram in Figure 6.13, we believed that transfer of holes from the pentacene to the Au floating gate occurs by tunnelling through the PMMA using possible localised defects present due to the presence of Au floating gate and by crossing the PMMA energy barrier as the HOMO level and the work function of PMMA and Au are very close (as shown in Figure 6.13). In turn, erasing occurs when a positive bias is applied to the gate electrode.

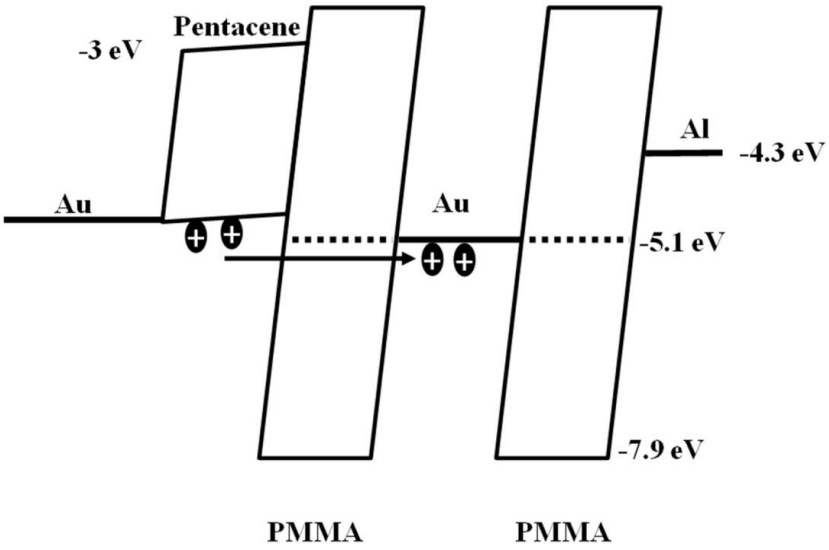

Figure 6.13: *Energy band diagram of the OTFMT in Figure 6.1.*

Some OFEMTs were also tested after one year of the fabrication as part of the stability measurements of memory devices. Figure 6.14 shows the transfer characteristics for a TFMT fabricated at the same time as the memory device in Figure 6.4 and measured after one year of the fabrication. It is clear that after one year of the fabrication, the OTFMT is operating with rather good performance with clear counterclockwise hysteresis in the transfer characteristics. This indicates that the present memory transistors have a long lifetime and could be used as the bases for commercial flash memory devices.

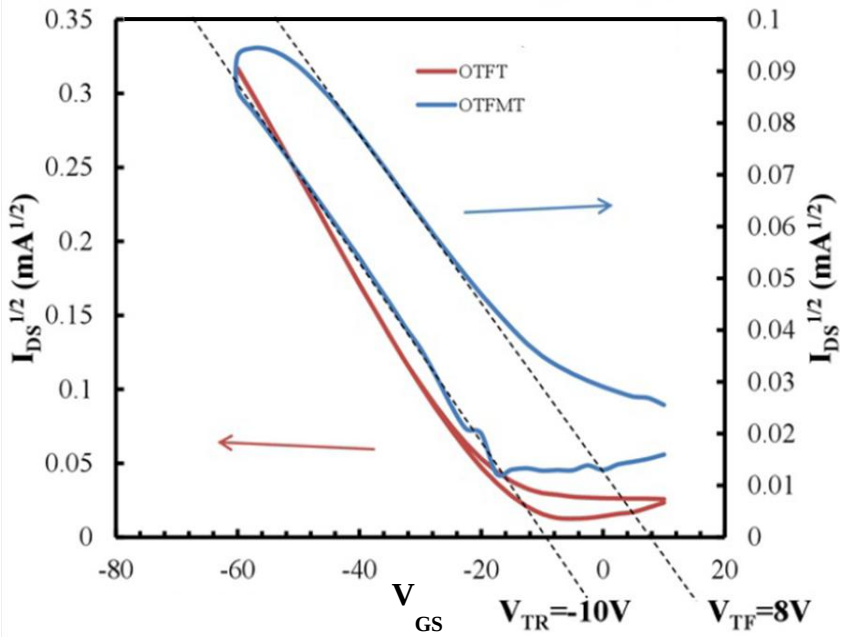

Figure 6.14*: Transfer characteristics of OTFMT measured after 12 months of the fabrication.*

6.3 PMMA-based OTFMTs, with SWCNTs as the floating gate

Single-walled carbon-nanotubes (SWCNTs) are one of the most promising candidates for creating the ubiquitous field-effect memory transistors for the next generation nanoelectronics due to their mechanical properties and excellent electrical properties [5-10]. In this section, we report on the performance of non-volatile memory effects of SWCNT-based field effect transistors structure. PMMA is used as the dielectric layer, and pentacene as the active layer in this device structure. Layer-by-Layer assembled composites were used for deposition of carbon nanotube as the charge storage layer instead of the Au thin layer and Au nanoparticles presented in the previous section (Section 6.2). The electrical characteristics of control devices of OTFTs structure are also investigated.

6.3.1 Fabrication process

The TFTs memory devices based on SWCNTs as nanofloating gate of structure Al/PMMA/SWCNTs/PMMA/pentacene/Au is similar to that of Figure 6.1 with SWCNTs used as the floating gate instead of the gold layer. The device was fabricated by thermally evaporating 50 *nm* thickness of an Al gate electrode through a shadow mask (Figure 3.10 B (a)) onto a clean glass substrate. A 300 *nm* thick insulating layer was formed by spin coating an anisole solution of PMMA on top of the gate electrode and cured it at 120 °C for 1 hour. The floating gate of SWCNTs was deposited using layer-by-layer (LbL) technique, which is a deposition technique based on charge reversal to build up bi-layer assemblies of oppositely charged molecules. The details of this technique were reported in Section 3.4.2.3(b). Prior to the deposition of the pentacene semiconducting layer, another thin film of PMMA was deposited onto the floating gate. Pentacene was thermally evaporated through a shadow mask (Figure 3.10 B (b)). Following deposition of the pentacene, the contact was defined by thermal evaporation of 50 *nm* of Au through a shadow mask (Figure 3.10 B (c)). The channel width was W = 1000 μm and the channel length was L = 147 μm. The control device without carbon-nanotubes CNTs was also fabricated. Double sweep current (*I*) versus voltage (*V*) characteristics of the transistors were recorded at room temperature (21 ± 2 °C).

6.3.2 OTFMTs characterisation

Figure 6.15(a) shows the output characteristic of SWCNTs-based OTFMT and the OTFT control device which is associated with memory structure. Both forward and reverse scans are shown in each measurement at a voltage scan rate of 2 $V\,s^{-1}$ with a V_{GS} value of -30 *V*. The output characteristics of the memory and control devices exhibited good linear behaviour at low V_{DS} values as well as good saturation region at high V_{DS}. Figure 6.15(b) shows the transfer characteristics of the memory transistor (initial curve) as well as the control transistor, the V_{DS} value was set at -25 *V*.

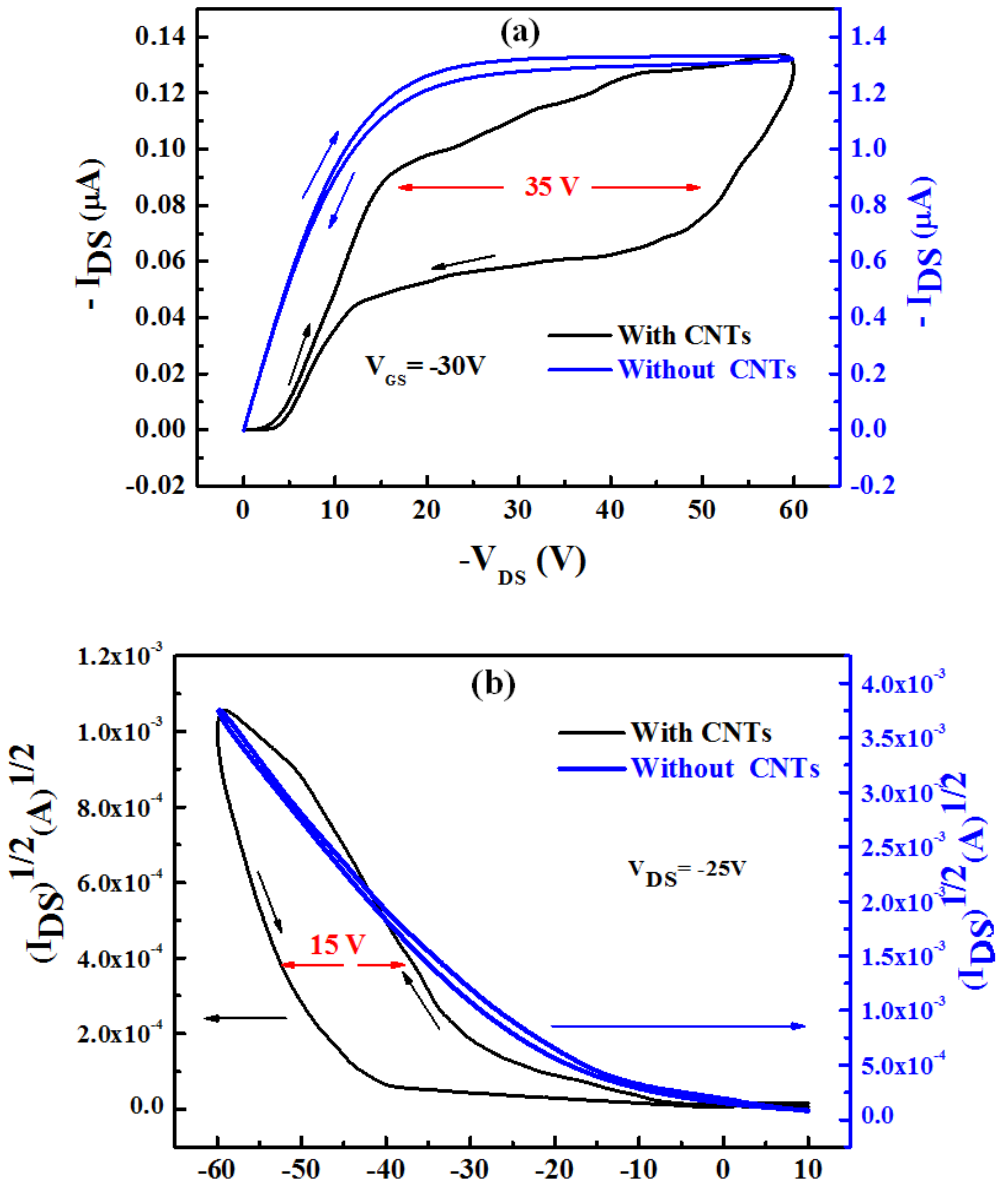

Figure 6.15: *(a) The output and (b) transfer characteristics of the OTFMT device with and without the SWCNTs floating gate.*

The effect of addition SWCNTs floating gate produces a clear hysteresis in both the output and transfer characteristics of the transistor, as shown in Figure 6.15. The hysteresis is the result of the charging and discharging of the SWCNTs floating gate with the appropriate applied voltages. Large memory windows were observed; a memory window of ΔV = 35 V was observed in the output characteristics and a memory window of ΔV = 15 V was observed in the transfer characteristics. Such large memory window for SWCNTs-based TFMTs is significantly dependent on dV_G/dt, which is the sweeping rate of the gate voltage due to the charge storage effect [11-17].

Clockwise hysteresis loop is observed for the output characteristic, whilst a counter-clockwise hysteresis loop is observed for the transfer characteristic when the gate voltage sweeps from positive to negative voltages. Such hysteresis loops are in good agreement with our recent studies for gold thin layer [18-20] and for gold nanoparticles [19], as described in previous section. These results are also consistent with Mabrook at el. [21, 22] results for gold nanoparticles-based TFMTs and with other research groups [11, 12, 23] for SWCNT-based TFMT devices. In addition, this is in agreement with our C–V characteristics of MIS structures with presence of SWCNTs as a floating gate, as shown in Figure 4.16.

Besides of the large memory window exhibited in SWCNTs-TFT memory devices, a relatively good field effect mobility; μ = 0.319 $cm^2\ V^{-1}s^{-1}$ has been observed. The threshold voltages were estimated of about -22 and -45 V for forward and reverse directions respectively. The on/off current ratio was 0.23 x 10^3. The amount of charges stored in the carbon nanotubes (Q) were estimated depending on C_i ($8.2 \times 10^{-9}\ F\ cm^{-2}$) and the ΔV_T (35 V). The number of charge carriers stored was calculated to be $1.7 \times 10^{12}\ cm^{-2}$. It is clear that although the hysteresis produced in the SWCNTs-based devices was larger than the hysteresis of devices with Au thin layer and AuNPs, all have the same amount of stored charges, which have similar values to our MIS structures memory devices.

The memory operation was again characterised by measuring the threshold voltage shift after charging the floating gate, as successive negative and positive voltage pulses were applied on the gate electrode with V_{DS} maintained at 0 V. The process of applied pulses was explained in a previous section. The magnitude of the voltage pulse was increased for each step but the pulse duration was kept at 1 s. The transfer

characteristic of the device was measured after each application of voltage pulse to calculate the shift in the threshold voltage compared to the unstressed device.

Figure 6.16 shows the effect of negative and positive pulses applied to the gate electrode of the SWCNT-based OTFMT. A clear shift to higher negative threshold voltages is observed for the application of negative pulses (write state) as shown in Figure 6.16(a), whereas, positive shifts of threshold voltages is observed due to the application of positive pulses (erase) as shown in Figure 6.16(b). These shifts are clearly presented in Figure 6.17 for pulses of -15 *V* and +15 *V* for write and erase states, respectively. This is similar behaviour as for the Au-based OTFMTs shown in Figures 6.7 and 6.9.

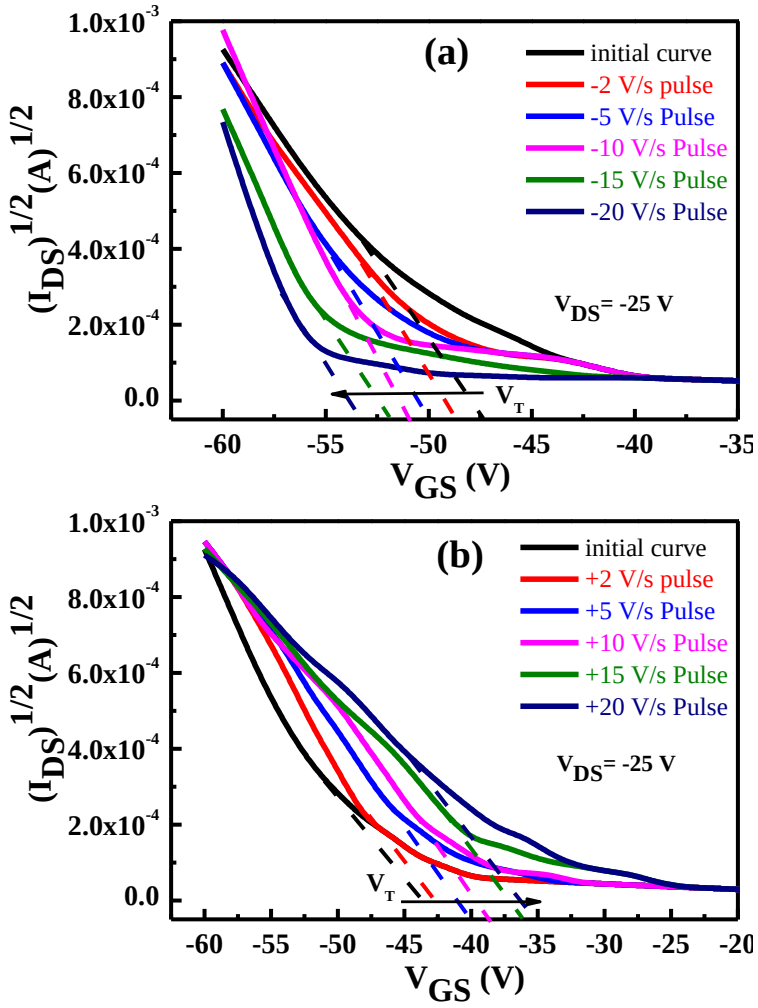

Figure 6.16: *The effect of (a) negative and (b) positive pulses on transfer characteristics for SWCNT-based OTFMT.*

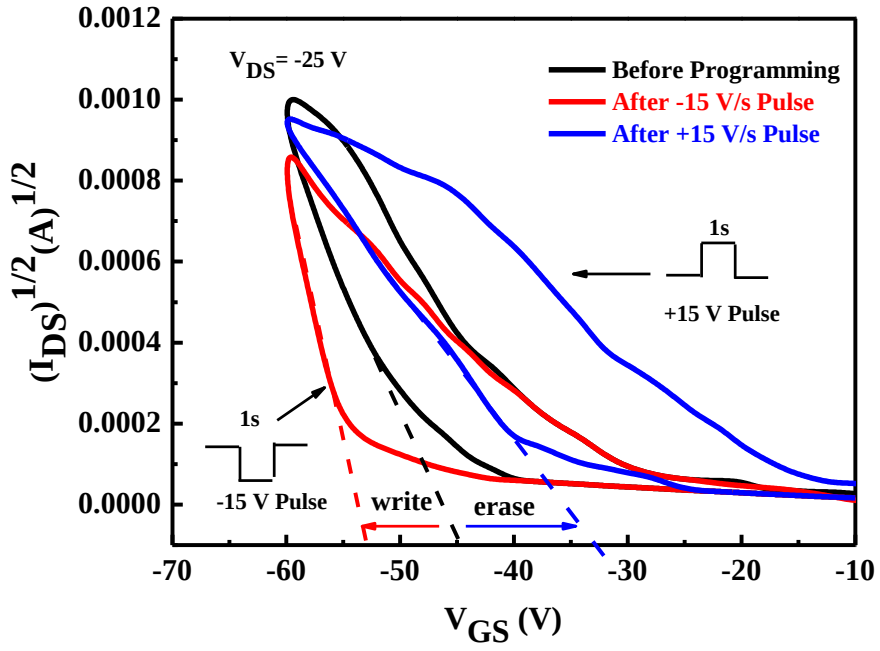

Figure 6.17: *Transfer characteristics of the SWCNT-based OTFMT after the application of positive and negative pulses of 15 V for 1 s.*

Figure 6.18(a) shows the programming pulses of SWCNT-based OTFTs, where the threshold voltage shifts as a result of the applied negative and positive pulses. As previously explained, the write state occurs when negative pulses (1 *s* pulses here) are applied to the gate electrode leading to the threshold voltage shift to more negative values compared to the unstressed device, while the application of a positive pulse to the gate electrode leads the transfer characteristic to shift rigidly toward positive gate voltages, erase state. These behaviours are evident in Figure 6.18(a) as the shift in threshold voltage increases with increase in the applied voltage pulses.

A clear memory behaviour in terms of writing and erasing for voltage pulses as low as 2 and 5 V, are shown in Figure 6.18(a). This is larger operating voltages as compared to that for our Au floating gate OTFMTs devices with voltage pulses of 1 V only. However, compared to results with results reported elsewhere of SWCNT-based OTFMTs [11, 13, 24, and 25], we find present results operate at much lower voltages.

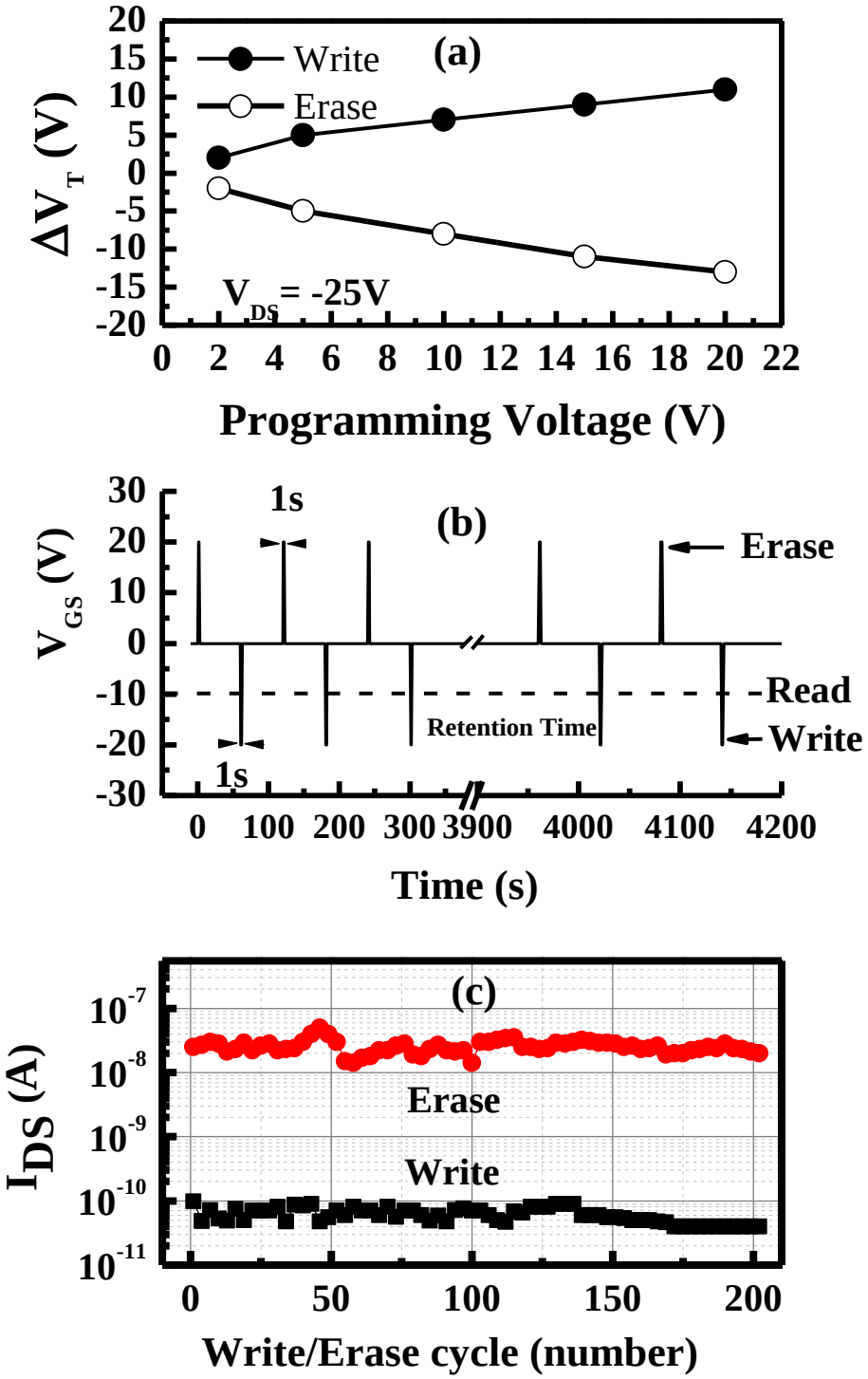

Figure 6.18: *(a) Programming characteristics, (b) pulses sequence and (c) retention current for the SWCNT-based OTFMT.*

For the purpose of measuring the endurance properties, the write/erase operations were repeated with continuous application of bias pulses of ±20 *V* for 1 *s*. After a certain number of write/erase cycles the reading process was carried out to establish if there is any change in the drain current. Figure 6.18(b) shows the test pulse sequence for endurance measurements of the SWCNT-based TFMTs at room temperature. As shown in Figure 6.18(b), there are three write/erase cycles in the first period with an initial delay of 60 *s* for each cycle, and then the drain current is measured by an applied reading bias of -10 *V*. After a retention time of one hour, the write/erase operations were repeated (two cycles, as shown in Figure 6.18(b)) and were followed with a reading process. This process was repeated for over 200 cycles and the I_{DS} value of the memory transistor was measured accordingly. It is observed that the current remains almost constant in both writing and erase states as shown in Figure 6.18(c). The average current recorded for the write and erase states are 7.12 x 10^{-11} *A* and 2.5 x 10^{-8} *A*, respectively.

6.4 PVP-based OTFMTs, with AuNPs as floating gates

The performance of nonvolatile organic field effect memory transistor using gold nanoparticles (AuNPs) as a floating gate is investigated in this section, where PVP is used as the dielectric layer, and pentacene used as the active layer. The electrical characteristics of control devices of OTFTs structure are also investigated.

6.4.1 OTFMTs fabrication

The schematic diagram of Al/PVP/AuNPs/PVP/pentacene/Au device structure for the bottom gate and top contacts organic transistor based non-volatile memory device is shown in Figure 4.18, chapter 4. This device was fabricated by thermally evaporating 70 nm thickness of an Al gate electrode through a shadow mask (Figure 3.10 C (a)) onto a clean glass substrate. 25 % (wt) of PVP solution in isopropanol (IPA) was spin coated on the gate electrode to a thickness of about 250 nm at 3000 rpm. The spun PVP layer was then baked at 80 °C for 10 min to form the thin film insulator. The

floating gate, AuNPS, was deposited using the self-assembly methods described in Section 3.4.2.3. Prior to deposition of a pentacene semiconducting layer, another thin film of PVP was deposited onto the floating gate. Pentacene was thermally evaporated through a shadow mask (Figure 3.10 C (b)) to a thickness of ~ 50 nm. Following the deposition of pentacene, source and drain contacts were defined by thermal evaporation of ~ 50 nm of Au through a shadow mask (Figure 3.10 C (c)). The channel width was W = 2670 μm and the channel length was L = 198 μm. The control device without AuNPs floating gate was also fabricated. Double sweep current (I) versus voltage (V) characteristics of the transistors were recorded at room temperature (21±2 °C).

6.4.2 OTFM Characterisation

Figure 6.19 shows the characteristics of OTFMTs for devices using AuNPs as the trapping layer in PVP gate dielectric layer, and the characteristics of the OTFT control device associated with the memory structure (blue colour in Fig. 6.19). Both forward and reverse scans are shown in each measurement, at voltage scan rate of 1 $V\ s^{-1}$. Figure 6.19(a) shows the output characteristics of the memory and control devices which exhibited good linear behaviour at low V_{DS} values as well as good saturation region at high V_{DS} with a gate voltage of -40 V. The transfer characteristic for the memory (initial curve, before programming pulses were applied) and control devices is shown in the Figure 6.19(b) with V_{DS} = -10 V. The OTFT devices exhibited almost no hysteresis in both characteristics, while a large memory window is evident on reversing the voltage scan direction of OTFMT. The output characteristic shows hysteresis window of ΔV = 23 V, similar behaviour was observed for the transfer characteristics (ΔV = 27 V).

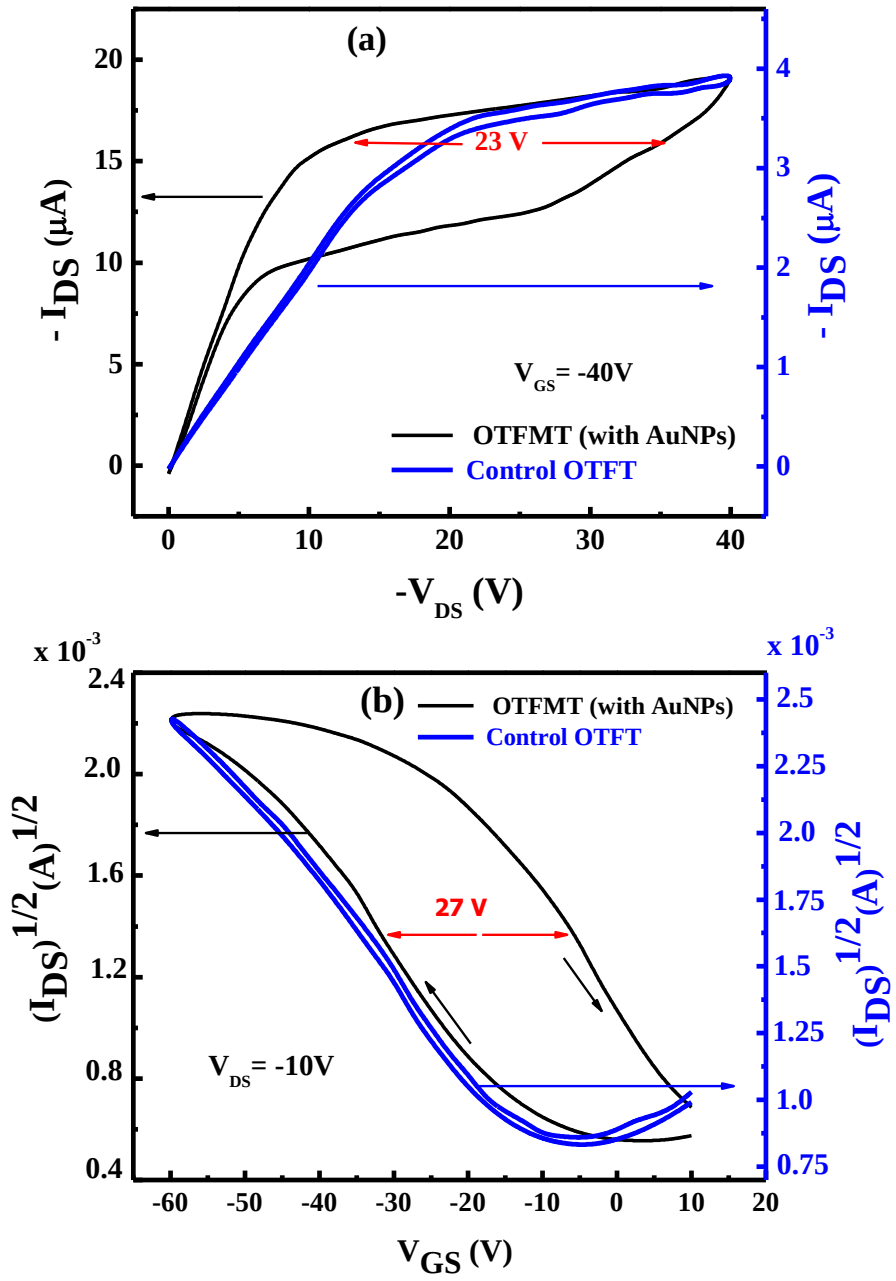

Figure 6.19: *(a) The output and (b) transfer characteristics of the PVP-based OTFT (control device) and OTFMT device.*

The field-effect mobility, μ, of the memory device is calculated to be in the region of 0.048 $cm^2\ V^{-1}\ s^{-1}$. This value is one order of magnitude lower than the OTFMT device fabricated on cross-linked PVP with the same configuration [1]. A lower mobility value is recorded for OTFMTs than that in OTFT devices (μ = 0.65 $cm^2\ V^{-1}\ s^{-1}$, as

shown in Section 5.4.2 in Chapter 5); this clearly indicates that gold floating gate has influenced the current flow in the transistor channel resulting in lower mobility due to the trapped charge carriers in the floating gate [18]. However, comparing the performance of this AuNPs-based OTFMT with the device using PMMA (as in Section 6.2), it can be found that all the electrical parameters produced by PMMA-based OTFMTs were significantly enhanced than that of a similar PVP-based OTFMTs at smaller applied values of V_{DS}.

The amount of charge stored in the gold nanoparticles Q is approximately 1.2×10^{12} cm^{-2} as the value of $C_i = 8.5 \times 10^{-9}$ F cm^{-2} and ΔV_T =23 V. It is clear that the charge stored in the AuNPs floating gate is relatively higher when PVP is used rather than PMMA. However, this magnitude of charge storage has similar values to those stored in our MIS memory structures (in Chapter 4, Section 4.3.4.2).

The charging effect by the application of negative and positive bias pulses to the gate are investigated and shown in Figure 6.20. The operation of applied bias pulses was the same as used for carbon nanotubes SWCNTs memory devices. The memory operation was characterized by measuring the threshold voltage shift after positive and negative voltage pulses were applied to the gate electrode. The magnitude of the voltage pulses were increased for each step but the pulse duration was kept at 1 *s* with V_{DS} maintained at 0 *V*. A clear shift to higher negative threshold voltages is observed for the application of negative pulses (write state) as shown in Figure 6.20(a), whereas, positive shifts of threshold voltages is observed due to the application of positive pulses (erase) as shown in Figure 6.20(b).

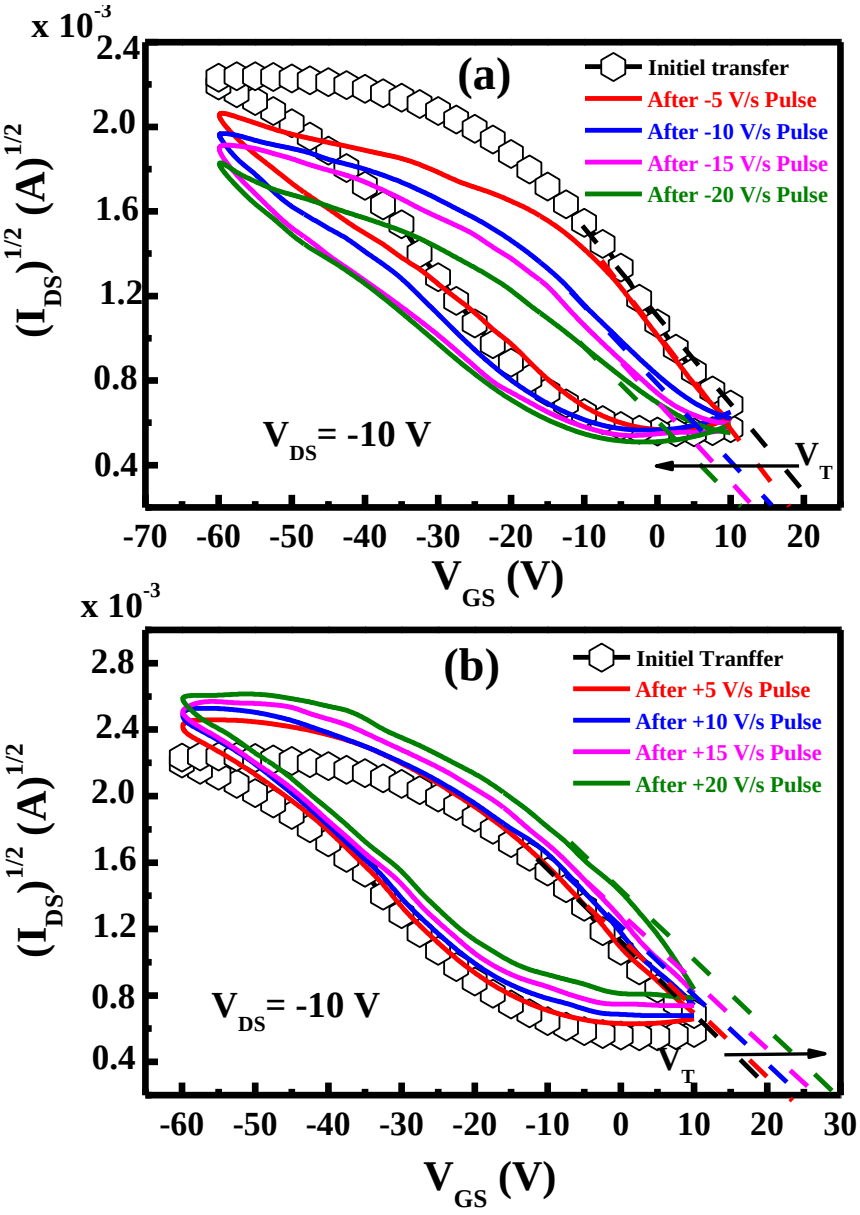

Figure 6.20: *The effect of (a) negative and (b) positive pulses on transfer characteristics for PVP-based OTFMT.*

The transfer characteristics of the devices were measured after each application of the voltage pulse to calculate the shift in the threshold voltage compared to the unstressed devices. Figure 6.21(a) shows the programming pulses (write/erase), where the threshold voltage shifts as the result of the applied negative and positive pulses.

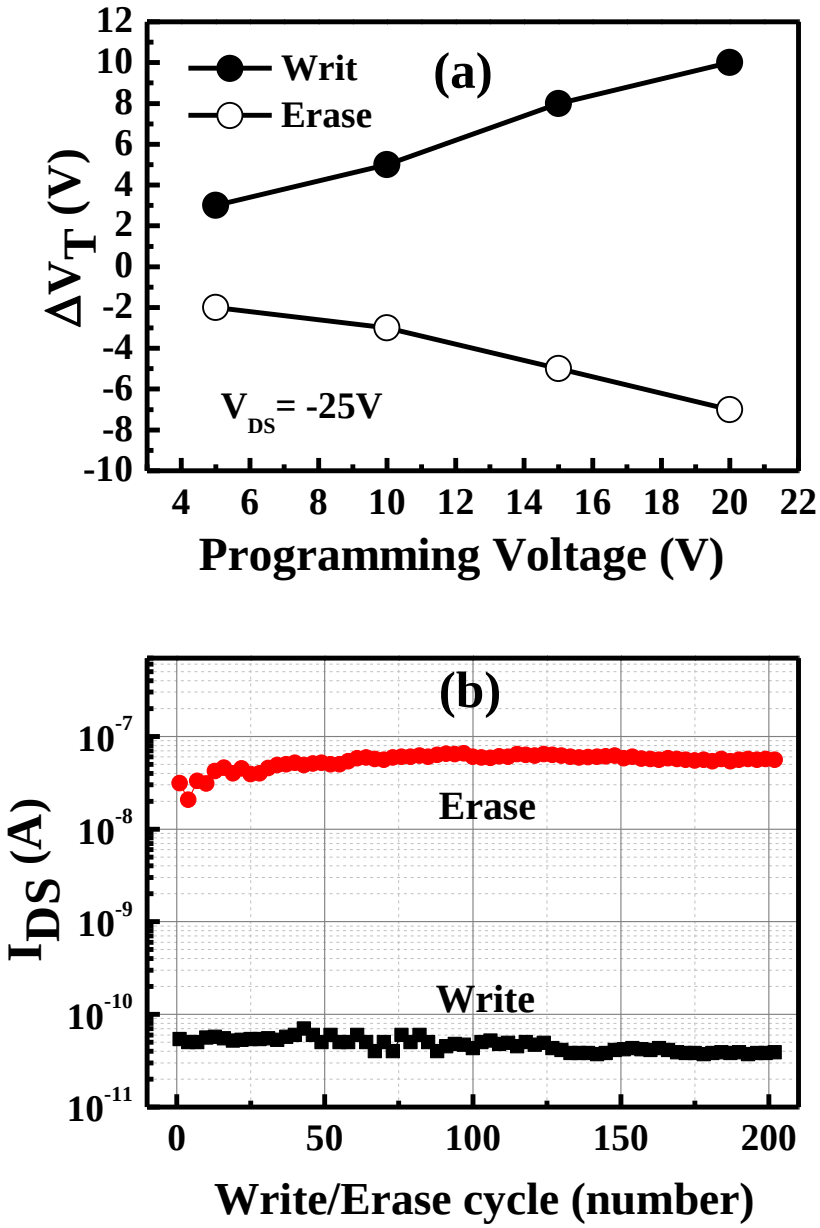

Figure 6.21: *(a) Programming characteristics and (b) retention current for the PVP-based OTFMT.*

There was V_T shift of around 3 *V* after the application of 5 *V* bias pulses for 1 *s* as shown in Figure 6.21(a). Therefore, clear charging and discharging of the charge carriers occurred in the bulk and/or interfaces of the PVP gate dielectric layer. The

shift in threshold voltage increases with the increase in the applied voltage pulses. Clear memory window behaviour was shown for voltage pulses of 5 *V*, as shown in Figure 6.21(a). Such operating voltages are similar to those of other OTFMTs devices investigated in this study. However, when compared with other researches in the same configurations [1, 26], and with researches of OFET memory devices built on silicon wafers [27] we found our devices exhibit a much lower operating voltages. The write/erase processes were defined as the states associated with the holes being trapped or detrapped after the application of the negative or positive gate biases [1], in a similar way as previous devices.

In a similar sequence as the SWCNT-based OTFMT, the endurance of the devices was studied. More than 200 cycles were used during this measurements and the I_{DS} was measured for write and erase states. Figure 6.21(b) shows the values of the I_{DS} as a function of cycles. It is clear that the current did not change dramatically after more than 200 cycles and it is easy to distinguish if the device in write or erase state. The average current recorded for the write and erase states are 5.5×10^{-11} *A* and 5×10^{-8} *A*, respectively.

6.5 Summary

The fabrication of four types of organic memory devices based on transistor structures has been demonstrated in this chapter. Three of these devices were based on PMMA as the insulator with different floating gate materials; a thin film of Au layer, Au nanoparticles, and single-walled carbon-nanotubes. The fourth type of OTFMTs was based on PVP as the insulator with Au nanoparticles as a floating gate.

The electrical properties of the organic TFMTs could be improved by the use of the Au nanoparticles layer as the floating gate compared with that of an Au thin film. Using appropriate negative or positive voltages, the floating gate may be charged and discharged, resulting in a clear shift in the threshold voltage of the transistors. The charge trapping effect is attributed to the presence of the floating gate, as carriers are injected from the pentacene surface through the top insulating layer. Negative and positive pulses of 1 *V* resulted in clear write and erase states in both devices. The

results augur well for the development of organic electronic circuits working at low operating voltages.

For OTFMTs devices using carbon nanotubes as a floating gate, large memory windows ($\Delta V > 35\ V$) as well as high carrier mobility ($\mu = 0.319\ cm^2\ V^{-1}\ s^{-1}$) are demonstrated. The floating gate may be charged and discharged resulting in a clear shift in the threshold voltage of the transistors after using appropriate negative or positive voltages pulses. Data retention properties for carbon memory devices were expected from the extrapolation of the measured data retention characteristics, and the hysteresis may be used as the basis of a stable memory at room temperature.

In the fourth type of OTFMTs using AuNPs floating gate and PVP as the insulating layer; a clear hysteresis is observed in the electrical characteristics, and shifts in the threshold voltage of the transfer characteristics. Pulses of 5 *V* resulted in clear write and erase states. A large memory window and good retention time are seen in this device.

The summary of the results for the four types of OTFMTs devices which were investigated in this study are shown in Table 6.2 below;

Table 6.2: *The electrical parameters of the OTFMTs devices.*

Structure	Charging pulse (*V*)	Mobility (cm^2/Vs)	Threshold voltage (*V*)		On/Off ratio	Memory window (*V*)	Charge capacity, *Q* (cm^{-2})
			V_{TF}	V_{TR}			
Au thin layer/PMMA	1	0.04	-20	-42	2.3×10^3	22	1.07×10^{12}
AuNPs/PMMA	1	0.18	15	-10	0.3×10^3	30	0.7×10^{12}
SWCNTs/PMMA	2 and 5	0.319	-22	-45	0.2×10^3	35	1.7×10^{12}
AuNPs/PVP	5	0.048	-5	22	0.27×10^3	23	1.2×10^{12}

As shown in the table 6.2, the electrical properties of the organic TFMTs using SWCNTs as the floating gate and PMMA as the insulator shows much improved parameters compared with that of Au floating gate based OTFMTs devices. Additionally, these organic memory devices exhibited good programmable memory characteristics with respect to the write/erase operations, leading to a large threshold voltage shifts. The data retention and endurance measurements confirmed that the pentacene based OTFMTs devices exhibited mechanical stability as well as good electrical reliability. Furthermore these data retention and endurance measurements confirmed the non-volatile memory properties for our devices in this study. Therefore, these methods could potentially be integrated with pentacene based OTFMTs electronic components/circuits.

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Chapter 7

Conclusions and Further Work

7.1 Conclusions

Pentacene-based nonvolatile organic thin film memory transistors (OTFMTs) operating at low programming voltages with long retention time were demonstrated in this study. In line to achieve this target, low-cost, high performance and hysteresis-free organic thin film transistors (OTFTs) were produced. In order to accomplish the OTFTs, metal-insulator-semiconductor (MIS) structures were fabricated and characterised using two different organic insulators, poly(methyl methacrylate) (PMMA) and poly(vinyl phenol) (PVP). These devices were characterised at room temperature under normal laboratory environments. All the MIS capacitors exhibited negligible hysteresis in the *C-V* characteristics with flat–band voltages of about -2 to -3 *V*. The small shift in threshold voltage away from the ideal 0 *V* originated from charge trap sites probably present in the interfaces between the insulator and the active layer.

Optimisation of fabrication procedure. Initial structural properties of evaporated pentacene showed poor surface morphology, poor grains connections, and smaller grains when high evaporation rate was used; resulting in poor conductivity. In contrast, optimum morphology surface, with large crystalline and connected grains was achieved using 0.03 $nm\ s^{-1}$ evaporation rate on 300 *nm* PMMA films. Large grains concurrent with a decrease in the density of grain boundaries reducing the density of traps and improving pentacene charge mobility. To further optimise the fabrication

process, uniform, crack-free and pinhole-free Au contacts were achieved when the gold layers were deposited seven days after the deposition of pentacene. On the contrary, surface defects were observed when Au electrodes were deposited directly after the evaporation of pentacene. The impact of the surface morphology of pentacene and Au electrodes was clearly reflected on the electrical characteristics of OFETs. All OTFTs exhibited classic p-type semiconductor behaviour in both output and transfer characteristics. This study gave clear experimental evidence that the quality of pentacene grown on PMMA was much enhanced compared to that of a similar film grown on PVP. It was also showed that PMMA-based OTFTs stored under vacuum between measurements have average values of mobility μ = 1.09 $cm^2\ V^{-1}\ s^{-1}$ (with a maximum mobility of ~ 1.32 $cm^2\ V^{-1}\ s^{-1}$), on/off current ratio ~ 2.75 × 10^5 and the threshold voltage V_T ~ -14 V. This in fact provides more evidence in support of using PMMA as the insulator in organic electronic devices.

Environment and endurance effects. The effect of the environment on devices properties was observed during this work. Devices are retested after two months of fabrication, and some devices are retested after one year of fabrication. Most of the devices were working with reasonable characteristics, good conditions and long stability. Furthermore, PMMA-based devices showed reasonable mobility with high on/off current ratio between 10^3 and 10^6.

Endurance properties of the fabricated OTFTs was demonstrated using constant gate bias at different stress time, different gate bias stress at constant stress time and applied constant gate bias at constant stress time with different drain bias stress. After the application of the stress voltages, negligible hysteresis was evident between the forward and reverse direction of the transfer characteristics and the shape of the transfer characteristics did not change with the bias stress. In fact this was an important parameter to monitor to make sure the control OTFTs are free of trap states and not affected by the application of voltages in the accumulation region. This behaviour makes the fabricated OTFTs suitable for high-performance memory device applications.

OMIS-based memory structures. Flash memory devices based on MIS structures using thin film of Au layer, Au nanoparticles and single walled carbon nanotubes as the floating gate were clearly demonstrated. Negligible hysteresis was exhibited for control devices (without floating gate), while memory devices exhibited clear hysteresis; this was indicative of the memory effect and charge storage in MIS structures. Also the hysteresis was centred close to 0 *V* for devices based on SWCNTs, giving the possibility to charge and discharge the memory devices at low voltages. A memory window of about 40 *V* was achieved at a ± 40 *V* sweep range for the AuNPs floating gate memory devices based on PVP. Also with the same voltage sweep, the memory windows for devices based on PMMA with thin layer of Au and AuNP floating gates were 22 *V* and 32 *V*, respectively. The average concentration of charge carriers stored in these memory devices was estimated to be in the range $10^{12}\ cm^{-2}$. For AuNPs and SWCNTs-based devices, the clockwise direction of the hysteresis, with a shift of the flatband voltage to a less negative voltage, indicates that electrons originating from the Al gate become trapped on the floating gate. This indicates that, in accumulation, electrons are injected from the Al electrode to the floating gate, which later becomes negatively charged. A reduces negative voltage were applied to the gate to produce inversion of the pentacene surface (the *C*-*V* curve is shifted towards less negative voltages).The opposite effect occurs in inversion, and electrons are transferred to the Al electrode from the floating gate.

OTFMTs. Successful fabrication of four types of organic memory devices based on OTFT structures has been demonstrated. Three of these devices were using PMMA as with different floating gate materials; a thin film of Au layer, Au nanoparticles, and single-walled carbon-nanotubes. The fourth type of OTFMTs device was with PVP as an insulator and with Au nanoparticles as a floating gate.

AuNPs-based OTFMTs. The electrical properties of AuNPs-based OTFMTs showed much improved memory behaviour compared to that of Au thin film as the floating gate. For both memory transistors, a clear hysteresis was evident in the output and transfer characteristics. The counterclockwise direction of the hysteresis in the transfer characteristics indicates a clear hole charging, and the floating gate can become

charged from the semiconductor surface. When a high enough negative bias is applied to the gate electrode, holes are injected from the semiconducting layer into the Au floating gate (through the top insulating layer), charging up the Au floating gate and programming the memory device. On the other hand, when a high enough positive voltage is applied to the gate electrode, holes are ejected from the floating gate through the pentacene layer (erase process). Therefore, using appropriate negative or positive voltages, the floating gate may be charged and discharged, resulting in a clear shift in the threshold voltage of the transistors. Negative and positive pulses of 1 V resulted in clear write and erase states in both devices.

SWCNTs-based OTFMTs. The electrical properties of the OTFMTs using SWCNTs as the floating gate and PMMA as the insulator enhanced the memory properties compared with that of Au floating gate based OTFMTs. Additionally, SWCNTs-based OTFMTs exhibited good programmable memory characteristics with respect to the write/erase operations, leading to a large threshold voltage shifts. Large memory windows ($\Delta V > 35\ V$) as well as high carrier mobility ($\mu = 0.319\ cm^2\ V^{-1}\ s^{-1}$) were demonstrated for such devices. The floating gate was charged and discharged resulting in a clear shift in the threshold voltage of the transistors after using appropriate negative or positive voltages pulses.

PVP-based OTFMTs. The fourth type of OTFMTs is based on AuNPs as the floating gate and PVP as the insulator. Devices exhibited clear hysteresis in their electrical characteristics, and shifts in the threshold voltage of the transfer characteristics were attributed to the charging and discharging of the floating gate. Pulses of 5 V resulted in clear write and erase states. A large memory window and good retention time are seen in this device.

Endurance behaviour. The data retention and endurance measurements, highlighted in Chapter 6, confirmed that pentacene-based OTFMTs exhibited mechanical stability as well as good electrical reliability. Furthermore the data retention and endurance measurements confirmed the non-volatile memory properties for our memory devices. Therefore, these methods could potentially be integrated with pentacene-based OTFMTs electronic components/circuits.

7.2 Further work

The change in V_{FB} in the fabrication of OMIS structures and V_{th} in OTFTs could be further investigated to produce more controllable devices for future technologies. A study of the electronic and structural nature of the interface between the semiconductor and insulator would also be beneficial. By fabricating more OMIS and OTFTs and studying the relationship between morphology and electronic behaviours is important at this stage. Tools such as SEM and TEM would give a bigger picture of the semiconductor/insulator interface.

Further studies on the transistors stability and endurance could be taken under different environmental conditions. If the OTFTs life time is improved, it will open the door for many applications such as digital components and sensors. The demonstration of stable and reliable OTFTs to be used in plastic technology needs further investigation and moving to flexible substrates. Also using solution processed organic semiconductors should be considered for the all printed organic electronic circuits.

Other floating gates such as ZnO or graphene oxide nanowires could lead to enhanced memory properties. Printed arrays of OMIS and OTFMs on flexible substrate are the ultimate target in near future. In fact, optimal combination of solution processed insulator and semiconductor is needed for future plastic technology.

Publications

Book Chapter

1- **S. J. Fakher**, M. F. Mabrook . Floating Gate Organic Memory with Low-Voltage Operation. In Dekker Encyclopedia of Nanoscience and Nanotechnology, Second Edition. Taylor and Francis: New York, 8 pages, 2013.

Publication in 2012

2- **S. J. Fakher**, and M. F. Mabrook, "Fabrication and characterization of non-volatile organic thin film memory transistors operating at low programming voltages," EPJAP, vol. 60, pp. 10201-1-10201-5, 2012.

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