DOCTOR OF PHILOSOPHY

Electrical, Environmental and Optical Stress Effects on PS-DNTT OTFTs

Za'aba, Nor

Award date:
2018

Awarding institution:
Bangor University

Bangor University

Electrical, Environmental and Optical Stress Effects on PS-DNTT OTFTs

by

Nor Khairiah Za'aba

A thesis submitted for the degree of Doctor of Philosophy

College of Physical and Applied Sciences

School of Electronics Engineering

2018

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

PAPERS AND CONFERENCE PRESENTATIONS

Papers:

1. **N.K. Za'aba**, JJ Morrison, DM Taylor (2017) "Effect of relative humidity and temperature on the stability of DNTT transistors: A density of states investigation" Organic Electronics 45 (2017) 174-181.
2. **N.K. Za'aba** and DM Taylor (2018) "Bias and Related Stress Effects in Organic Thin Film Transistors Based on dinaphtho [2,3-b:2′,3′-f] thieno[3,2-b] thiophene (DNTT)" Organic Electronics 62 (2018) 382-393.
3. **N.K. Za'aba** and DM Taylor (2018) "Photo-induced Effects in Organic Thin Film Transistors based on DNTT " – in preparation

Conference Presentations:

1. N.K. Za'aba and DM Taylor. (2016, July). Environmental Effects on the Operation of DNTT-based Thin Film Transistors. **International Conference on Electronic Materials (IUMRS-ICEM 2016**) at Suntec, Singapore. (oral presentation)
2. N.K. Za'aba and DM Taylor. (2017, January). Environmental Stability of the Density of States in Evaporated DNTT Films. **3rd Innovation in Large-Area Electronics Conference (innoLAE 2017)** at Genome Campus Conference Centre in Cambridge, United Kingdom. (poster presentation)

ABSTRACT

Exposure to moisture and elevated temperatures in organic thin film transistor (OTFT) usually results in significant degradation in the electrical performance. In this thesis the effects of temperature, *T*, and relative humidity, RH, on PS-DNTT OTFTs are investigated. Device characteristics were measured after 30-min exposure to RH that was gradually increased from 20% to 80% with *T* fixed at 20 ºC and also for *T* increasing from 20 ºC to 90 ºC with RH held at 10%. The turn-on and threshold voltages show a negative shift with minimal change in mobility upon exposure to higher RH and T. A very minimal change was observed in the deeper states in the density of states (DoS) that was extracted from transfer characteristics in the linear regime using the Grünewald approach. These results suggest that OTFT instability is due to the flatband voltage shift caused by hole trapping/detrapping in the polystyrene gate dielectric or at the polystyrene/DNTT interface.

Understanding the origin of electrical instability in OTFTs over long periods of time is also essential to realize high performance circuits. In this thesis, the effects of bias stress on PS-DNTT OTFTs is investigated over a range of temperature and relative humidity. It was found that the threshold voltage, V_T, always shifted in the direction of the applied gate voltage. It was also observed that the threshold voltage shift, ΔV_T, reduced as the drain voltage increased. The time-dependences of ΔV_T in both linear and saturation regimes are well described by the stretched exponential function. Contrary to most previous reports, the threshold voltage at long times, $V_T(\infty)$, asymptotes to a value well below the applied gate voltage. The V_T change is minimal with increasing humidity under saturation bias and temperature. In all cases, the DoS exhibits similar behavior with weak features appearing at the deeper states. This is unlikely to be related to DNTT as there is no change in the gate-voltage dependence of mobility, but rather due to a changing flat-band voltage when electron/hole occupancy of interface states changes as the device turns on.

Effect of illumination on the electrical performance as well the underlying physics of these effects are important for the development of several applications such as the backplane for display technology and photosensors. In this thesis the effect of illumination on PS-DNTT OTFTs has been investigated with light of different wavelengths and intensities. The greatest effect was observed at 460 nm with significant changes occuring in the subthreshold slope. Interestingly the profile of the deeper states in the DoS spectrum did apparently change. It was also found that changes in threshold voltage, turn-on voltage, subthreshold slope and responsivity all appear to saturate at higher light intensity due to a trap limited effect. Since there is no significant change observed in mobility, the DoS changes can be explained by (i) trapping of photogenerated electrons, (ii) an unstable shift in the light-induced flat-band ΔV_{FB}, caused by detrapping or neutralization of electrons as the transistor is turned on so that $\Delta V_T(\infty) < \Delta V_{ON}(\infty)$, (iii) accumulation of electrons in DNTT near to source contact or (iv) the effect of the electron quasi Fermi level, QFL. The effect of bias stress and illumination on PS-DNTT has also been investigated with different wavelengths, time and intensity. It was observed that the transfer characteristic shows a parallel shift toward more positive voltages under positive bias stress (PBS) regardless of the wavelength. However under negative bias stress (NBS) at $\lambda \geq 520$ mm, the transfer characteristic shifts negatively due to the dominant effect of hole trapping at the PS-DNTT interface.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deep gratitude to my supervisor, Professor Martin Taylor, for his support, encouragement, and guidance for my research work. His invaluable advice and ideas really help me to gain deeper understanding in the overall process of research and communication. He is the best adviser, the best teacher, and a role model for me.

Special thanks go to Dr. Eifion Patchett for all the helpful discussions and assisting me during my research work. I also owe thanks to Bruno Rostirolla who was my main point of contact when technical issues arose. Sincere thanks are given to Dr. Colin Watson, Dr. Paul Sayers, Dinesh, Vasil, Amjad and Fahad who have willingly helped me with their knowledge and contributed to a pleasant working atmosphere in the group. Many thanks go to Dr. Yanhua Hong and Ben Assinder for their assistance with AFM work.

I would like to show my deepest gratitude to my friends and family especially my parents, Za'aba Mahat and Najibah Shamsudin, for their continuous support and endless love throughout all my life. I also owe my deep thanks to my friend, Mazlina, who has been giving me invaluable support. Finally, my special thanks to my husband, Muhzill. This thesis would not have been possible without the wholehearted support and encouragement from my husband. This thesis is dedicated to all of them.

1 Introduction

1.1 Introduction

There has been significant advancement towards realizing high performance organic electronic circuits. Recently, Watson et. al [1] and Ogier et al [2] successfully fabricated, 5-stage ring oscillators operating at frequencies in the MHz range. Considerable research efforts are also being made in the development of functioning circuits that are compatible with roll-to-roll (R2R) processing [3, 4]. It is known that pentacene is among the most widely studied p-type semiconductor in organic thin film transistors (OTFTs). However, pentacene suffers from the disadvantage of oxidation when exposed to the atmosphere. Unlike pentacene, OTFTs based on dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) are more resistant to oxidation by atmospheric oxygen owing to the larger ionization potential. Moreover, the carrier mobility, μ, which is typically ~ 1 cm^2/Vs is comparable to amorphous silicon and higher than that of pentacene [3, 5]. There is also considerable research effort in the development of functioning circuits based on DNTT [6-8]. Recent reports have shown that OTFTs based on DNTT meet performance requirements for application in electronic circuits [3, 5, 7, 9-12].

Taking these factors together, a DNTT-based OTFT is a potential candidate for the realization of organic electronic circuits that are compatible with vacuum R2R processing. In 2011, Abbas *et al.* [13] introduced a fully vacuum-processed method suitable for R2R OTFT production. The method relied on the preparation of a polymerized dielectric material, tripropyleneglycol diacrylate (TPGDA) [14]. In 2013, Patchett *et al.* [3] fabricated 90 transistor arrays, inverters and ring oscillators with TPGDA as the dielectric layer. This report showed that, with TPGDA as a dielectric layer and polystyrene (PS) as a buffer layer, it was possible to achieve an average saturation mobility of 1.51 cm^2/Vs with a yield of ~ 90% [3]. Working 5- and 7-stage ring oscillators operating in the range from 120 Hz to > 2 kHz with rail voltages, V_{DD} increasing from -15 V to -90 V were also reported [3]. PS is favorable as the dielectric material in OTFT because it is very stable in air and easy to form a uniform thin film by spin coating. It is also well suited for printing technique such as inkjet. Moreover, PS can also be layered using R2R compatible doctor blading and slot dye techniques. Taylor

et al. [15] demonstrated considerable progress by fabricating circuits based on inverters, NOR and NAND logic gates, and more complicated circuits such as a modified Wilson mirror circuit and a simple memory element (SR latch). The logic gates were reported to operate at frequencies in excess of 1 kHz while the current mirror circuit produced currents up to 18 μA [3].

Despite the significant progress represented by the above reports, understanding the stability issues in OTFTs is still necessary to realize high performance circuits. The performance of circuits over long periods of time depends on the stability of individual transistors. Therefore, it is important to achieve long-term stability in the ambient environment at the individual transistor level to ensure high performance. Environmental and electrical stability are very critical issues that must be investigated. Exposure of OTFT to the ambient environment is known to induce degradation of electrical performance. The degradation has been typically attributed to the presence of moisture and oxygen. Although OTFT will be encapsulated, long-term O_2 and H_2O will diffuse through encapsulating films. Moreover, other aspects such as light and temperature are also known to affect the electrical performance of OTFTs. The bias-stress effect is known to change OTFT characteristics as a result of a prolonged application of gate voltage.

However, only a few papers reported on the environmental and bias stress stability of OTFTs based on DNTT and most of these studies only focused on achieving the best stability [5, 16]. Furthermore, there are no reports on OTFTs based on DNTT as the semiconductor and PS as the dielectric. Therefore this thesis aims to investigate the electrical and environmental stability of OTFT based on PS-DNTT as outlined in the next section.

1.2 Thesis Outline

The theoretical background of the work is presented in Chapter 2. Firstly the basic properties of organic semiconductors is discussed followed by a brief review of their charge transport and charge trapping properties. Then, the OTFT operation and the electrical characteristics, as well as the density of states, are explained. Finally, the environmental and the electrical stability of OTFTs are discussed.

The experimental methods are given in detail in Chapter 3, together with a list of the fabrication materials that are used – aluminium, gold, PS and DNTT. Then follows a description of the characterization procedures used for the bias stress and phototransistor measurements.

The effects of moisture and elevated temperatures on the PS-DNTT OTFTs are presented in Chapter 4. Here the density of states in DNTT is analyzed after exposure to a relative humidity (RH) that was gradually increased from 20% to 80% and temperatures from 20 ºC to 90 ºC.

In Chapter 5, the effects of bias stress are investigated over a range of temperature and relative humidity. Here the variation of the threshold voltage is monitored over time, after applying to the device a constant negative voltage on the gate and drain contacts. It also contains a study of the effect of positive bias stress on the operational stability of OTFTs.

In Chapter 6, the effect of illumination on PS-DNTT OTFTs is investigated and discussed. The response to different wavelengths is described first. The influence of electron and hole trapping was identified by monitoring changes in the transfer characteristics during and after illumination. The effect of intensity on the electrical performance was also investigated. Lastly, the dynamic responses to positive and negative bias stresses are discussed in detail.

In chapter 7, results are presented and discussed for the combined effect of bias and illumination on the DNTT OTFTs. In particular, the additional effect of bias stress on the electrical characteristics with a different wavelength, intensity and time are analyzed. Photoresponsivity and photosensitivity of the DNTT OTFTs to different wavelengths and intensity, when subjected to simultaneous bias, are also discussed.

Finally, in Chapter 8, the conclusions derived from various measurements are presented. Future work related to stability and development of n-type and complementary circuit, with DNTT as the p-type semiconductor that is compatible to vacuum roll to roll (R2R) of are also proposed.

2 Background Theory and Literature Review

2.1 Introduction

This chapter presents background theory of organic semiconductor devices. Firstly, the basic properties of the organic semiconductors are reviewed and is followed by discussion of their charge transport and charge trapping properties. Then, the OTFT operation, the electrical characteristics and the density of states are explained. Finally, the environmental and electrical stability of OTFTs are discussed.

2.2 Basic Properties of Organic Semiconductor

Most organic semiconducting materials consist of sp^2 hybridized carbon atoms. The electronic configuration of a carbon atom is $1s^2 2s^2 2p^2$. In the ground state, each 1s and 2s orbital are filled with a pair of electrons. In 2p orbitals, only a single electron occupies the $2p_x$ and $2p_y$ while the $2p_z$ orbital is empty as shown in Figure 2.1. In the excited state, one of the electrons from the 2s orbital is promoted to the $2p_z$ orbital resulting in three sp^2 hybridisation.

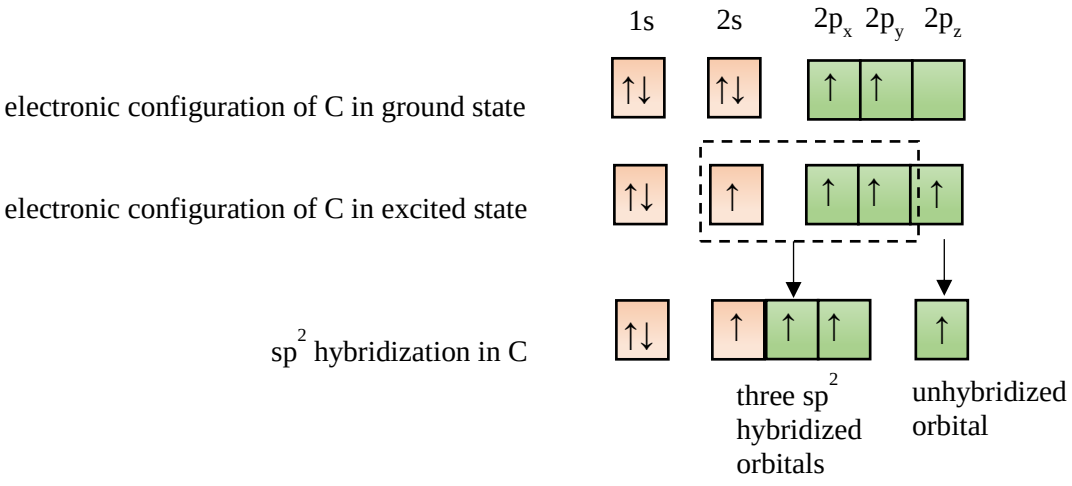

Figure 2.1 Electronic configuration of a carbon atom in the ground and excited states and after hybridisation.

A simple example of hybridization can be demonstrated by the ethylene (C_2H_4) molecule as shown in Figure 2.2(a). It can be seen that σ bonds are form from the overlap between sp^2 orbitals of carbon atoms with s orbitals of hydrogen atoms, ($\sigma(sp^2\text{- s})$). Another σ bond is form between two adjacent carbon atoms ($\sigma\ (sp^2\text{- } sp^2)$). On the other hand, the un-hybridised $2p_z$ orbitals of the carbon atoms form weak π bonds. In benzene, the formation of three double bonds (σ and π bonds) alternating with three single bonds (only σ bonds) between carbon atoms is known as conjugation. The electrons of the double bond are delocalised and move around the molecule as shown in Figure 2.2(b) and (c). The resulting π-bonds are filled with a pair of electrons and unoccupied anti-bonding, π∗, orbitals that are separated by an energy gap, E_g, the energy difference between the highest occupied molecular orbital, HOMO and the lowest unoccupied molecular orbital, LUMO as shown in Figure 2.2(d).

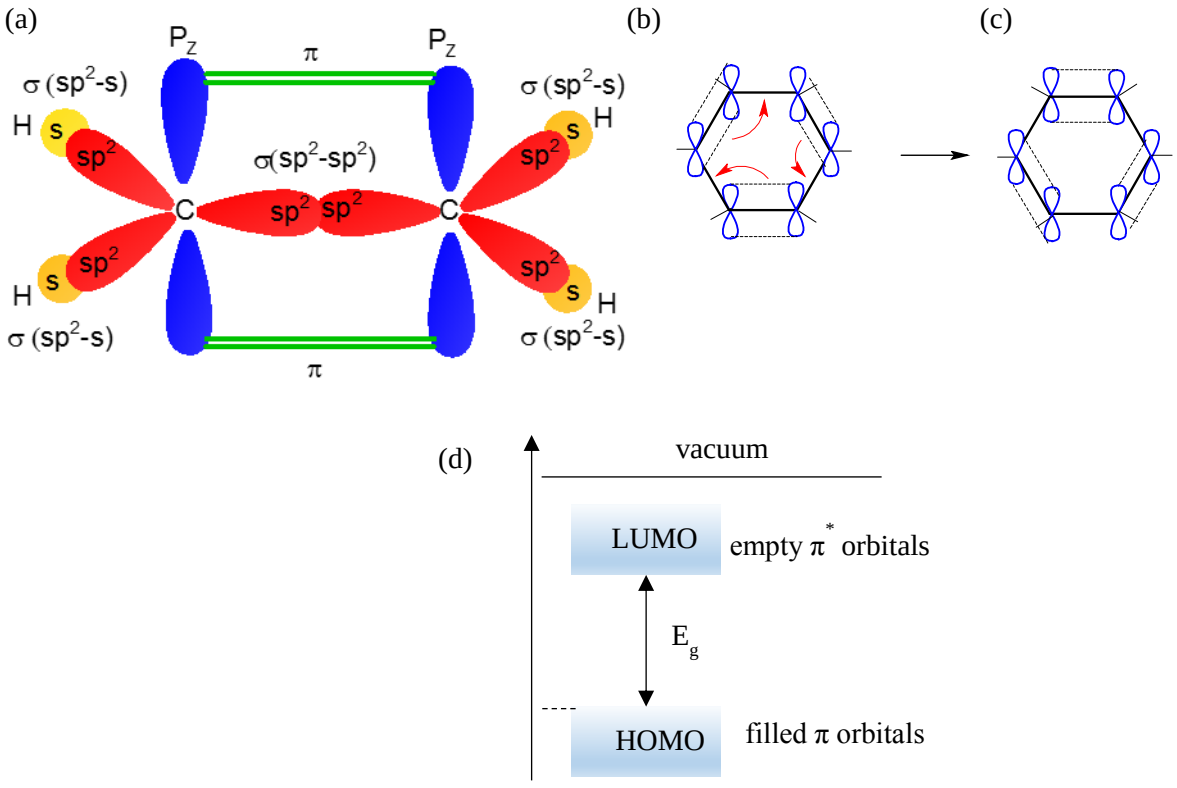

Figure 2.2 (a) Hybridisation of the ethylene molecule structure, (b) electron delocalization in benzene to form the structures seen in (c), and (d) schematic of energy level splitting between HOMO and LUMO.

2.3 Organic Semiconductors

Organic semiconductors can be generally classified as either polymers or small molecules. Most polymeric semiconductor materials are known to have excellent solubility which make them applicable for large area printing processes. On the other hand, the majority of small molecule semiconductor materials are insoluble and often deposited via a vacuum process. One of the most popular small molecule organic semiconductors is pentacene (Figure 2.3(a)). However it suffers instability towards oxidation which in turn causes the carrier mobility to decrease over time when exposed to oxygen and/or humidity [5]. In order to improve the air stability and mobility, Yamamoto and Takimiya [17] synthesized dinaphto-[2,3-b:2`,3`-f]thieno[3,2-b]thiophene (DNTT) (Figure 2.3(b)) with a larger ionization potential of 5.4 eV compared to that of pentacene of 5.0 eV. Owing to its larger ionization potential, the air stability was greatly enhanced. Additionally, DNTT was shown to have a mobility as high as 2.9 $cm^2/V.s$ [17] in evaporated films.

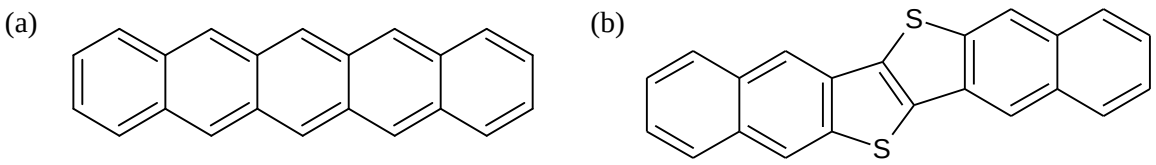

Figure 2.3 Molecular structures of (a) pentacene and (b) DNTT.

Unlike inorganic semiconductors, small molecule organic semiconductors are usually undoped (intrinsic semiconductors). Thus the notion of p-type or n-type organic semiconductors depend on the HOMO and LUMO levels rather than the possibility of doping. As for p-type semiconductors, holes are more easily injected than electrons while n-type it is vice versa. Generally, holes have higher mobility than electrons in organic semiconductor and is used to defining property of p-type organic semiconductor.

2.4 Charge Transport in Organic Semiconductor

The interaction of the delocalized π-electrons discussed in section 2.2 is the key to charge transport in organic semiconductors. Several models have been developed to describe the

charge transport properties. However this section only focuses on the most common transport mechanisms i.e. multiple trapping and release (MTR) and hopping transport.

2.4.1 Multiple Trapping and Release Transport (MTR)

The multiple trapping and release (MTR) model invoked the mobility edge assumption. The mobility edge separates extended states (delocalized states) from a high concentration of charge traps in the localized states (zero mobility). Charge carriers can only be transported via extended states above mobility edge but their movement will be interrupted by trapping in localized states [18]. Then the charge carriers are released back thermally to the extended states and contribute to the transport of charge under influence of an electric field. The MTR transport model predicts an Arrhenius-like temperature dependence. The thermally activated mobility, μ, is usually expressed as [19, 20]:

$$\mu = \mu_0 exp\left(\frac{-E_a}{kT}\right) \tag{2.1}$$

where E_a is the activation energy, with q the electronic charge, k Boltzmann's constant and T the absolute temperature

2.4.2 Hopping Transport

Charge transport through extended states may only occur in a highly ordered system. In a very disordered system, the charge carriers are strongly localized in the band gap. Thus the charge carrier is unlikely to move from localized states to delocalized states. Instead, charge transport is governed by hopping which takes place by thermal activation and tunneling between localized states within the band gap. Since the hopping transport involves some thermal activation, the charge mobility is expected to be temperature dependent following Mott's law [21, 22] described by:

$$\mu = \mu_0 exp\left[-(T_0/T)^{1/1+D}\right] \tag{2.2}$$

where T is temperature, T_0 is the characteristic temperature, μ_0 is the characteristic mobility and and D is the hopping space dimensionality. Transport of charge carriers through the

accumulation layer at the semiconductor-insulator interface of organic thin film transistors (OTFTs) can be described by a two-dimensional (2-D) system [23-26], thus equation (2.1) can be expressed as:

$$\mu = \mu_0 exp\left[-(T_0/T)^{1/3}\right] \tag{2.3}$$

2.5 Trap Density of States (DoS) in Organic Semiconductor

Organic semiconductors generally exhibit a disordered structure that leads to a distribution of localized states which can act as traps for charge carriers which in turn, could limit the charge transport and device performance. As shown in Figure 2.4, these localized states (trap density of states) are located in the band gap of the semiconductor between HOMO and LUMO. Shallow states usually located within a few *kT* of HOMO/LUMO while the deep states are located further away. Also, below the HOMO and above the LUMO are delocalized states in which carriers are mobile.

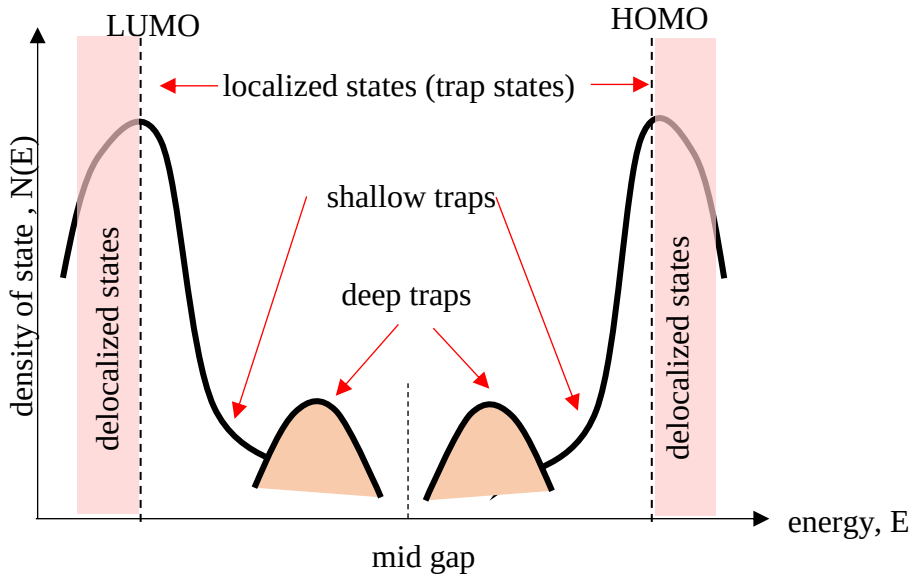

Figure 2.4 Schematic of density of states in an organic semiconductor adapted from [27].

Trap states in the semiconductor could originate from grain boundaries [28] , chemical impurities [29] or from the gate insulator [30]. Several methods have been developed to quantify the trap density of states (DoS) of OTFTs which have been comprehensively

reviewed by Kalb and Batlogg [31]. One of the simpler analytical methods for DoS extraction was introduced by Grünewald et al [32]. It is simple because, the trap DoS relative to the Fermi level can be extracted from a single transfer characteristic. This model has been applied to describe the DoS in both inorganic [33, 34] and organic [31, 35-37] semiconductors. Basically, the Grünewald model is based on the gate-induced incremental increases in device current and the band-bending resulting from the accumulation of charge carriers at the semiconductor/insulator interface [37]. Derivation of this method is presented in section *2.6.4*.

2.6 OTFT Operation and Characteristics

2.6.1 OTFT Device Architecture

Figure 2.5 shows four possible cross-sections of OTFT structures. The device structural configuration is based on the position of the electrodes (drain, source and gate) relative to the organic semiconductor. In a staggered structure, the source, and drain electrodes are located away from the semiconductor/insulator interface (Figure 2.5(a) and (c)) whereas in the coplanar structure, the source, and drain electrodes are in the plane of the interface as shown in (Figure 2.5(b) and (d)). Both staggered and coplanar structures are further categorized based on the position of the gate contact e.g. top-contact-bottom-gate and top-gate-bottom-contact.

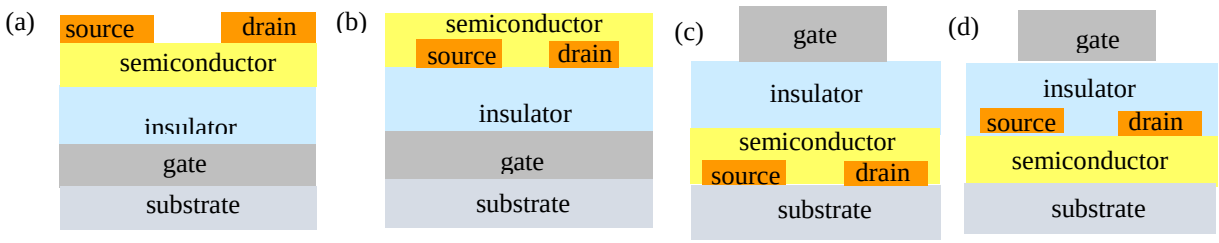

Figure 2.5 Cross-sections of simplified OTFT device configurations: (a) top-contact-bottom-gate (staggered), (b) bottom-contact-bottom-gate (coplanar), (c) top-gate-bottom-contact (staggered) and (d) top-gate-top-contact (coplanar).

2.6.2 OTFT Operation Principle

In order to explain the operation of an OTFT, it is important to understand the energy band diagram of the metal-insulator-semiconductor (MIS) structure. Figure 2.6 shows the MIS energy band diagrams based on a doped p-type inorganic semiconductor. In an ideal MIS structure, under a flatband condition, V_G = 0V the work function difference between metal, $q\phi_m$, and semiconductor, $q\phi_s$, is zero. The Fermi level, E_{FM} of the metal is aligned with the Fermi level, E_{FS} of the semiconductor as shown in Figure 2.6(a). Electron affinities for the insulator and semiconductor are denoted as χ_i and χ respectively. All bands remain flat and carriers are in thermal equilibrium. Here, the conduction band edge, E_C is analogues to the LUMO level in organic semiconductors whereas the valence band edge, E_V corresponds to the HOMO level. The energy gap between E_V and E_C is denoted as E_G while the potential energy difference between E_{FS} and the intrinsic Fermi level, E_{Fi} in the bulk is defined as $q\Phi_b$.

When a negative gate voltage, V_G is applied across the semiconductor, majority holes drift to, and accumulate near the insulator-semiconductor interface. As a result, E_V bends upwards and moves closer to E_{FS} at the insulator-semiconductor interface as shown in Figure 2.6(b). The difference between E_{FM} and E_{FS}, is equal qV_G. The potential energy drop across the insulator is defined as qV_0 and the amount of band bending from the interface into the bulk semiconductor is represented by qV_s. For a larger negative V_G, the amount of band bending is greater. When a small positive V_G is applied, majority holes move away from the interface thus exposing the immobile negative charges of the ionized acceptors as seen in Figure 2.6(c). As a result, a depletion region of immobilized charged acceptor ions is formed and the bands bend downwards. When a larger positive V_G is applied, the electric field is strong enough to cause electrons to accumulate at the interface. At this point, the band bending increases beyond E_{Fi} and causes inversion.

In contrast to a doped semiconductor, organic semiconductors are often undoped (intrinsic) and do not operate in the inversion mode but in the accumulation mode. In intrinsic case, the depletion mode is the same as flatband (no injected hole in the device) and accumulation. In intrinsic, the density of holes and electrons are always equal. At absolute zero temperature the valence band is completely filled and the conduction band is completely empty. At high temperature, electrons from valence band get enough thermal energy and left behind equal

number of holes in valence band. However, in organic semiconductor, E_{FS} generally is closer to the HOMO being held there by trap states. The band gap is too large to generate electron/hole pair thermally. For voltages more positive than flatband voltage, part of the applied voltage appears across semiconductor and the electrons in conduction band were attracted to the surface and the holes were pushed away from the interface shown in Figure 2.6(d). For voltages more negative than flatband voltage, holes were attracted to the semiconductor surface which is similar to the case of an extrinsic semiconductor in accumulation as shown in Figure 2.6(b).

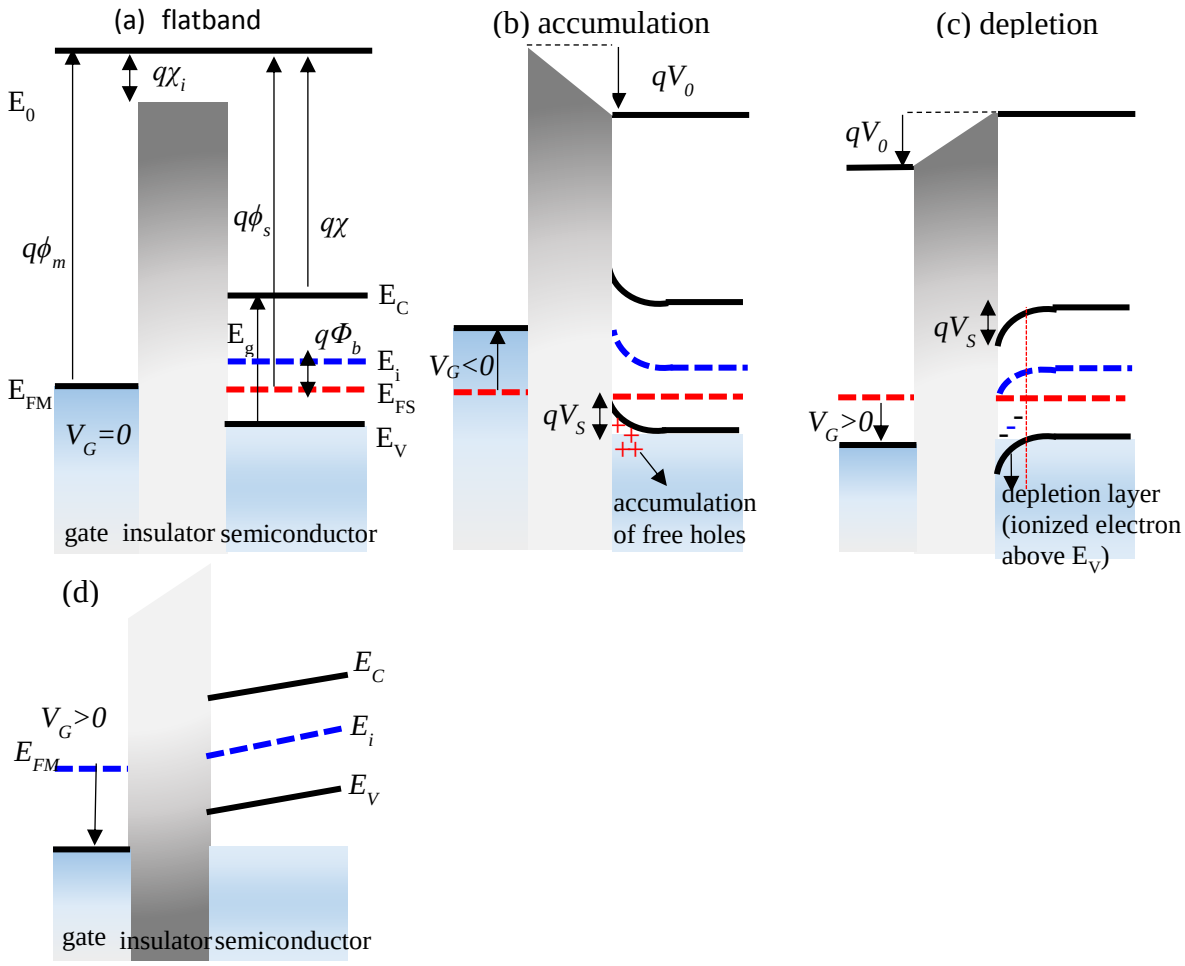

Figure 2.6 Band diagram of and ideal metal-insulator-semiconductor (p-type) structure showing (a) flatband conditions, V_G = 0 V (b) accumulation, negative V_G and (c) depletion positive gate V_G. Band diagram of intrinsic semiconductor with (d) positive gate voltage.

In general OTFTs operate in the accumulation regime. The operating principle of a p-type organic transistor is illustrated in Figure 2.7. When $V_G < 0$ V, and $V_D = 0$ V is applied between gate and source electrodes, holes are induced by the electric field across the insulator and accumulate at the semiconductor/insulator interface as shown in Figure 2.7(a). This accumulation of holes will form a conducting channel in the semiconductor between the source and drain electrodes. When a small drain voltage is applied ($V_D < 0$ V), the charge carriers flow from the source to the drain electrodes and generate a large drain current, I_D as shown in Figure 2.7(b). At this point, I_D increases linearly with the field induced charge density and is known as linear regime.

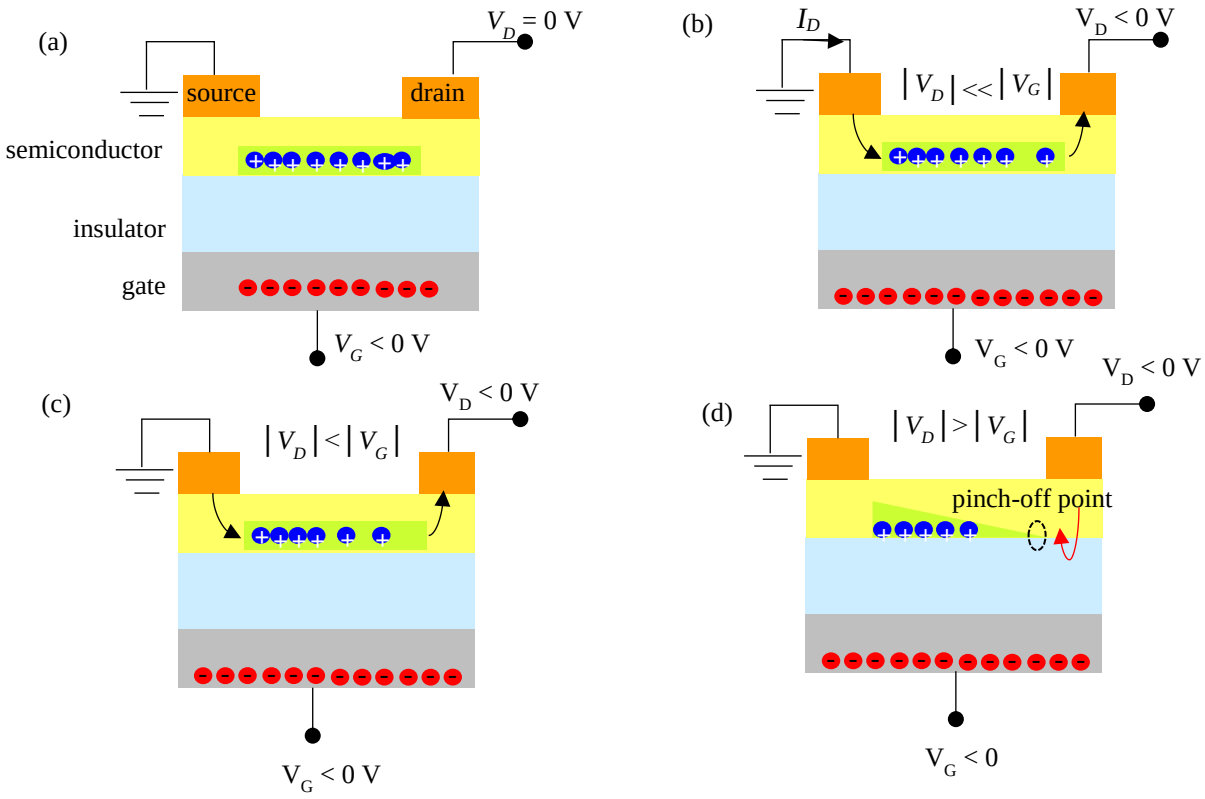

Figure 2.7 Operating stages of an OTFT, (a) -V_G, V_D= 0V, (b) -V_G, -V_D (slow), (c) -V_G, -V_D (medium) and (d) -V_G, -V_D (high).

As the drain voltage, V_D increases towards more negative values ($|V_D| < |V_G|$), for a given V_G, the charge density at the drain electrode starts to decrease but at the source electrode, they remain the same[38] as shown in Figure 2.7(c). Consequently, drain current I_D increases

at a slower rate and there is no longer a linear correlation. When V_D increases until a point where $|V_D| > |V_G|$, the channel at the drain electrode starts to pinch-off (Figure 2.7(d)) after which I_D saturates and become independent of V_D.

2.6.3 OTFT Characteristics and Parameter Extraction

The current-voltage characteristics of an OTFT were derived based on the gradual channel approximation with the x direction is defined as perpendicular to the channel and *y* parallel to the channel as shown in Figure 2.8. The edge of the source is at y=0 and the edge of the drain at y=*L*. It is assume that the mobility along the channel is constant. However, this is not always fulfilled in some organic semiconductor system. Then it is assume that the electric field, E_x through the insulator is much higher compared to the electric field, E_y along the channel. This is known as gradual channel approximation.

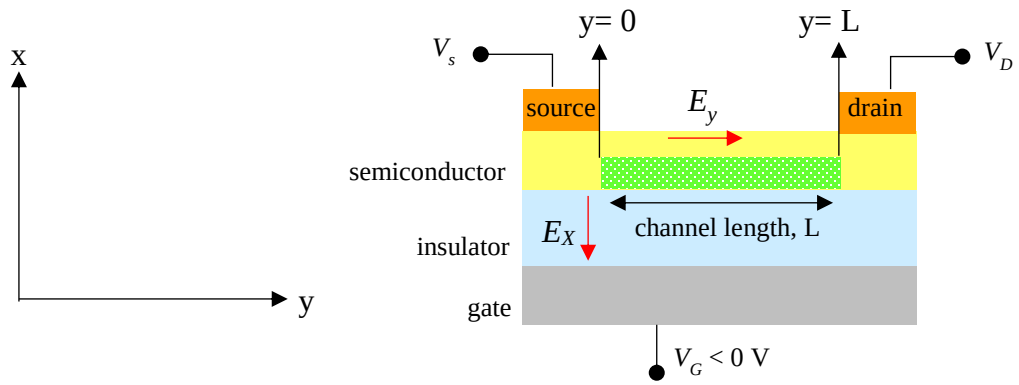

Figure 2.8 Cross-sectional view of the channel region of TFT used to derive the gradual channel approximation with x direction is perpendicular to the channel and y is parallel to the channel.

By applying a negative voltage V_D at the drain, the charge density $Q(y)$ that is induced by V_G along the channel is given by:

$$Q(y) = C_i[(V_G - V_T) - V(y)] \tag{2.4}$$

where *Ci* is the capacitance per unit area of the insulator, V_T is the threshold voltage and *V(y)* is the channel voltage. The charge density that flows from source to drain generates a current I_D *(y)* given by:

$$I_D = -WC_i[(V_G - V_T) - V(y)]\left(\mu E_y\right) \tag{2.5}$$

where *W* is the width of the channel and μ is the charge mobility. Substituting E_y = *-dV/dy* into equation (2.5) gives

$$I_D = \mu WC_i[(V_G - V_T) - V(y)]\left(\frac{dV}{dy}\right). \tag{2.6}$$

Integration of equation (2.6) along the channel from *y = 0* to *y = L* and *V(y) = 0* to *V(y)* =V_D leads to:

$$\int_0^L I_D dy = \mu WC_i \int_0^{V_D} [(V_G - V_T) - V(y)]dV \tag{2.8}$$

which eventually yields,

$$I_D = \frac{\mu WC_i}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right]. \tag{2.9}$$

For V_D << V_G the quadratic term in equation (2.9) can be neglected. This defines the linear regime of the OTFT and the drain current can be described by:

$$I_D = \frac{\mu_{lin} WC_i}{L}[(V_G - V_T)V_D] \tag{2.10}$$

where μ_{lin} is the field effect mobility in the linear regime and can be extracted from the transconductance, $\frac{\partial I_D}{\partial V_G}$ that is:

$$\mu_{lin} = \frac{L}{WC_{ins}V_D}\frac{\partial I_D}{\partial V_G}. \tag{2.11}$$

For $V_D \geq (V_G\text{-}V_T)$, the channel is in pinch-off, so I_D become independent of V_D and saturates. This is known as the saturation regime of the OTFT. Substituting $V_D = (V_G\text{-}V_T)$ into equation (2.9), the expression for the drain current in the saturation regime becomes:

$$I_D = \frac{\mu_{sat} W C_i}{2L} (V_G - V_T)^2 \tag{2.12}$$

where the field effect mobility in the saturation regime , μ_{sat} is given by:

$$\mu_{sat} = \frac{2L}{WC_{ins}} \left(\frac{\sqrt{\partial I_D}}{\partial V_G} \right)^2 . \tag{2.13}$$

The current-voltage characteristics of an OTFT can be described by output characteristics (I_D versus V_D) and transfer characteristics (I_D versus V_G). Figure 2.9(a) shows typical output characteristics obtained in the study for an OTFT based on DNTT with polystyrene as the gate insulator. It shows a clear linear and saturation region. The transfer characteristic in the linear regime plotted on linear and semilog axes is shown in Figure 2.9(b). The threshold voltage, V_T is defined as the gate voltage, V_G, intercept (i.e., $I_D = 0$) of the linear extrapolation of the $I_D - V_G$ plot. The linear mobility, μ_{lin} can be estimated from the slope of a linear fit to the I_D-V_G plot using equations (2.11). In the case of the saturation regime, the transfer characteristic is plotted as $I_D^{1/2}$-V_G and the saturation mobility, μ_{sat} can be determined from the slope of the linear fit the I_D-V_G plot using equation (2.13).

The onset voltage V_{ON} can be estimated from the semi-log plot of the transfer characteristics. It should correspond to the voltage above which I_D rises above its off value, i.e. the current flowing through the bulk semiconductor from source to drain in the absence of an accumulation channel. However in the present case, it was defined as the value of V_G when the magnitude of I_D increased above the displacement current, induced by the V_G sweep. I_{on}/I_{off}, is the ratio of the drain current in the on-state at a certain gate voltage to the drain current in the off-state. It is desirable to have this ratio as large as possible. The subthreshold slope, *SS* is extracted from the steepest slope of the semilog plot using the relation:

$$SS = \frac{\partial V_G}{\partial (log I_D)} . \tag{2.14}$$

For an intrinsic semiconductor, V_{ON}, should occur at flatband, $V_G = 0$V. Departures from this can be caused by the work function difference between the source-drain metal contacts

(usually gold) and the gate electrode (often aluminium). A more important effect is the flatband voltage shift caused by interface trapped charges, N_{it} which can be estimated from:

$$\Delta N_{it} \approx \frac{1}{q} C_{ins} \Delta V_{FB} \,. \tag{2.15}$$

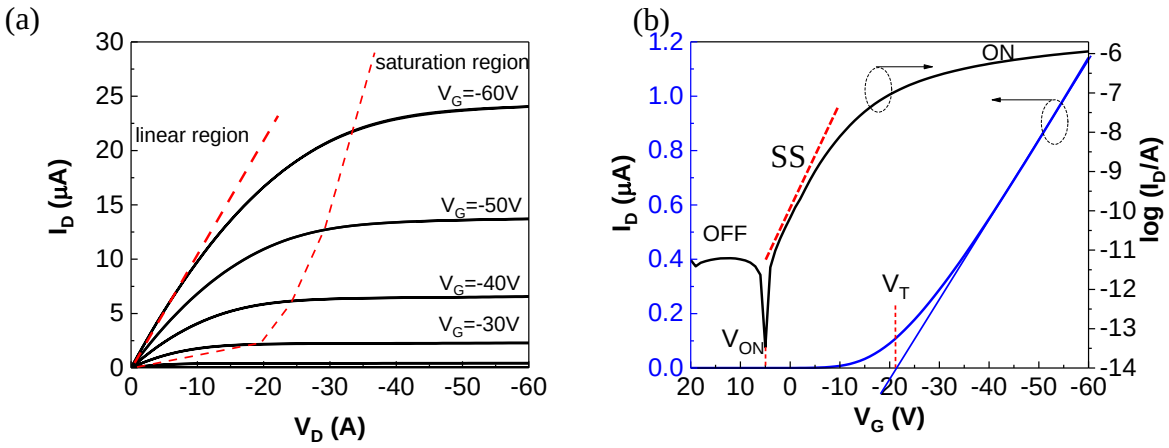

Figure 2.9 (a) Output characteristics and (b) The transfer characteristic of a PS-DNTT TFT measured in the dark at a drain voltage, V_D = -1V plotted in linear and semilog scale.

2.6.4 Extraction of the Density of Trap State Using the Grünewald Model

i. Grünewald Model

The extraction of DoS, from the transfer characteristic of a thin film transistor was performed using the Grünewald et al model [18]. This was accomplished by first developing the relationship between the gate-dependent insulator/semiconductor interface potential, V_0, and the effective forward voltage, $V_F = (V_G - V_{ON})$. This is achieved by numerically solving the equation

$$\exp(\beta V_0) + \beta V_0 - 1 = \beta \frac{C_i l}{\varepsilon_S \varepsilon_0 I_0} \left[V_F I(V_F) - \int_0^{V_F} I(\tilde{V}_F) d\tilde{V}_F \right] \tag{2.16}$$

where l is the thickness of the semiconductor, $\beta = q/kT$, ε_S the relative permittivity of the semiconductor and ε_0 the permittivity of free space. I_0 is the off-current at V_{ON}. Following

further manipulation, the total hole density $p(V_0)$ and the density of states $N(E)$ may be obtained from

$$p(V_0) = \frac{C_i^2}{\varepsilon_S \varepsilon_0 q^2} V_F \left(\frac{dV_0}{dV_F} \right)^{-1} \tag{2.17}$$

and finally, the density of states, N(E) from,

$$N(E) \approx \frac{dp(V_0)}{dV_0}. \tag{2.18}$$

The extraction method is described more fully in appendices A, B and C.

ii. Subthreshold Slope

Kalb and Batlogg [31] suggest that the derivation of subthreshold slope, *SS* could give a rough estimation of the DoS. Assuming that the DoS is independent of energy, *SS* can be described by [39]

$$SS = \frac{kTln10}{q} \left[1 + \frac{q}{C_i} \left(\sqrt{\varepsilon_S N_b} + qN_{it} \right) \right]. \tag{2.19}$$

Here N_b (in $cm^{-3}eV^{-1}$) is the density of deep bulk traps and N_{it} (in $cm^{-2}eV^{-1}$) is the density of interface traps. Assuming that there is no contribution from the bulk, equation (2.19) may written as:

$$SS = \frac{kTln10}{q} \left[1 + \frac{q^2}{C_i} N_{it} \right]. \tag{2.20}$$

and may be used to estimate the density of interface states.

2.7 Environmental and Electrical Stability in OTFT

1.2.1 Effect of RH and Temperature

OTFTs that are environmentally stable are of great importance for the development of functioning circuits. Exposure of an OTFT to ambient atmosphere leads to degradation in the device performance. In general, device degradation is manifest as a shift in V_{ON} and V_T, reduction in μ, increases in I_{off} and SS and the appearance of hysteresis in device characteristics. Risteska et al [40] showed that in a pentacene-based device, the presence of oxygen, O_2, during bias stress induce shifts in V_{ON} due to formation of acceptor-like states. Chabinyc et al [41] found that ozone, O_3, caused a shift in V_{ON} for OTFTs based on P3HT. However, this is not the case for DNTT. Patchett et al [3] showed that exposure to ambient air for 48 hours stabilized and improved the device performance.

Several reports investigated the effect of moisture on TFT performance. Hoshino et al [42] found that moisture increased I_{off} while Chabinyc et al [43] showed that moisture reduced μ. Noh et al [44] showed the presence of hysteresis in pentacene OTFTs based on polar insulators such as polyvinylpyrrolidone (PVP) and poly(methyl methacrylate) (PMMA) upon exposure to moisture suggesting that moisture induces a polarization in the bulk insulator. However, Hong et al [45] observed hysteresis in pentacene OTFTs with a non-polar insulator such as polystyrene. Ding et al [46] observed that moisture shifts V_T and increases I_{off} in DNTT OTFTs but μ remain unchanged. This suggests that the presence of moisture may induce charge trapping either at the insulator/semiconductor interface, in the insulator or in semiconductor causing changes in the flatband voltage. Goldmann et al [47] observed a step-like feature in the transfer characteristics of single crystal pentacene with SiO_2 as the insulator which was attributed to a water-related trap state in the semiconductor.

Generally, the effect of temperature on OTFTs is investigated for understanding the transport properties in the materials. However, thermal stability is also important for providing insight into degradation mechanisms for practical application. Previous reports showed that DNTT is thermally stable up to 250 ºC [48]. Further investigation was carried out by Kuribara et al [49] on DNTT to demonstrate sterilization processes for medical application. However these

papers only focused on applications and the detailed correlation between temperature and the device properties was not fully understood.

2.7.1 Effect of Bias Stress

Application of prolonged gate bias in OTFTs causes a shift, ΔV_T of the threshold voltage with time which is known as the bias stress effect. These instabilities are explained by trapping of the mobile carriers either within the semiconductor, semiconductor/insulator interface or in the insulator. If the charges are trapped at the interface, they no longer contribute to the current and cause the interface to become more repulsive to the remaining mobile charges. Thus a higher negative (positive) gate voltage is needed to maintain the drain current. Typically, threshold voltage shifts towards the applied gate voltage. In a p-type semiconductor, a negative gate bias causes holes to be trapped which leads to the shift in the threshold voltage towards more negative voltage. Meanwhile a positive gate bias, leads to positive shifts in the threshold voltage. If hole/electron trapping occurs in the deep traps (slow states) at the interface of the semiconductor/insulator or in the insulator, the shape of the transfer characteristics and hence the carrier mobility will not change. On the other hand, if hole/electron trapping occurs within the semiconductor or in fast interface states, the shape of the transfer characteristics will be affected with deleterious effect on mobility.

The bias stress effect has been extensively studied in p-type semiconductors and much progress has been made to demonstrate that it can be as stable as α-Si TFT. In the case of negative bias stress, for a pentacene/polyimide based OTFT which was annealed at 140 ºC for 12 hours, Sekitani et al [50] showed good stability with $\Delta V_T < 0.4$ V after stressing for 11 h. Zschieschang et al [9] investigated the stability of DNTT based OTFTs and observed ΔV_T =70 mV after stressing for 66 hours. As reviewed by Sirringhaus [51], moisture is one of the important factors that cause the bias stress effect in OTFTs [47, 52]. Several techniques were used to prevent the ingress of moisture including using self-assembled monolayers [53-55] or hydrophobic dielectrics such as low-*k* Cytop^{TM} [56, 57] to passivate the interface. Several reports had showed that, application of positive bias stress leads to a positive voltage shift [58-60]. This effect is believed to be due to electron trapping and injection at the

interface or in the insulator [51]. Under illumination within the band gap of the semiconductor, this effect is significantly enhanced [46, 61-65].

It is also worth noting that in many cases, bias stress had minimal effect on the carrier mobility [66-69]. However, there are some cases reported of mobility degradation [70, 71]. This is believed to be due to trapping of electrons in states at the interface [72]. Goldmann et al [47] observed degradation in the subthreshold slope, *SS* which is reflected in a step-like feature in the transfer characteristics of single crystal pentacene with SiO_2 insulator. This feature was attributed to the water related trap state in the semiconductor [47, 73]. It is also known that the bias-stress effect is reversible. It can be recovered over time in the dark by grounding the source, drain and gate electrodes, or more rapidly under illumination to remove the effect of hole trapping under negative bias stress [69, 74, 75].

The dependence of ΔV_T on time was quantitatively described the using stretched exponential function. Originally this model was developed to described the threshold instability in α-Si:H TFTs [76]. However many researchers have used this approach for describing the threshold instability in OTFTs [68, 77-80] which is given by:

$$\Delta V_T(t) = |V_T(\infty) - V_T(0)| \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \tag{2.10}$$

where $V_T(\infty)$ is the threshold voltage after a long stress time, $V_T(0)$ is the threshold voltage before bias stress, τ is the characteristic trapping time for filling the trap states, while β is the stretched-exponential factor related to the distribution in characteristic trapping time, τ. Mathjissen et al [80] described the time-dependence of ΔV_T in bottom-contact OTFTs with different semiconductors including polytriarylamine (PTAA), poly(3-hexylthiophene) (P3HT) and poly(9,9′-dioctyl-fluorene-co-bithiophene (F8T2). Choi et al [81] used the stretched exponential equation to compare the performances of OTFTs based on pentacene with different molecular weight of polystyrene. This work also showed that τ increases with molecular weight suggesting the presence of a higher trap density in low molecular weight PS. Zschieschang et al [75] investigated the effect of drain bias on the V_T stability and found that ΔV_T(t) is well described by the stretched exponential function. The work also showed that both $V_T(\infty)$ and τ increase as V_D is decreases suggesting that the number of charge carriers

available for trapping are greater when stressing at low V_D [82, 83]. Other than the stretched exponential function, Gomes et al [52] described the dependence of ΔV_T on time by a stretched-hyberbola [52]. In some cases the time-dependence of ΔV_T can be simplified to a power-law [54] or extended to a double stretched-exponential [84, 85].

The stretched-exponential function can be extended with the measurement of drain current decay with time. Most authors presumes that $V_T(\infty) = V_G$ such that $(V_G - V_T(\infty)) = 0$, i.e. when the gate field becomes insufficient to sustain an accumulation channel of free holes.[19, 86-88]. Based on this assumption Zhang et al [86] developed the extended model of the stretched exponential function based on drain current in the form of:

$$I_D(t)/I_D(0) = exp\left(-\frac{t}{\tau}\right)^{\beta}. \tag{2.11}$$

The model was based on measuring current in the saturation regime, but the square term seems to be missing from the entire equation (see section 2.6.3) which may be an editorial error. To date only a few reports have appeared on the bias stress effect in DNTT devices. Zschieschang et al found that *SS* does not return to its original value after stressing for 24 hours [5]. Hannah et al [16] showed the stability of the device improving with longer chain length in series of alkylphosphonic acids (C_nPA). However these papers only focused on achieving the best stability. Further studies of the bias stress effect in DNTT is essential and needs to be understood since DNTT shows excellent performance for electronic applications.

2.7.2 Effect of Illumination

The effect of illumination on the electrical performance as well the underlying physics of these effects are important for the development of several applications such as the backplane for display technology and photosensors. It is known that, when a device is illuminated with photons of energy equal to or higher than the band gap of the organic semiconductor a large number of excitons are generated. A fraction of these excitons will dissociate into holes and electrons. When a negative gate bias, $V_G < 0$ V and drain bias, $V_D < 0$ V is applied, these photogenerated holes will flow to the drain electrode, leading to an increase in the photocurrent while photogenerated electrons move away from the drain electrode and may

become trapped in localized states within the semiconductor, at the interface of the semiconductor/insulator or in the insulator.

Two mechanisms that are responsible for the change in transfer characteristics during illumination are known as the photoconduction and photovoltaic effects [89-91]. Noh et al [92] distinguished fast and slow responses in OTFTs based on pentacene and sexithiophene (6-T). The fast response was attributed to the photo-generation of holes and electrons that leads to an increase in the current through the bulk semiconductor between source and drain, also known as the photoconduction effect. The photocurrent usually dominates in the off-state of the device although some reports argue that the channel current itself is also enhanced [92-95]. The slow response was attributed to a light-induced shift in threshold voltage and leads to an increase in the channel current in the subthreshold region. This is known as the photovoltaic effect.

It has been discussed previously that the effect of hole trapping under negative bias stress could be removed by exposing the device to illumination [69, 74, 75]. Debucquoy et al [96] showed that illumination accelerates ΔV_T under positive bias stress. A similar effect was also observed by Taylor et al [65] using a MIS capacitor structure. Recently, phototransistors based on DNTT have been reported by Milvich et al [97], Yu et al [98] and Chu et al [99]. However these papers only focused on photosensor applications. The detailed correlation between light parameters and the device performance is not fully understood. Although the effect of light on organic semiconductors has been reported by many authors [54, 91, 94], there are no reports specifically describing electro-optical effects in DNTT devices.

2.8 Summary

This chapter presented the fundamental properties of organic semiconductors and the basic operation of OTFT. A procedure for the extraction of OTFT device parameters including density of state was also explained. Environmental and bias stress stability of OTFT were reviewed. Lastly the effect of illumination on OTFTs were also discussed. From the foregoing, DNTT is an excellent candidate for organic circuit applications. However, more needs to be understood about the stability of OTFTs based on DNTT. Accordingly, the

following chapters report a detailed study on environmental, bias stress and optical stability of OTFTs based on DNTT as the semiconductor and polystyrene as the gate insulator.

3 Experimental Details

3.1 Introduction

This chapter presents details of the materials and methods used in this work. The semiconductor and the insulator materials are introduced first and followed by a description of the processes used to fabricate the transistor test devices. Finally, the characterization procedures followed in the bias stress and phototransistor measurements are described.

3.2 Materials

In this work, dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) was used as the semiconductor material while polystyrene (PS) was used as the gate insulator. Figures 3.1(a) and (b) show the molecular structures of DNTT and PS. DNTT was synthesized by Dr. J. Morrison at Manchester University following the same route as published by Yamamoto and Takimiya [17]. PS with an average molecular weight, M_W of ~ 350,000 was purchased from Sigma Aldrich. Flexible polyethylene naphthalate (PEN) substrates were purchased from DuPont Tenjin.

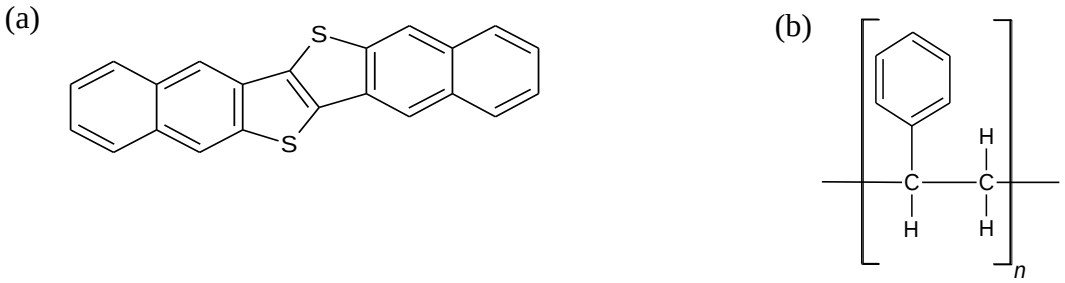

Figure 3.1 Molecular structures of (a) DNTT and (b) PS.

3.2.1 Preparation of the PS Solution

A 9% wt/wt solution of PS in toluene was prepared in the clean room at room temperature. PS pellets were dissolved into the toluene in a pre-cleaned glass vial. Vials were cleaned following the same methods as described above for the substrates. The resulting solution was

sonicated until the PS was fully dissolved. Finally, the solution was filtered with a 0.2 µm PTFE syringe filter and stored inside a fridge in the cleanroom when not in use.

3.2.2 Substrate Cleaning Procedure

The PEN substrates were cut into 6.5 cm x 6.5 cm squares to fit with the shadow masks. They were then placed in a beaker filled with Decon 90 /deionized water and sonicated in an ultrasonic bath for 10 minutes. After rinsing with deionized water the substrates were dried in a stream of nitrogen gas. The substrates were then given final rinses in deionized water, acetone, methanol and 2-propanol and again dried with nitrogen gas.

3.3 Device Fabrication

The device structure of bottom-gate top-contact PS-DNTT OTFTs used in this work is shown in Figure 3.2. Devices were fabricated using the same mask set as described by Patchett et al [3, 100]. The mask comprised of 18 x 5 array of 90 transistors as shown in Figure 3.3. Two blocks of 9 OTFTs were arranged in 5 rows. In each row the channel length, *L* increased in step from 50 µm to 200 µm. The block in the left-hand side has a width, *W* of 2 mm with aspect ratio, *W/L* ranging from 40 to 10. The right-hand side block had a constant *W/L* ratio of 20, yielding a width ranging from 1 mm in the first row to 4 mm in the fifth row. Five circular capacitors with a diameter of 2 mm were arranged diagonally across the substrate in order to extract the capacitance per unit area of the gate dielectric.

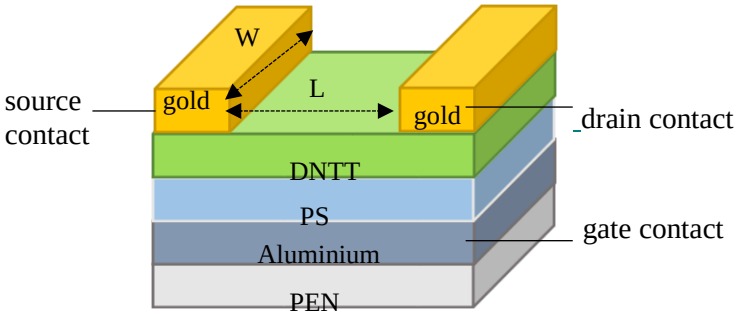

Figure 3.2 Structure of bottom-gate top-contact of PS-DNTT OTFT fabricated on PEN substrate where *L* and *W* are the channel length and width respectively.

Only OTFTs with *L*=150 µm or 200 µm and *W*= 2mm were used in this work. The fabrication of bottom-gate top-contact PS-DNTT OTFTs was undertaken in a nitrogen glovebox (Glovebox Technology Ltd) with an integrated, computer-controlled, multisource evaporator (Kurt Lesker Ltd) with pre-programmed evaporation rates and quartz crystal thickness monitors. Firstly, a 70-nm thick aluminium film was deposited onto the PEN substrate by thermal evaporation through the gate shadow mask to define the gate electrodes. PS was spin-coated onto the metallized substrate from the toluene solution at 1000 rpm for 60 s. The substrate was then placed on a hot-plate for 10 minutes at 100 ºC to dry off any remaining solvent. The resulting film was ~1 µm thick as determined by AFM measurement with a measured dielectric constant ~2.6. A 70-nm thick DNTT film as measured from the quartz crystal in the deposition chamber was then deposited onto the PS by thermal evaporation through a shadow mask to define the area of the semiconductor. Finally, 60-nm thick gold was deposited by thermal evaporation through the source-drain shadow mask to complete the devices. A photograph of the actual device is shown in Figure 3.4(a).

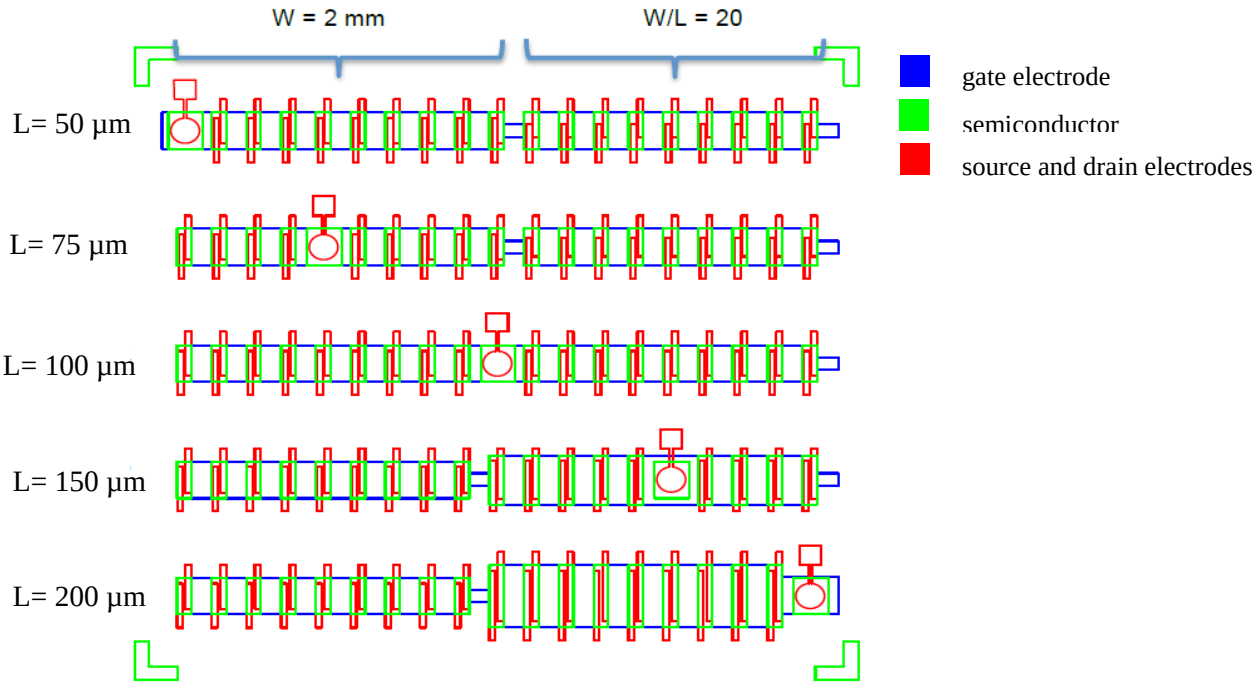

Figure 3.3 Mask features 18 x5 arrays of 90 transistors with 5 circular capacitors of 2mm diameter arranged diagonally across the substrate. Source and drain contacts are depicted in red, gate contacts in blue and semiconductor in green (adapted from [100]).

3.4 Transistor Characterization

Transistor characterization was performed using a source/measure unit (Keithley model 2636B). All measurements and data acquisition were automated using TSP™ Express software through a LAN connection. Transistor characterization was undertaken with two different arrangements. In Chapters 4 and 5, the test device was placed in an aluminium test box while in Chapters 6 and 7 devices were placed in a cryostat. Details of the transistor characterization setup for Chapter 6 and 7 will be described in section 3.6. For environmental and bias stress measurements (Chapter 4 and 5), the transistor was placed inside a grounded metal test box (Figure 3.4(b)) with dimensions of 11.7 cm x 9.2 cm x 2.8 cm. The OTFTs were mounted on a PTFE block fixed to the base of the box and connections made with gold wire and silver paste from the gate, source and drain electrodes to gold pins fixed into the block. Connections were made from the pins to BNC connectors and thence via tri-axial cables to the source-measure unit.

(a) (b)

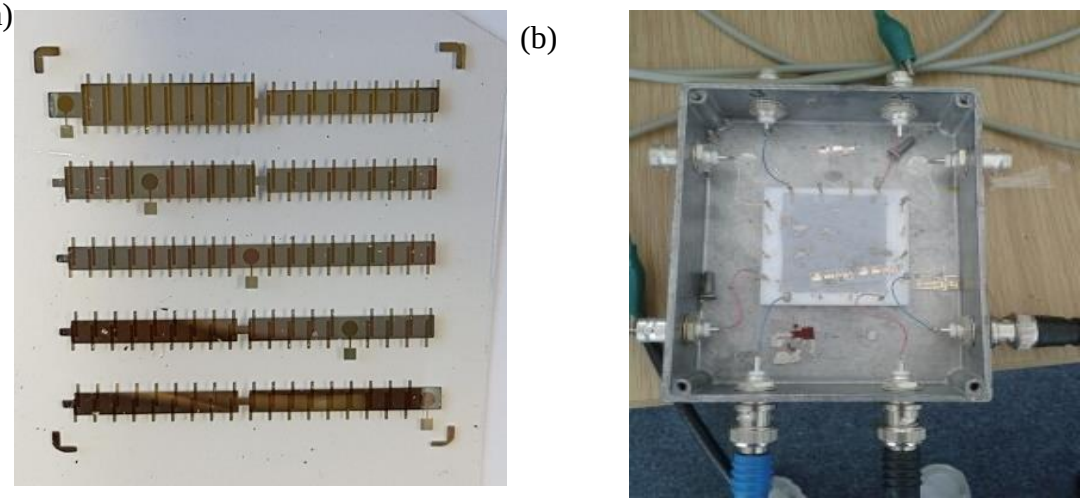

Figure 3.4 Photograph of the (a) actual PS-DNTT OTFTs and (b) aluminium test box.

The schematic diagram of the transistor characterization setup shown in Figure 3.5 is relevant to Chapter 4 and 5. For environmental testing, measurements were conducted in the dark inside an artificial climate chamber (CLIMACELL) to control the humidities (20% ≥ RH ≤ 80%) and temperatures (10 ºC ≥ T ≤ 90 ºC). The test device was placed inside the box without a lid and was held at the set conditions for 30 min to allow the device to come into equilibrium

with the test environment. For the bias stress tests under controlled conditions (humidity and temperature), measurements were conducted inside the CLIMACELL while others were conducted at room temperature in ambient air. Both measurements were conducted in the dark. Thus for the ambient environment, the tested device was placed inside the box with a lid.

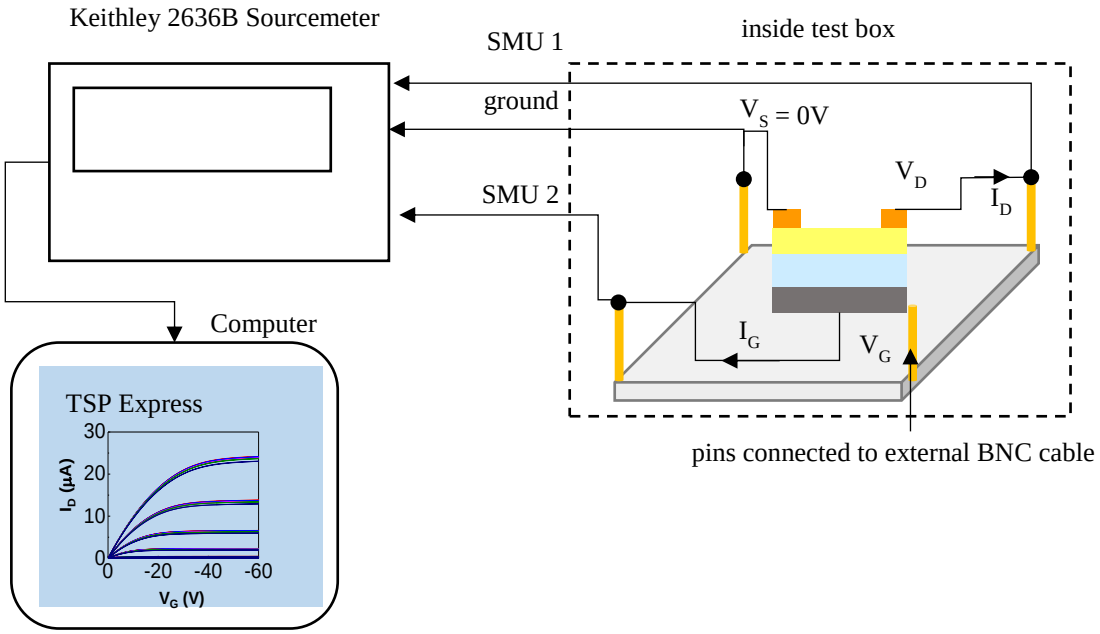

Figure 3.5 Schematic diagram of the transistor characterization setup. Test pins were connected to BNC connector to allow connection to the SMU unit

3.5 Bias Stress Characterization

The bias stress characterization procedure described here is relevant for the studies in Chapter 5. A typical flow diagram for the bias stress experiments is shown in Figure 3.6(a). First, the initial transfer characteristic was measured. Then the device was subjected to various bias stress conditions and stress times. The bias stress was frequently interrupted to measure the output characteristics and transfer characteristics in the linear (V_D = -1 V) and saturation (V_D = -60 V) regimes from which the electrical parameters were extracted. Figure 3.6(b) indicates a typical transfer curve, plotted on linear and semilog scales, both in the initial state and after bias stress. The shift of threshold voltage, ΔV_T, and turn-on voltage, ΔV_{ON}, were determined

as [V_T (t) – V_T (0)] and [V_{ON} *(t)* – V_{ON} *(0)*] respectively, where *t*=0 corresponds to pre-stress values.

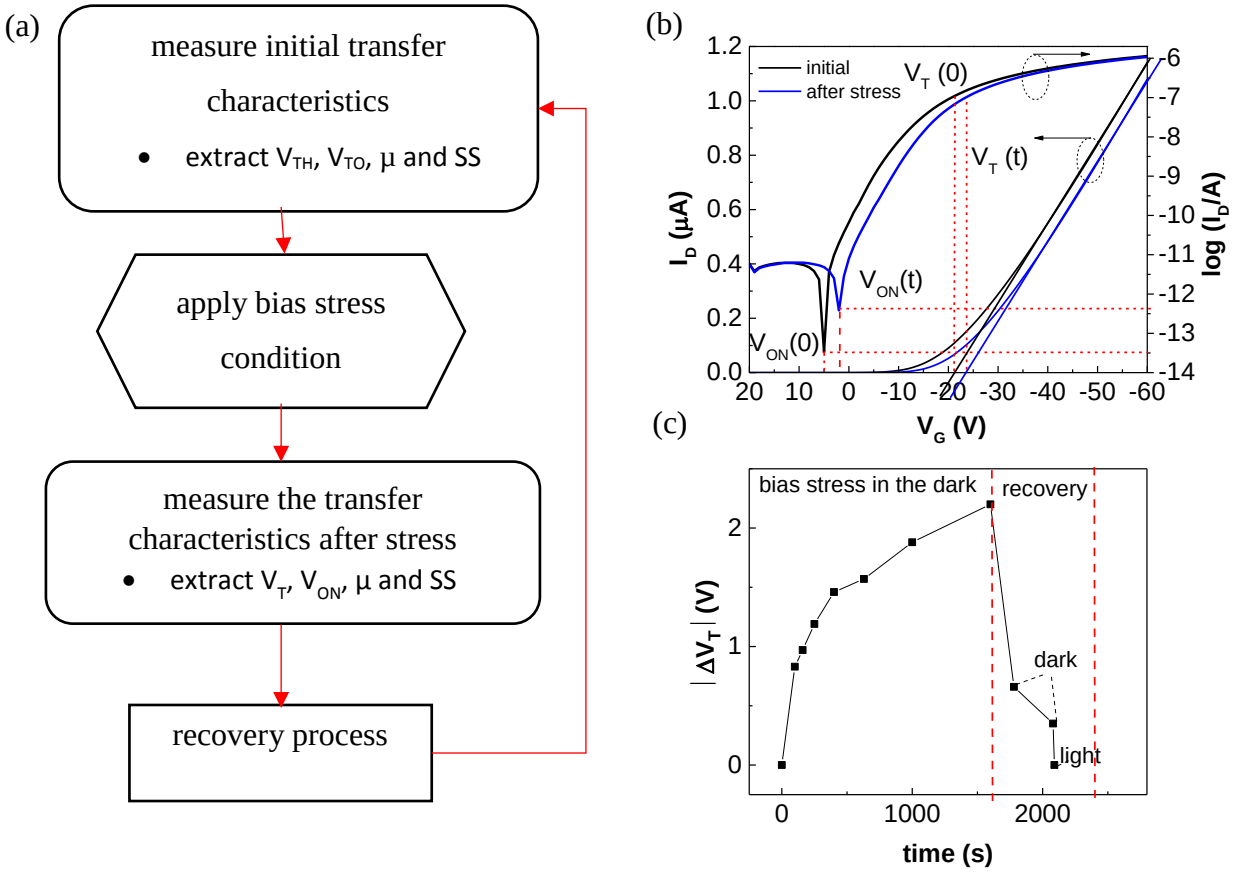

Figure 3.6 (a) flow diagram of a typical bias stress experiment. (b) Illustration of threshold voltage shift, ΔV_T, and turn-on voltage shift, ΔV_{ON} calculated as *[V_T (t) – V_T (0)]* and *[V_{ON} (t) – V_{ON} (0)]* respectively, where t=0 corresponds to pre-stress values. (c) Time-dependence of ΔV_T under stress and while recovering.

After completing a negative bias stress test, devices were subjected to a recovery procedure. The devices were left short-circuited in the dark for a few minutes and also under ambient light for a few seconds until V_{ON} and V_T recovered to their original values. The recovery was interrupted at fixed times to record the transfer characteristics of the transistor with a drain bias of $V_D = -1$ V by sweeping the gate bias from 20 to -60 V. Changes, ΔV_T, in the threshold voltage over time both under stress and while recovering is shown in Figure 3.6(c). It is seen, that the recovery of $\Delta V_{ON}/\Delta V_T$ was not complete even after 5 minutes relaxation in the dark.

However, with ambient light exposure for a few seconds, $\Delta V_{ON}/\Delta V_T$ fell to zero. Therefore, recovery by light exposure with source and drain terminals grounded ($V_D = V_G = 0$ V) became the usual procedure for resetting under negative bias stress. For positive bias stress, the recovery process was achieved by applying a negative gate bias [97]. This procedure removed the V_{ON}/V_T shifts and allowed the electrical characteristics of the device to return to their original state before proceeding with the next measurement.

3.6 Phototransistor Measurement

The characterization procedure described here is relevant for the studies in Chapter 6 and 7. The schematic diagram of the transistor characterization setup in the cryostat is shown in Figure 3.7(a). Only OTFT with L=150 µm and W= 2mm were used in this work. All electrical characterizations were conducted under atmospheric ambient and room temperature conditions. The illumination source was a xenon discharge lamp coupled to a monochromator (Jobin Yvon Triax 320) covering the range 400–700 nm. The test device was placed in the sample holder in a cryostat. Monochromatic light was transmitted into the cryostat through a quartz window and illuminated the top the device (Figure. 3.7(b)). The power of the light incident on the device was controlled by adjusting the exit slit and measured using a sensor (Anritsu model MA9411A1) at the device position.

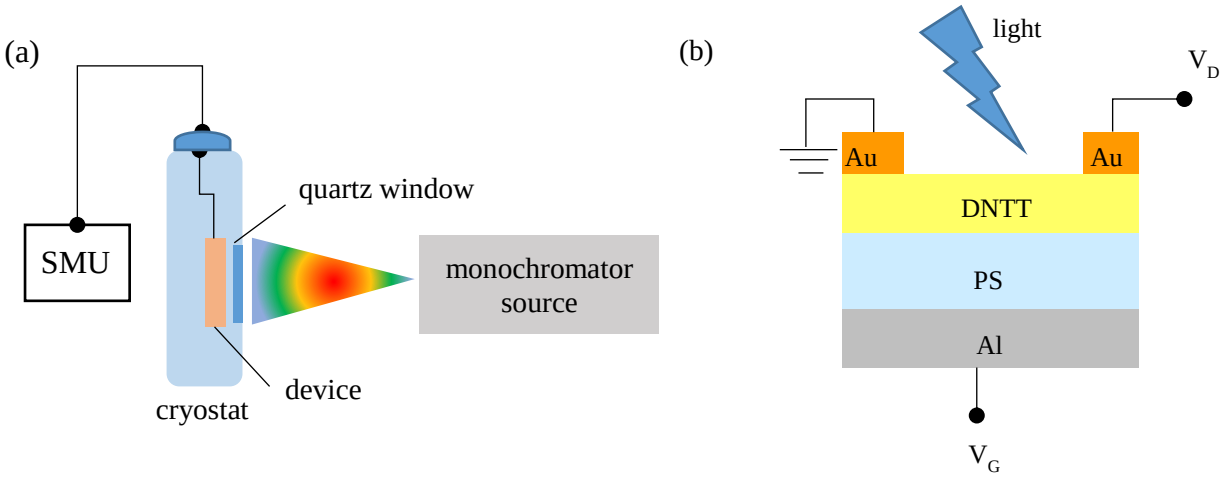

Figure 3.7 (a) Schematic diagram of the phototransistor measurement setup and (b) cross-section of a PS-DNTT device structure under illumination through the top of the DNTT film.

Following each measurement, the device was allowed to recover before subsequent measurements. This is done by exposing the device to the ambient light for few seconds if the V_{ON}/V_T shifts negatively. If V_{ON}/V_T had shifted positively due to electron trapping, the recovery of V_{ON}/V_T was achieved by applying negative gate bias. This drives the device into accumulation and has been shown [97] to be a way of removing/neutralizing electrons trapped at the device interface.

A typical flow diagram for the bias stress under illumination experiments is shown in Figure 3.8. First, the initial transfer characteristic was measured. Then the device was subjected to various bias stress and light conditions. After that, the transfer characteristic was measured again at V_D = -1 V from which the electrical parameters were extracted. Finally, the device was allowed to recover the original transfer curve following the same methods as described above before undertaking subsequent measurements.

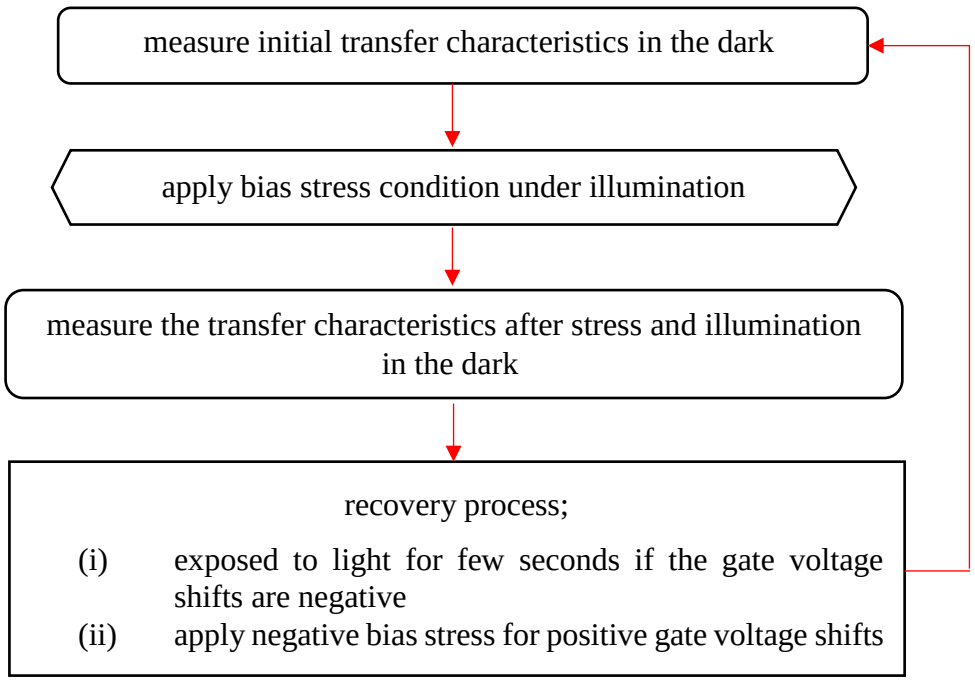

Figure 3.8 Flow diagram of a bias stress under illumination experiment

3.7 Summary

The procedure for fabrication of the PS-DNTT OTFTs using the equipment described above is an established approach for fabricating OTFTs. The transistor characteristics were obtained using two different setups. For the environmental and some of the bias stress measurements, the test device was attached to the sample holder in the test box. The test box was then placed inside the CLIMACELL cabinet to control humidities and temperatures. For the phototransistor measurements, the test device was placed in a sample holder that is mounted inside the cryostat parallel to the quartz window. This allowed monochromatic light to be transmitted into the cryostat through the quartz window to illuminate the top the device. Using the procedures described in this chapter, considerable insight is achieved into the role on the semiconductor/insulator interface in determining the extent of environmental, bias and light-induced instability in organic OTFTs.

4 Environmental Stability in PS-DNTT Thin Films Transistors: The DoS Investigation

4.1 Introduction

In this chapter, the effect of moistures and elevated temperatures on the PS-DNTT OTFTs are presented. The device performance was analyzed with a relative humidity (RH) that was gradually increased from 20% to 80% and temperatures from 20 ºC to 90 ºC. The density of state (DoS) in DNTT environmental was extracted using the Grünewald model in order to distinguish the presence of the traps either in the bulk semiconductor, bulk dielectric or at interface between semiconductor and dielectric.

4.2 Humidity Effect on Electrical Performance

Figures 4.1(a) and 4.1(b) show the output and transfer characteristics with increasing RH. The output characteristics (Figure 4.1(a)) obtained for both the forward (0 to -60 V) and reverse sweeps (-60 to 0 V) of drain voltage, V_D exhibit good linear and saturation regimes with negligible hysteresis at any RH. Moreover, the drain current, I_D was found to reduce ~16% as RH increases from 20% to 80% which was caused by the shift in the turn-on voltage, V_{ON}, and threshold-voltage, V_T, to more negative values [46] as shown in the transfer characteristics of Figure 4.1(b). The transfer characteristics (Figure 4.1(b)) obtained for both the forward (20 to -60 V) and reverse sweeps (-60 to 20 V) of gate voltage, V_G, exhibit minimal hysteresis. Moreover, the off-current, I_{off}, was found to increase significantly above 70% RH due to parasitic currents through water films on the device surface and/or increased gate leakage current. At lower RH the off-currents were determined by the displacement current of a few pA charging the gate capacitance.

The carrier mobility, μ, V_{ON}, V_T, subthreshold slope, SS, and on-off ratio, I_{ON}/I_{OFF} extracted from the transfer plot are given in Table 4.1 for the different values of RH. The carrier mobility is calculated from the slope of the transfer plot using equation (2.11) and measured C_i=2.37 nF/cm^2. It can be seen that the mobility reduced from 0.95 to 0.94 cm^2/Vs as RH increases to 80%. I_{ON}/I_{OFF} reduced at higher humidity due to increasing I_{OFF} at higher

humidity. *SS* slightly increase from 3.67 to 4.09 V/decade with increasing RH. It is also worth noting that the SS values are relatively high compared to previously reported for DNTT [101]. This is mainly the consequence of the relatively thick, and hence low C_i, gate dielectric used in our OTFTs. Simple scaling to the much thinner C_{14}-phosphonic acid treated AlO_x (C_i = 800 nF/cm^2) used by Zschieschang et al [101] in their DNTT transistors would result in an SS ~10 mV/decade which compares with 90 mV/decade reported by these authors.

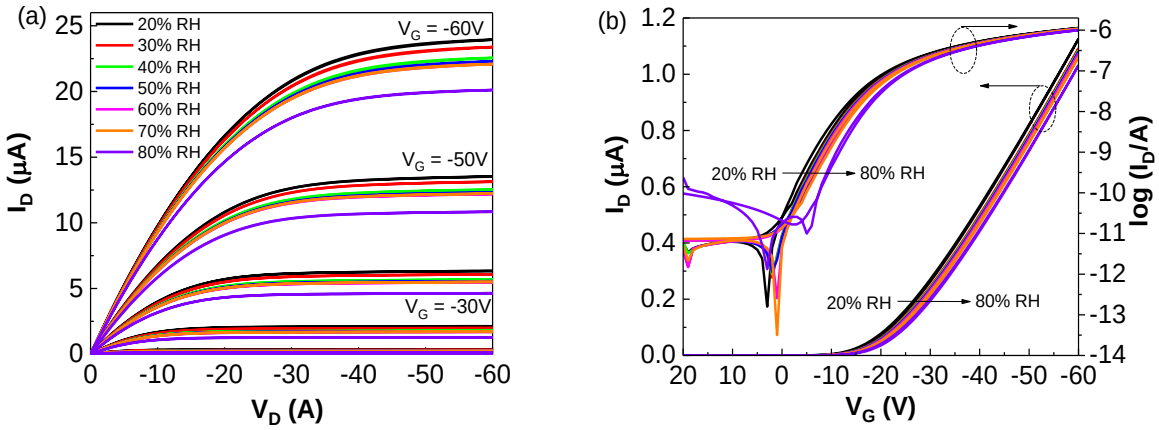

Figure 4.1 Effect of increasing relative humidity at 20 ^oC on (a) output and (b) transfer characteristics of a DNTT OTFT with polystyrene gate insulator. The transfer plots were obtained in the linear regime with drain voltage, V_D = -1 V.

The output and transfer characteristics obtained for forward and reverse sweeps with decreasing RH from 80% to 20% are shown in Figures 4.2(a) and 4.2(b). When RH was reduced back to 20% in stages over a period of 3 hours, only partial recovery occurred. The extracted parameter values for decreasing RH, are given in Table 4.1 in brackets. It can be seen that the mobility remain unchanged at 0.94 cm^2/Vs as RH decreases to 20% while the shifts in V_{ON} and V_T were much longer-term. The transfer plots show a translation of around 2.5 V along the V_G axis while maintaining the same profile. This is consistent with a shift, ΔV_{FB}, in the flatband voltage arising from hole trapping in the PS film or at the PS-DNTT interface. For an effective interface trapped charge density Q_{it}, which includes also the influence of charges in the insulator, $\Delta V_{FB} = -Q_{it}/C_i$. Thus a -2.5 V shift in the post-RH exposure transfer plots corresponds to an effective hole density of ~3.7 x 10^{10} cm^{-2} trapped in water-related states. Interestingly, the subthreshold slope improved slightly, but this is

likely to be related to the higher on-off ratios resulting from lower leakage currents as RH is reduced.

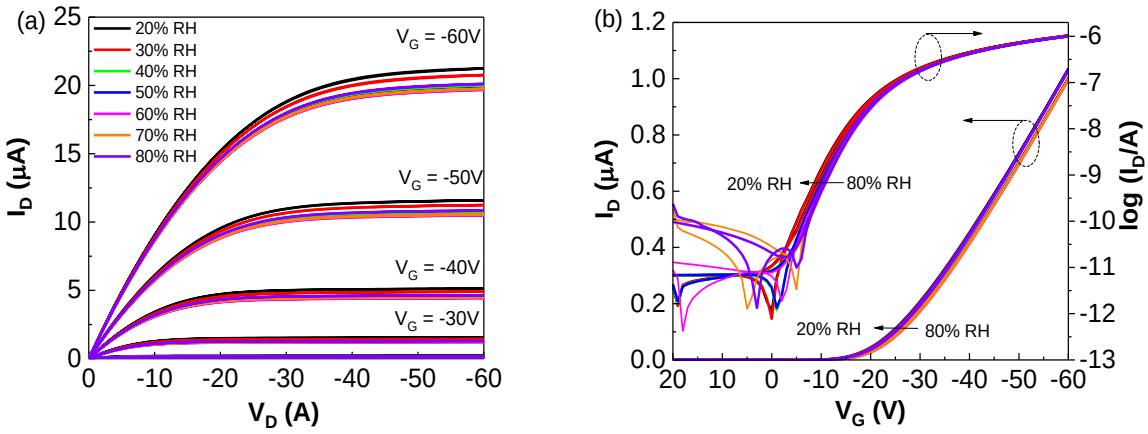

Figure 4.2 Effect of decreasing relative humidity on (a) output and (b) transfer characteristics. The transfer plots were obtained in the linear regime with drain voltage, V_D = -1V

Table 4.1 Device parameters extracted from the transfer characteristics measured in the forward voltage sweep with V_D = -1V, T = 20°C and RH increasing from 20% to 80%. The values in brackets are for decreasing RH.

RH	20%	30%	40%	50%	60%	70%	80%
***μ* (cm²/V.s)**	0.95 (0.94)	0.95 (0.93)	0.95 (0.93)	0.95 (0.93)	0.94 (0.93)	0. 94 (0.93)	0. 94 (0.94)
***V*$_{ON}$ (V)**	3 (0)	2 (0)	2 (-1)	2 (-1)	1 (-2)	1 (-5)	-6 (-6)
***V*$_T$ (V)**	-22 (-24)	-23 (-24)	-23 (-25)	-24 (-25)	-24 (-25)	-24 (-25)	-26 (-25)
***I*$_{ON}$/*I*$_{OFF}$**	1.8×10^5 (1.6×10^5)	1.7×10^5 (1.6×10^6)	1.7×10^5 (1.6×10^5)	1.7×10^5 (1.6×10^5)	1.7×10^5 (1.7×10^5)	1.6×10^5 (5.8×10^4)	1.5×10^4 (1.6×10^4)
SS (V/decade)	3.67 (3.56)	3.71 (3.65)	3.75 (3.71)	3.83 (3.72)	3.85 (3.84)	3.92 (3.91)	4.09 (3.90)

Figure 4.3(a) and (b) show the gate-voltage dependence of the mobility for increasing and decreasing RH respectively. It can be observed clearly that the rate of mobility increase and the maximum μ_{lin}, show only slight reductions with increasing RH (Figure 4.3(a). Furthermore, there is no significant change observed in the transfer characteristics. Therefore

the main effect of increasing RH is attributed to hole trapping at water-related defects at the PS-DNTT interface or in the bulk PS and are unlikely to contribute to the semiconductor DoS.

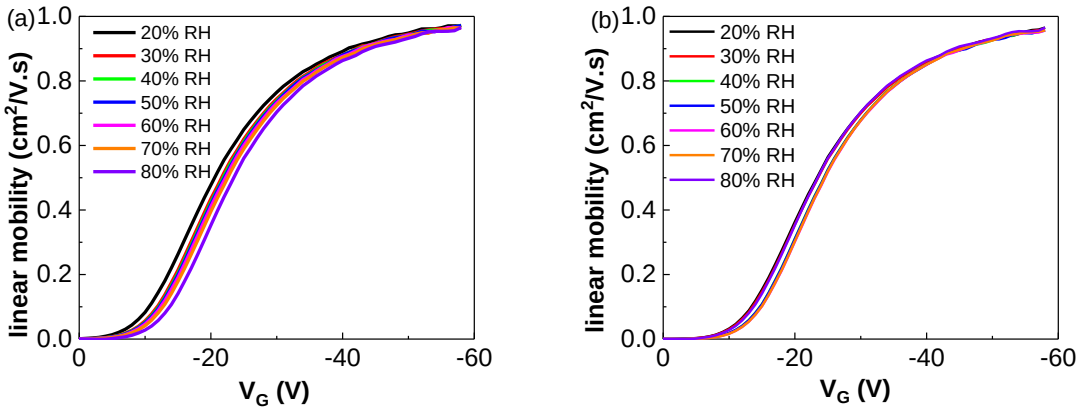

Figure 4.3 Gate-voltage-dependent mobility extracted by applying equation (2.11) to transfer characteristics obtained in the linear regime with (a) increasing RH and (b) decreasing RH.

4.3 Temperature Effect on Electrical Performance

The output and transfer characteristics with increasing temperature from 20 ºC to 90 ºC are shown in Figures 4.4(a) and 4.4(b). There is no hysteresis observed in the output characteristics (Figure 4.4(a)). It also can be observed from the transfer characteristics in Figure 4.4(b) that the drain current decreases at higher temperatures as a consequence of V_{ON} and V_T shifting to more negative values. The dashed lines in both figures show the recovery plot after the devices was left overnight at 20ºC and 10% RH. As can be seen from the transfer plot, very little recovery occurred.

Device parameters extracted from the transfer plots in Figure 4.4(b) are given in Table 4.2. The carrier mobility was calculated from the slope of the transfer plot using equation (2.11) and measured C_i=2.57 nF/cm^2. It can be seen that the maximum mobility slightly increased from 1.00 to 1.25 cm^2/Vs as temperature increased up to 90ºC. Both V_{ON} and V_T increase to more negative values while *SS* increases from 4.19 to 4.62 V/decade with increasing temperature. I_{ON}/I_{OFF} remain ~10^5 at all temperatures. After the device had relaxed overnight at 20ºC and RH=10%, *SS* reduced slightly below its initial value. On the other hand, the

maximum mobility reduced back to 1.10 cm^2/Vs which is slightly higher than measured initially. This is believed to be related to the higher mobility that occurred at ~90°C, which may be the result of morphological changes induced in the DNTT by increased molecular motion in the polystyrene (T_g ~100°C).

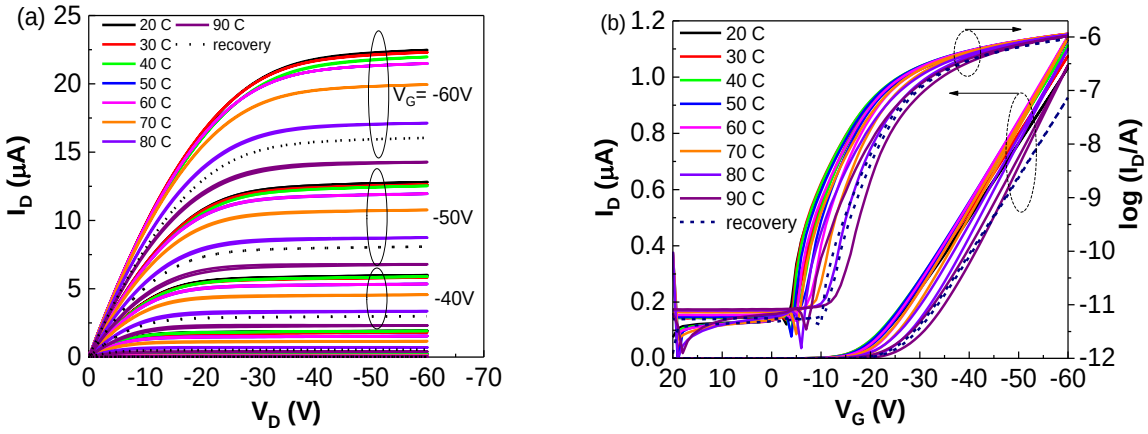

Figure 4.4 Effect of increasing temperature at RH = 10% on (a) output and (b) transfer (V_D = -1 V) characteristics of a DNTT OTFT with polystyrene gate insulator. The dashed plots were obtained after holding the device at 20 °C and 10% RH overnight.

Table 4.2 Device parameters extracted from the transfer characteristics in Figure 4.4(b) obtained during the forward voltage sweep with temperature increasing from 20°C to 90°C, RH = 10% and V_D = -1V. Values in the final column were obtained subsequently at 20°C after holding the device overnight at 20°C and 10% RH.

T (°C)	20	30	40	50	60	70	80	90	20
μ (cm^2/V.s)	1.00	1.07	1.10	1.13	1.16	1.19	1.22	1.25	1.10
V_{ON} (V)	-3	-3	-4	-4	-5	-5	-6	-7	-10
V_T (V)	-18	-20	-21	-21	-21	-23	-24	-27	-27
I_{ON}/I_{OFF} (x10 ^{5})	2.18	2.33	2.38	2.47	2.50	2.33	2.03	1.65	2.00
SS (V/decade)	4.19	4.10	4.15	4.22	4.41	4.37	4.40	4.62	3.53

The gate-voltage dependence of the mobility obtained at different temperatures are shown in Figure 4.5(a). It can be seen that the plots are shifted to more negative values consistent with

the shift in flatband voltage. At the highest gate voltages, the mobility saturates at values consistent with those given in Table 4.2. A plot of *log* μ as a function of $T^{-1/3}$ is shown in Figure 4.5(b) for the different temperatures. It can be seen that the temperature dependence fits the model for hopping conduction in a 2-dimensional sheet [23] given by $\mu = \mu_0 \exp -(T_0 / T)^{1/3}$ with T_0 = 288 K.

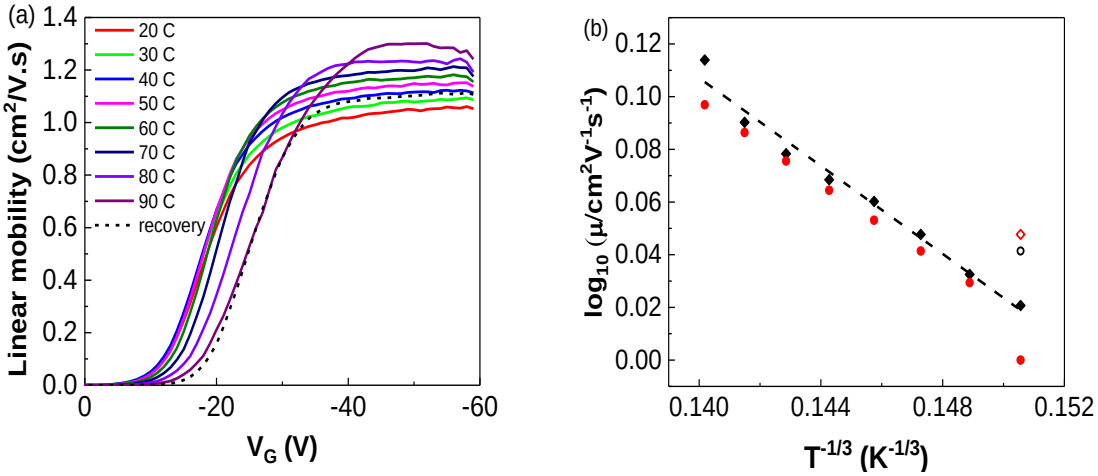

Figure 4.5 (a) Gate-voltage-dependent mobility obtained at different temperatures during the forward voltage sweep (20 V to -60 V) together with the dotted post-heating plot at 20°C. (b) Temperature dependence of the mobility from Table 4.2 (red dots) and values corresponding to V_G = -50V in figure 4.5(a) (black diamonds). The open data points were obtained at 20°C post-heating.

4.4 Environmental Effects on Density of States (DoS)

In the previous section, it was suggested that the main effect of RH and *T* is simply to cause a shift, ΔV_{FB}, in the flatband voltage arising from hole trapping in the PS film or at the PS-DNTT interface. To confirm this, the DoS of the semiconductor was extracted to identify any evidence of charge trapping within the DNTT band gap. The DoS spectrum of DNTT was extracted from the transfer characteristics by applying the Grünewald method [32] as outlined in Chapter 2, section 2.6.4 and Appendices A and B.

Firstly, the relationship between the gate-dependent insulator/semiconductor interface potential, V_0, and the effective forward voltage, $V_F = (V_G - V_{ON})$ was obtained from equation

(2.16) and plotted as shown in Figures 4.6(a) and 4.6(b). It can be observed that as RH increases (Figure 4.6(a)), plots of V_0 rise slower with V_F. Unlike for the RH case, V_0 rises more rapidly with increasing temperature as shown in Figure 4.6(b). Then the DoS, $N(E)$ can be obtained with equations (2.17) and (2.18) and plotted as a function of energy relative to the Fermi level, E_F, $(V_0 = E - E_F)$ as shown in Figure 4.7(a) for different RH and in Figure 4.8(a) for different temperatures.

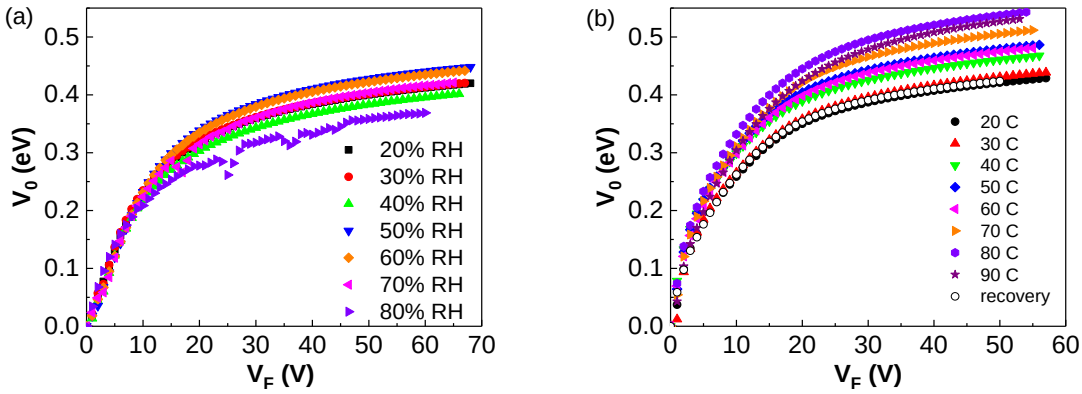

Figure 4.6 Plots of V_0 versus V_F showing the effect of (a) relative humidity and (b) temperature.

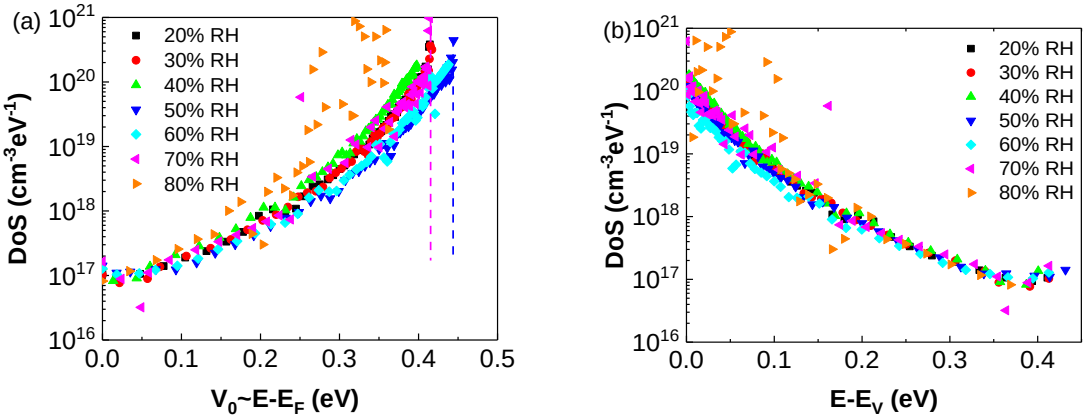

Figure 4.7 Density of states for different values of RH plotted relative to (a) V_0 ($=E-E_F$) and (b) the mobility edge assumed to coincide with ~E_V.

Ideally, the DoS should be plotted relative to the valence band edge, E_V. Kalb and Battlogg [31]simply assume a value for (E_F-E_V) e.g. ~0.5 eV in pentacene. On the hand, some authors

assumed that a sharp rise observed in the DoS at high V_0 as a band edge [34, 35]. However, in our case, we assume that when the effective mobility becomes constant at ~1 cm^2/Vs (Appendix A), this coincides with a transport band edge (Appendix B) or E_V in the case of a p-type semiconductor [30, 102]. Upon evaluating the relevant energy, the DoS may be replotted as a function of (E-E_V) as shown in Figures 4.7(b) and 4.8(b). It can be observed in Figure 4.7(b) that the effect of RH on the DoS is minimal with the plots obtained for all relative humidities coalescing to a single curve over most of the range. Figure 4.8(b) shows the DoS for different temperatures. Similar profiles as RH were also observed but with a slight increase in deeper states at higher temperatures which eventually mask the weak feature lying between ~0.25 and ~0.35 eV above E_V. Similar feature with a peak ~10^{19} $cm^{-3}eV^{-1}$ was also observed in pentacene within the energy range (~0.28 eV) due to oxygen-related defects [103]. However, this peak is significantly higher than observed in our case ~2 x 10^{17} $cm^{-3}eV^{-1}$ [30, 103]. Even though the oxidation of sulphur atoms in DNTT to disulphones is possible, this requires exposure to strong oxidizing agents. Diemer et al [36] reported that the presence of isomers in 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES ADT) lead to strong peaks in the DoS at ~0.4 eV above the valence band. However, this was not possible in the molecular structure of DNTT. Moreover, in later cases (Chapter 5, 6 and 7), the density of states exhibits similar behavior. As there is no change in the hole mobility, the weak features appearing at the deeper states are unlikely to be associated with DNTT itself but rather due to a changing flat-band voltage when electron/hole occupancy of interface states changes as the device turns on.

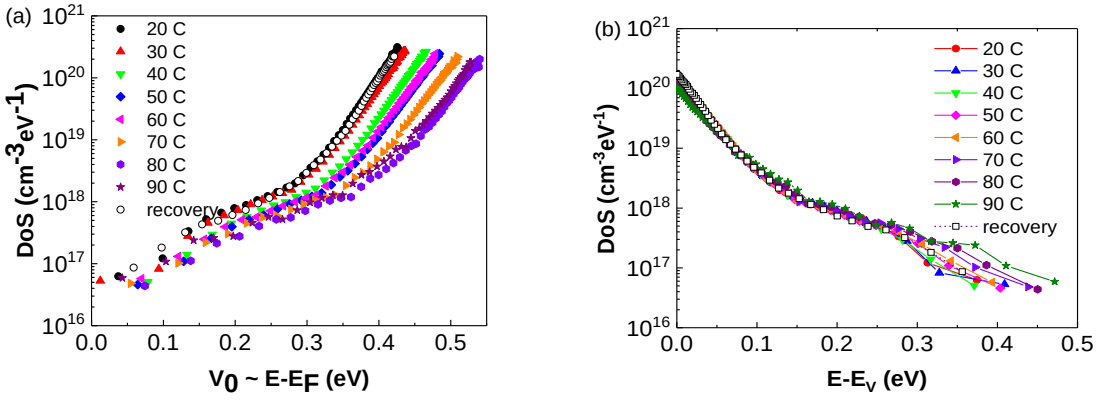

Figure 4.8 Density of states for different values of temperature plotted relative to (a) V_0 *(=*E-E_F) and (b) the mobility edge assumed to coincide with E_V.

In Figure 4.9, the DoS obtained here is compared with those obtained (a) by applying the Oberhoff computer model to single-crystal DNTT transistor characteristics [104], and (b) from Scanning Kelvin Probe Microscopy (SKPM) [105] on evaporated thin films of DNTT incorporated into transistor structures. The computer generated DoS profile showed a rapid decrease in state density from 10^{22} $cm^{-3}eV^{-1}$ to a plateau at ~10^{17} $cm^{-3}eV^{-1}$. A similar feature was observed from SKPM measurements on DNTT films evaporated onto SAM surface modified AlO_x. However, the profile extended by ~60 meV to deeper states [105]. In the present case, the DoS shows a more gradual decrease from ~10^{20} $cm^{-3}eV^{-1}$ but asymptoting to the same concentration (~10^{17} $cm^{-3}eV^{-1}$) of deeper states. It was reported that the density of states obtained for evaporated pentacene films decreases to ~10^{18} $cm^{-3}eV^{-1}$ [31, 105, 106]. This indicates that the DoS in pentacene was higher than in our evaporated DNTT films over a similar energy range.

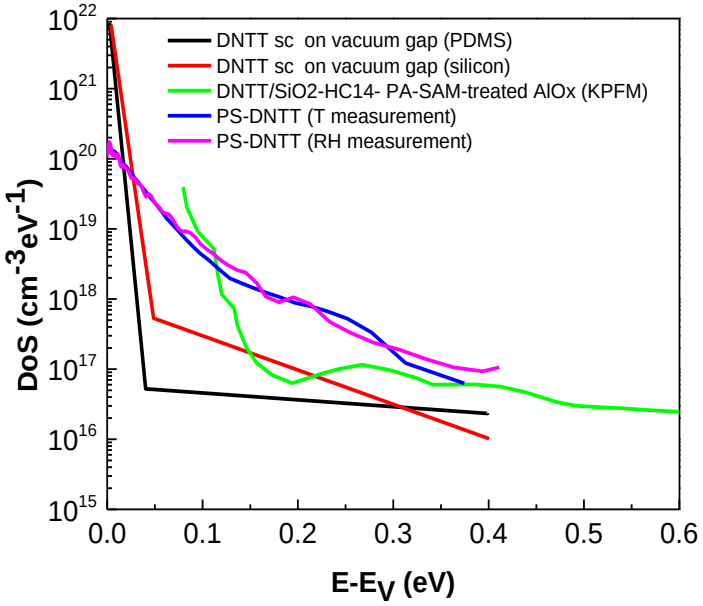

Figure 4.9 Comparison of DoS spectra obtained in the present work using the Grünewald et al model with those obtained by applying the Oberhoff et al model to single-crystal DNTT [104] and from evaporated films using Scanning Kelvin Probe Microscopy [105].

4.5 Summary

The effect of relative humidity in the range 20 – 80% on DNTT-PS OTFT was investigated. It was observed that I_{off} increases significantly above 70% RH due to parasitic currents through water films on the device surface. Both V_{ON} and V_T shifted negatively as RH% increased due to hole trapping within the PS gate dielectric. However, only partial recovery occurred when RH was reduced back to 20%. The effect of temperature in the range 20 ºC – 90 ºC was also investigated. The shifts in V_{ON}, V_T observed with increasing temperature are similar to the changes caused by increasing RH. However, the mobility increased slightly from 1.00 to 1.25 cm^2/Vs and fits the model for hopping conduction in a 2-dimensional sheet with T_0 = 288 K. The density of states spectra with respect to different RH and temperature were extracted from transfer characteristics obtained in the linear regime using the Grünewald model [32]. It was observed that the changes in DoS were minimal to the relative humidity range 20 – 90%. The DoS for different temperatures showed a similar profile as in RH. However, a slight increase was observed in the deeper states as temperature increases. These results confirm that the device instability observed is ascribed almost entirely to flatband voltage shifts caused by hole trapping in the polystyrene dielectric or its interface with DNTT.

5 Effect of Bias Stress on PS-DNTT Thin Film Transistor Stability

5.1 Introduction

In this chapter, the bias stress effect in PS-DNTT OTFTs is reported, with a particular focus on the device characteristics when voltages are applied in combination with other sources of instability. The results are grouped and discussed as follows.

i. A study of the operational stability of OTFTs under negative bias stress. Here the variation of the threshold voltage is monitored over time, after applying to the devices a constant negative voltage on the gate and drain contacts.
ii. A study of the effect of relative humidity on the bias stress instability.
iii. A study of the effect of temperature on the bias stress instability.
iv. A study of the effect of positive bias stress on the operational stability of OTFTs.

5.2 Negative bias stress instability in PS-DNTT TFTs

5.2.1 Gate Bias Stress

The bias stress effect in PS-DNTT TFT was investigated with two sets of stress conditions. In the first, V_D = 0 V and various negative gate-source voltages (V_G = -5, -10, -20, -30 and -40 V) were applied. In the second stress condition, V_D was set equal to V_G and ranged from -5 to -40 V. Both stress conditions were applied for 1600 s in the dark under ambient conditions typically T= (15 ºC-20 ºC) and RH= (40%-70%). Figures 5.1(a) and 5.1(b) show the output characteristics recorded before and after negative bias stress with different V_G. Clear linear and saturation behaviors were observed at lower and higher V_D respectively. There was negligible hysteresis observed between forward and reverse scans at any stress condition. However, the magnitude of I_D slightly decreased after the 1600 s stress, with the greatest reduction observed when stressing at V_D = 0 V, V_G = -40 V.

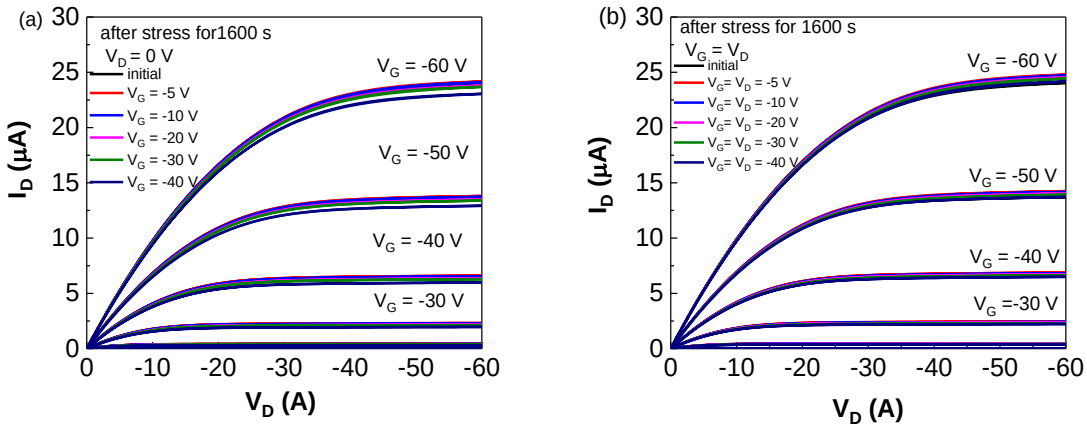

Figure 5.1 Output characteristics in forward and reverse sweeps obtained following bias stress with (a) V_D = 0 V and V_G = -5, -10, -20, -30 and -40 V, and (b) $V_G = V_D$ ranging from -5 to -40 V. In all cases the stress time was applied for 1600 s.

Figures 5.2(a) and 5.2(b) indicate the evolution of the transfer characteristics of the same device measured in the linear regime (V_D= -1 V) obtained during a forward V_G sweep (+20 V to -60 V) before and after stress. As can be seen, the negative gate bias stress for both stress conditions, causes the transfer curves to shift to more negative voltages without a significant variation of the shape. Such a phenomenon is associated with hole trapping at the interface or in the bulk dielectric layer and related to the shift in the flat-band voltage, ΔV_{FB}. Therefore, the interface trapped charge density, N_{it} can be estimated using equation (2.14) in Chapter 2.

The dependence of ΔV_T and ΔV_{ON} on V_G applied while stressing are shown in Figures 5.3(a) and 5.3(b) respectively. Both stress conditions ($V_G = V_D$ and V_D = 0 V) show a more pronounced negative shift at higher values of V_G. This effect occurs as a result of a higher density of holes induced in the channel at higher gate-source voltages. This in turn leads to an increase in the number of holes trapped in the interface states [69, 83]. Therefore, as seen in Figure 5.3(b), the corresponding increase in the density of trapped holes, ΔN_{it}, is between 6.0 x 10^{10} cm^{-2} and 7.5 x 10^{10} cm^{-2} as V_G increases to -40 V depending on the value of V_D.

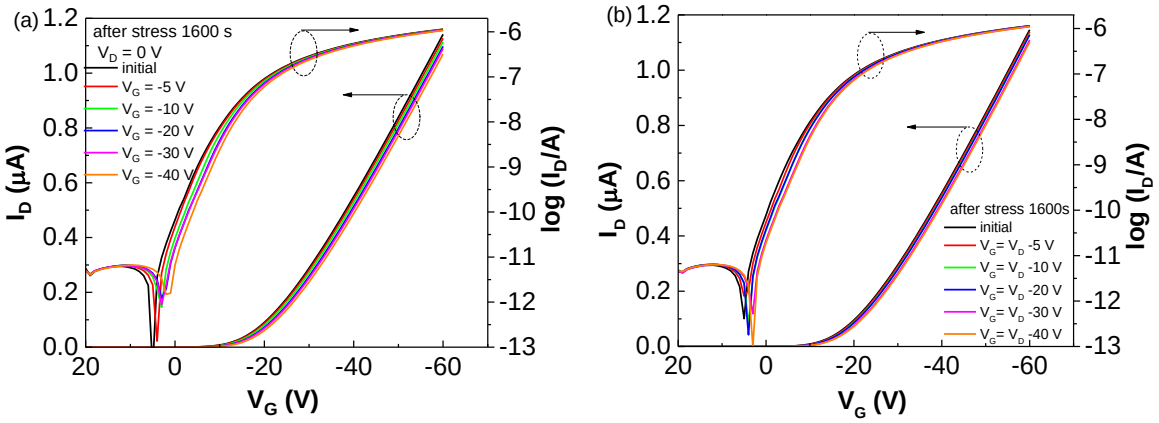

Figure 5.2 Influence of gate bias stress on transfer characteristics obtained at V_D = -1 V with (a) zero drain-source voltage (V_D = 0 V) and various gate-source voltages (V_G = -5, -10, -20, -30 and -40 V) and (b) drain-source voltage equal to gate-source voltage (V_G = V_D) which ranging from -5 to -40 V for 1600 s in ambient air.

When V_D = 0 V, both ΔV_T and ΔV_{ON} increase rapidly whereas under simultaneous gate-source and drain-source bias (V_G = V_D), slower changes are seen in ΔV_T and ΔV_{ON}. This can be explained as follows. By applying a negative gate bias stress V_G to the gate electrode, and V_D = 0 V, holes accumulate uniformly at the insulator/semiconductor interface forming a channel that will provide a conduction path between source and drain electrodes [Figure 5.3(c)]. When V_G = V_D, the potential difference between the gate and drain electrode is zero, which weakens the electric field near the drain contact and in turn, reduces the number of charge carriers towards the drain end of the channel as illustrated in Figure 5.3(d). Therefore the number of charge carriers available for trapping are greater when stressing at V_D = 0 V compared with stressing at V_G = V_D, which leads to a reduction in ΔV_T and ΔV_{ON} as suggested by Zschieschang et al [82] and Zan and Kao [83].

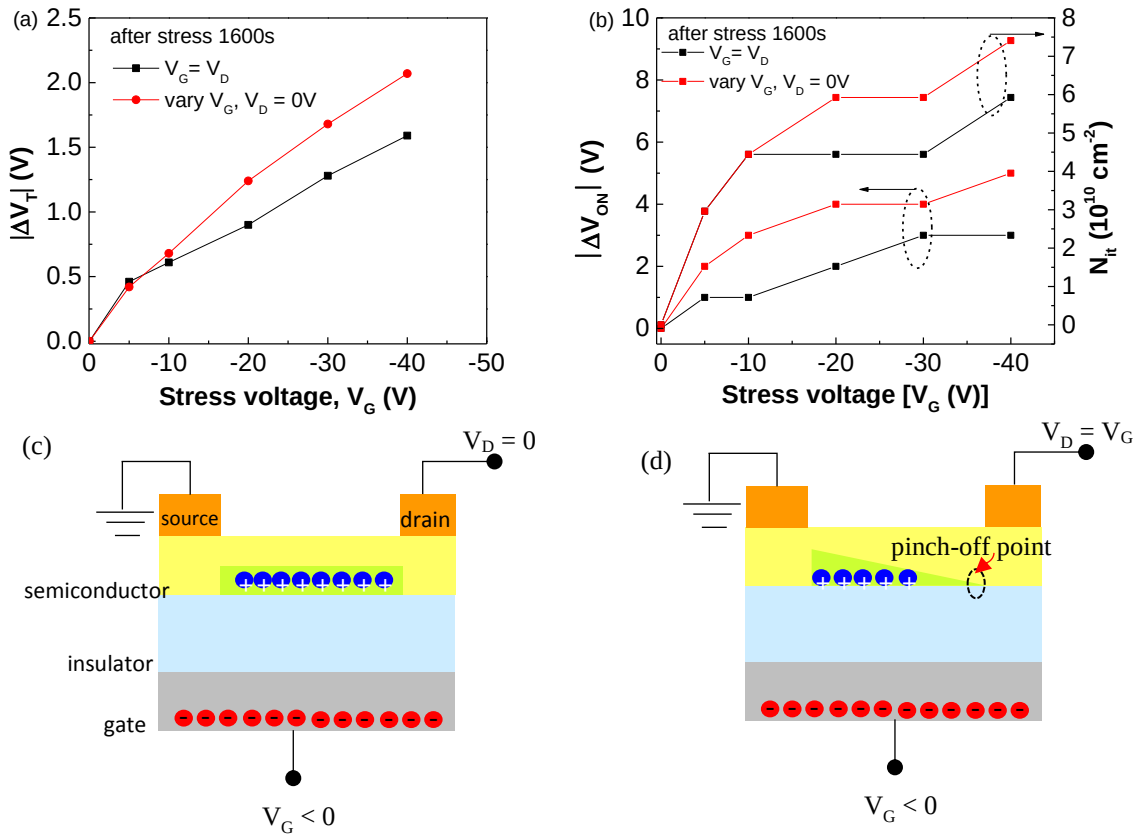

Figure 5.3 (a) Shift of threshold voltage, ΔV_T and (b) shift in turn-on voltage, ΔV_{ON} and corresponding N_{it} after 1600 s stress. Illustration in (c) shows that by applying a negative gate voltage, V_G between the gate electrode and the grounded source electrode, V_D = 0 V, charge carriers accumulated uniformly along the insulator-semiconductor interface. (d) When V_D = V_G the channel is pinched-off which results in a reduction of charge density at the drain end of the channel.

The gate-voltage-dependent mobility was also extracted from the local slope of the transfer characteristics. Figure 5.4(a) and 5.5(b) clearly show that, the curves move in parallel and the maximum mobility before and after bias stress is unchanged. Furthermore, there is no significant change, $\Delta\mu$ in in the maximum mobility, when plotted as a function of gate-source bias stress (see inset of Figure 5.4(a) and 5.4(b)). These results confirm that trap states in the semiconductor play a negligible role in the bias stress effect. Therefore, ΔV_T, caused by the negative gate-bias stress can be attributed to an increase in holes trapped within the PS gate dielectric, or at the DNTT/PS interface.

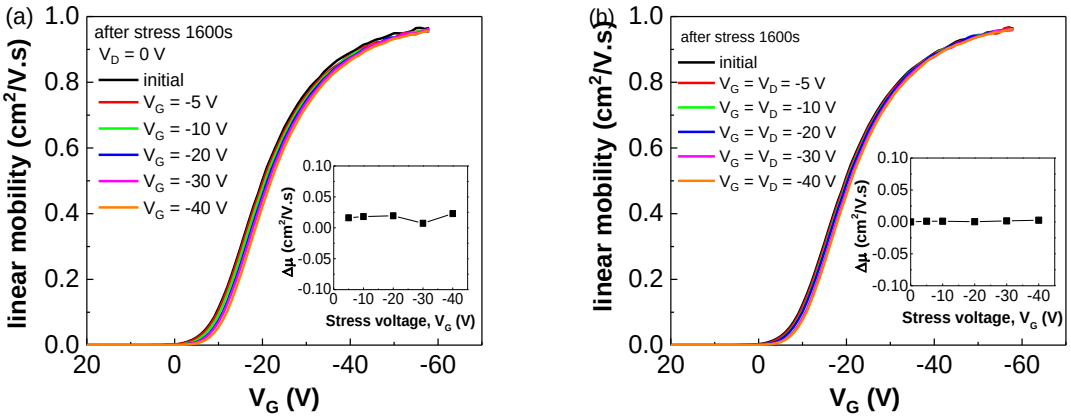

Figure 5.4 Linear mobility as a function of gate bias after stress conditions, corresponding to (a) V_D = 0 V with V_G = -5, -10, -20, -30 and -40 V and (b) V_G = V_D ranging from -5 to -40 V.

The proposed mechanism for charge trapping at the PS-DNTT interface is illustrated in Figure 5.5. At zero gate voltage, there is no band bending occur as shown in Figure 5.5(a). At low V_G, valence band, E_V bend upwards and slowly lowering fermi level, E_F at semiconductor/insulator interface inducing a low concentration of holes leading to low interface trapping as shown in Figure 5.5(b). As V_G increases, band bending increases, effectively lowering E_F, at the interface. Consequently large a high concentration of the holes above E_F are induced at PS-DNTT interface which in turn causes high interface trapping with some trapped in the bulk insulator (Figure 5.5(c)).

Even though N_{it} provides a useful comparison, it only gives information on the occupied interface trap density, rather than any details of the DoS distribution within the band gap. The mobility plot in Figure 5.4 suggests that DNTT itself is insensitive to bias stress. To confirm this the DoS of the semiconductor was extracted for each bias stress condition by applying the Grünewald model to transfer plots obtained within the linear regime [107].

Figures 5.6(a) and 5.6(b) show the DoS distribution plotted as a function of E-E_V. It can be observed that the effect of bias stress is minimal with the plots obtained before and after bias stress coalescing to a single curve with a weak feature superimposed at deeper energies. Under all bias stress conditions, the initial DoS distribution decreases exponentially from 2

x 10^{20} cm^{-3} eV^{-1} to 1 x 10^{18} $cm^{-3}eV^{-1}$ within 0.1 eV above E_V. Thereafter the DoS shows a broad, weak feature superimposed on a slowly decaying background which eventually decreases to ~10^{17} cm^{-3} eV^{-1} at ~0.4 eV above E_V.

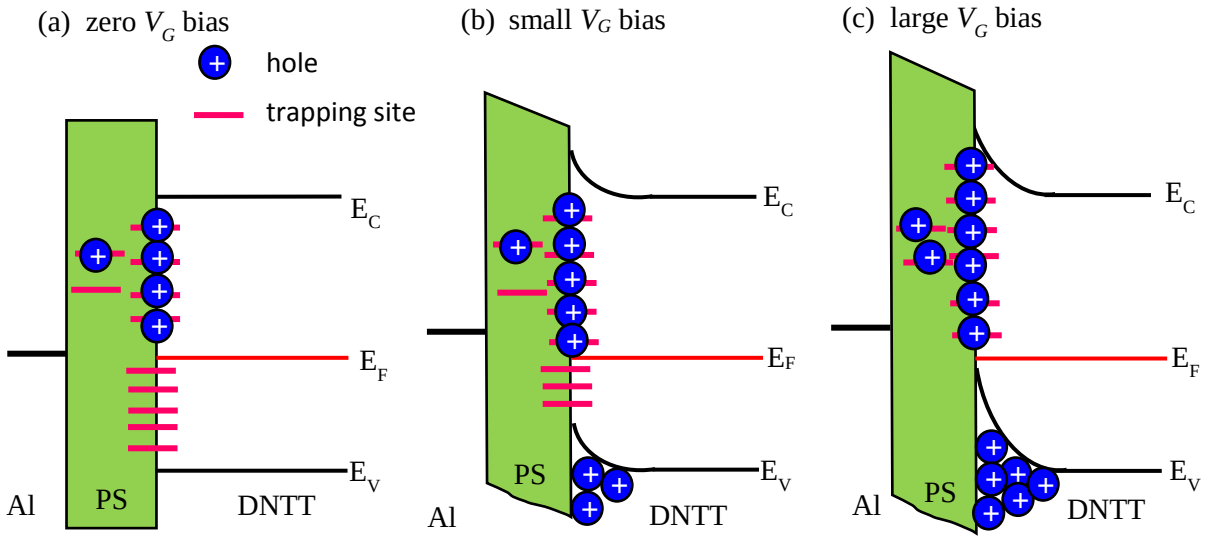

Figure 5.5 Schematic band diagram illustrating the effect of traps at the interface of semiconductor/insulator for (a) V_G = 0 V, (b) small V_G and (c) large V_G.

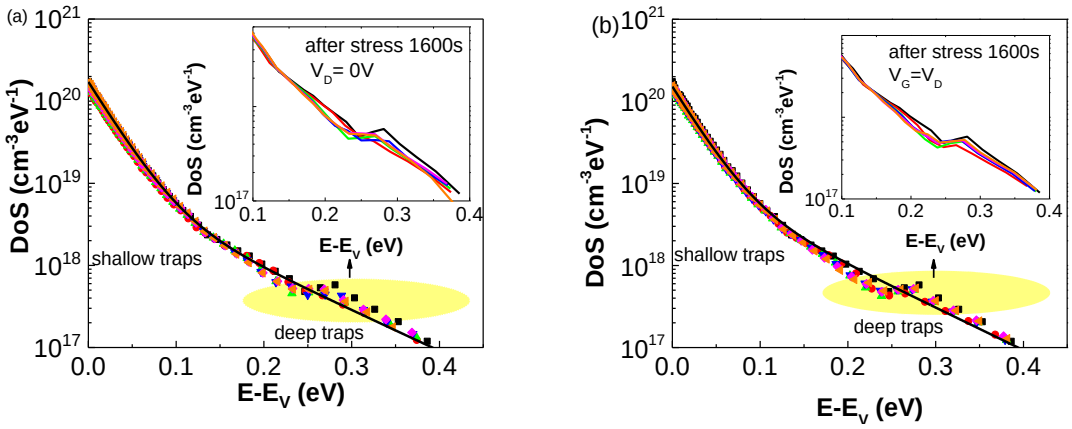

Figure 5.6 The DoS as a function of E-E_V before stress (black data point) and after bias-stress with stress condition of (a) V_D = 0V and stress voltage, V_G = -5 V (red), -10 V (green), -20 V (blue), -30 V (magenta) and -40 V(orange) and (b) V_G =V_D ranging from -5 to -40 V with same color assignment as (a). The solid black lines in the main plots represent the double exponential fits to equation (5.1) for shallow and deep traps.

The DoS distribution was fitted with the double exponential function of a localized states DoS according to:

$$N(E) \approx \frac{N_{t1}}{E_{t1}} exp\left(-\frac{E}{E_{t1}}\right) + \frac{N_{t2}}{E_{t2}} exp\left(-\frac{E}{E_{t2}}\right) \quad (5.1)$$

where N_{t1} and N_{t2} are the total trap densities in the shallow and deep states respectively while E_{t1} and E_{t2} are the characteristic energies decay of the distributions in the shallow and deep states respectively. Since the DoS distribution for each curve exhibits similar features, only one curve was fitted with equation (5.1) as shown by the solid line in Figure 5.6. Under bias stress V_G = -40 V, V_D = 0 V, fitting parameters related to the shallow states ≤ 0.1 eV, are N_t ~ 4.16 x 10^{18} cm^{-3} with E_t ~ 25 meV. The characteristics energy is slightly lower than in pentacene thin films, E_t ~ 32 meV reported by Kalb using the same method [107]. For deeper states ≥ 0.1 eV, N_t ~ 7.98 x 10^{17} cm^{-3} with E_t ~ 88 meV.

5.2.2 Recovery

After completing a bias stress test, selected devices were subjected to a recovery procedure. The devices were left short-circuited in the dark for a few minutes and also under ambient light for a few seconds until V_T recovered to its original value. The recovery was interrupted at fixed times to record the transfer characteristics of the transistor with a drain bias of V_D = −1 V by sweeping the gate bias from 20 to -60 V.

It can be clearly observed in Figure 5.7(a), that the transfer curves shift back towards the one obtained prior to stressing. Changes in the threshold voltage (ΔV_T) over time both during stress and under recovery are shown in Figure 5.7(b). It is observed, that the recovery of ΔV_T was only partial after 5 minutes relaxation in the dark. However, with ambient light exposure for a few seconds, ΔV_T fell to zero and the transfer curve was restored within ~ 10 s to its original value, thus providing a rapid method of re-setting the device ahead of further measurements. Such a fast recovery property is technologically relevant and could be utilized in practical applications such as in a memory device.

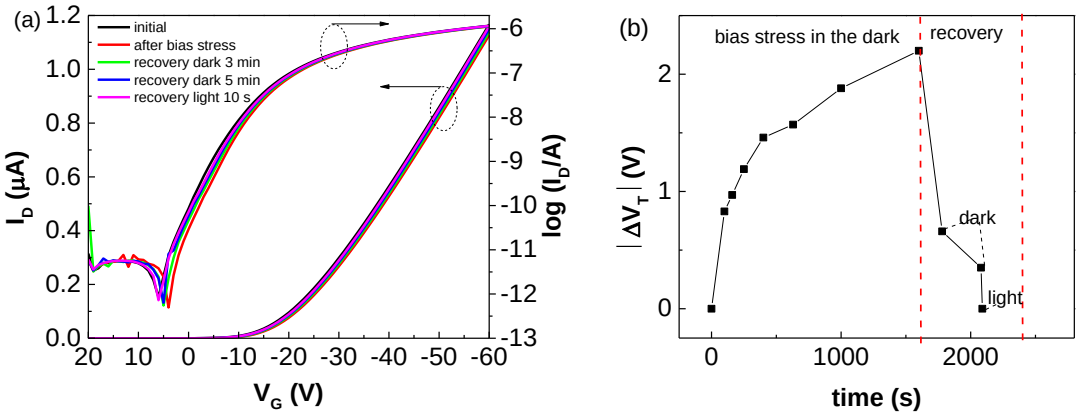

Figure 5.7 (a)Transfer curves and (b) time dependence of ΔV_T. The device was subjected to bias stress $V_G = -40$ V, $V_D = 0$ V in the dark for 1600 s. The recovery process was performed in the dark and under ambient illumination with $V_G = V_D = 0$ V.

The above behaviour was further studied by evaluating the DoS during the stress and recovery period. The DoS distribution from E_V to 0.4 eV is shown in Figure 5.8(a). Figure 5.8(b) shows the DoS in the range $E_V > 0.1$ eV after light induced recovery. It is seen that after the bias stress (red line), the DoS distribution reduced slightly, but slowly reaches the initial (black line) DoS distribution after recovery with light exposure (blue line). However relaxation in the dark conditions exhibits a slow recovery to the initial (black line) DoS distribution.

The charge detrapping mechanism during recovery can be explained as follows. During bias stress, holes are trapped at the interface as shown in Figure 5.8(c). When the gate bias is zero, the density of holes in the accumulation layer vanishes and E_F rises at the interface (Figure 5.8(d)). This leads to hole detrapping from interface traps now appearing below E_F accompanied by a return to flat band conditions. The detrapping process is accelerated under ambient light because of the light induced electrons may effectively neutralize trapped holes [74]. Therefore, recovery by light exposure with source and drain terminals grounded ($V_D = V_G = 0$ V) became the usual procedure for resetting. Overall, the recovery process in this device was relatively fast. However further experiments were required to accurately describe the relaxation phenomenon in this device.

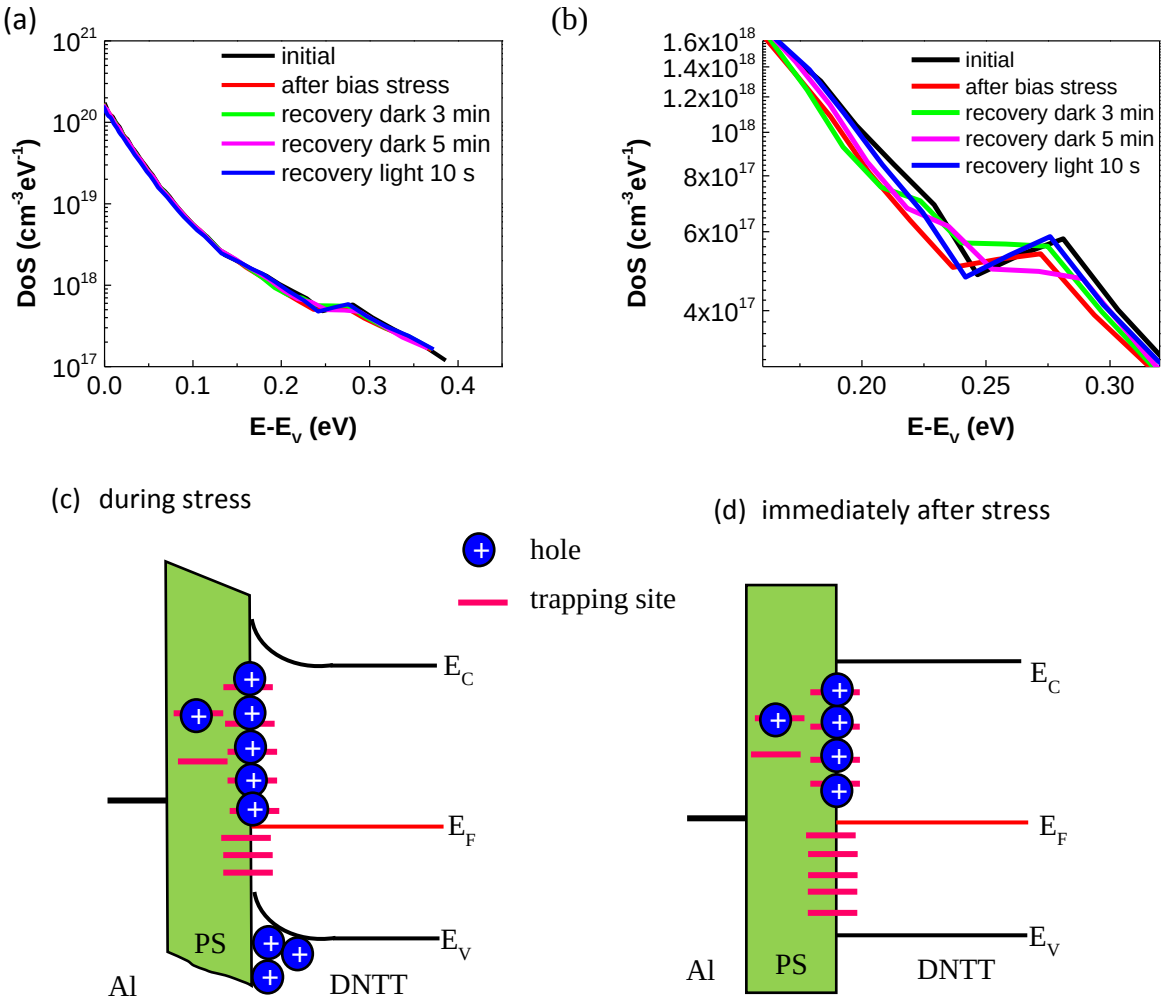

Figure 5.8 (a) The DoS distribution as a function of as a function of E-E_V after stress and during recovery time. (b) An expended view of changes in the deep states. Proposed schematic band diagram illustrating the effect of traps at the interface of semiconductor/insulator (c) under stress and (d) after recovery time.

5.2.3 Effect of Stress Time

This section reports the time-dependence of the stress effect. Initially, the device was subjected to a constant negative gate bias, V_G = -40 V and drain bias, V_D = 0 V for 100 s in the dark at room temperature. Immediately after stress, the output characteristics were recorded followed by transfer characteristics in the linear (V_D = -1 V) and saturation (V_D = -60 V) regimes. After the device had recovered, the experiment was repeated with increasing stress times up to 10000 s. Then the same measurement was continued on the same sample

but with different drain biases, V_D in the linear, V_D < -20 V, and saturation, $V_D \geq$ -20 V regimes.

Figure 5.9 shows the output characteristics taken before and after bias stress with stress conditions corresponding to V_G = -40 V and various V_D (0 to -40 V) for times ranging from 100 s to 10000 s. After all stress conditions and time, for each gate voltage V_G, the drain current exhibits excellent linear and saturation behavior at low and high V_D respectively. No noticeable hysteresis was observed between the forward and backward scan. However, the drain current, I_D, reduced after with increasing stress time, with the reduction being greatest for stressing in the linear regime (low V_D), as reported by others e.g. in pentacene TFTs [75, 83].

Figures 5.10 and 5.11 show plots of I_D vs V_G obtained at V_D= -1 V (linear region) and $I_D^{1/2}$ vs V_G obtained at V_D= -60 V (saturation region), before and after bias stress. Under any stress condition, I_D decreases due to a shift of both V_{ON} and V_T to more negative gate voltages as stress time increased. The plots of log I_D-V_G before and after the bias stresses show that the subthreshold slope also does not change after the transistor has undergone bias stressing. This suggests that bias stress simply arises from hole trapping in interface traps or in the insulator itself. However, there is considerable discussion as to whether the traps are located in the semiconductor, in the insulator or at interface between the semiconductor and insulator [51].

Figures 5.12 and 5.13 show the gate-voltage dependence of the mobility, extracted using equations (2.11) and (2.13) respectively. It can be observed that both plots show a simple translation along the voltage axis. This is readily explained by a shift in threshold voltage caused by a change the flatband voltage, ΔV_{FB}.[108] Hole trapping in semiconductor states would have distorted the transfer characteristics and hence the V_G-dependence of mobility. Interestingly, both μ_{lin} and μ_{sat} exhibit maximum values ~ 1 cm^2/V.s with only a small reduction appearing after stress. However, μ_{lin} saturates at higher V_G while μ_{sat} still slowly increased as V_G increased. The inset shows a negligible shift in the maximum field-effect mobility, $\Delta\mu$ as a function of stress time.

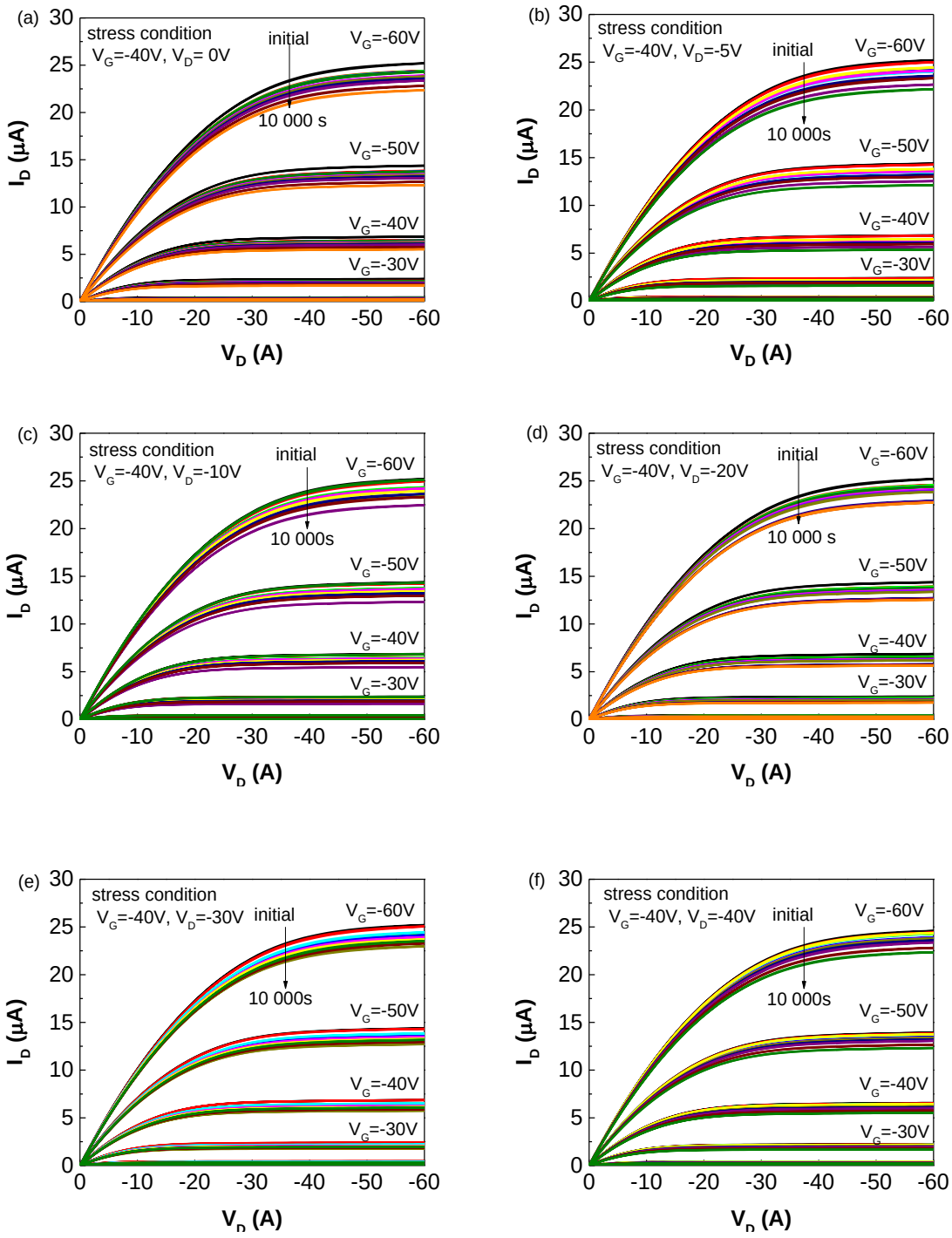

Figure 5.9. Output characteristics for forward and reverse sweeps obtained after stressing for increasingly longer time with a constant gate voltage, V_G = -40 V and with drain voltages, V_D of (a) 0 V, (b) -5 V, (c) -10 V, (d) -20 V, (e) -30 V and (f) -40 V.

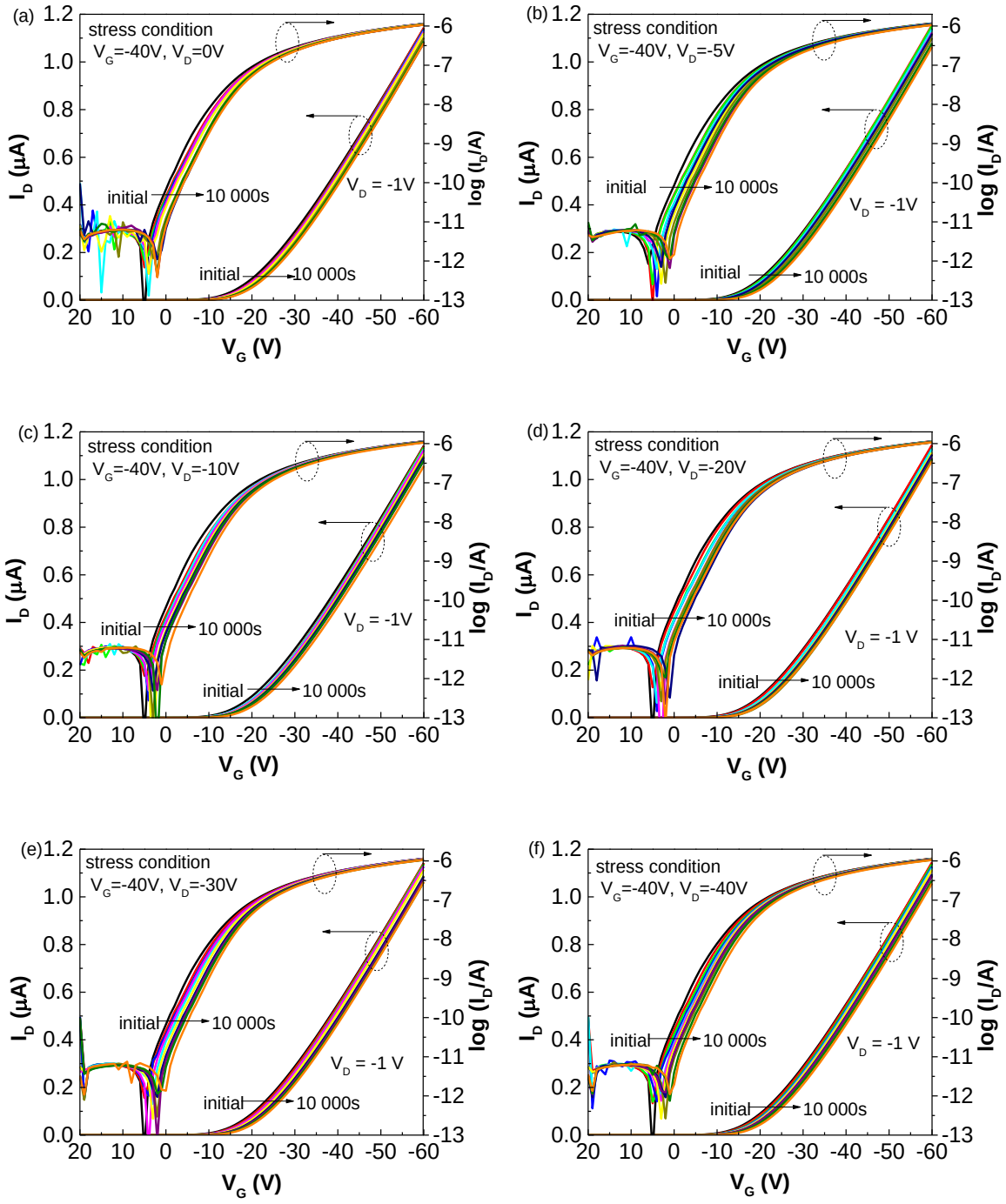

Figure 5.10 Transfer characteristics showing the time-dependence of the bias stress resulting from applying a constant gate voltage, V_G = -40 V and drain voltages, V_D of (a) 0 V, (b) -5 V, (c) -10 V, (d) -20 V, (e) -30 V and (f) -40 V. In all cases the characteristics were obtained with V_D = -1 V.

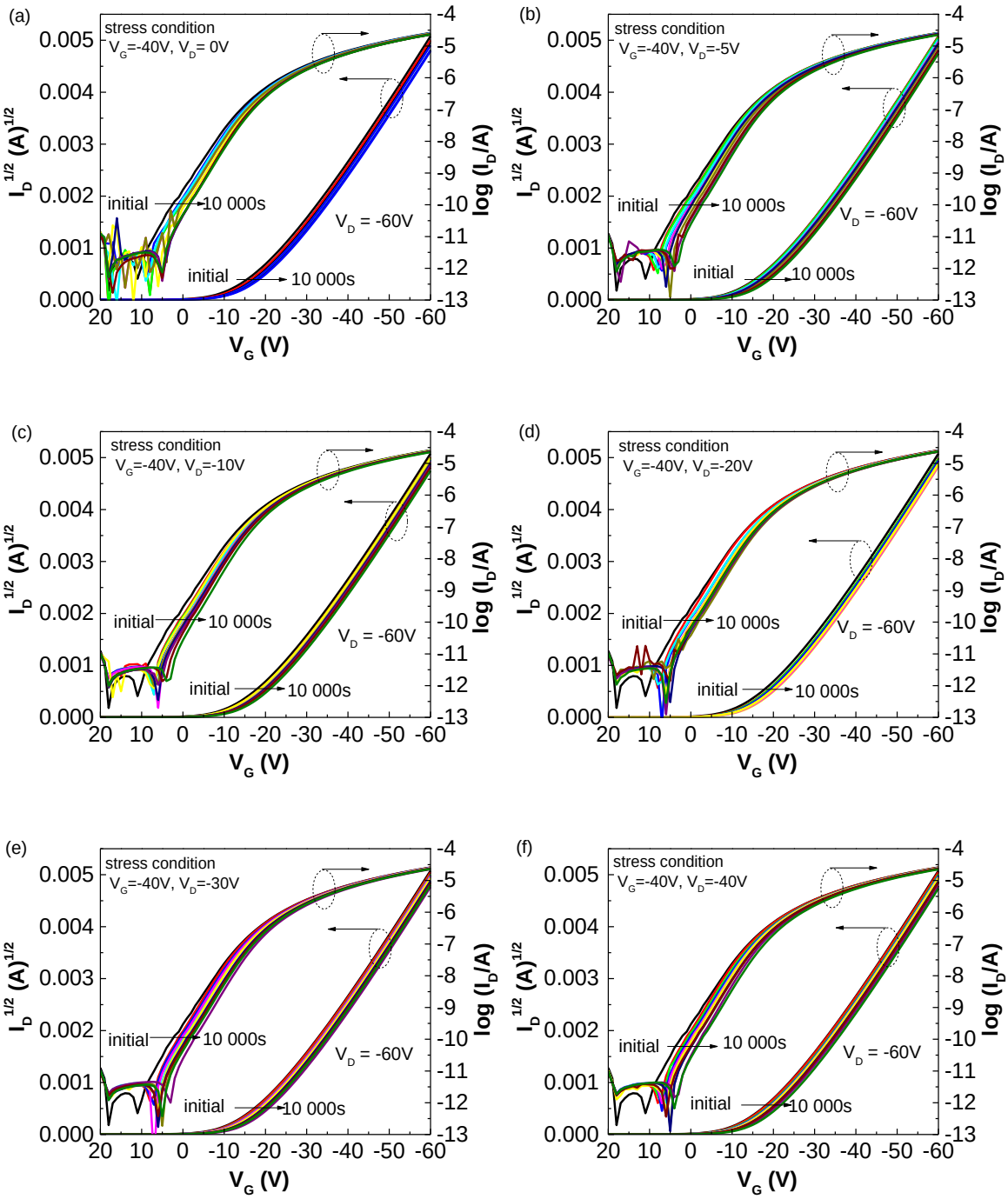

Figure 5.11 Transfer characteristics showing the time-dependence of the bias stress resulting from applying a constant gate voltage, V_G = -40 V and drain voltages, V_D of (a) 0 V, (b) -5 V, (c) -10 V, (d) -20 V, (e) -30 V and (f) -40 V. In all cases the characteristics were obtained with V_D = -60 V.

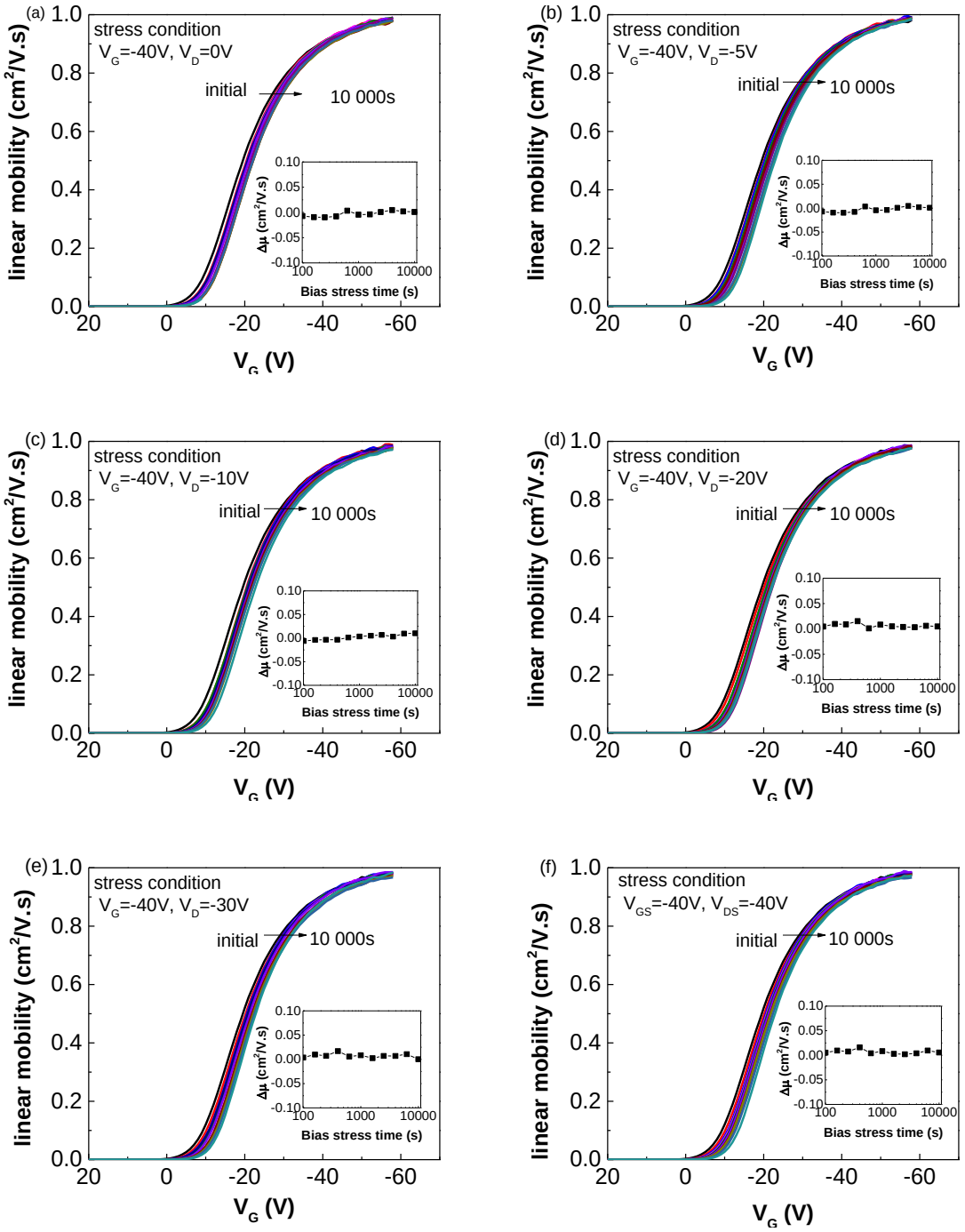

Figure 5.12 Linear mobility as a function of gate bias following constant gate bias stress of V_G = -40 V and with drain bias (a) V_D = 0V, (b) V_D = -5V, (c) V_D = -10V, (d) V_D = -20V, (e) V_D = -30V and (f) V_D = -40V for various times up to 10000s. Each inset show the shift in the maximum mobility as a function of bias stress time.

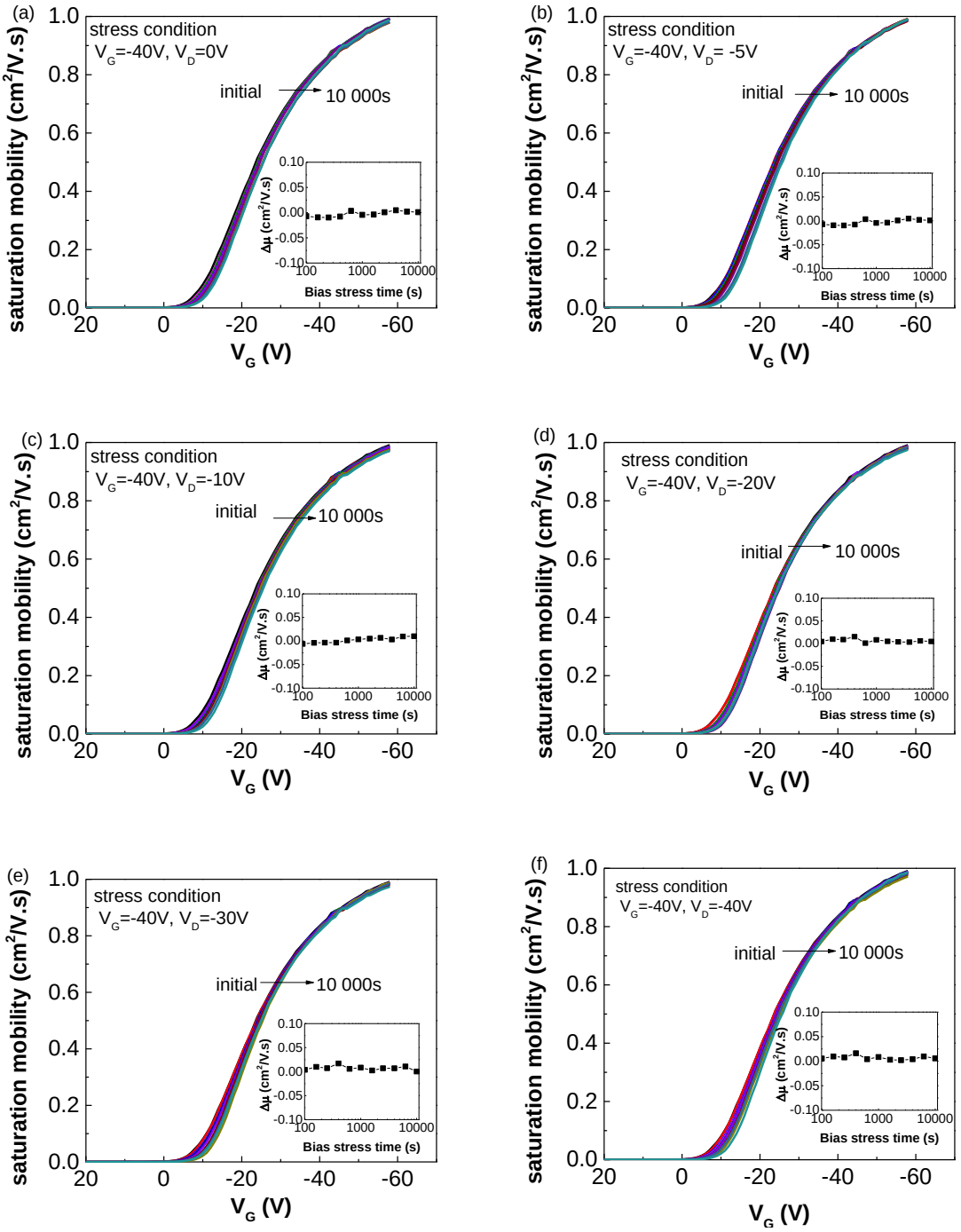

Figure 5.13 Saturation mobility as a function of gate bias following constant gate bias stress of V_G = -40 V and with drain bias (a) V_D = 0V, (b) V_D = -5V, (c) V_D = -10V, (d) V_D = -20V, (e) V_D = -30V and (f) V_D = -40V for various times up to 10000s. Each inset show the shift in the maximum mobility as a function of bias stress time.

Figures 5.14(a) and (b) show the time dependence of ΔV_T extracted from the linear and saturation transfer characteristics. In both cases, ΔV_T measured from both transfer characteristics were found to decrease when the drain bias increases from 0 to -40 V. This has been explained previously due to lower hole concentration towards the drain end of the channel when stressing in the saturation regime (high V_D) which in turn results in fewer charge carriers being trapped [75, 83].

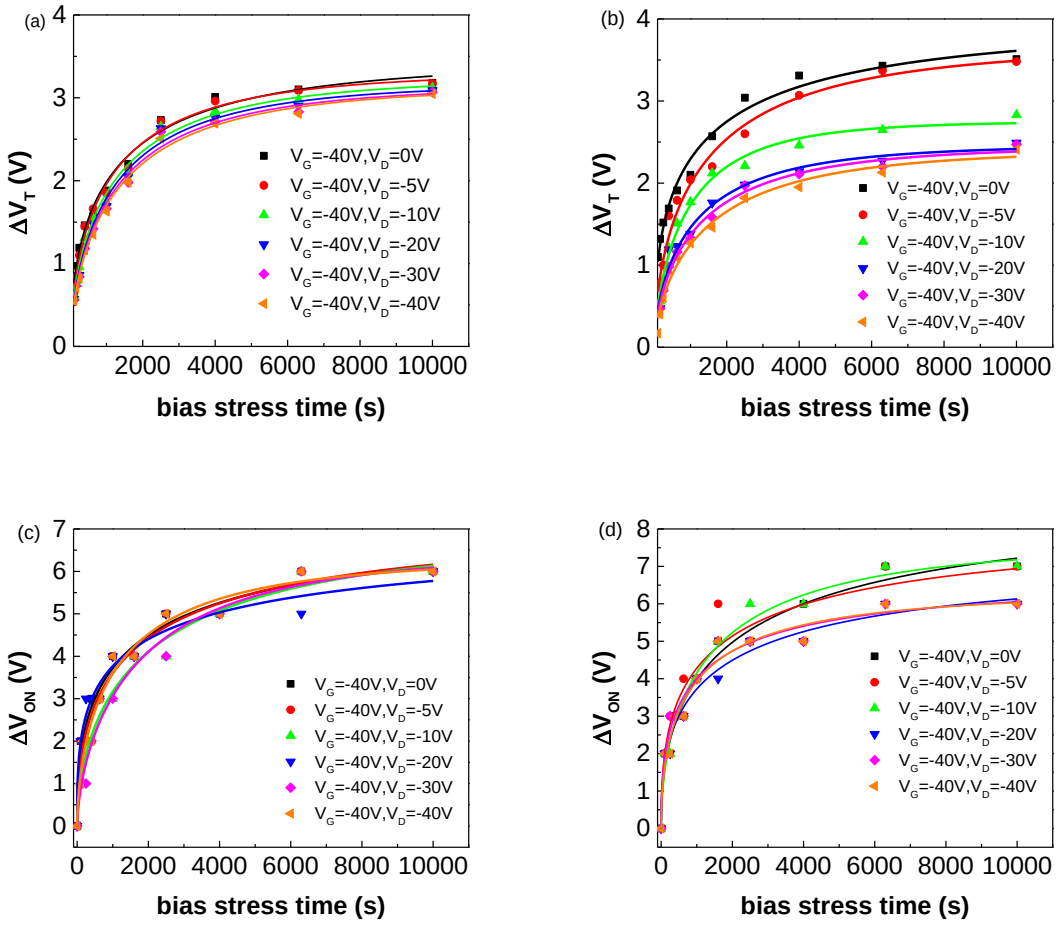

Figure 5.14 Shifts of threshold voltage, V_T at (a) V_D =-1V and (b) V_D =-60V and turn-on voltage, V_{ON} at (c) V_D =-1V and (d) V_D =-60V as a function of bias stress time obtained from transfer characteristics. The solid lines in both figures represent the stretched-exponential fits made to the data using equation (5.2).

Figures 5.14(c) and 5.14(d) show the time dependence of ΔV_{ON} extracted from the linear and saturation transfer characteristics. The magnitude of ΔV_{ON} was slightly higher than ΔV_T. This is because changes in ΔV_T involve other physical parameters such as changes in the subthreshold region and mobility whereas changes in ΔV_{ON} only involve charge trapping at the interface. It has been observed in Figure 5.14(c) that ΔV_{ON}, is almost independent with V_D while in Figure 5.14(d), V_D dependence is not systematic.

The dependence of ΔV_T on time is generally described by the stretched exponential function given by [67, 80], i.e.

$$\Delta V_T(t) = |V_T(\infty) - V_T(0)| \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \tag{5.2}$$

where $V_T(\infty)$ is the threshold voltage after long stress times, $V_T(0)$ its value prior to bias stress, τ is a characteristic time constant and β the stretching factor describing the distribution in trap times. The solid curves in Figures 5.14(a) and 5.14(b) represent the stretched exponential fitting of equation (5.2) to the data using the fitting parameters listed in Table 5.1 for different drain-bias stress conditions (V_G = -40 V and V_D ranging from 0 V to -40 V).

Table 5.1 Parameters obtained by fitting equation (5.2) to the measured bias stress-induced ΔV_T in Figures 5.14(a) and 5.14(b).

V_D (V)	$\lvert V_T(\infty)-V_T(0) \rvert$ (V)		τ (s)		β	
	Linear	**saturation**	**Linear**	**saturation**	**Linear**	**saturation**
0	3.44	3.94	1.32×10^3	1.35×10^3	0.54	0.45
-5	3.31	3.67	1.20×10^3	1.52×10^3	0.60	0.60
-10	3.23	2.75	1.30×10^3	1.01×10^3	0.62	0.69
-20	3.16	2.46	1.33×10^3	1.18×10^3	0.78	0.65
-30	3.14	2.45	1.39×10^3	1.36×10^3	0.79	0.64
-40	3.13	2.36	1.47×10^3	1.58×10^3	0.92	0.66

The stretched exponential fits confirm the decreasing trend in $|V_T(\infty)-V_T(0)|$ apparent in Figures 5.15(a) and 5.15(b) as the stress conditions change from the linear to the saturation regime. Only minor changes are seen in τ, which is almost constant at ~1.33 x 10^3 s in the linear regime and ~1.4 x 10^3 s in the saturation. The time-constant distribution parameter, τ increases as V_D increases (albeit more slowly when extracted from saturation transfer characteristics) suggesting a tendency to a less broad distribution. This effect has also been observed in pentacene OTFTs [75]. Interestingly, many authors [19, 67, 86] assume that $V_T(\infty) = V_G$ which occurs when the effective gate field seen by free holes in the channel is reduced to zero. This is clearly not the case here as $|V_T(\infty) - V_T(0)| < 4V$ is significantly lower than $|V_G - V_T(0)| \sim 20V$ as seen in Figure 5.10.

The time dependence of ΔV_{ON} is also fitted with the stretched exponential fitting of equation (5.2) as shown by solid lines in Figures 5.14(c) and 5.14(d). The fitting parameters for ΔV_{ON} are listed in Table 5.2 for the different drain-bias stress conditions. The magnitude of $|V_{ON}(\infty) - V_{ON}(0)|$ is slightly higher than $|V_T(\infty) - V_T(0)|$. This is expected since $|V_{ON}(\infty)| > |V_T(\infty)|$. Similar to ΔV_T, $V_{ON}(\infty) = V_G$ is also clearly not the case here since $|V_{ON}(\infty) - V_{ON}(0)| < 9\,V$ is significantly lower than $|V_G - V_{ON}(0)| \sim 34\,V$. It is also observed that the magnitudes of $|V_{ON}(\infty) - V_{ON}(0)|$ and τ in Figures 5.15(c) and 5.15(d), are found to decrease as drain bias stress voltage is increased. β are in the range of 0.43 to 0.64 in the linear regime while a much narrower range in the saturation from 0.56 to 0.62.

Table 5.2 Parameters obtained by fitting equation (5.2) to the measured bias stress-induced ΔV_{ON} in Figures 5.14(c) and 5.14(d).

V_D (V)	$\lvert V_{ON}(\infty)-V_{ON}(0) \rvert$		τ (s)		β	
	Linear	**Saturation**	**Linear**	**Saturation**	**Linear**	**Saturation**
0	7.06	8.47	1.95 x 10^3	2.59 x 10^3	0.43	0.448
-5	6.97	7.93	1.97 x 10^3	1.80 x 10^3	0.48	0.42
-10	6.83	7.63	2.32 x 10^3	1.54 x 10^3	0.56	0.56
-20	6.81	7.06	1.80 x 10^3	1.95 x 10^3	0.37	0.43
-30	6.45	6.49	1.97 x 10^3	1.10 x 10^3	0.64	0.45
-40	6.28	6.29	1.33 x 10^3	1.03 x 10^3	0.59	0.51

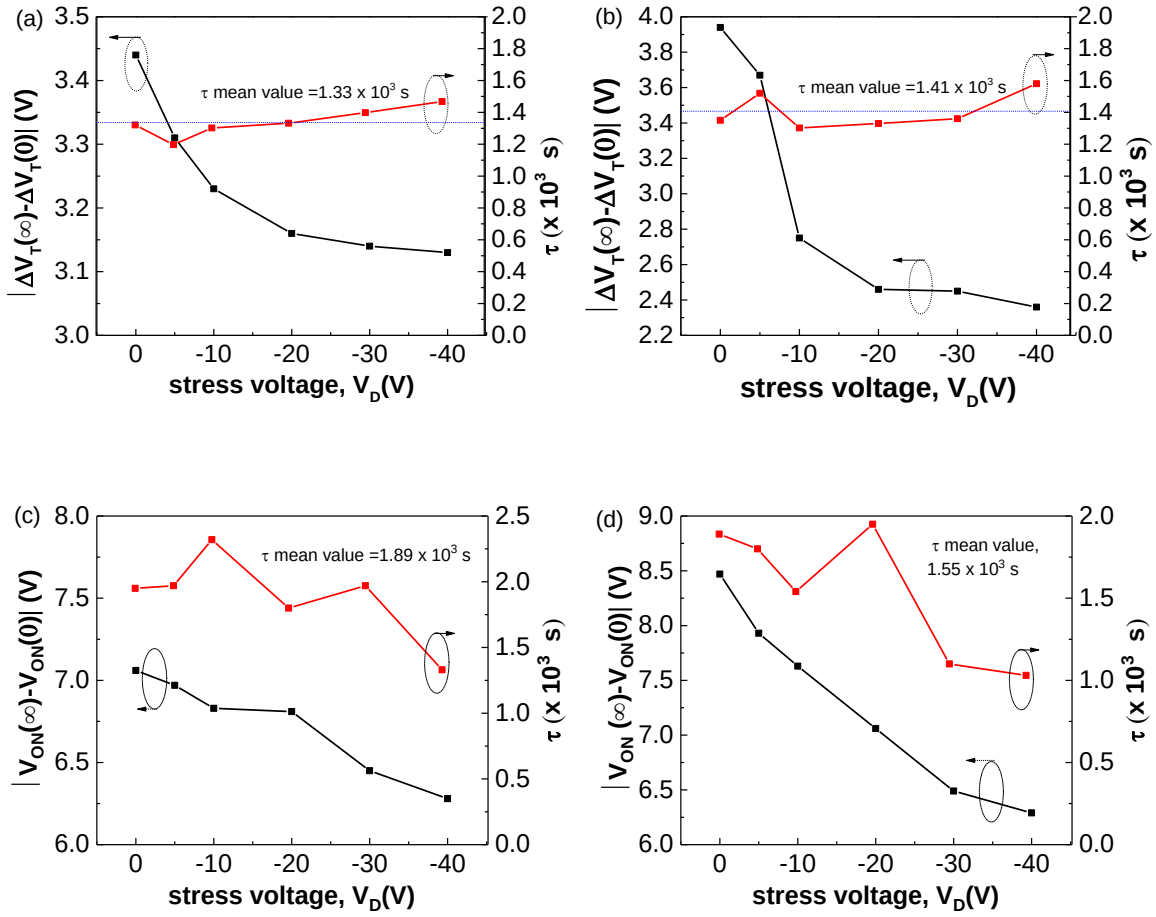

Figure 5.15 $|V_T(\infty) - V_T(0)|$ and τ as a function of drain voltage, V_D obtained at (a) V_D = -1V and (b) V_D =-60V . $|V_{ON}(\infty) - V_{ON}(0)|$ and τ as a function of drain voltage, V_D obtained at (c) V_D = -1V and (d) V_D =-60V.

As noted above, the measurement of ΔV_T from the transfer curve has some inaccuracy, since the device may recover partially when measuring the transfer characteristics. Therefore other workers [86] have avoided this problem by monitoring the decay of the drain-source current, I_D, with time under bias stress instead of measuring ΔV_T from the transfer characteristics. Figures 5.16(a), 5.17(a) and 5.17(c) show the time decay of $I_D(t)$ normalized to its initial value $I_D(0)$ under continuous bias stress for increasing stress times ranging from 10^2 s to 10^4 s. In between each plot, the device was illuminated under short-circuit conditions to return V_T to its initial value, as described above. Since the plots do not follow the same trajectory, it is possible that recovering the initial V_T does not recover exactly to the initial interface conditions of the devices for each run. This suggest that relaxation to the initial state in the

dark or when illuminated may not necessarily be the result of detrapping but due to interface trapping of counter charges.

In the following, we concentrate therefore on the 10,000 s decay curves (Figures 5.16(b), 5.17(b) and 5.17(d)). The stretched-exponential description for ΔV_T in equation (5.2) can be extended to derive the dependence of I_D with time [86]. In the linear regime, in the presence of a threshold voltage shift ΔV_T, I_D is described by:

$$I_D(t) = K\left[V_G - \left(V_T(0) + \Delta V_T(t)\right)\right]V_D \tag{5.3}$$

here $K = \mu_{lin} C_{ins} \frac{W}{L}$ and upon substituting from equation (5.2)

$$I_D(t) = K\left[V_G - V_T(0) - \Delta V_T(\infty) + \Delta V_T(\infty) e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]V_D \tag{5.4}$$

where $\Delta V_T(\infty) = V_T(\infty) - V_T(0)$. Then after normalizing $I_D(t)$ to its initial value $I_D(0)$, equation (5.4) becomes

$$\frac{I_D(t)}{I_D(0)} = \frac{\left[V_G - V_T(0) - \Delta V_T(\infty) + \Delta V_T(\infty) e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]}{V_G - V_T(0)} \tag{5.5}$$

which simplifies to

$$\frac{I_D(t)}{I_D(0)} = \left(1 - \frac{\Delta V_T(\infty)}{V_G - V_T(0)}\right) + \frac{\Delta V_T(\infty)}{V_G - V_T(0)} e^{-\left(\frac{t}{\tau}\right)^{\beta}}.$$

or

$$\frac{I_D(t)}{I_D(0)} = A + B e^{-\left(\frac{t}{\tau}\right)^{\beta}}. \tag{5.6}$$

In the saturation regime, ΔV_T over time is defined by the square-law equation for $I_D(t)$:

$$I_D(t) = \frac{K}{2}\left[V_G - \left(V_T(0) + \Delta V_T(t)\right)\right]^2 \tag{5.7}$$

which after substituting from equation (5.2) becomes

$$I_D(t) = \frac{K}{2}\left[V_G - V_T(0) - \Delta V_T(\infty) + \Delta V_T(\infty) e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]^2. \tag{5.8}$$

After normalization, to the initial value, the degradation of $I_D(t)$ over time in the saturation regime is given by:

$$\frac{I_D(t)}{I_D(0)} = \left\{ \frac{\left[V_G - V_T(0) - \Delta V_T(\infty) + \Delta V_T(\infty) e^{-\left(\frac{t}{\tau}\right)^{\beta}} \right]}{V_G - V_T(0)} \right\}^2 \tag{5.9}$$

which reduces to

$$\frac{I_D(t)}{I_D(0)} = \left\{ \left(1 - \frac{\Delta V_T(\infty)}{V_G - V_T(0)} \right) + \frac{\Delta V_T(\infty)}{V_G - V_T(0)} e^{-\left(\frac{t}{\tau}\right)^{\beta}} \right\}^2$$

$$= \left[A + B e^{-\left(\frac{t}{\tau}\right)^{\beta}} \right]^2 \tag{5.10}$$

with *A = 1-B*. Equations (5.13) and (5.17) described $I_D(t)/I_D(0)$ in the linear and saturation regimes respectively. Zhang et al [86] developed this model based on the current in the saturation regime but the square term seems to be missing from the entire equation which may be an editorial error. Most authors described the extended model of the stretched exponential function based on drain current decay in the form of $I_D(t)/I_D(0) = exp\left(-\frac{t}{\tau}\right)^{\beta}$, which presumes that , $\Delta V_T(\infty) = (V_G - V_T(0))$, [19, 86-88] which is clearly not the case here as discussed above. This was implicitly accepted also by Padma et al [109], whose results indicate a drain current asymptoting to a finite value rather than zero at infinite time, which will indeed be the case if $\Delta V_T(\infty) < (V_G - V_G(0))$.

The 10,000 s $I_D(t)/I_D(0)$ decay in Figure 5.16(b) corresponding to V_D in linear was fitted with equation (5.6) while Figures 5.17(b) and 5.17(d) were fitted with equation (5.10) corresponding to V_D in saturation regime respectively. By adjusting parameter values, excellent fits (dashed lines) can obtained to each of the experimental plots using the values listed in Table 5.3. The experimental plot is also fitted with the predicted values (solid lines) by substituting the relevant parameter values from Table 5.1 into equations (5.6) and (5.10) respectively.

Table 5.3 Parameters for the fits of equation (5.6) in the linear and equation (5.10) in saturation regimes to the normalized current decay $I_D(t)/I_D(0)$ data in Figure 5.17(b), 5.18(b) and 5.18(d).

V_D (V)	τ (s)	β	V_T (0) (V)	$\Delta V_T(\infty)$ (V)	R^2
Linear					
-5	2050	0.75	-21	3.08	0.99141
Saturation					
-30	2395	0.58	-19	2.47	0.9993
-40	4247	0.54	-19	4.09	0.99867

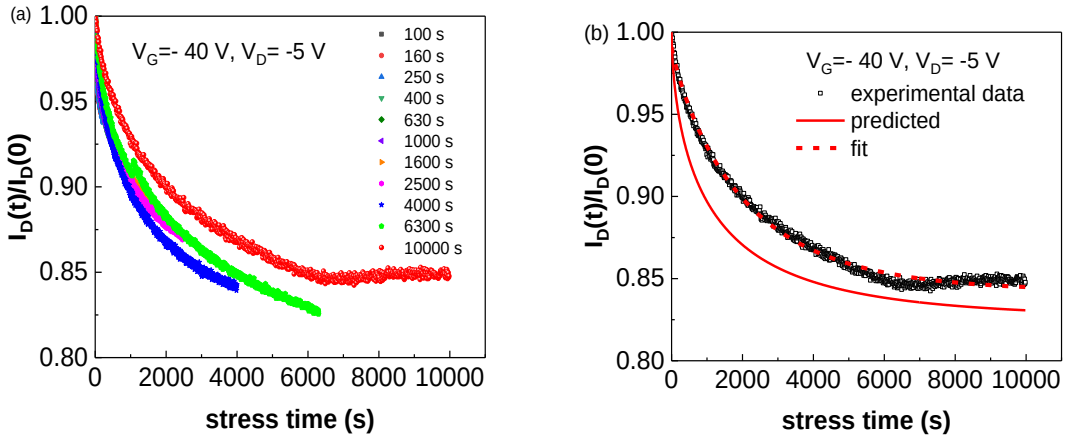

Figure 5.16 (a) Time-dependence of $I_D(t)/I_D(0)$ with V_G= -40 V and V_D =-5 V over various times ranging from 100 s to 10,000 s. In (b) the 10,000 s data is replotted together with fits based on equation (5.6). The solid line is fit of the data using values from Table 5.1 while the dashed line represents the best fits using fitting parameters as listed in Table 5.3.

The predicted curve (solid lines) under V_D = -5 V (Figure 5.16(b)) and V_D=-30 V (5.17(b)) do not fit well with the experimental data but it is likely to be lying in the middle of $I_D(t)/I_D(0)$ under continuous bias stress for different times. While for V_D=-40 V, the predicted curve appears to envelope all curves as shown in Figure 5.17(d). It is found that both equations (5.13) and (5.17) are very sensitive to the value of $V_T(0)$. So any possible ambiguity related to the extraction of the threshold voltage, V_T from the transfer-curves could affect the fitting.

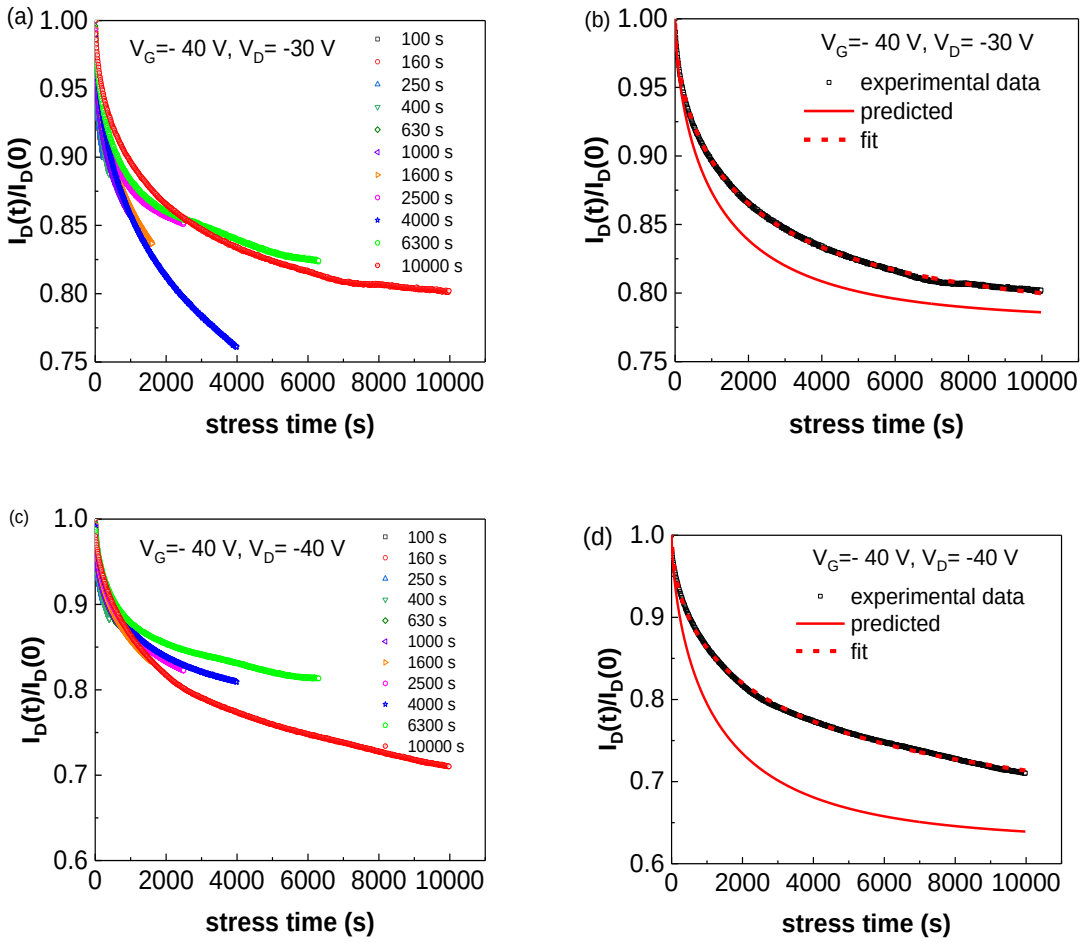

Figure 5.17 Time-dependence of $I_D(t)/I_D(0)$ with V_G = -40 V and (a) V_D = -30 Vand (c) V_D = -40 V over various times ranging from 100 s to 10,000 s. In (b) and (d) the 10,000 s data is replotted together with fits based on equation (5.10). The solid line is fit of the data using values from Table 5.1 while the dashed line represents the best fits using fitting parameters as listed in Table 5.3

The effect of bias stress on PS-DNTT was also studied by investigating their density of state, DoS distribution using Grünewald model. Figure 5.18(a) to 5.18(f) show the DoS plotted as a function of E-E_V. Under all bias stress conditions, the initial DoS distribution decreases from 1 x 10^{20} $cm^{-3}eV^{-1}$ to 1 x 10^{17} $cm^{-3}eV^{-1}$ following a double-exponential decay (solid lines in Figure 5.18). As can be seen that the effect of bias stress is minimal with the plots obtained before and after bias stress coalescing to a single curve with weak features superimposed at deeper energies.

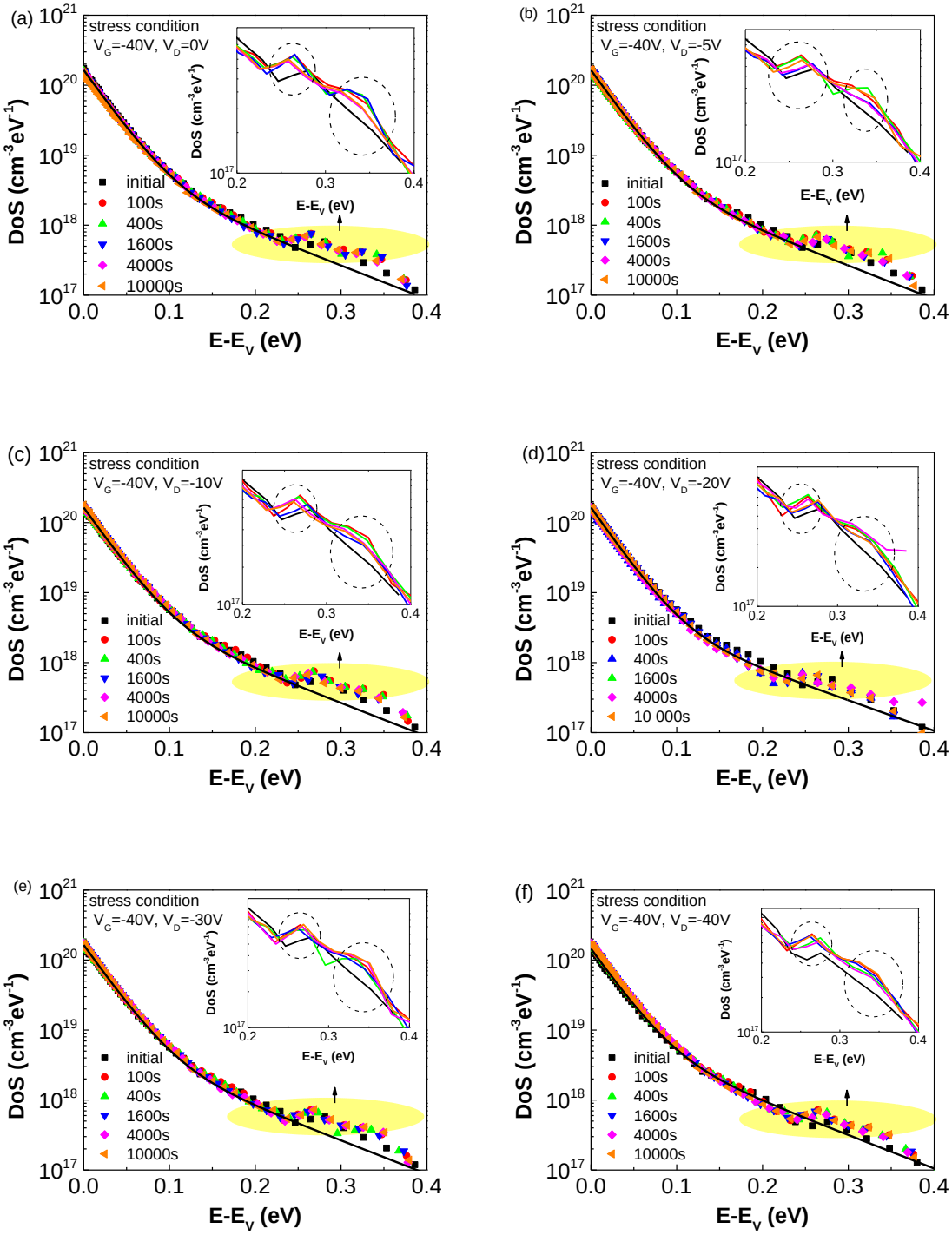

Figure 5.18 Density of states plotted as a function of E-E_V for a constant gate voltage, following bias stress with V_G = -40 V and V_D of (a) 0 V, (b) -5 V, (c) -10 V, (d) -20 V, (e) -30 V and (f) -40 V. Each inset shows a magnified view of the density of state distribution from 0.2 eV to 0.4 eV above E_V.

5.2.4 Effect of Long Term Stress

Figure 5.19(a) shows the transfer characteristics in the linear regime both before and after subjecting an OTFT to gate voltage stress V_G = -40 V at a drain voltage of V_D = 0 V for 12 hours. As can be seen, the transfer characteristics display a similar pattern i.e. a simple translation along the V_G axis as seen in the section 5.2.1 and 5.2.3. The threshold voltage, V_T, shifts from -20 V to -25 V and turn-on voltage, V_{ON} from 8 V to 1 V. The maximum linear mobility, μ_{lin}, as estimated from equation (2.11) appears to be slightly reduced from 1.03 cm^2/V.s to 0.99 cm^2/V.s as shown in Figure 5.19(b). This indicate that long term bias stress has little effect on mobility, as reported for several other OTFT structures and material combinations [11,15,43].

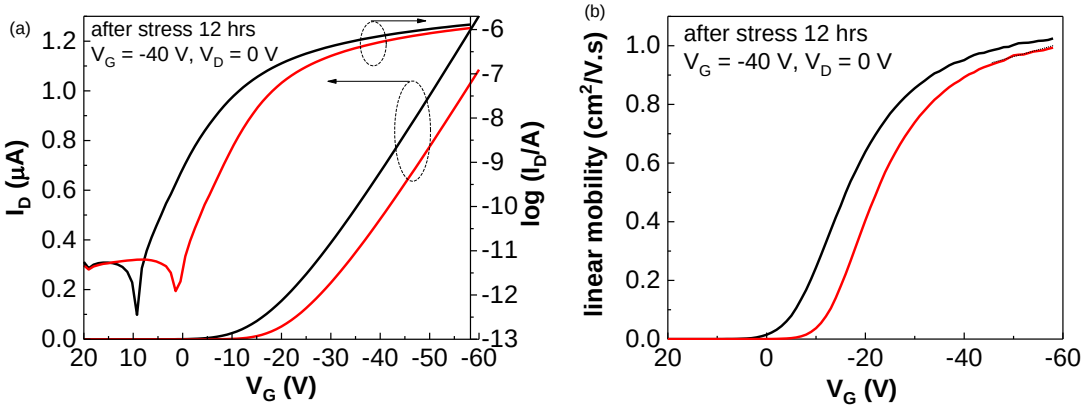

Figure 5.19 (a) Transfer characteristics in forward sweep obtained at V_D = -1 V and (b) Gate-voltage-dependent mobility after 12 hrs stress at V_G =-40 V and V_D = 0 V.

However simply shifting the post-stress curve by V_{ON} = 8.0 V to fit the subthreshold region (semi-log transfer plot) and V_T = 6.5 V above threshold (linear transfer plot), reproduces the initial curve (dashed line) with no indication of change of shape in the transfer characteristic (Figure 5.20(a)). As discussed later, such a difference may be explained either by detrapping during acquisition of the transfer plot or as a result of changes in the DoS of DNTT. The extracted subthreshold slope, SS (3.89 to 3.91 V/decade) remains almost unchanged while the on-off ratio, I_{ON}/I_{OFF} extracted from the plots is ~2.4 x10^5. Figure 5.20(b) shows that the

DoS after stress is similar to the initial DoS confirming that no new electronic states are created within the band gap of DNTT.

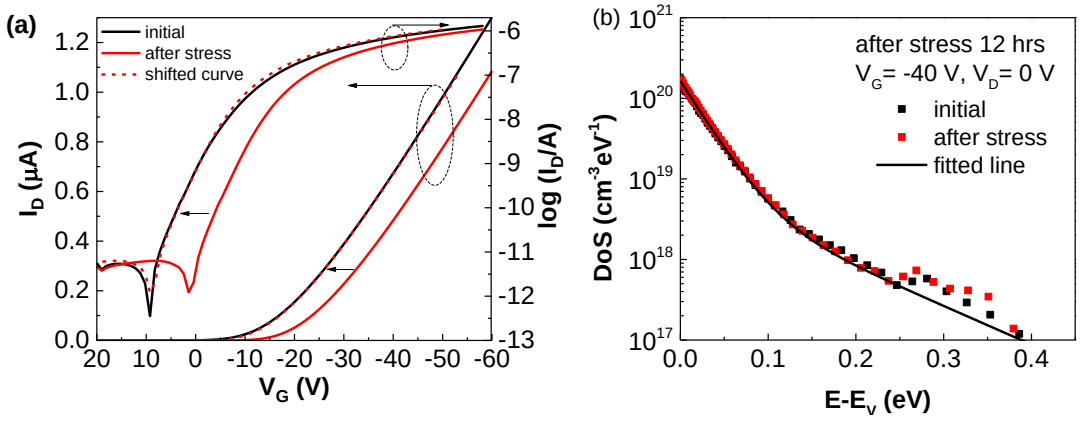

Figure 5.20 (a) Transfer characteristics before and after 12 hours bias stress. The dashed line show that shifting the post-stress plots along the voltage axis by 8.0 V (semi-log plot) and 6.5 V (linear plot) reproduces the pre-stress plots. (b) The DoS distribution as a function of of E-E_V before and after 12 hrs stress at V_G =-40 V and V_D = 0 V.

5.2.5 Influence of the Relative Humidity on Negative Bias-Stress Instability.

Since moisture may be implicated in bias stress effects [42, 110], in this section, the influence of relative humidity (RH%) on negative bias stress instability is investigated. First, the initial transfer characteristic was measured at T = 20 ºC and RH= 20%. Prior to each measurement, the test device was held at the set conditions for 30 min to come into equilibrium. Then the same device was subjected to bias stresses of V_G = -40 V, V_D = 0 V and V_D = V_G = -40 V, for 1600 s which were measured sequentially at 20, 40 and 60% RH at 20 ºC. Between the consecutive measurements, the device was illuminated for a few seconds to fully recover V_T to the initial state. Figures 5.21(a) and 5.21(b) show the transfer characteristics of the TFT exposed to different relative humidity. It can be seen that the bias stress causes a negative shift of the transfer characteristics even at 20%RH. As RH increases, larger shifts in the transfer characteristics were observed for V_G = -40 V, V_D = 0 V while for V_D = V_G = -40 V bias, the shifts were very small. Figure 5.22 shows that the field-effect mobilities were nearly unchanged.

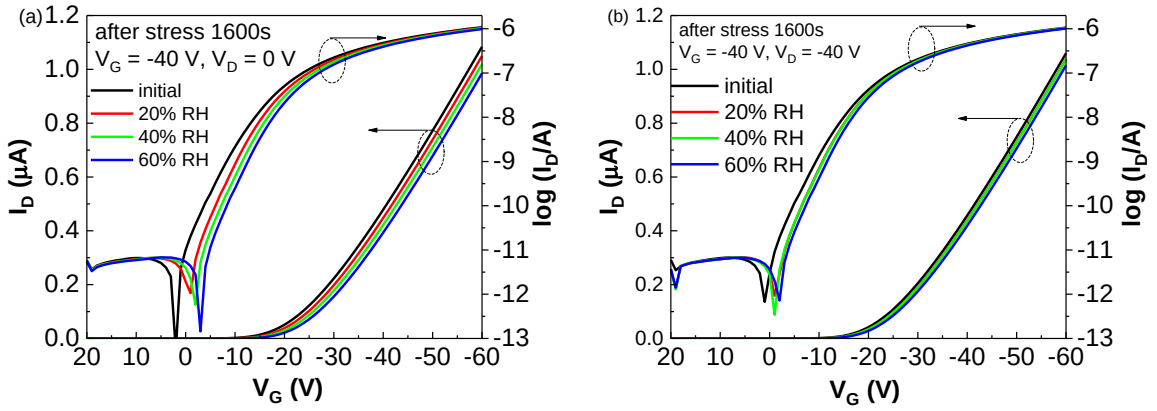

Figure 5.21 Dependence of the bias stress effect on RH. The stress conditions are (a) V_G = -40 V, V_D = 0 V and (b) V_D = V_G = -40 V.

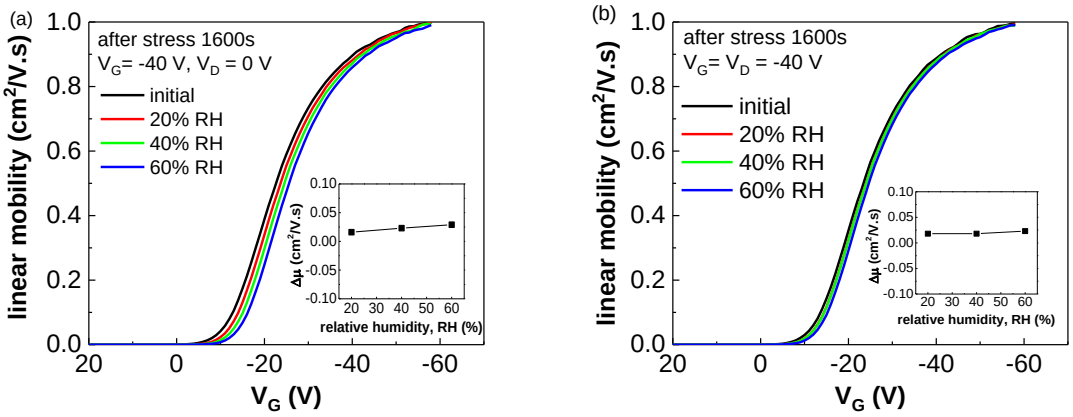

Figure 5.22 Gate-voltage-dependent mobility for stress conditions of (a) V_G = -40V, V_D = 0 V and (b) V_D = V_G = -40V obtained at relative humidity 20%, 40% and 60%.

Figures 5.23(a) and 5.23(b) show the changes ΔV_T and ΔV_{ON} respectively, plotted as a function of RH. Also shown are the corresponding values obtained from the same device in the absence of bias stress. It can be observed that RH increases both ΔV_T. In the presence of bias stress at V_G = V_D = -40 V, ΔV_T almost independent of RH while with V_G = -40V and V_D = 0 V, ΔV_T increases with RH. Interestingly, the shifts ΔV_{ON} in the onset voltage are larger but again appear to be superimposed on an underlying shift arising simply from the increase in RH. These results suggest that the traps responding to bias stress may be different to those responding to changes in RH. It is worth noting that ΔV_T and ΔV_{ON} were significantly

suppressed by applying $V_G = V_D$ = -40 V, in contrast to the grounded V_D. This phenomenon has been explained previously in section 5.3.1, as a result of the decrease in carrier concentration at the drain end of the channel in saturation compared to that in the linear regime.

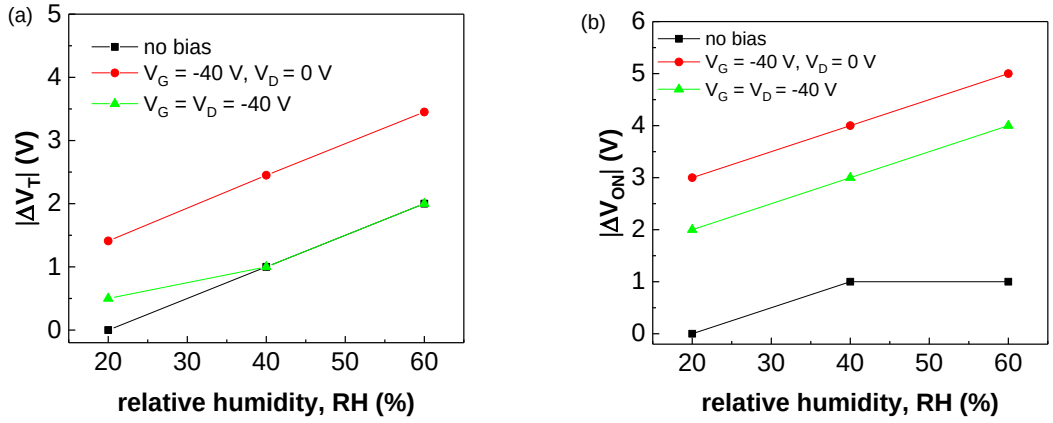

Figure 5.23 Dependence of (a) ΔV_T and (b) ΔV_{ON} on RH% without bias and with bias stress of $V_G = V_D$ = -40 V and V_G = -40 V, V_D = 0 V over 1600s.

Figure 5.24(a) shows the normalized time-dependent decay of drain current, $I_D(t)/I_D(0)$ under $V_G = V_D$ = -40 V bias stress over 1600 s at various RH. $I_D(t)/I_D(0)$ shows 15%, 19% and 22% decay at 20%, 40% and 60% RH respectively. The solid lines show that $I_D(t)/I_D(0)$ at various RH are well fitted to equation (5.10) with the parameters listed in Table 5.4. The dependences of the extracted characteristic time, τ, and β on RH are shown in Figure 5.24(b) where τ decreases with increasing RH while β increases slightly. The stretching parameter β obtained from the fits, is between 0.41 and 0.53, and is comparable to those values obtained from pentacene with PS as the dielectric which are around 0.41-0.43 [86] and 0.55-0.63 [81]. It is also worth noting that the trapping time, τ, values are significantly lower than those previously reported by the same approach for a TFT based on pentacene with a PS/Al_2O_3 dielectric (1.5 x 10^8 s) [86] and a PS-SiO_2 dielectric (3.2 x 10^5 s to 21.0 x 10^6 s) [81]. However, these authors fitted their data using a stretched exponential equation of the form $I_D(t)/I_D(0) = exp\left(-\frac{t}{\tau}\right)^{\beta}$. By applying a similar approach to fit our

data, the trapping time, τ ranges from 10^4 s to 10^5 s. In other words, the stretched exponential based on the assumption that $V_T(\infty) = V_G$, can easily overestimate the value of the trapping time, τ.

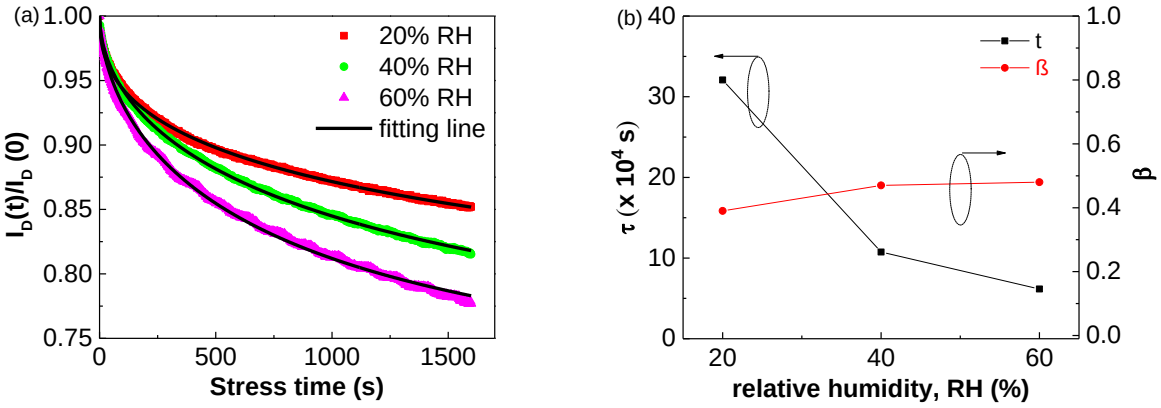

Figure 5.24 (a) Evolution of the drain current during bias stress at V_D = V_G = -40 V over 1600 s for different relative humidity. The solid lines in (a) represent the fits made to the data using equation (5.10) with the parameters listed in Table 5.4. (b) Plots of τ and β as a function of RH%.

Table 5.4 Parameters fits of equation (5.10) to the normalized current decay $I_D(t)/I_D(0)$ data in Figure 5.24(a) under bias stress of $V_G = V_D$ = -40 V and with $\Delta V_T(\infty)$ assumed equal to 4.09 V

RH%	***τ* (s)**	***β***	***V_T* (0) (V)**	**$\lvert \Delta V_T(\infty) \rvert$ (V)**	***R^2***
20	32 080	0.39	-26	4.09	0.99722
40	10 750	0.47	-26	4.09	0.99956
60	6169	0.48	-26	4.09	0.99919

We had showed previously [37] that the effect of RH on the DoS was minimal with the plots obtained for all relative humidities coalescing to a single curve over most of the range. In the present results, (Figures 5.25(a) and 5.25(b)) weak features were observed in the deeper states at all RH similar to the DoS obtained with bias stress measured in lab environment (50%-70% RH). This indicates that removing moisture during the bias stress does not change the behavior of the DoS in the DNTT film.

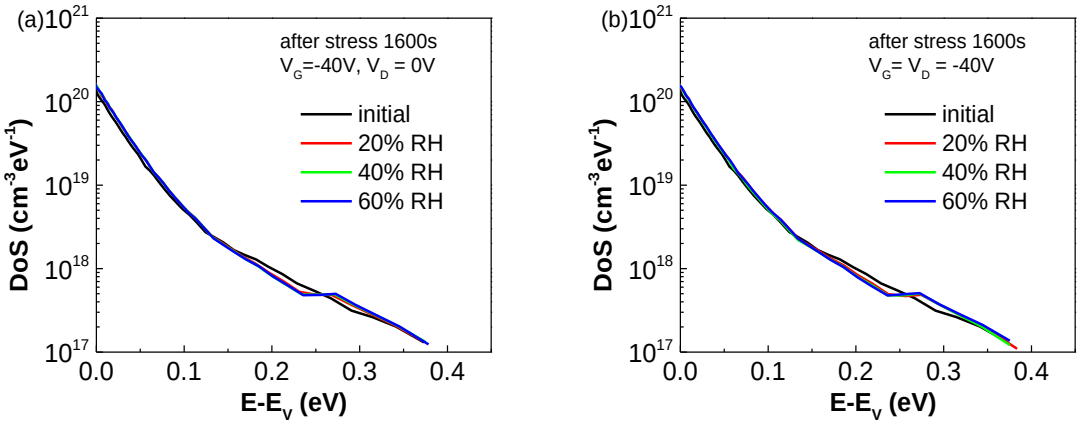

Figure 5.25 DoS as a function of E-E_V before and after stress conditions of (a) V_G = -40V, V_D = 0 V and (b) V_D = V_G = -40V obtained at relative humidity 20%, 40% and 60%.

5.2.6 Effect of Temperature on Bias Stress Induced Instability

It has been shown already [37] that temperature strongly influences the threshold voltage, V_T, and mobility, μ. Here the combination of bias stress and temperature is investigated. Measurements were performed in a climatic chamber, at a constant relative humidity of 20 % with temperature varying from 20 ºC to 60 ºC in 10 ºC step. Prior to each measurement, the test device was held at the set conditions for 30 min to come into equilibrium with the test environment. The initial transfer characteristic was measured at T = 20 ºC and RH = 20%. Then, the device was subjected to bias stresses of V_G = -40 V, V_D = 0 V and V_D = V_G = -40V, over the temperature range 20 ºC to 60 ºC for 1600 s. Between consecutive measurements, the device was illuminated for a few seconds to fully recover V_T to the initial state. The transfer characteristics were measured at the end of stressing. Figures 5.26(a) and 5.26(b) show the evolution of the transfer characteristics measured with V_D = -1 V, as temperature increased. It is observed that the transfer curves under negative gate bias shift negatively with increasing temperature.

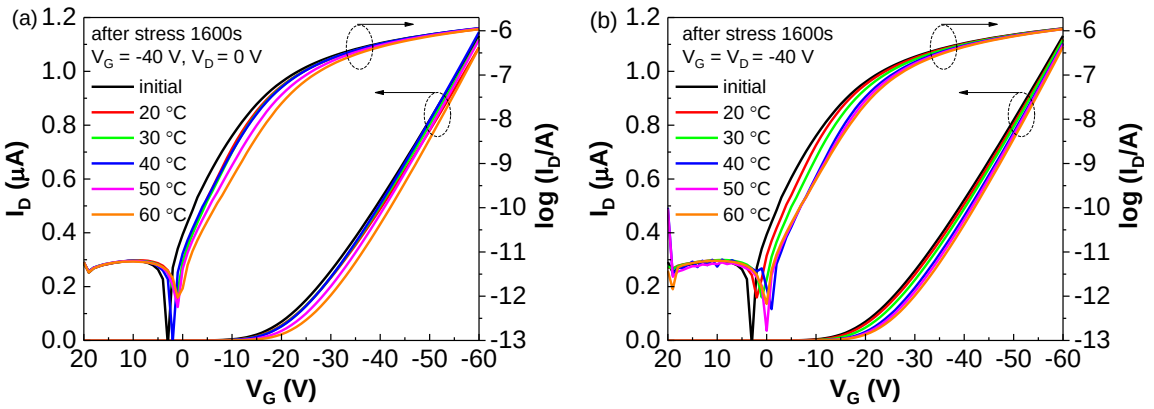

Figure 5.26 Transfer characteristics for stress conditions of (a) V_G = -40 V, V_D = 0 V and (b) V_D = V_G = -40 V at temperature ranging from of 20 ºC to 60 ºC.

Figure 5.27(a) and 5.27(b) show the shifts in threshold voltage, ΔV_T and turn-on voltage, ΔV_{ON} as a function of stress temperature. It can be observed that bias stress has a greater effect on ΔV_{ON} than on ΔV_T which only show a slight increase at all temperatures. Unlike the humidity the case, the effect of drain voltage was minimal.

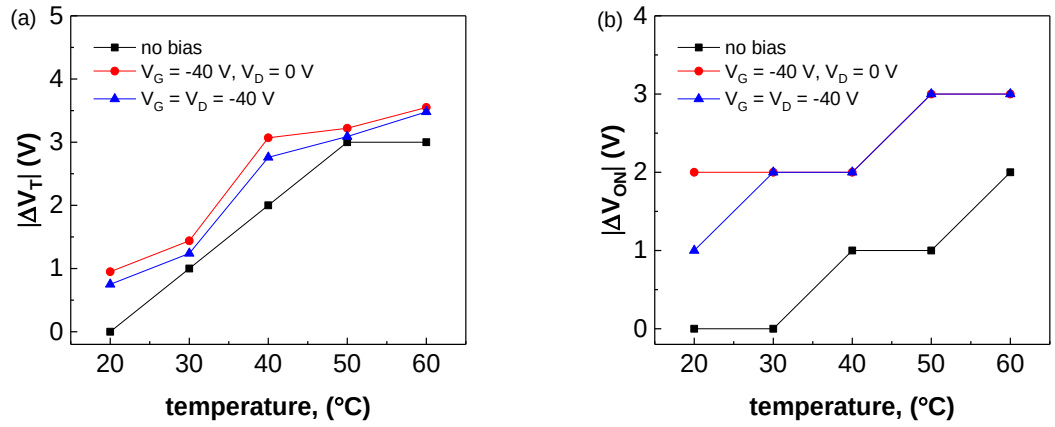

Figure 5.27 Dependence of (a) ΔV_T and (b) ΔV_{ON} on temperature without bias and under bias stress of V_G = V_D = -40 V and V_G = -40 V, V_D = 0 V over 1600s.

Figures 5.28(a) and 5.28(b) show the gate-voltage-dependent mobility plotted at different temperatures. It is observed that the maximum mobility increases with increasing

temperature. A similar dependency of mobility with temperature was also observed in the absence of bias stress as seen in the inset of Figure 5.28(a). However, in the absence of bias stress, the initial rate of rise is similar at all temperatures while under bias stress the plot shifted to more negative V_G, which is consistent with the shift in flat-band voltage.

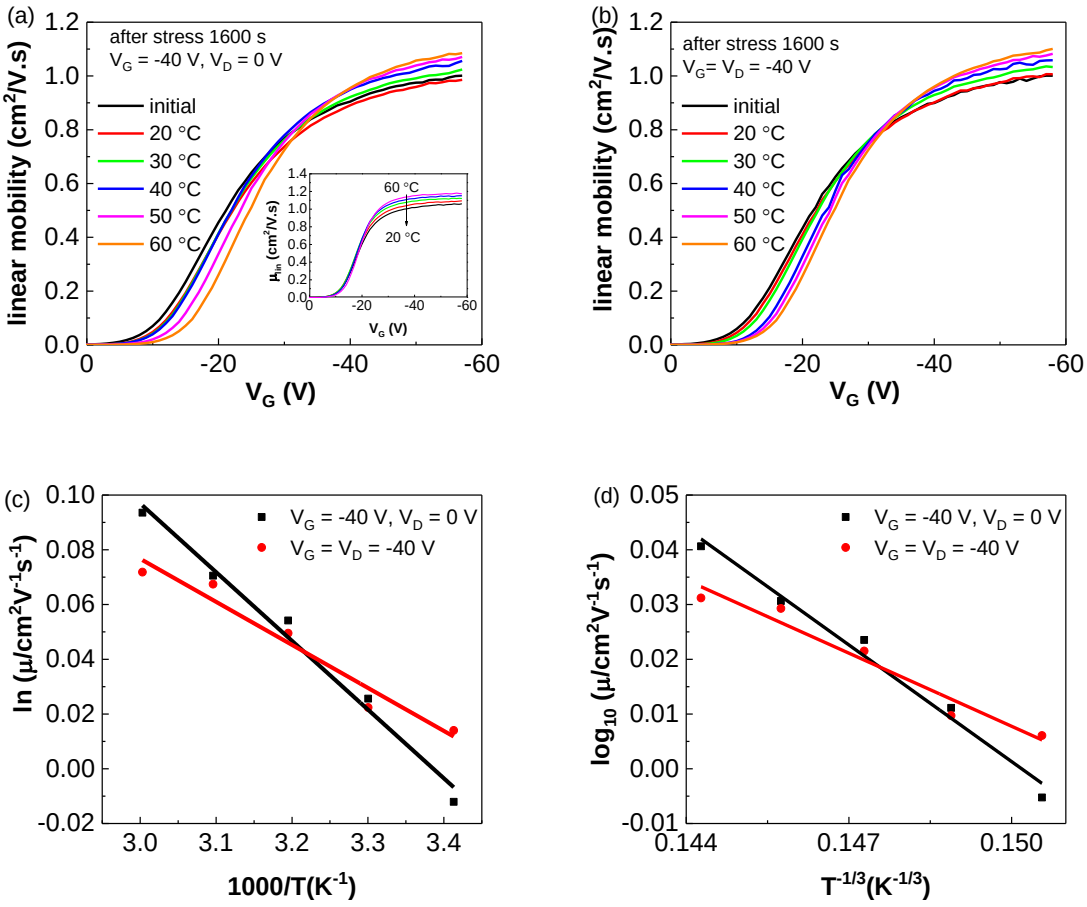

Figure 5.28 Gate-voltage-dependent mobility for stress conditions of (a) V_G = -40 V, V_D = 0 V and (b) V_D = V_G = -40 V obtained at temperature ranging from 20 ºC to 60 ºC. The inset shows the mobility without bias stress. (c) Arrhenius plot of mobility plotted in as a function of temperature and (d) as a function of $T^{-1/3}$. The solid lines in (c) are fits according to equation (5.18) while in (d) are fits to the 2-dimensional hopping conduction model.

Plots of *ln μ* as a function of reciprocal temperature, *1000/T* are shown in Figure 5.28(c) for the different stress conditions. It can be seen that under bias stress, the mobility exhibited an Arrhenius behaviour in the tested range of temperature given by [111] i.e.

$$\mu = \mu_0 exp\left(\frac{-E_a}{kT}\right) \tag{5.11}$$

where E_a is the activation energy. From the slopes of the curves, the activation energy, E_a is calculated to be between 21.5 meV and 13.8 meV and is significantly lower than reported by Guo for pentacene which is around 83-350 meV [111]. Our data are also consistent with a 2-D hopping conduction model of the form $\mu = \mu_0 exp\left[-(T_0/T)^{1/3}\right]$ as shown in Figure 5.28(d). However the extracted, T_0 were very low (T_0=155 K for V_G = -40 V, V_D = 0 V and T_0 = 40 K V_D = V_G = -40 V) compared to T_0 = 280 K presented in reference [37] and in Chapter 4.

To further explore the effect of temperature on the bias stress effect, the time dependence of the decay of drain current, I_D was tested under the bias stress condition V_D = V_G = -40 V. Figure 5.29(a) shows that the values of the normalized drain current, $I_D(t)/I_D(0)$ decreases as temperature increases. The solid lines in Figure 5.29(b) indicate that $I_D(t)/I_D(0)$ at 20 ºC to 60 ºC are well fitted to equation (5.10) with the parameter listed in Table 5.5. Unlike the situation for changing RH, the good fits here could only be obtained by adjusting $\Delta V_T(\infty)$ from 4.09 V to 7.29 V and decreasing τ by more than an order of magnitude over the temperature range from 20 ºC to 60 ºC. This suggests that, (a) the density of interfacial hole traps almost doubles over the temperature range, with little or no change in the distribution factor β, and (b) holes in the channel equilibrate faster with interface states at higher temperatures.

Table 5.5 Parameters fits of equation (5.10) to the normalized current decay $I_D(t)/I_D(0)$ data in Figure 5.29(a) under bias stress of V_G = V_D = -40 V.

C(º)	***τ* (s)**	***β***	***V_T* (0) (V)**	**$\Delta V_T(\infty)$ (V)**	***R^2***
20	29954	0.47	-24	4.09	0.99939
30	11220	0.45	-24	4.85	0.9997
40	5604	0.48	-24	5.64	0.99992
50	3750	0.47	-24	6.45	0.99903
60	3187	0.45	-24	7.29	0.9997

The magnitude of the trapping time, τ is significantly reduced as stress temperature increases from 20 ºC to 60 ºC suggesting that excitation from traps is an activated process is thermally activated i.e.

$$\tau = \tau_0 exp\left(\frac{E_\tau}{kT}\right) \tag{5.12}$$

where τ_0 is a characteristic trapping time and E_τ = 0.48 eV (Figure 5.29(b)) is the trapping activation energy. This value is slightly lower than literature values for organic TFTs based on SiO_2, which are usually in the range of 0.51-0.62 eV [80, 112]. These and our results suggest, unexpectedly perhaps, that a higher proportion of traps are empty at higher temperatures so that the mean time to trapping, which is inversely proportional to the density of available interface traps, decreases. This could be considered as being equivalent to, but difficult to separate from, a trap creation process.

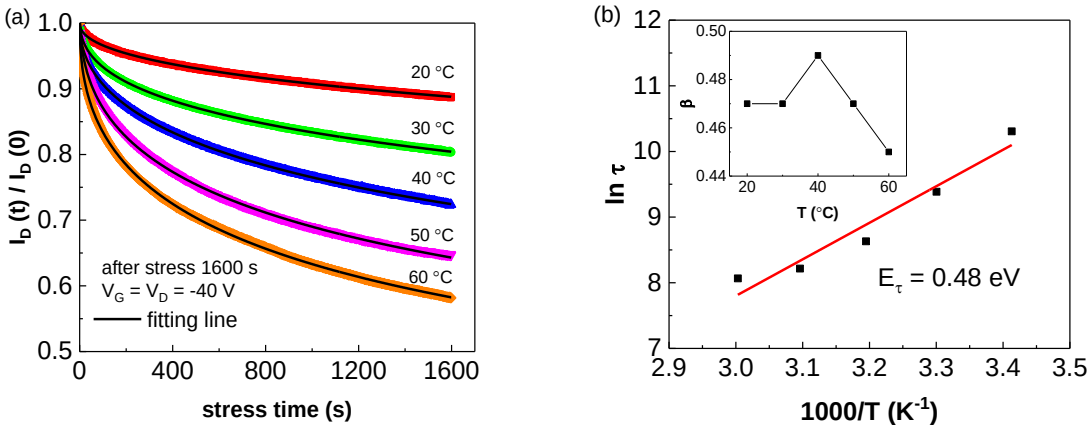

Figure 5.29 (a) Time-dependent normalised drain current decay for different temperatures with the stress condition of $V_G = V_D = -40$ V. The solid lines represent the fits made to the data using equation (5.10) with the parameter listed in Table 5.5. (b) Plots of τ and β as a function of temperature.

Figure 5.30(a) and 5.30(b) show the DoS as a function of E-E_V. The degradation of the subthreshold slope from 3.52 to 4.18 V/decade as temperature increases results in an increase in magnitude of the weak features and a shift to deeper energies. In addition, the distribution

of shallow states within ~100 meV of the mobility edge also changes. The fitted lines shown as the insets in Figure 5.30(a) and 5.30(b) are well described by the single exponential function as equation (5.1). The fit parameters are listed in Table 5.6. It can be seen that as temperature increases, the total trap density, N_t, appears to decrease slightly. This is consistent with the observation that at higher temperature more holes filled the trap state which in turn reduced the total trap density and thereby caused the hole mobility to increase slightly as shown in Figures 5.28(a) and (b).

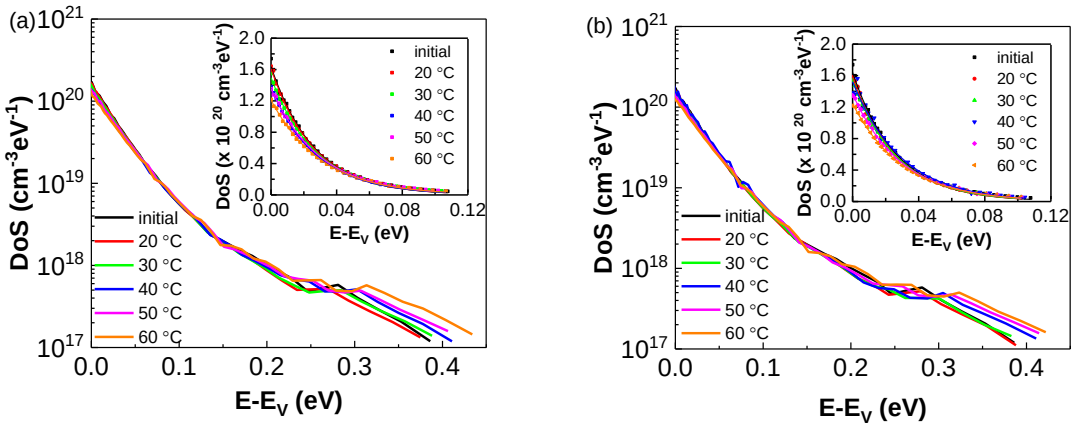

Figure 5.30 DoS as a function of E-E_V before and after stress conditions of (a) V_G = -40 V, V_D = 0 V and (b) V_D = V_G = -40 V under taken at temperatures ranging from 20 ºC to 60 ºC. The inset shows the shallow trap distribution on a linear scale. The solid lines represent an exponential fit made to the data using equation (5.1).

The characteristic slope exhibits a slight increase from E_t ~ 26.4 meV to E_t ~ 30.4 meV as temperature increases. These values are slightly lower than the characteristic energy E_t ~ 37 meV reported for pentacene-based field-effect transistors in the literature [103]. At higher temperature, the DoS also shows a slight increase in the energy range lying between 0.3 eV to 0.4 eV above *Ev*. This observation is related to the increase in subthreshold slope which showed an increase from 3.52 V/decade to 4.18 V/decade and from 3.73 V/decade to 4.25 V/decade under bias stress of V_G = -40 V, V_D = 0 V and V_G = V_D = -40 V respectively as the temperature increases.

In our previous report, [37] we had shown that at higher temperature, under short-circuit conditions, a slight increase in deeper states appeared between ~0.25 and ~0.35 eV above E_V. Similar features were also observed in the present results. In the shallow trap distribution, the bias stress increases slightly the characteristic energy E_t compared with just the effect of temperature as shown Figure 5.31(a), while decreasing slightly in the total trap density, N_t (Figure 5.31(b)). This suggests that bias stress has a minimal effect compared with effects related to temperature alone.

Table 5.6 Extracted total trap density, N_t and characteristic energy decay of the distribution, E_t

T	***N*$_t$ (x 10^{18} cm^{-3})**		***E*$_t$ (meV)**	
(ºC)	V_D=0V,V_G=-40V	V_D=V_G=-40V	V_D=0V,V_G =-40V	V_D=V_G=-40V
20	4.25	4.18	26.42	26.43
30	4.08	4.15	27.37	27.09
40	3.83	3.87	28.14	29.39
50	3.95	3.97	29.23	29.21
60	3.68	3.77	30.43	30.40

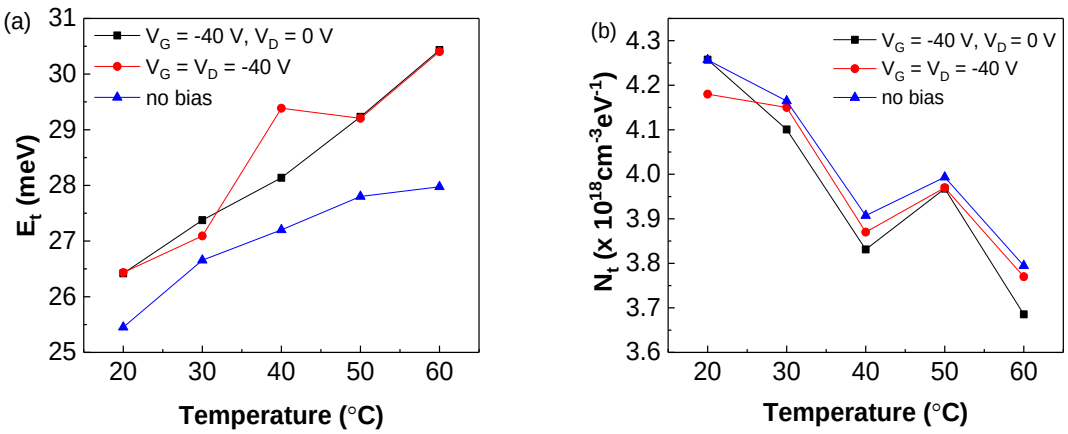

Figure 5.31 Dependence of (a) E_t and (b) N_t on temperature without bias and under bias stress of V_G =V_D = -40 V and V_G = -40 V, V_D = 0 V over 1600s.

5.3 Positive Bias Stress Instability in PS-DNTT

The effect of positive bias stress on the electrical performance of a PS-DNTT TFT was investigated by measuring the transfer characteristics in the dark before and after stressing. In this case, the initial state was achieved by applying negative bias stress to fully recover to the initial state from the previous stressing. Figure 5.32(a), shows the evolution of the transfer characteristics as a function of stress time. The extracted parameters are listed in Table 5.7. The application of positive bias stress of V_G = 30 V and V_D = 0 V for 2500 s shifted the curves toward more positive voltage. It is observed throughout the stress period, that the subthreshold region continues to shift positively while the subthreshold slope degrades. However, at higher currents, i.e. above threshold voltage no further shift occurred as seen in the linear characteristics in Figure 5.32(a). The gate-voltage dependent mobility remained unchanged by positive voltage stressing as shown in Figure 5.32(b).

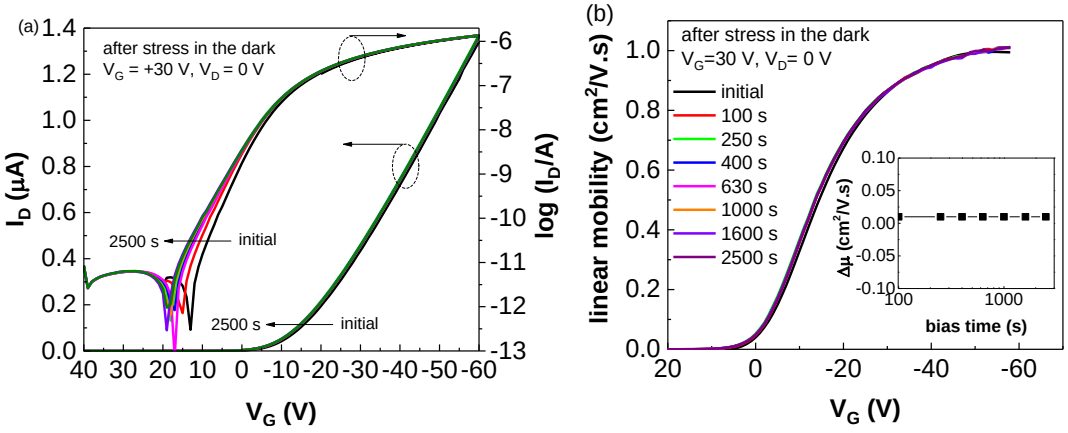

Figure 5.32 (a)Transfer characteristics and (b) gate-voltage dependent mobility after bias stress at V_G = +30 V and V_D = 0 V for stress times up to 2500 s. The inset in (b) shows the change in the maximum mobility as bias stress time increases.

The shift of threshold voltage ΔV_T is shown as a function of stress time in Figure 5.33(a). ΔV_T is only slightly affected by the stress which is caused by electrons trapping at the interface between semiconductor and insulator. The red line in Figure 5.33(a) indicates that the time dependence of ΔV_T can be described by the stretched-exponential function given by equation (5.2). The positive bias stress is found to significantly reduce the threshold voltage

shift for times approaching infinity. Now $\Delta V_T(\infty)$=1.76 V. which is significantly lower than for negative bias stress. The characteristic trapping time, τ at 0.52 x10^3 s is also significantly reduced compared to the value obtained with negative bias stress under ambient conditions.

As seen in Figure 5.33(b), the shift in turn-on voltage ΔV_{ON} is much greater than for ΔV_T with increasing stress time. The red line in Figure 5.33(b) indicates that the time dependence of ΔV_{ON} is also well fitted by a stretched exponential function. Interestingly, the maximum shift in turn-on voltage shift expected for times approaching infinity was significantly higher $\Delta V_{ON}(\infty)$= 6.0 V, than the threshold voltage $\Delta V_T(\infty)$. This may be explained by the fact that trapped electrons were neutralized when the gate voltage sweeps towards negative voltage as more holes were induced in the channel, thus suppressing ΔV_T above the subthreshold region.

Table 5.7 Device parameters extracted from the transfer characteristics after stress conditions of V_G = +30 V and V_D= 0 V in the dark. Characteristics were obtained with V_D = -1 V, at T = 20ºC and 10% RH.

Time	V_T **(V)**	V_{ON} **(V)**	μ_{lin} **(cm²/V.s)**	***SS*** **(V/decade)**	I_{ON}/I_{OFF}
Initial	-16.8	11	1.00	4.19	3.80 x 10^5
100 s	-16.4	14	0.99	5.43	3.79 x 10^5
250 s	-16.1	16	0.99	5.51	2.46 x 10^5
400 s	-15.8	16	0.99	5.54	2.48 x 10^5
630 s	-15.5	16	0.99	5.54	2.49 x 10^5
1000 s	-15.2	17	0.99	5.57	2.43 x 10^5
1600 s	-15.1	17	0.99	5.60	2.40 x 10^5
2500 s	-15.0	17	0.99	5.60	2.42 x 10^5

The increase of subthreshold slope is shown as a function of stress time in Figure 5.33(c) and is reflected in the systematic increase in the density of the deeper states in the range 0.15 ≤ (E-E_V) ≤ 0.4 eV as shown in Figure 5.33(d). Kalb et al [103] have described the degradation in subthreshold slope as being due to the deep traps, which is reflected in a broad peak in the of DoS plot, and cause a reduction in the field-effect mobility. However there is no change in mobility observed in our case. Therefore, it is unlikely that the change in the subthreshold slope is due to the creation of deep trap states in the band gap of DNTT.

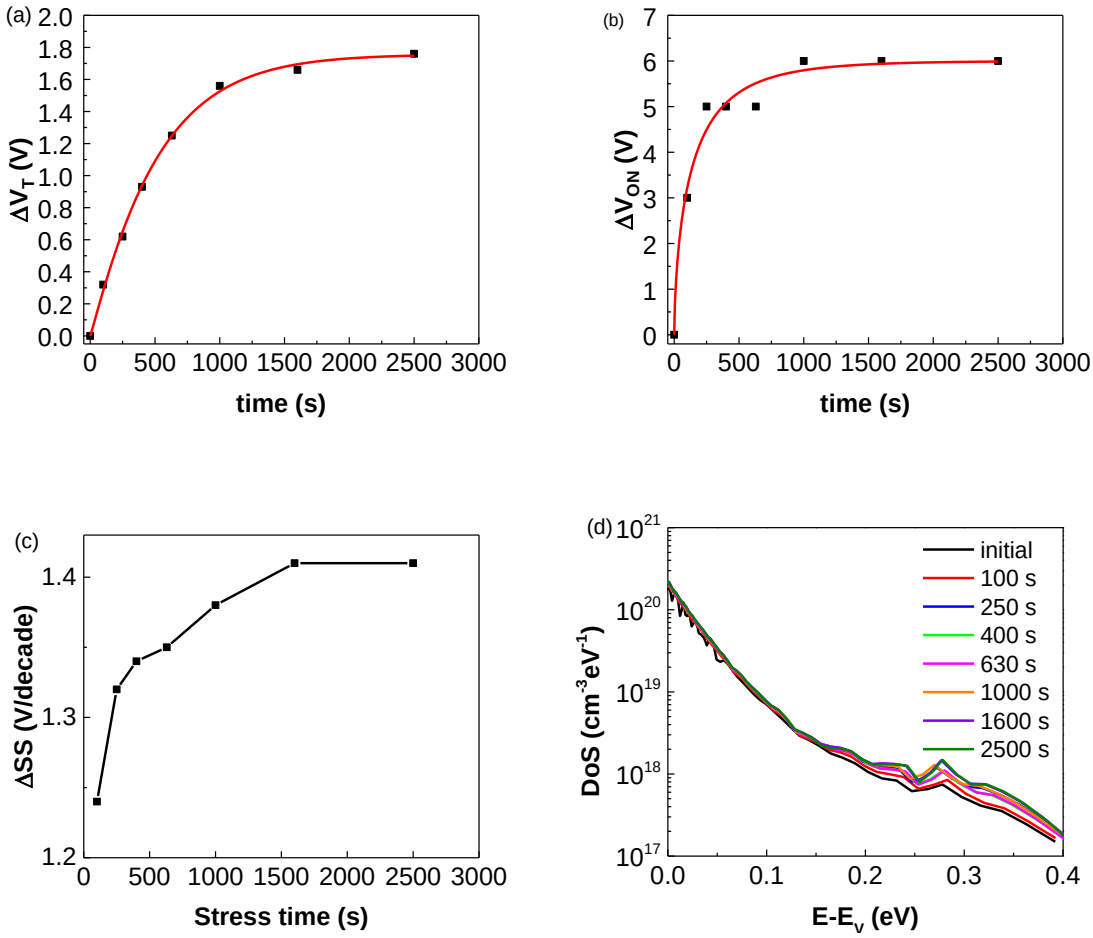

Figure 5.33 (a) Shift of threshold voltage, (b) turn-on voltage and (c) subthreshold slope as a function of stress time. (d) The DoS distribution as a function of E-E_V before and after stress conditions of V_G = +30 V and V_D = 0 V.

5.4 Summary

In this chapter, effects of bias stress in OTFTs based on PS-DNTT over a range of temperature and relative humidity were investigated. It has been shown that ΔV_T and ΔV_{ON} shifted negatively under negative gate bias stress due to interface hole trapping. The greatest effect was observed when stressing in the linear rather than the saturation regime. This is because when stressing in the saturation regime, the hole concentration towards the drain end of the channel is decreased which leads to a reduction in the number of charge carriers

available for trapping towards the drain end of the channel. The time-dependence of ΔV_T in both linear and saturation regimes are well described by a stretched exponential time-dependence. Contrary to most previous reports, the threshold voltage at long times, $V_T(\infty)$, asymptotes to a value that is far lower than the applied gate voltage. This suggests that the interface trap density in this devices is sufficiently low which limits the extent of any change in flat-band voltage.

The different trajectories of the drain current decay in successive measurements indicate that that the initial V_T does not recover exactly the initial interface conditions. This suggests that device relaxation may not result entirely from hole detrapping but also due to interface trapping of electrons. Exposure to increasing relative humidity and temperature lead to slight changes in both ΔV_T and ΔV_{ON}. The DoS in the DNTT film does not change upon reducing RH. However, a slight increase in the deeper state was observed as temperature increases.

It has been shown that ΔV_T and ΔV_{ON} shifted positively under positive gate bias stress due to electron trapping at the interface. However, changes in ΔV_{ON} with increasing stress time is much greater than for ΔV_T. This is believed due to neutralization of trapped electrons as the gate voltage sweeps towards negative voltage. The increase in the subthreshold slope that is reflected in the density of state is unlikely due to the creation of deep trap states in the DNTT but rather due to changing occupancy of interface states, thereby changing the flat-band voltage.

6 Photo-induced Effects in PS-DNTT Thin Films Transistors

6.1 Introduction

In this chapter, the effect of illumination on PS-DNTT transistors is investigated and discussed. The response to different wavelengths is described first. The influence of electron or hole trapping was identified by monitoring changes in the transfer characteristics during and after illumination. The effect of intensity on the electrical performance was also investigated. Lastly, the dynamic responses under positive and negative bias stresses are discussed in detail.

6.2 Results

6.2.1 Effect of Monochromatic Wavelength

The effect of monochromatic illumination on the electrical performance of a DNTT-TFT was investigated by measuring the transfer characteristics in the dark and then under illumination. From the UV-Vis spectra of DNTT, it is known that the absorption peak is in the ultraviolet and blue region [97, 98]. In this work, wavelengths covering the visible region were used. The device characteristics were obtained at 460 nm; 0.31 mW/cm^2, initially, then at 520 nm; 0.31 mW/cm^2, 570 nm; 0.31 mW/cm^2, 600 nm; 0.33 mW/cm^2 and 630 nm; 0.35 mW/cm^2. The response of the device to the illumination was obtained (a) under illumination and (b) in the dark after a 10 min light soaking during which the source, drain and gate electrodes were grounded.

Figure 6.1(a), 6.1(b), 6.1(c) and 6.1(d) show the evolution of the transfer characteristics on linear and log scales during forward (20 V to -60 V) and reverse sweeps (-60 V to 20 V) with V_D = -1 V recorded during illumination and in the dark after illumination . It can be observed that the transfer characteristics exhibit a parallel shift towards more positive voltages regardless of the wavelength. However, at 460 nm the shifts are much larger resulting in large increases in the on-current, I_{ON}, especially in the subthreshold region where significant changes in subthreshold slope, *SS* also occur.

The insets of Figures 6.1(a) and 6.1(c) show that, the gate-voltage-dependent mobility curves move in parallel. There is no significant change in in the maximum mobility observed. Clockwise hysteresis is observed in this device both during and after illumination as indicated by the arrows. The biggest hysteresis was observed under 460 nm illumination.

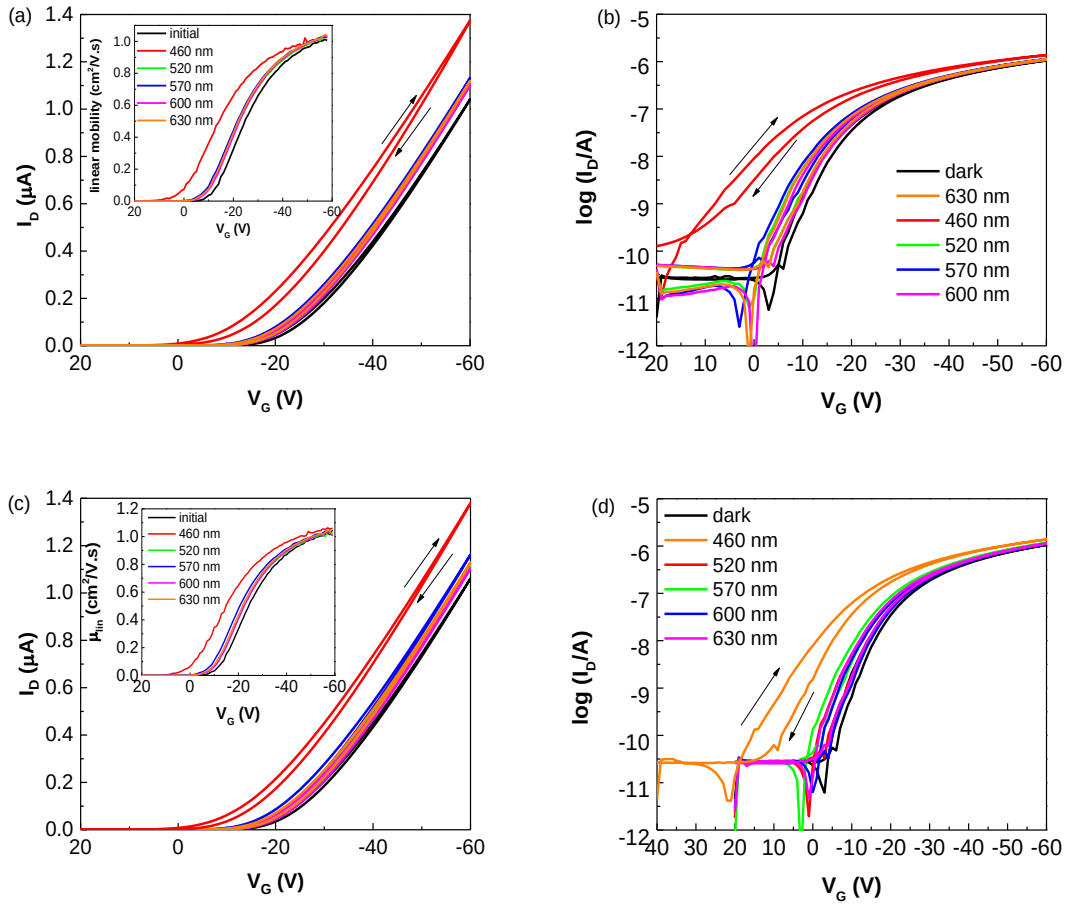

Figure 6.1 Transfer characteristics plotted on (a) linear and (b) semi-log scales for an illuminated device and in the dark after 10 min illumination on (c) linear and (d) semi-log scales. The intensity at different wavelengths varied in the range 0.31 to 0.35 mW/cm^2. Insets in (a) and (c) show the corresponding linear mobility as a function of gate voltage.

To make comparison easier, the results for 460 nm are replotted in Figure 6.2. Figure 6.2(b) shows that the semi-log I_D-V_G characteristic under 460 nm illumination in the forward sweep follows the characteristic after illumination. However during the return sweep, I_D under illumination departs from the reverse sweep post-illumination plot as the former asymptotes

to a higher off-current of ~ 10^{-10} A. The post-illumination plot returns to the original off-current of ~ 2 x 10^{-11} A.

The gate-voltage-dependent mobility obtained during and after illumination is shown in the inset of Figure 6.2(a). Both measurements exhibit a similar initial rate of rise in the forward and reverse sweeps as reflected in the linear plot of I_D-V_G in Figure 6.2(a). However, during the reverse voltage sweeps, the maximum mobility obtained at V_G = -60 V was slightly higher than seen in the forward voltage sweep. No shift is observed between the plots obtained during and after illumination.

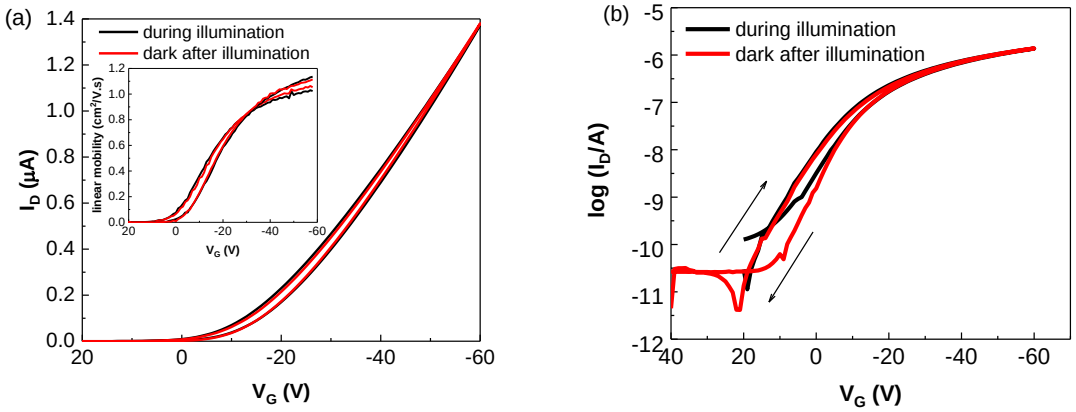

Figure 6.2 (a) Transfer characteristics plotted on (a) linear and (b) semi-log scales obtained during illumination and after illumination at wavelength 460 nm. The inset in (a) shows the corresponding linear mobilities as a function of gate voltage.

The changes in ΔV_T and ΔV_{ON} during and after illumination shown in 6.3(a) are consistent with interface electron trapping. In both cases, the largest changes were obtained at 460 nm. It is also worth noting that ΔV_{ON} was significantly higher than ΔV_T. The change in the effective interface trapped charge density, ΔN_{it} can be estimated from $\Delta N_{it} \approx \frac{1}{q} C_{ins} \Delta V_{ON}$. The largest shift in ΔV_{ON} suggests an effective electron trap density of 3.30 x 10^{11} cm^{-2} (Figure 6.3(b)). After illumination, an effective interface trap density of 3.55 x 10^{11} cm^{-2} corresponding to ΔV_{ON} = 24 V still remains in the device. The changes in subthreshold slope, ΔSS, during and after illumination are shown as an inset in Figure 6.3(b). The largest changes

obtained with 460 nm during illumination were comparable (4.1 V/decade) with the one obtained after illumination (3.8 V/decade).

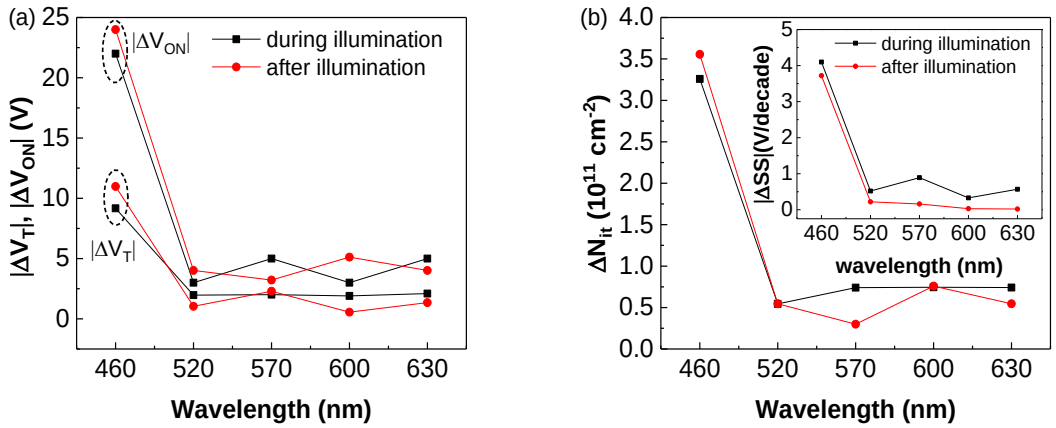

Figure 6.3 (a) Shift of threshold voltage, ΔV_T and turn-on voltage, ΔV_{ON} and (b) density of trapped charges, ΔN_{it} from ΔV_{ON} at the interface obtained during and after illumination. Inset of Figure (b) shows the change in subthreshold, ΔSS. The intensity at different wavelength varied from 0.31 to 0.35 mW/cm^2.

In Figures 6.4(a) and (b), the post-illumination transfer characteristics for 520 nm are shifted by an amount equal to either ΔV_{ON} or ΔV_T from the dark. It can be observed that, shifting the post-illumination semi-log transfer characteristics in the forward and reverse sweeps by an amount ΔV_{ON}, reproduced the dark characteristics with only minimal change in shape in the subthreshold region. Shifting the linear transfer plot by ΔV_T, showed almost no change at all. The situation is very different for 460 nm illumination (see Figures 6.4(c) and (d)). Now, shifting the semi-log transfer characteristics obtained in either forward or reverse gate voltage sweeps by an amount equal to ΔV_{ON} does not reproduce the dark characteristic and a significant change occurs in the subthreshold slope. Interestingly, though, above the subthreshold region, the post-illumination characteristics reproduce the dark characteristics after shifting the plots by an amount equal to ΔV_T.

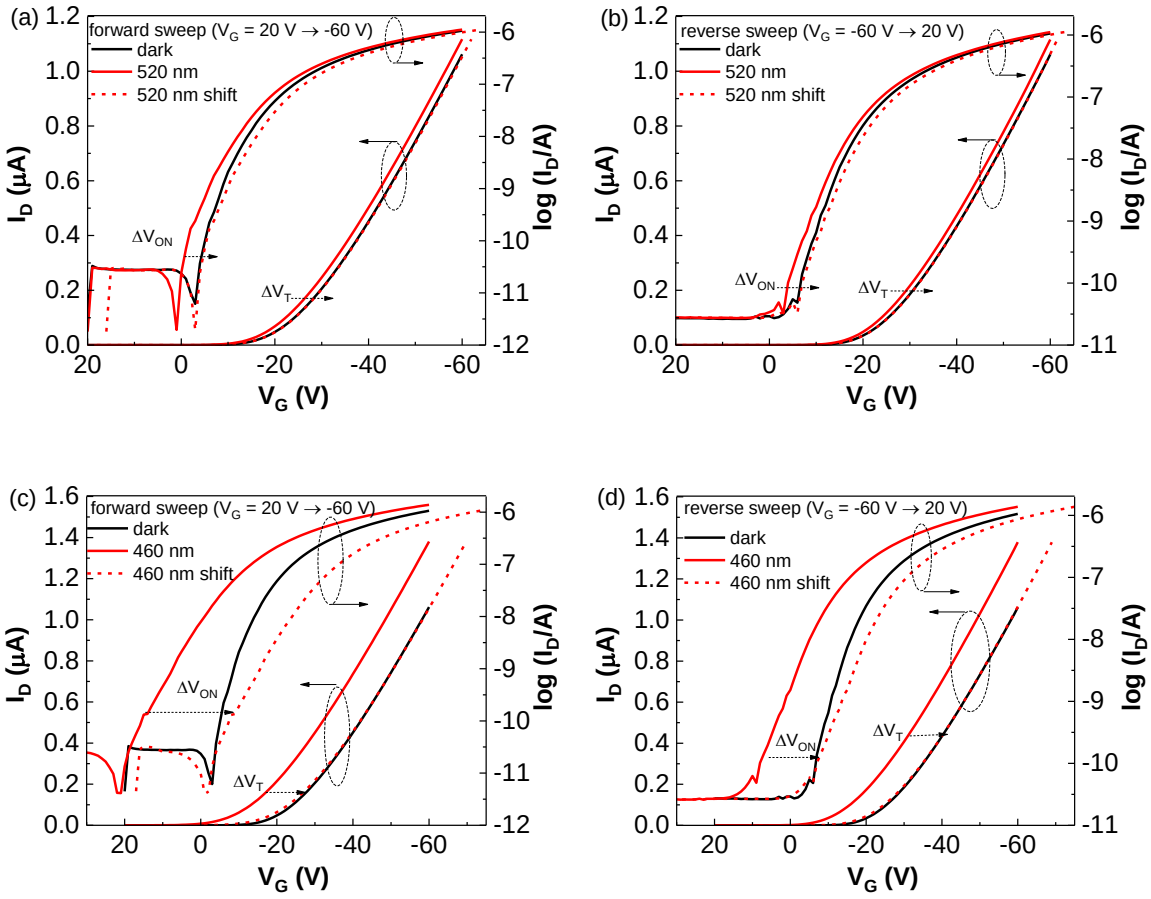

Figure 6.4 Transfer characteristics in linear and semi-log scales recorded after illumination at 520 nm during (a) forward and (b) reverse gate voltage sweeps and at 460 nm during (c) forward and (d) reverse gate voltage sweeps. The dashed lines correspond to the illuminated characteristics shifted by an amount equal to the difference ΔV_{ON} and ΔV_T from the dark. The intensity for both wavelengths is 0.31 mW/cm^2.

6.2.1.1 Photosensitivity and photoresponsivity

The photosensitivity, P and photoresponsivity, R of a phototransistor are usually expressed as:

$$P = \frac{I_{D(light)} - I_{D(dark)}}{I_{D(dark)}} \tag{6.1}$$

$$R = \frac{I_{D(light)} - I_{D(dark)}}{P_{opt}.A} \tag{6.2}$$

where $I_{D(light)}$ and $I_{D(dark)}$ are the drain currents obtained under illumination and in the dark respectively and P_{opt} is the measured power of the incident light per unit area and A is the effective device area (channel width x channel length) [89, 91]. Plots of photosensitivity, P, versus gate voltage, V_G, at different wavelength, λ, during and after illumination are shown in Figure 6.5(a) and 6.5(b) respectively. The highest value of ~10^4 occurs at 460 nm and is two orders of magnitude greater than at any other wavelength. On the other hand, for λ > 460 nm only limited photoresponse is observed.

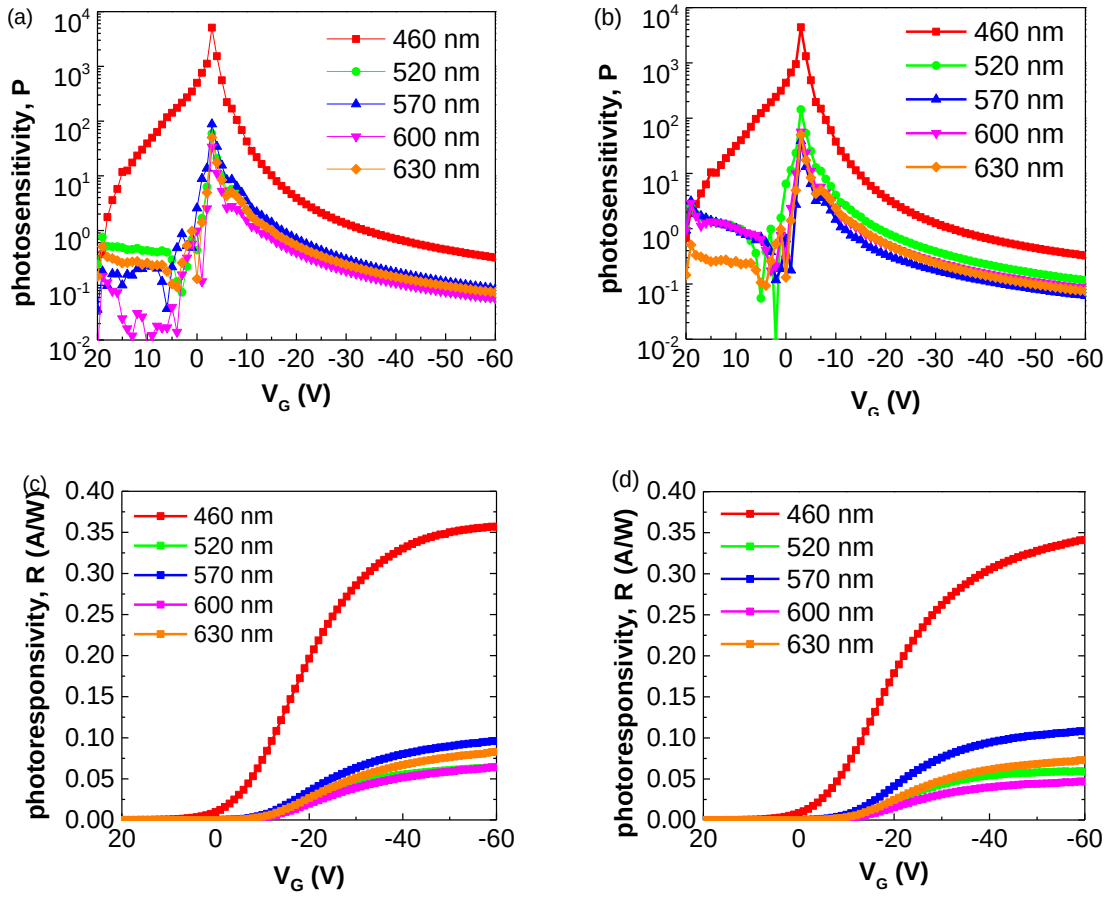

Figure 6.5 Photosensitivity, P, of PS-DNTT OTFT as a function of V_G obtained (a) during illumination and (b) after illumination. Photoresponsivity, R, of PS-DNTT OTFT obtained (c) during illumination and (d) after illumination.

It is also observed that at all wavelengths, a maximum occurs in the photosensitivity at V_G = -3.0 V close to the turn-on voltage, V_{ON}, of the non-illuminated device. As V_G sweeps to

more negative voltages, *P* is reduced due to a comparable number of photogenerated and field-induced charge carriers in the channel. A plot of photoresponsivity, *R*, versus gate voltage for different wavelengths (Figure 6.5(c) and 6.5(d)) shows that *R* increases rapidly to a maximum value of 0.35 A/W when the transistor is fully turned on.

Figures 6.6(a) and 6.6(b) compare values of *P* and *R* obtained at 460 nm during the forward gate voltage sweep (V_G = 20 V to -60 V) with corresponding values from the reverse gate voltage sweep (V_G = -60 V to 20 V) in. The maximum *P* obtained in the forward sweep is slightly higher than in the reverse sweep. For voltages more positive than 15 V, the magnitude of *P*, in the reverse sweep, during illumination was enhanced. This is consistent with the increase in the off-state drain current (Figure 6.2 (b)) and arises from the photoconduction effect. The photoresponsivity, *R*, in the reverse sweep for both cases decreases from the maximum value yielding lower values at all gate voltages.

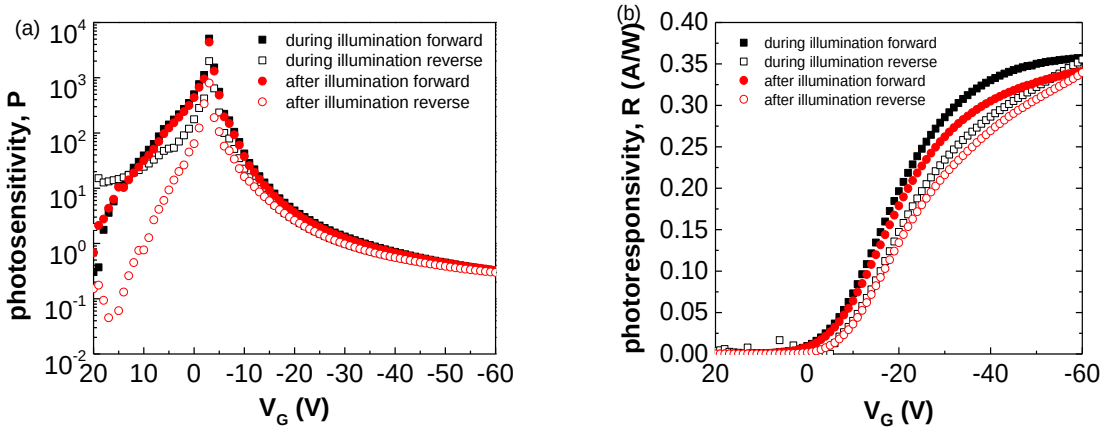

Figure 6.6 (a) Photosensitivity, *P* and (b) photoresponsivity, *R* of PS-DNTT OTFT in the forward gate voltage sweeps (V_G = 20 V to -60 V) and reverse gate voltage sweeps (V_G = -60 V to 20 V) obtained during and after 460 nm illumination.

6.2.1.2 Density of States

Changes observed in the subthreshold region of the transfer characteristics indicates the possibility that illumination has created new band gap states in the DNTT. To investigate this possibility, the DoS in the illuminated PS-DNTT TFT was extracted by applying the Grünewald model to transfer plots obtained in the linear regime. Figures 6.7(a) and (b)

display the DoS for different wavelengths. For λ > 460 nm the plots show almost identical distribution with only a slight increase in the deeper states between ~0.10 and ~0.35 eV above E_V. The DoS distribution obtained during 460 nm illumination exhibits a clear increase in deep trap states between ~0.15 eV and ~0.35 eV above E_V, reflecting the changes in subthreshold slopes in Figure 6.4(c) Similar DoS distributions were also observed after illumination.

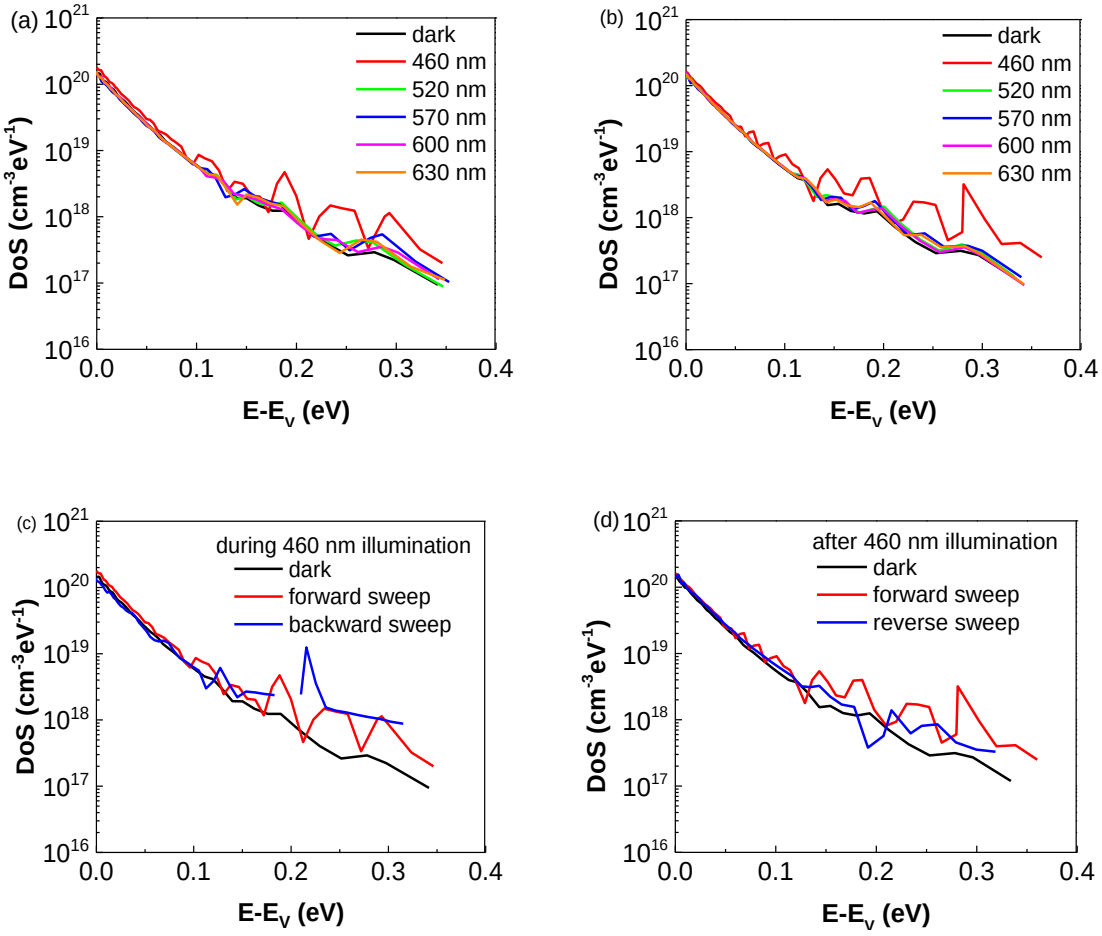

Figure 6.7 DoS distribution obtained (a) during illumination and (b) in the dark after a 10 min illumination. Comparison of DoS in the forward and reverse gate voltage sweeps obtained (c) during illumination and (d) after illumination.

A comparison of DoS between forward and reverse sweep obtained during 460 nm illumination is shown in Figure 6.7(c). It can be seen that there is a discontinuity in the DoS in the reverse sweep which arose because of the uncertainty in determining the exact value

of V_{ON} as shown in figure 6.2(b). However, the post-illumination DoS during the reverse sweep slowly decreases and almost returns to its initial dark distribution (Figure 6.7(d)).

6.2.2 Effect of Monochromatic Light Intensity

In this section, the effects of illumination intensity for fixed wavelength ranging from 460 nm to 630 nm are presented. Here we only focus on the device characteristics obtained in the dark after 10 mins of exposure to illumination. The intensity at each wavelength was adjusted by controlling the exit slit of the monochromator, which slightly broadened the spectrum falling on the device. The irradiance power at each wavelength was varied from 0.05 mW/cm^2 to 0.49 mW/cm^2.

Figure 6.8 shows the transfer characteristics obtained in forward sweeps (V_G = 40 V to -60 V) plotted in (a) linear and (b) semilog scales respectively. As the intensity increased, the transfer characteristics shifted to more positive voltage regardless of the wavelength. This suggests that electron-hole pair generation and subsequent interface electron trapping occurs even at wavelengths corresponding to weak absorption in DNTT i.e for λ>500 nm. Not surprisingly, the largest shift occurred at λ = 460 nm corresponding to the peak absorption in DNTT.

Figures 6.9 show that the shifts, (a) ΔV_T in threshold voltage, (b) ΔV_{ON} in turn-on voltage and (c) ΔSS in subthreshold slope, increased with increasing intensity. At 460 nm, ΔV_T, ΔV_{ON}, and ΔSS increased much more rapidly than at longer wavelengths, but tended to saturate at higher intensities. For all wavelengths, the maximum mobility barely changed as shown in Figure 6.9(d) suggesting that neither the morphology nor the structure of the DNTT is affected even at the highest light intensity.

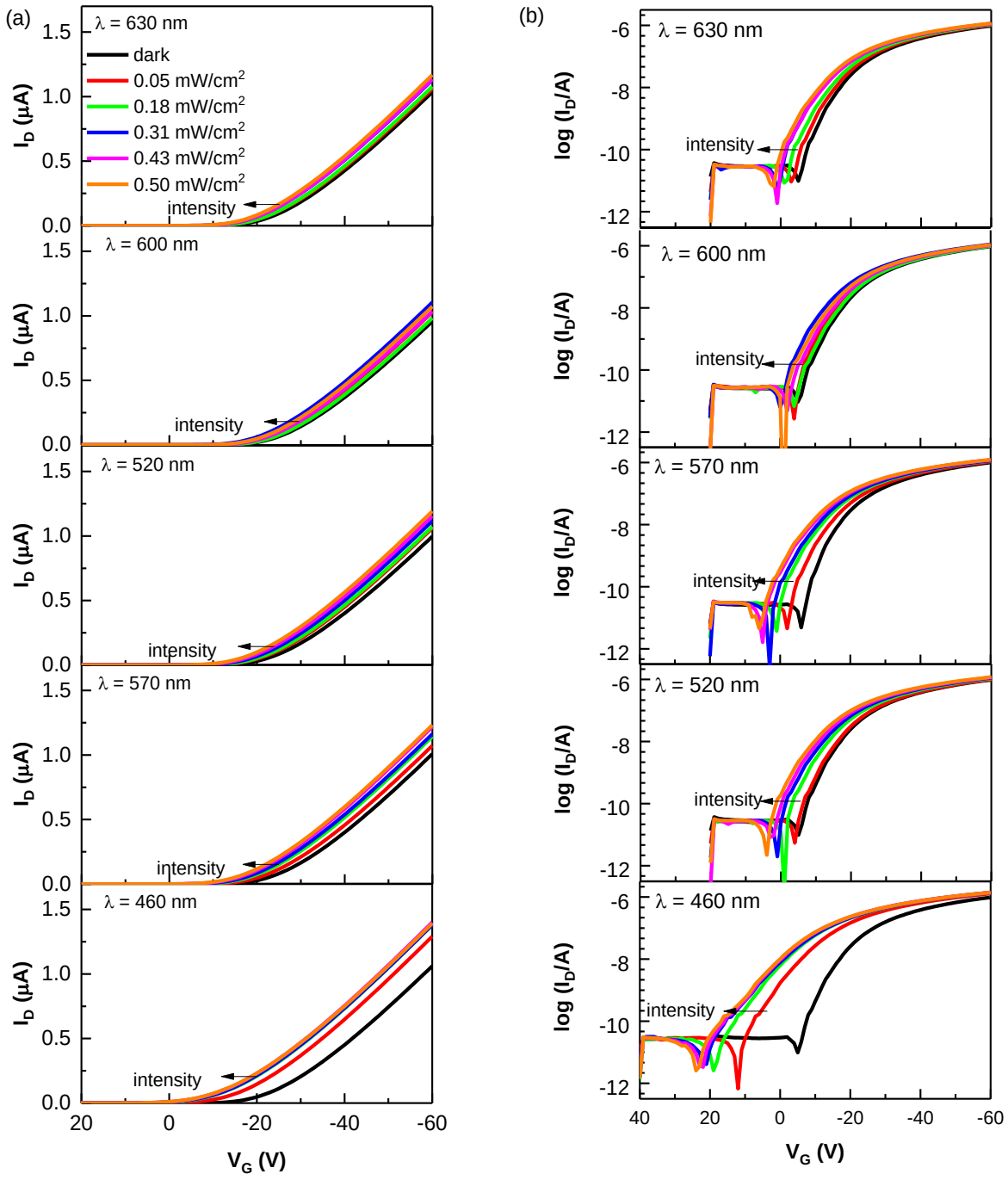

Figure 6.8 Effect of different light intensities on the forward transfer characteristics measured in the dark after a 10 min illumination during which the source, drain and gate electrodes were grounded. Transfer characteristics were recorded with gate voltage sweep from 20V to -60V and are plotted on both (a) linear and (b) semilogarithmic scales.

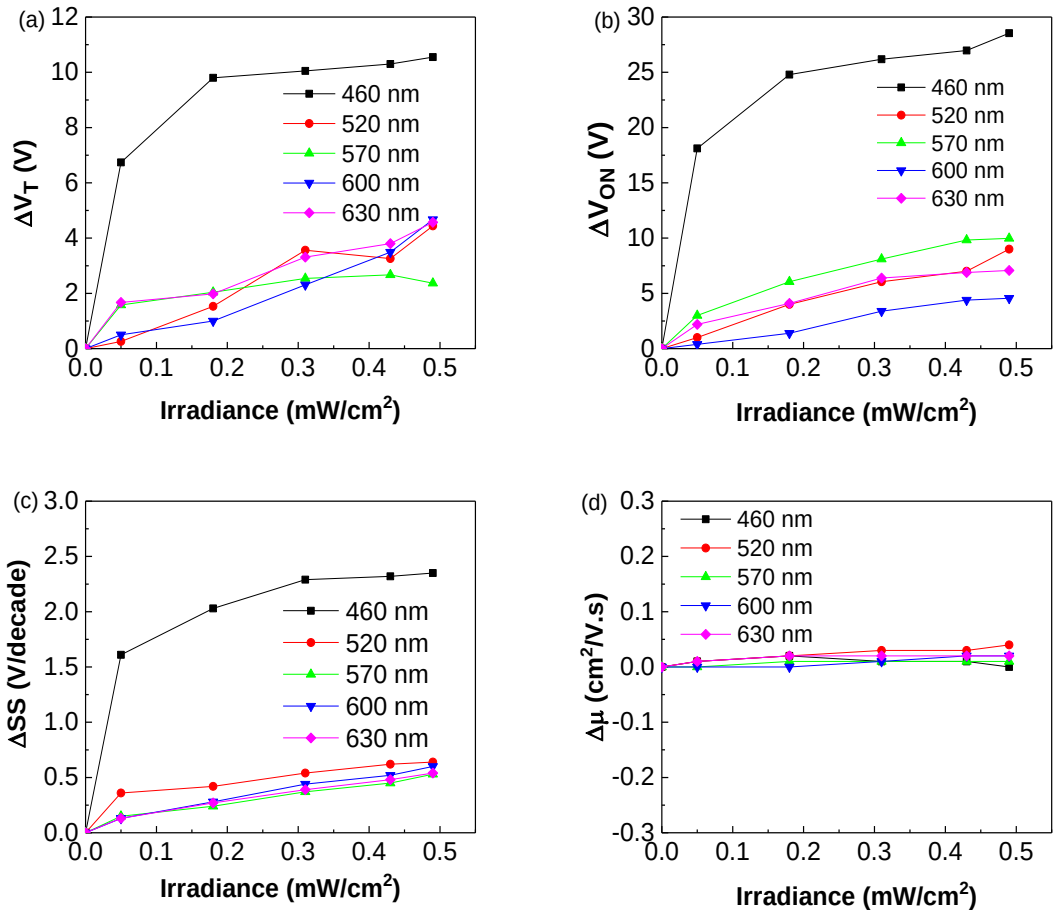

Figure 6.9 Changes in (a) threshold voltage, ΔV_T, (b) turn-on voltage, ΔV_{ON}, (c) subthreshold slope, ΔSS and (d) maximum mobility, $\Delta\mu$ as a function of illumination intensity. All characteristics were obtained in the dark after illumination.

6.2.2.1 Photosensitivity and photoresponsivity

In Figure 6.10(a) the maximum photosensitivity, P_{MAX}, is seen to increase with illumination intensity while in Figure 6.10(b) maximum photoresponsivity, R_{MAX}, seems to saturate at higher intensity. The values at 0.35 W/cm^2 are consistent with those in Figure 6.6(b). As before, the highest values of P_{MAX} obtained at 460 nm correspond to the peak absorption in DNTT. A plot of $1/R_{MAX}$ (inset Figure 6.10(b)) for λ = 460 nm is directly proportional to the light intensity which, according to equation (6.2), shows that I_D *(light)* - I_D *(dark)* = constant for the range of light intensities studied. However, this is not true at other wavelengths.

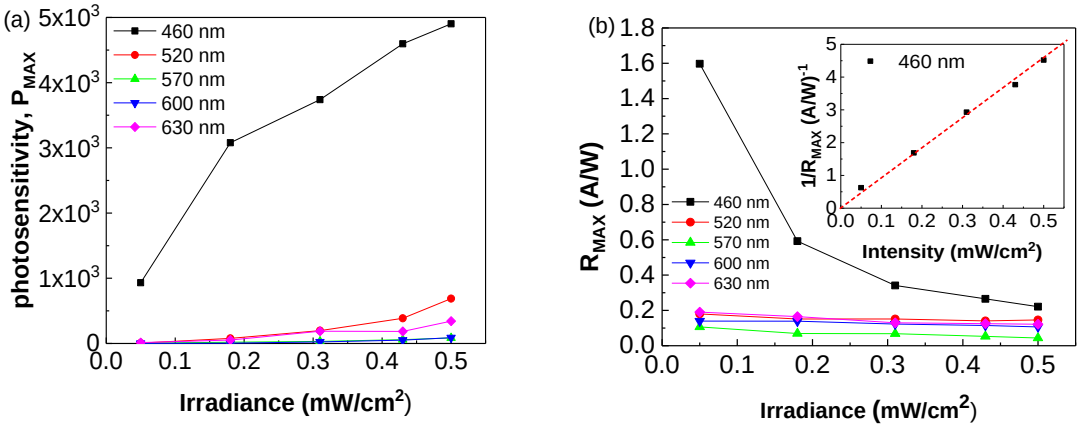

Figure 6.10 Maximum (a) photosensitivity, P_{MAX}, and (b) photoresponsivity, R_{MAX}, of PS-DNTT OTFT as a function of intensity obtained in the dark after 10 min illumination. Inset of Figure 6.10(b) shows 1/R as a function of intensity indicating that I_D *(light)* - I_D *(dark)* = constant according to equation 6.2.

6.2.2.2 Density of States

Figures 6.11(a) and (b) give the DoS for different intensities of 520 nm and 460 nm light respectively. For λ = 520 nm the plots show almost identical distributions regardless of the intensity. On the other hand, for λ = 460 nm, features appear at $E_V \geq 0.1$ eV which are consistent with the presence of deep trap states as in Figure 6.7(b).

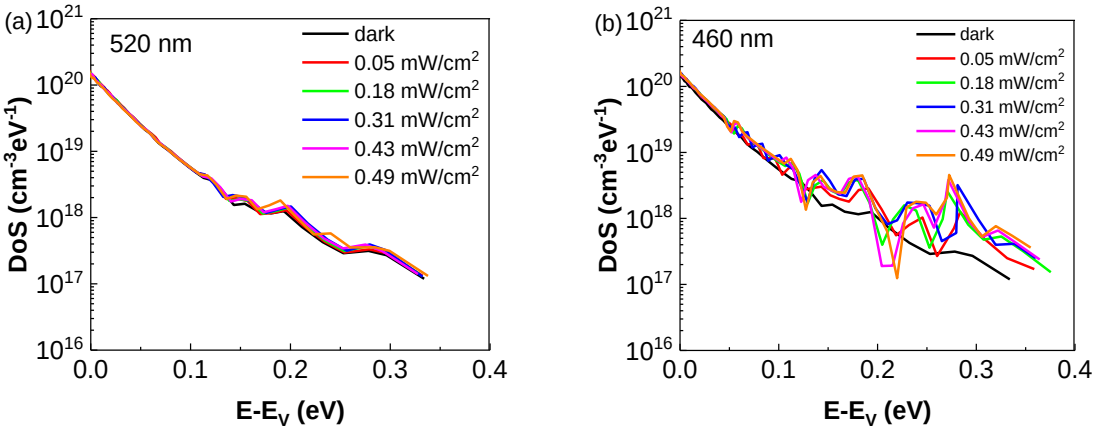

Figure 6.11 The DoS distribution as a function of E-E_V with illumination at wavelength (a) λ = 520 nm and (b) λ = 460 nm at different intensities.

6.2.3 Dynamic Photoresponse to Light Pulses

The dynamic photoresponse of PS/DNTT TFTs was investigated by switching the incident light on and off alternately with equal intervals of 100 s for 1600 s and noting the changes in source-drain current, I_D. Figure 6.12(a) shows the photoresponse when illuminated with 630, 520 and 460 nm light pulses under positive bias stress of V_G = 5 V, V_D = -1V. Almost no photoresponse was observed for 520 nm and 630 nm light exposure.

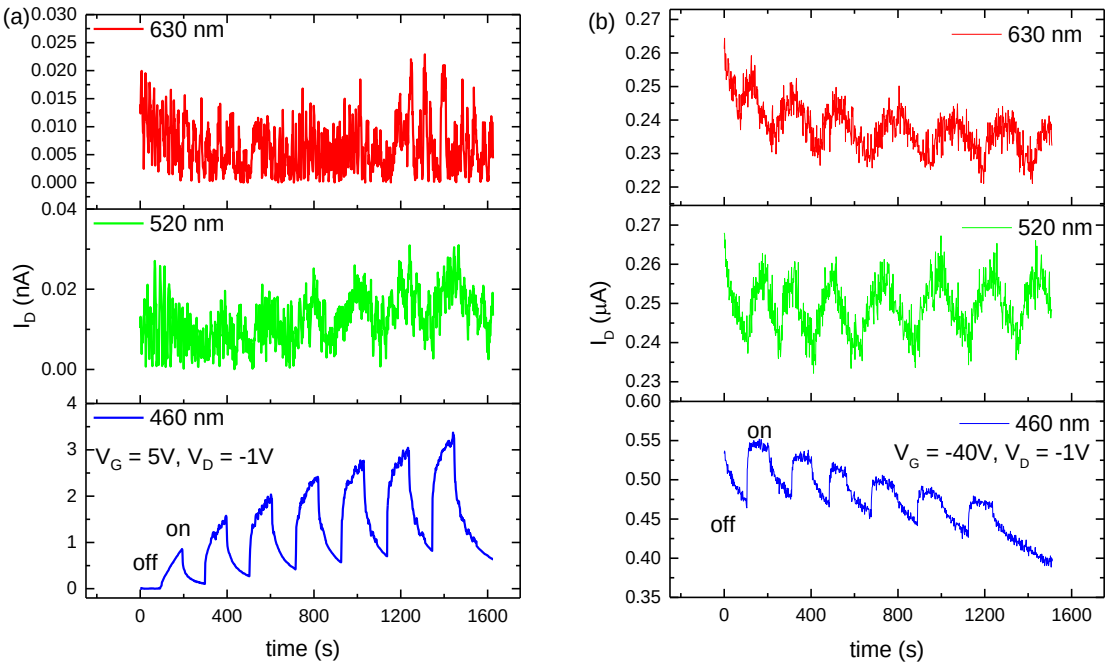

Figure 6.12 Time response for periodic illumination with 630, 520 and 460 nm pulses with (a) V_G = 5V, V_D = -1V and (b) V_G = -40V, V_D = -1V.

For 460 nm illumination, during each on(off) period, I_D shows a rapid increase(decrease) followed by a slower increase(decrease). In successive pulses the response increased but on a steadily increasing background. The 100 s dark period was insufficient to return the device to the initial condition. This is an example of persistent photoconductivity reported by several others workers. The response to light pulses of wavelength 630 and 520 nm with negative bias stress (V_G = -40 V, V_D = -1 V) is relatively slow and of small amplitude (Figure 6.12(b)). For 460 nm, the response was entirely different. I_D increased rapidly on turning on the light

but decayed more slowly on turning off the light. Furthermore, the response for successive pulses now decreased on a decreasing background.

6.3 Discussion

It is known that, the UV-Vis spectrum of DNTT shows strong absorption in the ultraviolet and blue region [97, 98]. Therefore, the greatest effect on ΔV_{ON} and ΔV_T would be expected when illuminating with 460 nm light as seen in Figure 6.3(a). Maxima in photosensitivity, P_{MAX} and photoresponsivity, R_{MAX} also occur at 460 nm (Figure 6.5) which correlates well with the notion that P and R arises from photoexcitation in the DNTT [97]. P_{MAX} is found to increase with increasing intensity from 0.05 mW/cm^2 to 0.49 mW/cm^2, as shown in 6.10(a). However, $\Delta V_{T,}$ ΔV_{ON}, ΔSS and R_{MAX} eventually saturate at higher intensities as shown in Figures 6.9(a), 6.9(b) and 6.9(c) and 6.10(b) respectively

Figure 6.13(a) summarizes three possible underlying mechanisms that were proposed to explain the effect of illumination in the organic phototransistor in the off-state. Basically, electron-hole pairs are generated in the film when photons with energy within the absorption range of DNTT are absorbed. Then, (i) photogenerated electrons move towards the source electrode while photogenerated holes will move away from source towards the drain via the bulk of DNTT or (ii) near the surface of DNTT and PS yielding a photocurrent element to the drain current. Also, (iii) the photogenerated electrons will drift towards, and are trapped in, interface traps. As shown in the band diagram of Figure 6.13(b), interface trapped electrons lying below the Fermi energy, E_F,will induce a positive shift in in the flatband-voltage, $V_{FB} = -Q_{it}/C_i$, adding to the drain current via the photovoltaic effect.

When the transistor is in the on-state, ($V_G < 0$), the valence band, E_V, bends upwards, increasing the interface hole concentration and lowering the Fermi level, E_F, at the semiconductor/insulator interface thus increasing the drain current. This is the normal field effect current. Under illumination, a photocurrent will be generated in the bulk DNTT as before. Figure 6.14(a) indicates four possible mechanisms when the transistor is in the on-state, ($V_G < 0$). (i) Photogenerated electrons will flow to the source possibly enhancing hole injection there whereas some photogenerated holes will be attracted to the drain thereby

adding to the drain current. (ii) Some of the photogenerated electrons will be trapped at the interface. However, most of the photogenerated holes will be attracted to the interface by the gate field, where some will either become (iii) trapped in interface states or (iv) will neutralize/deeply trapped trapped electrons at the interface. In both cases, this will cause a negative shift in V_{FB} which reduces the drain current. As shown in the band diagram of Figure 6.14(b), the Fermi level, E_F, moving down in the gap will cause electron detrapping from some interfacial traps while increasing the possibility of hole trapping. These ideas are now used to explain the results presented above.

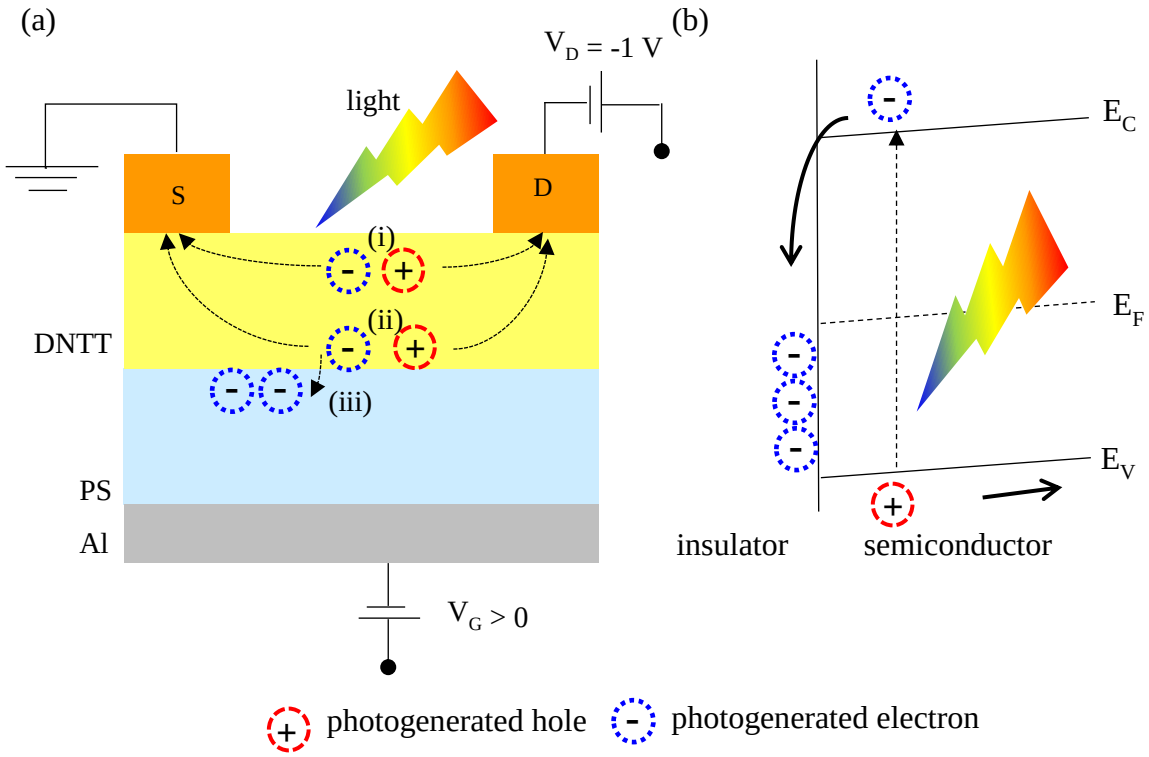

Figure 6.13 (a) Cross-section diagram PS-DNTT TFT illustrates three possible mechanisms of photogenerated carrier under illumination in the off-state including; (i) electrons move towards source while holes move towards the drain via the bulk or (ii) near DNTT-PS surface and (iii) electrons trapping at the interface. (b) The corresponding band diagram at the interface between insulator and semiconductor.

For $\lambda \geq 520$ nm, the idea of a simple flat-band voltage shift, ΔV_{FB}, works well. Reducing the gate voltage, V_G, by an amount equal to ΔV_{ON}, regardless of the direction of gate voltage sweeps, produced the dark characteristics with only minimal change in the shape of the

subthreshold region as shown in Figure 6.4(a) and 6.4(b). Moreover, there is no significant change in the DoS plots (Figures 6.7(a) and 6.7(b)) nor in the field-effect mobility (inset of Figures 6.1(a) and 6.1(c)). This confirms that when $\lambda \geq 520$ nm, a flat-band voltage shift caused by electron trapping at the interface is the dominant mechanism induced by light in a PS-DNTT TFT.

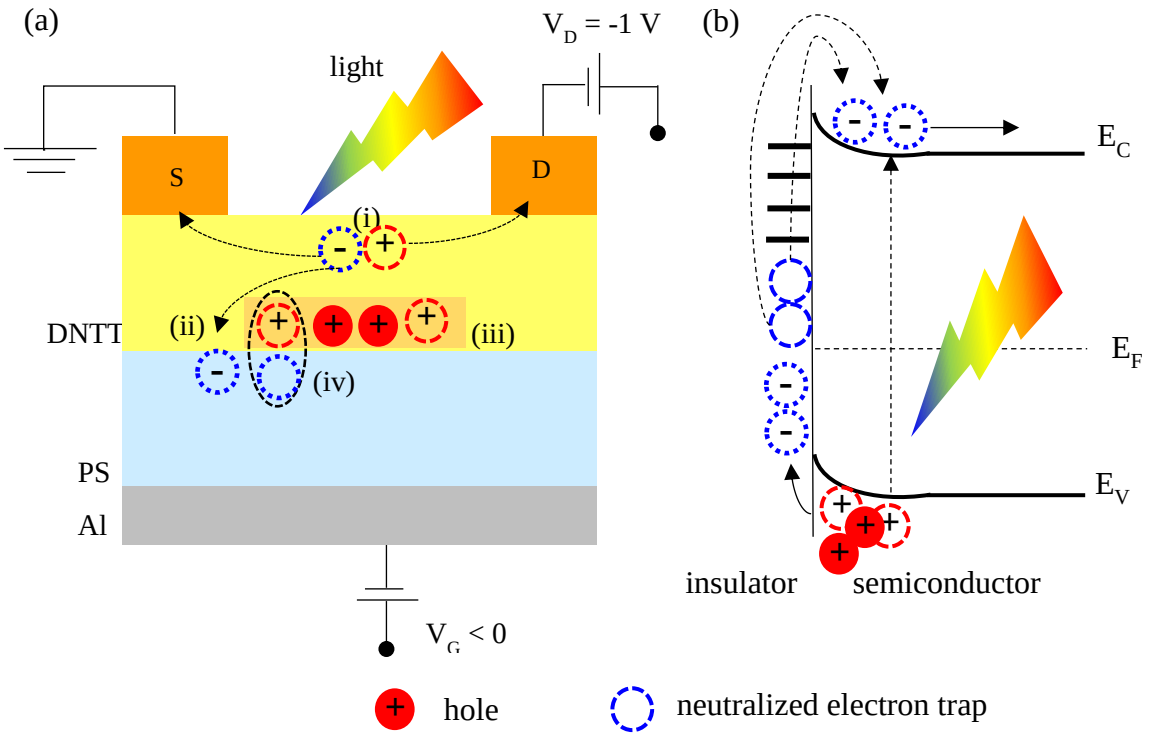

Figure 6.14 (a) Cross-section diagram PS-DNTT TFT illustrates four possible mechanisms for photogenerated carriers in a transistor under illumination in the on-state. (i) Electrons move towards source while holes move towards the drain. (ii) Electrons within a diffusion length of the interface will be trapped there. Most holes will be attracted to the interface by the gate field, where some will either become (iii) trapped in interface states or (iv) will neutralize interface trapped electrons. (b) The corresponding band diagram at the interface between insulator and semiconductor showing electron neutralization/detrapping in the subthreshold region.

In contrast to the longer wavelength cases, the semi-log plot of the post 460 nm illumination characteristics obtained in either forward or reverse gate voltage sweeps does not reproduce the dark characteristic and a significant change occurs in the subthreshold slope after shifting the plots by an amount equal to ΔV_{ON} (Figure 6.4(c) and 6.4(d)). Moreover, the DoS under

illumination with 460 nm light shows significant changes. Strangely, however, there is no significant change observed in the mobility as seen in Figure 6.9(d). Furthermore, Figure 6.11(b) shows that the DoS changes are apparently almost independent of intensity. It was argued earlier in section 6.2.1 that ΔV_{ON} and ΔV_T were caused by electron trapping at the insulator/semiconductor interface or in the insulator itself. It was further argued that the change in ΔSS was due to de-trapping or neutralization of these electrons resulting in an unstable V_{FB} and a change in ΔSS. Therefore, features in the DoS in the subthreshold region may reflect the changing V_{FB} rather than the creation of new hole states in DNTT.

Clockwise hysteresis observed in Figure 6.2(b) in both irradiated device and post irradiation suggests that in the forward sweep, electrons detrap or are neutralized by recombination with holes or by interface hole trapping as illustrated by the band diagrams in 6.14(b) and 6.15(a). Virtually no hysteresis is seen in the initial dark transfer characteristic. This indicates that the photo-induced charges dictate the observed hysteresis by changing the interface trap occupancy during gate voltage sweep. The forward sweeps under illumination and post-illumination are identical as are the above subthreshold regions of the return sweeps (Figure 6.2(b)). There is no indication of a photocurrent. However, the drain current, I_D, under illumination asymptotes to higher off-current in the return sweep. The increased drain current in the off-state could be due to several possible reasons. Firstly, it is likely to be related to accumulation of more trapped electrons in the subthreshold region while in reverse sweep. This is because band bending slowly decreases which in turn increases the Fermi level, E_F, in the gap causing detrapping of trapped holes above E_F. Another possible reason is due to the accumulation of electrons in DNTT near the source contact as suggested earlier. These accumulated electrons will effectively reduce the potential barrier to holes between the source and the DNTT channel resulting in positive shift in ΔV_T and a significant increase in the drain current, I_D.

However, post-illumination, the off-current in the return sweep returns to the low value seen at start of the forward sweep as shown in Figure 6.2(b). This suggests that most of the photo-induced charges are probably trapped in shallow bulk traps since these carriers could detrap rapidly as pointed out by Salleo et al [54]. The effect of light on the electron quasi Fermi level (QFL) should be considered as well. Under illumination, quasi-Fermi levels, QFL for

holes and electrons are introduced to characterize the non-equilbrium state. As the light intensity is increased, the electron QFL will move closer to the lowest unoccupied molecular orbital (LUMO) so that more interface electron traps become available for trapping electrons This in turn reduces the band-bending for a particular gate bias [91, 113]. As a consequence the drain current, I_D, increases rapidly as interface trap states are immediately filled by electrons, and emptying as soon as the light is terminated. This is evidenced by the identical off-current at the start of post-illumination sweep (Figure 6.2(b)). This concept is briefly illustrated in the band diagram in Figure 6.15(b).

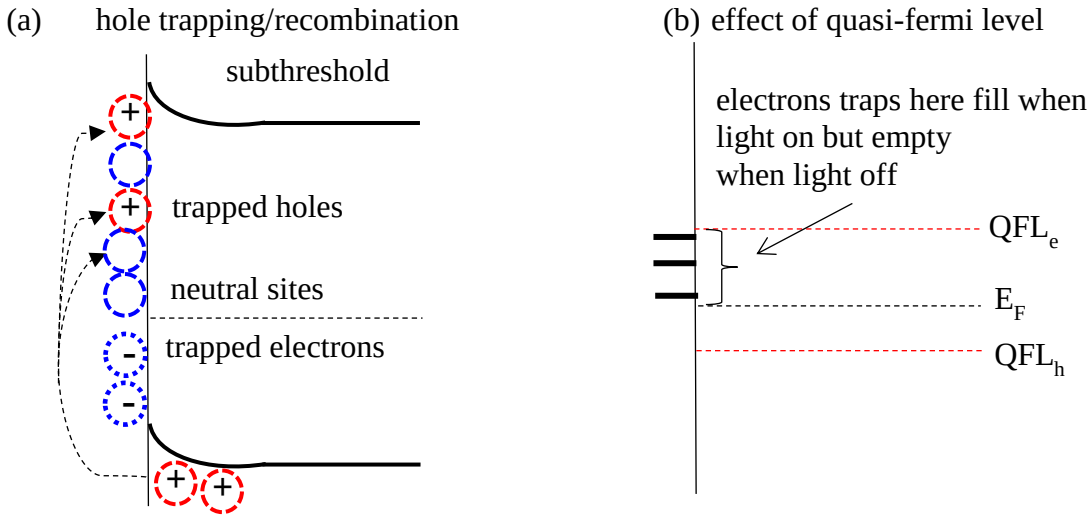

Figure 6.15 Schematics of energy band diagram showing (a) electrons traps neutralized by recombination with holes or by interface hole trapping in the subthreshold region and (b) effect of light on the quasi-Fermi level, QFL.

It is also worth mentioning that Hamilton [91] used the idea of the electron QFL as an alternative explanation for the larger subthreshold slope observed in a F8T2 [poly(9, 9-dioctylfluorene-co-bithiophene)] illuminated TFT. However, how the QFL affected the subthreshold slope was not clearly explained. Watson et al [113] also used the idea of the electron QFL to explain one of their results based on photocapacitance response with metal-insulator- semiconductor MIS structures based of poly(3-hexylthiophene)/ poly (amide-imide) (P3HT/PAI) bilayer. Their capacitance-voltage measurements are not complicated by channel currents as in the transistor so that interface trapping effects are more readily identified. They found that, under illumination the QFL mechanism could activate interface

traps for photo-generated electrons, while allowing rapid de-trapping, and the device returning to its pre-irradiation state after terminating the illumination.

This is likely also to be the case for the fast transient behavior of drain current response to 460 nm illumination pulses under positive bias stress of V_G = 5 V, V_D = -1 V (Figure 6.12(a)). The drain current, I_D, increases rapidly as interface trap states are immediately filled by electrons during illumination and emptying as soon as the light is terminated. However, I_D post-illumination does not return to its pre-irradiation state suggesting that not all electrons were rapidly de-trapped or neutralized. Some of the electrons may become deeply trapped at the interface. Residual electrons remained in the trap states at the start of the subsequent illumination period and caused the response to increase on a steadily increasing background. Another possible explanation for the fast dynamic response is electron accumulation in DNTT near the source contact as suggested above. That could improve source hole injection and further enhance the photocurrent element to the drain current. The dynamic response under illumination also comprised a slow transient that continued during the light-off period. This slow transient behavior is again consistent with interface electron trapping during illumination and de-trapping/neutralization as soon as the light is terminated. The process would induce shifts in ΔV_{ON} and ΔV_T.

Similarly, I_D increases when illuminated under negative bias stress (V_G = -40 V, V_D = -1 V) and decreases as the light is terminated Figure 6.12(b). Unlike positive bias stress, the response for successive pulses decreased with a decreasing background. As proposed above, biasing the device into strong accumulation moves E_F lower in the gap as a result of band-bending. Hence, most photogenerated holes will be attracted to the interface by the gate field. There they will either be trapped in interface states or neutralize trapped electrons leading to a negative shift in V_{FB} which reduces the drain current. Residual holes still in trap states at the start of the subsequent illumination period will cause a response that decreases on a steadily decreasing background.

The QFL is dependent on the intensity and photogeneration efficiency of the incident illumination. Therefore, it is expected that the DoS will change with intensity. However, the DoS at 460 nm illumination is almost independent of intensity. Moreover, it has been shown

in the inset of Figure 6.10(b) that *1/R* is directly proportional to the light intensity for λ = 460 nm indicating that [I_D *(light)* - I_D *(dark)]* is constant according to equation (6.2). In such a case the QFL effect can be neglected. It was argued earlier that hysteresis observed under illumination is dictated by interface trap occupancy by photo-induced charges. As intensity increased this trap occupancy seems to saturate resulting in the saturation of $\Delta V_{T,} \Delta V_{ON}$, ΔSS and R_{MAX} at higher intensity as shown in Figures 6.9(a), 6.9(b) and 6.9(c) and 6.10(b) respectively. This is in agreement with Milvich et. al [97] and Debucquoy et al [96] who show that under strong illumination, ΔV_T, is limited by trapping.

6.4 Summary

The effect of illumination on PS-DNTT devices was investigated with results obtained over a range of wavelengths and intensities. Both V_T and V_{ON} shifted positively regardless of the wavelength, with the greatest shifts being observed at 460 nm. For $\lambda \geq 520$ nm, there are no significant changes in either the DoS spectrum or the gate-voltage dependence of the field effect mobility suggesting the flat-band voltage shift, ΔV_{FB}, caused by electron trapping at the interface. For λ = 460, the profile of the deeper states in the DoS spectrum reflecting the significant change in the subthreshold slope. As there is no change in the gate-voltage dependence of the field effect mobility, it is unlikely that the observed changes in the DoS are due to creation deep trap states in the band gap of DNTT. Rather the effect is explained due to (i) trapping of photogenerated electrons, (ii) an unstable shift in the light-induced flat-band ΔV_{FB}, caused by detrapping or neutralization of electrons as the transistor is turned on so that $\Delta V_T < \Delta V_{ON}$, (iii) accumulation of electrons in DNTT near to source contact or (iv) the effect of the electron quasi Fermi level, QFL.

It has been shown that the dynamic photoresponse at 460 nm under positive and negative bias stresses consisted of fast and slow components. During on period, I_D increased rapidly due to the effect of the electron QFL and also electron accumulation in DNTT near the source contact. The slow transient behavior of the I_D under illumination and during the light-off period arises from de-trapping/neutralized of trapped electrons. However, the post illumination I_D does not return to its pre- irradiation state when the light is turned off and the response for successive pulses increased but on a steadily increasing background under

positive gate bias stress. On the other hand, the response for successive pulses decreased on a decreasing background under negative gate bias stress.

7 Effect of Illumination and Bias Stress PS-DNTT Thin Films Transistors

7.1 Introduction

It had be showed in chapter 6, that the effect of illumination on PS-DNTT transistors with $\lambda \geq 520$ nm, V_T and V_{ON} shift positively due to the flat-band voltage shift, V_{FB}, caused by electron trapping at the interface. The greatest effects were observed at 460 nm with a significant change in the subthreshold slope were unlikely to be due to the creation of deep trap states in the DNTT. This chapter focusses on the combined effect of bias and illumination on the DNTT TFTs is investigated and discussed. In particular, the additional effect of bias stress on the TFT photo-response to different wavelength, intensity and time are analyzed.

7.2 Results

7.2.1 Effect of Bias Stress Under Ambient Light

In this section, the combined effect of bias stress and ambient light on the electrical performance of a PS-DNTT TFT is presented. The device characteristics were measured in the dark after applying a negative (NBS) and positive bias stresses (PBS) for 2500 s under ambient light. These experiment were conducted with the same device as that in chapter 5. Therefore it had previous measurement history which caused a slightly positive turn-on voltage, V_{ON} = -9 and threshold voltage V_T = -18 V when measured in the dark.

Figure 7.1(a) exhibits the transfer characteristics obtained at V_D = -1V after stressing under ambient light with NBS of V_G = -40 V and V_D = 0 V for 2500 s. It can be observed that ΔV_T and ΔV_{ON} shifted positively by 1 and 9 V respectively with a clockwise hysteresis. The magnitude of ΔV_{ON} seen after illumination with ambient light was found to be lower than in the previous experiments (Figure 6.1(d)) with fixed wavelength, 460 nm corresponding to the absorption peak in DNTT. This is not surprising since only a fraction of the ambient light incident on the device is absorbed. However, ΔV_{ON} for ambient illumination is much higher than measured for $\lambda > 460$ nm owing to the shorter wavelength component in ambient light. A significant change appears in the subthreshold slope, *SS* which increases from 4.18 V/decade to 5.80 V/decade. Figure 7.1(b) shows that the shift in the transfer characteristic

after illumination is accelerated under a PBS of V_G = 30 V and V_D = 0 V for 2500 s. V_T and V_{ON} shifted by 14 and 24 V respectively and *SS* increased from 4.01 V/decade to 5.78 V/decade. No increase in off-current is observed under either stress condition. The gate-voltage dependent mobility under NBS and PBS are shown in Figures 7.2(a) and 7.2(b). No significant change in mobility is observed suggesting that neither the morphology nor the structure of the DNTT is affected by ambient light.

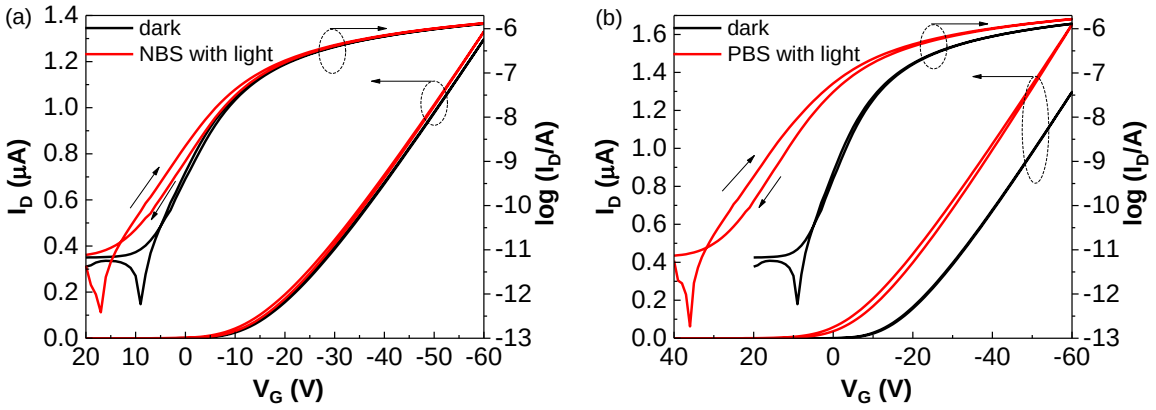

Figure 7.1 Transfer characteristics in the dark and after illumination with (a) NBS of V_G = -40 V, V_D= 0 V and (b) PBS of V_G = 30 V, V_D = 0 V for 2500 s.

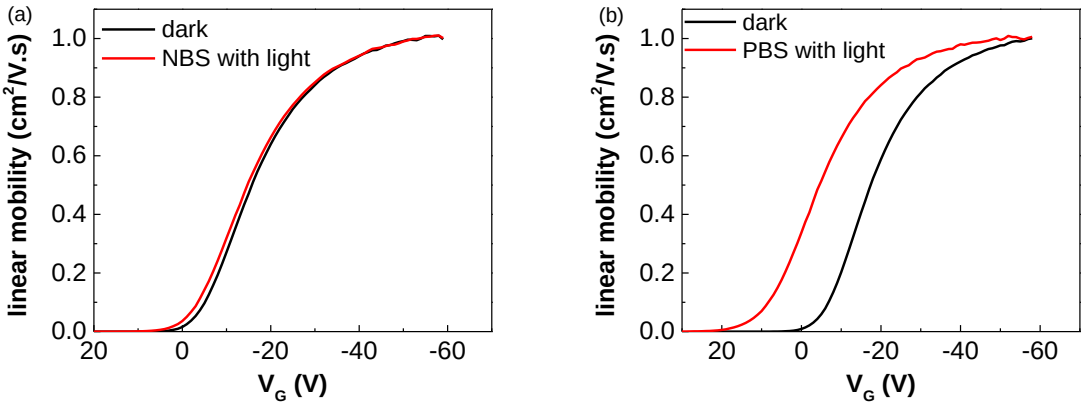

Figure 7.2 Gate-voltage dependent mobility in the forward sweep, in the dark and after illumination under (a) NBS of V_G = -40 V, V_D= 0 V and (b) PBS of V_G = 30 V, V_D = 0 V for 2500 s in both cases.

Figures 7.3(a) and (b) show dark and post stress characteristics under NBS and PBS respectively. It can be observed that, shifting the linear transfer plot by ΔV_T, under NBS, reproduced the dark characteristics. Under PBS, a slight change appears during V_G sweeps from -10 V to -30 V but thereafter slowly coalescing to the dark characteristics above the subthreshold region. The reverse sweep reproduces faithfully the dark characteristic. On the other hand, after shifting the semi-log transfer characteristic by an amount equal to ΔV_{ON} from the dark, the changes in subthreshold slope under NBS and PBS become more obvious. This feature is slightly enhanced in the characteristic under PBS above the subthreshold region.

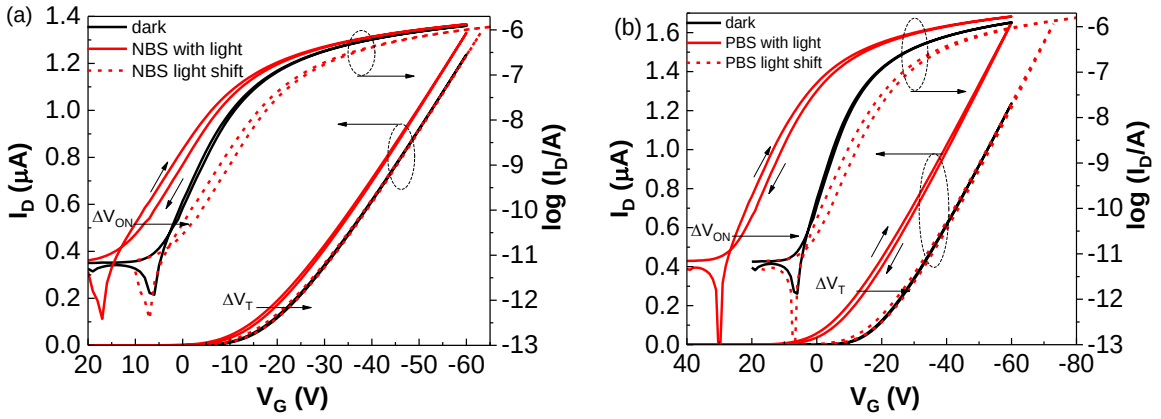

Figure 7.3 Transfer characteristics recorded in the dark and after ambient illumination, (a) under NBS and (b) under PBS for 2500 s. The dashed lines correspond to the illuminated characteristics shifted by an amount equal to the difference ΔV_{ON} and ΔV_T from the dark.

Changes observed in the subthreshold region of the transfer characteristics indicates the possibility that illumination has created new band gap states in the DNTT. To investigate this possibility, DoS in the illuminated PS-DNTT TFT was extracted by applying the Grünewald model to transfer plots obtained in the linear regime. Figure 7.4(a) displays the DoS under NBS and PBS. It can be seen that the shallow states remain unaffected. Under NBS, the DoS appears to increase for E-$E_V \geq 0.15$.This feature is enhanced under PBS for E-$E_V \geq 0.10$ eV.

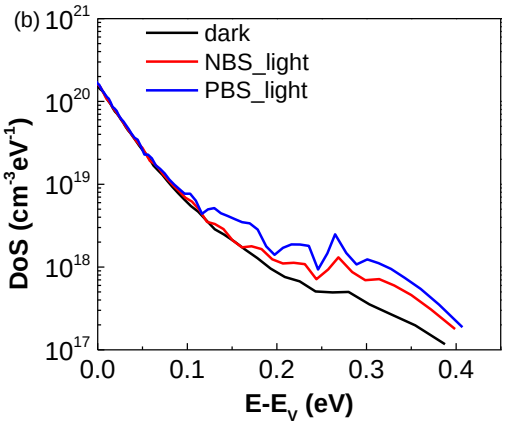

Figure 7.4 DoS distribution as a function of E-E_V before and after illuminated with NBS of V_G = -40 V, V_D= 0 V and PBS of V_G = 30 V, V_D = 0 V for 2500 s.

7.2.2 Gate Bias Stress in the Presence of Monochromatic Illumination.

7.2.2.1 Effect of Wavelength

In the previous section, the effect of ambient illumination was presented. Here the effect of monochromatic light on bias stress is presented. A fresh device but from the same fabrication batch as in Chapter 6 were subjected to NBS and PBS under monochromatic illumination. The wavelengths and intensities were as follows: λ = 460 nm and intensities of 0.31 mW/cm^2; 520 nm, 0.31 mW/cm^2; λ = 570 nm, 0.31 mW/cm^2; λ = 600 nm, 0.33 mW/cm^2 and λ = 630 nm, 0.35 mW/cm^2, all for 600 s.

Figure 7.5(a) shows the transfer characteristics obtained for V_D = -1 V, during a forward gate voltage sweep (V_G = 20V to -60V) following NBS (V_G = -40 V, V_D = 0 V) under the different wavelengths. For λ > 460 nm all curves shifted negatively. Such behavior is similar to that induced by negative bias stress in the dark. However when λ = 460 nm, the transfer characteristic shifted positively. This wavelength corresponds to a high photogeneration rate of electron-hole pairs in the DNTT.

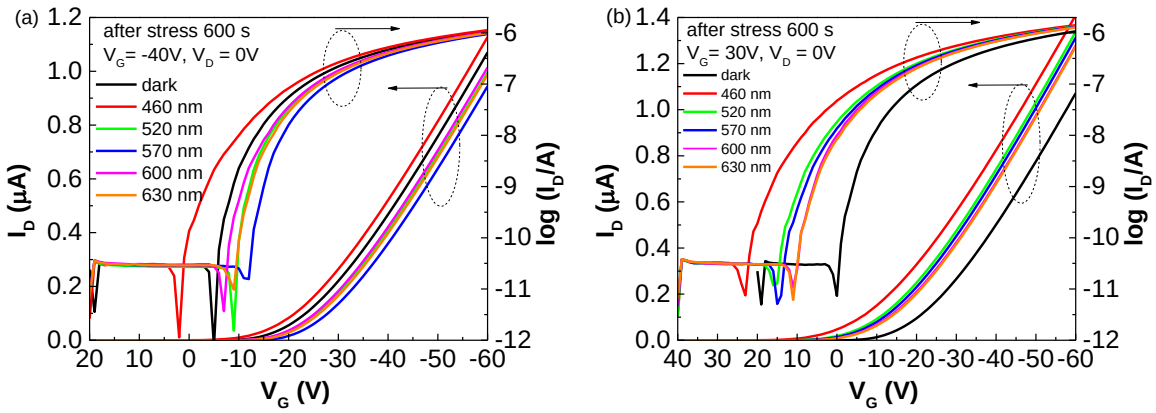

Figure 7.5 Transfer characteristics obtained in a forward gate voltage sweep (V_G = 20V to -60V) with (a) NBS of V_G = -40 V, V_D= 0V and (b) PBS of V_G = 30 V, V_D = 0 V under various wavelength**.** The intensity for different wavelengths varied between 0.31 to 0.35 mW/cm^2

The effect of illumination on a PBS of V_G = 30 V, V_D = 0 V for 600 s at different wavelengths is shown in Figure 7.5(b). A noticeable positive shift was observed in the transfer characteristics under illumination at all wavelengths with the largest changes obtained at 460 nm. Figures 7.6(a) and 7.6(b) show the changes in ΔV_{ON} and ΔV_T respectively plotted as a function of wavelengths. Also shown are the corresponding values obtained from Chapter 6 (Figure 6.3(a)) in the absence of bias stress. When λ = 460 nm, both ΔV_T and ΔV_{ON} were enhanced under PBS while suppressed by applying NBS. The magnitude of ΔV_{ON} was also significantly higher than ΔV_T. The dependence of ΔSS on wavelengths is shown in Figure 7.6(c). Under NBS, the change in the subthreshold slope, ΔSS at λ = 460 nm, is 1.0 V/decade while under PBS, ΔSS showed a further shift up to 4.2 V/decade. For all wavelengths, the maximum mobility barely changed, as shown in Figure 7.6(d)

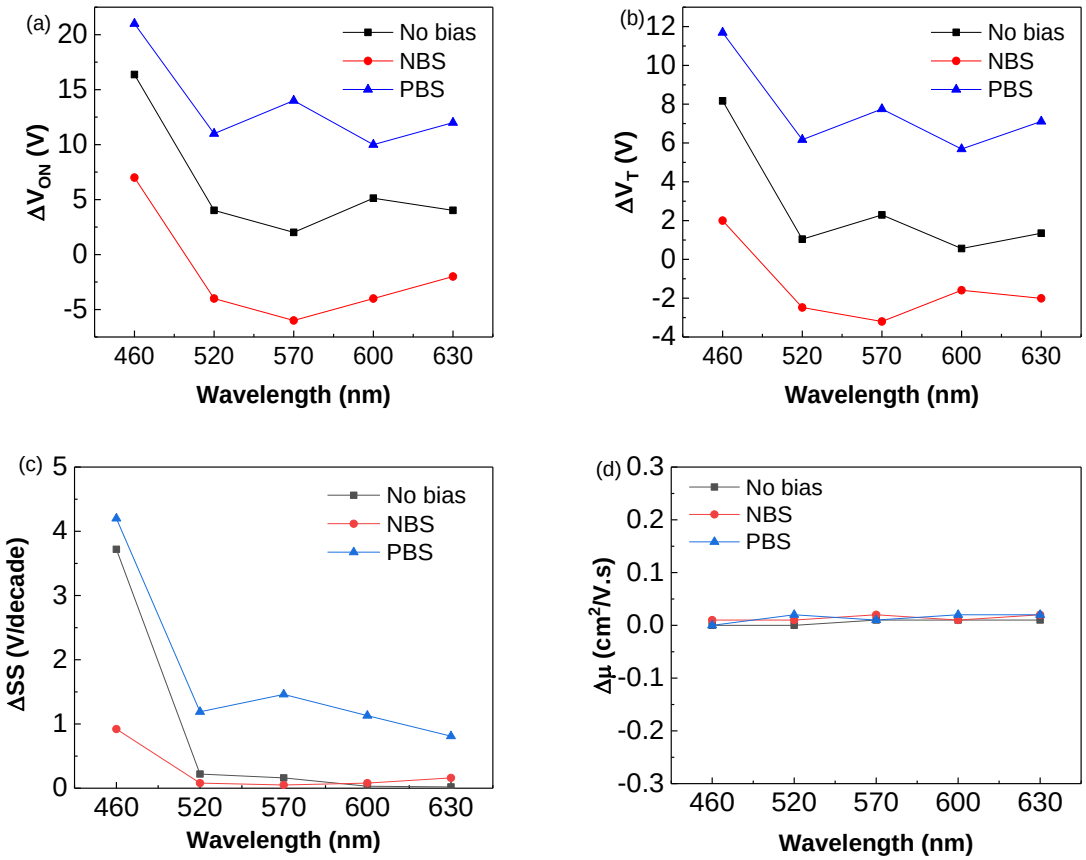

Figure 7.6 Shifts of (a) turn-on voltage, ΔV_{ON}, (b) threshold voltage, ΔV_T, (c) subthreshold slope, ΔSS and (d) maximum mobility, $\Delta\mu$ without bias stress and under NBS and PBS as a function of wavelengths.

In order to observe the effect in the subthreshold region more clearly, the semilog transfer characteristic obtained after bias stress and illumination was replotted by shifting the original data towards the initial characteristics by an amount equal to ΔV_{ON}. It is seen that under NBS with λ = 520 nm, there is no change in the shape of the transfer characteristic (Figure 7.7(a)). Furthermore, on shifting the linear plot by ΔV_T again the dark plot is reproduced.

Following PBS under illumination with 520 nm light, a significant change is observed when the semilog plot is shifted towards the dark plot by an amount equal to ΔV_{ON} (Figure 7.7(b)). Interestingly, the departure from the dark plot is enhanced compared to the effect of illumination alone (Figure 6.4(a)). Nevertheless, above threshold, the linear post-illumination plot reproduced the dark characteristics after shifting by an amount equal to ΔV_T. Bias stress

with λ = 460 nm causes significant changes in the subthreshold region for both polarities of stress voltages, as seen in Figures 7.7(c) and (d) after shifting the post-illumination semilog plots by ΔV_{ON}. Shifting the linear plots by ΔV_T reproduces very well the initial dark plot for NBS. Under PBS, a slight change appears during V_G sweeps from -10 V to -45 V but thereafter slowly coalescing to the dark characteristics above V_G = -50 V.

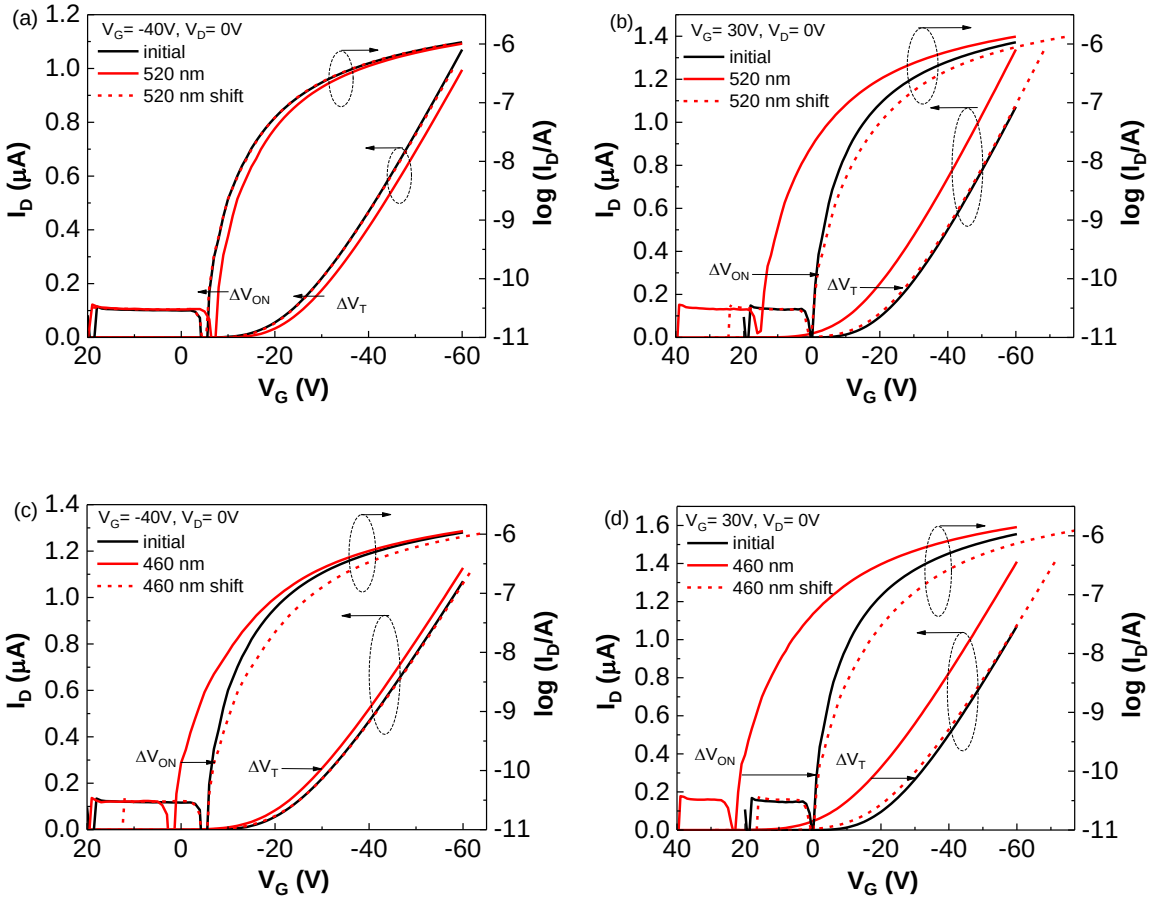

Figure 7.7 Transfer characteristics on linear and semi-log scales recorded during forward gate voltage sweeps (V_G = 20 V to -60 V) in the dark and after illumination at 520 nm, under (a) NBS and (b) PBS and at 460 nm, under (c) NBS and (d) PBS. The dashed lines correspond to the illuminated characteristics shifted by an amount equal to the differences ΔV_{ON} and ΔV_T from the dark.

Figure 7.8(a) and 7.8(b) represent the gate-voltage dependence of the mobility under both stress conditions. Under negative bias stress, the maximum mobility, μ_{lin} remains nearly

constant at 1.0 cm^2/V.s confirming that the morphology and structure is not affected by illumination (Figure 7.8(a)). Under positive bias stress, the maximum mobility appears to be slightly higher due to the effect of the shift in threshold voltage as demonstrated in Figure 7.8(b).

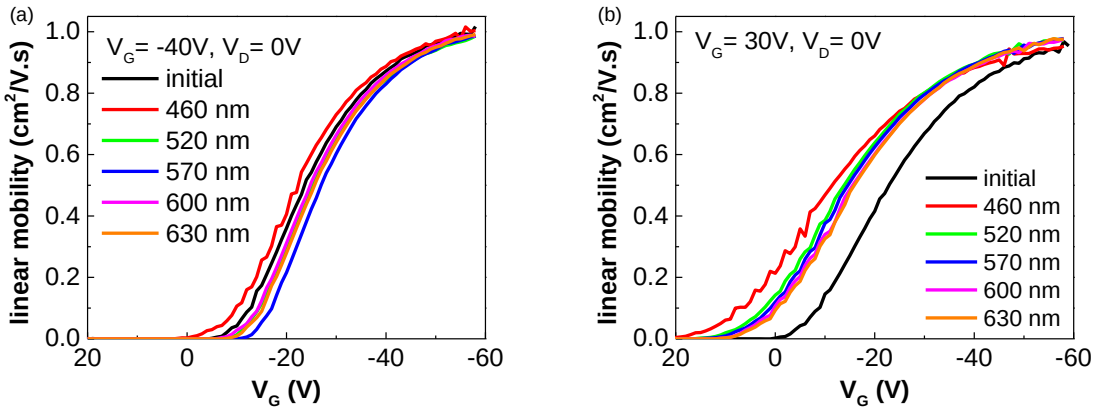

Figure 7.8 Gate-voltage-dependent mobility as a function of wavelength with (a) NBS of V_G = -40 V, V_D= 0 V and (b) PBS of V_G = 30 V, V_D = 0 V. The intensity at different wavelength varied between 0.31 and 0.35 mW/cm^2

The effect of bias stress on the photosensitivity, *P* at different wavelengths is shown in Figure 7.9(a) and 7.9(b). Under both NBS and PBS, the photosensitivity peaks at ~5 x 10^3 for λ = 460 nm under both stress conditions. Over most of the voltage range, *P* observed for $\lambda > 460$ nm under NBS is almost negligible. By contrast, photosensitivity, *P* was enhanced by PBS over the whole V_G range reaching maximum values similar to that obtained at 460 nm in the previous chapter. The V_G-dependence of photoresponsivity, *R*, for illumination under NBS is shown in Figure 7.9(c). Positive values of *R* were only obtained for λ = 460 nm. For $\lambda > 460$ nm, the maximum photoresponsivity, R_{MAX}, was negative. This finding shows that NBS suppresses the effect of illumination on the device. Under PBS, R_{MAX} increased significantly regardless of wavelength. At 460 nm, R_{MAX} at 0.37 A/W, is only slightly higher than that obtained from the phototransistor measurement in Figure 6.5(d) which was ~0.34 A/W.

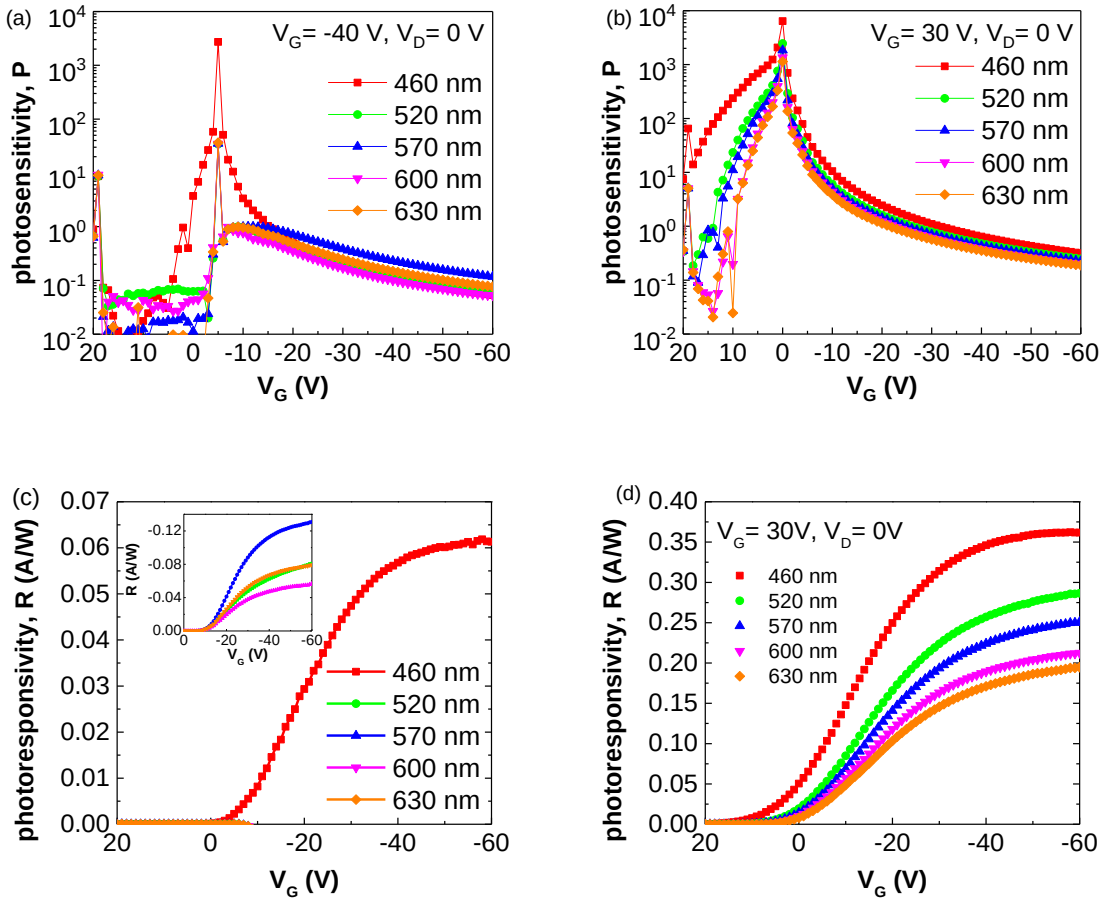

Figure 7.9 Photosensitivity, P of a PS-DNTT TFT as a function of V_G after stressing with light of various wavelengths with (a) NBS V_G = -40 V,V_D = 0 V and (b) PBS V_G = 30 V, V_D = 0 V. Also shown is the photoresponsivity, R following illumination with (c) NBS V_G = -40 V, V_D = 0 V and (d) PBS, V_G = 30 V, V_D = 0 V. The inset in (c) shows photoresponsivity, R for $\lambda > 460$ nm.

The DoS plotted as a function of E-E_V after application of NBS under illumination is shown in Figure 7.10(a). For λ > 460 nm, the DoS distribution is almost identical to the initial spectrum over the whole range of E-E_V. For λ = 460 nm, however, a distinct increase is seen in the deep trap states between ~0.15 eV and ~0.35 eV above E_V. A similar feature was also observed under PBS, regardless of the wavelength (Figure 7.10(b)).

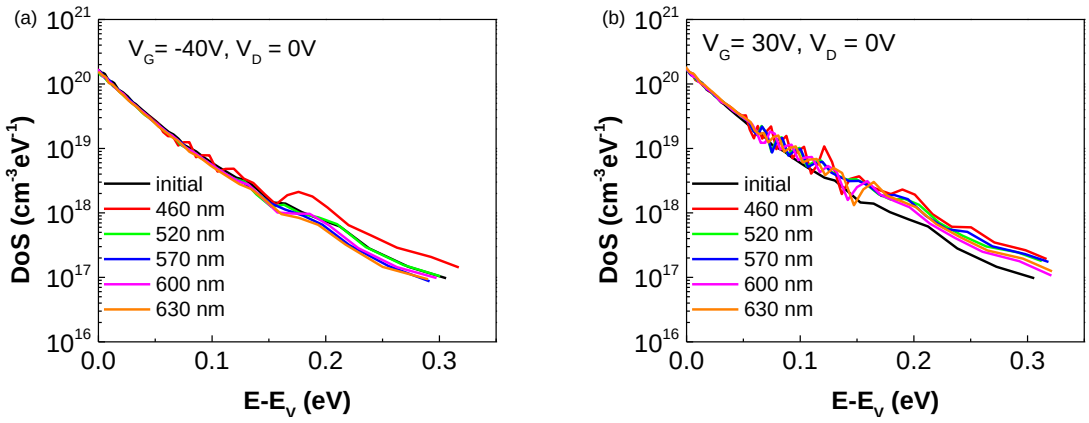

Figure 7.10 The density of states as a function of E-E_V following illumination with (a) NBS V_G = -40 V, V_D= 0 V and (b) PBS V_G = 30 V, V_D = 0 V at various wavelength**.**

7.2.2.2 Effect of stress time

From the foregoing, it is seen that the greatest optical response occurs when illuminating devices with band gap light i.e. λ = 460 nm. Accordingly, in this section the effect of stress time under negative and positive bias stress with illumination at 460 nm with intensity of 0.31 mW/cm^2 is investigated. The results for NBS and PBS in the forward gate sweeps are shown in Figure 7.11(a) and (b) respectively.

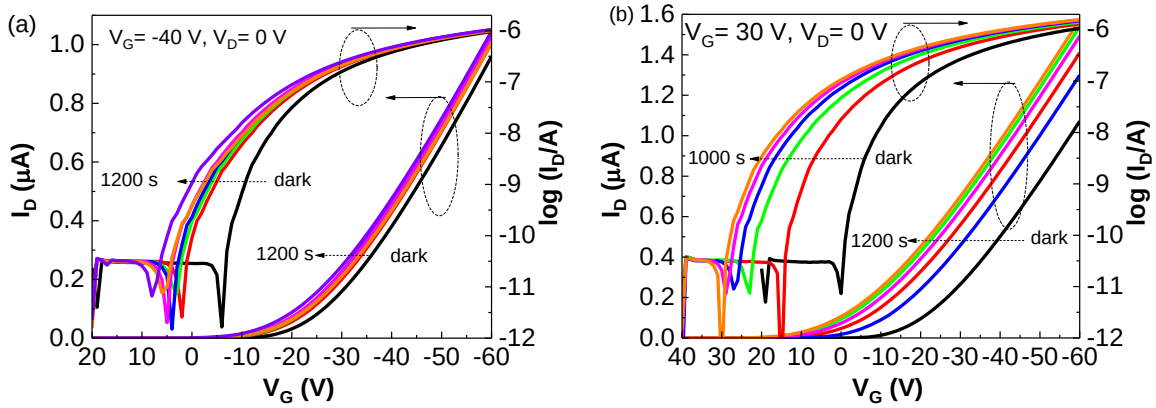

Figure 7.11 Transfer characteristics as a function of stress time with (a) NBS, V_G = -40 V, V_D = 0 V and (b) PBS, V_G = 30 V, V_D = 0 V illuminated at 460 nm with intensity 0.31 mW/cm^2

In the case of NBS, the device was stressed up to 1200 s. Under PBS, device was stressed for only 1000 s. This is because at 1000 s V_{ON} is already at 30 V. Stressing for longer than 1000 s may have damaged the gate dielectric under PBS conditions. All transfer characteristics exhibit a positive shift with a change in the subthreshold region under both stress conditions. In the case of PBS, the shifts are larger than for NBS.

Figures 7.12(a) and (b) show the time dependence of ΔV_T and the time dependence of ΔV_{ON} under PBS and NBS. In both stress conditions, the magnitude of ΔV_{ON} was significantly higher than ΔV_T. The latter can be well described by the simple-exponential function:

$$\Delta V_T(t) = |V_T(\infty) - V_T(0)| \left[1 - e^{-\left(\frac{t}{\tau}\right)}\right] \cdot \tag{7.1}$$

where $V_T(\infty)$ is the threshold voltage when time approaches infinity, V_{T0} is the threshold voltage before bias stress and τ the characteristic trapping time. The solid lines indicate the corresponding fitting and the extracted parameters are listed in Table 7.1.

Table 7.1 Parameters obtained by fitting equation (7.1) to the measured ΔV_T in Figure 7.12(a).

Stress conditions	$\lvert V_T(\infty)-V_T(0) \rvert$ **(V)**	τ **(s)**
Negative bias stress, NBS: V_G = -40V and V_D = 0 V	3.86	1456
Positive bias stress, PBS: V_G = 30V and V_D = 0 V	17.51	379

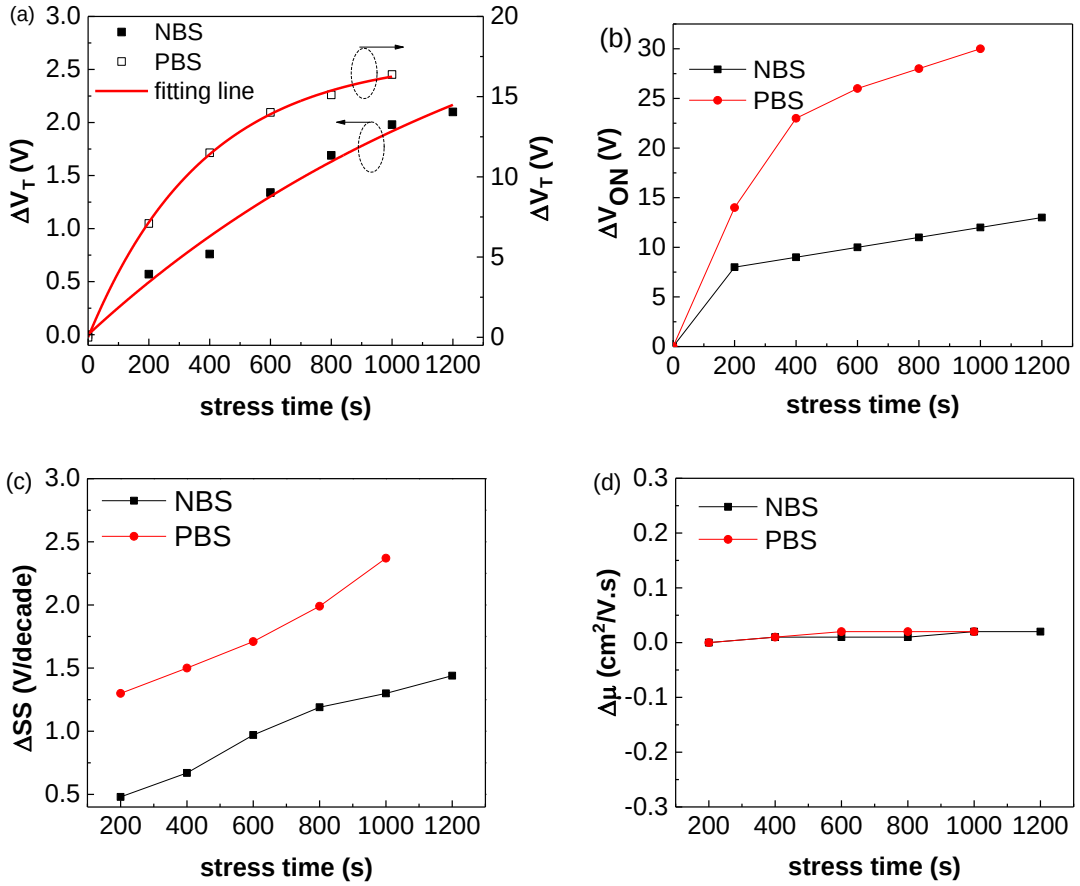

Figure 7.12 Shifts of (a) threshold voltage, ΔV_T, (b) turn-on voltage, ΔV_{ON}, (c) subthreshold slope, ΔSS and (d) maximum mobility, $\Delta\mu$ as a function of stress time under PBS and NBS for λ = 460 nm with intensity of 0.31 mW/cm^2. The solid lines in figure (a) represent the data fitted by simple-exponential function.

Interestingly the magnitude of $|V_T(\infty) - V_T(0)|$ and τ under NBS are comparable to the values obtained in the dark as listed in Table 5.1 (3.13 V and 1470 s). This indicates that the addition of illumination does not substantially stimulate the rate of trapping. The trapping rate increases significantly under positive bias stress accompanied by a large increase in ΔV_T. However, in the absence of illumination $|V_T(\infty) - V_T(0)|$ at ~1.76 V (Figure 5.33(a)) is significantly lower than in the present case. This indicates that photo-generation increases the number of charge carriers available for trapping thus increasing the maximum threshold voltage shift expected for $t \rightarrow \infty$. Figures 7.12(c) and (d) show the time dependences of ΔSS and $\Delta\mu$ under PBS and NBS. The increase in subthreshold slope is reflected in the increase in the density of states deeper than 0.1 eV in Figures 7.13(a) and 7.13(b).

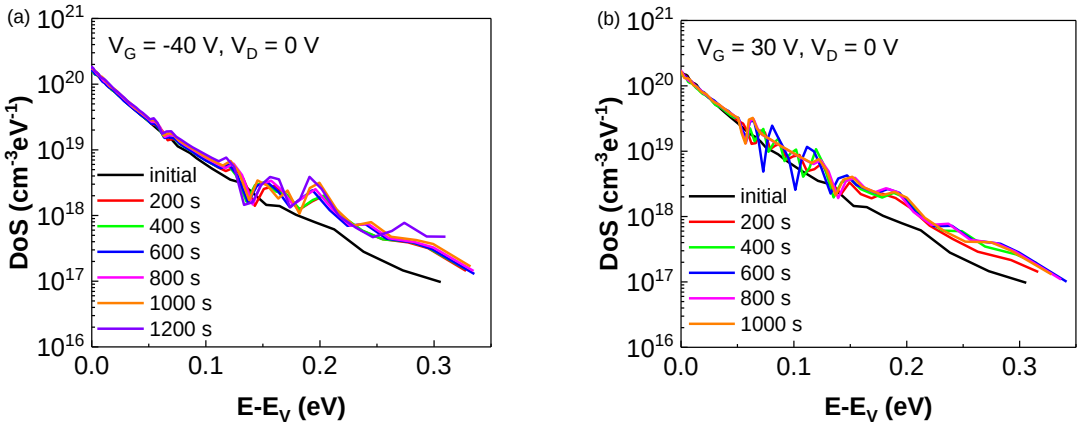

Figure 7.13 The distribution of density of state as a function of E-E_V with a stress conditions of (a) NBS V_G = -40 V, V_D = 0 V and (b) PBS V_G = 30 V, V_D = 0 V illuminated at 460 nm with variation of stress time**.**

7.2.2.3 Effect of intensity

In the previous section, the light intensity was held constant at 0.31 mW/cm^2. Here the device characteristics were measured in the dark after applying NBS and PBS for 600 s with intensity (irradiance) between 0.05 mW/cm^2 and 0.49 mW/cm^2. As shown in Figures 7.14(a) and (b), the transfer characteristics shifted to more positive voltage as the intensity increased and, as before, the shifts are greater for PBS.

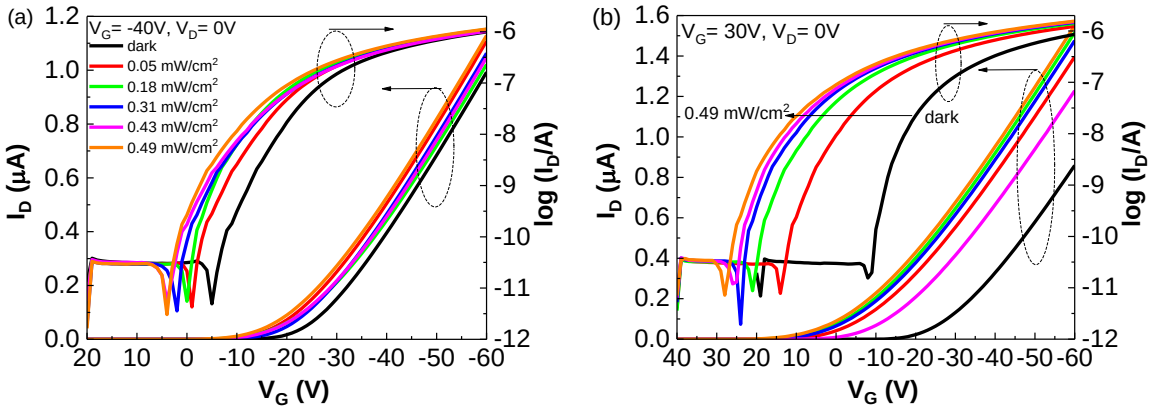

Figure 7.14 Transfer characteristics with stress conditions of (a) NBS V_G = -40 V, V_D = 0 V and (b) PBS V_G = 30 V, V_D = 0 V illuminated with different intensities of light of 460 nm wavelength.

The dependence of ΔV_{ON} ΔV_T, ΔSS and $\Delta\mu$ on illumination intensity both with and without bias are shown in Figure 7.15. It is clear that in without bias and under PBS, ΔV_{ON}, ΔV_T, and ΔSS increased rapidly but tended to saturate at higher intensities. Negative bias stress, however, suppressed the positive shifts in ΔV_T and ΔV_{ON}. Without bias stress, ΔV_{ON} and ΔV_T lay between the values extracted for NBS and PBS in the dark. Interestingly, the reduction in ΔV_{ON} with NBS is much greater than the increase arising from PBS. . Only a slight change is observed in ΔSS in the presence of PBS while $\Delta\mu$ was nearly unchanged regardless the bias stress conditions.

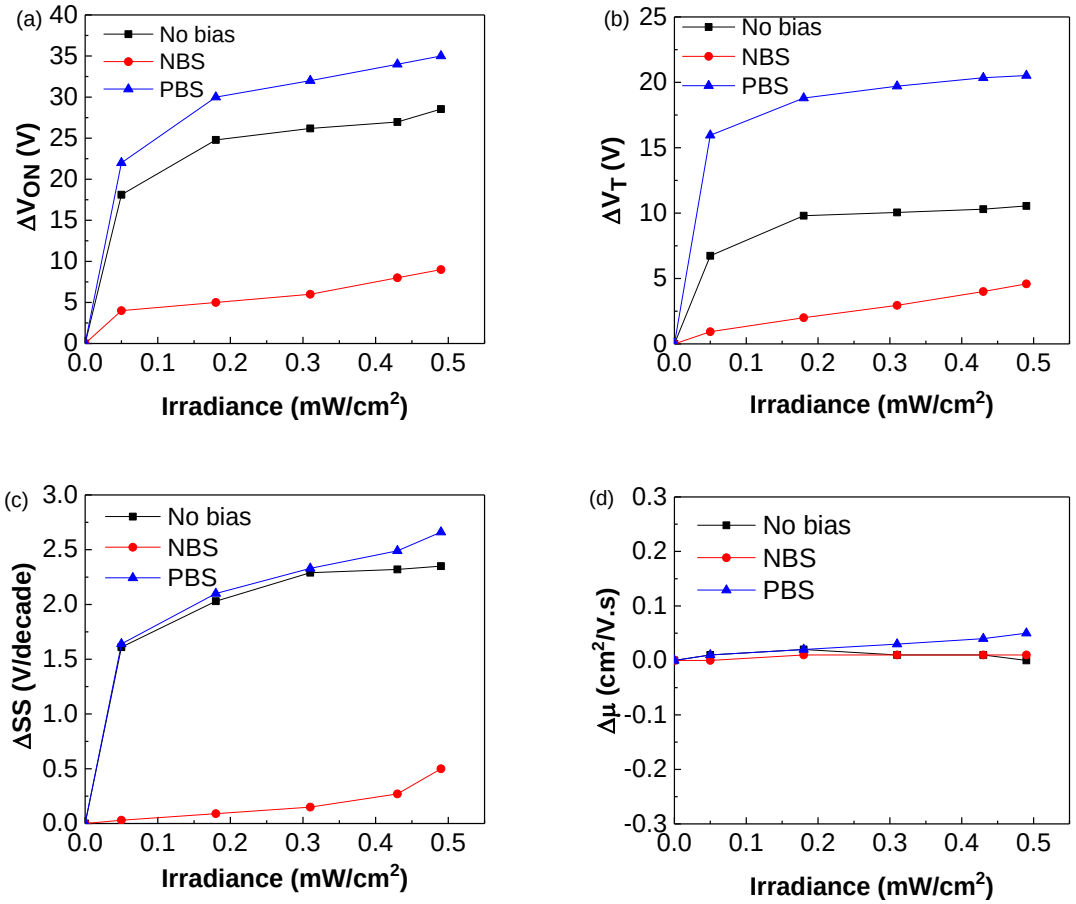

Figure 7.15 Shifts of (a) turn-on voltage, ΔV_{ON}, (b) threshold voltage, ΔV_T, (c) subthreshold slope, ΔSS and (d) maximum mobility, $\Delta\mu$ as a function of illumination intensity without and with bias.

Figure 7.16(a) gives the dependence of maximum photosensitivity, P_{MAX}, on illumination intensity. As can be seen, P_{MAX} increases under positive bias stress while under negative gate

bias stress, the response is suppressed. On the other hand, as intensity increases, the maximum photoresponsivity, R_{MAX}, is found to decrease, but tended to saturate at higher intensities (Figure 7.16(b)). The DoS plotted as a function of E-E_V for different light intensities is shown in Figures 7.17(a) and (b). Reflecting the change in SS, new features appear in the DoS suggesting the creation of new states deeper than 0.10 eV. However, the DoS is relatively insensitive to changes in intensity, suggesting that these are not real.

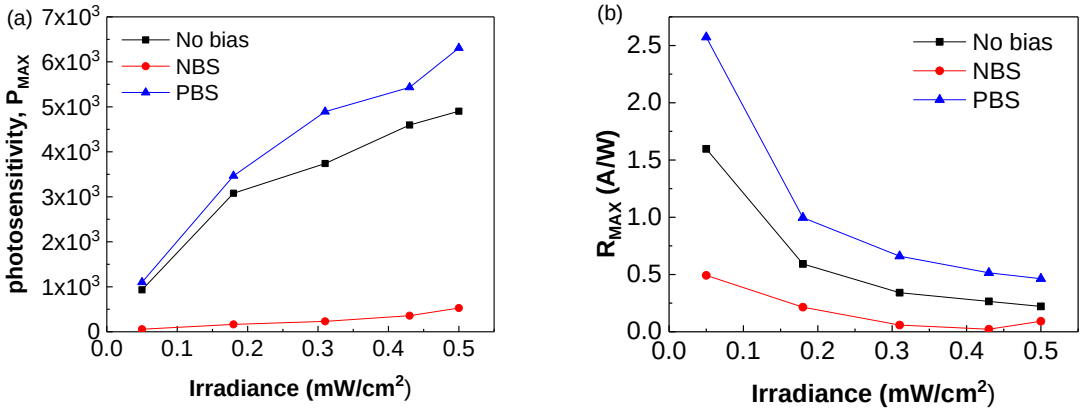

Figure 7.16 Maximum (a) photosensitivity, P_{MAX} and (b) photoresponsivity, R_{MAX} in a PS-DNTT TFT with and without bias stress and plotted as a function of the intensity of the 460 nm illumination.

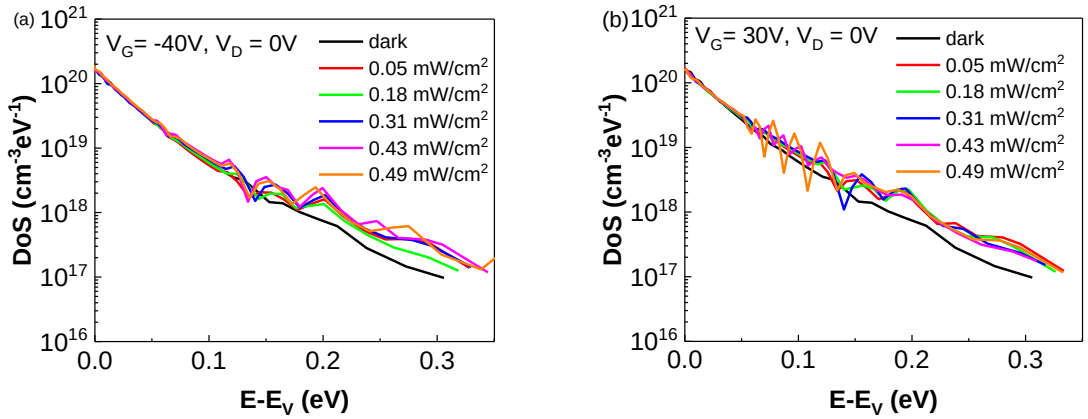

Figure 7.17 The distribution of density of state as a function of E-E_V with a stress conditions of (a) NBS V_G = -40 V, V_D= 0V and (b) PBS V_G = 30V, V_D = 0V illuminated at different intensities.

7.3 Discussion

The combined effect of bias stress and ambient light on the electrical performance of a PS-DNTT TFT has been investigated. For $\lambda > 460$ nm all curves shifted negatively similar to that induced by negative bias stress in the dark. This can be explained by the dominating effect of hole trapping at the PS-DNTT interface [90]. Furthermore, under the prevailing electrical conditions, the photogenerated electrons will move away from the interface. However when $\lambda = 460$ nm, the transfer characteristic shifted positively due to a high photogeneration rate of electron-hole pairs in the DNTT.

Interestingly, under PBS, all the transfer characteristics exhibit a parallel shift towards more positive voltages, with significant change in shape in the subthreshold region, regardless of the wavelength. Moreover the DoS distribution exhibited a clear increase in deep trap states between ~0.15 eV and ~0.35 eV above E_V. Since these are almost independent of intensity and with no significant changes in mobility suggests that that the observed changes in the DoS are not real. Rather this effect is explained by changes in occupancy of traps at the interface due to detrapping of electrons/holes which cause an unstable flatband voltage resulting in $\Delta V_T < \Delta V_{ON}$. The identical off-current at the start of the post-illumination sweeps with the dark current (Figure 7.5(b)) suggests trapping of photo-induced charges in shallow bulk traps since these carriers could detrap very fast.

A similar effect has been observed previously without the presence of bias stress but only at 460 nm. This indicates that the addition of PBS increases the rate of electron trapping regardless of the wavelength. As pointed out in the previous chapter the effect of the electron quasi Fermi level, QFL, is dependent on light intensity and can also explain the fast transient behavior. This is unlikely to be the case here since ΔV_T, ΔV_{ON}, ΔSS and R_{MAX} (Figures 7.15(a), (b) and (c), and 7.16(b)) appear to saturate at higher intensity due to trap limited effect. Interestingly the difference in ΔV_{ON} between PBS and no bias is smaller than ΔV_T between PBS and no bias (Figures 7.15(a) and (b)). As shown in Figure 7.7(d), shifting the linear plots by ΔV_T only reproduces the dark characteristics above $V_G = -50$ V. This suggests under PBS, the concentration of trapped electrons is increased thus a larger gate voltage is needed to detrap/neutralize electrons.

7.4 Summary

The effect of bias stress and illumination on PS-DNTT devices was investigated with different wavelengths, time and intensity. Under NBS, for $\lambda \geq 520$ nm, the phototransistor transfer characteristic shows a parallel shift toward more negative voltages due to the dominant effect of hole trapping at the PS-DNTT interface. On the other hand, for $\lambda = 460$ nm, the phototransistor transfer characteristic shifted positively. Unlike for the NBS case, the phototransistor transfer characteristic shifted positively under PBS regardless of the wavelength. Increased time effectively increases ΔV_T and ΔV_{ON} under PBS but NBS suppresses both parameters. Increased illumination intensity saturates trap occupancy resulting in the saturation of ΔV_T, ΔV_{ON}, ΔSS and R_{MAX} at higher intensity. As there is no change in the gate-voltage dependence of mobility, it is unlikely that the observed changes in the DoS are due to the creation of deep hole trap states in the band gap of DNTT. Furthermore, the changes seen in the DoS spectra are apparently almost independent of intensity. Therefore it is believed that the effect is due to changes in trap occupancy resulting in an unstable flat-band voltage shift. This is consistent with $\Delta V_{ON} > \Delta V_T$. The accumulation of holes in the channel as the device turns on neutralizes the trapped electrons, either by direct recombination or by interface hole trapping. Band bending is such that electron detrapping can also occur.

8 Conclusion

8.1 Conclusion

The work reported in this thesis is concerned with the environmental and electrical stability of OTFT based on DNTT as the semiconductor and PS as the dielectric. The main experimental technique was to analyze transfer characteristics and extract shifts in V_{ON} and V_T under influence of humidity, temperature, bias stress and light. Using the Grünewald model, the density of states, spectra were derived from transfer characteristics obtained in the linear regime. This allowed us to identify the presence of the traps either in the bulk semiconductor, bulk dielectric or at the interface between semiconductor and dielectric.

In Chapter 4, the effect on relative humidity and temperature on the density of states in thin film transistors based on PS-DNTT OTFT was investigated. It was observed that V_{ON} and V_T shifted negatively as RH% and T increased. This is believed due to hole trapping at the interface or in the insulator. However, mobility increased slightly with temperature from 1.00 to 1.25 cm^2/Vs and fits the model for hopping conduction in a 2-dimensional sheet with T_0 = 288 K. It was observed that the DoS in DNTT is insensitive to the relative humidity in the range 20 – 80%. As temperature increases, the only change observed in the DoS was a slight increase in the deeper states lying more than ~0.3 eV above the mobility edge.

In Chapter 5, it was shown that the main feature for negative gate bias stress is a negative shift in threshold/turn-on voltage related to hole trapping within the PS gate dielectric, and/or at the DNTT/PS interface. Under simultaneous gate-source and drain-source bias (V_G=V_D), slower changes are seen in ΔV_T and ΔV_{ON} compared to a bias stress with zero drain voltage (V_D = 0V). This is because of the zero potential difference between the gate and drain electrode which leads to a reduction in the number of charge carriers available for trapping towards the drain end of the channel. ΔV_T and ΔV_{ON} during stressing do depend on the drain-source bias but does not influence the trapping time, τ, extracted by fitting the stretched exponential function to the data. Application of the stretched exponential function to the threshold voltage shift ΔV_T based on the assumption that $\Delta V_T(\infty) = V_T(\infty) - V_T(0)$ shows an excellent fit to the drain current decay. Contrary to most previous reports, the threshold voltage at long times, $V_T(\infty)$, asymptotes to a value that is far lower than the applied gate

voltage. This was attributed to a low interface trap density in our devices, which limits the extent of any change in flat-band voltage. This gives rise to a smaller ΔV_T, and a shorter time-constant for the trapping process, although values for the parameter β are similar to those reported by others.

The different trajectories of the drain current decay insuccessive measurements indicate that that relaxation to the initial state when illuminated was not identical for each run suggesting that device relaxation may not necessarily be the result of detrapping but due to interface trapping of counter charges. Adding bias stress to devices under different RH% revealed a slight increase in both ΔV_T and ΔV_{ON}. Reducing RH under bias stress does not change the DoS in the DNTT film. Adding bias stress to a device at high temperatures leads to slight changes in both ΔV_T and ΔV_{ON}. The dependence of mobility on temperature can be described equally well by Arrhenius and 2-D hopping conduction models. However the extracted, T_0 was lower than observed when investigating the effects related to temperature alone in Chapter 4. A very minimal change in the behavior of the DoS was observed in comparison to changes already taking place with just temperature.

It has been shown that positive gate bias stress causes shifts in threshold voltage towards more positive voltage due to electron trapping at the interface. The shift in turn-on voltage ΔV_{ON} with increasing stress time is much greater than for ΔV_T suggesting that trapped electrons were neutralized as the gate voltage sweeps towards negative voltage. As there is no change in the gate-voltage dependence of mobility, it is unlikely that the change in the subthreshold slope is due to the creation of deep trap states in the DNTT but rather due to an unstable flatband voltage so that $\Delta V_T(\infty) < \Delta V_{ON}(\infty)$.

In Chapter 6, the effect of illumination on PS-DNTT devices was investigated with light of different wavelengths and intensities. The phototransistor characteristics shifted positively regardless of the wavelength, with the greatest effects being observed at 460 nm. For $\lambda \geq 520$ nm, the flat-band voltage shift, ΔV_{FB}, caused by electron trapping at the interface is the dominant mechanism with only minimal change in the shape of the subthreshold region and no significant change in either the DoS spectrum or the gate-voltage dependence of the field effect mobility. Illumination at λ = 460 nm did apparently change the profile of the deeper states in the DoS spectrum reflecting the significant change in the subthreshold slope.

However, it is argued that the observed changes in the DoS are not real. They are almost independent of intensity, though it is found later that the $\Delta V_{T,} \Delta V_{ON}$, ΔSS and R_{max} appear to saturate at higher intensity due to a trap limited effect. No significant changes are observed in mobility. Rather the effect is explained due to (i) trapping of photogenerated electrons, (ii) an unstable shift in the light-induced flat-band ΔV_{FB}, caused by detrapping or neutralization of electrons as the transistor is turned on so that $\Delta V_{T}(\infty) < \Delta V_{ON}(\infty)$, (iii) accumulation of electrons in DNTT near to the source contact or (iv) the effect of the electron quasi Fermi level, QFL. It has been shown that the fast transient behaviour of the I_D response to 460 nm illumination pulses under positive (V_G = 5 V, V_D = -1V) and negative bias stresses (V_G = -40 V, V_D = -1 V) are consistent with the effect of the electron QFL and also electron accumulation in DNTT near the source contact. On the other hand, the slow dynamic response under illumination and during the light-off period again arises from de-trapping/neutralization of trapped electrons as soon as the light is terminated. However, the post-illumination I_D does not recover to its pre-irradiation state when the light is turned off. Under positive bias stress, it is presumed that some of the deeply trapped electrons may not de-trap. These residual trapped electrons increase cumulatively at the start of the successive illumination periods, resulting in an increased response on a steadily increasing background under positive bias stress. Under negative bias stress the dynamic response decreases but on a steadily decreasing background similar to the dark bias stress effect, suggesting the presence of holes either trapped in interface states or de-trapping/neutralization of electrons in interfacial traps.

In Chapter 7, the effect of bias stress and illumination on PS-DNTT devices was investigated with different wavelengths, time and intensity. For $\lambda \geq 520$ nm, the phototransistor transfer characteristic shows a parallel shift toward more negative voltages under NBS due to the dominant effect of hole trapping at the PS-DNTT interface. Under PBS, both ΔV_T and ΔV_{ON} increase regardless of the wavelength. Increased time effectively increases ΔV_T and ΔV_{ON} under PBS but NBS suppresses both parameters. Increased illumination intensity saturates trap occupancy resulting in the saturation of $\Delta V_{T,} \Delta V_{ON}$, ΔSS and R_{MAX} at the higher intensity. It is assumed that the observed changes in the DoS are not due to the creation of deep hole trap states in the band gap of DNTT because the changes seen are apparently almost independent of intensity with no significant changes observed in mobility. This can be

explained by changes in trap occupancy resulting in an unstable flat-band voltage shift. This is consistent with $\Delta V_{ON} > \Delta V_T$. The accumulation of holes in the channel as the device turns on neutralizes the trapped electrons, either by direct recombination or by interface hole trapping. Band bending is such that electron detrapping can also occur.

The results presented in this thesis demonstrate that the PS-DNTT system is stable and worth considering for circuit fabrication. Although the subthreshold slope is relatively high ~ 4.0 V/decade the subthreshold slope could be reduced significantly by using much thinner dielectrics with much higher C_i gate dielectric for faster switching of the OTFT. Furthermore, a significant increase in drain current leading to photosensitivity ~10^4 under the blue and ambient light in PS-DNTT OTFT indicates that it could have promising applications in photosensing.

8.2 Future work

In order to gain more understanding of the trapping mechanisms and identifying the origin of the degradation, it would be necessary to investigate the chemical changes in the PS-DNTT OTFT using the techniques such as charge accumulation technique, CAS spectroscopy. Access to such equipment would allow changes due to the chemical interaction of the semiconductor with O_2 and H_2O to be identified [114] and compared to the results obtained from electrical measurements.

Previous reports showed that DNTT with TPGDA as the dielectric and PS as the buffer layer exhibits excellent performance as individual transistors and in organic circuits [3, 15]. Therefore it would be interesting also to investigate the trapping behavior with TPGDA and PS as the dielectric material and to compare with TPGDA alone. Follow up experiments can be undertaken to verify the trapped charge using scanning Kelvin Probe Microscopy (SKPM).

In comparison to the p-type material, n-type semiconductors are less developed. Therefore it would be interesting to investigate n-type TFT with TPGDA/PS or other dielectrics with comparable mobility and V_T to those in DNTT. The environmental and electrical stability of the n-type TFT could then be followed by fabrication of n-type organic circuits such as

inverter, ring oscillators and logic gates. It would also be interesting to develop complementary circuits with DNTT as the p-type semiconductor. However, to achieve continuous R2R compatible vacuum deposition, PS needs to be replaced by an evaporable dielectric buffer layer. One of the options is using n-octylphosphonic acid (C8PA) [15]. Another option is to replace TPGDA with other vacuum evaporated material.

APPENDIX A

A. The form of the V_0 vs V_F plot for constant mobility in the linear regime of operation

In Chapter 2, section 2.6.4, Equation (2.16) i.e.

$$\exp(\beta V_0) + \beta V_0 - 1 = \beta \frac{C_i l}{\varepsilon_S \varepsilon_0 I_0}\left[V_F I(V_F) - \int_0^{V_F} I(\tilde{V}_F) d\tilde{V}_F \right] \tag{A.1}$$

was derived by Grünewald et al [32] and is the starting point for the following derivation . When V_0 is greater than a few kT the exponential term on the left side of equation (A.1) dominates so that,

$$\exp(\beta V_0) = C_1\left[V_F I(V_F) - \int_0^{V_F} I(\tilde{V}_F) d\tilde{V}_F \right] \tag{A.2}$$

where

$$C_1 = \beta \frac{C_i l}{\varepsilon_s \varepsilon_0 I_0}.$$

When the mobility, μ, becomes independent of gate voltage, the transfer plot becomes linear following equation (2.10) in Chapter 2 of section 2.6.3. Therefore,

$$I_D = K[(V_G - V_T)] = K[V_F + V_{ON} - V_T]$$

with

$$K = \frac{W C_i V_D}{L}.$$

Referring to Figure A1, if the transfer plot becomes linear at V_{FL}, then equation (A.2) can be rewritten as

$$\exp(\beta V_0) = C_1\left[V_F K(V_F + V_{ON} - V_T) - \int_{V_{FL}}^{V_F} K(\tilde{V}_F + V_{ON} - V_T) d\tilde{V}_F - C_2 \right] \tag{A.3}$$

where C_2 is a constant given by

$$C_2 = \int_0^{V_{FL}} I(\tilde{V}_F) d\tilde{V}_F$$

Integrating equation (A.3) then yields

$$\exp(\beta V_0) = C_1 K \left[\frac{V_F^2}{2} + \frac{V_{FL}^2}{2} + V_{FL}(V_{ON} - V_T) - C_2 \right]$$

i.e.

$$\exp(\beta V_0) = \alpha_1 (V_F^2 + \alpha_2)$$

or

$$V_0 = \frac{1}{\beta} \ln \alpha_1 (V_F^2 + \alpha_2), \qquad V_F > V_{FL}. \tag{A.4}$$

Here $\alpha_{1,2}$ are constants given by

$$\alpha_1 = \frac{Wl}{2L} \cdot \frac{\beta \mu C_i^2}{\varepsilon_S \varepsilon_0 I_0} \quad \text{and} \quad \alpha_2 = \left(V_{FL}^2 + 2V_{FL}(V_{ON} - V_T) - \frac{2L}{W \mu C_i V_D} \int_0^{V_{FL}} I(\tilde{V}_F) d\tilde{V}_F \right)$$

and can be evaluated from device parameters and the numerical integration of the transfer curve, $I(V_F)$, below V_{FL}. Equation (A.4) shows that when the mobility becomes constant, which we assume occurs as the Fermi level crosses the mobility/valence band edge, the plot of V_0 vs V_F will not saturate. Rather, for the device parameters relevant to this work, the plot will continue to rise approximately linearly over the range of gate voltage applied.

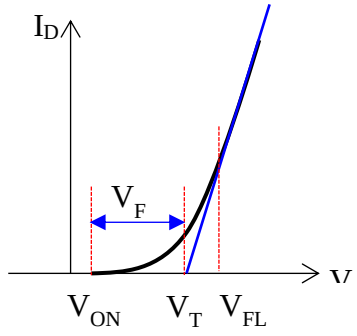

Figure A.1 Transfer characteristics showing V_{ON}, V_T, V_F and V_{FL}.

APPENDIX B

B. Construction Used to Estimate the Mobility (Valence Band) Edge

To estimate the mobility/valence band edge, the following procedure was used. Firstly, draw a tangent to the mobility-V_G plot as shown in Figure B.1(a) to estimate the mobility edge, The voltage, V_G, at which the tangent departs the experimental curve is noted and corrected for V_{ON} to give V_F, i.e $V_F = V_G - V_{ON}$ =-49-(-3)= -46 V. This value is then used to extract the relevant value of V_0, Figure B.1(b). Interestingly, the tangent drawn to the linearly rising section of the V_0 vs V_F plot departs the plot at the same V_F identified from the mobility plot. This value of V_0 is then assumed to be the degree of band bending when E_F crosses the mobility (valence band) edge.

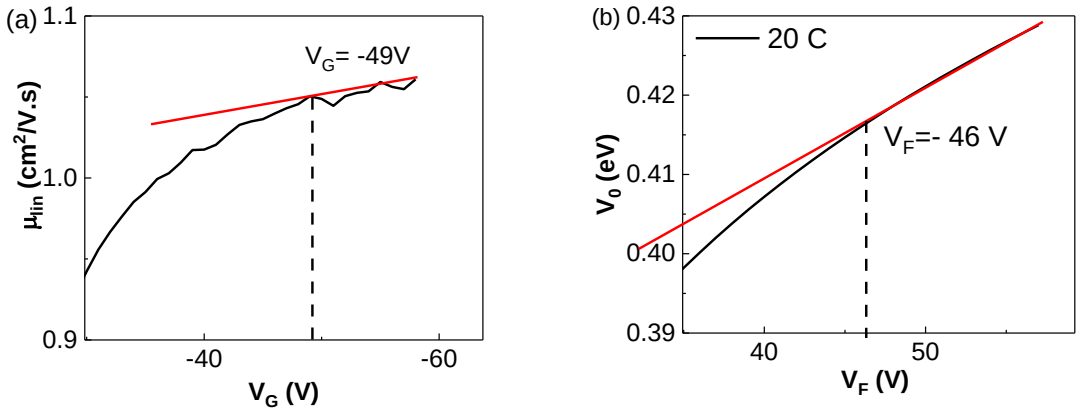

Figure B.1 Constructions used to estimate onset of mobility edge.

APPENDIX C

C. Sensitivity Analysis of DoS

Correctly identifying the flatband condition is clearly important for properly assigning the DoS energy range. In this section, a sensitivity analysis is done by using the same experimental transfer plot - that for T = 20°C and RH = 10% in Figure 4.8(b) - and systematically change the values of V_{ON} (section C.2) and I_{OFF} (section C.3) used for calculating the DoS.

i. Effect of V_{ON}

Here we test the sensitivity of the DoS calculations to errors in correctly identifying the voltage, V_{0N}, corresponding to the flatband condition. In the results given in the main text for T = 20°C and RH = 10%, V_{ON} was estimated to be -3 V. In Figure S3 is shown the effect of changing the value over the range 1 to -6 V. As can be seen, this results in a minor shift in the V_0 vs V_F plots (a), resulting in a minimal effect on the DoS whether plotted relative to (b) E_F or (c) E_V. The main effect is on the magnitude of the trap feature at ~0.25 eV.

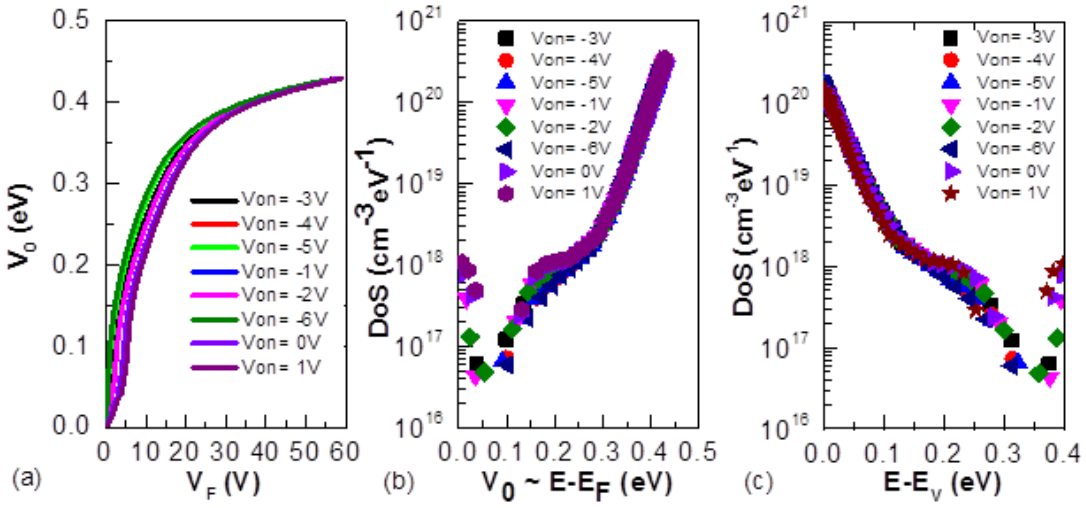

Figure C.1 Effect of V_{ON} on (a) V_0 vs V_F and DoS as a function of (b) V_0 and (c) E-E_V

ii. Effect of I_{OFF}

Here we test the sensitivity of the DoS calculations to errors in correctly identifying the flatband current, I_{0FF}. If parasitic currents are present, I_{OFF} will be overestimated. Accordingly, we investigated the effect of reducing I_{OFF} from 10 pA down to 0.1 pA. Interestingly, plots of V_0 vs V_F and DoS vs V_0 show systematic changes with choice of I_{OFF} as shown in Figure C.2(b). However, when DoS is plotted relative to the mobility edge, all plots coalesce to the same DoS confirming that when plotted in this form, the extracted DoS is insensitive to the value chosen for I_{OFF}.

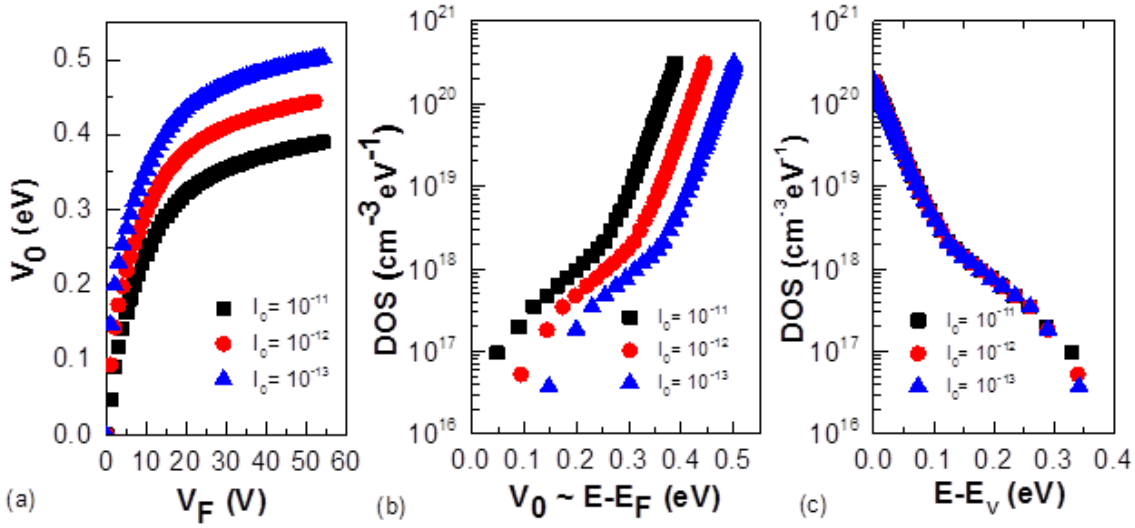

Figure C.2 Effect of I_{0FF} on (a) the plot of V_0 vs V_F and on the DOS as a function of (b) V_0 and (c) E-E_V.

REFERENCES

[1] C. P. Watson, B. A. Brown, J. Carter, J. Morgan, and D. M. Taylor, "Organic Ring Oscillators with Sub-200 Ns Stage Delay Based on a Solution-Processed P-Type Semiconductor Blend," *Advanced Electronic Materials,* vol. 2, 2016.

[2] S. D. Ogier, H. Matsui, L. Feng, M. Simms, M. Mashayekhi, J. Carrabina, L. Terés, and S. Tokito, "Uniform, High Performance, Solution Processed Organic Thin-Film Transistors Integrated in 1 MHz Frequency Ring Oscillators," *Organic Electronics,* vol. 54, pp. 40-47, 2018.

[3] E. R. Patchett, A. Williams, Z. Ding, G. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, and D. M. Taylor, "A High-Yield Vacuum-Evaporation-Based R2R-Compatible Fabrication Route for Organic Electronic Circuits," *Organic Electronics,* vol. 15, pp. 1493-1502, 2014.

[4] J. Noh, M. Jung, K. Jung, G. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, and V. Subramanian, "Fully Gravure-Printed D Flip-Flop on Plastic Foils Using Single-Walled Carbon-Nanotube-Based TFTs," *IEEE Electron Device Letters,* vol. 32, pp. 638-640, 2011.

[5] U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern, and H. Klauk, "Flexible Low-Voltage Organic Transistors and Circuits Based on a High-Mobility Organic Semiconductor with Good Air Stability," *Advanced Materials,* vol. 22, pp. 982-985, 2010.

[6] A. Reuveny, S. Lee, T. Yokota, H. Fuketa, C. M. Siket, S. Lee, T. Sekitani, T. Sakurai, S. Bauer, and T. Someya, "High-Frequency, Conformable Organic Amplifiers," *Advanced Materials,* vol. 28, pp. 3298-3304, 2016.

[7] F. Ante, D. Kälblein, T. Zaki, U. Zschieschang, K. Takimiya, M. Ikeda, T. Sekitani, T. Someya, J. N. Burghartz, and K. Kern, "Contact Resistance and Megahertz Operation of Aggressively Scaled Organic Transistors," *Small,* vol. 8, pp. 73-79, 2012.

[8] J. A. Avila-Niño, E. R. Patchett, D. M. Taylor, H. E. Assender, S. G. Yeates, Z. Ding, and J. J. Morrison, "Stable Organic Static Random Access Memory from a Roll-to-Roll Compatible Vacuum Evaporation Process," *Organic Electronics,* vol. 31, pp. 77-81, 2016/04/01/ 2016.

[9] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, and J. Blochwitz-Nimoth, "Dinaphtho [2, 3-b: 2′, 3′-f] thieno [3, 2-b] thiophene (DNTT) Thin-Film Transistors with Improved Performance and Stability," *Organic Electronics,* vol. 12, pp. 1370-1375, 2011.

[10] G. A. Abbas, Z. Ding, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett, and D. M. Taylor, "A High-Yielding Evaporation-Based Process for Organic

Transistors Based on the Semiconductor DNTT," *Organic Electronics,* vol. 15, pp. 1998-2006, 2014.

[11] D. M. Taylor, E. R. Patchett, A. Williams, Z. Ding, H. E. Assender, J. J. Morrison, and S. G. Yeates, "Fabrication and Simulation of Organic Transistors and Functional Circuits," *Chemical Physics,* vol. 456, pp. 85-92, 2015.

[12] D. M. Taylor, "Vacuum-Thermal-Evaporation: The Route for Roll-to-Roll Production of Large-Area Organic Electronic Circuits," *Semiconductor Science and Technology,* vol. 30, p. 054002, 2015.

[13] G. Abbas, H. Assender, M. Ibrahim, and D. M. Taylor, "Organic Thin-Film Transistors with Electron-Beam Cured and Flash Vacuum Deposited Polymeric Gate Dielectric," *Journal of Vacuum Science & Technology B,* vol. 29, p. 052401, 2011.

[14] G. Abbas, Z. Ding, K. Mallik, H. Assender, and D. M. Taylor, "Hysteresis-Free Vacuum-Processed Acrylate–Pentacene Thin-Film Transistors," *IEEE Electron Device Letters,* vol. 34, pp. 268-270, 2013.

[15] D. M. Taylor, E. R. Patchett, A. Williams, N. J. Neto, Z. Ding, H. E. Assender, J. J. Morrison, and S. G. Yeates, "Organic Digital Logic and Analog Circuits Fabricated in a Roll-to-Roll Compatible Vacuum-Evaporation Process," *IEEE Transactions on Electron Devices,* vol. 61, pp. 2950-2956, 2014.

[16] S. Hannah, J. Cardona, D. A. Lamprou, P. Šutta, P. Baran, A. Al Ruzaiqi, K. Johnston, and H. Gleskova, "Interplay between Vacuum-Grown Monolayers of Alkylphosphonic Acids and the Performance of Organic Transistors Based on Dinaphtho [2, 3-b: 2′, 3′-f] thieno [3, 2-b] thiophene," *ACS Applied Materials & Interfaces,* vol. 8, pp. 25405-25414, 2016.

[17] T. Yamamoto and K. Takimiya, "Facile Synthesis of Highly Π-Extended Heteroarenes, Dinaphtho [2,3-b:2‘,3‘-f] chalcogenopheno [3,2-b] chalcogenophenes, and Their Application to Field-Effect Transistors," *Journal of the American Chemical Society,* vol. 129, pp. 2224-2225, 2007.

[18] G. Horowitz, R. Hajlaoui, and P. Delannoy, "Temperature Dependence of the Field-Effect Mobility of Sexithiophene. Determination of the Density of Traps," *Journal de Physique III,* vol. 5, pp. 355-371, 1995.

[19] F. Di Girolamo, C. Aruta, M. Barra, P. D’Angelo, and A. Cassinese, "Organic Film Thickness Influence on the Bias Stress Instability in Sexithiophene Field Effect Transistors," *Applied Physics A,* vol. 96, pp. 481-487, 2009.

[20] D. Guo, T. Miyadera, S. Ikeda, T. Shimada, and K. Saiki, "Analysis of Charge Transport in a Polycrystalline Pentacene Thin Film Transistor by Temperature and Gate Bias Dependent Mobility and Conductance," *Journal of Applied Physics,* vol. 102, p. 023706, 2007.

[21] M. Vissenberg and M. Matters, "Theory of the Field-Effect Mobility in Amorphous Organic Transistors," *Physical Review B,* vol. 57, p. 12964, 1998.

[22] N. Mott, "Conduction in Glasses Containing Transition Metal Ions," *Journal of Non-Crystalline Solids,* vol. 1, pp. 1-17, 1968.

[23] N. Lustig and W. Howard, "Variable Range Hopping Conductivity in Hydrogenated Amorphous Silicon Thin Film Transistors," *Solid State Communications,* vol. 72, pp. 59-61, 1989.

[24] J. Wang and C. Jiang, "Electrical Transport Mechanism of Single Monolayer Pentacene Film Employing Field-Effect Characterization," *Organic Electronics,* vol. 16, pp. 164-170, 2015.

[25] A. Aleshin, H. Sandberg, and H. Stubb, "Two-Dimensional Charge Carrier Mobility Studies of Regioregular P3ht," *Synthetic Metals,* vol. 1, pp. 1449-1450, 2001.

[26] B. Hamadani and D. Natelson, "Gated Nonlinear Transport in Organic Polymer Field Effect Transistors," *Journal of Applied Physics,* vol. 95, pp. 1227-1232, 2004.

[27] J. A. Carr and S. Chaudhary, "The Identification, Characterization and Mitigation of Defect States in Organic Photovoltaic Devices: A Review and Outlook," *Energy & Environmental Science,* vol. 6, pp. 3414-3438, 2013.

[28] S. Himmelberger, J. Dacuña, J. Rivnay, L. H. Jimison, T. McCarthy-Ward, M. Heeney, I. McCulloch, M. F. Toney, and A. Salleo, "Effects of Confinement on Microstructure and Charge Transport in High Performance Semicrystalline Polymer Semiconductors," *Advanced Functional Materials,* vol. 23, pp. 2091-2098, 2013.

[29] O. D. Jurchescu, J. Baas, and T. T. Palstra, "Effect of Impurities on the Mobility of Single Crystal Pentacene," *Applied Physics Letters,* vol. 84, pp. 3061-3063, 2004.

[30] W. L. Kalb, S. Haas, C. Krellner, T. Mathis, and B. Batlogg, "Trap Density of States in Small-Molecule Organic Semiconductors: A Quantitative Comparison of Thin-Film Transistors with Single Crystals," *Physical Review B,* vol. 81, p. 155315, 2010.

[31] W. L. Kalb and B. Batlogg, "Calculating the Trap Density of States in Organic Field-Effect Transistors from Experiment: A Comparison of Different Methods," *Physical Review B,* vol. 81, p. 035327, 2010.

[32] M. Grünewald, P. Thomas, and D. Würtz, "A Simple Scheme for Evaluating Field Effect Data," *Physica Status Solidi (B),* vol. 100, pp. K139-K143, 1980.

[33] K. Weber, M. Grünewald, W. Fuhs, and P. Thomas, "Field Effect in a-Si:H Films. Influence of Annealing and Light Exposure," *Physica Status Solidi (B),* vol. 110, pp. 133-142, 1982.

[34] P. Pattanasattayavong, A. D. Mottram, F. Yan, and T. D. Anthopoulos, "Study of the Hole Transport Processes in Solution-Processed Layers of the Wide Bandgap Semiconductor Copper (I) Thiocyanate (CuSCN)," *Advanced Functional Materials,* vol. 25, pp. 6802-6813, 2015.

[35] S. Hunter, A. D. Mottram, and T. D. Anthopoulos, "Temperature and Composition-Dependent Density of States in Organic Small-Molecule/Polymer Blend Transistors," *Journal of Applied Physics,* vol. 120, p. 025502, 2016.

[36] P. J. Diemer, J. Hayes, E. Welchman, R. Hallani, S. J. Pookpanratana, C. A. Hacker, C. A. Richter, J. E. Anthony, T. Thonhauser, and O. D. Jurchescu, "The Influence of Isomer Purity on Trap States and Performance of Organic Thin-Film Transistors," *Advanced Electronic Materials,* vol. 3, 2017.

[37] N. K. Za'aba, J. J. Morrison, and D. M. Taylor, "Effect of Relative Humidity and Temperature on the Stability of DNTT Transistors: A Density of States Investigation," *Organic Electronics,* vol. 45, pp. 174-181, 2017.

[38] A. Brown, C. Jarrett, D. De Leeuw, and M. Matters, "Field-Effect Transistors Made from Solution-Processed Organic Semiconductors," *Synthetic Metals,* vol. 88, pp. 37-55, 1997.

[39] A. Rolland, J. Richard, J. Kleider, and D. Mencaraglia, "Electrical Properties of Amorphous Silicon Transistors and Mis-Devices: Comparative Study of Top Nitride and Bottom Nitride Configurations," *Journal of the Electrochemical Society,* vol. 140, pp. 3679-3683, 1993.

[40] A. Risteska, J. Bedolla, J. E. Northrup, W. Bergholz, V. Wagner, and D. Knipp, "Gap States in Small Molecule Thin-Film Transistors," *Advanced Electronic Materials,* vol. 2, 2016.

[41] M. L. Chabinyc, R. A. Street, and J. E. Northrup, "Effects of Molecular Oxygen and Ozone on Polythiophene-Based Thin-Film Transistors," *Applied Physics Letters,* vol. 90, p. 123508, 2007.

[42] S. Hoshino, M. Yoshida, S. Uemura, T. Kodzasa, N. Takada, T. Kamata, and K. Yase, "Influence of Moisture on Device Characteristics of Polythiophene-Based Field-Effect Transistors," *Journal of Applied Physics,* vol. 95, pp. 5088-5093, 2004.

[43] M. L. Chabinyc, F. Endicott, B. D. Vogt, D. M. DeLongchamp, E. K. Lin, Y. Wu, P. Liu, and B. S. Ong, "Effects of Humidity on Unencapsulated Poly(thiophene) Thin-Film Transistors," *Applied Physics Letters,* vol. 88, p. 113514, 2006.

[44] Y. H. Noh, S. Y. Park, S.-M. Seo, and H. H. Lee, "Root Cause of Hysteresis in Organic Thin Film Transistor with Polymer Dielectric," *Organic Electronics,* vol. 7, pp. 271-275, 2006.

[45] S. Hong, J. Choi, and Y. Kim, "Degraded Off-State Current of Organic Thin-Film Transistor and Annealing Effect," *IEEE Transactions on Electron Devices,* vol. 55, pp. 3602-3604, 2008.

[46] Z. Ding, G. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, E. R. Patchett, and D. M. Taylor, "Effect of Oxygen, Moisture and Illumination on the Stability and Reliability of Dinaphtho [2, 3-b: 2′, 3′-f] thieno [3, 2-b] thiophene (DNTT) OTFTs

During Operation and Storage," *ACS Applied Materials & Interfaces,* vol. 6, pp. 15224-15231, 2014.

[47] C. Goldmann, D. Gundlach, and B. Batlogg, "Evidence of Water-Related Discrete Trap State Formation in Pentacene Single-Crystal Field-Effect Transistors," *Applied Physics Letters,* vol. 88, p. 063501, 2006.

[48] T. Yokota, K. Kuribara, T. Tokuhara, U. Zschieschang, H. Klauk, K. Takimiya, Y. Sadamitsu, M. Hamada, T. Sekitani, and T. Someya, "Flexible Low-Voltage Organic Transistors with High Thermal Stability at 250 C," *Advanced Materials,* vol. 25, pp. 3639-3644, 2013.

[49] K. Kuribara, H. Wang, N. Uchiyama, K. Fukuda, T. Yokota, U. Zschieschang, C. Jaye, D. Fischer, H. Klauk, and T. Yamamoto, "Organic Transistors with High Thermal Stability for Medical Applications," *Nature Communications,* vol. 3, p. 723, 2012.

[50] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, and T. Sakurai, "Suppression of Dc Bias Stress-Induced Degradation of Organic Field-Effect Transistors Using Post-Annealing Effects," *Applied Physics Letters,* vol. 87, p. 073505, 2005.

[51] H. Sirringhaus, "Reliability of Organic Field-Effect Transistors," *Advanced Materials,* vol. 21, pp. 3859-3873, 2009.

[52] H. L. Gomes, P. Stallinga, F. Dinelli, M. Murgia, F. Biscarini, D. De Leeuw, T. Muck, J. Geurts, L. Molenkamp, and V. Wagner, "Bias-Induced Threshold Voltages Shifts in Thin-Film Organic Transistors," *Applied Physics Letters,* vol. 84, pp. 3184-3186, 2004.

[53] M. de Pauli, U. Zschieschang, I. D. Barcelos, H. Klauk, and A. Malachias, "Tailoring the Dielectric Layer Structure for Enhanced Carrier Mobility in Organic Transistors: The Use of Hybrid Inorganic/Organic Multilayer Dielectrics," *Advanced Electronic Materials,* vol. 2, 2016.

[54] A. Salleo, F. Endicott, and R. Street, "Reversible and Irreversible Trapping at Room Temperature in Poly(thiophene) Thin-Film Transistors," *Applied Physics Letters,* vol. 86, p. 263505, 2005.

[55] T. N. Ng, J. A. Marohn, and M. L. Chabinyc, "Comparing the Kinetics of Bias Stress in Organic Field-Effect Transistors with Different Dielectric Interfaces," *Journal of Applied Physics,* vol. 100, p. 084505, 2006.

[56] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, "Organic Small Molecule Field-Effect Transistors with Cytop™ Gate Dielectric: Eliminating Gate Bias Stress Effects," *Applied Physics Letters,* vol. 90, p. 092104, 2007.

[57] S. H. Kim, S. Nam, J. Jang, K. Hong, C. Yang, D. S. Chung, C. E. Park, and W.-S. Choi, "Effect of the Hydrophobicity and Thickness of Polymer Gate Dielectrics on the Hysteresis Behavior of Pentacene-Based Field-Effect Transistors," *Journal of Applied Physics,* vol. 105, p. 104509, 2009.

[58] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, "General Observation of N-Type Field-Effect Behaviour in Organic Semiconductors," *Nature,* vol. 434, p. 194, 2005.

[59] D. Kumaki, T. Umeda, and S. Tokito, "Influence of H_2O and O_2 on Threshold Voltage Shift in Organic Thin-Film Transistors: Deprotonation of SiOH on SiO_2 Gate-Insulator Surface," *Applied Physics Letters,* vol. 92, p. 78, 2008.

[60] G. Gu and M. G. Kane, "Moisture Induced Electron Traps and Hysteresis in Pentacene-Based Organic Thin-Film Transistors," *Applied Physics Letters,* vol. 92, p. 33, 2008.

[61] V. Podzorov and M. Gershenson, "Photoinduced Charge Transfer across the Interface between Organic Molecular Crystals and Polymers," *Physical Review Letters,* vol. 95, p. 016602, 2005.

[62] H. H. Choi, H. Najafov, N. Kharlamov, D. V. Kuznetsov, S. I. Didenko, K. Cho, A. L. Briseno, and V. Podzorov, "Polarization-Dependent Photoinduced Bias-Stress Effect in Single-Crystal Organic Field-Effect Transistors," *ACS Applied Materials & Interfaces,* vol. 9, pp. 34153-34161, 2017.

[63] C. P. Watson, M. Devynck, and D. M. Taylor, "Photon-Assisted Capacitance–Voltage Study of Organic Metal–Insulator–Semiconductor Capacitors," *Organic Electronics,* vol. 14, pp. 1728-1736, 2013.

[64] C. P. Watson, E. M. Lopes, R. F. de Oliveira, N. Alves, J. A. Giacometti, and D. M. Taylor, "Interface State Contribution to the Photovoltaic Effect in Organic Phototransistors: Photocapacitance Measurements and Optical Sensing," *Organic Electronics,* vol. 52, pp. 79-88, 2018/01/01/ 2018.

[65] D. M. Taylor, J. A. Drysdale, I. Torres, and O. Fernández, "Electron Trapping and Inversion Layer Formation in Photoexcited Metal-Insulator-Poly(3-hexylthiophene) Capacitors," *Applied Physics Letters,* vol. 89, p. 183512, 2006.

[66] S. Zilker, C. Detcheverry, E. Cantatore, and D. De Leeuw, "Bias Stress in Organic Thin-Film Transistors and Logic Gates," *Applied Physics Letters,* vol. 79, pp. 1124-1126, 2001.

[67] G. Gu, M. G. Kane, and S.-C. Mau, "Reversible Memory Effects and Acceptor States in Pentacene-Based Organic Thin-Film Transistors," *Journal of Applied Physics,* vol. 101, p. 014504, 2007.

[68] A. Benor, A. Hoppe, V. Wagner, and D. Knipp, "Electrical Stability of Pentacene Thin Film Transistors," *Organic Electronics,* vol. 8, pp. 749-758, 2007.

[69] R. Street, A. Salleo, and M. Chabinyc, "Bipolaron Mechanism for Bias-Stress Effects in Polymer Transistors," *Physical Review B,* vol. 68, p. 085316, 2003.

[70] R. Street, "Bias-Induced Change in Effective Mobility Observed in Polymer Transistors," *Physical Review B,* vol. 77, p. 165311, 2008.

[71] H. Gleskova, S. Gupta, and P. Šutta, "Structural Changes in Vapour-Assembled N-Octylphosphonic Acid Monolayer with Post-Deposition Annealing: Correlation with Bias-Induced Transistor Instability," *Organic Electronics,* vol. 14, pp. 3000-3006, 2013.

[72] M. Calhoun, C. Hsieh, and V. Podzorov, "Effect of Interfacial Shallow Traps on Polaron Transport at the Surface of Organic Semiconductors," *Physical Review Letters,* vol. 98, p. 096402, 2007.

[73] K. Pernstich, D. Oberhoff, C. Goldmann, and B. Batlogg, "Modeling the Water Related Trap State Created in Pentacene Transistors," *Applied Physics Letters,* vol. 89, p. 213509, 2006.

[74] A. Salleo and R. Street, "Light-Induced Bias Stress Reversal in Polyfluorene Thin-Film Transistors," *Journal of Applied Physics,* vol. 94, pp. 471-479, 2003.

[75] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk, "Bias Stress Effect in Low-Voltage Organic Thin-Film Transistors," *Applied Physics A,* vol. 95, pp. 139-145, 2009.

[76] M. Powell, "Charge Trapping Instabilities in Amorphous Silicon-Silicon Nitride Thin-Film Transistors," *Applied Physics Letters,* vol. 43, pp. 597-599, 1983.

[77] L. Wang, G. Liu, F. Zhu, F. Pan, and D. Yan, "Electrical Instability in Vanadyl-Phthalocyanine Thin-Film Transistors," *Applied Physics Letters,* vol. 93, p. 395, 2008.

[78] D. Kawakami, Y. Yasutake, H. Nishizawa, and Y. Majima, "Bias Stress Induced Threshold Voltage Shift in Pentacene Thin-Film Transistors," *Japanese Journal of Applied Physics,* vol. 45, p. L1127, 2006.

[79] S. Cipolloni, L. Mariucci, A. Valletta, D. Simeone, F. De Angelis, and G. Fortunato, "Aging Effects and Electrical Stability in Pentacene Thin Film Transistors," *Thin Solid Films,* vol. 515, pp. 7546-7550, 2007.

[80] S. G. Mathijssen, M. Cölle, H. Gomes, E. C. Smits, B. de Boer, I. McCulloch, P. A. Bobbert, and D. M. de Leeuw, "Dynamics of Threshold Voltage Shifts in Organic and Amorphous Silicon Field-Effect Transistors," *Advanced Materials,* vol. 19, pp. 2785-2789, 2007.

[81] H. H. Choi, W. H. Lee, and K. Cho, "Bias-Stress-Induced Charge Trapping at Polymer Chain Ends of Polymer Gate-Dielectrics in Organic Transistors," *Advanced Functional Materials,* vol. 22, pp. 4833-4839, 2012.

[82] U. Zschieschang, R. T. Weitz, K. Kern, and H. Klauk, "Bias Stress Effect in Low-Voltage Organic Thin-Film Transistors," *Applied Physics A: Materials Science & Processing,* vol. 95, pp. 139-145, 2009.

[83] H.-W. Zan and S.-C. Kao, "The Effects of Drain-Bias on the Threshold Voltage Instability in Organic TFTs," *IEEE Electron Device Letters,* vol. 29, pp. 155-157, 2008.

[84] H. H. Choi, M. S. Kang, M. Kim, H. Kim, J. H. Cho, and K. Cho, "Decoupling the Bias-Stress-Induced Charge Trapping in Semiconductors and Gate-Dielectrics of Organic Transistors Using a Double Stretched-Exponential Formula," *Advanced Functional Materials,* vol. 23, pp. 690-696, 2013.

[85] N. V. Subbarao, M. Gedda, P. K. Iyer, and D. K. Goswami, "Enhanced Environmental Stability Induced by Effective Polarization of a Polar Dielectric Layer in a Trilayer Dielectric System of Organic Field-Effect Transistors: A Quantitative Study," *ACS Applied Materials & Interfaces,* vol. 7, pp. 1915-1924, 2015.

[86] X.-H. Zhang, S. P. Tiwari, and B. Kippelen, "Pentacene Organic Field-Effect Transistors with Polymeric Dielectric Interfaces: Performance and Stability," *Organic Electronics,* vol. 10, pp. 1133-1140, 2009.

[87] T. Miyadera, S. Wang, T. Minari, K. Tsukagoshi, and Y. Aoyagi, "Charge Trapping Induced Current Instability in Pentacene Thin Film Transistors: Trapping Barrier and Effect of Surface Treatment," *Applied Physics Letters,* vol. 93, p. 259, 2008.

[88] M. Barra, F. V. Di Girolamo, N. A. Minder, I. Gutiérrez Lezama, Z. Chen, A. Facchetti, A. F. Morpurgo, and A. Cassinese, "Very Low Bias Stress in N-Type Organic Single-Crystal Transistors," *Applied Physics Letters,* vol. 100, p. 79, 2012.

[89] A. D. Mottram, Y.-H. Lin, P. Pattanasattayavong, K. Zhao, A. Amassian, and T. D. Anthopoulos, "Quasi Two-Dimensional Dye-Sensitized In_2O_3 Phototransistors for Ultrahigh Responsivity and Photosensitivity Photodetector Applications," *ACS Applied Materials & Interfaces,* vol. 8, pp. 4894-4902, 2016.

[90] R. Liguori, W. Sheets, A. Facchetti, and A. Rubino, "Light-and Bias-Induced Effects in Pentacene-Based Thin Film Phototransistors with a Photocurable Polymer Dielectric," *Organic Electronics,* vol. 28, pp. 147-154, 2016.

[91] M. C. Hamilton, S. Martin, and J. Kanicki, "Thin-Film Organic Polymer Phototransistors," *IEEE Transactions on Electron Devices,* vol. 51, pp. 877-885, 2004.

[92] Y.-Y. Noh, J. Ghim, S.-J. Kang, K.-J. Baeg, D.-Y. Kim, and K. Yase, "Effect of Light Irradiation on the Characteristics of Organic Field-Effect Transistors," *Journal of Applied Physics,* vol. 100, p. 094501, 2006.

[93] Y.-Y. Noh, D.-Y. Kim, and K. Yase, "Highly Sensitive Thin-Film Organic Phototransistors: Effect of Wavelength of Light Source on Device Performance," *Journal of Applied Physics,* vol. 98, p. 074505, 2005.

[94] K. J. Baeg, M. Binda, D. Natali, M. Caironi, and Y. Y. Noh, "Organic Light Detectors: Photodiodes and Phototransistors," *Advanced Materials,* vol. 25, pp. 4267-4295, 2013.

[95] A. Pierre and A. C. Arias, "Solution-Processed Image Sensors on Flexible Substrates," *Flexible and Printed Electronics,* vol. 1, p. 043001, 2016.

[96] M. Debucquoy, S. Verlaak, S. Steudel, K. Myny, J. Genoe, and P. Heremans, "Correlation between Bias Stress Instability and Phototransistor Operation of Pentacene Thin-Film Transistors," *Applied Physics Letters,* vol. 91, p. 103508, 2007.

[97] J. Milvich, T. Zaki, M. Aghamohammadi, R. Rödel, U. Kraft, H. Klauk, and J. N. Burghartz, "Flexible Low-Voltage Organic Phototransistors Based on Air-Stable Dinaphtho [2,3-b:2′, 3′-f] thieno [3, 2-b] thiophene (DNTT)," *Organic Electronics,* vol. 20, pp. 63-68, 2015.

[98] F. Yu, S. Wu, X. Wang, G. Zhang, H. Lu, and L. Qiu, "Flexible and Low-Voltage Organic Phototransistors," *RSC Advances,* vol. 7, pp. 11572-11577, 2017.

[99] Y. Chu, X. Wu, J. Lu, D. Liu, J. Du, G. Zhang, and J. Huang, "Photosensitive and Flexible Organic Field-Effect Transistors Based on Interface Trapping Effect and Their Application in 2d Imaging Array," *Advanced Science,* vol. 3, 2016.

[100] E. R. Patchett, "A Roll-to-Roll Compatible Vacuum-Evaporation Route to Organic Circuit Production," Ph. D. Ph. D. Thesis, Prifysgol Bangor University, 2014.

[101] U. Zschieschang and H. Klauk, "Low-Voltage Organic Transistors with Steep Subthreshold Slope Fabricated on Commercially Available Paper," *Organic Electronics,* vol. 25, pp. 340-344, 2015.

[102] N. Mott and E. Davis, *Electronic Process in Non-Crystalline Materials*: Oxford University Press, 1971.

[103] W. L. Kalb, K. Mattenberger, and B. Batlogg, "Oxygen-Related Traps in Pentacene Thin Films: Energetic Position and Implications for Transistor Performance," *Physical Review B,* vol. 78, p. 035334, 2008.

[104] W. Xie, K. Willa, Y. Wu, R. Häusermann, K. Takimiya, B. Batlogg, and C. D. Frisbie, "Temperature-Independent Transport in High-Mobility Dinaphtho-thieno-thiophene (DNTT) Single Crystal Transistors," *Advanced Materials,* vol. 25, pp. 3478-3484, 2013.

[105] S. Yogev, E. Halpern, R. Matsubara, M. Nakamura, and Y. Rosenwaks, "Direct Measurement of Density of States in Pentacene Thin Film Transistors," *Physical Review B,* vol. 84, p. 165124, 2011.

[106] E. G. Bittle, J. I. Basham, T. N. Jackson, O. D. Jurchescu, and D. J. Gundlach, "Mobility Overestimation Due to Gated Contacts in Organic Field-Effect Transistors," *Nature Communications,* vol. 7, p. 10908, 2016.

[107] W. L. Kalb, F. Meier, K. Mattenberger, and B. Batlogg, "Defect Healing at Room Temperature in Pentacene Thin Films and Improved Transistor Performance," *Physical Review B,* vol. 76, p. 184112, 2007.

[108] S. M. Sze, *Semiconductor Devices: Physics and Technology*: John Wiley & Sons, 2008.

[109] N. Padma, S. Sen, S. N. Sawant, and R. Tokas, "A Study on Threshold Voltage Stability of Low Operating Voltage Organic Thin-Film Transistors," *Journal of Physics D: Applied Physics*, vol. 46, p. 325104, 2013.

[110] T. Jung, A. Dodabalapur, R. Wenz, and S. Mohapatra, "Moisture Induced Surface Polarization in a Poly(4-vinyl phenol) Dielectric in an Organic Thin-Film Transistor," *Applied Physics Letters*, vol. 87, p. 182109, 2005.

[111] D. Guo, S. Ikeda, K. Saiki, H. Miyazoe, and K. Terashima, "Effect of Annealing on the Mobility and Morphology of Thermally Activated Pentacene Thin Film Transistors," *Journal of Applied Physics*, vol. 99, p. 094502, 2006.

[112] R. Häusermann and B. Batlogg, "Gate Bias Stress in Pentacene Field-Effect-Transistors: Charge Trapping in the Dielectric or Semiconductor," *Applied Physics Letters*, vol. 99, p. 175, 2011.

[113] C. Watson, E. Lopes, R. de Oliveira, N. Alves, J. Giacometti, and D. Taylor, "Interface State Contribution to the Photovoltaic Effect in Organic Phototransistors: Photocapacitance Measurements and Optical Sensing," *Organic Electronics*, vol. 52, pp. 79-88, 2018.

[114] R. Di Pietro, D. Fazzi, T. B. Kehoe, and H. Sirringhaus, "Spectroscopic Investigation of Oxygen-and Water-Induced Electron Trapping and Charge Transport Instabilities in N-Type Polymer Semiconductors," *Journal of the American Chemical Society*, vol. 134, pp. 14877-14889, 2012.