# DOCTOR OF PHILOSOPHY

## Development of thin film flexible and transparent electronics

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# *DEVELOPMENT OF THIN FILM FLEXIBLE AND TRANSPARENT ELECTRONICS*


PRIFYSGOL
BANGOR
UNIVERSITY

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A thesis submitted in partial fulfilment for the degree of

*Doctor of Philosophy*

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*"Life is and will ever remain an equation incapable of solution, but it contains certain known factors."*

- *Nikola Tesla*

# ABSTRACT

This thesis focuses on the development of transparent and flexible components such as silver nanowire (AgNW) based transparent conducting electrodes (TCEs) and metal oxide thin film transistors (TFTs) with the aim of improving the stability and performance under real-world conditions. The electrical and environmental stability of these components is, therefore, investigated. For AgNWs a 3-step post processing method was used to enhance the electrical, surface properties of AgNWs TCEs. Thermal embossing process parameters were optimised using a Taguchi orthogonal array, where pressure, time and temperature of the embossing step were all varied. An in-depth study of the effect of thermal embossing, effect of $N_2$ plasma treatment and photonic sintering on the AgNW TCE properties was undertaken. X-ray photoelectron spectroscopy, atomic force microscopy and scanning electron microscopy analysis of AgNW TCEs revealed several mechanisms responsible for the reduction of sheet resistance and surface roughness. However, transmittance and haze remained unchanged after post processing of TCEs. Electrical and environmental stability of AgNW TCEs is investigated through accelerated lifetime testing (ALT) and method to enhance stability of AgNW TCEs are developed.

A Plackett-Burman design was applied to optimise the production of anodised ($Al_2O_3$) dielectric films for ZnO thin film transistor (TFTs). A comprehensive study of the effect of the processing parameters on the performance of anodized $Al_2O_3$ gate dielectric films for ZnO TFTs is conducted. The impact of the process factors on the overall performance of the ZnO TFTs is also investigated. The development of low voltage metal oxide TFTs based upon ZnO and flexible IGZO is reported using $Al_2O_3$ as the gate dielectric. The performance of transparent IGZO TFTs base on AgNW and ITO gate electrode is also studied.

Understanding the origin of electrical instability in inorganic metal oxide TFTs over long periods is also essential to realize high performance circuits. In this thesis, the effects of positive gate bias stress (PGBS) on IGZO TFTs are also investigated. It was found that the threshold voltage, $V_T$, always shifted in the direction of the applied gate voltage. It was also observed that the threshold voltage shift, $\Delta V_T$, is reduced with CYTOP passivation and white light illumination. A density of states (DoS) analysis is carried out during PGBS to confirm the origin of trap states due to bias stressing.

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1. **Dinesh Kumar** and J. Kettle. "IGZO TFT performance investigation using Taguchi Orthogonal arrays." (Under review in Micro & Nano Letters)
2. **Dinesh Kumar**, T. C. Gomes, N. Alves, L. F. Santos, G. C. Smith and Jeff Kettle "UV phototransistors based upon spray coated and sputter deposited ZnO TFTs" (Under review in IEEE Sensors Journal)
3. **Dinesh Kumar**, V. Stoichkov, E. Brousseau, G. C. Smith and J. Kettle. "High performing silver nanowires transparent conducting electrodes with a sheet resistance of 2.5 Ω $Sq^{-1}$ based upon a roll-to-roll compatible post-processing technique." *RSC Nanoscale* 11(2019) 5760.
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7. **Dinesh Kumar**, V. Stoichkov, S. Ghosh, G. Smith, J. K. "Mixed-dimension silver nanowires for solution-processed, flexible, transparent and conducting electrodes with improved optical and physical properties. *Flex. Print. Electron*. 2 (2017) 15005.

## PATENT APPLICATION

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2. Jeff Kettle and **Dinesh Kumar**. Enhancing the stability of AgNW transparent conducting electrodes with 2.5Ω-Sq sheet resistance by the use of post-processing. First edition of the **IEEE International Conference on Flexible and Printable Sensors and Systems - FLEPS 2019** (Oral presentation- paper published in IEEE explore digital library)
3. **Dinesh Kumar** and Jeff Kettle. High performing AgNW transparent conducting electrodes with a sheet resistance of 2.5 Ω Sq−1 based upon a roll-to-roll compatible post-processing technique. **Fifth Innovation in Large-Area Electronics Conference (innoLAE 2019)** at Genome Campus Conference Centre in Cambridge, United Kingdom. (Oral presentation)
4. **Dinesh Kumar** and Jeff Kettle. Control over voltage threshold shift in IGZO TFTs with enhanced electrical characteristics using novel passivation. **Fifth Innovation in Large-Area Electronics Conference (innoLAE 2019)** at Genome Campus Conference Centre in Cambridge, United Kingdom. (Poster presentation)
5. **Dinesh Kumar**, Tiago Gomes, Neri Alves, Jeff Kettle. Understanding UV Sensor Performance in ZnO TFTs through the Application of Multivariate Analysis. **International Conference: IEEE SENSORS 2018** held at Delhi, India during 28-31 October 2018. (paper published in IEEE explore digital library)
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# CONTENTS

# Chapter 1. Introduction

There has been significant research to realise the high performance of transparent and flexible electronics. Market demand for high-performance electronics has also increased because of new emerging applications. It is now estimated that the market for flexible electronics will reach $300 billion by 2028, with growth from $29.28 billion in 2017 to over $63 billion in 2023 [1]. Flexible electronics could transform the way we make and use electronic devices. Many applications that require bendability to conform to the curved surface are driving the progress in the field, which in turn opens the door to futuristic applications such as foldaway smartphone displays, solar cells on plastic substrates, advanced medical devices, mobile health, and wearable sensors [2]. The anticipation is that these new form-factors will expand the scope of microelectronics and lead to further innovation. However, materials, packaging and manufacturing must evolve together with these devices to make these concepts economical and environmentally sustainable. Added value features such as flexibility and transparency have the potential to radically transform the electronics industry and spur a new era of growth. Figure 1.1 shows the current market size of the printed, organic and flexible electronics industry for year 2019 [3].

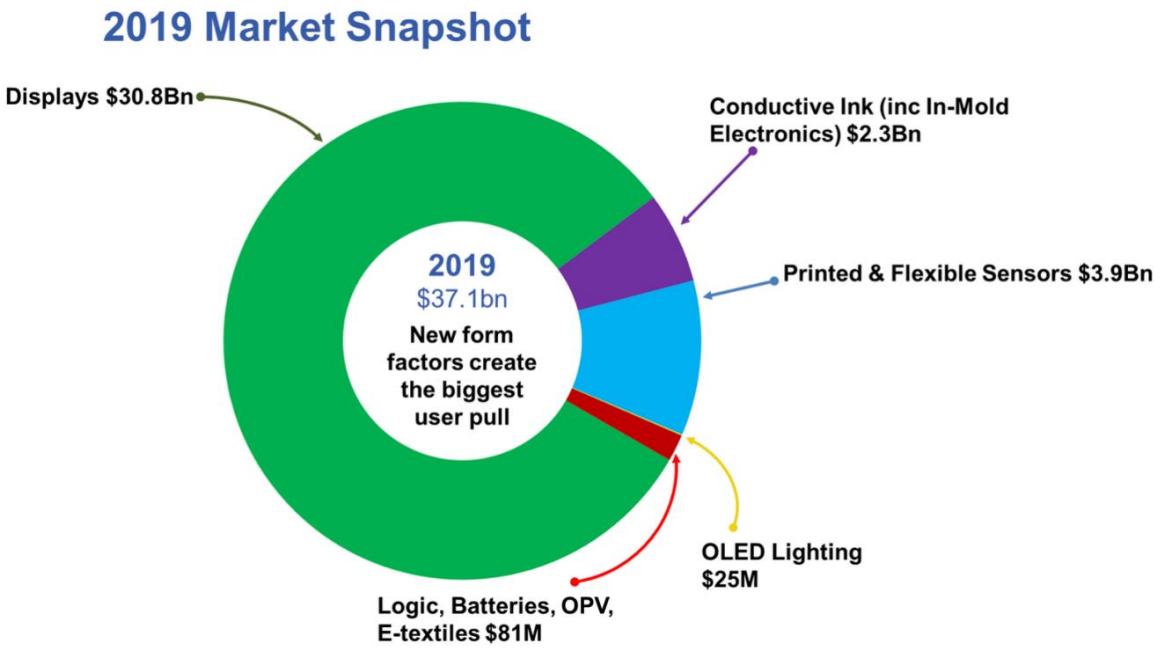


Figure 1.1: Current market size of the printed, organic and flexible electronics industry [3].

Transparent electronics use transparent conductive oxides (TCOs) [4], wide band-gap semiconductors [5], 1-D inorganic nanostructures [6] and nanomaterials like metallic silver nanowires (AgNWs). Over the past two decades the use of transparent conductive materials has rapidly increased as a result of the increasing demand for display technology [7] and the development of thin film based solar cells. TCEs are also a crucial component of next generation electronic devices such as portable organic solar cells, organic light emitting diodes (OLEDs), bendable displays, touch screens, modern personal electronic devices, and transparent stretchable heater [8][9]. AgNWs with well-defined dimensions is a promising material for electrical and optical devices, particularly for flexible transparent conductive electrodes (TCEs). They are considered a strong competitor as a substitute to Indium Tin Oxide (ITO) in many of the applications. One of the primary reasons for this is that the incumbent technology (ITO) is not flexible; upon repeated bending, the films are known to crack and lose conductivity [10], which is particularly prohibitive for future product emergence of flexible electronic devices. When deposited from solution, AgNWs combine several advantages such as high optical transparency, low sheet resistance ($R_{sh}$) and mechanical flexibility. Despite the significant progress in TCEs represented by the above reports, understanding the stability issues and challenges such as long-term environmental stability, high surface roughness, electrical shorting problems must be overcome to fully integrate these new electrodes into high performance commercial devices and circuits.

High mobility thin-film transistors are also crucial for future high resolution and fast response flexible displays [11]. The issue of low mobility ($\sim$1 $cm^2\ V^{-1}s^{-1}$) of electrons in amorphous silicon (a-Si) based TFT backplanes has led to the rise of new technologies that will overcome this problem. Metal oxides are one of such replacement technologies that have been researched and gained huge industry acceptance over the last few years. Today the display industry is extensively using metal-oxide TFT backplane technology in displays based on liquid crystal and light emitting diode (LEDs). Zinc oxide (ZnO) and especially indium gallium zinc oxide (IGZO) has been extensively studied over the last few decades, with much current academic and industrial research and development. Other favourable aspects of ZnO include its broad chemistry leading to many opportunities for wet chemical etching, low power threshold for optical pumping, radiation hardness, and biocompatibility. Optical pumping is a process in which light is used to raise (or "pump") electrons from a lower energy level in an atom to a higher energy level. ZnO and related compounds (IGZO) offer carrier mobility of more than $10cm^2V^{-1}s^{-1}$ approaching $100cm^2V^{-}$

$^{1}s^{-1}$ [12][13]. High mobility oxide semiconductors, along with high-k gate dielectrics, are projected to be key ingredients for future transparent and emerging flexible and stretchable electronics [14]. Shown in Figure 1.2 are the applications of flexible electronics such as sensing, computing, data storage, and energy.

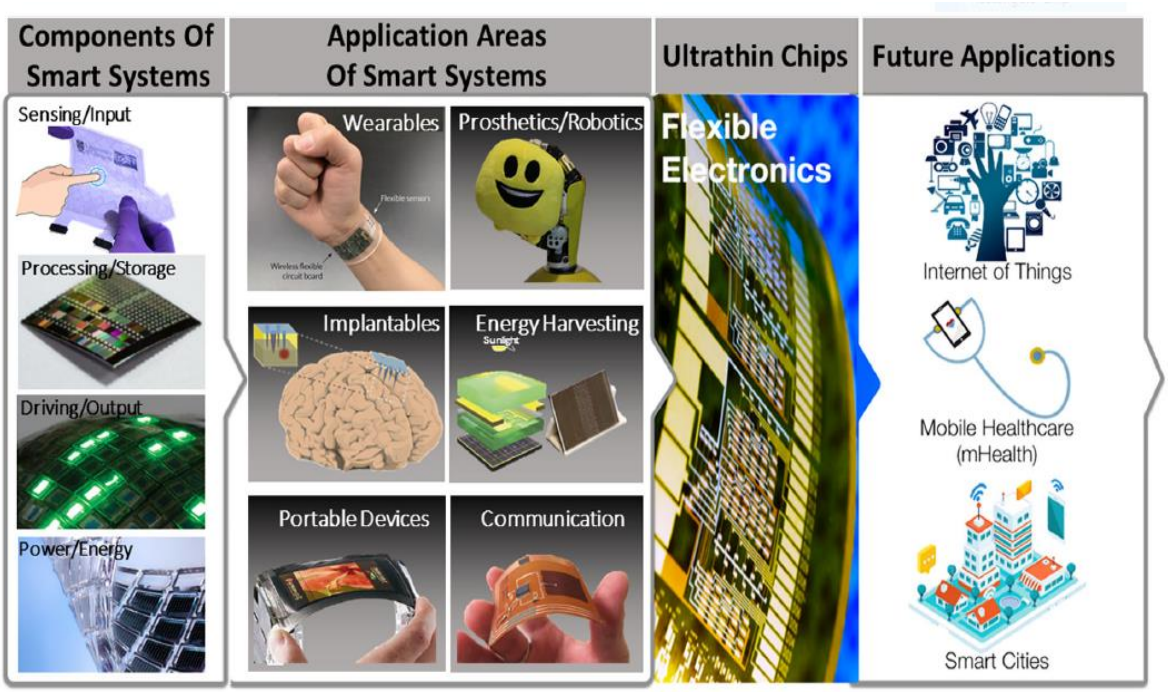


Figure 1.2: Applications of flexible electronics enabled through underpinning research in areas such as sensing, computing, data storage, and energy [1].

This thesis investigates high performance transparent components including AgNW TCEs for OPV, metal oxide TFTs and their electrical and environmental stability as outlined in the next section.

## 1.1 Highlights and Structure of this Thesis

This thesis focuses on the development of transparent and flexible components such as silver nanowire transparent conducting electrodes (AgNW TCEs), metal oxide TFTs with the aim of improving their stability and performance under real world conditions.

The highlights of this research are:

- The world leading Figure of Merit (FOM = 933) of AgNW TCE which is 2 × better as compared with current literature.
- Detailed stability analysis of AgNW TCE performance as a function of temperature and high current conditions.

- Demonstration of improved electrical and surface roughness performance of flexible AgNW TCEs using post R2R processing techniques (thermal embossing, $N_2$ plasma treatment and photonic sintering).
- Demonstration of mixed dimension AgNWs for solution-processed, flexible, transparent and conducting electrodes with improved optical and physical properties.
- Demonstration of improved performance of metal oxide TFTs and demonstration of process optimisation techniques such as Taguchi orthogonal array and Plackett-Burman Design for screening active factors.
- Demonstration of flexible, low voltage and transparent IGZO TFTs with high performance.

The structure of this thesis is as follows:

**Chapter 2** provides a background of the science behind this research. In this chapter, a state-of-the-art review of transparent electronics, AgNW TCEs, and their post processing, metal oxide TFT development is discussed. Then, the TFT operation and the electrical characteristics, as well as the density of states, are explained. Finally, the electrical and environmental stability of AgNW TCEs is discussed.

**Chapter 3** reports the experimental methods, setups used for manufacturing and characterisation of flexible TCEs and Metal oxide TFTs.

**Chapter 4** is the first results chapter demonstrating the outcomes of flexible TCEs, TCEs post processing and performance optimisation using Taguchi Orthogonal Arrays. Also presented are the results from solution processed mixed dimension AgNW flexible TCEs with improved the optical and physical properties. Finally, the effect of post processing on high current and temperature stability of AgNW TCEs has been investigated.

**Chapter 5** reports the ZnO based TFTs development, as well as optimisation of high-k anodic dielectric ($Al_2O_3$) for TFTs using Plackett-Burman design.

**Chapter 6** presents the effect of positive gate bias stressing on IGZO TFTs, flexible IGZO TFTs performance. Moreover, transparent AgNW film gated IGZO TFTs electrical, optical performance are reported and compared with TFTs on incumbent ITO transparent electrodes.

**Chapter 7** summarises the main results from the thesis and discusses possible directions for further work.

# Chapter 2. Literature Review of Transparent Electronics

This chapter details the current state and progress in the following areas investigated during this Ph.D.: silver nanowire based (AgNW) transparent conductive electrodes (TCEs) and metal oxide thin film transistors (TFTs). Basic fundamental background theory of TCEs and metal oxide TFTs are presented. Electrical, optical and physical properties, as well as deposition methods and post processing of AgNW TCEs, are reviewed. Then, the materials for TCEs, TFTs and n-channel TFT operation principles are explained. Furthermore, process optimization techniques such as Taguchi Orthogonal Arrays (OA) and Plackett-Burman Design (PBD) are detailed. Finally, the environmental and electrical stability of TCEs and TFTs are discussed.

## 2.1 Review of Transparent and Flexible Electronics

This section reviews the state of the art concerning transparent and flexible electronics, with the focus on AgNW based TCEs as well as ZnO and IGZO based TFTs. Flexible and transparent electronics presents a new age of electronic technologies. Recently, various applications in wearable electronics, flexible transparent OLED displays [15]–[20], radio-frequency identifications (RFIDs) [21] and sensing systems [22]–[25] have been demonstrated. Also, the technical progress in metal oxide TFTs is a significant factor for promoting the development of transparent and flexible displays [26]–[31].

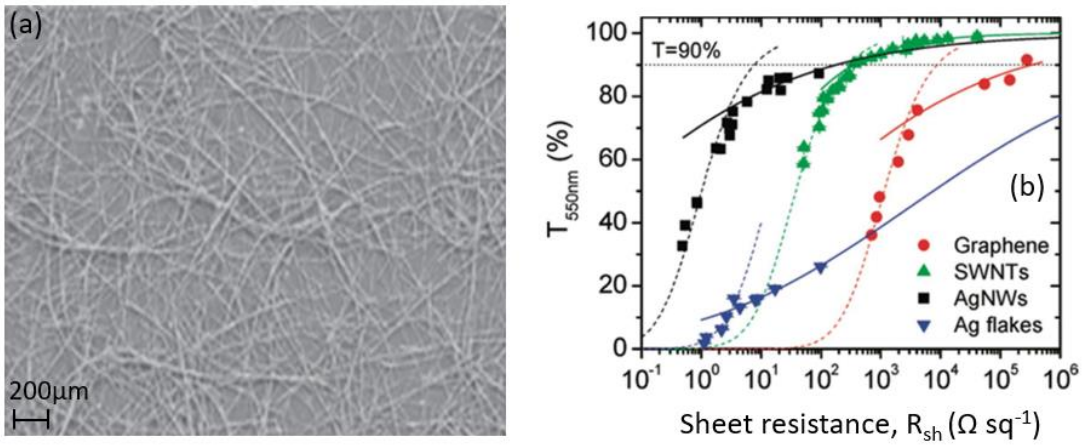


Figure 2.1: (a) SEM image of a AgNW transparent electrode, (b) Optical transmittance as a function of sheet resistance for silver, graphene and single walled carbon nanotubes (SWNTs) [32].

Shown in Figure 2.1(a) are SEM images of a AgNW transparent electrode, (b) Transmittance as a function of sheet resistance for silver, graphene, single walled carbon nanotubes (SWNTs). It is evident that AgNWs are one of the most promising in terms of electrical and optical performance, outperforming graphene and SWNTs. This is because even low density of AgNWs on substrate produces high transmittance and low sheet resistance.

Shown in Table 2.1 is a general guide to the different transparent conductive material electrode fabrication.

Table 2.1: General guide to transparent conductive material electrode fabrication [33]. + symbols indicate positive results – symbols represent poor results.

| Fabrication method[a] | TCOs | Graphene | CNTs | AgNWs |
|---|---|---|---|---|
| Chemical vapour deposition | +++ | +++ | + | - |
| Sputtering | +++ | - | - | - |
| Spin coating | - | + | ++ | ++ |
| Spray deposition | ++ | + | +++ | +++ |
| Screen printing | -- | + | ++ | ++ |
| Cost | Low-high | High | High | Medium |
| Processing temperature ($^0$C) | > 200[b]-1000 | RT-1000[c] | RT-700[c] | RT-700 |
| Uniformity | +++ | + | ++ | ++ |
| Typical thickness (nm) | 100-300 | <5 | <10 | 25>600[d] |
| Typical Rsh Ω sq$^{-1}$ | 5-100 | 30-5000 | 60-300 | 1-50 |
| Transmission (at 550 nm) | 80-97 % | 80-96 % | 80-91 % | 80-96 % |

[a] Fabrication method refers to the production of electrodes directly, not to the production of the integral components which are used to fabricate the network.

[b] Deposition temperatures of transparent conductive oxides (TCOs) frequently need several hundred degrees Celsius or the use of vacuum processes such as sputtering.

[c] Networks can be fabricated at room temperature (RT) but if device fabrication requires high temperature processes vacuum or encapsulation is required to stabilize the films.

[d] Thickness is diameter and density dependent though with high mechanical pressure it can be reduced to the diameter of a single nanowire.

The search for materials which can be used to make thin films that simultaneously show high transparency, low sheet resistance [34] and flexibility [35] has mainly focused on nanostructures such as conducting polymer [36], graphene [37], carbon nanotubes (CNT) [38], copper nanowires [39] and AgNWs [40]–[43]. Nanowires are one dimensional nanostructures possessing diameter of the order of a nanometer ($10^{-9}$ meters). CNT, graphene, and transparent conducting polymer films show low conductivity as compared to metal nanostructures and hence metallic nanostructures are

an appealing alternative. Metallic nanostructured materials are normally solution processed and deposited as disordered percolation networks. A solution process technique, such as spray coating can be used to readily prepare AgNW TCEs [44], [45]. Spray pyrolysis is a process in which a thin film is deposited by spraying a solution on a heated surface. This process can be carried out at low temperature (<80 $^0$C) and does not require any vacuum equipment.

The focus of this thesis is on AgNWs films so CNT, graphene, and TCO are not discussed. There are three specific advantages of AgNW networks as transparent conductive materials. First is the low sheet resistances attainable with AgNW percolative networks, which can be approximately 10 $\Omega sq^{-1}$. Secondly, they can demonstrate flexibility on plastic substrates and thirdly they possess high transparency in the infra-red region of the electromagnetic spectrum [46]. However, creating TCEs with high conductivity and transparency is not a trivial matter, since these properties are often mutually exclusive. Nevertheless, AgNW based TCEs are relatively less expensive and are compatible with a roll-to-roll manufacturing process [47]–[52].

### 2.1.1 Review of State-of-the-Art in Transparent Electrodes

Over the last couple of decades, extensive work has been performed for the development of new TCEs. Shown in Table 2.2, is a summary of the best performing AgNW TCEs compared with other TCEs and their fabrication processes.

Table 2.2: A summary of the best performing non TCO electrodes compared with other TCEs.

| Reference | Material | FoM | Rsh ($\Omega$ sq$^{-1}$) | T(%) | Remark/Process |
|---|---|---|---|---|---|
| L. Li *et al.* [53] | metal grid | 198.3 | 9.8 | 83.1 | Photolithography |
| J. Y. Lee *et al.* [54] | AgNWs | 150 | 16 | 86 | Solution process |
| Y. Jia *et al.* [55] | AgNWs | 207.3 | 35 | 95 | Dynamic Heating Method |
| H. Du *et al.* [56] | AgNWs | 212.8 | 7.1 | 79.2 | Spin coating |
| C. Preston *et al.* [57] | AgNWs | 300 | 13 | 91 | Lamination process |
| L. J. Andres *et al.* [58] | AgNWs | 338 | 20.2 | 94.7 | Spray coating |
| A. Kim *et al.* [59] | ZnO/AgNWs/ZnO | 487.9 | 8 | 91 | DC magnetron sputtering |
| S. H. Jo *et al.* [60] | CNT/PEDOT:PSS | 6 | 280 | 80 | spray coating |
| N. Kim *et al.*[61] | PEDOT:PSS | 76 | 46.1 | 90 | Solution process |
| S. Bae Jo *et al.* [62] | Graphene | 116.1 | 30 | 90 | CVD |

In early 2008 J. Y. Lee *et al.* demonstrated one of the first solution processed AgNW network TCEs [54]. Since then, a major focus has been on the inorganic synthesis methods to synthesize significant quantities of metallic nanowires, such as copper or

AgNWs, with well controlled physical dimensions, formulated into stable dispersions [46], [63]–[68]. A. Kim *et al.* reported the best performing composite electrode based on AgNWs and ZnO films showing sheet resistance 8 Ω $sq^{-1}$ and transmittance 91% at 550 nm [59], although this process relied on a vacuum deposition step.

## 2.2 Review of Properties of Transparent Conductive Electrodes

TCEs are characterised by various electrical and optical properties such as sheet resistance, transmittance and haze [69], [70]. As TCEs play a critical role in electronic devices including liquid crystal displays, OLEDs and photovoltaics, the preferred TCE properties generally depend on their application. For instance, large optical haze (percentage of the transmitted light which is scattered) is disadvantageous to applications of TCEs in most electronic displays, however, large haze can enhance efficiency in photovoltaics because of the extended optical path length which increases the probability of photon absorption by the photosensitive material [71][72]. Irrespective of device type, the two most significant performance parameters are the TCE sheet resistance and optical transmittance. Thermal stability, processability and chemical compatibility with other materials, and work function are other key parameters.

Shown in Table 2.3 are the desired properties of transparent conductive TCEs for main applications in photovoltaics, OLEDs, film heaters and touch screens.

Table 2.3: Desired properties of transparent conductive electrodes for main applications [33]. The number of plus symbols indicates the importance of the property to the application.

| Application | Transparency | Conductivity | Flexibility | Haze |
|---|---|---|---|---|
| Photovoltaics | +++ | +++ | + | +++ |
| OLED | ++ | ++ | + | + |
| Film Heaters | + | +++ | ++ | + |
| Touch Screens | +++ | ++ | ++ | + |

### 2.2.1 Sheet Resistance ($R_{sh}$)

In terms of electrical properties, the low sheet resistance is usually desired. The sheet resistance of a TCE is a critical factor that requires precise control during the electrode fabrication process depending on the desired application. For example, in modern displays and touchscreen applications, in order to allow for fast screen response, the sheet resistance of the TCE has to be as low as possible. In the case of AgNWs, several physical characteristics of the nanowires themselves and network morphology affect the electrical

properties of nanowire networks and the sheet resistance [73]. In general, there is an increase in resistance of the network with a decrease in the length of the nanowires used and this trend is continued if the nanowire diameter is decreased [40], [46], [74]. For very low values of nanowire diameter, surface scattering effects lead to an increase in sheet resistance. Shown in Figure 2.2 (a) are the sheet resistance of AgNW films as a function of increased silver content and (b) AgNW weight percent (wt. %). As more AgNW material is deposited percolation network becomes bigger and more AgNWs junctions are created, leading to a decrease in the sheet resistance.

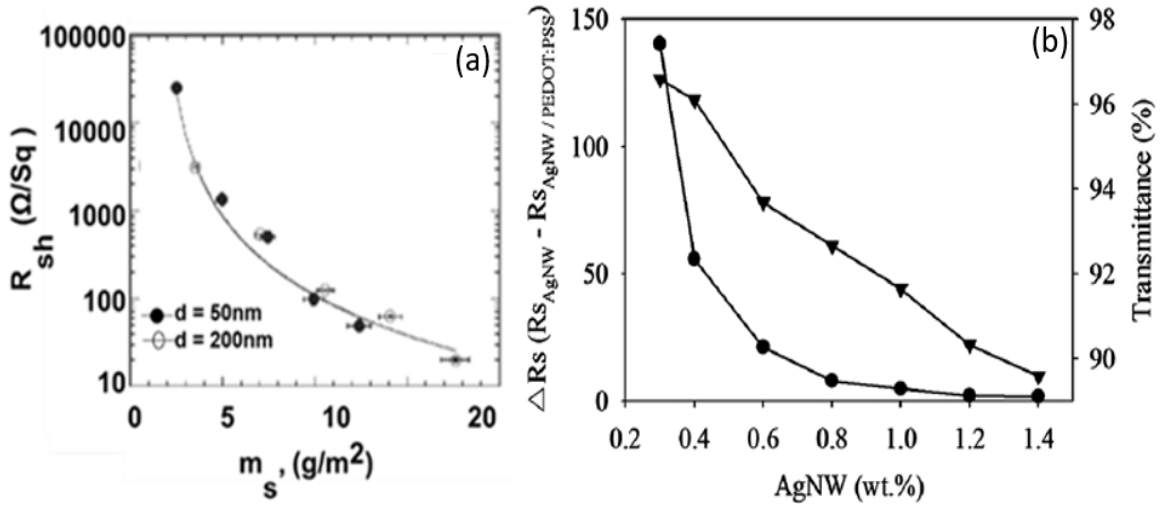


Figure 2.2: (a) The sheet resistance of AgNW films as a function of silver content and (b) the sheet resistance differences between single-layer AgNW films and AgNW/PEDOT:PSS films and the transmittance at 550 nm as a function of the concentration of AgNWs [75].

The nanowire density, which is deposited onto a substrate, plays a major role in the conduction properties of the network. In many studies, it has been shown that increasing the number of nanowires decreases the resistance; however, this also results in a decrease in the optical transmission of the network. Literature shows that the sheet resistance decreased with an increase in AgNW contents on the substrate [76],[77], as shown in figure 2.2 (a). Maintaining an equilibrium between the electrical and optical properties has long been a challenge for transparent conductive materials and fabrication processes. Electrical conductivity requirements differ according to the application of TCEs, for example, solar cells require a TCE sheet resistance on the scale of 10Ω $sq^{-1}$ [78][79]. Sheet resistance ($R_{sh}$) is normally measured using a four point probe, from which sheet resistance can be calculated from equation 2.1 [80], where, ρ(t) is the film

sheet resistivity, t is film thickness, V is the applied voltage and I is the current passing through TCE. This equation is used in this thesis for sheet resistance calculations.

$$R_{Sh} = \frac{\rho(t)}{t} \qquad \text{Eq. 2.1}$$

$$\rho(t) = \frac{t * V(4.532)}{I} \qquad \text{Eq. 2.2}$$

### 2.2.2 Transmittance (T)

Another important property of transparent electrodes is transmittance. Percentage transmittance is defined as the percentage of light passing through the AgNW network exclusive of the absorption in the reference substrate and is given by the following equation 2.3:

$$\%T = \frac{S(\lambda) - D(\lambda)}{R(\lambda) - D(\lambda)} \times 100\% \qquad \text{Eq. 2.3}$$

Where, S is the intensity of light at wavelength λ, D is the dark intensity at wavelength λ, and R is the reference intensity at wavelength λ.

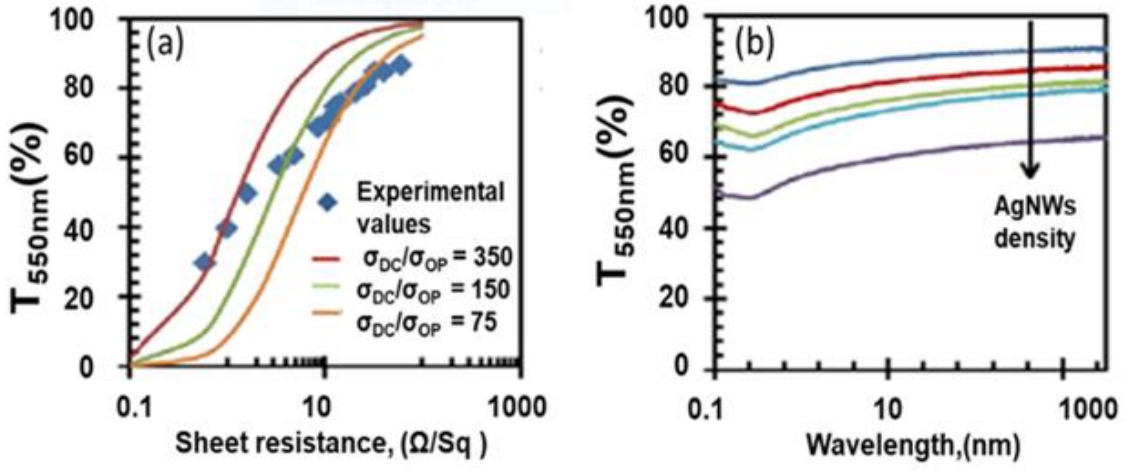


Figure 2.3: (a) Plot of AgNW film transmittance (λ = 550 nm) versus sheet resistance data for films deposited on PET (b) Transmittance spectra for various AgNW films [81].

Shown in Figure 2.3 (a) is the plot of AgNW film transmittance (λ = 550 nm) versus sheet resistance data for films deposited on polyethylene terephthalate (PET) and Figure 2.3 (b) is the transmittance spectra for various AgNW films. It has also been shown

in the literature that longer AgNWs form a better network due to longer conducting paths, lower deposition density and an increased number of junctions between AgNWs, leading to lower junction resistance and high transmittance [82]. These factors indicate that the optimum of AgNWs should be longer, as this can improve the conductivity of TCEs, and thinner AgNWs as this decreases the deposition area and light scattering, improving the optical transparency and haze.

### 2.2.3 Figure of Merit (FoM)

To evaluate the trade-off between Transmittance (T) and sheet resistance ($R_{sh}$) values, a combined 'Figure of Merit' can be used to evaluate the quality of a transparent electrode. The Figure of merit (FoM) is often reported in the literature [58][83] and is given by equation 2.4. This equation is used in this thesis for FOM calculations.

$$FOM = \frac{188.5}{R_{sh}\left(\sqrt{\frac{1}{T}} - 1\right)} \qquad [58] \qquad \text{Eq. 2.4}$$

The best reported FoM [59] of composite AgNW/ZnO TCE to date is 487.9. In this work AgNWs form a random percolating network embedded between the ZnO layers prepared by direct current (DC) magnetron sputtering at room temperature.

### 2.2.4 Mechanical Flexibility

In contrast to ITO, AgNW TCEs on plastic are mechanically flexible. The literature confirms that the mechanical flexibility of the AgNW electrodes is particularly good. For example, J. Kettle *et al.* demonstrated that AgNWs TCE remains robust even after extortionate bending tests (100 cycles with a bending radius of 20 mm) [58]. After testing, no modification of the optical properties was observed and a drop lower than 5% in sheet resistance after 100 bending cycles were recorded. Conversely, ITO electrodes showed a drop of 77% in sheet resistance after the first 10 bending cycles and catastrophic failure after 20 cycles during the same test.

Recently, Y. Wang *et al.* reported that the relative change in sheet resistance of the film over 300 bending cycles of outward and inward bending was less than 1.5% and the films exhibited good conductivity and heating performance [84]. Figure 2.4 shows the relative change in the sheet resistance of the AgNW TCE versus the number of bending

cycles, where R and $R_0$ represent the sheet resistance of films before and after the bending test, respectively.

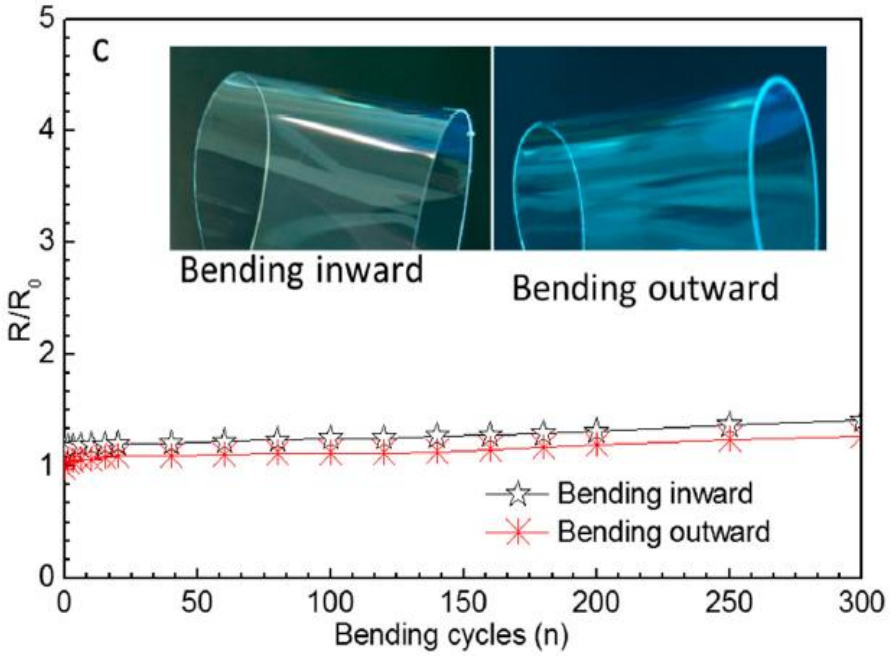


Figure 2.4: Example of a transparent conductive electrode showing the relative change in the sheet resistance of the AgNW TCE versus the number of bending cycles [79].

## 2.3 Post Processing Treatment

After the AgNW deposition process, some nanowires protrude from the TCE surface and some of them lie on top of each other, which results in increased surface roughness to a few hundred nanometers. However, much lower surface roughness is needed for various TCE applications. For instance, the active films in organic solar cells are thin (typically between 100 to 300nm) [85]. Optical, electrical and physical properties of AgNW based transparent electrodes depends on a number of factors including type of AgNWs [58],[86], deposition process [87] and also post treatment of electrodes such as thermal annealing [88][89], mechanical pressing [90]–[92], fast sintering [93], etc.

To enhance the quality and performance of TCEs, post-processing treatments on electrodes are needed. For example, H. H. Khaligh *et al.* reported the hot rolling of AgNW TCEs for surface roughness minimization, achieving the root-mean-square surface roughness ($R_q$) of 7nm and the maximum peak-to-valley ($P_V$) value 30 nm, making the electrodes suitable for typical organic devices [91]. In addition, the adhesion of the AgNWs to the substrate significantly increased with this process.

Shown in Table 2.4 are the surface roughness data of the AgNW electrodes post processed using a hot rolling process.

Table 2.4: Surface roughness data of the annealed AgNW TCEs and post processed using hot rolling [94].

| Post treatment | RMS Roughness, Rq (nm) | Max peak to valley, $P_V$ (nm) |
|---|---|---|
| Annealed | 14 | >90 |
| Rolled | 7 | <30 |

Shown in Figure 2.5 are SEM images of tilted (45°) AgNW film on PET after (a) annealing, and (b) hot rolling. (c) shows a SEM image of a tilted (85°), a hot-rolled electrode which demonstrates that the nanowires are embedded in the substrate surface.

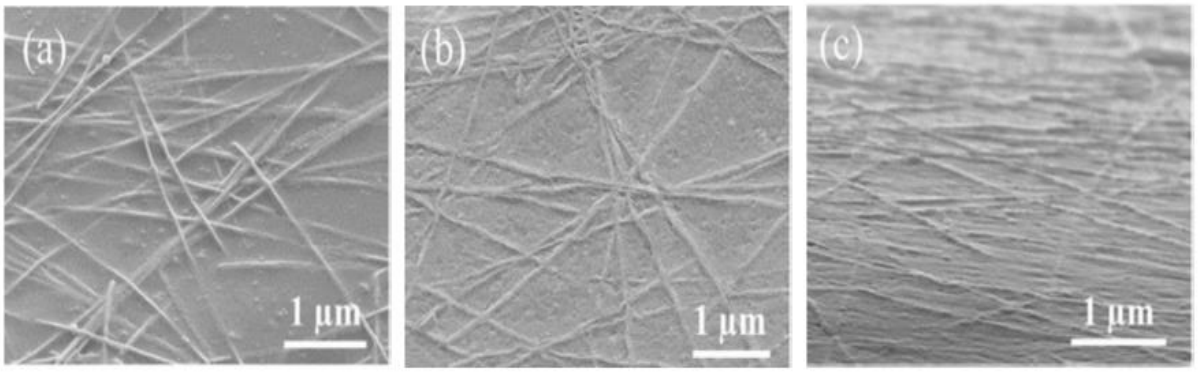


Figure 2.5: SEM images of tilted (45°) AgNW film on PET after (a) annealing, (b) hot rolling. (c) SEM image of a tilted (85°) hot-rolled electrode [91].

The post treatment on TCEs is shown to mostly affect the resistance and surface roughness of the nanowire network. Even though AgNW TCEs have better electrical and optical properties, some drawbacks need to be addressed. For example, one major issue is too high surface roughness of AgNW TCEs which causes shorting of device electrodes [95]. This imposes difficulties to integrate AgNW TCEs in many electronic devices such as solar cells and TFTs.

A simple post processing technique used is plasma treatment of the surface of AgNW TCEs for the reduction of the sheet resistance cited in the literature. For example, Jun Li *et al.* demonstrated that argon (Ar) plasma treatment removes the residual surfactant, polyvinylpyrrolidone (PVP), and enhances the contact between adjacent AgNWs. They reported AgNWs TCEs with a sheet resistance of 7.2 $\Omega\ sq^{-1}$ and a transmittance of 78% at 550 nm [96].

Another new technology for post processing AgNW TCEs is photonic curing that allows the sintering of AgNWs on low temperature, flexible substrates such as paper and plastic in less than 2 ms [97][98]. D. J. Lee *et al.* reported improvements in sheet resistance of AgNW TCE using the intense pulsed light (IPL) method, which welds the interconnections among AgNWs in a short time without heat or pressure treatment [99], [100]. They achieved the sheet resistance of 12.6 Ω $sq^{-1}$ with a transmittance of 85.7% at 550 nm.

## 2.4 Physical and Chemical Deposition Techniques

Physical methods such as sputtering, evaporation, laser deposition and chemical methods like chemical vapour deposition, sol-gel, chemical bath deposition, electroplating have been used for preparing TCEs. The best performances are generally obtained using physical methods such as chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD). However, these are not generally scalable to roll to roll manufacturing processes. Historically some of the earliest TCEs were deposited by solution processing using spray pyrolysis.

Based on the direct fabrication of devices, there are many deposition techniques for semiconductors and electronic materials. To obtain thin films with good quality, two common deposition techniques: physical and chemical depositions are used. Shown in Table 2.5 is a summary of the above mentioned deposition techniques.

**Table 2.5: A summary of deposition techniques [101].**

| **Physical deposition** | **Chemical deposition** |
|---|---|
| Vacuum thermal evaporation | Sol-gel technique |
| Electron beam evaporation | Chemical bath deposition |
| Laser beam evaporation | Spray pyrolysis technique |
| Molecular beam epitaxy | Electroplating technique |
| Ion plating evaporation | Low pressure (LPCVD) |
| DC sputtering | Plasma enhanced (PECVD) |
| RF sputtering | Atomic layer deposition (ALD) |

In this thesis, the spray pyrolysis technique, electron beam evaporation and radio frequency (RF) sputtering for deposition of thin films were used.

## 2.5 Review of Thin Film Transistors and Circuits

TFTs are widely used as a backplane to drive display components, such as LCD, OLED, and even μ-LCD. Response time and resolution of display highly dependent upon the mobility

of charge carriers and hence high mobility TFTs are crucial for future high resolution and fast response flexible displays [102].

A TFT is a type of field-effect transistor (FET) made by depositing thin films of a semiconductor layer as well as the dielectric layer and metallic contacts over a supporting substrate. The main differentiator from other FET technologies is that common substrate is glass or polyimide, unlike conventional FETs, where the semiconductor is used as substrate. Glass and certain plastic films are good insulators and this limits the leakage current to a minimum. In 1962, P. K. Weimer [103] fabricated the first *n*-channel TFT employing a top gate, staggered structure with micro-crystalline cadmium sulfide (CdS) deposited by evaporation in vacuum as the channel layer and silicon monoxide as the dielectric layer. These TFTs possessed field-effect mobility values of 1.1 $cm^2V^{-1}s^{-1}$and an on-off current ratio of 10.

Since these early studies, a number of materials have been utilised in TFTs. Metal oxides, such as ZnO and IGZO, show better air stability and higher electron mobility. However, oxide-based TFTs so far provide only high-performance *n*-channel TFTs, which prevents the realization of CMOS technology. Therefore, organic-inorganic hybrid complementary structures comprised of *n*-type oxide semiconductor and *p*-type organic semiconductor can be potential candidates for complementary circuit design.

Metal oxide semiconductors have been demonstrated the TFTs with a number of materials specifically ZnO [104]–[106], zinc tin oxide (ZTO) [107]–[111], indium zinc oxide (IZO)[112]–[114], indium gallium oxide (IGO)[115] , and indium gallium zinc oxide (IGZO) [103], [116]–[122].

Amongst metal oxide semiconductors, IGZO, ZnO, and IZO are more attractive because they can be processed at room temperature whilst maintaining good performance, making them compatible with flexible substrates and consequently reducing manufacture costs. IGZO and IZO films, which are normally deposited by physical vapor deposition or RF-magnetron sputtering at room temperatures, show amorphous nature and still achieve high electron mobility. The amorphous material structure of the IGZO films is stable up to 500 $^0$C in air. Due to this, IGZO and IZO are predominantly attractive for microelectronic circuits on flexible substrates and mobility as high as 100 $cm^2V^{-1}s^{-1}$, and on/off current ratio of $10^7$ have been demonstrated. For example, C. M. Hsuet *et al.* [123] fabricated IGZO films on glass substrates using co-sputtering, demonstrating high carrier mobility around about 163.4 $cm^2V^{-1}s^{-1}$.

The rapid progress in the field of *n*-channel metal oxide TFTs has motivated research on *p*-channel metal oxide TFTs to realise metal oxide-based CMOS circuits that enable low power consumption, large-area electronics. For example, C. W. Shih, reported high performance *p*-tin oxide (SnO) thin-film transistor (*p*-TFT) by a simple process of reactive sputtering from a tin (Sn) target under oxygen environment, demonstrating high field effect mobility 7.6 $cm^2V^{-1}s^{-1}$, subthreshold slope 140 mV/dec, and on-off current ratio $3 \times 10^4$ [124]. Nickel oxide (NiO) is an attractive *p*-type semiconductor because its properties are very beneficial for many photocatalytic, battery, electrochromic and chemical sensing applications [125]. Fukai Shan *et al.* reported a full solution processed NiOx/AlOx TFTs with an operating voltage of 3.5 V that exhibits high hole mobility of around 25 $cm^2V^{-1}s^{-1}$ [126]. E. Fortunato *et al.* reported copper oxide ($Cu_2O$) based TFTs deposited by reactive RF magnetron sputtering at room temperature and the TFTs exhibited field-effect mobility of 3.9 $cm^2V^{-1}s^{-1}$and an on/off ratio of $2\times10^2$.

Oxide TFTs based electronics are not limited to lab scale research but are now expanding to the commercialization in display applications. W. J. Nam *et al.* successfully fabricated and demonstrated 55-inch OLED TV using IGZO TFTs [127]. Additional applications have also been demonstrated such as ring oscillators by Jiawei Zhang *et al.* [128], a complementary circuit based on *n*-type IGZO and *p*-type tin monoxide (SnO) with an oscillation frequency of 2.63kHz and the peak-to-peak oscillation amplitude 36.1 V at a supply voltage of 40 V.

The ongoing research and continuous increase in TFT performance could establish new markets. A complementary electronic device requires both *p*-channel and *n*-channel TFTs. Complementary inverters are preferred compared to only *n* or *p*-channel inverters because they allow low power consumption, higher gains, and low noise margins. Reported complementary inverters on glass or flexible substrates are mostly composed of organic TFTs for both *p*-channel and *n*-channel. Devices in organic electronics, *p*-type material development occurred much quicker. Among organic semiconductors, *p*-type pentacene has been the most widely studied material, with hole mobility values of 0.1 ~ 1 $cm^2\ V^{-1}\ s^{-1}$. However, recent development has seen hole mobilities >10 $cm^2\ V^{-1}\ s^{-1}$ [129] reported for solution processed polymers. Therefore, hybrid organic-inorganic complementary structures composed of the *n*-type oxide semiconductor and *p*-type organic semiconductor are potential candidates for circuit design based on CMOS technology. For example, Takeya *et al.* reported solution-processed organic($C_{10}$-DNBDT-NW)-inorganic(IZO) hybrid CMOS inverter exhibiting a high gain reaching 890 [130].

## 2.6 Materials for Transparent and Flexible TFTs

In this section properties of various materials used for manufacturing transparent and flexible TFTs are described. They include transparent and flexible substrates, dielectric layer materials of different kinds.

### 2.6.1 Transparent and Flexible Substrates

TCEs and TFTs are usually made on optically transparent substrates. The properties of plastic substrates affect quality and carrier transportation behaviour and limit maximum fabrication temperature. Polymer optical films can be classified according to the glass transition temperature ($T_g$) into three types [131]: (1) conventional polymers ($T_g < 100\ ^0C$), (2) common high temperature polymers ($100 \leq T_g < 200\ ^0C$), and (3) high temperature polymers ($T_g \geq 200\ ^0C$). Glass transition temperature is the temperature, below which the physical properties of plastics change to those of a glassy or crystalline state. Table 2.6 lists the basic properties of three kinds of polymer substrates, which are presently widely used, namely polyimide (PI), polyethylene-napthalate (PEN) and polyethylene terephthalate (PET).

Table 2.6: Basic properties of commonly used flexible transparent substrates [132].

| Material | $T_g$ ($^0C$) | $\lambda_c$ (nm) | CTE (ppm $^0C$) | Chemical resistance | Surface roughness |
|---|---|---|---|---|---|
| PI | 300 | 500 | 12 | Good | Good |
| PEN | 140 | 380 | 20 | Good | Moderate |
| PET | 80 | 300 | 33 | Good | Moderate |
| PDMS | -120 | 200 | 301 | Good | Poor |

Among all of the flexible substrates, PI shows the highest $T_g$, the smallest coefficient of thermal expansion (CTE) and surface roughness. Additionally, PI has also good chemical stability in acid, alkali and organic solvents. Though the cut-off wavelength ($\lambda_c$) is in the visible range, the PI substrates have deep colour and poor optical transmittance. Colourless and optically transparent polyimide (CPI) films have only recently been developed. It appears that the CPI substrates will be one of the best choices for next generation flexible transparent electronics [133]. The optical transparency of PET substrates is good (> 85%) [134] and they are currently widely used as the protection layer in various liquid crystal displays devices (LCDs), such as televisions, computers and cell phones. However, the main drawback of PET is its low $T_g$ ($\approx 80\ ^0C$), which may bring challenges in device fabrication, integration and operation. Furthermore, PET possesses

a high-water vapour transmission rate. PEN substrate has a higher $T_g$ ( ≈ 140 $^0$C) than PET, which makes it a suitable substrate for manufacturing devices [135]. Recently, polydimethylsiloxane (PDMS) substrates are used in flexible electronics applications. PDMS is a type of elastomer and upon flexing and stretching, it induces no plastic deformation [136]. Also, it shows high optical transmittance, short $\lambda_c$, which makes PDMS the perfect substrate for the emerging stretchable electronics [137]. It is worth noting that ultra-thin (25-100 μm) flexible glass [138], [139], for example, Willow by Corning company [140], is also regarded as a promising substrate for flexible transparent electronics. It shows a higher processing temperature (~ 500 $^0$C), good resistance to scratching and higher optical transmittance [141]. However, up to now, a few pieces of research on flexible glass were reported in the literature.

To decrease the surface roughness of substrates and gas permeability, as well as increase the chemical resistance and adhesion of the films, a barrier or encapsulation layer is often used onto the substrates. The commonly used encapsulation materials are $Al_2O_3$, $Si_3N_4$, SiO and $SiO_2$, which are electrically insulating and easily grown by chemical vapour deposition [142]–[145].

### 2.6.2 Dielectric Layers

The quality of the dielectric and the semiconductor/dielectrics interface is of vital importance in many transparent electronic applications. Currently, there are three types of dielectric materials that are commonly used in flexible metal oxide TFTs.

**Inorganic dielectrics:** Silicon dioxide ($SiO_2$) and silicon nitride ($Si_3N_4$) are two kinds of inorganic dielectric materials adopted from a-Si:H and poly-Si TFTs. Nevertheless, the high deposition temperature (above 100 $^0$C) for high-quality films by plasma enhanced chemical vapour deposition (PECVD) hinders their application on flexible substrates. Instead of $SiO_2$ [146], high-k dielectrics ($Al_2O_3$, $HfO_2$) are more widely used in flexible transparent metal oxide TFTs, because they can be synthesized at low temperature by atomic layer deposition (ALD) or solution processes like anodization of aluminum [147]. Inorganic dielectrics, such as $Al_2O_3$, exhibit low-temperature fabrication convenience and result in excellent device performance. However, mechanical failure may occur when the films are under tensile or compressive strains.

**Organic dielectrics:** Organic dielectric materials [148], such as poly(methyl methacrylate) (PMMA) and polystyrene (PS), can sustain larger strain [149] because the

molecules in them are linked through the van der Waals forces and/or hydrogen bonds which are weak interactions. In addition, simple and low-cost processes, such as spin coating and printing, can be used to deposit polymer dielectrics. More recently, low-k fluorinated polymers such as CYTOP have been used as dielectric materials [150]–[152]. Also, CYTOP has been used as a passivation layer in TFTs due to its hydrophobic nature [153], [154].

**Organic/inorganic hybrid dielectrics**: Even though polymeric dielectrics withstand greater strain than their inorganic counterparts and can relax the stress in the channel layer, they have some drawbacks. Firstly, polymers are usually soft, and consequently, the deposition of the channel layer may induce damage inside the polymer layer or at the polymer/channel interface, which will significantly influence the transport behaviour of charge carriers. Secondly, the dielectric constants (k) of most polymers are relatively low (2.5-2.6 for PVP). Thirdly, the polymeric dielectrics are more hydrophobic than inorganic materials, which is undesirable for the direct growth of channel semiconductors [155]. By utilizing a stacked organic/inorganic hybrid gate dielectric, [156] these problems can be solved. Also, by introducing inorganic nanoparticles into polymer matrices to form polymer nanocomposites. This was achieved, for example, Lai *et al.* fabricated a nanocomposite dielectric by incorporating high-k $Al_2O_3$ nanoparticles into polymer PVP films [157]. Majewski and co-workers reported solution processed high-k nanocomposite/low-k polymer bilayer (Barium strontium titanate and barium zirconate nanoparticles were dispersed in a poly (vinylidene fluoride-co-hexafluoropropylene) P(VDF-HFP) polymer matrix) gate dielectric used for the fabrication of organic field-effect transistors (OFETs) that operate effectively at 1V [158].

Various approaches can be used to manufacture flexible electronic devices. Each of them has its distinct requirements regarding the process parameters and utilized materials:

(1) A silicon wafer thinned down to thicknesses below 50 μm becomes flexible, however, investigation on bending limits before a mechanical fracture or failure occurs needs to be carried out [159].
(2) The thinned die can then be attached to a flexible substrate [160].
(3) Devices can be manufactured on polymers such as PET or PEN, which are attached to a rigid, low-cost substrate.

(4) Transfer printing methods can be used to fabricate electronic devices on a large scale, and then transferred to a plastic substrate.

(5) Direct fabrication of devices on unconventional flexible substrates can combine the advantages of standard semiconductor technologies and large area processing, but suffers from the limited thermal stability of flexible substrates [161]. In this thesis, the latter approach was adopted for device fabrication.

### 2.6.3 Metal oxide semiconductors

The oxides of post-transition metals such as ZnO and IGZO have been known for a decade and these materials have large bandgap and wide controllability of carrier concentration, which can make them useful for transparent thin film transistor (TFTs) applications. The conduction mechanism in metal oxide semiconductors is very different from that in conventional Si-based semiconductors. Amorphous silicon has poor carrier transport properties (~1 $cm^2V^{-1}s^{-1}$) relative to single crystalline silicon materials (~500 $cm^2V^{-1}s^{-1}$). This is associated to the structure and conduction mechanism between amorphous and single crystal materials. Si has a strong covalent bond, and the conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding ($sp^3$ σ *) and bonding ($sp^3$ σ) states of Si hybridized orbitals, and its bandgap is formed by the energy splitting of the σ - σ * level shown by Figure 2.6 (a). The mobility of amorphous silicon is small, as carrier transport is controlled by hopping between localized tail states and band conduction is not achieved. Therefore, this hopping mechanism is strongly related to the local range order or structure, such as the strained and disordered chemical bonds from rather deep and high density of localized states below conduction band minimum (CBM) and above valence band maximum (VCM), causing the carrier trapping process. On the other hand, the oxide semiconductors have strong ionicity and charge transfer occurs from heavy metal ion to oxygen atoms shown by Figure 2.6 (b). When heavy metal ions and oxygen ions come close, charge transfer occurs due to largely different electron affinity and ionization potential (Figure 2.6 (c)). In addition, the Madelung potential which comes from the difference between cations and anions by virtue of their opposing charges stabilizes the ionized states during the ionic bonding process. As a result, in Figure 2.6 (c), the Madelung potential induces the energy splitting and the conduction band minimum (CBM) is occupied the 2p orbital of oxygen and the valence band maximum un-occupied by ns orbital of cations.

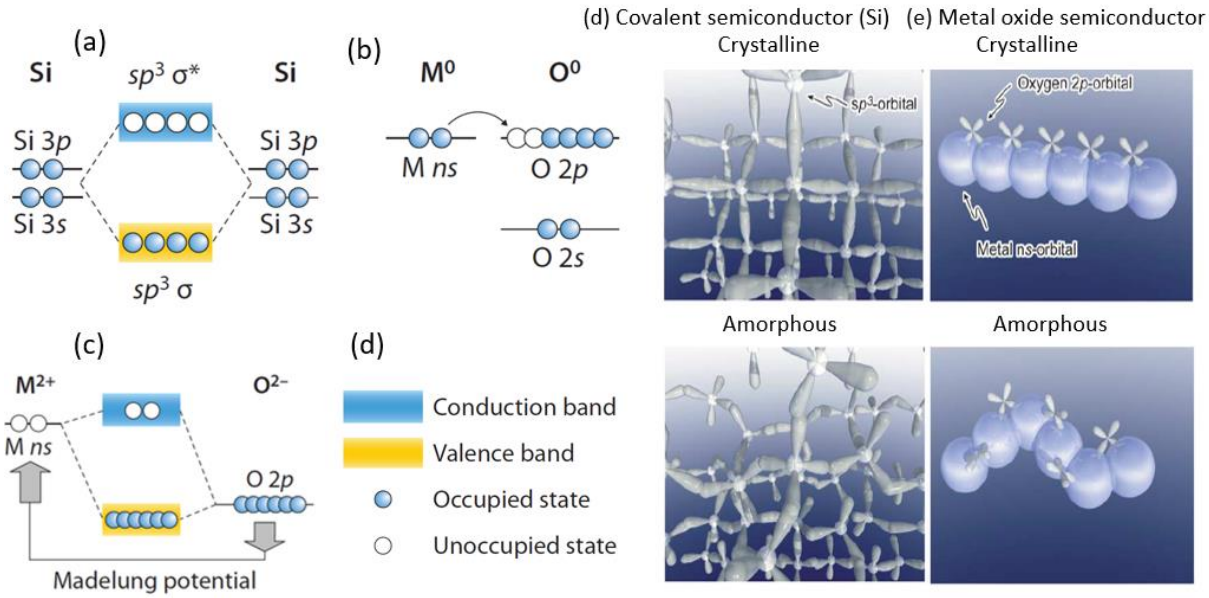


Figure 2.6: Schematic electronic structures of silicon and ionic oxide semiconductors. (a–c) [163].Bandgap formation mechanisms in (a) covalent and (b, c) ionic semiconductors. Closed and open circles denote occupied and unoccupied states, respectively. (d, e) Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors [164]. (d) Covalent semiconductors with $sp^3$ orbitals (e) metal oxide semiconductors with the s-orbital overlap of metal cation.

The CBMs with large spatial sized s-orbital of heavy cations overlaps with the neighbouring metal s orbital, and makes the conduction path for carriers which are not influenced largely by disordered local structure. This is the reason why metal oxide semiconductors have high mobility even though there is an amorphous structure. Figure 2.6 shows the schematic drawing of the structure Si-based and metal oxide semiconductors structure. Figure 2.6 (a) is the Si semiconductor layer which has the hopping mechanism to transfer the electron carriers. In single crystal structure, there is a transfer path with hopping mechanism because of the long-range order in crystal structure using $sp^3$ hybridization orbitals, and have a large amount of electron field mobility. However, the amorphous structure does not have any long-range order in this structure, and electron carriers cannot move fast in this structure because of the barrier with random structure. In a metal oxide semiconductor, large sized s-orbital of metal ion has an overlapping between an adjacent atom, and there provides the current path of electron carrier. Even though there has an amorphous structure in the metal oxide layer, s-orbital is easy to overlap as shown in Figure 2.6 (b).

Amorphous oxide semiconductors have a potential fluctuation above the mobility edge and the distribution of potential barriers exists in the conduction band. These

different paths cause different conductance for electron transmission over the potential barrier. In other words, the carrier density creates the degenerated conduction for amorphous IGZO and crystalline IGZO.

The low defect density in the a-IGZO layer is the reason why IGZO has a good subthreshold slope in the transfer curve. This is therefore possible to apply the low voltage driven TFTs for having low power consumption.

## 2.7 Device Structures of TFTs

Shown in Figure 2.7 are the typical TFTs device structures [165], determined by the position of the gate, source, and drain contacts relative to the active semiconductor film [166]. The basic structures are either coplanar or staggered. In a staggered structure, also called top-contact structure, the gate contact is on the opposite side of the semiconductor film from the source and drain contacts, as shown in Figure 2.7 (a) and (c). In such an arrangement, the source-drain contacts are in direct contact with the induced channel. In a coplanar structure, also called bottom-contact structure, the gate, source, and drain contacts are all located on the same side of the semiconductor film, as shown in Figure 2.6 (b) and (d). TFTs are also categorized as bottom gate (Figure 2.7 (a) and (b)) or top gate ((Figure 2.7 (c) and (d)) based on the position of gate. In this thesis, we have used bottom-gate top-contact structure.

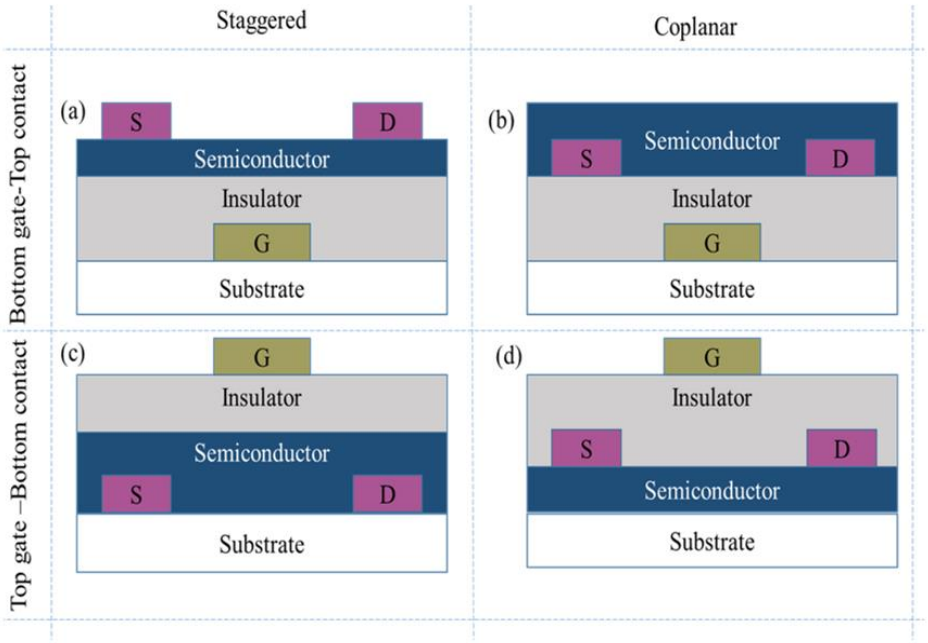


Figure 2.7: Cross-sections of simplified TFT device configurations: (a) Bottom-gate staggered structure (top-contact); (b) Bottom-gate coplanar structure (bottom-contact); (c) Top-gate staggered structure; (d) Top-gate coplanar structure [167].

## 2.8 Operation Principles of TFTs

The TFT is a three-terminal device, in which a voltage ( positive for *n*-type and negative for *p*-type material) applied to gate electrode controls current flow between source and drain electrodes under an applied voltage bias [168]. In electron transporting TFTs, modulation of a negative channel current flowing between the metallic source and drain terminals by the applied positive gate voltage ($V_G$) forms the basis of the device operation. The gate electrode is always separated from the semiconductor by the gate dielectric. The source terminal is always grounded ($V_S$=0V). Electrode materials with appropriate work functions (i.e. matching energies) are selected to optimize electron injection and reduce parasitic effects such as contact resistance. Application of $V_G$ modulates the conductivity of the semiconductor region in proximity of the gate dielectric. When a source-drain voltage ($V_{DS}$) is applied to the device, injected charge carriers (holes or electrons for *p*-channel and *n*-channel devices, respectively) accumulate at the semiconductor/insulator interface giving rise to a channel current that flows between the source and drain terminals. When the electric field strength corresponding to $V_{DS}$ is significantly smaller than that of $V_G$, the TFT operates in the so-called 'linear' regime: the distribution of electrons across the channel is uniform and the channel drain current ($I_D$) varies linearly with the applied $V_{DS}$. If the field strengths corresponding to $V_G$ and $V_D$ are comparable, the device enters the 'saturation' regime, where $I_D$ saturates and becomes independent of $V_{DS}$. This is the point at which the depletion of electrons occurs at the region closest to the drain electrode, and thus the channel is described as pinched-off.

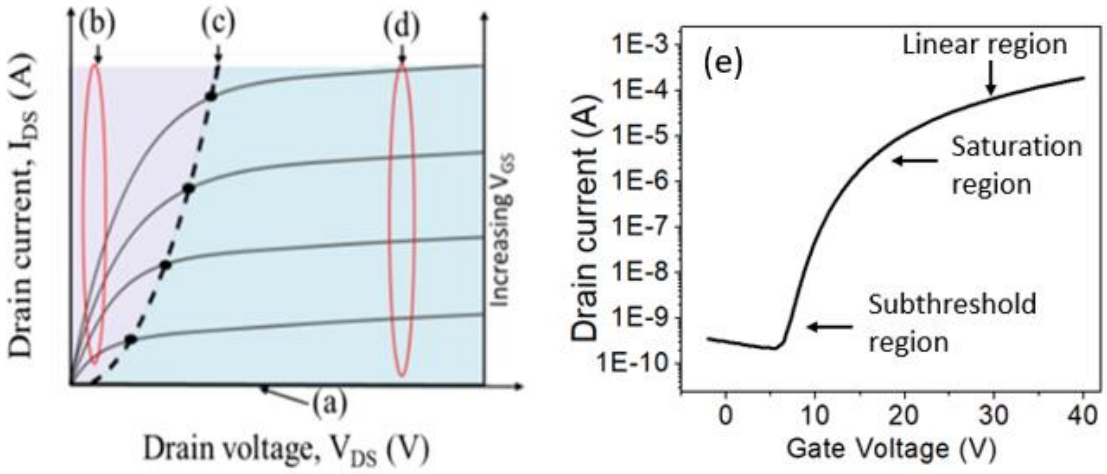

Figure 2.8 shows the four regions of *n*-channel TFT operation (a) off region (b) linear region (c) pinch off points (d) saturation region in a bottom-gate top-contact metal oxide TFT output characteristics and (e) transfer characteristics of n- channel TFT.

An oxide TFT device can be considered as two capacitor plates separated by an insulator between source/drain contact and gate contact as shown in figure 2.9 (a). To better understand the working of metal oxide TFTs, the energy band diagrams of a metal insulator semiconductor (MIS) structure are shown in Figure 2.9. Different from metal oxide semiconductor field-effect transistor (MOSFET) operations using an inversion-mode, organic or oxide semiconductor TFTs are operated in the accumulation-mode [169][170]. Figure 2.9 shows several energy band diagrams as viewed through the gate of an *n*-channel TFT operating in such mode. For simplicity, hereafter the operation of TFTs will be reviewed by assuming an oxide semiconductor channel.

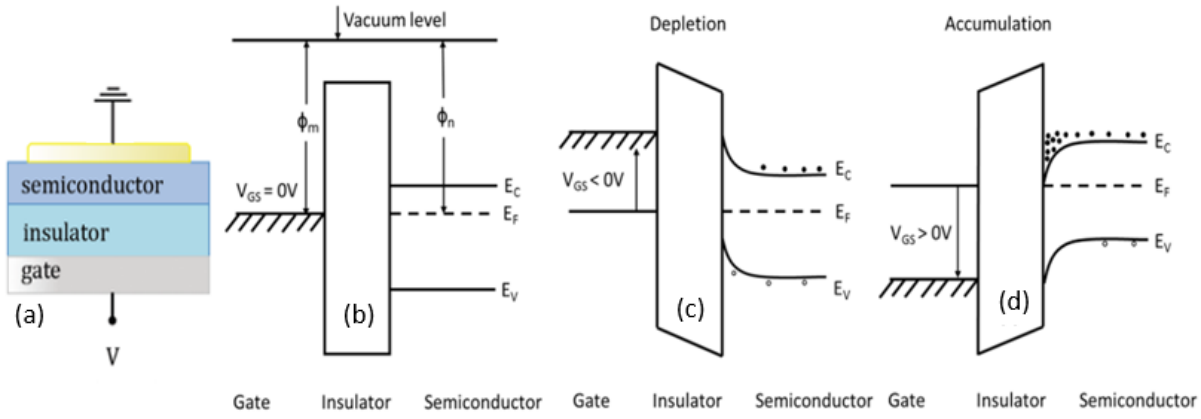


Figure 2.8: (a) Schematic cross-section representation of a MIS capacitor. Energy band diagrams of MIS capacitor as viewed through the gate for different biasing conditions: (b) equilibrium, (c) $V_{GS}$ <0 V, and (d) $V_{GS}$ >0 V [166].

For an ideal MIS device, the work functions of the metal ($\Phi_m$) and semiconductor ($\Phi_n$) are equal which leads to the alignment of Fermi levels at equilibrium and no band bending or charge accumulation or depletion at the semiconductor interface. Figure 2.9 (b) shows an energy band diagram of such a device in equilibrium, with 0V applied to the gate. Figure 2.9 (c) shows an energy band diagram with the gate biased negatively. The applied negative bias repels mobile electrons from the semiconductor, leaving an electron depletion region near the insulator/semiconductor interface. When compared with the no bias condition, this biasing condition has a reduced conductance due to the reduced number of mobile electrons in the semiconductor. Figure 2.9 (d) shows an energy band diagram with the gate biased positively. The applied positive bias attracts mobile

electrons, forming an accumulation region near the insulator/semiconductor interface and these excess mobile electrons lead to an increase in the conductance.

The current-voltage characteristics of a TFT were derived based on the gradual channel approximation[171][172] with the x direction is defined as perpendicular to the channel and y parallel to the channel as shown in Figure 2.10. The edge of the source is at y = 0 and the edge of the drain at y = L. In this approximation, the charge carrier density per unit area in the channel varies as function of position in the y direction, thus the carrier concentration in channel is dependent on the lateral potential, V(y), which is largely determined by the drain potential $V_D$ as well as the material properties of the channel[173]. The external parameters controlling the drain current $I_{DS}$ are gate-to-source voltage ($V_{GS}$) and the drain-to-source voltage ($V_{DS}$). When gate-to-source voltage is set to be a value larger than the threshold voltage, $V_T$, of the TFT, carriers in the semiconducting channel layer between the source and drain are generated.

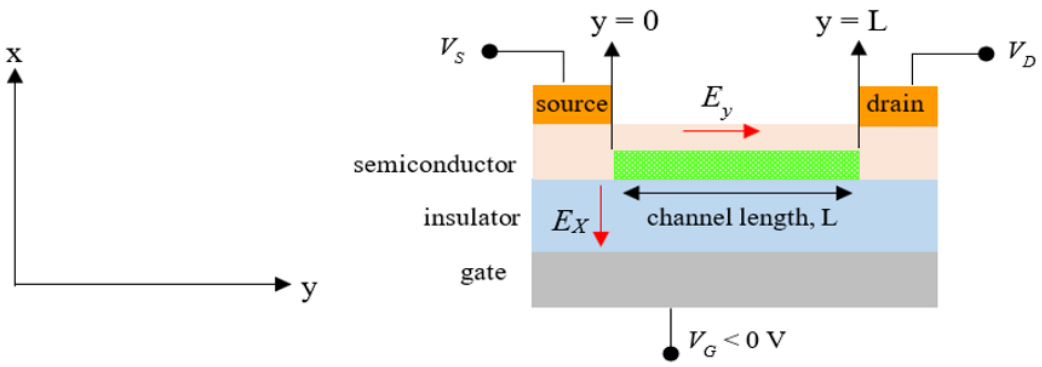


Figure 2.9: Cross-sectional view of the channel region of TFT used to derive the gradual channel approximation with x direction is perpendicular to the channel and y is parallel to the channel.

It is assumed that the carrier mobility along the channel is constant. However, in practical reality this is not always fulfilled, the threshold voltage changes along the channel since the channel voltage is not constant. Also, assume that the electric field component $E_y$ along the y-coordinate is dominant compared to the electric field component $E_x$ along the x-coordinate so that the current flows in the channel to the y-dimension only. This is known as gradual channel approximation. The boundary conditions for the channel voltage V(y) are as follows:

$$V(y=0) = V_S = 0 \text{ and } V(y=L) = V_{DS} \quad \text{Eq. 2.5}$$

Also, it is presumed that the entire channel region is in accumulation mode, that is:

$$V_{GS} \geq V_T,\ V_{GD} = V_{GS} - V_{DS} \geq V_T \qquad \text{Eq. 2.6}$$

Assuming $C_i$ is the capacitance per unit area of the gate insulator and $V_C$ channel potential equal to zero, the charge density Q in the channel, when gate potential is greater than threshold voltage, is related to gate voltage as follows:

$$Q = -C_i\,(V_{GS} - V_T) \qquad \text{Eq. 2.7}$$

Let $Q_I(y)$ be the total mobile electron charge in the accumulation layer. The charge can be expressed as a function of the gate-to-source voltage $V_{GS}$ and the channel voltage $V_C(y)$ by equation 2.8:

$$Q = -C_i\,[\,V_{GS} - V_T - V_C(y)] \qquad \text{Eq. 2.8}$$

Let dR be the incremental resistance of the differential channel segment *dy* and *dQ* the corresponding differential charge. If all mobile electrons in the accumulation layer have uniform mobility, the incremental resistance can be expressed as follows:

$$dR = -\frac{dy}{W\mu Q_I(y)}\,dy \qquad \text{Eq. 2.9}$$

Where *W* is the channel width, μ is the field-effect mobility. Note that the minus sign is due to the negative polarity of the accumulation layer charge $Q_I$. We will assume that the channel current density is uniform across the segment. According to the one-dimensional model, the channel current, $I_{DS}$, flows between the source and drain in the y-coordinate direction. Using Ohm's law for this segment, the voltage drop along the incremental segment dy in the y-direction is given by equation 2.10:

$$dV_C = dR\ I_{DS} = -\frac{I_{DS}}{W\mu Q_I(y)}\,dy \qquad \text{Eq. 2.10}$$

Integrating the above equation along the channel from y=0 to y=L, using the boundary conditions stated earlier yields,

$$\int_0^L I_{DS}\,dy = -W\mu \int_0^{V_{DS}} Q_I(y)\ dV_C \qquad \text{Eq. 2.11}$$

The left-hand side of this equation is simply equal to $I_{DS}L$. The integral on the right-hand side is evaluated by replacing $Q_I(y)$ with equation 2.9. Thus,

$$I_{DS}L = W\mu\, C_i \int_0^{V_{DS}} (\,V_{GS} - V_T - V_C\,)dV_C \qquad \text{Eq. 2.12}$$

Assuming that the channel voltage $V_C$ is the only variable in equation 2.11 that depends on the position y, the drain current is as follows:

$$I_{DS} = \mu C_i \frac{W}{L}((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2) \quad \text{Eq. 2.13}$$

In the linear region ($V_{DS} \ll V_{GS}$) the drain current can be written as:

$$I_{DS} = \mu C_i \frac{W}{L}(V_{GS} - V_T)V_{DS} \quad \text{Eq. 2.14}$$

When the TFT is biased within the pinch-off region and $V_{DS} = V_{GS} - V_T$, the drain current saturates. For the saturation region ($V_{DS} > V_{GS} - V_T$), equation 2.14 is no longer valid. The saturation drain current can be obtained by substituting $V_{DS} = V_{GS} - V_T$ into equation 2.13, yielding:

$$I_{DS} = \mu C_i \frac{W}{2L}(V_{GS} - V_T)^2 \quad \text{Eq. 2.15}$$

The gradual channel approximation assumes that the mobility is independent of the gate voltage and that the S/D contacts have negligible resistance.

## 2.9 Extraction of Performance Parameters of TFTs

TFTs are characterized by measuring the output and transfer characteristics. By measuring the output and transfer characteristics, the important TFT performance parameters such as saturation mobility ($\mu_S$) in the saturation regime, the threshold voltage ($V_T$), Turn ON voltage ($V_{ON}$), on-off current ratio ($I_{on}/I_{off}$), and subthreshold slope (SS) were obtained.

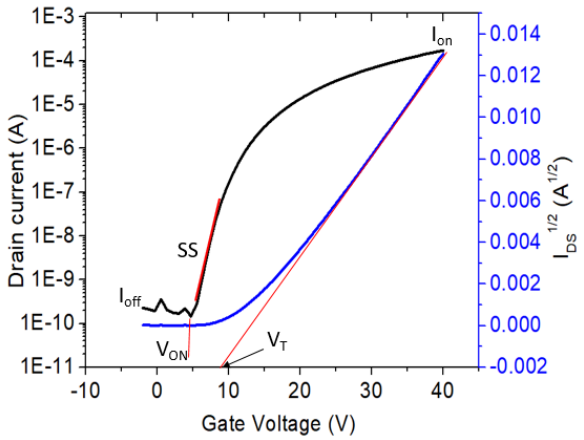


Figure 2.10: The transfer characteristic of a *n*-channel TFT and square root of $I_{DS}$, showing various performance parameters such as drain ON current ($I_{on}$), drain off current ($I_{off}$), the TFT threshold voltage ($V_T$), TFT turn ON voltage ($V_{ON}$), subthreshold slope (SS).

Shown in Figure 2.11 the transfer characteristic of a *n*-channel TFT illustrating various performance parameters like subthreshold slope (SS), the threshold voltage ($V_T$) and drain ON current ($I_{on}$). The mobility in the saturation regime can also be extracted from the transfer characteristics. The saturation mobility can be extracted from the slope (equation 2.16) of the curve, which plots the square root of the saturation current as a function of the gate to source voltage ($V_{GS}$). The threshold voltage $V_T$ can be determined by extrapolating this linear region to the horizontal x-intercept, as shown in Figure 2.11.

$$slope = \frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}} = \sqrt{\frac{WC_i\mu_S}{2L}} \qquad \text{Eq. 2.16}$$

$$\mu_S = \left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \frac{2L}{WC_i} \qquad \text{Eq. 2.17}$$

Drain current on-off ratio is also extracted from the transfer characteristics. This ratio was determined by taking the ratio between the maximum on-current measured ($I_{on}$) and the minimum off-current measured when the TFT is off ($I_{off}$). Subthreshold swing is also the inverse of the subthreshold slope. The inverse subthreshold slope (SS) is estimated as the minima on a $(\partial(\log I_{DS})/\partial V_{GS})^{-1}$ vs. $V_{GS}$ graph.

$$SS = \frac{d|V_{GS}|}{d\ log|I_{DS}|} \qquad \text{Eq. 2.18}$$

where, SS is the subthreshold slope in V/decade.

## 2.10 State-of-the-Art Performance in Metal Oxide TFTs

The main progress of metal oxide TFTs is summarized in Table 2.7. Adamopoulos *et al.* reported high-mobility (85 $cm^2V^{-1}s^{-1}$) Li-doped ZnO TFTs based on $ZrO_2$ high-k dielectric grown by spray pyrolysis in ambient air [174]. This is one of the highest reported mobility values for transistors based on a combination of a solution-processed oxide semiconductor and an oxide high-k dielectric to date. Hu *et al.* [120] reported a high mobility (142 $cm^2V^{-1}s^{-1}$) Cu-contacted IGZO TFT by depositing an $Al_2O_3$ passivation layer on the back channel using RF sputtering. The underlying mechanism for the high mobility

was attributed to the generation of an In-rich layer at the IGZO and $Al_2O_3$ interface that increases the carrier concentration.

Table 2.7: Some of the state of the art flexible transparent TFTs based on ZnO and related materials from 2011-2019. "--" means not mentioned or not clear in the literature.

| Material | Technique | $T_{dep.}$ /$T_{post.}$($^0$C ) | Substrate | Dielectric | $\mu$($cm^2V^{-1}s^{-1}$) | On/off | Reference | Year |
|---|---|---|---|---|---|---|---|---|
| ZnO | Spray Pyrolysis | 300/500 | $Si^{++}$ | $SiO_2$ | 25 | $10^6$ | Adamopoulos *et al.* [175] | 2011 |
| Li-doped ZnO | Spray Pyrolysis | 400 | ITO | $ZrO_2$ | 85 | $10^6$ | Adamopoulos *et al.* [174] | 2011 |
| InSnO | Co-sputtering | 150 (Vacuum) | Si | $SiO_2$ | 28.7 | $10^9$ | Seo *et al.* [176] | 2016 |
| ZTO | CVD | 350 | -- | -- | 14.6 | $10^7$ | Park *et al.* [177] | 2017 |
| IGZO | Spin | --/500 | Thin glass | $Ta_2O_5$ | 23.8 | $10^6$ | Dai *et al.*[155] | 2013 |
| IGZO | Sputtering | RT/300 (Ar) | glass | $Al_2O_3$ | 142 | $10^8$ | Hu *et al.*[120] | 2017 |
| IGZO | Sputtering | RT/400 | glass | $Al_2O_3$ | 14 | -- | Nam *et al.*[178] | 2018 |
| IGZO | Sputtering | 100 | glass | $Al_2O_3$ | 26.03 | $10^7$ | Liu *et al.* [179] | 2019 |

## 2.11 Process Optimization Techniques

In this section, process optimization techniques, Taguchi methods and Plackett-Burman design are discussed. Process optimisation techniques are an important tool for reducing the production time but have not been widely applied in metal oxide TFT development. The positive outcomes of process optimization techniques are minimized cost, maximized production with better accuracy.

### 2.11.1 Taguchi Orthogonal Arrays

The method of laying out the conditions of experiments linking multiple factors was first proposed by R.A. Fisher [180]. The method is commonly known as the factorial design of experiments. Most of the research processes usually involve a significant number of factors and a full factorial design results in a large number of experiments. To decrease the number of experiments to a practical level, only a small set from all the possibilities is selected. The method of selecting a limited number of experiments that produce the most information is known as a partial fraction experiment [181]. A well planned set of experiments, in which all parameters of interest are varied over a specified range, is a much better approach to obtain systematic data. Dr. Taguchi of Nippon Telephones and Telegraph Company, Japan has developed a method based on "Orthogonal Array" experiments which gives much reduced" variance " for the experiment with" optimum

settings " of control parameters. Taguchi constructed a special set of general design guidelines for factorial experiments that cover many applications [182]. This method uses a special set of arrays called orthogonal arrays (OA). These standard arrays lay down the way of conducting the minimal number of experiments, which could give the full information of all the factors that affect the performance parameter. The root of the OA method lies in choosing the level combinations of the input design variables for each experiment run.

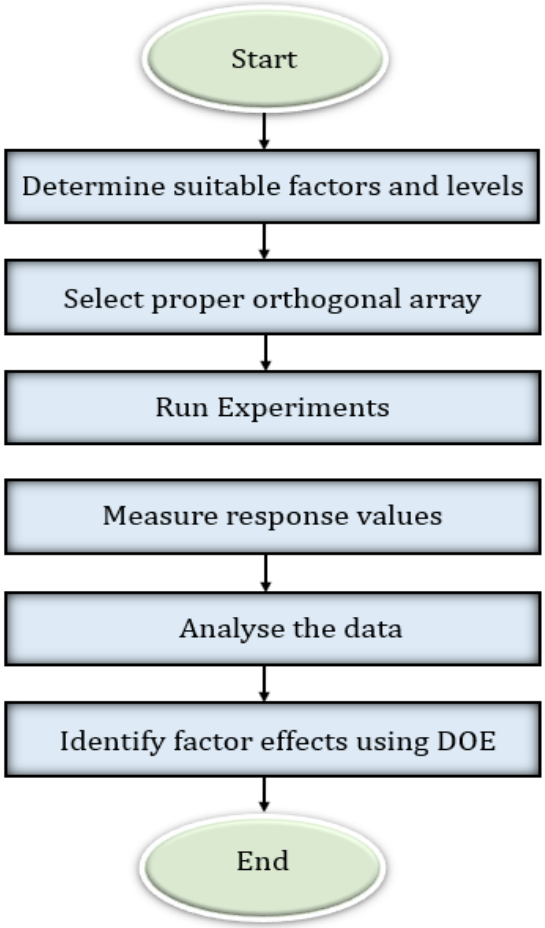


Figure 2.11: Taguchi method design procedure for process optimisation.

There are many standard OAs available, each of the arrays are designated for a specific number of independent design variables and levels. For example, in order to perform an experiment to understand the influence of 4 different independent variables (as used in this work) with each variable having 3 set values (level values), then an $L_9$ OA might be the right choice.

Shown in Figure 2.12 is the Taguchi method design procedure for process optimisation. This procedure starts with determining suitable factors and levels and selecting proper OA. Then, all experiments are run according to selected OA. Finally, after measuring the response values analyse the data using design of experiment (DOE) software tool.

The $L_9$ OA is selected for understanding the effect of 4 independent factors each having 3 factor level values [183][184]. This array assumes that there is no interaction between any two factors. While in many cases, no interaction model assumption is valid, there are some cases where there is clear evidence of an interaction.

**Table 2.8: General Layout of $L_9$ orthogonal array (OA).**

| $L_9$ ($3^4$) Orthogonal array | | | | | |
|---|---|---|---|---|---|
| Run number | Independent variables (input factors) | | | | Performance parameter value |
| | Variable 1 | Variable 2 | Variable 3 | Variable 4 | |
| 1 | 1 | 1 | 1 | 1 | p1 |
| 2 | 1 | 2 | 2 | 2 | p2 |
| 3 | 1 | 3 | 3 | 3 | p3 |
| 4 | 2 | 1 | 2 | 3 | p4 |
| 5 | 2 | 2 | 3 | 1 | p5 |
| 6 | 2 | 3 | 1 | 2 | p6 |
| 7 | 3 | 1 | 3 | 2 | p7 |
| 8 | 3 | 2 | 1 | 3 | p8 |
| 9 | 3 | 3 | 2 | 1 | p9 |

Shown in Table 2.8 is the general layout of $L_9$ OA. There are entirely 9 experiments to be conducted and each experiment is based on the combination of level values as shown in Table 2.8. For example, the third experiment is conducted by keeping the independent design variable 1 at level 1, variable 2 at level 3, variable 3 at level 3, and variable 4 at level 3.

### 2.11.2 Properties of Orthogonal Arrays

The orthogonal arrays have the following distinct properties that reduce the number of experiments to be conducted.

The vertical column under each independent variables of Table 2.8 has a special combination of level settings. All the level settings appear an equal number of times. For

$L_9$ array under variable 4, level 1, level 2 and level 3 appears thrice. This is called the balancing property of orthogonal arrays.

All the level values of independent variables (input factors) are used for conducting the experiments. The sequence of level values for conducting the experiments shall not be changed. This means one cannot perform experiment 1 with variable 1, level 2 setup and experiment 4 with variable 1, level 1 setup. The reason for this is that the array of each factor column is mutually orthogonal to any other column of level values. The inner product of vectors corresponding to weights is zero. If the above 3 levels are normalized between -1 and 1, then the weighing factors for level 1, level 2, level 3 are -1, 0, 1 respectively. Hence the inner product of weighing factors of independent variable 1 and independent variable 3 would be

$$(-1 * -1+-1*0+-1*1) +(0*0+0*1+0*-1) +(1*0+1*1+1*-1) =0 \quad \text{Eq.2.5}$$

The design of experiments using the OA is, in most cases, efficient when compared to many other statistical designs. The minimum number of experiments that are required to conduct the Taguchi method can be calculated based on the degrees of freedom approach.

$$N_{Taguchi} = 1 + \sum_{i=1}^{NV} (L_i - 1) \quad \text{Eq.2.6}$$

where, NV is the number of independent variables and $L_i$ is the number of levels.

For example, in the case of 8 independent variables study having 1 independent variable with 2 levels and the remaining 7 independent variables with 3 levels ( L18 orthogonal array), the minimum number of experiments required based on the above equation is 16. Because of the balancing property of the orthogonal arrays, the total number of experiments shall be multiple of 2 and 3. Hence, the number of experiments for the above case is 18.

### 2.11.3 Assumptions of the Taguchi Method

The additive assumption implies that the individual or main effects of the independent variables on performance parameter are separable. Under this assumption, the effect of each factor can be linear, quadratic or of higher order, but the model assumes that there exists no cross-product effects (interactions) among the individual factors. That means

the effect of independent variable 1 on performance parameter does not depend on the different level settings of any other independent variables and vice versa. If at any time, this assumption is violated, then the additivity of the main effects does not hold, and the variables interact violated, then the additivity of the main effects does not hold, and the variables interact.

### 2.11.4 Plackett-Burman Design

Plackett–Burman's designs are experimental designs presented in 1946 by Robin L. Plackett and J. P. Burman. An established and economical approach that gives information only on the effects of single factors, but not on interactions, is the Plackett–Burman Design (PBD) method. At the early stage of an experimental search, it is important to identify the subspace of active factors among many, in other words, many factors are considered and the objective is to identify those factors that have large effects. This is known as factor screening (to identify a set of active factors from a larger set of factors). The number of runs n in a PB design is equal to a multiple of four[185]. Plackett and Burman only included the designs with $n \leq 100$, and they also omitted the design where $n = 92$. For PB designs where the number of runs is equal to a power of two, the designs coincide with the regular ones, and the rest of the PB designs are non-regular.

Shown in Table 2.9 the 12-run PBD matrix. In this thesis a 12 run PBD with eight factors and 2-levels fractional factorial design was applied to study N-1 variables using N experimental runs, where N is a multiple of four. In Table 2.9, the letter L and H refers to the “low value” and “high value” for each process factor, respectively.

Table 2.9: Layout of Plackett-Burman matrix for 12 runs screening 8 factors (A-H).

| Run | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 1 | L | L | L | L | L | L | L | L |
| 2 | H | L | H | H | L | H | H | H |
| 3 | L | L | L | H | L | H | H | H |
| 4 | H | L | L | L | H | L | H | H |
| 5 | H | H | L | H | H | H | L | L |
| 6 | L | H | L | H | H | H | L | L |
| 7 | H | H | H | L | L | L | H | L |
| 8 | L | L | H | L | H | H | H | H |
| 9 | H | L | H | H | H | L | L | L |
| 10 | H | H | L | L | L | H | L | H |
| 11 | L | H | H | L | H | H | H | L |
| 12 | L | H | H | H | L | L | L | H |

## 2.12 Accelerated Lifetime Testing

A challenging issue, which has not received much attention, is the stability of AgNWs over long periods. For example, silver is known to be prone to electromigration [186], where the flow of current causes the slow movements of ions in a conductor. It is also observed that AgNWs are unstable at temperatures as low as 200 $^0$C [187] and are affected by light exposure and environmental conditions.

Long-term stability of manufactured devices is very important and the best method to check or test their stability is to subject devices to different accelerated environmental conditions such as high temperature/humidity or high voltage/current. Accelerated Lifetime Testing (ALT) is needed at various stages of a product development cycle, for example, when identifying optimal material sets, providing relative comparisons of device stability [188] and also information on the product's failure mechanisms [189]. As devices are applied in more commercial applications, there is a greater need to predict the expected life in the outdoor operational environment. For the longer term, companies trying to commercialize this technology would also need predictive ageing to estimate warranty provisions. An alternative technique is to use life test models based upon quantitative ALT to address lifetime and try to quantify the degradation through the application of a mathematical model.

### 2.12.1 Quantitative Accelerated Life Tests (QALT)

For all life tests, some time-to-failure information (or time-to-an-event) for the product is required since the failure of the product is the event that needs to be understood [185]. Accelerated life testing is the process of testing a product or device by subjecting it to conditions (stress, strain, temperatures, voltage, vibration rate, pressure, etc.) above its normal conditions to uncover faults and potential modes of failure in a short amount of time. Performed correctly, accelerated testing can significantly reduce test times, resulting in reduced time to market, lower product development costs.

There are several types of accelerated testing approaches and the accelerated testing strategy must be carefully designed to fit the product under consideration. Quantitative accelerated life tests (QALT), on the other hand, are designed to quantify the life of the product and to produce the data required for accelerated life data analysis. This type of test involves the controlled application of accelerated stress conditions to stimulate product failure and provide life data more quickly. The life data obtained from these tests can be used to estimate a probability density function for the product under

normal use conditions and to calculate reliability, probability of failure, mean life, failure rate, and other important reliability metrics for the product.

## 2.13 Electrical and Environmental effects in AgNW Films

Electrical current flow in conductors can cause their temperatures to rise if resistance is high. If the temperature approaches the melting point, the conductor will degrade. This is a particular problem in AgNWs as the diameters are very low and current densities are high, therefore understanding the electrical stability of AgNW films is of importance. Most of the previously reported works on the electrical failure of AgNWs focused on the observation of failure under current flow, without a solution offered for how to mitigate the phenomenon. For example, Khaligh *et al.* demonstrated that when AgNW electrodes conduct current at levels encountered in organic solar cells, the electrodes can fail within two days [190]. The reason for electrode failure is the Joule heating effect which causes the nanowires to breakdown and thus produces an electrical discontinuity in the nanowire network [191].

More heat is created at the localised junction of AgNWs, and consequently, failure occurs sooner in more resistive electrodes and at higher current densities [192]. Heat in conductors is transferred to other components and insulation materials, primarily by conduction and convection, so thermal damage can be caused to these. High currents can also cause component parameter values, such as resistance, to drift over time. This effect is also accelerated by high operating temperatures.

Another important issue for the failure of silver nanomaterials is that they are susceptible to oxidation or sulfidation under normal environmental conditions. For example, Jiu *et al.* reported that AgNW electrodes can be easily damaged in the air due to sulfidation or oxidation based on humidity and harmful gases [193]. Hence, for wide applications of AgNW films over long durations, one still needs to design suitable test conditions and search for suitable coating materials for AgNW TCE encapsulation.

## 2.14 Summary

This chapter presented the fundamental properties of AgNWs, metal oxides semiconductors and the basic operation principle of TFTs. TCEs based on various materials, applications and their post processing were reviewed. Typical TFT four possible device structures were discussed. Materials properties for optically transparent polymer/plastic film substrates, dielectric and TFT active layers were detailed. State-of-

the-art performances in metal oxide TFTs were reviewed. Process optimization techniques, Taguchi methods, Plackett-Burman design were discussed. Accelerated life testing and electrical effects in AgNW films were reviewed. The long-term stability of manufactured devices is very important and the best method to check or test their stability is to subject devices to different accelerated real-world environmental conditions.

# Chapter 3. Experimental Methods Used for Fabrication and Characterization

This chapter presents details of the materials and methods used during this Ph.D. work. The methods and experimental setups used for manufacturing silver nanowire (AgNW) transparent conductive electrodes (TCEs), ZnO TFTs, IGZO TFTs, high-k $Al_2O_3$ dielectric and their measurements are described. Further, IV characterization of TCEs, TFTs and the density of states is described. Also, experimental setups for accelerated lifetime testing (ALT) of TCEs, TFTs and post processing of TCEs are presented.

## 3.1 AgNWs solution Preparation

Three types of AgNWs were used for the preparation of AgNWs solution, namely thin short nanowire; AgNWs-60S ($d_{mean}$ = 60 nm, $L_{mean}$ = 20-30 μm), thin long nanowire; AgNWs-30L ($d_{mean}$ = 30 nm, $L_{mean}$ = 100-200 μm) and thick long nanowires; AgNWs-100L ($d_{mean}$ = 100 nm, $L_{mean}$ = 100-200 μm). All AgNWs dispersions were prepared in the clean room at room temperature. All AgNWs materials were diluted with ethanol to the concentration of 0.4 mg/ml for preparation of AgNWs solution. All AgNWs solutions were ultrasonicated just prior to spray coating on PEN substrates and this was done in order to ensure that the AgNWs were dispersed properly in the suspension before spray coating. A short duration was used (<5 minutes) at low power in order to ensure no breakage of AgNWs.

### 3.1.1 Materials and AgNW Solution Preparation

AgNWs (silver purity 99.5%, concentration 20 mg/mL in ethanol) were purchased from ACS materials. Flexible transparent substrates of polyethylenenapthalate (PEN) with thickness 125 μm were used for manufacturing TCEs. Polymethylmethacrylate (PMMA, molecular weight 495K, 8% solution in anisole) was purchased from Microchem. For this work, a PMMA buffer layer was employed to reduce the surface roughness of the substrates. High performance liquid chromatography (HPLC) grade isopropyl alcohol (IPA), ethanol (EtOH) and acetone were purchased from Sigma-Aldrich and used for cleaning of substrates. Deionized (DI) water was used from the in-house facility of Bangor University. Nickel shims were used for the embossing process explained in section 3.2. Zinc oxide nanoparticles of average particle size less than 100nm were purchased from Sigma-Aldrich and used to further improve surface properties of TCEs.

Shown in Table 3.1, the list of all selected materials used for the TCE preparation.

Table 3.1: Selected materials used for TCEs preparation.

| Type | Materials | Diameter (nm) | Length (µm) | Purity (%) | Concentration (mg/mL) | Thickness (µm) |
|---|---|---|---|---|---|---|
| Silver nanowires | AgNWs-60S | 60 | 20-30 | 99.5 | 20 | - |
| | AgNWs-30L | 30 | 100-200 | 99.5 | 20 | - |
| | AgNWs- 100L | 100 | 100-200 | 99.5 | 20 | - |
| Nanoparticle | ZNO NP | < 100 | - | - | - | - |
| Solvents | IPA | - | - | 98 | - | - |
| | Ethanol | - | - | 95 | NA | - |
| | Acetone | - | - | 99.9 | NA | - |
| Substrates | PEN | - | - | - | - | 125 |
| | ITO on PET | - | - | - | - | 127 |
| Buffer layer | PMMA | - | - | - | - | 10 |
| Anti-sticking solution | BGLGZ83 | - | - | - | - | - |
| Stamp | Ni Shim | - | - | - | - | 200 |

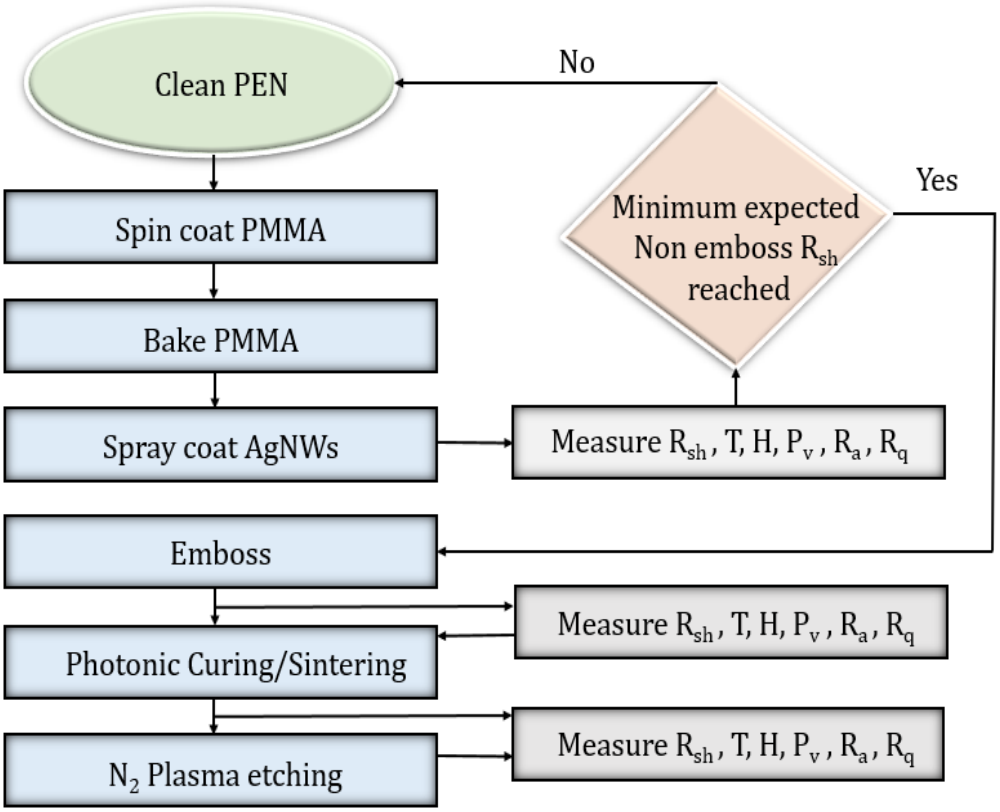


Figure 3.1: AgNW TCEs preparation flow chart, showing process steps of spray coating and post processing of AgNW TCEs. $R_{sh}$ is sheet resistance, T is transmittance, and H is % haze of TCE and PV, Pa and Pq are roughness parameters peak to valley, average roughness, and RMS roughness respectively.

### 3.1.2 Fabrication Steps of AgNW Electrodes

Shown in Figure 3.1, is the flow chart of fabrication steps for AgNW TCEs. PEN film was cut into 15×18 $mm^2$ substrates and thoroughly cleaned with DI water, acetone and IPA, followed by drying with a jet of dry nitrogen. For this work, a PMMA buffer layer was spin coated onto the PEN substrates at 2000 rpm followed by annealing at 100 $^oC$ for 1 minute. AgNWs were spray coated onto the substrates. Finally, post processing steps; thermal embossing, $N_2$ plasma and photonic sintering were performed.

### 3.1.3 Experimental Setup for Spray Coating AgNWs

In this thesis, the spray coating technique has been used for AgNWs film deposition. This method is inexpensive, easy to use and does not require any complex equipment. Furthermore, using this method, the AgNWs solution can be distributed uniformly on the substrate. Initial spray deposition was performed using hand spray coater. Later spray coating was conducted using a custom-built system with ultrasonic spray atomiser supplied by MTI in South Korea. The substrates were placed on the substrate heater at 60 $^0C$ and the AgNWs dispersion was sprayed onto the heated substrates to evaporate the ethanol carrier. The deposition time for preparing the initial electrode film with $R_{Sh} \approx 25$ $\Omega\ sq^{-1}$ was 5 minutes ±5 seconds. Composite ZnO NP/ AgNWs transparent electrodes were manufactured by spray coating nanoparticles onto post-processed AgNWs films.

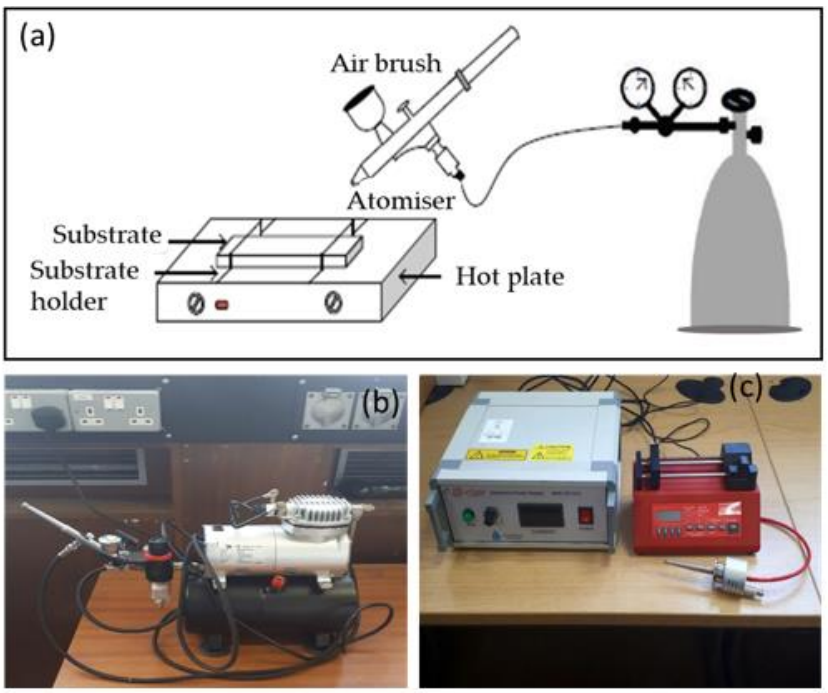


Figure 3.2: (a) Schematic illustration of spray deposition setup, (b) hand spray deposition setup, (c) ultrasonic spray coater, power supply, and atomizer.

Shown in Figure 3.2 (a) is the schematic illustration of spray deposition setup, (b) hand spray deposition setup, (c) ultrasonic spray coater, power supply and atomizer. For the AgNWs spray coating, a back pressure of the air was kept at 1 bar. A piston-type oil-less airbrush compressor was used to achieve a uniform gas/liquid flow rate (0.2 ml $min^{-1}$) at the spray nozzle. The spray nozzle diameter was 0.5 mm and the fluid cup capacity was 7 $cm^{-3}$.

## 3.2 AgNWs Film Deposition and Post Processing Approach

In this work three post-processing methods were sequentially applied onto the AgNW TCEs to achieve high performance; thermal embossing, Nitrogen ($N_2$) plasma treatment and photonic sintering of electrodes. Figure 3.3 shows the fabrication procedure for applying these treatment processes. All three post processing techniques are undertaken sequentially, but these are all transferrable onto a R2R system.

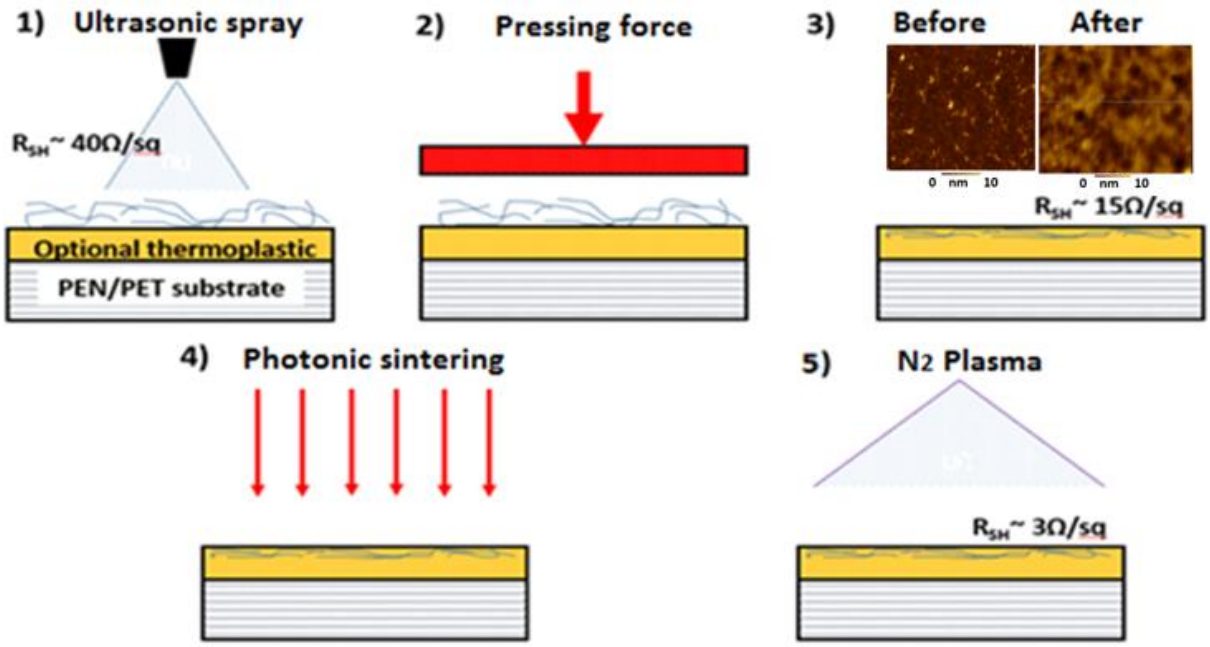


Figure 3.3: AgNWs film deposition and post processing approach: thermal embossing, photonic sintering, $N_2$ plasma treatment are used for post-treatment.

### 3.2.1 Embossing Experimental Setups for AgNW TCEs

AgNW TCEs were thermally embossed to enhance electrical and surface smoothness properties. For this purpose, two experimental setups were used; firstly, an in-house embossing machine is shown in Figure 3.4 and secondly a nano imprint lithography (NIL) system manufactured by Obducat, as shown in Figure 3.5.

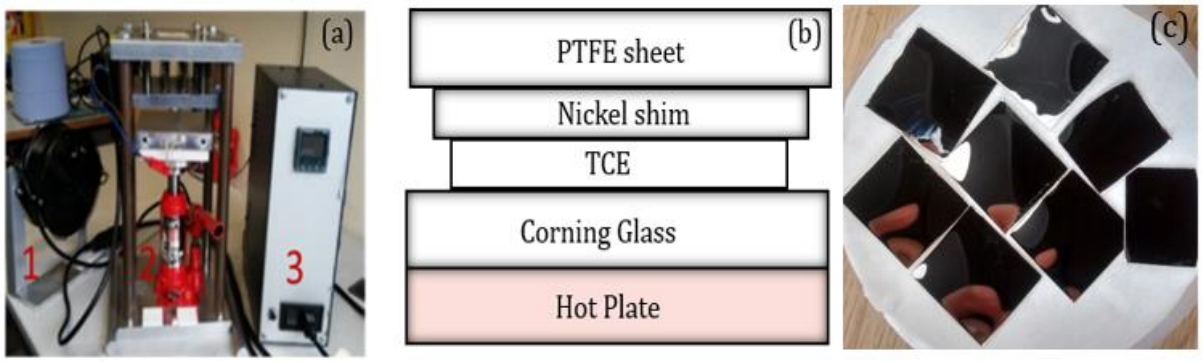


Figure 3.4: (a) In house embossing machine from left (1) Fan for cooling, (2) embosser with having sample holder pneumatic pressing arrangements and (3) temperature controller, (b) Stack of components used for embossing TCEs and (c) image of nickel shims.

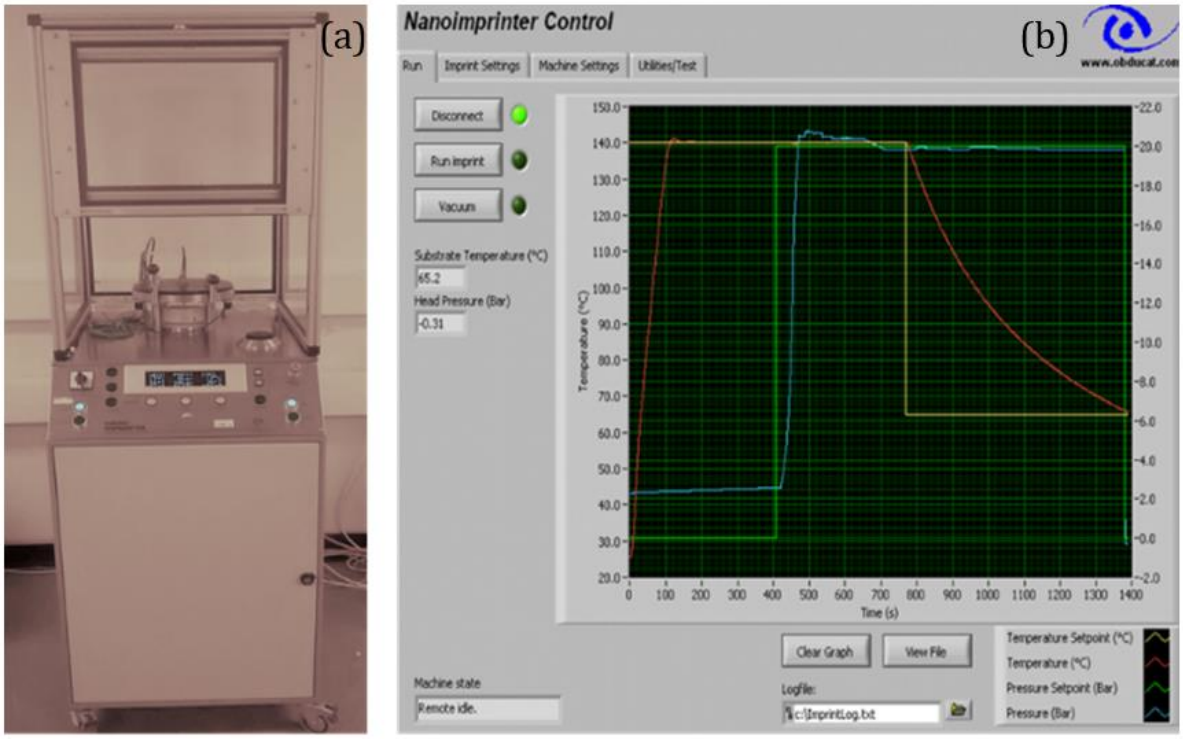


Figure 3.5: (a) Nanoimprinter Obducat 2.5 used for embossing TCEs and (b) Nano imprinter typical profile of controlled embossing process parameters: time, temperature and pressure.

The in-house embossing machine consisted of a fan for cooling down the hot plate, two flat and heated aluminium plates for embossing the samples and a Clarke CBJ2B 2 tonne bottle jack having automatic overload protection was used for creating pressure on plates. The 'stack' needed for the thermal embossing process was optimised and consisted of the following components; (1) TCE coated PEN substrate, a glass square piece, a nickel shim, a PTFE square piece, which were placed on the lower plate of embossing machine.

All components on the hot plate were heated to 140 $^0$C and a 20 minutes wait time (settling time) was applied. The pressure was held for 20 minutes. Finally, the hot plate was cooled to 60 $^0$C using fan air cooling and the pressure was released from the stack. Individual components of the stack were gently separated from each other to avoid any damage to AgNW TCEs. Thermal embossing was used to compress AgNWs on the surface of the substrate. The post-processing leads to improvements in surface roughness, sheet resistance, however, there is no change in transmittance and haze. The thermal-embossing process was conducted using a 2″ nickel shim (shown in Figure 3.4 (c)), supplied by Nanotypos in Greece, formed from a polished silicon wafer to ensure flatness. The anti-sticking layer BGL-GZ-83 was spin coated onto the nickel shims before use in the thermal embossing to avoid sticking of the AgNWs and thermoplastic to the nickel shim during the embossing procedure. The nickel shim was cleaned thoroughly using solvents before use.

Table 3.2: Specifications of in house and Obducat NIL 2.5 embossing systems.

| Specification | In-house system | NIL2.5 |
|---|---|---|
| Max temperature | 200 $^o$C | 250 $^o$C |
| Max pressure | - | 70 Bar |
| Heat up time to 140 $^o$C | 3 min | 2 min |
| Cool down time from 140 $^o$C to 60 $^o$C | 15 min | 10 min |
| Max substrate size | 4 inches | 2.5 inches |
| Loading | Manual | Manual |
| Unloading | Manual | Manual |
| Substrate-cooling capability | Air-cooling | Liquid $N_2$ / Air-cooling |
| Software control | No | Lab-view controlled |

A summary of the two embossing systems is shown in Table 3.2. Sheet resistance, haze and transmittance were measured before and after application of thermal embossing using nano imprint lithography (NIL) system. Moreover, thermal embossing of AgNW TCEs was performed at predetermined process conditions according to $L_9$ OA as discussed in the next Chapter 4.

### 3.2.2 Post Processing using Nitrogen Plasma and Photonic Curing

The nitrogen plasma treatment process was conducted using a Diener second 'Nano' plasma treatment system shown in Figure 3.6 (a) at ambient pressure after 30 seconds of nitrogen purge. Three gases namely, nitrogen, argon and oxygen were used initially for plasma treatment on AgNWs TCEs. There was approximately a 50 percent reduction in

resistance after the plasma treatment of nitrogen as well as argon gas. However, in the case of oxygen plasma treatment, the AgNWs TCEs became non-conductive. Why N2

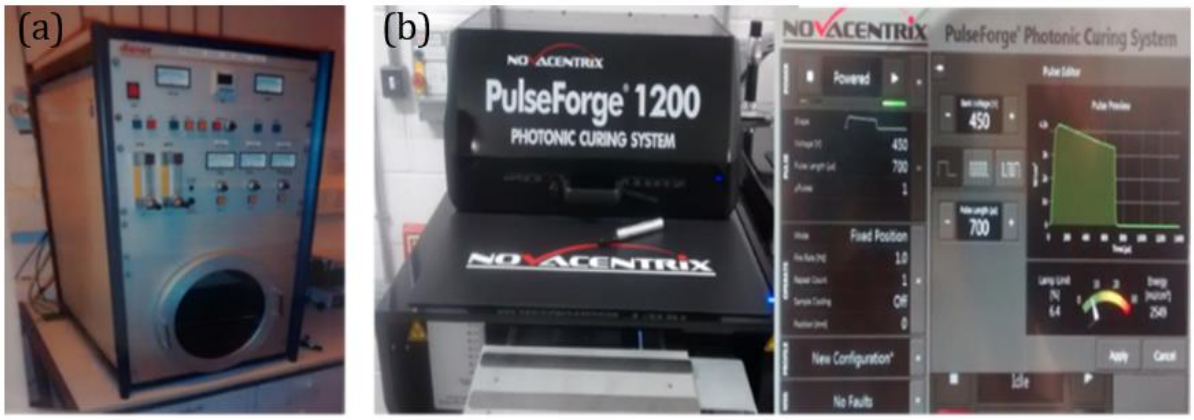


Figure 3.6: (a) Diener second 'Nano' plasma treatment system, (b) Photonic sintering setup and typical profile of photonic curing system.

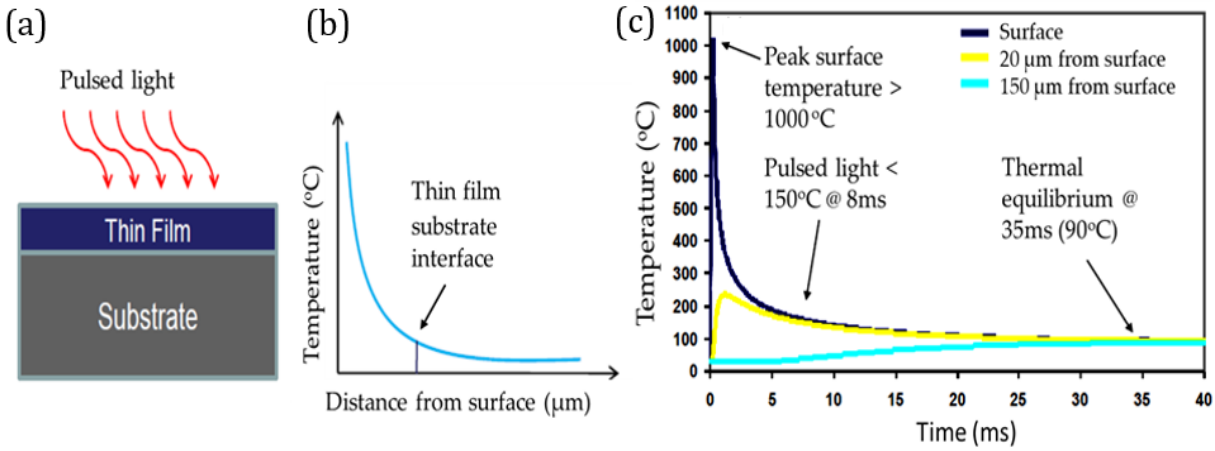


Figure 3.7: (a), (b) Illustration of Photonic curing process, (c) Typical Single pulse (300 μ sec length) thermal profile.

A Novacentrix Pulse Forge 1200 photonic curing system shown in Figure 3.6 (b) was used for sintering only the top surface of AgNW films. Photonic curing was performed using carefully timed and controlled flash lamps to heat only the surface and not the entire thickness of the material. The required exposure time is usually less than 1 millisecond using this setup. It allows high temperature, high performance inks to be used on low temperature, low cost, flexible substrates. Pulse conditions (>10 parameters) are carefully tuned to each material application. Photonic curing can be performed using single or multiple pulses. Figure 3.7 (a) and (b) shows the photonic sintering process. Figure 3.7 (b) demonstrates that as the distance from the surface of a thin film is increased

the temperature of photonic curing decreases (thus affects only the top of the surface). A typical single pulse profile is shown in Figure 3.7 (c)

## 3.3 TFT Fabrication

During this Ph.D. work, various techniques were used for the fabrication of TFTs based on inorganic metal oxide materials. Two methods of active layer deposition were used, one of these is spray pyrolysis and other being a sputtering deposition. Gate dielectrics were produced using anodization and electron beam evaporation. TFTs were also manufactured on dry $SiO_2$ wafers (200µm thick) purchased from Micro Chemicals.

### 3.3.1 Materials used for TFT Preparation

In this work, ZnO and IGZO were used as the semiconductor materials while $SiO_2$ and $Al_2O_3$ were used as the gate insulator. Kapton polyimide (PI) film substrates were used for manufacturing flexible IGZO TFTs, discussed in chapter 6 in detail. Shown in Table 3.3 are the materials used for TFT manufacture.

Table 3.3: Materials selected for TFT manufacture.

| Type | Materials | Stoichiometry | Length (µm) | Purity (%) | Concentration (mg/mL) | Thickness (µm) |
|---|---|---|---|---|---|---|
| TFT active layer | ZnO | - | 20-30 | 99.9 | 20 | 0.02 |
| | IGZO | 1:1:1 | 100-200 | 99.9 | 20 | 0.02 |
| Dielectrics | $Sio_2$ | - | - | - | - | 200 |
| | $Al_2O_3$ | - | - | - | - | 0.02 - 0.1 |
| Solvents | IPA | - | - | 98 | - | - |
| | Ethanol | - | - | 95 | NA | - |
| | Acetone | - | - | 99.9 | NA | - |
| Substrates | Kapton (PI) | - | - | - | - | 25 |
| | ITO on PET | - | - | - | - | 127 |
| | PEN | - | - | - | - | 125 |

### 3.3.2 ZnO Precursor Solution Preparation and Deposition

In the case of ZnO, Zinc acetate dihydrate is dissolved in methanol at a 3% (w/w) concentration for making the precursor solution. Spray coating deposition was carried out using an airbrush nozzle actuated by a micro-controlled servo motor to spray a zinc acetate dihydrate solution onto pre-heated (350 $^0$C) substrates. The substrate heating promotes the solvent evaporation as the solution spray reaches the substrate surface and causes the zinc acetate pyrolysis and subsequent formation of a thin ZnO layer. Spray deposition was carried out at air pressure 0.7 bar and nozzle kept 20 cm distance from the substrate on a hotplate. For optimum film formation, the airbrush nozzle was actuated for 3 short intervals of 5 seconds within three 60s pause intervals. The resulting ZnO films

obtained by this deposition procedure were very uniform, with an average thickness of 20 nm (determined by AFM).

### 3.3.3 Fabrication Steps for Oxide Semiconductor with Solution Process and Radio Frequency (RF) Sputtering

In this section two deposition processes; spray pyrolysis and sputter coating are described. Shown in Figure 3.8, are the TFT fabrication steps as follows: 1) Gate metal deposition, 2) gate insulator deposition, 3) channel deposition, 4) post-deposition annealing, 5) source/drain contact deposition. Heavily doped silicon-$SiO_2$ substrates of area 10×10 $mm^2$ were thoroughly cleaned (to remove contamination on substrate surface) with DI water, acetone and IPA, followed by drying with a jet of dry nitrogen and dehydrated at 100 $^0$C for a minimum of 20 minutes. The substrates are then treated with an oxygen plasma for 5 minutes to eliminate any remaining impurities. ZnO active layer is then deposited on $SiO_2$ substrates using an airbrush spray-pyrolysis system onto the pre-heated substrates.

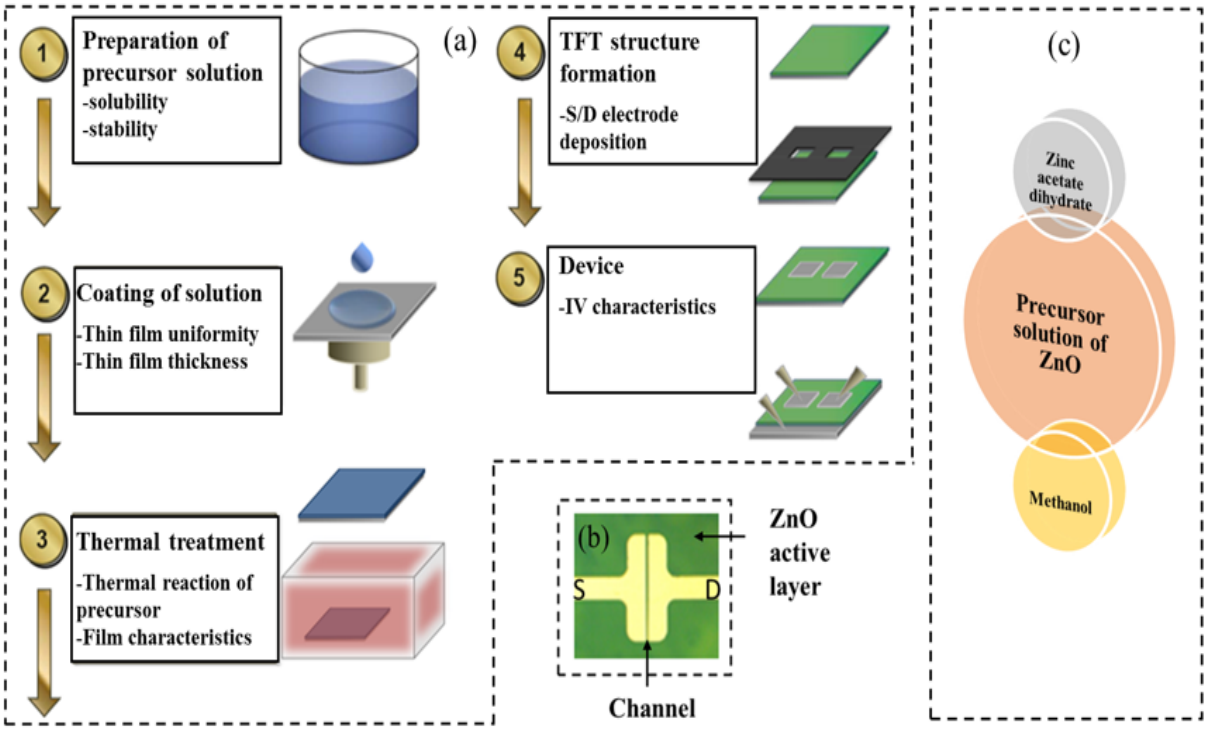


Figure 3.8: (a) Fabrication steps for oxide semiconductor solution process (b) Optical microscope image (top view) of bottom gate ZnO TFT manufactured in this work using solution process (c) ZnO solution formulation.

The sputter coating method was also deployed for the deposition of oxide semiconductors. Sputtering is a physical vapour deposition (PVD) technique and relies on

the bombardment of a target of the source material with high energy inert ions. The ions impact generates a series of collisions between atoms of the target, leading to the ejection of some of these atoms. Sputtered atoms condense on the substrate and coat a thin layer. Argon (Ar) was generally used as the primary process gas. A characteristic feature of sputtering is the glow discharge cloud which appears between the target and substrate as shown in Figure 3.9 (a). RF sputtering can be used with both conductive and insulating targets. The frequency used for RF sputtering used was 13.56 MHz. The process parameters that control grain structure are substrate type/temperature, base pressure, deposition temperature, deposition rate, and process pressure (controls number of collisions). The physical nature of this process allows its use with virtually any existing source material. Shown in Figure 3.9 (b) Image of Leybold UNIVEX 350 sputter coater (left) and E-beam thermal evaporator (right). In this thesis work, RF sputtering was used for ZnO, IGZO active layer deposition and E-beam thermal evaporator was used to deposit $Al_2O_3$ high-k dielectric layer.

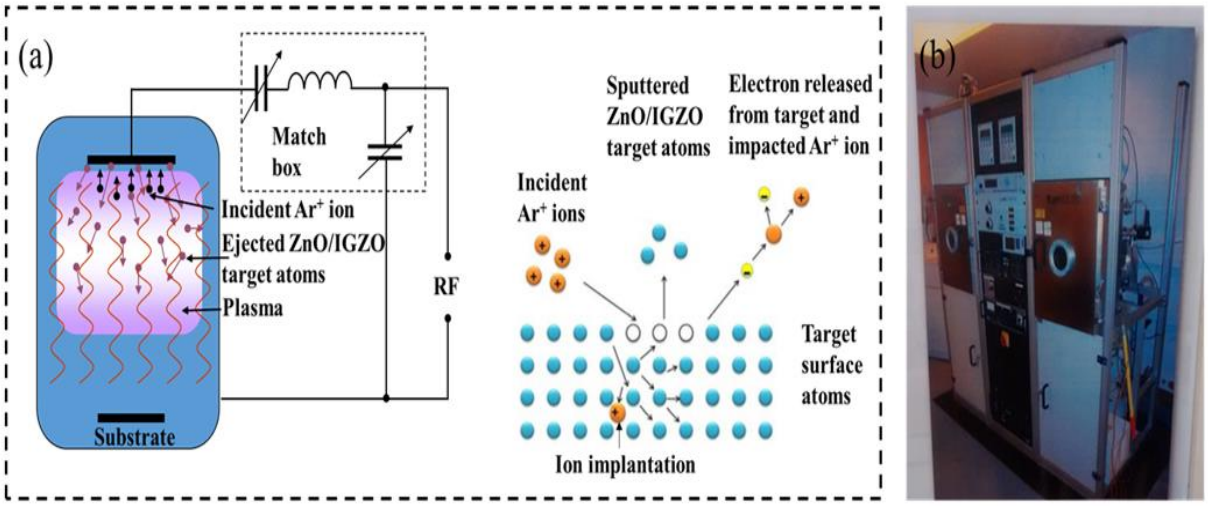


Figure 3.9: (a) RF sputtering mechanism Ionized Ar atoms diffuse from the glow discharge region into the cathode sheath, then are accelerated toward the ZnO/IGZO target via a large electric field. (b) Image of Sputter coater (left) and e-beam thermal evaporator (right).

### 3.3.4 Source Drain Contact Thermal Evaporation

Source, drain and gate contacts were deposited using thermal UNIVEX 350 Leybold thermal evaporator. Thermal evaporation is also a PVD technique commonly used for depositing metals layers like Al and is a much simpler process than sputtering. Sublimation of the source atoms is accomplished by bringing a metal bit to its respective melting point with the application of a large current to a resistive thermal tungsten boat

or filament coil. Shown in Figure 3.10 (a) are the typical prerequisites of a thermal evaporation setup. Figure 3.10 (b) shows the image of the Leybold thermal evaporator. Thermal evaporation was accomplished in a high vacuum ($10^{-6}$ - $10^{-7}$ torr). Atoms evaporated from the bit producing vapour pressure travel on a ballistic trajectory from the molten source material to the substrate surface. A high vacuum is required to minimize collisions of source atoms with background species. It traverses the chamber and hits the 'cold' substrate surface thus desublimates and coats the substrate. For better uniformity of deposited layer low evaporation rate of 1 nm per second was used.

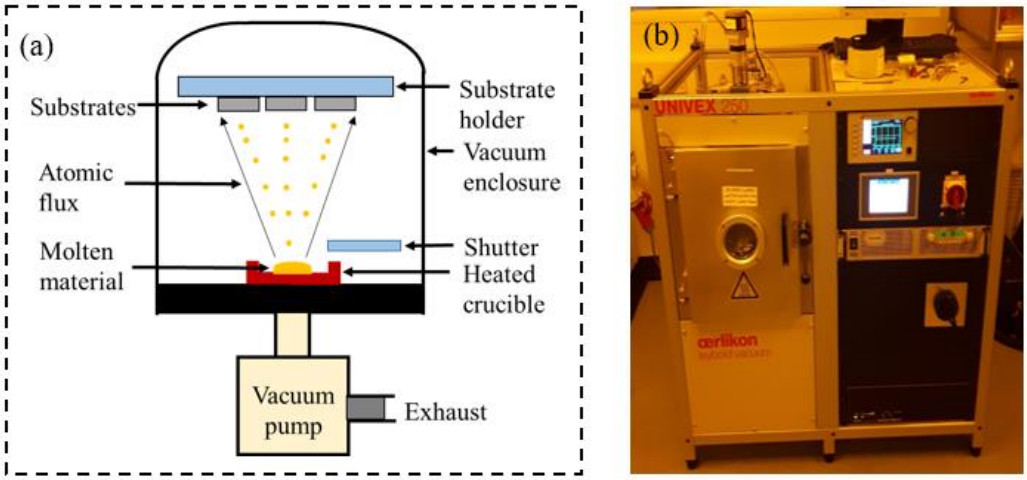


Figure 3.10: (a)Schematic illustration of a thermal evaporation system showing all important parts, (b) Image of Leybold thermal evaporator.

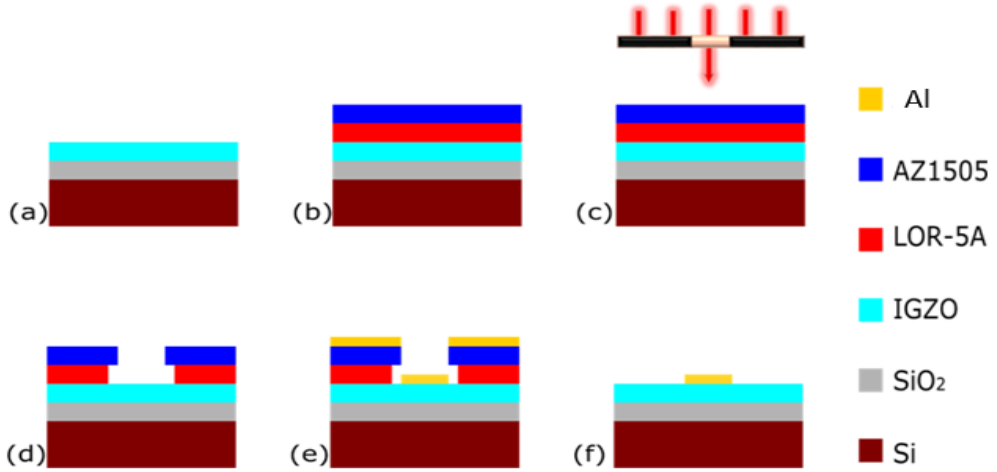


Figure 3.11: Lift-off process defining the metal electrodes. (a) Starting with IGZO layer on $SiO_2$/Si substrates, (b) spin-coating the bi-layer AZ1505 +ve photoresist on top of LOR-5A resist, (c) UV exposure through mask, (d) developing the bi-layer in AZ726 MIF, (e) thermally evaporating Al with Cr adhesion layer, and (f) lift-off the bi-layer to define the metal electrodes.

### 3.3.5 Lift-Off Process

In addition to shadow masks, small channel (5-100μm) TFTs were also fabricated on $SiO_2$ substrates using the photolithography process. The bi-layer lift-off process was used to define the electrodes, as depicted in Figure 3.11. First 500 nm LOR-5A resist then 500nm AZ1505 positive-tone photoresist films were spun-coated over the IGZO layer on top of the $SiO_2$/Si substrates. The bi-layer was then UV-exposed with ~112 mW/cm$^2$ to define the contact electrodes. The pattern was transferred to the bi-layer using the commercial AZ726 MIF developer. 100 nm of Al was thermally evaporated on the patterned photoresist using a Leybold 250 system, with 7nm of Cr as an adhesion layer. Finally, the bi-layer was removed in 1165 photoresist stripper using a sonication bath to create the Al/Cr contact electrodes.

## 3.4 Characterization of TCEs and TFTs

In this section, all electrical and optical characterization methods used for TFTs and AgNW TCEs are explained.

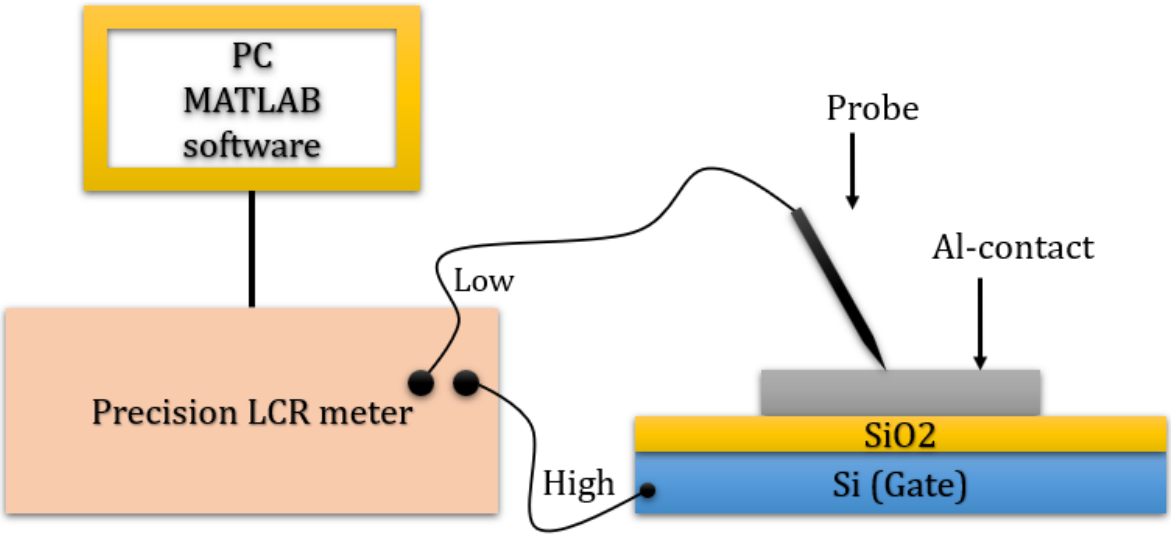


Figure 3.12: (a) Schematic diagram of the MIM CV/Cf and capacitance characterization setup. Test probes were connected to BNC connector to allow connection to the precision LCR meter.

### 3.4.1 TFT CV/Cf and MIM Capacitance Characterization

All metal insulator metal (MIM) CV/Cf and capacitance measurements were performed using Hewlett Packard 4284A 20Hz-1MHz precision LCR meter and Solartron SI 1255 HF frequency response analyser source measure unit connected to three probe tips mounted

on micromanipulators. All measurements and data acquisition were automated using MATLAB software. The schematic diagram of MIM CV/Cf and capacitance characterization setup is shown in Figure 3.12.

### 3.4.2 UV Saturation Experiment Setup

All UV sensing saturation experiment (detailed in chapter 5) measurements of ZnO TFTs as photo sensor were performed using Agilent B2900A precision source measured unit connected to three probe tips mounted on micromanipulators. All measurements and data acquisition were automated using B2900A Quick IV measurement software and Keithley 237 was connected to source UV LED. The schematic diagram of UV saturation experiment is shown in Figure 3.13.

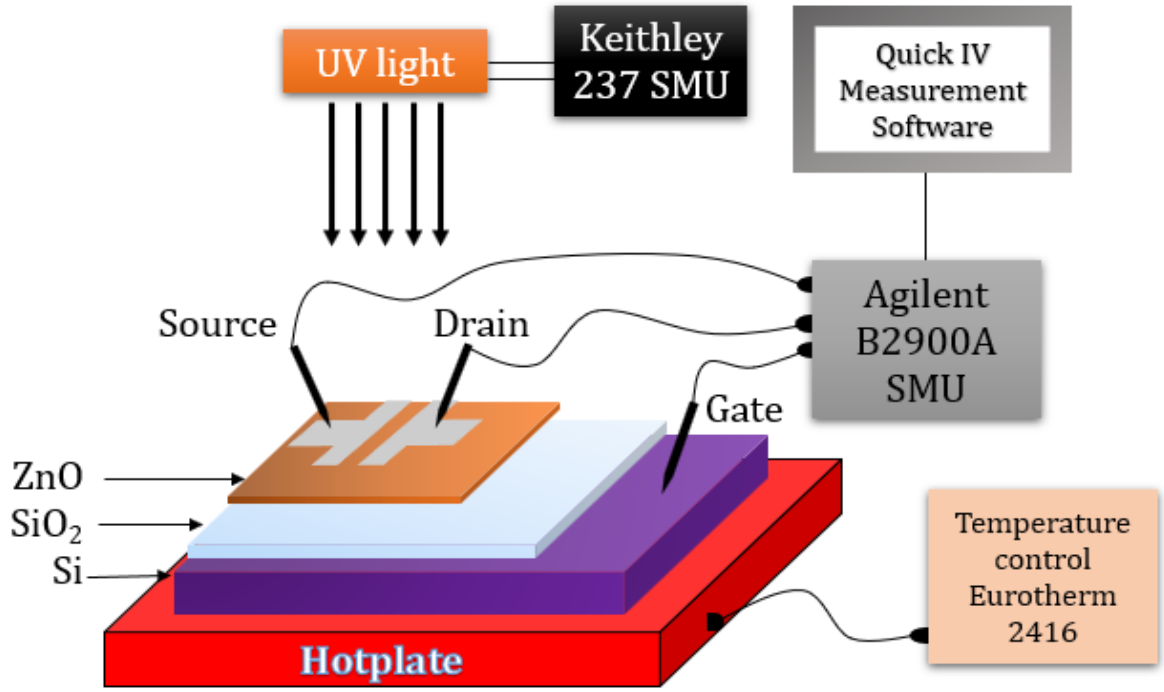


Figure 3.13: (a) Schematic diagram of UV saturation experiment characterization setup. Test probes were connected to BNC connector to allow connection to the Agilent B2900A precision SMU and Keithley 237 was connected to source UV LED.

### 3.4.3 TFT Current Voltage (IV) Characterization

All TFT IV measurements were performed using Agilent B2900A or Keithley 4200 precision source measure unit connected to three probe tips mounted on micromanipulators. All measurements and data acquisition were automated using B2900A Quick IV measurement software or TSP™ Express software through a LAN

connection. The schematic diagram of the transistor characterization setup is shown in Figure 3.14.

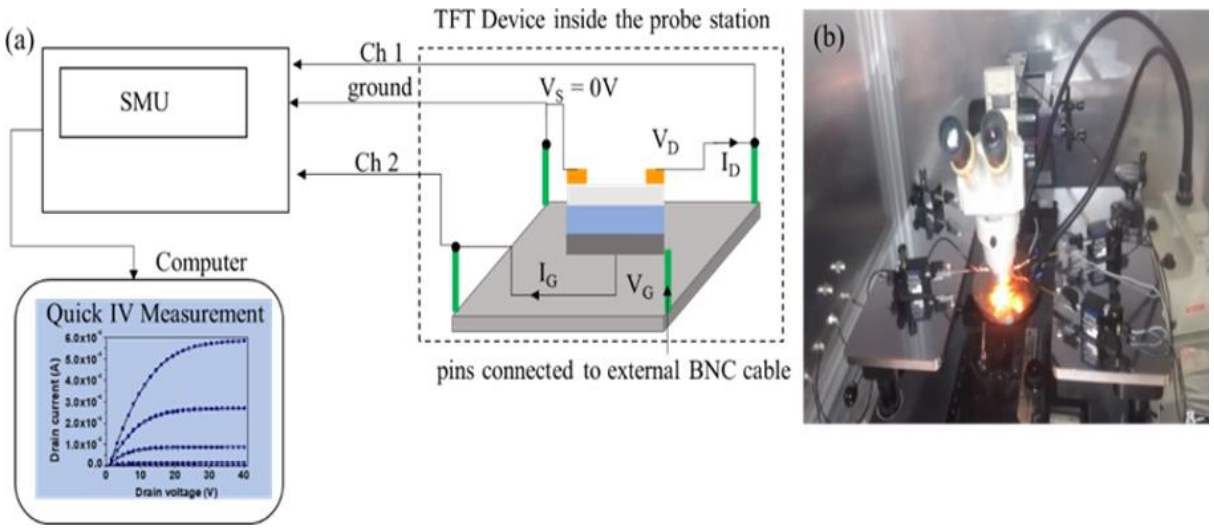


Figure 3.14: (a) Schematic diagram of the transistor characterization setup. Test pins were connected to BNC connector to allow connection to the SMU unit, (b) Image of probe station used for TFTs IV characterization.

### 3.4.4 IV Characterization and Accelerated Lifetime Testing (ALT) of AgNW TCEs

Shown in Figure 3.15 are the experimental setups for accelerated lifetime testing of AgNW TCEs, (a) environmental chamber (b) circuit board for ALT showing AgNW TCEs connected to crocodile clips, power supply, and Bo test SMU.

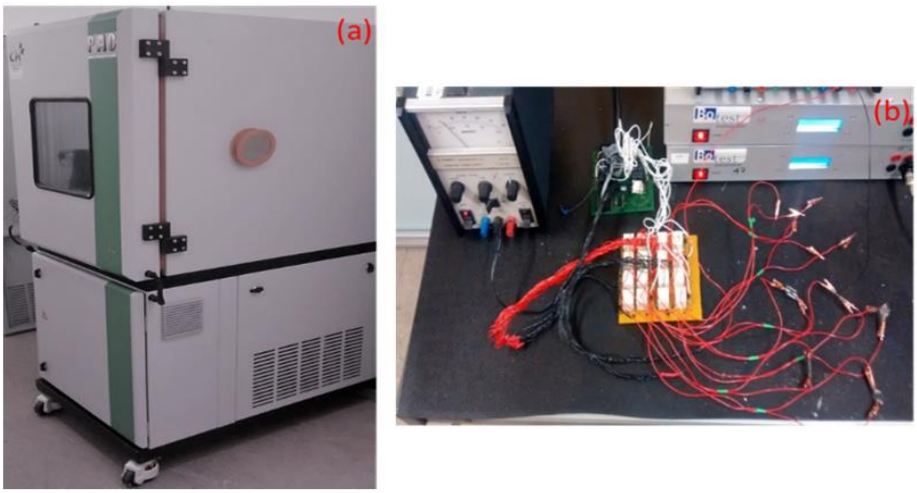


Figure 3.15: Experimental setup for accelerated lifetime testing of AgNW TCEs. (a) Environmental chamber (b) Circuit board for ALT showing AgNWs samples connected to crocodile clips, power supply, and Bo test SMU.

To evaluate the long-term stability of the post processing upon the AgNWs stability, a bespoke accelerated life testing (ALT) system was constructed. This enabled high current biasing of the AgNW electrodes and repeated resistance calculations every 30 minutes, during which the bias momentarily switched off (~5 seconds). To accelerate the degradation, samples were placed in an environmental chamber (Weiss UK ltd). Simultaneous high bias and temperature degradations were conducted at varying stress levels so that the stability could be assessed under 'normal operation conditions', which was defined as $I_{Bias}$ = 20 mA/cm$^2$ and an ambient temperature of 20 $^0$C, which is typical settings for an OLED or OPV.

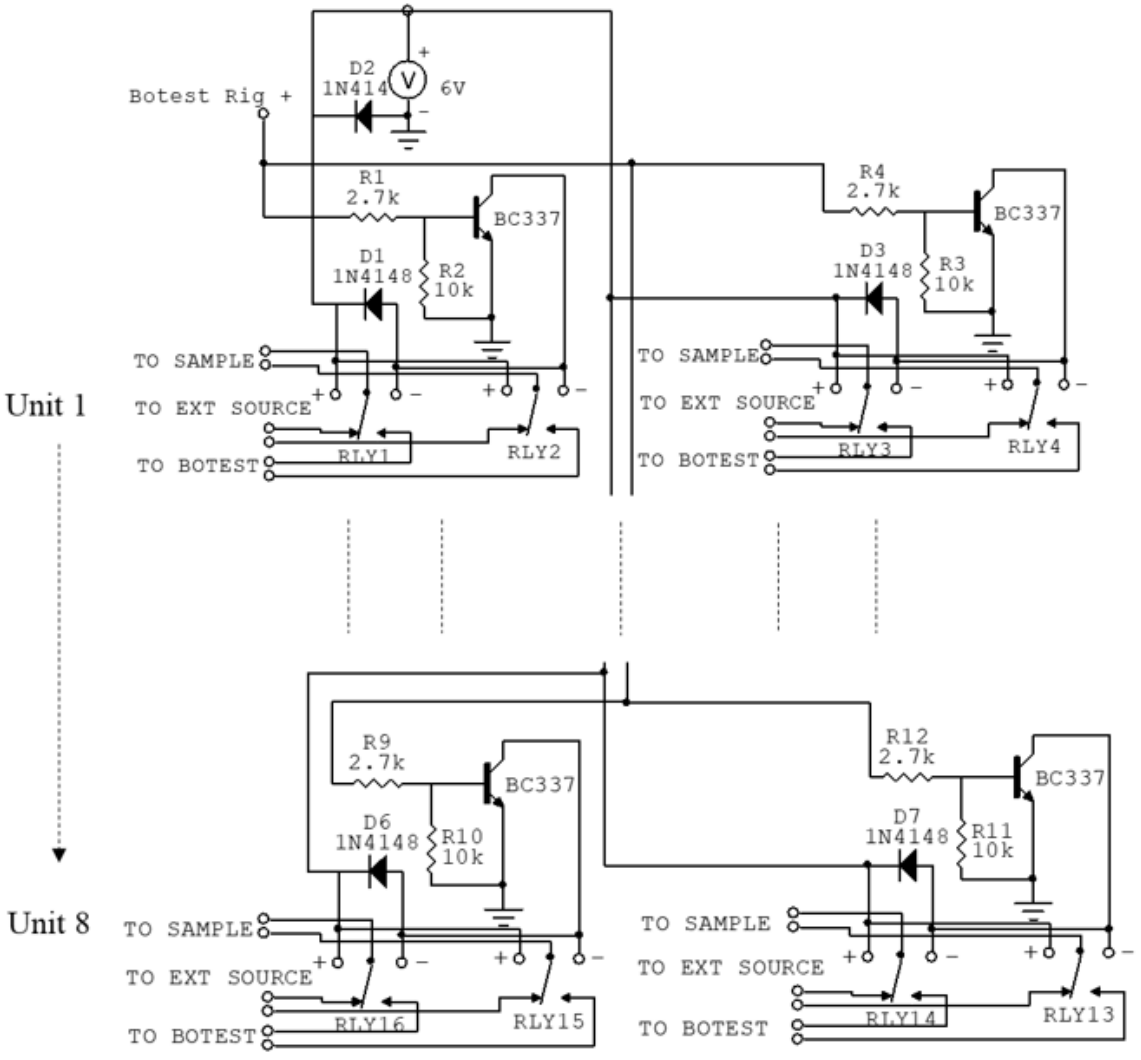


Figure 3.16: Circuit design for accelerated lifetime testing AgNW TCEs, first and last units are shown for simplicity because all units are the same.

The circuit of the developed ALT is shown in Figure 3.16 was designed and implemented on the printed circuit board. The main electronic components used were relays, bipolar junction transistors (as switching transistors) and diodes (as current

limiters). For simplicity only first and last units (out of eight) are shown because each unit is a replica of other units. The Botest software was controlled by an auto clicker, which starts a new measurement cycle every 30 seconds for eight TCEs connected to SMU via a multiplexer. The measurement cycle runs a full IV sweep on each TCE connected to the multiplexers in turn.

### 3.4.5 Setup for Sheet Resistance Measurement of AgNW TCEs

Sheet resistance measurements were conducted using the four-probe setup as shown in Figure 3.17 (a). This system is a combination of the multi height probe stands with the RM3000 Test Unit, with the added feature of a removable X-Y micro position table. Figure 3.17 (b) shows a schematic of 4-point probe configuration. Typical probe spacing s is approximately 1 mm. Each probe tip is supported by springs on the other end to minimize sample damage during probing. A high impedance current source is used to supply current through the outer two probes and a voltmeter is used to measure the voltage across the inner two probes (See Figure 3.17 (b)) to determine the thin layer resistivity. For a very thin layer (thickness t << s), the $R_{sh}$ is given by equation 2.1 (Chapter 2).

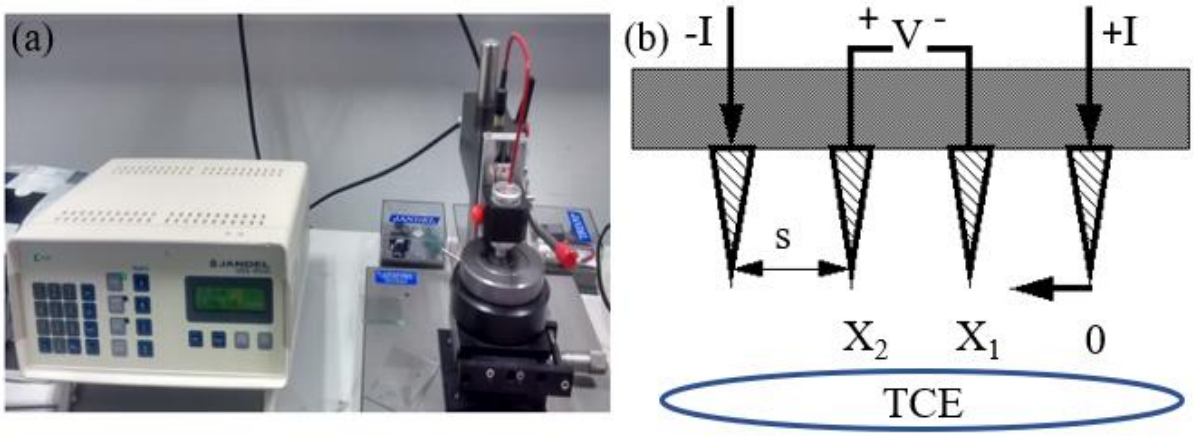


Figure 3.17: (a) Jandel multipurpose four-point system and (b) Schematic of 4-point probe configuration.

### 3.4.6 Atomic Force Microscopy

Atomic force microscopy (AFM) was used to measure film thicknesses by scanning across a scratch made using the sharp edge of Knife in the layer. AFM was also used to measure average, RMS and peak to valley surface roughness of device layers. These measurements were performed using a Digital Instruments Nanoman V running in tapping mode.

### 3.4.7 Scanning Electron Microscopy

Scanning electron microscopy (SEM) was used to obtain high resolution surface and cross section imaging of fabricated TCEs layers. Scanning electron microscope (SEM) images were obtained using a Leo 1455VP SEM operating at 30 kV with 10 pA beam current at a typical magnification of ×10000.

### 3.4.8 Optical Characterization

Figure 3.18 (a) shows the Ocean Optics HR4000 UV-Vis-NIR spectrometer and (b) Shimadzu UV-3600 spectrophotometer used in this work. UV-Vis spectrophotometry was used in the absorption peak measurements of AgNW films, ZnO, IGZO active layer (Shimadzu UV-3600 spectrophotometer). The Shimadzu UV-3600 spectrophotometer has three detectors with a resolution of 0.1 nm and has a wavelength range of 185-3300nm. The spectrometer used for in-situ absorption measurements was an HR4000 UV-Vis-NIR supplied from Ocean Optics Inc. The unit has a wavelength range of 350-1100nm. This device requires the reference to be taken before the absorption measurement.

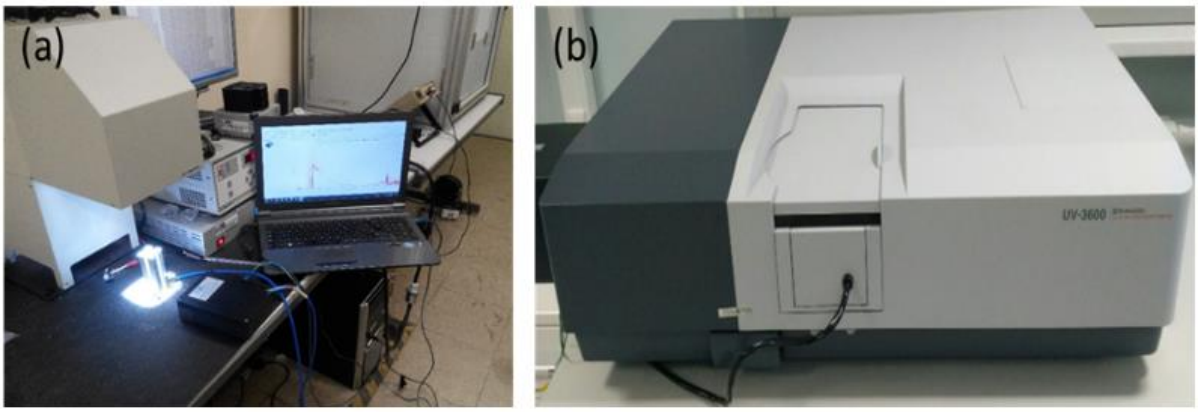


Figure 3.18: (a) Ocean Optics HR4000 UV-Vis-NIR spectrometer and (b) Shimadzu UV-3600 spectrophotometer.

### 3.4.9 White light interferometry (WLI) and haze measurements

The surface roughness is an important factor for the optimum performance of thin-film electronic devices such as TFTs, OLEDs, and OPVs. To characterise the surface roughness of thin films, white light interferometry was used. Shown in Figure 3.19 is the experimental setup for surface roughness measurement using Micro XAM. Surface roughness was estimated by white light interferometry (WLI) using a Micro XAM surface mapping microscope (KLA Tencor, USA).

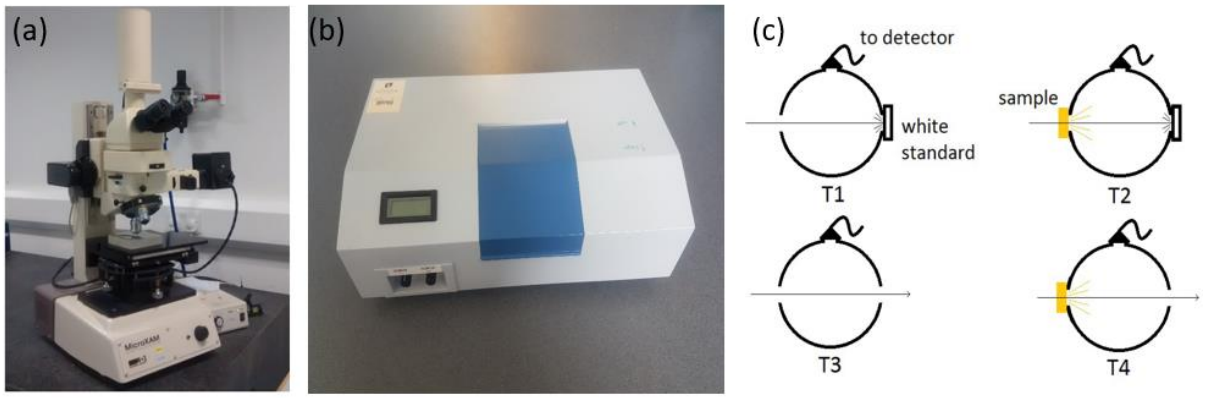


Figure 3.19: (a) Experimental setup for surface roughness measurement using Micro XAM and (b) Image of haze meter used in this work and (c) Four scan configurations for haze measurement [194].

A haze meter was used to measure the amount of light that is scattered when passing through AgNW TCE. Shown in figure 3.19 (b) is the image of the haze meter used in this work. The haze found to be 0.3% for AgNW TCE with 24.1 Ω/sq sheet resistance.

Haze measurement involves four scans using the configurations shown in Figure 3.19 (c). In configuration T1 exit from an integrating sphere is closed with white standard, while in configuration T2 additionally a sample is placed at the entrance to the sphere. In configuration T3 light can pass through the sphere undisturbed and in configuration T4 it is scattered by the sample at the entrance to the sphere.

The integrate scans used in two spectral ranges: all visible range (380-780nm) and the range where samples do not absorb (600-780nm). The integrated area under each spectrum was used in equation 3.4 [192]:

$$Haze = \left[\frac{T4}{T2} - \frac{T3}{T1}\right] * 100\% \qquad \text{Eq. 3.4}$$

### 3.4.10 Bias Stress Characterization

The positive gate bias stress (PGBS) characterization procedure described here is relevant for the studies in Chapter 6. A typical flow diagram for the bias stress experiments is shown in Figure 3.18(a).

First, the initial transfer characteristic of IGZO TFT was measured. Then the device was subjected to various bias stress conditions for 11000s stress time. The bias stress was frequently interrupted to measure the output and transfer characteristics in saturation ($V_D$ = 40 V) regime from which the transistor parameters were extracted.

Figure 3.20 (b) presents a typical transfer curve, plotted on linear and semi-log scales, both in the initial state and after bias stress. The shift of threshold voltage, $\Delta V_T$, was determined as [$V_T$ (t) – $V_T$ (0)], where t=0 corresponds to pre-stress values.

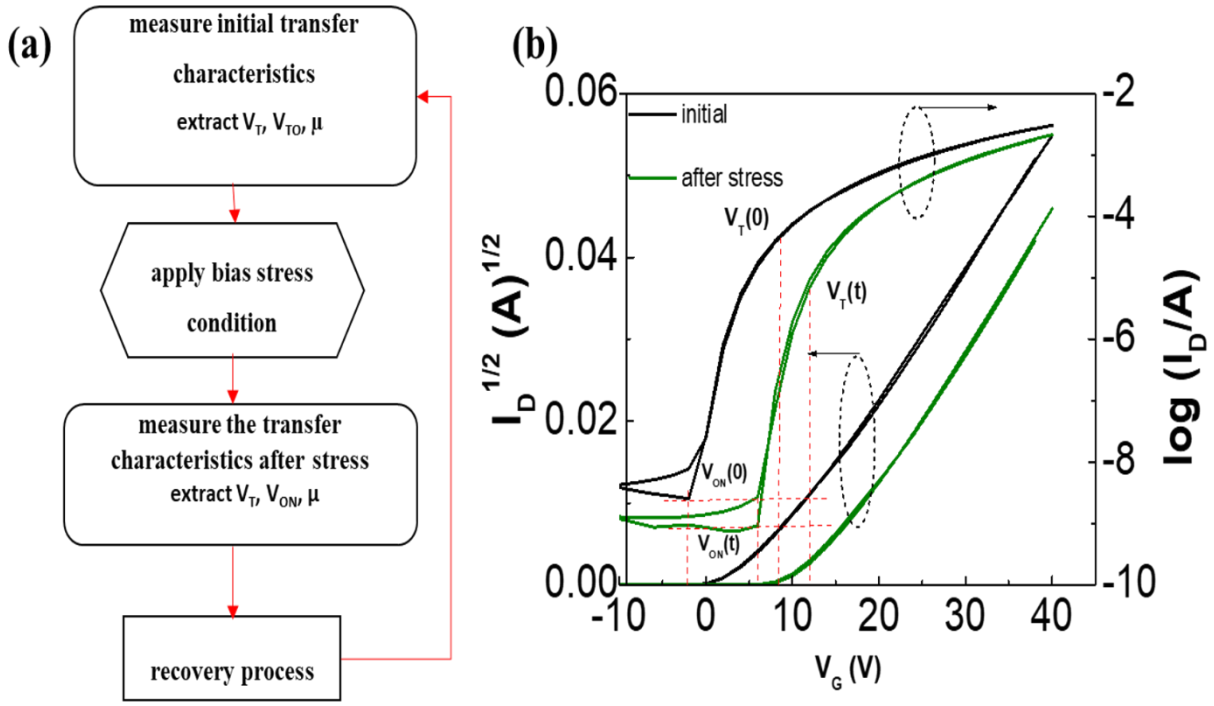


Figure 3.20: (a) Flow chart of a typical bias stress experiment. (b) Illustration of threshold voltage shift, $\Delta V_T$, calculated as [$V_T$ (t) – $V_T$ (0)], where t=0 corresponds to pre-stress values.

After completing a positive bias stress test, devices were subjected to a recovery procedure. The devices were left short-circuited in the dark for a 21minutes or under white light for a few seconds (180s) until $V_T$ recovered to its original value. Due to fast recovery under white light, recovery of all devices was performed using white light.

## 3.5 Extraction of the Density of Trap State Using the Grünewald Model

The extraction of Density of States (DoS), from the transfer characteristic of a thin film transistor, was performed using the Grünewald *et al.* model [195]. This was accomplished by first developing the relationship between the gate dependent insulator/semiconductor interface potential, $V_0$, and the effective forward voltage, $V_F = (V_G - V_{ON})$. This is achieved by numerically solving the equation 3.5.

$$exp(\beta V_0) + \beta V_0 - 1 = \beta \frac{C_i\, l}{\varepsilon_s\, \varepsilon_0 I_0} \left[V_F\, I(V_F) - \int_0^{V_F} I(V_F)\, dV_F\right] \qquad \text{Eq. 3.5}$$

where, *l* is the thickness of the semiconductor, β = q/kT, k the Boltzmann, T the absolute temperature, q the charge of the carrier, $\varepsilon_S$ the relative permittivity of the semiconductor and $\varepsilon_0$ the permittivity of free space. $I_0$ is the off-current at $V_{ON}$. Following further manipulation, the total electron density $n(V_0)$ and the density of states N(E) may be obtained from equation 3.6

$$n(V_0) = \frac{{C_i}^2}{\varepsilon_s\, \varepsilon_0 q^2}\, V_F\, [\frac{dV_0}{dV_F}]^{-1} \qquad \text{Eq. 3.6}$$

Finally, the density of states, N(E) from equation 3.7,

$$N(E) \approx \frac{dn(V_0)}{dV_0} \qquad \text{Eq. 3.7}$$

# Chapter 4. Application of Thermal Embossing to Enhance the Properties of AgNW TCEs

This chapter reports a low-cost method for manufacturing silver nanowire (AgNW) transparent conductive electrodes (TCEs). The initial optimisation and production processes are explained at the start of section 4.1. The report of AgNWs TCEs shows remarkable electrical performance, surface planarity, and environmental stability. This process relies on three sequential steps, which are roll-to-roll (R2R) compatible; thermal embossing, infrared sintering, and plasma treatment. This process leads to the demonstration of a conductive film with a sheet resistance of 2.5 Ω $sq^{-1}$ and high transmittance, thus demonstrating the highest reported Figure-of-merit in AgNWs to date (FoM = 933). A further benefit of the process is that the surface roughness is substantially reduced compared to traditional AgNW TCEs processing techniques. Finally, consideration of the long-term stability is given by developing an accelerated life test process that simultaneously stresses the applied bias and high temperature. Regression line fitting shows that approximately 150-times improvement in the stability is achieved at 'normal operational conditions' when compared to traditionally deposited AgNW films. X-ray photoelectron spectroscopy (XPS) is used to understand the root cause of the improvement in long-term stability, which is related to reduced chemical changes in the AgNWs.

## 4.1 Initial AgNW TCE Fabrication and Optimisation

Initial AgNW TCEs manufacturing work and optimisation began with spray coating AgNW dispersions in ethanol with different volumes and different concentrations on flexible PEN substrates. To obtain high transmittance with low sheet resistance a number of input factors like AgNW dispersion flow rate, the angle between nozzle and substrate and distance of spray nozzle were varied as shown in chapter 3 Figure 3.2.

Figure 4.2 shows (a) transmittance as a function of wavelength for two separate AgNWs (D = 60nm) on PEN electrodes, (b) transmittance as a function of wavelength for two separate AgNWs (D =100-200nm) electrodes, (c) transmittance at 550nm as a function of sheet resistance for different diameter AgNWs types (d) sheet resistance as a function of amount of AgNWs deposited by spray coating on PEN, (e) transmittance as a function of amount of AgNWs deposited by spray coating on PEN and (f) % haze of TCEs

amount of AgNWs deposited by spray coating. It can be observed that both transmittance as well as sheet resistance decreases, and haze increases with an increase in volume or silver amount. This indicates that a trade-off between sheet resistance and transmittance is necessary, which is determined by the final application of AgNW TCEs. The data is supported by earlier studies in AgNWs, but Figure 4.2(c) is remarkable as the transparency of wider diameter AgNWs remains high even for lower sheet resistance. Where possible, it was decided to use these AgNWs in the work.

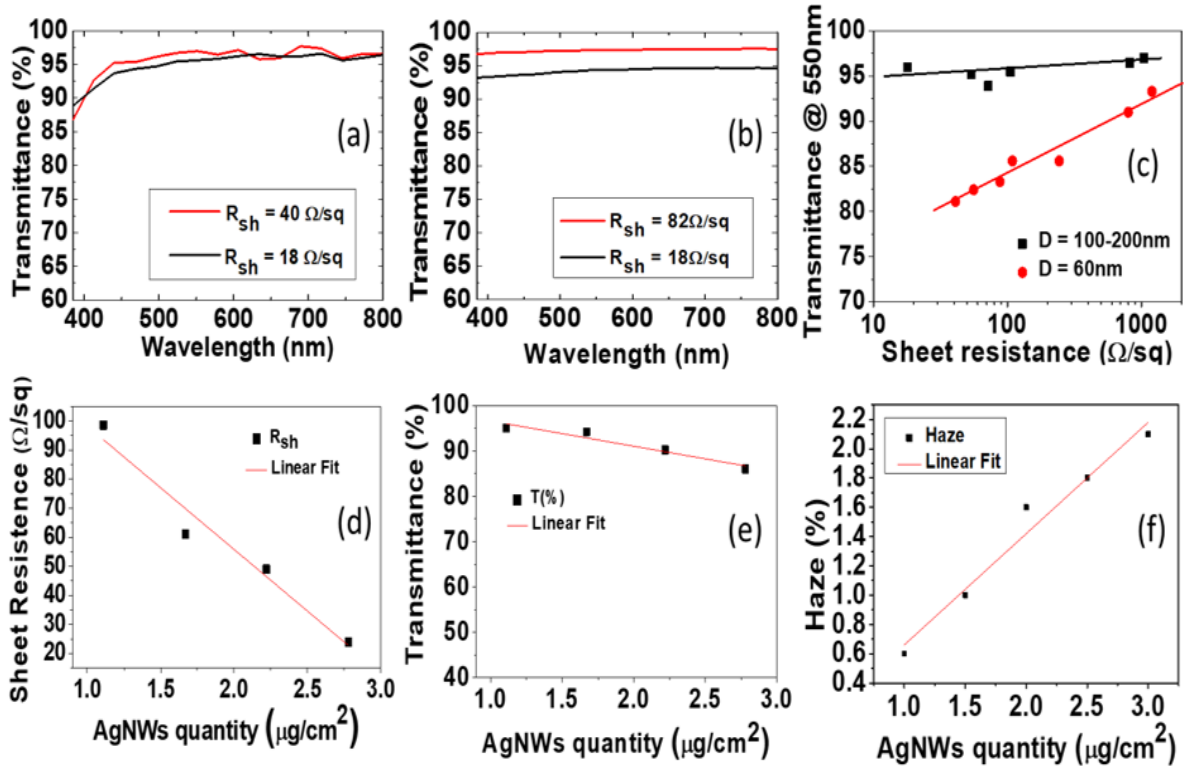


Figure 4.1: (a) Transmittance as a function of wavelength for two separate AgNWs (D = 60nm) on PEN electrodes, (b) Transmittance as a function of wavelength for two separate AgNWs (D =100-200nm) electrodes, (c) Transmittance at 550nm as a function of sheet resistance for different diameter AgNWs types (d) Sheet resistance as a function of amount of AgNWs deposited by spray coating on PEN, (e) Transmittance as a function of amount of AgNWs deposited by spray coating on PEN and (f) % haze of TCEs amount of AgNWs deposited by spray coating.

## 4.2 Effect of Thermal Embossing on AgNW TCEs Properties

The effect of thermal embossing on electrical, optical and surface properties of TCEs was studied. Table 4.1 shows the results for sheet resistance, transmittance, haze, and surface roughness parameters obtained after measuring AgNW TCEs before and after application of thermal embossing. The percentage decrease in sheet resistance ($R_{sh}$) average

roughness ($R_a$), R.M.S roughness ($S_q$) and peak to valley roughness ($P_v$) were calculated. Average (Ave) and standard deviation (s.d) of various performance parameters for ten samples are shown in Table 4.1. Standard deviation is a number used to express how measurements for a group are spread out from the average, or estimated value. A low standard deviation means that most of the numbers are very close to the expected value. The standard deviation should be as low as possible.

Table 4.1: Average (Ave) and standard deviation (s.d) of Sheet resistance, transmittance and surface roughness parameters before and after embossing.

| Statistics | $R_{sh}$ before Ω-sq | $R_{sh}$ after Ω-sq | T (% ) | H (%) | $R_a$ (nm) | $R_a$ after (nm) | $P_v$ (nm) | $P_v$ after (nm) | $R_q$ (nm) | $R_q$ after (nm) | % age decrease in $R_{sh}$ | % age decrease in $R_a$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ave | 39.38 | 22.48 | 87.12 | 0.4 | 14.68 | 8.03 | 163.49 | 68.32 | 18.59 | 9.79 | 42.59 | 44.70 |
| S.d. | 5.11 | 2.90 | 1.08 | 0.13 | 2.18 | 0.86 | 58.73 | 10.46 | 3.04 | 1.52 | 6.32 | 6.49 |

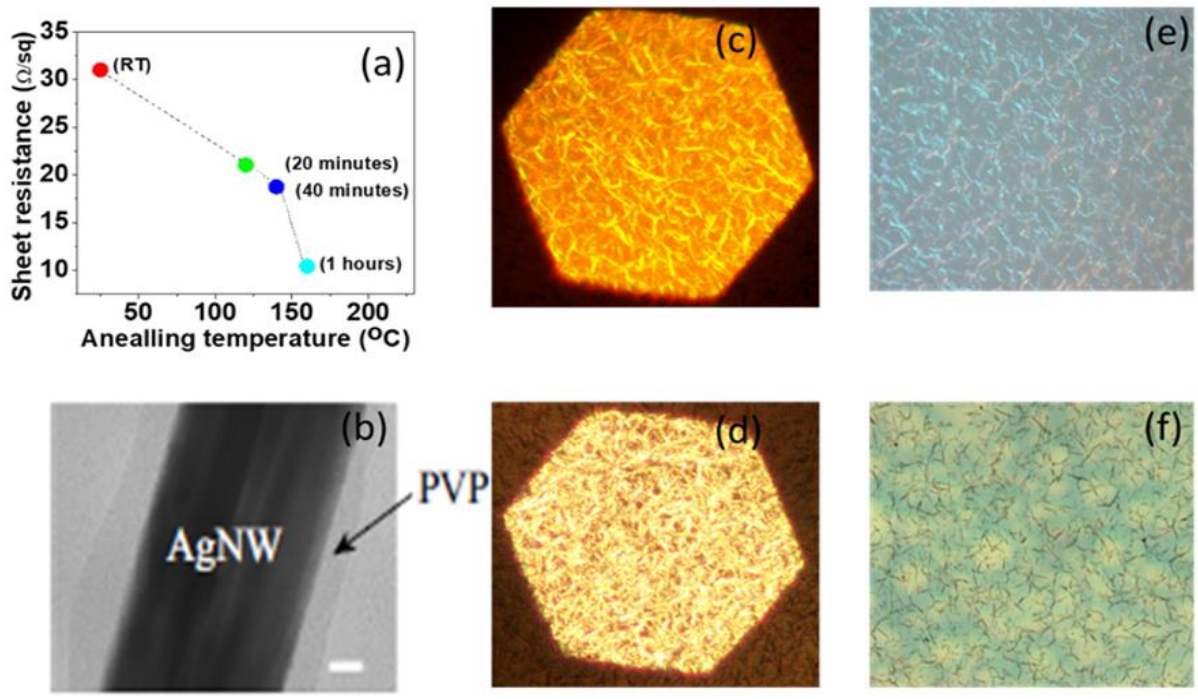


Figure 4.2: (a) Sheet resistance as a function of annealing temperature measured at different annealing times, (b) SEM image of AgNW showing polyvinylpyrrolidone (PVP) capping, (c) optical microscopic image (50 × magnification) of non-embossed AgNW film on PEN (d) optical microscopic image (50 × magnification) of embossed AgNW film on PEN, (e) optical microscopic image (20 × magnification) of non-embossed AgNW film on PEN and (f) optical microscopic image (20 × magnification) of embossed AgNW film on PEN.

It is worth mentioning that there is an average 42.59% reduction in sheet resistance and 44.70% reduction in the roughness average $R_a$ after the thermal embossing step. Similarly, there is a reduction in other surface parameters, $P_V$ and $R_q$ as shown in Table 4.1. In AgNW TCEs the junction of the AgNWs is the source of high resistance and residual surfactant polyvinylpyrrolidone (PVP) capping can increase the sheet resistance of the AgNWs at these junctions. Shown in Figure 4.2 (a) is the reduction in sheet resistance as a function of annealing temperature measured at different annealing times. The reduction in sheet resistance on the application of heating and thermal embossing is probably due to the thinning down PVP layer shown in Figure 4.2 (b).

## 4.3 Taguchi Orthogonal Array Optimisation before and after Thermal Embossing Process

Pressure, time and temperature of the embossing step were all varied, and the process was optimised using the Taguchi Parameter Design method. All embossing operations were conducted under ambient conditions rather than under vacuum. Sheet resistance, haze, and transmittance were measured before and after the application of thermal embossing using nano imprint lithography (NIL) system.

A Design of experiment (DOE) software tool was used to assist and optimise the thermal embossing process. A Taguchi $L_9$ OA discussed in section 2.10.1 was chosen with 3 factors (ABC) and three level design was selected for estimating the effect of different factors; A=Pressure of embossing (5 bar, 15 bar, 20 bar ), B=Time of embossing (30 seconds, 2 min, 10 min), C=Temperature of embossing ( 60 $^0$C, 90 $^0$C, 120 $^0$C) on the sheet resistance of electrodes. AgNW TCEs were embossed at different conditions shown in Table 4.2 and 9 experimental runs. After performing all experimental runs sheet resistance and transmittance were measured. The sheet resistance of TCEs was changed, however no change in transmittance was observed, so this is not reported. The Taguchi OA Factorial settings and properties were divided based upon early trials and literature values and are shown in Table 4.2.

Table 4.2: Taguchi OA Factorial settings and properties of embossing factors.

| Factors | Name | Units | Type | Number of Levels | OA Column Index | Level 1 (Low) | Level 2 | Level 3 (High) |
|---|---|---|---|---|---|---|---|---|
| P | Pressure | bar | Quantitative | 3 | 1 | 5 | 15 | 20 |
| T | Temperature | $^0$C | Quantitative | 3 | 2 | 60 | 90 | 120 |
| t | Time | min | Quantitative | 3 | 3 | 0.5 | 2 | 10 |

The response, defined as the percentage change in sheet resistance ($R_{sh}$), was analysed using DOE software tool for the varying test runs. The main effect plots are shown in Figure 4.3 (a), (b), (c) and (d) the term effect plot extracted from DOE analysis. In the DOE, the main effect is the effect of an independent variable (input factors) on a dependent variable (output factors) averaging across the levels of any other independent variables.

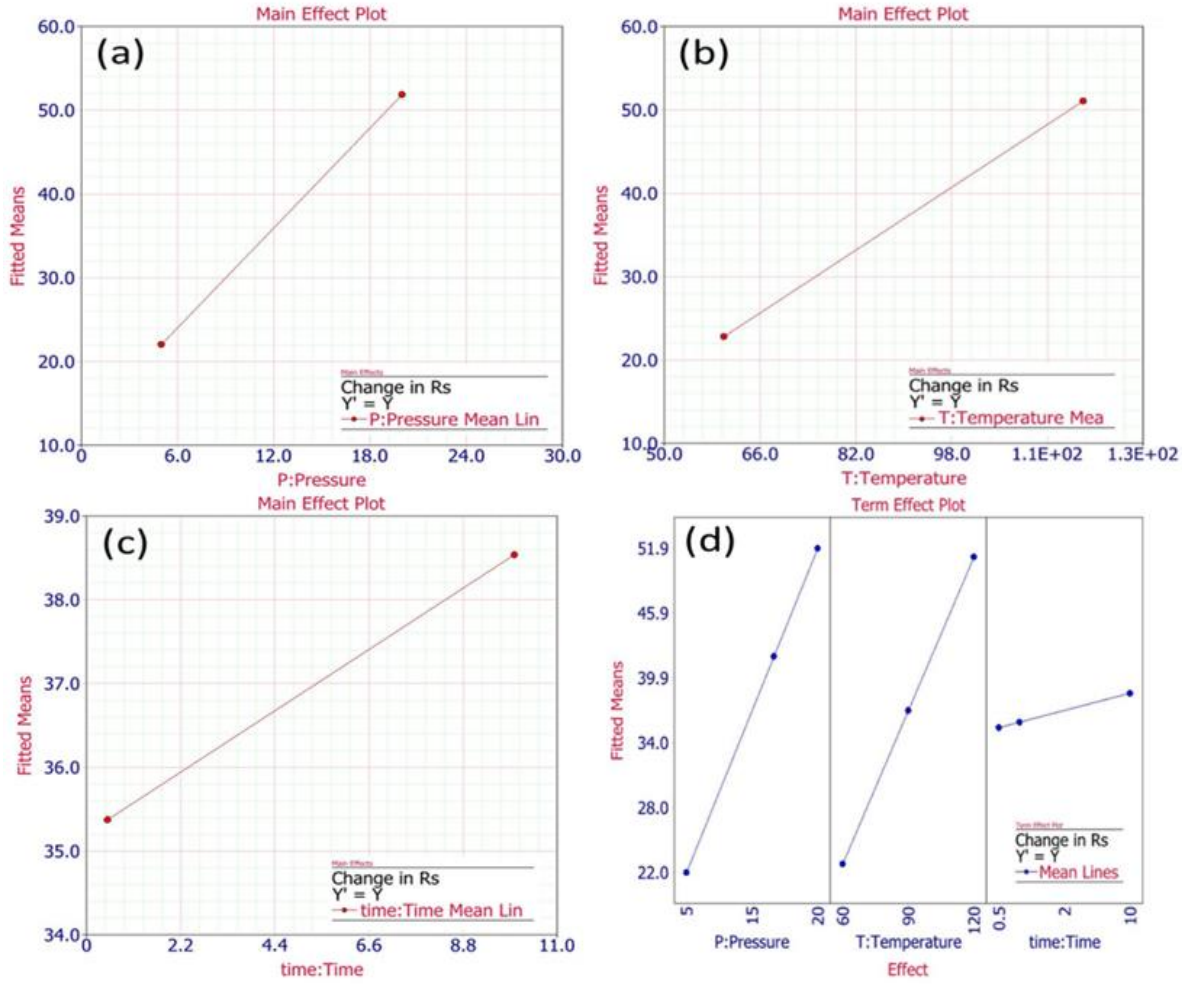


Figure 4.3: Main effect plots(a) change in sheet resistance as a function of embossing pressure variation, (b) change in sheet resistance as a function of embossing temperature variation and (c) change in sheet resistance as a function of embossing time variation (d) term effect plot for change in sheet resistance as a function of embossing pressure, temperature and time.

Shown in Figure 4.4 (a) is the Pareto chart based on linear regression analysis of the main effects and (b) the Pareto chart for main effects and 2-way interactions calculated by considering the change in sheet resistance. The Pareto chart shows the standardized effect of each term (i.e. factor or combination of factors) for a particular

response. The thick blue line shows the threshold value for the 'significance' test. If a bar is having a value lower than the significance value, we can define this factor as having a 'significant effect,' based upon a significance level of 0.05. It can be observed from 4.4 (a) Pareto chart regression that embossing pressure and temperature are the significant factors for reducing the sheet resistance in our process. It can be noted that pressure is most significant and of greater significance than temperature. This can be attributed to the better integrity of the electrical junctions created due to the mechanical pressing force. Figure 4.4 (b) shows the Pareto chart analysis of variance (ANOVA) for change in sheet resistance. It can be observed that there is no 2-way interaction between the factors.

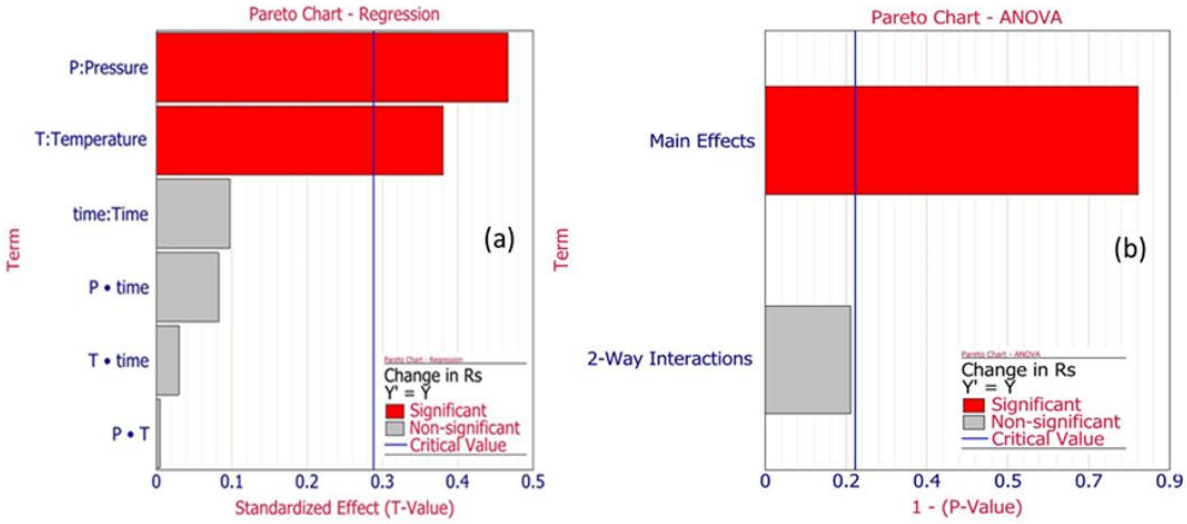


Figure 4.4: (a) Pareto chart-regression (b) Pareto chart analysis of variance (ANOVA) for change in sheet resistance.

## 4.4 Effect of Photonic Curing and $N_2$ Plasma on AgNW TCEs

After thermal embossing, another post processing step of applying a $N_2$ plasma cleaning was carried out on AgNWs coated substrates. The treatment process was conducted using a Diener second 'Nano' plasma treatment system at ambient pressure after a 30 seconds nitrogen purge. In this system, a 13.56 MHz RF Generator was used at 100 watts power to generate $N_2$ plasma for 120 seconds. The effect of plasma cleaning was observed and sheet resistance and transmittance were measured before and after plasma cleaning. AgNW electrodes were Nitrogen ($N_2$) plasma treated for 2 minutes, which result in an average 39.8 % reduction of sheet resistance, although no change in transmittance was noted. This reduction in sheet resistance is attributed to the removal of the PVP layer [96]and the enhancement of the contact between AgNWs.

NIR photonic curing was performed using a Novacentrix system, mentioned in section 3.2.2 and Figure 3.6 (b) was used to rapidly anneal the surface of AgNW TCEs. This results in improvements in electrical conductivity due to the welding of AgNWs junctions. Various AgNW TCE samples were subjected to a photonic curing/sintering process to find appropriate voltage (450V) pulse. The sheet resistance across the AgNWs electrode was measured using four probe system described in chapter 3 before and after applying sintering voltage pulse. Samples were mounted to the system and exposure varied from 450V, 400μs to 750μs with single energy pulse 1488mJ/cm$^2$ to 2712mJ/cm$^2$. The process ensured sintering occurred within the top 1μm of the film surface, rather than the entire thickness of the substrate and therefore impacted mostly upon the AgNW film. By concentrating the sintering so close to the surface, flexible and polymeric substrates can be used, and surface damage can be minimised.

It was found that a pulse duration of 600 to 700 μs was the most suitable for AgNW TCEs photonic curing because there is a maximum reduction in sheet resistance at around 700 μs. Longer duration pulses than 700μs or multiple pulses (1800 μs – 3 pulses) were not suitable because the polymeric substrate began to melt at sides of AgNW samples. Photonic sintering resulted in an average 40.8% reduction of sheet resistance, and no change in transmittance was noted. The individual and combined effects of post processing steps on properties of the AgNWs electrode are tabulated in the next section 4.5 Table 4.3.

## 4.5 Effect of Post Processing on Electrical and Optical Performance of AgNW TCEs

The overall impact of the individual post processing techniques and their combined effect is shown in Table 4.3. It can be seen that the optimised individual post-process of thermal embossing, sintering, and $N_2$ plasma treatment have a similar effect upon the reduction in $R_{sh}$; leading to a reduction of ~50%, when compared to the control samples. By using all three post processing techniques sequentially, a substantial 93.4% reduction in the sheet resistance was obtained. Optimisation of the sequence of the different processing steps was conducted and the optimum sequence was (1) NIR sintering, (2) thermal embossing and (3) $N_2$ plasma treatment. Importantly, none of the post processing techniques show a compromise in the optical transmittance or the optical haze of the samples with no change observed in these parameters (shown in Table 4.3). As discussed earlier, a FoM can often be used in TCEs to compare performances (defined in equation 2.4). The FoM for the

combined post processing technique shows a value of 933; this is substantially higher than the highest reported in the literature, 487.9, and represents the best performing TCE based upon AgNWs, or ITO-replacements. As a comparison, the performances are benchmarked against the incumbent technology (ITO) which is reported for both glass and PET substrates (Table 4.3). In both cases, the AgNW TCEs prepared with the post processing technique show significantly enhanced performance over the ITO.

Table 4.3: Electrical and optical performance before and after post-processing, showing changes in sheet resistance ($R_{Sh}$) and optical properties and the 'Figure of Merit' (FoM) is shown and benchmarked against ITO.

| Process | $R_{sh}$ (Before post process) $\Omega$ sq$^{-1}$ | $R_{sh}$ (After Post process) $\Omega$ sq$^{-1}$ | Percentage reduction in $R_{sh}$ (%) | Optical transmittance @ 550nm (%) | Optical haze (%) | FoM (After Post process) | Average Percentage change in FoM |
|---|---|---|---|---|---|---|---|
| Embossing | 40.4 | 18.1 | 55.2 | 92.9 | 0.2 | 278.9 | 120.8 |
| Sintering | 42.4 | 19.1 | 55.0 | 94.0 | 0.3 | 314.1 | 97.1 |
| $N_2$ plasma | 41.4 | 20.1 | 51.4 | 92.7 | 0.3 | 242.8 | 90.2 |
| Combined | 37.6 | 2.48 | 93.4 | 89.5 | 0.2 | 932.9 | 518.4 |
| Combined and with ZnO NP coating | 37.1 | 2.98 | 81.7 | 85.2 | 0.4 | 758.7 | 498.6 |
| ITO on PET | 40.0 | n/a | n/a | 85.0 | 0.4 | 55.7 | n/a |
| ITO on glass | 12.0 | n/a | n/a | 84.0 | 0.5 | 172.4 | n/a |

## 4.6 Surface Topographic Properties

In this section, surface roughness parameters before and after post-processing are investigated. In the context of TCEs, the surface roughness of the sample is very important. In OPVs and TFTs, the low surface roughness of TCEs can lead to AgNWs penetrating through the active regions of the devices leading to electrical shorts.

### 4.6.1 Surface Topographic Properties Before and After Post Processing

The positive changes in surface roughness after post processing are reported in Table 4.4. The data shows that the root mean square surface roughness ($R_q$) is reduced to 3.6 nm from 6.4nm, the average roughness ($R_a$) is reduced to 2.7 nm from 4.9 nm and the maximum peak-to-valley to 60.8 nm from 105.9 nm after the post processing techniques. The surface roughness was benchmarked also against incumbent technology (also shown in Table 4.4) and it is evident that after post processing, there is a 21.5 to 45.4 percent reduction in the $R_a$, $R_q$, $P_v$ surface roughness parameters.

Given the significant enhancements in electrical and surface topographic properties, it is necessary to discuss their origins. SEM images of AgNW TCEs before and after post embossing are shown in Figure 4.5 (a) and (b) respectively. Based on this, it can be said that the percolating network of AgNWs after embossing possess shows a more uniform height as the variation in SEM contrast is less obvious. Whilst topography can be somewhat difficult to evaluate using SEM, the images do show that the embossing step leads to improved physical contact between percolating AgNWs and is therefore likely to increase the number of electrical connections between AgNWs and integrity of the contact junctions. As the embossing temperature was low, it is unlikely there is any 'fusing' of AgNWs electrodes due to this alone. The reduction in SEM contrast indicates reduced secondary electron emission and is likely to be as the AgNWs are partially-embedded within the polymer substrate. The embedding of the AgNWs into the polymer surface is likely to contribute to the reduction in surface roughness as the top surface topography is determined by the smoothness of the nickel shim which determines the embossed surface smoothness, rather than the protrusions of the AgNWs. In Figure 4.5 (c), it is apparent that the AgNWs have compressed and are embedded into the PMMA layer and some appear to have fractured during the embossing stage. It is clear that the applied pressure and temperature need to be optimised as over pressurising during the embossing stage can lead to fractures which will diminish sheet resistance.

Table 4.4: Surface topographic properties before and after post-processing, showing changes in average surface roughness (Ra), root-mean square roughness (Rq) and Peak to Valley roughness (Pv) and benchmarked against ITO measured using WLI.

| Sample | $R_a$ (Before Post process), nm | $R_a$ (After Post process), nm | % Change in $R_a$ | $R_q$ (Before Post process), nm | $R_q$ (After Post process), nm | % Change in $R_q$ | $P_V$ Peak to valley (Before Post process) nm | $P_V$ Peak to valley (After Post process) nm | % Change in peak to valley $P_V$ |
|---|---|---|---|---|---|---|---|---|---|
| AgNWs Combined | 6.8 | 3.7 | 45.4 | 8.5 | 4.9 | 43.0 | 101.4 | 79.6 | 21.5 |
| AgNWs and with ZnO NP coating | 4.9 | 2.7 | 44.9 | 6.4 | 3.6 | 43.8 | 105.9 | 60.8 | 42.6 |
| ITO on PET | 3.3 | n/a | n/a | 4.7 | n/a | n/a | 52.2 | n/a | n/a |
| ITO on glass | 1.1 | n/a | n/a | 2.2 | n/a | n/a | 10 | n/a | n/a |

The physical changes that occur as a result of photonic sintering are also shown in the SEM image in Figure 4.5 (d, e). The data in Table 4.4 shows that the average $R_{sh}$ reduces by ~50% after sintering. Based on the SEM images, the sintering process affects the AgNWs by melting and moderately deforming the AgNWs so that the formation of better electrical junctions between individual nanowires is achieved which leads to the enhanced conductivity in films. In previous work, high temperature processing has been shown to remove residue polyvinyl propyl (PVP) in the AgNWs, leading to improved chemical purity [58], which is also likely to contribute to the improvement in the $R_{Sh}$. Because the changes related to $N_2$ plasma treatment are most likely to be changed in the material chemistry, this is better discussed in section 4.11, where XPS studies of the surface chemistry are discussed. The $N_2$ plasma treatment is likely to also remove the PVP which results in the improvement in sheet resistance. The effect of zinc oxide nanoparticles to further improve surface properties is discussed in the next section 4.6.2.

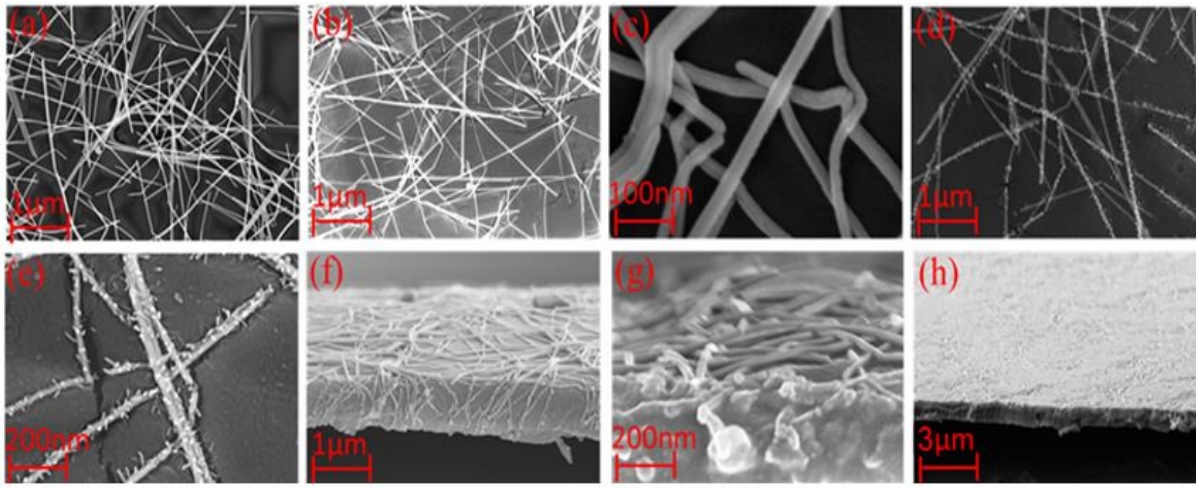


Figure 4.5: SEM images of (a) AgNWs before embossing, (b) after embossing and (c) after embossing at higher resolution, (d) after embossing and sintered, (e) after embossing/sintering at a higher resolution. Cross sectional SEM images show (f) before embossing, (g) before embossing at higher resolution and (h) sample that has been embossed and sintered.

### 4.6.2 Application of Zinc Oxide Nanoparticles to Further Improve Surface Properties

After post processing, a zinc oxide (ZnO) nanoparticle dispersion in ethanol was spray coated directly on the post processed TCEs. Film thickness was measured using a cross-sectional SEM and was measured at 40±3 mm. By spray coating of the ZnO nanoparticles, a further planarization layer is deposited onto the AgNWs film, without significantly impacting on either $R_{sh}$ or optical transmittance. This is best illustrated in the WLI data

shown in Figure 4.6, which shows surface roughness changes in a control sample, post-processed sample and post-processed sample with ZnO overcoating. ZnO nanoparticles couple with AgNWs to form a composite electrode and it should further decrease in surface roughness. This is possibly due to filling up of vacate gap with ZnO nanoparticles and hence lowers the roughness parameter values.

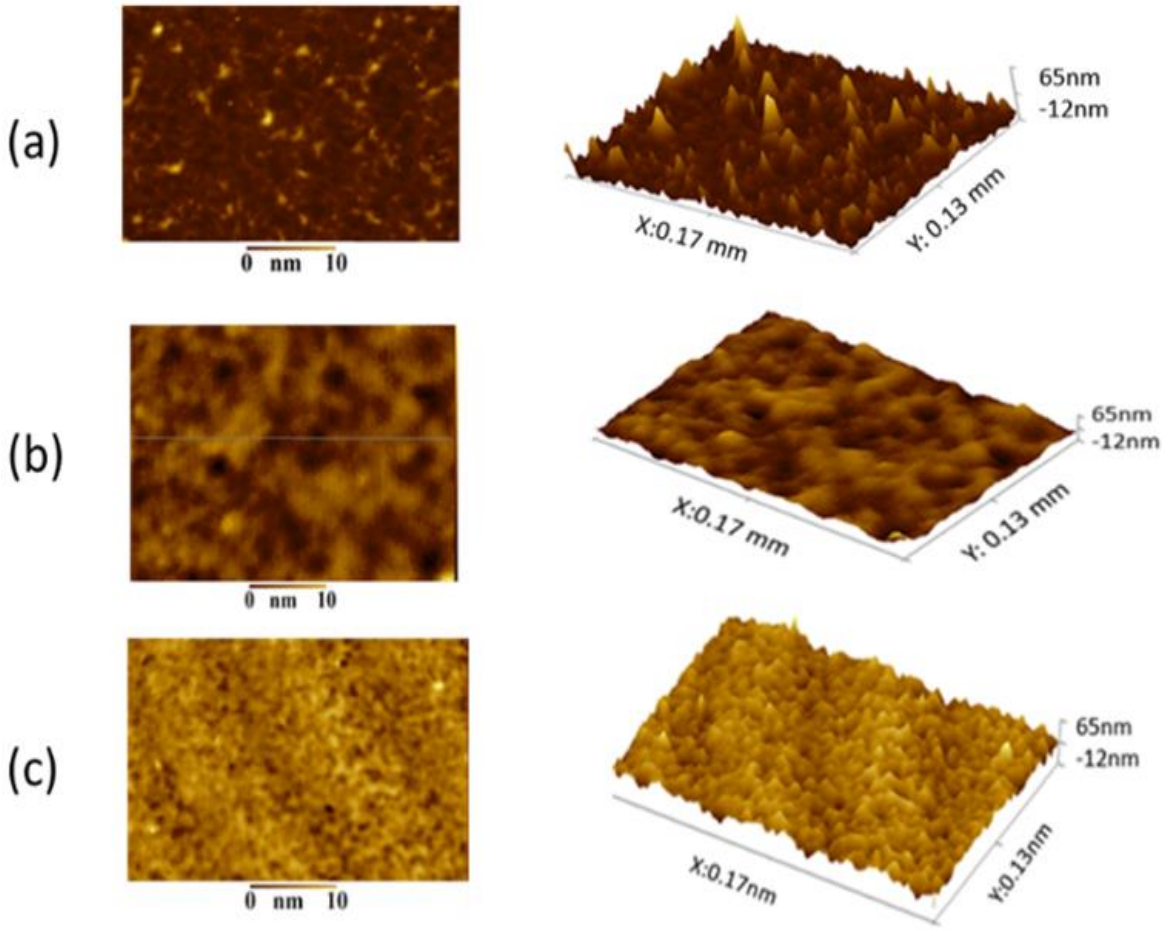


Figure 4.6: Surface topography images using white light interferometry (WLI), (a) the control sample, (b) post-processed sample and (c) post-processed sample with ZnO overcoating.

The roughness is quantified in Table 4.4 (mentioned earlier) and the combined AgNWs-ZnO electrode is shown to possess roughness much lower than the control sample and is comparable to ITO on PET. It is clear from the WLI data that the ZnO fill up the voids created by the network of AgNWs and covers any remaining AgNWs that are protruding and thus improves the surface roughness. The result is significant for a second reason; for OPVs and OLEDs, ZnO is often used as an interlayer as the energy levels are favourable for electron extraction or hole injection (for OPVs and OLEDs, respectively). Therefore, the

ZnO layer has dual functionality as it planarises the AgNWs electrode and ensures energy alignment between the transparent electrode and the active region.

### 4.6.3 Demonstration of OPV Device

To demonstrate the suitability of the AgNWs electrode films, inverted Organic Photovoltaics (OPVs) were fabricated onto the developed TCEs. This work was performed with the help and support of my supervisor Dr. J. Kettle. To benchmark the AgNW TCEs, PSC devices were also made using ITO coated PET substrates ($R_{sh}$ = 60 Ω/square, transmittance = 84% purchased from Sigma Aldrich) that were first cleaned using deionised water, acetone and isopropanol in an ultrasonic cleaner, then treated in a UV-ozone reactor with oxygen plasma for 10 minutes. The remaining device fabrication procedure was the same. The AgNW and ITO substrates were coated with ZnO with a film thickness of 80nm. Samples were transferred into a nitrogen atmosphere glovebox ([$O_2$], < 1ppm; [$H_2O$], <100ppm), where the active layers and contacts were applied. The absorber was deposited inside a glove box by spin-coating using the two-step procedure. Active layer BHJ blends using PTB7-Th (as a donor) and [6,6]-phenyl-$C_{71}$-butyric acid methyl ester ($C_{71}$-PCBM) (as an acceptor) with weight ratios 1 : 1.5 were prepared and mixed with chlorobenzene solvent with a concentration of 30 mg $mL^{-1}$. Active layers were applied by spin-casting from a 45 $^0$C solution. The active layer was annealed at 45 $^0$C for 15 minutes before thermal evaporation of the cathode was performed through a shadow mask to define the device area and consisted of 8 nm of $MoO_3$ and 100 nm of silver (Ag) to form the cathode of the device.

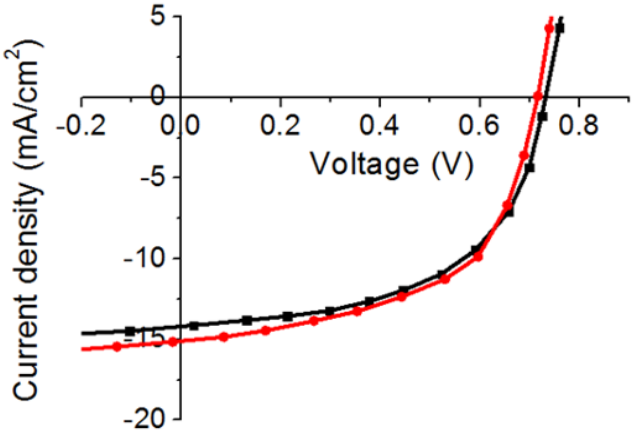


Figure 4.7: Typical current–voltage characteristics for PTB7-Th:PCBM OPV using ITO-based electrodes on PET (black) and glass substrates and AgNWs-based electrode (red) under 100mW/cm$^2$ AM1.5 illumination.

The measurement system used to characterize the devices consisted of a Newport solar simulator with 100 mWcm$^{-2}$ AM1.5G output (calibrated using a silicon reference cell from RERA in the Netherlands. The open circuit Voltage ($V_{oc}$), short-circuit current density ($J_{SC}$), fill factor (FF) and PCE values are averaged from twelve cells.

The performance was benchmarked against an ITO electrode manufactured on PET. Shown in Figure 4.7 are the IV characteristics under AM1.5G illumination from a set of 12 devices made with ITO or AgNW front electrodes, with the remainder of the device structure not changing during these tests. IV characteristics are shown for the device which was closest to the mean in both sets of devices, and the PV performance parameters and manufacturing yield are reported in Table 4.5

Table 4.5: IV characteristics of PTB7-Th: PCBM solar cells measured with 100 mWcm$^{-2}$ AM1.5G output. Performances and yield are measured from 12 devices.

| Sample | $V_{OC}$ (V) | $J_{SC}$ (mA/cm$^2$) | FF | PCE | Yield |
|---|---|---|---|---|---|
| ITO on PET | 0.732 | -16.3 | 0.56 | 6.70 | 100% |
| AgNWs on PEN | 0.716 | -16.8 | 0.58 | 7.00 | 100% |

In terms of performance, the AgNWs shows a moderately improved PV performance; this is primarily due to an increase in short circuit current density ($J_{SC}$) of around 0.6 mA/cm$^2$ and Fill Factor of 2%, compared to the sample made on an ITO substrate leading to a drop in the PCE. One would expect the AgNWs device to have a higher FF than the device made on ITO-PET due to the lower $R_{Sh}$, but the observed differences in the FF are minor. Considering the IV characteristics reported in Figure 4, the series resistance ($R_S$) of the AgNWs device is moderately better than that of the ITO-PET device, but there appears to be a decrease in shunt resistance ($R_{Sh}$). This decreased $R_{sh}$ is attributed to the increased shunts and parasitic pathways between AgNWs films and the PTB7-Th:PCBM active layer as the ZnO might not fully planarise the gap in-between the AgNWs and the active layer. In the case of a larger device or modules, the use of AgNWs would have an even greater impact upon PV performance as the $R_{Sh}$ plays a much more significant role as the area increases. The open circuit Voltage ($V_{OC}$) of the AgNWs electrode device is slightly lower as AgNWs possess a lower work-function and this accounts for the observed decrease of $V_{OC}$ [196]. In addition to the slight performance increase, the AgNWs do possess a number of additional advantages over ITO including the

improved mechanical robustness, no post treatment requirements and is not processed in vacuum.

Device performance has also been tested in resistive heaters and shown in Figure 4.8. The performances demonstrated for bias condition (5V, 300mA), showing that heat can be applied very quickly and over an extended temperature range (limited by the temperature compatibility of the substrate). This data shows that the post-processed electrodes can be used for a range of applications.

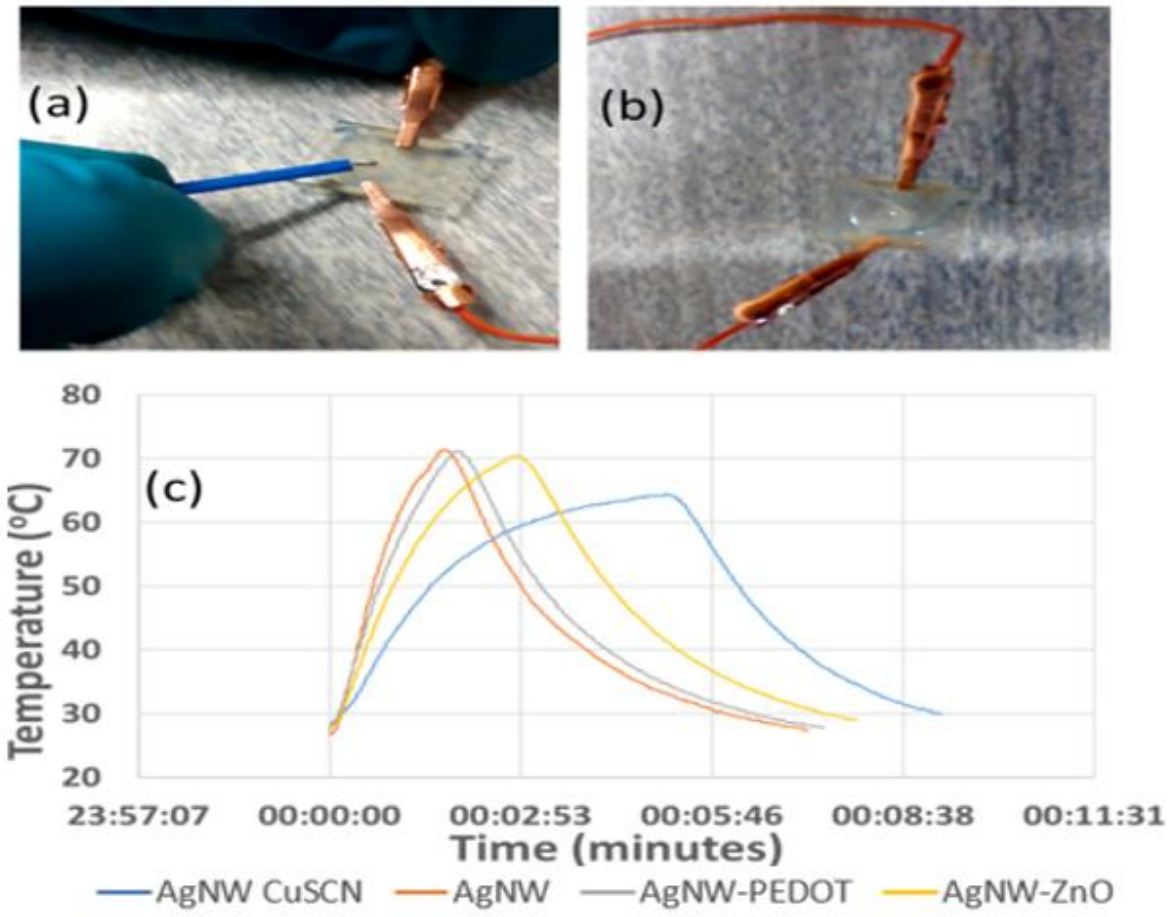


Figure 4.8: (a), (b) Images of transparent heaters, (b) Temperature profile of transparent heaters with different over-coatings.

## 4.7 Mixed AgNW TCEs

In this section individual AgNWs and mixed AgNWs type TCEs with a similar $R_{Sh}$ of 25±1 Ω sq-1 results are presented. Individual types of AgNWs with different mean diameter D and length L used for the study, namely thin-short nanowire; AgNWs-60S (D = 60 nm, L = 20-30 µm), thin-long nanowire; AgNWs-30L (D = 30 nm, L = 100-200 µm) and thick-long

nanowires; AgNWs-100L (D = 100 nm, L = 100-200 μm). The shorter nanowires are advantageous for achieving high conducting networks at low concentration and the longer nanowires provide higher conductivity performance. The combined advantages of short and long nanowires were exploited by coating them together. Two mixed AgNWs composition were prepared, one consisted of the type: thin-short nanowires (AgNWs-60S) with thin-long nanowires (AgNWs-30L), denoted as 'AgNWs-M1', and another one consist of the type: thin-short nanowires (AgNWs-60S) with thick-long nanowires (AgNWs-100L), denoted as AgNWs-M2. Mixed composite AgNWsAgNWs-M1 dispersion was prepared by mixing AgNW-60S and AgNWs-30L as supplied in 1:1 volume by volume (V/V) ratios and then diluted with ethanol to 0.4 mg/mL final concentration. Similarly, AgNWs-M2 was prepared with AgNWs-60S and AgNWs-100L. AgNW dispersions in ethanol of each type (0.5 mg/mL) were sonicated at low power for 5 minutes to minimized aggregates before air spray coating. Individual AgNWs and mixed AgNWs type TCEs were prepared using the same process discussed in chapter 3 section 3.3. The deposition time for preparing electrodes with $R_{Sh} \approx 25\ \Omega\ sq^{-1}$ was found to be approximately 5 minutes ±5 seconds. However, using mixed geometry electrodes, the deposition time was approximately 50% lower due to more inter connections made by short AgNWs to connect the gap between longer nanowires. This represents a significant advantage for future scale up of the technology. The mixed AgNWs results show moderate improvement in the electrical/optical performance and the surface roughness.

SEM images of the conducting surface of AgNW electrodes prepared from fixed dimension type AgNWsAgNWs-30L and AgNWs-60S is shown in Figure 4.9 (a) and Figure 4.9 (b) while a mixed composition type AgNWs-M2 is shown in Figure 4.9 (c). The inter mixing of short-thin nanowires AgNWs-60S with long-thick nanowires AgNWs-100L can be clearly seen from Figure 4.9 (c), which provides more event surface coverage and as a result of fewer aggregations at nanowire junctions.

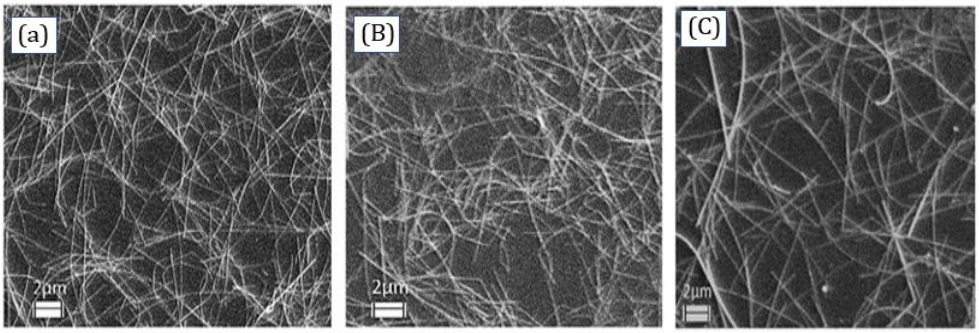


Figure 4.9: SEM images of (a) AgNWs-30L (b) AgNWs-60, (c) AgNWs-M2.

### 4.7.1 Optical and Electrical Properties

The transmittance spectra of TCE prepared by the different types of AgNWs dispersion with a similar $R_{Sh}$ of 25±1 Ω $sq^{-1}$ are shown in Figure 4.10 (a). This value of $R_{Sh}$ was chosen as it represents a sizeable improvement over ITO on a flexible substrate and is comparable to the value of ITO often used on glass substrates. It can be seen from Figure 4.10 (a) that longer AgNW electrodes (AgNWs-100L, AgNWs-30L) shows 5-10% transmittance improvement in the visible region of spectrum compare to the shorter nanowires AgNWs-60S. In addition, the thin-long nanowires (AgWS-30L) electrode was found to show higher transmittance than the thick-long nanowires (AgNWs-100L) electrode with similar $R_{Sh}$ of 25Ω$sq^{-1}$.

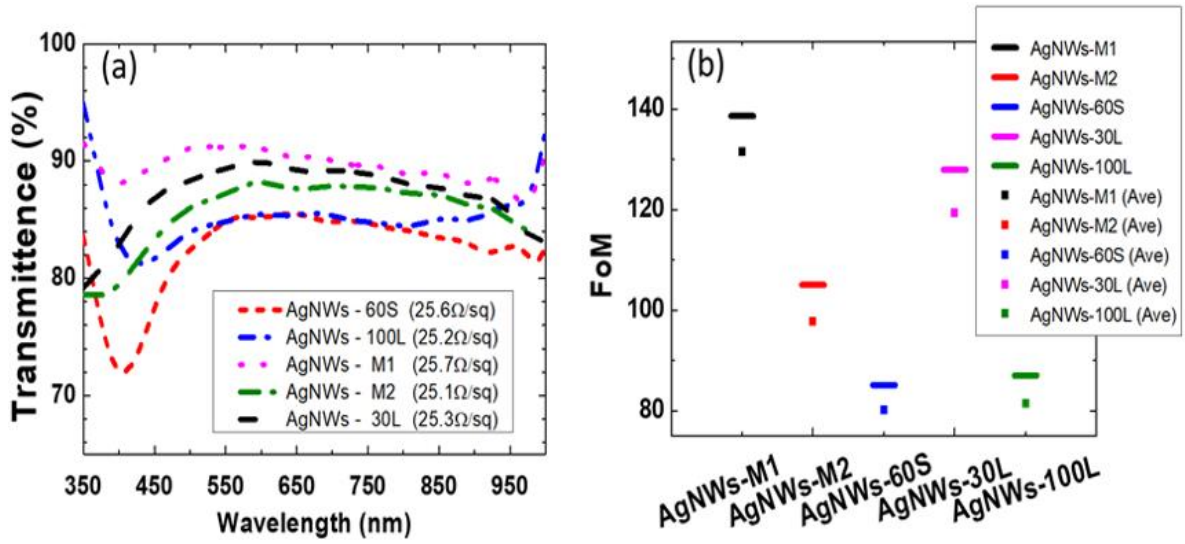


Figure 4.10: (a)Transmittance spectra of AgNWs-30L, AgNWs-60S, AgNWs-100L, AgNWs-M1 and AgNWs-M2 composite electrodes with $R_{sh}$ of 25 Ω $sq^{-1}$, (b)FoM and average FoM of AgNWs-30L, AgNWs-60S, AgNWs-100L, AgNWs-M1 and AgNWs-M2 composite electrodes with sheet resistance of 25 Ω $sq^{-1}$.

The mixed composition AgNWs-M1 electrode shows similar overall transmittance values to the longer nanowire component AgNWs-30L, but with moderate improvement in the region 400 nm to 550 nm of the visible spectrum. This could be a significant result for academics and industrialists working with blue OLEDs, who wish to maximize the light output in this region. Likewise, the AgNWs-M2 electrode displayed better transmittance compared to its parent AgNW electrodes of AgNWs-60S and AgNWs-100L and improved performance in the blue-green spectrum. Due to the reduced aggregation and better percolation of the mixed AgNWs films, the transparency is greater for the same sheet resistance, and the overall silver content of the film is lower. For the

AgNW TCEs, the silver content is calculated at 0.2 mg $cm^{-2}$ for mixed, which compares to 0.3 mg $cm^{-2}$ for long AgNWs and 0.4 mg $cm^{-2}$ for short AgNWs.

To quantify the optical and electrical properties a Figure of merit (FoM) is commonly defined in literature given in equation (2.4), discussed in Chapter 2. For comparison, commercial ITO film on PET used in our laboratory was measured and the FoM found to be 58 ($R_{Sh}$ = 60 Ω $sq^{-1}$, transparency = 90%, source Sigma Aldrich, UK). The FoM values calculated for various AgNW electrodes of 25 Ω $sq^{-1}$ $R_{Sh}$ with transmittance (%T) at 550 nm is plotted in Figure 4.10 (b). Among the different AgNWs type electrodes studied, the mixed composition AgNW electrodes AgNWs-M1 (FoM = 138.6, Table 4.6) has the highest FoM value while lowest for short-thin nanowires AgNWs-60S (FoM = 85.1, Table 4.6). The optical performance of the mixed-composition electrodes (AgNWs-M1, AgNWs-M2) in terms of FoM is found to be higher as compared to the parent electrodes (AgNWs-30L, AgNWs-60S, AgNWs-100L) having same $R_{Sh}$ of 25 Ω sq−1. In Table 4.6, the best and average performances of the three most promising combinations are shown i.e. AgNWs-M2**,** short AgNWs-60S, and long AgNWs-30L**.** When considering the FoM, the mixed AgNWs films show around 10-15% improvement over the best obtained results from an AgNWs film prepared from a single nanowire geometry (AgNWs-30L). In addition, the mixed AgNWs film shows 30-40% improvement over AgNWs films prepared with short nanowires. The results support the conclusion that short nanowires do not provide good percolating networks and therefore exhibit poorer performance than longer nanowires. However, they could still have industrial applications, should they be used in combination with longer nanowires.

Table 4.6: Average (from 5), best and standard deviation (s.d) of sheet resistance and transmittance of (AgNWs-M2), short (AgNWs-60S) and long (AgNWs-30L) electrodes.

| Type | $R_{sh}$ (Ω $sq^{-1}$) (Best) | $R_{sh}$ (Ω $sq^{-1}$) (Average) | $R_{sh}$ (Ω $sq^{-1}$) (s.d) | T (%) (Best) | T (%) (Average) | T (%) (s.d) | FoM (Best) | FoM (Average) |
|---|---|---|---|---|---|---|---|---|
| AgNWs-M1 | 25.7 | 25.9 | 0.2 | 90.2 | 89.8 | 0.5 | 138.6 | 131.6 |
| AgNWs-M2 | 25.1 | 25.4 | 0.4 | 87.1 | 86.4 | 0.9 | 105.0 | 97.8 |
| AgNWs-60S | 25.6 | 26.0 | 0.8 | 84.7 | 84.1 | 0.4 | 85.1 | 80.1 |
| AgNWs-30L | 25.3 | 25.8 | 0.7 | 89.3 | 88.8 | 0.6 | 127.9 | 119.4 |
| AgNWs-100L | 25.2 | 25.4 | 0.3 | 84.8 | 84.0 | 1.0 | 87.0 | 81.4 |

### 4.7.2 Surface Roughness

The surface roughness of the conductive surface of the AgNW electrodes was examined by white light interferometry (WLI) and AFM. Figure 4.11 shows the topological images of AgNWs-30L, AgNWs-60S, and AgNWs-M2 electrodes, respectively.

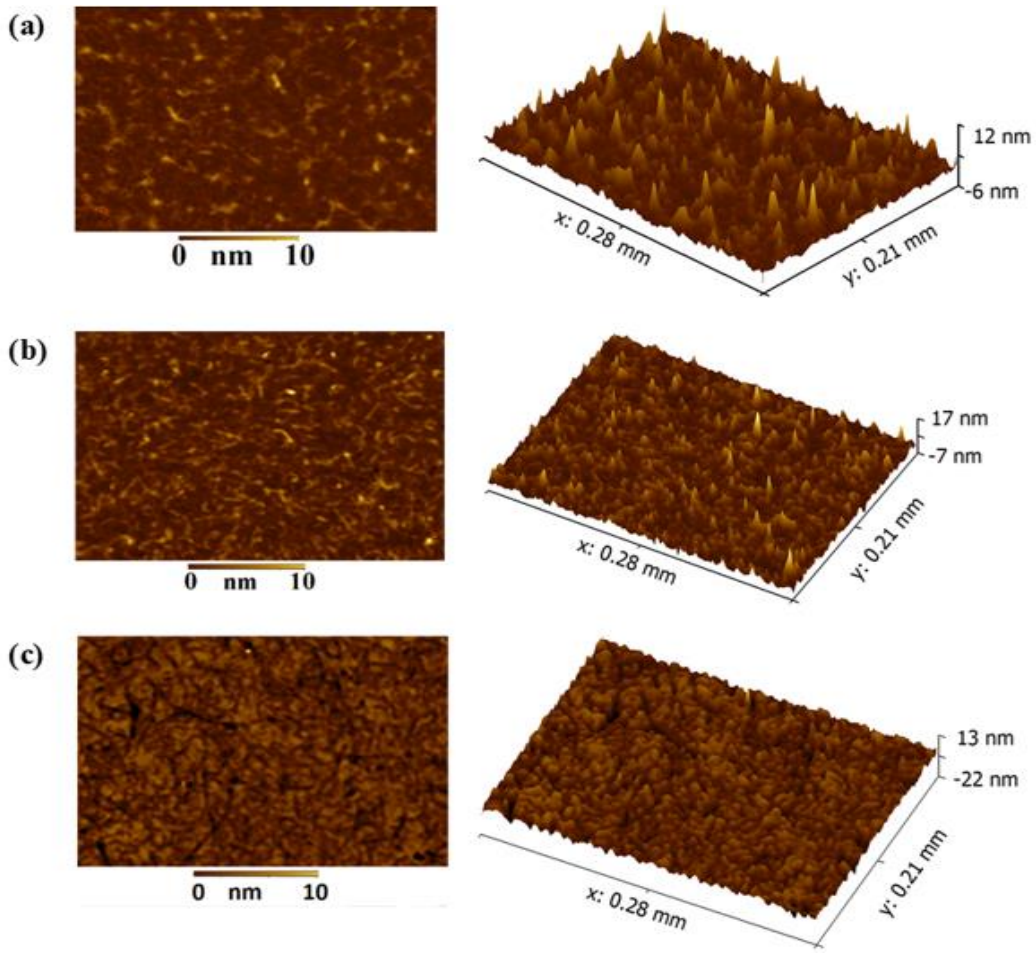


Figure 4.11: WLI topological images of a) AgNWs-60S, b) AgNWs-30L c) AgNWs-M2 on PMMA coated PEN.

Table 4.7 shows the surface roughness of various types of nanowires electrodes, (AgNW-30L, AgNW-60S, AgNWs-100L, AgNWs-M1, AgNWs-M2) by WLI measurement over a large area of 278 x 207 $\mu m^2$. In this work, the surface roughness was calculated from an average of five different samples and the average root mean square roughness ($R_q$) and maximum peak-to-valley ($P_V$) roughness was calculated.

For all samples, the highest average $P_V$ roughness was obtained for the short nanowires ($P_V$ = 87.2nm), although the surface roughness is overall much lower than other reports. The low peak-to-valley roughness was attributed to the PMMA layer, which possibly facilitates the embedding of nanowires, thereby smoothening the surface.

Table 4.7: Surface roughness parameters of mixed (AgNWs-M2), short (AgNWs-60S) and long (AgNWs-30L) electrodes.

| Type | Rq (nm) average | Rq (nm) STDV | Pv (nm) average | Pv (nm) STDV |
|---|---|---|---|---|
| AgNWs-M1 | 3.2 | 0.2 | 75.2 | 2.1 |
| AgNWs-M2 | 4.1 | 0.4 | 80.9 | 2.9 |
| AgNWs-60S | 8.5 | 1.2 | 87.2 | 3.9 |
| AgNWs-30L | 6.2 | 0.6 | 85.9 | 3.8 |
| AgNWs-100L | 5.9 | 0.3 | 80.1 | 2.0 |

The root mean square roughness ($R_q$) for the mixed composition AgNW electrodes (AgNWs-M1, AgNWs-M2) are found in the range 3-4 nm while for the fixed dimension type nanowires electrodes (AgNWs-30L, AgNWs-60S, AgNW-100L) the values are in the range 6-8 nm. This indicates that the mixed composition AgNW electrodes possess a somewhat smoother surface compared to the fixed dimension type AgNW electrodes, attributed due to a more evenly distributed surface coverage. For illustration, topological images of a short, a long and mixed composition type nanowire electrode are shown in Figure 4.11. It can be seen by visual inspection of Figure 4.11 that AgNWs-M2 ($R_q$ = 3.7 nm, PV = 79.6 nm), based electrodes topological image is smoother compared with AgNWs-30L ($R_q$ = 5.5 nm, $P_V$= 77.3 nm) and AgNW-60S ($R_q$ = 7.9 nm, $P_V$ = 81.7 nm) electrodes. The high surface roughness of AgNW TCE is a result of multiple AgNWs overlapping one another or by aggregation. A low volume of material is used during this deposition, so the long AgNWs are dispersed quite evenly across the sample and the amount of overlap is relatively low. Long AgNWs tend to form more aggregates during the spray coating deposition, so by minimizing the volume deposited, the concentration of aggregates is reduced, thus lowering the overall surface roughness. Subsequently, the short AgNWs are deposited; these do not tend to form large aggregates. Therefore, they act as an 'in-fill' into the long AgNW mesh, providing the percolation and ensuring no major aggregation points are formed.

The advantage of mixed composition silver nanowires, comprising of short nanowires length (L = 25 μm) with long nanowire (L = 150 μm), include shorter spray deposition time, better electrical/optical properties (as evidenced by the FoM values) and lower surface roughness electrodes. We believe that the simple technique demonstrated in this work will be effective in saving time and cost for large-scale production of AgNW based transparent conducting electrodes and helpful for further development of metallic nanowire-based electrodes in general.

## 4.8 Effect of Post Processing on Stability of AgNW Films

To study the stability of AgNW films, AgNW TCEs were subjected to various high temperature and current conditions to access the lifetime, failure at 10 %, 25% of the initial value of electrode resistance (shown in Table 4.8). One of the examples to test the lifetime of AgNWs TCEs is shown in Figure 4.12. Embossed and non-embossed (normal or non-post processed) AgNWs TCEs were subjected to 300 mA at 65 $^0$C temperature to observe the effect of embossing on high current and 65 $^0$C stability. It can be clearly observed from Figure 4.12 (a) and (b) that embossed AgNW TCEs are much stable as compared to normal due to negligible change or degradation for embossed samples due to less heat dissipation.

Table 4.8: Failure (300 mA, RT, 65 $^0$C) at 10 %, 25% of initial value of electrode resistance.

| Post process | Stress condition | Failure at 10 % of initial value (Ω) | Time for failure at 10 % of initial value (hours) | Failure at 25 % of initial value (Ω) | Time for failure at 25 % of initial value (hours) |
|---|---|---|---|---|---|
| No | 300 mA at RT | 26.51 | 264.00 | 30.13 | 401.25 |
| | | 20.13 | 362.25 | 22.88 | 645.00 |
| Embossed | | 16.94 | 960.00 | 19.25 | 2358.00 |
| | | 14.96 | 1788.00 | 17.00 | 4308.00 |
| No | 300 mA at 65 $^0$C | 27.83 | 5.46 | 31.63 | 13.69 |
| | | 38.50 | 4.50 | 43.75 | 11.29 |
| Embossed | | 17.38 | 62.25 | 19.75 | 165.75 |
| | | 15.84 | 60.00 | 18.00 | 153.00 |

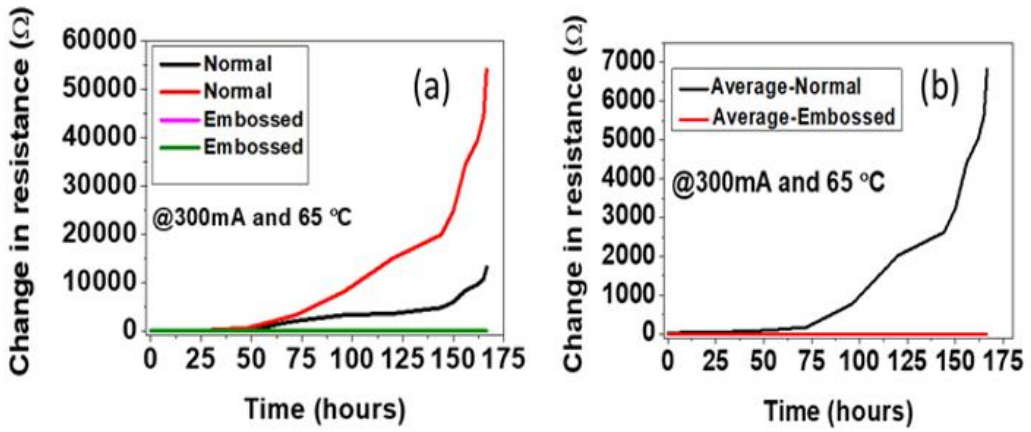


Figure 4.12: Effect of embossing on high current 300 mA at 65 $^0$C temperature stability (a) Change in resistance for normal and embossed AgNW TCEs up to 166.5 hours (b) Average change in resistance for normal and embossed AgNW TCEs up to 166.5 hours.

## 4.9 QALT Testing of the Reliability of AgNW Films

To study stability, quantitative accelerated life testing (QALT) can be applied to relate failure rates achieved at elevated stress levels to what might be under normal operational conditions. For this work, four experimental tests were conducted using a (2^2) full factorial experimental design with the following two-stress, two-level conditions; 45 $^0$C/150mA/cm$^2$, 45$^0$C/250mA/cm$^2$, 65$^0$C/150mA/cm$^2$ and 65$^0$C/250mA/cm$^2$ applied to accelerate the degradation. When the temperature and current density are the accelerated stresses of a test, then a modified Eyring model can be developed and used as the life test model to relate degradation at an elevated stress level to that at a lower, operational level. This is shown in equation 4.1 and is referred to as the Temperature-current (TI) relationship. Equation 4.1 can be used for predicting life at lower operational conditions, where life is shown as a function of temperature ($V$) and current density ($I$) and all other components are fitting parameters and calculation of the acceleration factor (AF) (equation 4.2). Six samples were used each test condition and a Weibull 2-point distribution was applied for each stress level (defined in equation 4.3, where $\beta$ is defined as the shape parameter, $\eta$ is the scale parameter, $t$ is the time and $f(t)$ is the probability of failure. Shown in Table 4.9 are the fitting parameters of the TI model, which have been calculated for the time to increase in resistance by 10% (T10%) and 25% (T25%) of the original value. To compare the impact of post-processing, a consistent definition of failures is needed. For this work, we calculated the time for 63% of the population of AgNW electrodes tested to have declined a particular value [such as 10% increase in resistance (T10%) or 25% increase (T25%)]. This value is often referred to as B(63%). By considering equation 4.2, when $t = \eta$, the cumulative number of failures in the population, $F(t) = 63\%$, so $\eta$ is equivalent to B (63%).

$$L(I,\ V) = \frac{A}{I^n e^{-\frac{B}{V}}} \qquad \text{Eq. 4.1}$$

$$A_F = \frac{L_{USE}}{L_{Accelerated}} = \frac{{I_A}^n}{I_O}\ e^{D\left(\frac{1}{V_O} - \frac{1}{V_A}\right)} \qquad \text{Eq. 4.2}$$

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}} \qquad \text{Eq. 4.3}$$

Based upon equation 4.1, life is a function of two stress conditions, so life versus temperature and life versus current density can be plotted on a logarithmic scale to show how varying temperature or current density affects the life of the AgNW films, whilst the other variable is kept constant. This is shown in Figure 4.13 (a) and (b) for life model fittings from Table 4. The general trend is to be expected; as the stress level of current density (a) or temperature (b) is increased, the anticipated life of the AgNW film decreases. It is evident from Figure 4.13 that the stability of the post processed samples is substantially higher than the non-post processed samples, by around three orders of magnitude under normal operational conditions ($I_{bias}$=20mA/cm$^2$ and temperature). This is because the post processed samples possess a lower resistance due to improved electrical contact. As the power dissipated across the electrode is related to bias current and resistance by $P_D = I^2.R$, then the 'as used' sample will experience 16x more power dissipation that the post-processed sample, leading to increased Joule heating, which causes the nanowires to break up and thus creates an electrical discontinuity in the nanowire film [197]. As more heat is created, the probability of failures increases. Furthermore, during the post-processing procedure, the AgNWs are partially embedded within the underlying polymer, which is likely to act as a barrier layer limiting the impact of oxidation and sulfidation.

Table 4.9: Fitted parameters (FP)obtained using mean likelihood estimation (MLE) for post-processed samples and as-used samples. β is defined as the shape parameter, η the scale parameter from the Weibull 2-point probability distribution in equation 4.2. The values of A, B, and n are also fitting parameters from the temperature-current model. in equation 4.1.

| FP | Post-processed T10% | As used T10% | Post-processed T25% | As used T25% |
|---|---|---|---|---|
| A | 7.79e-7 | 2.0e-6 | 9.51e-8 | 3.20e-7 |
| B | 9359 | 7824 | 10220 | 8440 |
| n | 1.74 | 1.92 | 1.68 | 1.82 |
| β | 2.47 | 2.08 | 2.42 | 2.11 |
| η | 63353 | 433 | 175002 | 1005 |

An important characteristic often assessed in life test models is the acceleration factor (AF), which shows the ratio of the AgNWs life at the 'operational' stress level to its life at an accelerated stress level and is defined in equation 4.1. Both the post processed and 'as used' samples show similar characteristics, but the 'as used' samples appear to degrade quicker with increases in current density.

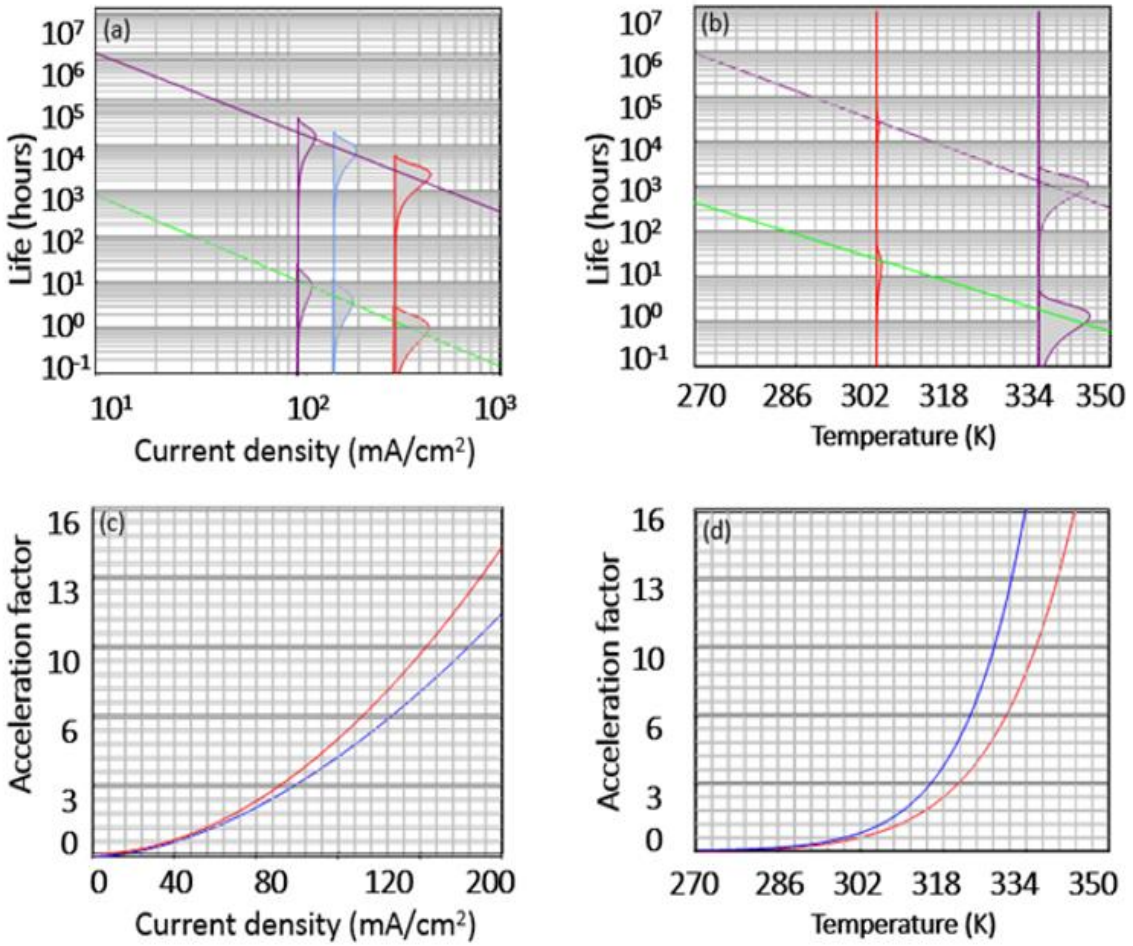


Figure 4.13: Regression line fitting for post-processed and 'as-used' AgNW films of the expected time to reach T90% as a function of (a) current density (mA/cm$^2$) and (b) temperature (K). Included in (a) and (b) are the fitted probability distribution functions for each stress level. The Acceleration Factor (AF) as a function of current density and temperature and RH humidity are shown in (c) and (d), respectively.

To evaluate the stability fully, further experiments have been conducted by applying different interlayers onto the AgNW electrodes to see the interaction between two layers. A single stress condition was applied ($I_{bias}$ = 300mA/cm$^2$ and temperature = 65 $^0$C), enabling a relative comparison of stability to be obtained, which is reported in Figure 4.14 The least stable electrode was the 'as used' electrode which had no post processing conducted. The poor stability is due to thermal oxidation of AgNWs as the sample is exposed to the environment. When AgNW films are exposed to air and water, they can be easily oxidized, leading to a sharp increase in sheet resistance and haze of the AgNWs films[198]. After the post-processing, the AgNWs are moderately embedded into PMMA and this appears to act as a barrier to inhibit the level of oxidation. By applying a further overcoating the stability is enhanced, although the most significant improvement is obtained by using the ZnO interlayer. The application of PEDOT+DMSO shows the

lowest stability as an overcoating layer and is likely to be related to the reactive nature of Ag to environmental sulphur which causes sulfidation.

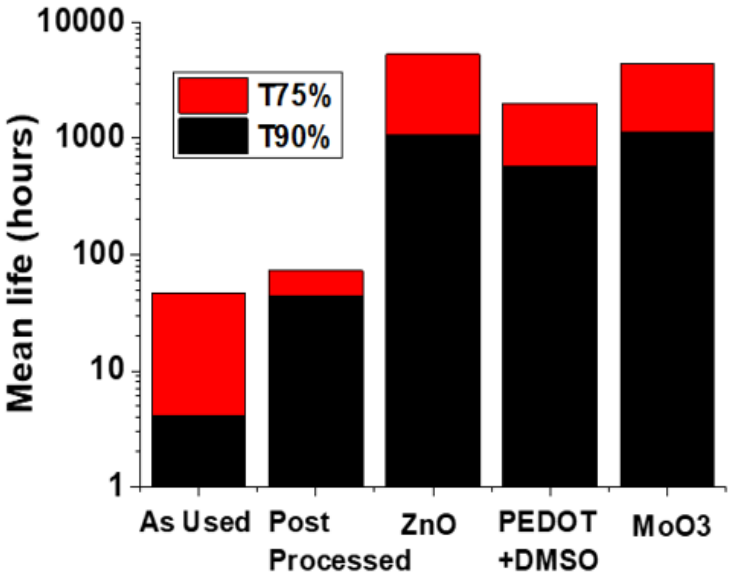


Figure 4.14: Bar chart showing mean time to reach T10% (black) and T25% (red) for AgNW films including non-post processed ('as used'), post processed, and post processed with ZnO, PEDOT:PSS+DMSO and $MoO_3$ transport layers. All samples were tested under the same conditions with a current density of 300mA/cm$^2$ and a temperature of 60 $^0$C applied.

It is worth noting that the optical properties did not change upon ageing. For example, the optical haze of the aged samples was compared to freshly prepared samples. For samples without any interlayers (i.e. ZnO/PEDOT:PSS), the optical haze of fresh samples was measured at 4.81%, which changed less than ±0.10% after ageing. This value is an average of three samples.

## 4.10 Adhesion and Mechanical Testing

The AgNWs adhesion was determined through a pull-off test using TQC SP302 standard tape (width 1cm). The procedure followed the ISO 2409 standard which is used for the determination of adhesion of polymeric layers such as paints and varnish [199]. Considering the AgNW films, no cracks or delamination was observed by visual inspection after the pull-off test which confirmed robust adhesion and compatibility between the PMMA and AgNWs. Measurements of the sheet resistance before and after showed no discernible difference for the post-processed samples (<5% relative difference). By contrast, for non-processed samples, the sheet resistance increased by 65%, showing that the post-processing increases the adhesion of the conductive coating also.

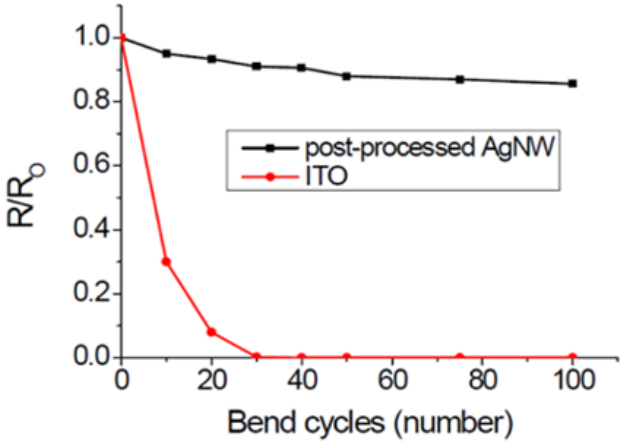


Figure 4.15: Effect of bending on sheet resistance of post processed AgNW and ITO TCE.

The bend testing was performed to demonstrate the enhanced mechanical performance of the post-processed AgNW based electrodes during repeated bending. Under a 100-cycle test with a bending radius of 20mm, almost no effect was observed while dramatic failure appeared in the ITO electrode in the same test. The test shows that the mechanical flexibility of the samples is not affected by the post-processing of the AgNW films as shown in Figure 4.15, where R and $R_0$ represent the sheet resistance of films before and after the bending test, respectively.

## 4.11 XPS Analysis of the AgNW Films

XPS analysis was conducted on the AgNW films to investigate the impact of embossing, $N_2$ plasma treatment and accelerated ageing on the surface chemistry. All XPS measurements were performed at Chester University with the help of Dr. J. Kettle and Prof. G. C. Smith. Surface compositions as determined by XPS are shown in Table 4.10, after correction for the presence of small amounts of silicon found as a surface contaminant. All samples showed high levels of C and O, in most cases relatively strong Ag signals also present. All samples also showed low levels of S, Cl and N. The data in Table 4.10 shows the chemical stoichiometry of the different samples. For a deeper analysis, high-resolution scans were made of the individual photoelectron lines and curve fitted to a known reference data for silver and polymers.

The C1s spectra were typical of those obtained from a poly (methyl methacrylate) PMMA surface, with the hydrocarbon component arising from the backbone and the pendant methyl groups, and the oxygenated components arising from the two carbon-oxygen bonded components of the ester group. The variation in the presence of carbon in

this form indicates that there are different levels AgNW coverage between different samples. Samples that have been embossed show higher levels of carbon surface, indicating they have been submerged into the underlying PMMA.

Table 4.10: Surface composition obtained by XPS, showing the impact of $N_2$ plasma treatment, embossing and ageing upon the chemical changes at the surface.

| Element | As prepared | Thermal embossing | $N_2$ plasma treatment | Thermal embossing and $N_2$ plasma treatment | As prepared and aged | Thermal embossing and $N_2$ plasma treatment and aged |
|---|---|---|---|---|---|---|
| C 1s | 66.66 | 72.92 | 61.73 | 62.31 | 67.42 | 70.95 |
| O 1s | 19.72 | 22.15 | 27.10 | 25.12 | 22.20 | 24.91 |
| Ag 3d | 7.99 | 1.58 | 7.11 | 8.19 | 5.09 | 1.01 |
| S 2p | 1.66 | 0.29 | 1.86 | 2.07 | 2.13 | 0.14 |
| Cl 2p | 1.00 | 0.17 | 0.96 | 0.91 | 0.83 | 0.22 |
| N 1s | 2.97 | 2.89 | 1.24 | 1.40 | 1.79 | 2.32 |
| Na 1s | - | - | - | - | 0.55 | 0.45 |

The levels of Ag did not change significantly upon $N_2$ plasma treatment; however, the embossed samples showed much lower levels of Ag (consistent with the SEM images and Carbon XPS data). Nevertheless, even after thermal embossing, Ag was clearly present at the surface, indicating that the Ag was not fully embedded into the substrate during this processing step. By comparison, the $N_2$ plasma treated sample showed a decrease in the surface concentration of C and an increase in the surface concentration of O compared to the control. We speculate that the $N_2$ plasma removes hydrocarbon impurities from the AgNW films, namely the PVP used in end-capping during the synthesis, and this leads to the reduction in C and the improved electrical properties. This is supported by the reduction in the surface concentration of N after $N_2$ plasma treatment, which is also likely to be due to the removal of PVP. The increase in O content after thermal embossing is likely to be because of the raised temperature in ambient air leading to increased oxidisation.

On all samples, the Ag $3d_{5/2}$ – $3d_{3/2}$ doublets were sharp, intense, symmetrical in shape and typically 1.2 – 1.3 eV in width. In all cases, the binding energy of the $3d_{5/2}$ component was found in the range 368.8 – 369.3 eV, somewhat higher than the internationally-accepted reference value of 368.27 eV for clean metallic silver [200]. In all cases, a doublet separation of 6.02 ± 0.01 eV was found. Ag is unusual among metallic elements in that its oxides tend to give photoelectron peak binding energy shifts to lower binding energy than the metallic state. Here, a shift to higher binding energy is seen. This

is occasionally seen in the presence of alloying elements, but that cannot be the case here. Instead, it is more likely that the shift is due to charge transfer between the nanowires and the (insulating) PMMA/PEN substrates. This would be consistent with the results reported by Lin & Wang [201]and from other studies of deposited Ag layers. It could alternatively be a function of a more tightly bound crystal structure of the Ag in the form of nanowires compared to bulk metal.

Ageing the as-prepared sample cause small increases in the surface concentrations of O, S and C. Ageing of the post-processed sample caused an increase in the surface concentration of C and small reductions in the surface concentrations of the other elements present, except for Ag where a significant reduction from ~8% to ~ 1%, suggesting coverage of the Ag by a carbon-containing material as a consequence of the ageing process.

Sulphur was detected at low levels on all samples, with a possible correlation with the level of Ag (correlation coefficient $r^2 = 0.79$). This is consistent with the reactive nature of Ag to environmental S and the consequent formation of silver sulphides. Inspection of the S 2p photoelectron peaks showed the majority of S present to be in a sulphide state, $S^{2-}$, consistent with AgS. The thermal embossed and aged samples show low levels of S indicating why these samples remain stable. By ensuring a greater proportion of the AgNWs are submerged into the underlying PMMA, they remain less susceptible to environmental ageing.

## 4.12 Summary

This chapter reports the high performing AgNW electrodes. High performance achieved in terms of the low sheet resistance and surface roughness as well as high stability. The process relies upon three sequential steps; thermal embossing, infrared sintering and a nitrogen plasma treatment. This process leads to the demonstration of a conductive film with a sheet resistance of 2.5Ω Ω $sq^{-1}$and 85% transmittance, thus demonstrating the highest reported Figure-of-merit in AgNW TCEs to date (FoM = 933). A further benefit of the processes surface roughness is substantially reduced compared to traditional AgNWs techniques. Accelerated life testing has been applied to show that the process leads to enhanced long-term stability in AgNW films. X-ray photoelectron spectroscopy (XPS) is used to understand the improvement in long-term stability. The overall properties of the transparent electrodes developed show enhanced properties over the incumbent technology; ITO.

# Chapter 5. Development of ZnO TFTs Using Design of Experiments (DOE) Techniques

In this chapter, the development of low voltage metal oxide thin film transistors (TFTs) based upon Zinc Oxide (ZnO) is reported. Firstly, a comprehensive study of the influence of the processing parameters on the performance of anodized $Al_2O_3$ insulating films for ZnO TFTs built is conducted. In particular, a combinational science approach is undertaken in order to provide a rapid methodology to optimize the layer deposition. This approach could provide a step-change for process optimization for researchers in the area of flexible electronics. To accomplish this, 'screening' of the anodization parameters was carried out by using a Plackett–Burman Design (PBD), which enables several parameters to be varied simultaneously, with the reduced number of experiments, enabling identification of the most significant factors which impact the TFT performance. We studied eight different process parameters that influence the performance parameters of ZnO TFTs (mobility, threshold voltage) by using analysis of variance (ANOVA). This procedure could be adopted more widely in flexible electronics to increase the speed of product development.

Taguchi orthogonal array (OA) has then been applied for optimisation of ZnO TFTs performance under different input conditions. In addition to the combinational science approach, a detailed comparative study of sputtered and sprayed ZnO film properties and their impact upon TFT performance has been studied. Further for UV sensing applications UV saturation experiment on ZnO TFTs for both methods of deposition are explained using TFT behaviour on saturation after UV exposure. State of the art performances for sprayed ZnO TFTs mobility of 15.5 $cm^2V^{-1}s^{-1}$ and high on/off ratio of $2.1x10^6$ is achieved and. However, for sputtered TFTs mobility of 1.19 $cm^2V^{-1}s^{-1}$ and on/off ratio of $7.67x10^3$ is achieved. It has been investigated how annealing temperature affects the structural and optical properties of TFTs. The band gap values are evaluated and approximately agrees with that of bulk ZnO at room temperature. However, bandgap ($E_g$) decreases as the annealing temperature increases due to the increase in grain size. AFM images of the samples show that there is an increase in roughness as annealing temperature increases, indicating an increase in grain size. X-ray photoelectron spectroscopy (XPS) is used to understand the root cause of improved electrical performance.

## 5.1 Development of High-k Dielectric ($Al_2O_3$)

Most transistors and ZnO-based circuits operate at relatively high voltage, exceeding 20V. This is a disadvantage for practical low power applications such as for battery powered portable devices that operate at voltages below 5V. To achieve lower operational voltage, optimization of the TFT dielectric layer is necessary. This is not without challenges as the control over the defect density in the dielectric is key to ensure reproducible performances in ZnO-based TFTs. These defects depend on the deposition technique of ZnO but are also highly dependent on the properties of the gate insulator and the quality of the gate insulator/semiconductor interface. A possible way to overcome both challenges is the use of thin layers (<20 nm) of dielectric, with high dielectric constant (> 6). The dielectric must have simultaneously (i) high capacitance per unit area, (ii) low leakage currents to minimize power loss, (iii) low surface roughness to minimize dispersion and thus improve carrier mobility and (iv) a low density of the interfacial trap states to minimize instability of the threshold voltage. Aluminium oxide ($Al_2O_3$) is a high-k dielectric that can be used as the gate material for TFTs. An approach used to deposit high-quality $Al_2O_3$ films is anodization. Importantly, anodization is a self-limiting process as thin film growth occurs in different directions during the process, resulting in pinhole-free, homogenous oxides. In this process, the aluminium layer is normally thermally deposited on substrates which are then immersed in an electrolytic aqueous solution, for example, tartaric acid, and then a constant current is applied at the Al electrode until a pre-determined voltage is achieved, which defines the film thickness. The thickness (t in nm) of the $Al_2O_3$ films is determined by the anodization voltage ($V_A$) during the anodisation process by the relation, $t = c \times V_A$, c being anodization constant of Al and can vary depending on the experimental conditions for the oxide growth [202]. The thickness of dielectric layer was estimated from above relation because $Al_2O_3$ is difficult to measure $Al_2O_3$ underneath part towards Al layer. The chemical equations involving anodisation of aluminium are given below:

$$4Al + 3O_2 \rightarrow 2Al_2O_3 \qquad \text{Eq. 5.1}$$

$$2Al + 3H_2O \rightarrow Al_2O_3 + 3H_2 \qquad \text{Eq. 5.2}$$

where, the formation of $Al_2O_3$ is directly proportional to the amount of water or oxygen molecules in the electrolyte. There is evidence that some excess oxygen is retained in the bulk of $Al_2O_3$, which can promote the tunneling effect which leads to higher leakage current.

For high performing TFTs, the dielectric must possess (i) a large capacitance per unit area, (ii) a low leakage current and (iii) a low surface roughness to minimize carrier scattering, allowing optimal carrier mobility in the transistor channel during accumulation; and (iv) a low interfacial trap density to minimize threshold voltage instabilities.

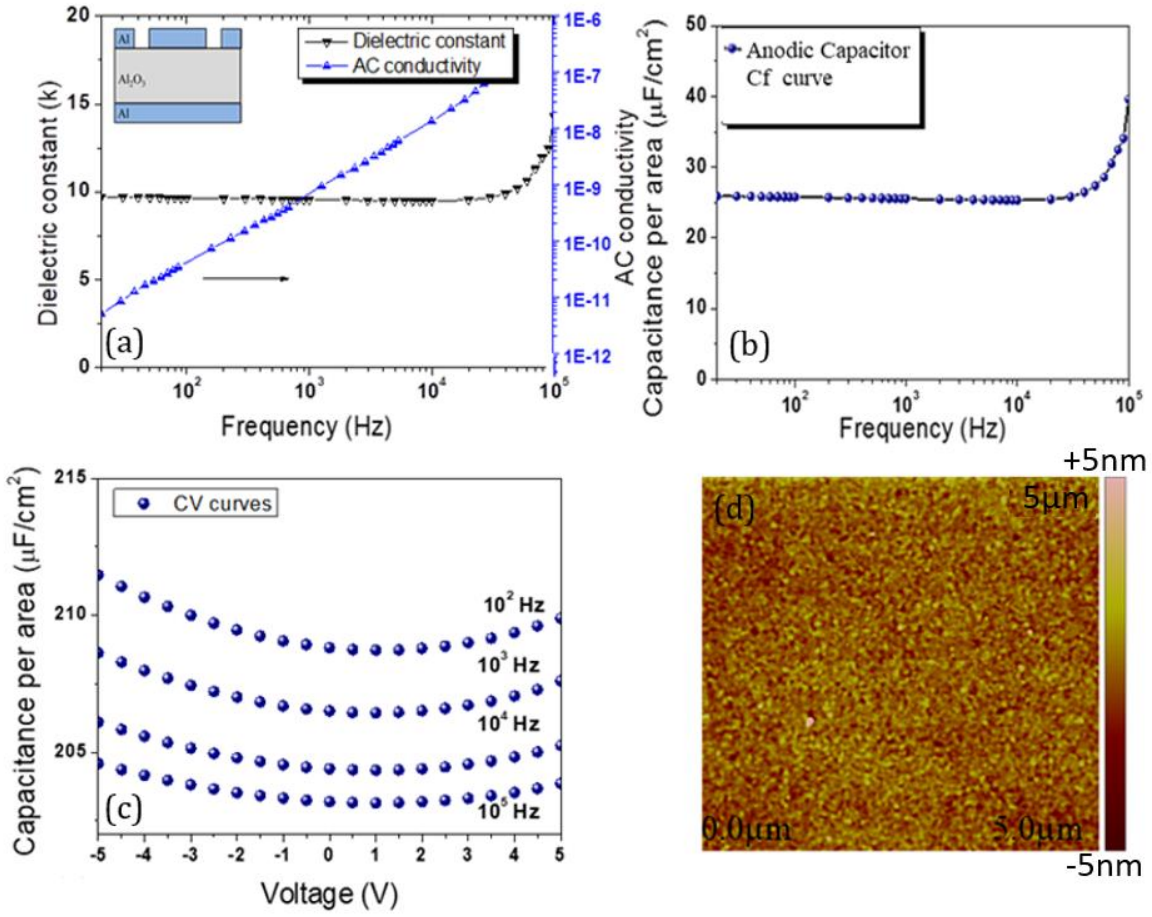


Figure 5.1: (a) Dielectric constant of $Al_2O_3$ and AC conductivity (log scale) versus frequency, (b) C-f curve of the anodic capacitor, (c) C-V curve at different frequencies of the anodic capacitor, (d) AFM image of $Al_2O_3$ gate dielectric layer.

Shown in Figure 5.1(a) are the dielectric constant (K=9.8) of anodic $Al_2O_3$ was calculated from the measured values of capacitance versus frequency in metal insulator metal (MIM) capacitors. The dielectric constant does not vary with the frequency from 20 Hz to 10 kHz, but the ac conductivity increases linearly with an increase in frequency as

shown in Figure 5.1(a). The ac conductivity is related to the energy loss obtained from the polarization mechanism. The increase in ac conductivity can be understood by the equation 5.3.

$$\sigma_{ac}(\omega) = \sigma_{total}(\omega) - \sigma_{dc} = A\omega^{s} \qquad \text{Eq. 5.3}$$

where, ω is the angular frequency, s is the frequency exponent and A is a constant independent of frequency.

Figure 5.1 (b) shows that capacitance is constant over wide range of frequency (20 to 10 kHz). RMS and average roughness of $Al_2O_3$ gate dielectric layer is 0.75 nm, 0.57 nm respectively shown in AFM image in Figure 5.1 (d).

## 5.2 Optimisation of Anodic $Al_2O_3$ using Plackett-Burman Design

The optimisation of anodic $Al_2O_3$ dielectric was performed because in most of the previously reported works no detailed study was carried out for all input factors of anodisation process. In this work, a two-level multivariate analysis based on a Plackett-Burman design has been applied to optimise the fabrication of anodised ($Al_2O_3$) dielectric films for ZnO TFTs. The electrical performance parameters of the devices were measured and Analysis of Variance (ANOVA) of the combined responses has been applied to identify how the $Al_2O_3$ dielectric fabrication process influences the electrical properties of the TFTs. Using this approach, the levels for the manufacturing factors to achieve optimal overall device performance have been identified and the factors which have a higher influence on the device performance parameters have been ranked. The crosschecked analysis of the TFT performance parameters demonstrated that the appropriate control of the anodisation process can have a higher impact on TFT performance than the use of traditional methods of surface treatment of the dielectric layer.

In this work, eight different factors with two levels considered for the anodisation process are listed in Table 5.1. Aluminium films were evaporated onto glass substrates and anodisation process was carried out according to factors and levels are given in Table 5.1. After anodisation, the films were removed from the solution and the impact of post annealing considered; samples were either left to dry at room temperature or annealed at 150 $^0$C for 1 hour. The performance of the $Al_2O_3$ films as a dielectric layer was tested by manufacturing metal-insulator-metal (MIM) capacitor structures and bottom-gate/top-

contact ZnO TFTs. For TFTs, ZnO films were deposited onto the $Al_2O_3$ film by RF sputtering method explained in Chapter 3. The thickness (40nm), as well as the evaporation rate (0.5 Å/s) of the ZnO films, were controlled by a quartz crystal sensor. To complete the transistors and the MIM capacitors, a top layer of aluminium (70 nm) was thermally evaporated through a shadow mask to form a circular electrode, which has a central electrode with 1 mm of diameter surrounded by a concentric ring, with a 400-µm gap. This external ring was grounded, working as a guard ring for the MIM capacitor. The electrical performance of both types of devices (ZnO TFTs and $Al_2O_3$ MIM capacitors) were evaluated for each test run. Fourteen parameters were used for the analysis, which were separated in three different groups: i) parameters for evaluation of the $Al_2O_3$ oxide film, obtained from impedance/capacitance spectroscopy measurements in MIM capacitors and AFM images; ii) parameters obtained from the TFT characterisation curves, associated with the carrier transport in the semiconducting film or at the semiconductor/dielectric interface; and iii) parameters obtained from the source-to-gate current curves, focusing on the quality of the dielectric layer during a TFT measurement.

Table 5.1: Factors chosen for use in the screening test of the two-level factorial factors by the PBD and correspondent values.

| Factors | Factors name | Unit | Low value | High value |
|---|---|---|---|---|
| A | Thickness of Al-layer | nm | 60 | 200 |
| B | Al evaporation rate | Å /s | 5 | 15 |
| C | $H_2O$ content | % | 16 | 30 |
| D | Electrolyte temperature | $^0C$ | 40 | 60 |
| E | pH of the electrolyte | - | 6 | 5 |
| F | Current density | $mA/cm^2$ | 0.45 | 0.65 |
| G | Annealing | C | No | 150 $^0C$ |
| H | Final voltage | V | 30 | 40 |

The first group includes the $Al_2O_3$ dielectric constant (ε), the ac conductivity at low frequencies ($\sigma_{LF}$) and the AC conductivity at high frequencies ($\sigma_{HF}$). As an additional response parameter of the dielectric film quality, the root mean square (RMS) roughness of the anodised surface, determined from atomic force microscopy (AFM) images was considered. The second group comprises the ZnO TFT electron mobility (µ), the threshold voltage ($V_T$), the hysteresis of the transfer curve ($\Delta V_H$), the "off" state current ($I_{off}$), the "on" state current ($I_{on}$) and the on/off ratio ($I_{on}/I_{off}$). The third group used as response parameters the gate current in the depletion state ($I_{dep}$), the gate current in the accumulation state ($I_{acc}$), the voltage of minimal gate current in forward scan ($V_{for}$) and the voltage of minimal gate current in reverse scan ($V_{rev}$). In this thesis, focus on the

response parameters from the second group, which are more important to the TFT performance, was kept.

The design of experiments used for screening the anodisation factors introduced in Table 5.1 is based on a matrix sequence of the twelve runs according a Plackett-Burman design (PBD) presented in Table 5.2 (discussed in Chapter 2). In Table 5.2, the letter L and H refers to the "low value" and "high value" for each process factor, respectively, whereas the letters A to H refers to the anodisation factors. For each experimental run, a set of measurements (TFT curves, AC impedance and AFM) was carried out for an average of eight samples used for each run. It is worth to mention that the combination of experimental runs and their respective low and high levels of the factors specified in Table 5.2 were determined in a way that is possible to apply Analysis of Variance (ANOVA) for screening the most significant ones. Moreover, another characteristic of the PBD matrix in Table 5.2 is its orthogonality, i.e., for each level (high or low) in one factor, there is an even number of "highs" and "lows" for all the remaining factors of the matrix. ANOVA has been used to identify which processing condition of the dielectric layer contributes more significantly to a determined best TFT response parameter (e.g. $\mu$, $V_T$, $I_{on}$, $I_{off}$, $\Delta V_H$, $I_{dep}$).

Table 5.2: Plackett-Burman matrix for 12 runs experiments screening eight factors (A-H).

| Run | A | B | C | D | E | F | G | H |
|---|---|---|---|---|---|---|---|---|
| 1 | L | L | L | L | L | L | L | L |
| 2 | H | L | H | H | L | H | H | H |
| 3 | L | L | L | H | L | H | H | H |
| 4 | H | L | L | L | H | L | H | H |
| 5 | H | H | L | H | H | H | L | L |
| 6 | L | H | L | H | H | H | L | L |
| 7 | H | H | H | L | L | L | H | L |
| 8 | L | L | H | L | H | H | H | H |
| 9 | H | L | H | H | H | L | L | L |
| 10 | H | H | L | L | L | H | L | H |
| 11 | L | H | H | L | H | H | H | L |
| 12 | L | H | H | H | L | L | L | H |

## 5.3 ZnO TFT using anodic $Al_2O_3$ as the gate dielectric

To analyse the results TFT performance parameters were extracted from each test run, which were used as output responses for the Plackett Burman design. Figure 5.2 (a) and (b) show, respectively, the output and transfer curves for a TFT manufactured using Test Run 3 from Table 5.2. Figure 5.2 (b) inset shows a cross-section schematic of the TFT structure used for this work. The $\sqrt{I_{DS}}$ vs. $V_G$ curve is also depicted in Figure 5.2 (b), allowing the evaluation of the TFT mobility ($\mu$) from the slope of the curve and the threshold voltage ($V_T$) from the extrapolation of the linear region to the horizontal axis.

The drain current and saturation mobility was calculated using equations 2.15 and 2.17 as described in Chapter 2 respectively.

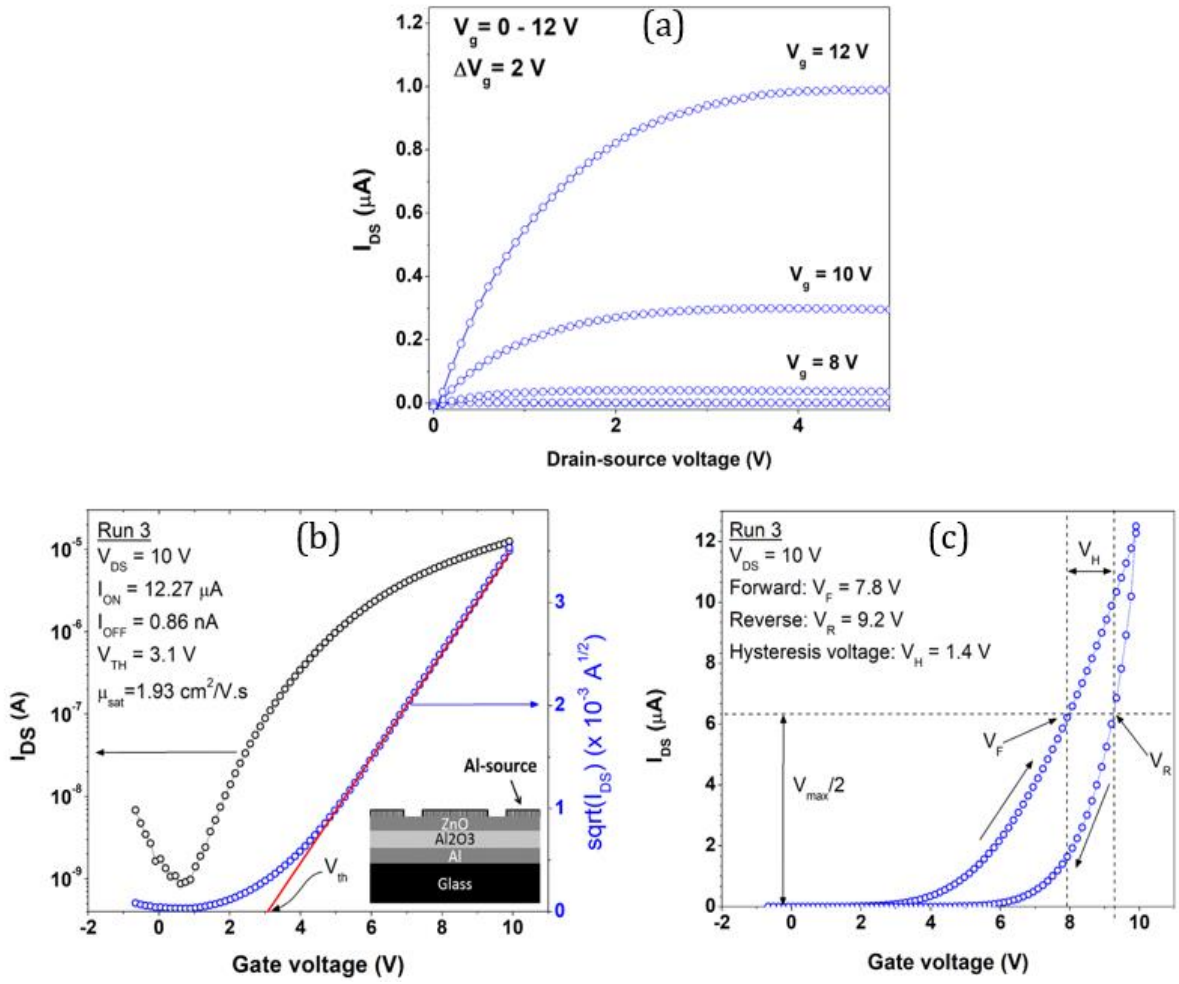


Figure 5.2: a) Output curves sweeping $V_G$ from 0 to 12 V, in of 2 V steps; b) transfer curve and $I_D^{1/2}$ vs. $V_G$ for $V_{DS}$ = +10 V. Inset: schematic of the ZnO TFT structure; c) transfer curve, for $V_{DS}$=10 V, showing the hysteresis between forward and reverse voltage scan; All curves were obtained from a ZnO TFT with anodised $Al_2O_3$ prepared as specified in run 3, Table 5.2.

In Figure 5.2 (c), the transfer curve shows clearly the hysteresis for a device constructed in accordance with Run 3 (where $\Delta V_H$ = 1.5 V).

From the transfer curves for run 3, a mobility of 1.27 $cm^2\ v^{-1}\ s^{-1}$, an on-off ratio of 1.4 $x10^4$ and the threshold voltage of 3.5 V were obtained. The performance parameters, namely, "on" current, "off" current and on/off ratio were defined as the maximum channel current in accumulation, the lowest channel current in depletion, and their ratio, respectively. The TFT transfer curves normally show hysteresis of the channel current ($I_D$) when the voltage at the gate electrode ($V_G$) was swept in forward or in reverse

direction. The evaluation of the hysteresis was undertaken using the method reported elsewhere [203], in which the hysteresis magnitude ($\Delta V_H$) is defined as the voltage difference in the transfer curves, between forward and reverse scan, when the channel current is half of its maximum value.

## 5.4 Influence of the Dielectric Layer Fabrication Factors on the ZnO TFTs Characteristics

To study how variations in the dielectric layer manufacturing process affect the TFT characteristics, we analysed the characterization parameters ($\mu$, $V_T$, $\Delta V_H$, $I_{on}$, $I_{off}$ and $I_{on}/I_{off}$) from TFTs which were built using the same ZnO layer process conditions and different dielectric layers fabricated according to the PBD defined by Tables 5.1 and 5.2. The mean values ($\overline{Y_n}$) and the standard deviation $\bar{s}_n$ values of the TFT response parameters (each run has an average of 8 devices) are presented in Table 5.3. The mean value from all experiments (between-runs) for a particular response is denoted by $\overline{Y_T}$ whereas $s_T$ is the correspondent between-runs standard deviation (SD) of the within-run means. Moreover, $\bar{s}_n$ is the mean of the within-run standard deviation.

Table 5.3: Mean and standard deviation values of response parameters from the performance of ZnO TFTs using anodized $Al_2O_3$ for the 12 experimental runs using PBD method.

| Run | $\mu$ ($cm^2.V^{-1}.s^{-1}$) | | $V_{TH}$ (V) | | $I_{ON}$ ($\mu A$) | | $I_{OFF}$ (nA) | | $I_{ON}/I_{OFF}$ ($x10^3$) | | $\Delta V_H$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{Y_n}$ | $s_n$ | $\overline{Y_n}$ | $s_n$ | $\overline{Y_n}$ | $s_n$ | $\overline{Y_n}$ | $s_n$ | $\overline{Y_n}$ | $s_n$ | $\overline{Y_n}$ | $s_n$ |
| **1** | 1.30 | 0.11 | 4.09 | 0.65 | 4.31 | 1.13 | 5.58 | 0.77 | 0.76 | 0.14 | 3.54 | 0.58 |
| **2** | 0.15 | 0.02 | 0.31 | 1.00 | 1.97 | 0.77 | 0.48 | 0.21 | 4.73 | 2.96 | 3.50 | 0.56 |
| **3** | 1.59 | 0.17 | 3.99 | 0.64 | 3.44 | 0.64 | 1.82 | 0.61 | 2.09 | 0.75 | 2.05 | 0.33 |
| **4** | 0.11 | 0.06 | 3.90 | 0.96 | 2.90 | 0.74 | 0.27 | 0.12 | 12.83 | 6.39 | 1.93 | 0.41 |
| **5** | 0.33 | 0.06 | 2.90 | 0.67 | 3.52 | 0.63 | 0.66 | 0.25 | 6.53 | 3.99 | 2.17 | 0.41 |
| **6** | 0.21 | 0.06 | 3.26 | 0.88 | 3.08 | 0.46 | 0.48 | 0.19 | 7.51 | 3.69 | 2.58 | 0.38 |
| **7** | 0.09 | 0.05 | 2.63 | 0.82 | 0.49 | 0.30 | 0.42 | 0.10 | 1.15 | 0.56 | 4.10 | 0.35 |
| **8** | 0.19 | 0.02 | 2.66 | 0.58 | 0.57 | 0.14 | 0.26 | 0.10 | 2.63 | 1.41 | 4.44 | 0.72 |
| **9** | 0.39 | 0.04 | 2.73 | 0.58 | 2.07 | 0.35 | 0.36 | 0.13 | 6.44 | 2.49 | 2.34 | 0.37 |
| **10** | 0.06 | 0.03 | 3.06 | 1.02 | 0.34 | 0.11 | 0.26 | 0.12 | 1.80 | 1.51 | 4.74 | 0.54 |
| **11** | 0.15 | 0.02 | 4.53 | 1.00 | 0.48 | 0.15 | 0.41 | 0.14 | 1.27 | 0.50 | 1.31 | 0.29 |
| **12** | 0.14 | 0.02 | 3.46 | 1.23 | 0.42 | 0.11 | 0.58 | 0.24 | 0.83 | 0.34 | 6.05 | 0.55 |
| | | | | | | | | | | | | |
| $\overline{Y_T}$ | 0.39 | | 3.13 | | 1.97 | | 0.97 | | 4.05 | | 3.23 | |
| $s_T$ | 0.50 | | 1.09 | | 1.46 | | 1.51 | | 3.69 | | 1.41 | |
| $\bar{s}_n$ | | 0.06 | | 0.84 | | 0.40 | | 0.17 | | 1.46 | | 0.41 |

From Table 5.3, it is possible to qualitatively estimate the influence of the variation on the factors from the comparison of the between-run standard deviation ($s_T$) to the

mean of the in-run standard deviation ($\bar{s}_n$). The value of the between-run standard deviation compared to the total mean of the response also suggests that the manufacturing factors influence the observed response parameters. For instance, focusing on the TFT mobility, the between-runs SD (0.50 $cm^2.V^{-1}.s^{-1}$) is even higher than the total mean value (0.39 $cm^2.V^{-1}.s^{-1}$), and several times higher than the mean in-run SD ($\bar{s}_n$ = 0.06 $cm^2.V^{-1}.s^{-1}$), indicating that factor variation has strong influence on the TFT mobility.

Table 5.4: Ranking of the factor effects considering the TFT mobility response parameter. The corresponding computed sum of squares of the effects, F-value, p-value, significance, percentage contribution, and cumulative contribution of each factor on the effects are also tabulated.

| Response: TFT mobility | | | | | | | |
|---|---|---|---|---|---|---|---|
| Factor | Effect | Sum of squares | F-value | p-value | significant | Contribution (%) | Cumulative contribution (%) |
| H | -0.50 | 0.250 | 1218.8 | < 0.001 | yes | 26.93 | 26.93 |
| B | -0.46 | 0.210 | 1024.3 | < 0.001 | yes | 22.63 | 49.56 |
| C | -0.41 | 0.172 | 834.8 | < 0.001 | yes | 18.45 | 68.01 |
| A | -0.41 | 0.167 | 813.1 | < 0.001 | yes | 17.97 | 85.98 |
| E | -0.32 | 0.104 | 507.5 | < 0.001 | yes | 11.21 | 97.19 |
| D | 0.16 | 0.024 | 118.2 | < 0.001 | yes | 2.61 | 99.81 |
| F | 0.04 | 0.002 | 7.5 | 0.0077 | no | 0.16 | 99.97 |
| G | -0.02 | 0.000 | 1.4 | 0.2482 | no | 0.03 | 100.00 |

To understand if the manufacturing factors have a statistically significant impact upon the quality of the dielectric layer, ANOVA calculations were performed considering the response parameters obtained from all samples in all experimental run. The calculated effects from all sources of variation (factors) on the TFT mobility, the sum of squares and the percentage of contribution are presented in Table 5.4, showing the ranking of the factors considering the effect on the TFT mobility. Six factors (H, B, C, A, E, and D) are significant within the confidence interval. However, as a convention, we decided to consider as relevant only factors whose contribution to the effect is superior to the fraction correspondent to a uniform distribution among all the 8 factors (i.e., superior to 12.5%). This criterion was used to discriminate the factors which contribute more to the effect of factors, which, even though are significant, contribute less to the observed effect. Factors F and G were found to be non-significant, which means that the

calculated effect of these parameters on the mobility could not be distinguished from noise. The factors which contribute most to the TFT mobility are (in rank order): the final voltage for the anodization process, the Al-evaporation rate, the electrolyte water content, and the thickness of the Al layer. All these factors presented a negative effect on the mobility, which means that when the factor is set on the "high" value, a decrease in the TFT mobility was observed.

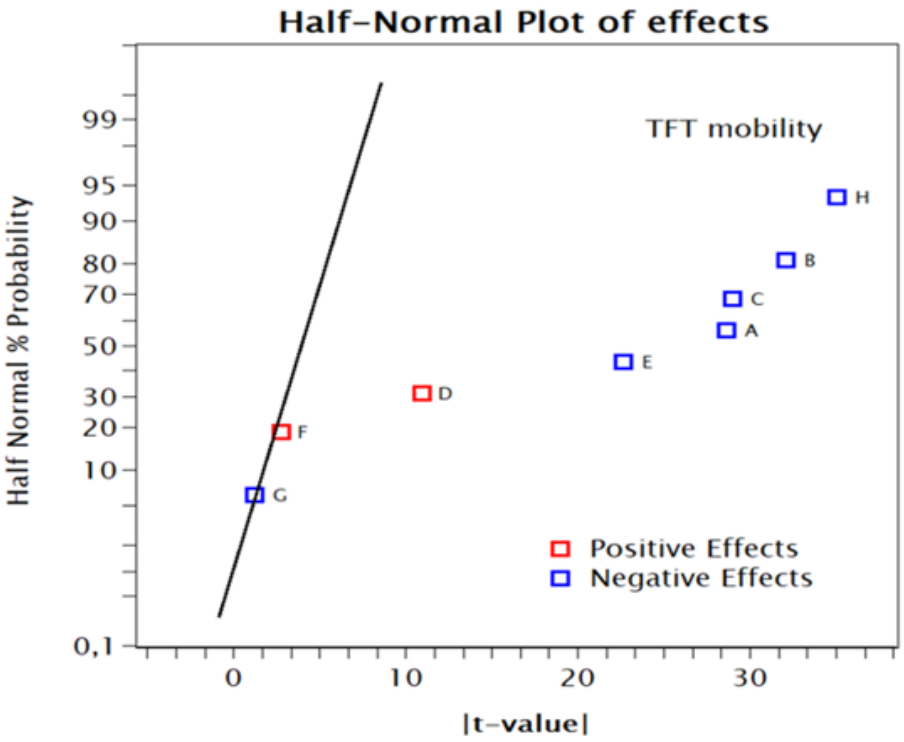


Figure 5.3: Half Normal Plot of effects using the TFT mobility as the response parameter.

The corresponding half-normal plot for the absolute effects is also shown in Figure 5.3. The half-normal plot highlights that the factors H, B, C, A, E and D does not follow the normal distribution, considering a confidence interval of 99% (*p*-limit of 0.01). For the considered number of degrees of freedom and confidence interval, the t-value (defined as the square root of the F-ratio from equation 1) limit is 2.642. The vertical axis of Figure 5.3 is in "probability scale", which represents the inverse of a cumulative Gaussian distribution, that is, Y′= norminv(Y/100). The function norminv($x_p$) computes the deviate $x_p$ associated with the given lower tail probability p(0.01, in the present case) of the standardized normal distribution. $x_p$ is calculated for the given p such that.

$$p = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_p} e^{-u^2/2}\, du \quad for -\infty < x_p < \infty \qquad 5.4$$

Therefore, the cumulative Gaussian distribution is represented by the straight line of Figure 5.3. Factors distancing the cumulative Gaussian distribution contribute to the rejection of the null hypothesis (H0).

To discriminate the effects by varying the different manufacturing factors, we performed ANOVA on all the results, leading to the Pareto charts of effects presented in Figure 5.4. In these charts, the most significant factors are ranked and the threshold limit of significance (p = 0.01) is represented by a vertical dashed line. A factor in which absolute effect surpasses the p-limit is considered significant.

The effect of a factor upon a response parameter is defined as positive (negative) if the response presents an absolute increase (decrease) by changing the factor level from "low" to "high". Colours are used to distinguish if the effect is negative or positive in the Pareto charts of Figure 5.4. The Pareto charts show that several factors influence each response parameter considering a confidence interval of 99%. For the "off" current, all factors were found to be significant, whereas 7 factors were significant for both the mobility and the on-off ratio, 6 factors for the hysteresis, 5 factors for the "on" current, and 4 factors for the threshold voltage. Moreover, the factors ranking and effect sign (positive or negative) change considerably among the observed responses. For improved factor screening, we considered only the factors, which have a higher relative contribution to each response parameter, as described before during the analysis of Figure 5.3 and Table 5.4.

The anodization current density (factor F) is not among the most relevant factors in any of the cases, and the annealing treatment (factor G) and the electrolyte temperature (factor D) appear just once each among all cases, having smaller contributions to the observed effects. Table 5.5 also presents the sign of the influence of the factor (positive or negative) on the effect for each response, indicating the sign of the effect for a particular factor value ("high" or "low").

The final voltage (H) is directly associated to the thickness of the $Al_2O_3$ and it is expected that the higher the thickness, the lower the TFT mobility, "on" current and "off" current because of the lower electric field at the semiconductor/dielectric interface; this is supported by the data obtained in Table 5.5.

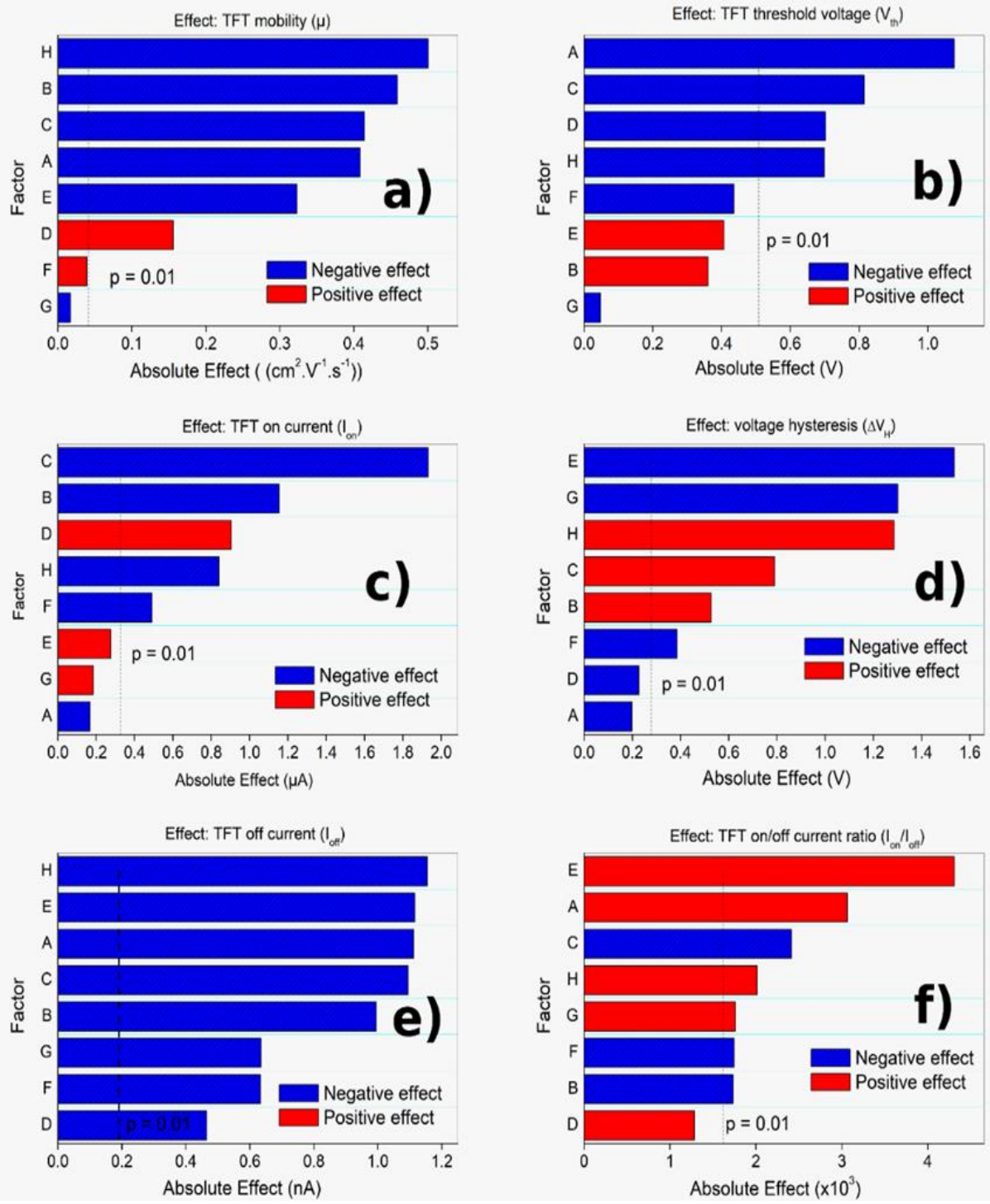


Figure 5.4: Pareto charts of the absolute effects on a) TFT mobility; b) TFT threshold voltage; c) voltage hysteresis; d) TFT "on" current; e) TFT "off" current; f) TFT on/off ratio.

The results are presented in Table 5.5, where the percentage contribution and the cumulative contribution from the most significant factors are computed. Considering as relevant the factors whose relative contribution to the effect is superior to 12.5%, we notice a better screening of the manufacture factors (cells highlighted in yellow on Table

5.5). The exception is the threshold voltage, which has 4 significant factors and still has 4 relevant factors, summing up a cumulative contribution superior to 85%.

Table 5.5: Relative Contribution to the Effects and Cumulative Relative Contribution from the Manufacture Factors Considering the (i) TFT Mobility, (ii) TFT Threshold Voltage, (iii) Voltage Hysteresis, (iv) TFT "On" Current, (v) TFT "Off" Current, and (vi) TFT On-Off Ratio as the Response Parameters.

| Response: carrier mobility | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| - | y | H | 26.93 | 26.93 |
| - | y | B | 22.63 | 49.56 |
| - | y | C | 18.45 | 68.01 |
| - | y | A | 17.97 | 85.98 |
| - | y | E | 11.21 | 97.19 |
| + | y | D | 2.61 | 99.81 |
| + | n | F | 0.16 | 99.97 |
| - | n | G | 0.03 | 100.00 |

| Response: threshold voltage | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| - | y | A | 35.26 | 35.26 |
| - | y | C | 20.17 | 55.42 |
| - | y | D | 14.98 | 70.40 |
| - | y | H | 14.80 | 85.21 |
| - | n | F | 5.76 | 90.97 |
| + | n | E | 5.02 | 95.98 |
| + | n | B | 3.95 | 99.93 |
| - | n | G | 0.07 | 100.00 |

| Response: TFT channel "on" current | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| - | y | C | 53.59 | 53.59 |
| - | y | B | 19.12 | 72.71 |
| + | y | D | 11.72 | 84.44 |
| - | y | H | 10.13 | 94.56 |
| - | y | F | 3.46 | 98.02 |
| + | n | E | 1.09 | 99.11 |
| + | n | G | 0.49 | 99.60 |
| - | n | A | 0.40 | 100.00 |

| Response: TFT channel "off" current | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| - | y | H | 18.97 | 18.97 |
| - | y | E | 17.72 | 36.70 |
| - | y | A | 17.62 | 54.31 |
| - | y | C | 17.08 | 71.39 |
| - | y | B | 14.09 | 85.48 |
| - | y | G | 5.74 | 91.21 |
| - | y | F | 5.71 | 96.92 |
| - | y | D | 3.08 | 100.00 |

| Response: TFT on/off ratio | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| + | y | E | 38.17 | 38.17 |
| + | y | A | 19.30 | 57.47 |
| - | y | C | 11.98 | 69.45 |
| + | y | H | 8.35 | 77.80 |
| + | y | G | 6.38 | 84.18 |
| - | y | F | 6.27 | 90.45 |
| - | y | B | 6.16 | 96.62 |
| + | n | D | 3.38 | 100.00 |

| Response: transfer curve hysteresis | | | | |
|---|---|---|---|---|
| | | Factor | Contribution (%) | Cumulative Contribution (%) |
| - | y | E | 34.44 | 34.44 |
| - | y | G | 24.75 | 59.20 |
| + | y | H | 24.14 | 83.34 |
| + | y | C | 9.11 | 92.45 |
| + | y | B | 4.05 | 96.50 |
| - | y | F | 2.17 | 98.67 |
| - | n | D | 0.75 | 99.43 |
| - | n | A | 0.57 | 100.00 |

| | | | |
|---|---|---|---|
| + | positive effect | A: Thickness of Al-layer | E: pH of the electrolyte |
| - | negative effect | B: Al-evaporation rate | F: Current density |
| y | significant fator | C: Water content | G: Annealing |
| n | non-significant factor | D: Temperature of electrolyte | H: Final voltage |
| | contribution > 12.5% | | |

Hickmott reported that the maximum amount of charges introduced into the $Al_2O_3$ layer during the anodization process can be more than 100 times larger when aqueous electrolytes are used [204]. The effect of $H_2O$ content in the electrolyte can be explained by considering the equations 5.1 1nd 5.2 used to describe the $Al_2O_3$ growth onto metallic

Al in section 5.2. While water residue is likely to be present on the surface, some water molecules or oxygen atoms can also be trapped in the $Al_2O_3$ bulk, creating defects that affect the electrical properties of the oxide layer, as well as the oxide surface roughness.

Conduction in the TFT channel initiates when the gate electric field at the interface induces the filling of gap states, moving the Fermi level closer to the conduction band and increasing the charge carrier concentration. Therefore, for voltages below $V_T$, most of the charge carriers are in localized states and the transport is dominated by hopping, which results in low mobility values. The threshold voltage itself is mainly influenced by the presence of shallow states in the bandgap, which is affected by the thickness of the dielectric layer and the oxide dielectric constant. Moreover, the higher density of traps resulting from a thicker dielectric layer can be also responsible for the observed higher transfer curve hysteresis. The water content (C) in the electrolyte causes a higher $Al_2O_3$ surface roughness, which causes more carrier scattering at the dielectric interface, leading to lower mobility, as well as "on" current and "off" current. The lower threshold voltage for higher water content may be because most of the defects formed in the dielectric layer are due to dipoles and not to charged states.

The Al-layer thickness (A) and the Al-evaporation rate (B) are also factors which affect the anodized oxide layer morphology and conductivity in such a way that the higher these factors, the lower are the TFT mobility and "on" current (higher carrier scattering at the interface) and the "off" current (lower channel intrinsic current, probably to defect states). The data in Table 5.5 also indicates that the pH of the electrolyte (E) impacts negatively the transfer curve hysteresis, denoting that, for slower $Al_2O_3$ deposition rates (a more conductive electrolyte results in slower oxide growth), less charge traps are formed at the TFT semiconductor/dielectric interface. Hysteresis originates from the delay in releasing charges from traps. During the forward sweep of VG, traps with energy lower than the Fermi level are filled. During the reverse sweep, however, the charges are not released from the traps immediately, shifting the transfer curve compared to forward sweep. Therefore, interface states and traps in the bulk can be considered the main cause of hysteresis.

Factor E (pH of the electrolyte) is also the most important contribution to the TFT on/off ratio. Considering that both the "on" and "off" currents are negatively affected by the pH of the electrolyte, one concludes that the decrease of the "off" current is higher than the decrease of the "on" current, causing an increase on the on/off current ratio when

the factor is at its "high" level. A similar reasoning can be applied to explain why factor A (Al-film thickness) has a positive impact on the on/off ratio, despite its negative impact on both the TFT "on" and "off" currents. Another factor that has a high negative contribution to the transfer curve hysteresis (and, consequently to the charge traps density) is the annealing of the $Al_2O_3$ films before the ZnO sputtering. The substrate annealing promotes the desorption of adsorbed species (molecular oxygen, moisture, etc.) to the dielectric layer surface which can cause charge trapping at the semiconductor/dielectric interface during transistor operation.

## 5.5 ZnO TFT Overall Performance

A useful purpose of this work would be to identify the impact of the process factors on the overall performance of the ZnO TFTs. To analyse the effects of the manufacturing process, it is necessary to identify targets for each response parameter. We considered that, for the mobility, the "on" current and the on/off ratio, the best response is the highest value as possible, whereas, for the threshold voltage, the "off" current and the hysteresis, the best response is as low as possible. Using this criterion, Table 5.6 has been constructed, where the most appropriate target level (only H or L) was selected for each response. For each TFT response parameter, as different process factors could potentially lead to an optimized response, a method to identify the optimal process factor was needed. Therefore, we considered as a major criterion the highest number of occurrences of each target level, as observed, for instance, for factor A in Table 5.6 (3× H vs 1× L, resulting in a target level H). However, for factor H (final voltage), each target level occurs twice, requiring the use of a second criterion. We considered the highest sum of the percentage contribution of factor H to each response parameter (which can be obtained from Table 5.5), resulting in a target level L for factor H. As a result, the factor levels have an optimal combination of transistor performance in the last row of Table 5.6 shown below.

It can be clearly seen that that factor F (current density) does not contribute significantly to the overall TFT performance and can be ignored, even though ANOVA showed initially that it was significant for some response parameters. The scores of the factors for all parameters studied, calculated by ANOVA, are summarized in Table 5.7. The lines of the Table are organized by separating the manufacturing factors in three different groups: (i) factors prior to the anodization step (the Al layer thickness and evaporation rate), (ii) factors directly associated with the anodization process ($H_2O$ content, temperature of the electrolyte, pH of the electrolytic solution, current density and final

voltage), and (iii) the postprocessing factors: in this case just the "annealing" step. Each cell of the Table representing a significant factor (based upon the 12.5% relative contribution stated before) contains a number which represents the ranking of the factor influence on the associated response parameter.

Table 5.6: Optimal Choice for the Level of Each Manufacturing Factor Considering the Individual Responses and the Overall Optimized Performance Considering the Six Response Parameters from the TFT Transfer Curve[a]

| | FACTORS | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| RESPONSES | A | B | C | D | E | F | G | H |
| Mobility | H | L | L | n | n | n | n | L |
| Threshold Voltage | L | n | H | H | n | n | n | H |
| On current | n | L | L | n | n | n | n | n |
| Off current | H | H | H | n | H | n | n | H |
| On/off ratio | H | n | n | n | H | n | n | n |
| hysteresis | n | n | n | n | L | n | H | L |
| | | | | | | | | |
| Optimum value | H | L | H | H | H | n | H | L |

[a] Yellow cell with a "n" indicates that the factor influence can be neglected.

The scores of the factors for all parameters studied, calculated by ANOVA, are summarized in Table 5.7. The lines of this table are organized by separating the manufacturing factors in three different groups: (i) factors prior to the anodization step (the Al layer thickness and evaporation rate), (ii) factors directly associated to the anodization process ($H_2O$) content, temperature of the electrolyte, pH of the electrolytic solution, current density and final voltage), and (iii) the postprocessing factors: in this case just the "annealing" step. Each cell of the table representing a significant factor (based upon the 12.5% relative contribution stated before) contains a number which represents the ranking of the factor influence on the associated response parameter.

From Table 5.7, it is possible to identify that factors F and G (current density and annealing, respectively) are the factors that have the lowest overall impact upon performance considering all TFT response parameters. On the other hand, factors A, C, and H (Al-film thickness, $H_2O$ content in the electrolyte, and final voltage, respectively) are the factors, which have the highest impact on the overall performance. To rank the factors which impact most the overall performance, we can consider two criteria: (i) the

number of times each factor appears as significant in Table 5.7 and (ii) the lowest sum of the order of significance in each line of Table 5.7. According to the first criterion, factors A, C, and H are tied. However, by the second criterion, factor H (final voltage) is the most relevant factor, since it has the lowest sum of the order of significance. Factors A and C are still tied by such criterion. Moreover, factor H affects most TFT mobility, which is commonly attributed as the most important TFT performance parameter. Therefore, Table 5.7 can be used to determine which process factors are the most important to the device performance, and which ones have a lower effect or can be neglected, in the case of the need of a full factorial DOE (when the interactions of the factors play an important role in the response parameters).

Table 5.7: Comparative Table of the Significance Scores of Process Factors Considering All Studied Response Parameters[a]

| PARAMETERS | | | $\mu$ | $V_{th}$ | $I_{on}$ | $I_{off}$ | $I_{on}/I_{off}$ | $\Delta V_H$ |
|---|---|---|---|---|---|---|---|---|
| I) | Thick Al layer | A | 4 | 1 | | 3 | 2 | |
| | Al Evap. Rate | B | 2 | | 2 | 5 | | |
| | | | | | | | | |
| II) | $H_2O$ content | C | 3 | 2 | 1 | 4 | | |
| | Temp.Electrolyte | D | | 3 | | | | |
| | pH Electrolyte | E | | | | 2 | 1 | 1 |
| | Current density | F | | | | | | |
| | Final voltage | H | 1 | 4 | | 1 | | 3 |
| | | | | | | | | |
| III) | Annealing | G | | | | | | 2 |
| | | | | | | | | |

| | |
|---|---|
| I) Pre-anodisation factors<br>II) anodisation factors<br>III) post-anodisation factor | Negative factor<br>Positive factor |

[a] The number in each cell represents the order of significance found by ANOVA for the respective pair of factor and parameter. Only factors that presented relative contribution superior to 12.5% were considered.

## 5.6 Optimisation of Sputter Coated ZnO TFTs using Taguchi OA

The Plackett Burman approach was useful for optimisation of the anodisation process as there were many factors influencing the performance. Taguchi orthogonal array L9 ($3^4$) was also used to optimize the ZnO TFT manufacture process parameters via the design of experiment (DOE). Taguchi method was used because a smaller number of factors are

needed to optimise the ZnO TFTs manufacture process with greater non-linearity as factors are changed and moreover, it gives better accuracy.

The Taguchi OA factorial settings and properties of factors shown in Table 5.8. Four factors (ABCD) and three level (1,2,3) Taguchi design was selected for estimating the effect of different factors; A= sputter rate (0.5 Å/s, 1 Å/s, 2 Å/s), B = Temperature of post annealing (0 $^0$C, 250 $^0$C, 450 $^0$C), C = Thickness of ZnO active layer ( 20nm, 40nm, 60nm), D =Environment of annealing (D = 100 % $N_2$, 50 % $N_2$and D = in air) on response parameters like mobility, threshold voltage, on-off drain current of ZnO TFTs.

Table 5.8: Taguchi OA Factorial settings and properties of RF sputtering, annealing process factors.

| Abbreviation | Name | Units | Type | Number of Levels | OA Column Index | Level 1 (Low) | Level 2 | Level 3 (High) |
|---|---|---|---|---|---|---|---|---|
| A | Sputter rate | Å/s | Quantitative | 3 | 1 | 1 | 2 | 3 |
| B | Annealing | $^0$C | Quantitative | 3 | 2 | 1 | 2 | 3 |
| C | Thickness | nm | Quantitative | 3 | 3 | 1 | 2 | 3 |
| D | Environment | NA | Quantitative | 3 | 4 | 1 | 2 | 3 |

Shown in Table 5.9 the Taguchi orthogonal array L9 ($3^4$) with 9 runs. Run is the experiment number performed for Optimisation of process parameters.

Table 5.9: Taguchi OA $L_9$ ($3^4$) showing 9 experiment runs with 4-factors and 3-levels.

| $L_9$ ($3^4$) Orthogonal array | | | | | |
|---|---|---|---|---|---|
| Run Number | Factors | | | | Performance parameter |
| | A | B | C | D | Mobility |
| 1 | 1 | 1 | 1 | 1 | 0.01 |
| 2 | 1 | 2 | 2 | 2 | 0.22 |
| 3 | 1 | 3 | 3 | 3 | 0.23 |
| 4 | 2 | 1 | 2 | 3 | 0.07 |
| 5 | 2 | 2 | 3 | 1 | 0.20 |
| 6 | 2 | 3 | 1 | 2 | 0.30 |
| 7 | 3 | 1 | 3 | 2 | 0.11 |
| 8 | 3 | 2 | 1 | 3 | 0.14 |
| 9 | 3 | 3 | 2 | 1 | 0.37 |

## 5.6.1 Pareto Chart and Term Effects for Mobility

Shown in Figure 5.5 (a) is the Pareto chart showing the impact of changes in the input process factors on mobility. The thick blue line indicates the threshold value of the significance test. If the term effect is greater than the significant level, the factor is deemed significant. The factors lower than the significance level, the noise in the experiment is as greater as the effect of changing the factor, so it isn't considered as significant. It can be

clearly observed from this plot that annealing at 450 $^0$C (B[3]) is most significant factor causing increase in mobility of ZnO TFTs. This is because post annealing removes physical defects, such as sputter damage, and stabilizes the oxygen concentration.

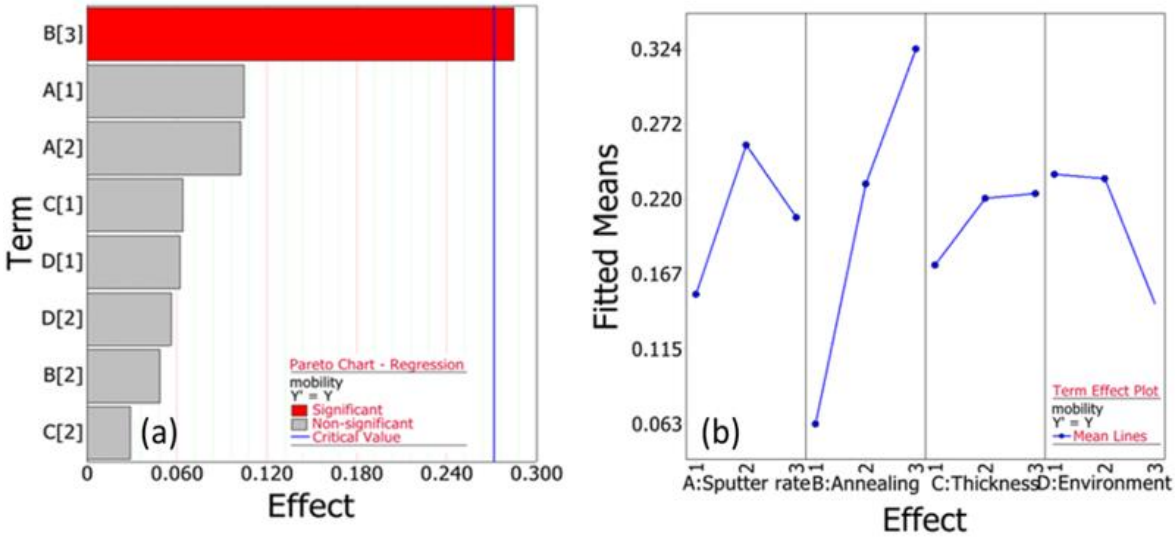


Figure 5.5: Pareto chart regression for (a) mobility, (b) Term effect plot for mobility.

It can be seen from Figure 5.5 (b) that there is an increase in mobility from lower sputter rates (0.5 to 1 Å/s-better uniformity). However, at a high sputter rate of 2 Å/s the mobility falls due to non-uniformities and higher amorphous nature of the deposited active layer. The structure and morphology of the ZnO films are dependent on temperature, gas flow rate and time of annealing. High temperature annealing larger then than 400 $^0$C led to bigger grain size and better crystallinity. The significance of the effect of annealing on the increase in the saturation mobility can be seen in Figure 5.5 (b). Maximum mobility of 0.37 $cm^2\ V^{-1}\ s^{-1}$ at 450 $^0$C was achieved due to better crystallinity of ZnO film caused by post annealing. Moreover, annealing treatment minimizes the crystalline defects, and hence, enhances the field effect mobility.

Also, it can be observed from the term effect plot that with the increase in channel thickness mobility increases. This is due to an enhancement in the crystalline quality and channel conductance of the ZnO films as the channel thickness increased.

Annealing under 100 % $N_2$ atmosphere was performed and it can be seen from Figure 5.5 (b) that mobility under this environment is the highest. This is because nitrogen is inert and reacts with virtually nothing under the conditions used for semiconductor processing. Since the nitrogen is a non-reactive gas (neutral) that does not participate in any oxidation or reduction reactions, the trap states at the interface were minimised.

Overall, the results show that post annealing in the inert environment leads to better performance of ZnO TFTs and thus is the most important factor to control during the fabrication.

## 5.7 Comparison of Sprayed and Sputtered ZnO TFTS

In this section comparative study of sputtered and solution-processed ZnO films and the impact upon TFT performance is descried. Sprayed TFTs on $SiO_2$ substrates were manufactured by Prof. Lucas Fugikawa Santos group in UNESP, Brazil and all testing was carried out at Bangor University. Sputtered TFTs on $SiO_2$ substrates were manufactured at Bangor based on Taguchi OA optimisation process. This work focuses on comparing spray and sputtered ZnO TFTs, differences in the microstructure and chemical composition are studied and reasoning for these discrepancies is given based on XPS analysis of the ZnO films.

### 5.7.1 Optical Spectroscopy of ZnO Films

In this section optical properties of the ZnO films deposited from sputtering and spray deposition are compared. A Tauc plot provides means for determining the optical band gap ($E_g$) in ZnO and can be used to understand if different processing routes and annealing temperatures impact on the $E_g$, which is shown in Figure 5.12. The optical band gap values were obtained by extrapolating the linear part of the curves in Figure 5.12 (a) and (b) with the intercept of this linear part with the x-axis. The absorption coefficient (α) can be expressed by applying the Tauc model in the high absorption region, equation (5.5) [205].

$$(\alpha h\nu)^2 = A(h\nu - E_g) \qquad \text{Eq. 5.5}$$

Figure 5.6 (a), (b) shows the plot of $(\alpha h\nu)^2$ versus photon energy ($h\nu$) for sputtered and spray coated ZnO films, respectively with the calculated values of $E_g$ summarised in Table 5.10. It is apparent that annealing and processing conditions only moderately affect the film's optical bandgap but that spray coated films possess a lower optical bandgap than sputtered ones. The value of bandgap energy ($E_g$) agrees approximately with the room temperature bandgap of ZnO (3.3 eV) [206][207]. The decrease in optical $E_g$ with increasing annealing temperature can be attributed to improvements in the atomic structure order which also results in bandgap narrowing; a

view supported by Jeon *et al* [208]. Based upon the data in Table 5.10, it is plausible to state that large improvements in atomic structure can be obtained from the annealing of sputter deposited films than spray coated ones by annealing.

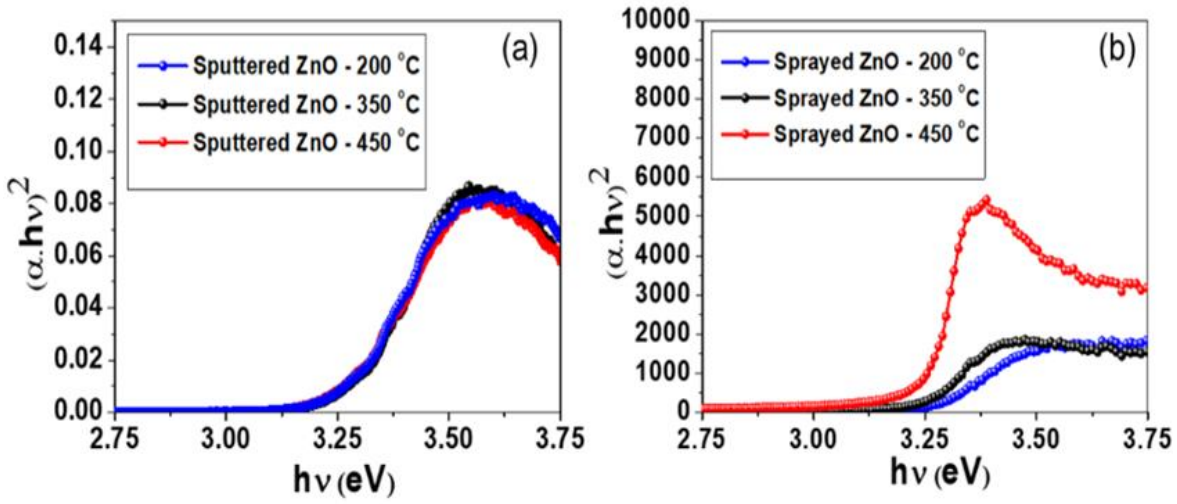


Figure 5.6: Plot of $(\alpha h\nu)^2$ versus photon energy ($h\nu$) of ZnO film with different annealing temperatures (a) Sputtered ZnO film and (b) Sprayed ZnO film.

Table 5.10: Band gap energy, $E_g$ of the ZnO films at different annealing temperatures for sputtered and sprayed samples.

| Annealing Temperature [$^0$C] | Bandgap energy Sputtered [eV] | Bandgap energy Sprayed [eV] |
|---|---|---|
| 200 | 3.30 | 3.28 |
| 350 | 3.28 | 3.26 |
| 450 | 3.26 | 3.25 |

## 5.7.2 Atomic Force Microscopy of ZnO Films

The surface properties of ZnO films were investigated using Atomic Force Microscopy (AFM). AFM topography image analysis reveals that smoother films are achieved when they are deposited by sputtering at room temperature, as confirmed in Figure 5.7. However, there is a very small increase in roughness at the higher temperatures of annealing for both sputtered as well as spray deposited films. The surface roughness of the films was evaluated in terms of root mean square ($R_q$), average ($R_a$) and peak to valley ($R_{max}$) and are shown in Table 5.11. This small increase in roughness can be attributed to increases in grain sizes, which can be verified from the AFM images in Figure 5.7. It appears that as the temperature of the substrate is increased, particularly for values greater than 200 $^0$C, there is a tendency for ZnO to form larger crystallites, resulting in a more irregular surface. The dynamics and the irregularity of the size of the drops from

solution sprayed onto substrate also contributing to increase in roughness due to the low homogeneity in the distribution of the drops sprayed along the substrate [174].

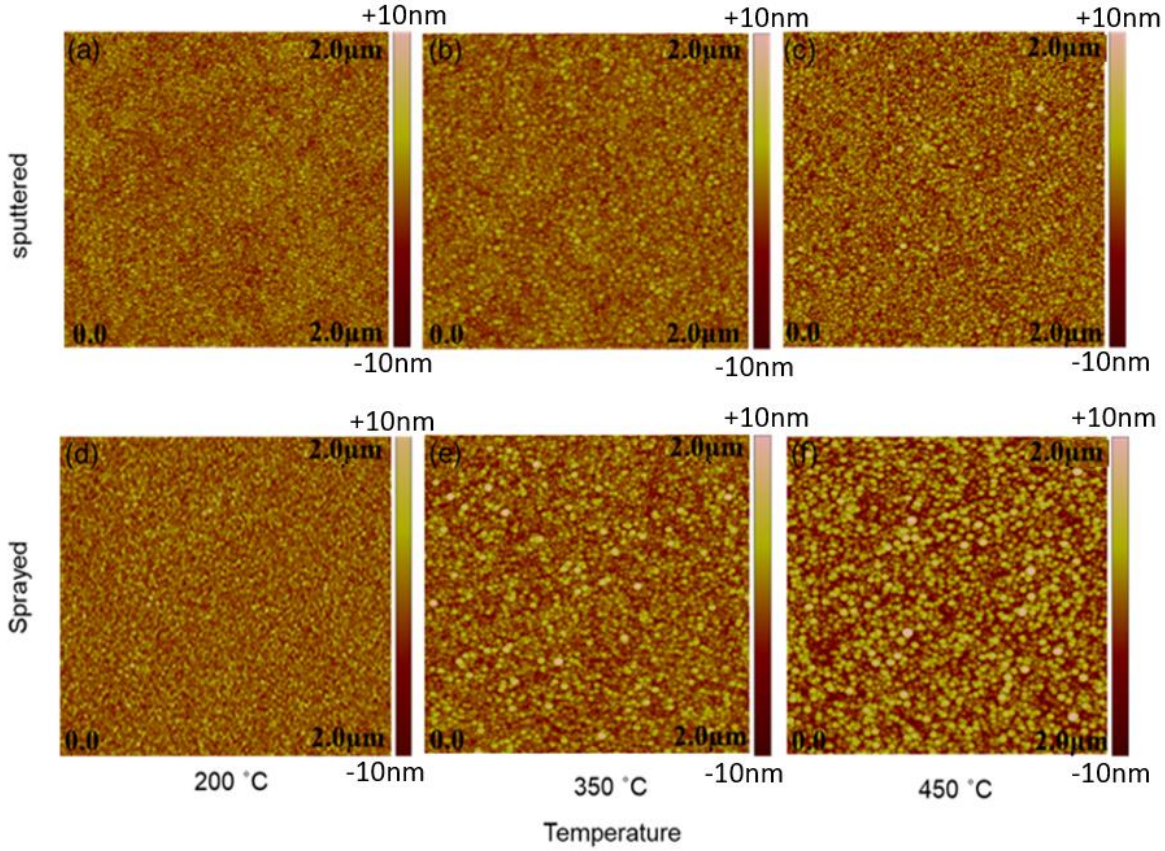


Figure 5.7: (a), (b), (c) sputtered AFM topography images of sputtered and (d), (e), (f) sprayed ZnO films annealed at different temperatures shown above.

Table 5.11: Surface roughness parameters of sprayed and sputtered active layers of ZnO TFTs measured from an average of 6 samples.

| Annealing | Sprayed Roughness Parameters | | | Sputtered Roughness Parameters | | |
|---|---|---|---|---|---|---|
| Temperature [°C] | $R_q$ [nm] | $R_a$ [nm] | $R_{max}$ [nm] | $R_q$ [nm] | $R_a$ [nm] | $R_{max}$ [nm] |
| 200 | 1.43 | 1.09 | 14.3 | 0.60 | 0.48 | 5.30 |
| 350 | 1.51 | 1.15 | 14.6 | 0.62 | 0.49 | 5.40 |
| 450 | 1.96 | 1.55 | 17.6 | 0.74 | 0.56 | 11.15 |

## 5.7.3 X-Ray Diffraction of ZnO Films

X-Ray diffraction (XRD) has been used to analyse the differences between the microstructures of spray and sputtered samples. In Figure 5.14, the XRD scans for the higher temperature samples which were annealed at 350 $^0$C temperature to 450 $^0$C are shown. The XRD patterns show substantially different diffraction patterned with a single prominent peak in the case of sputtered films.

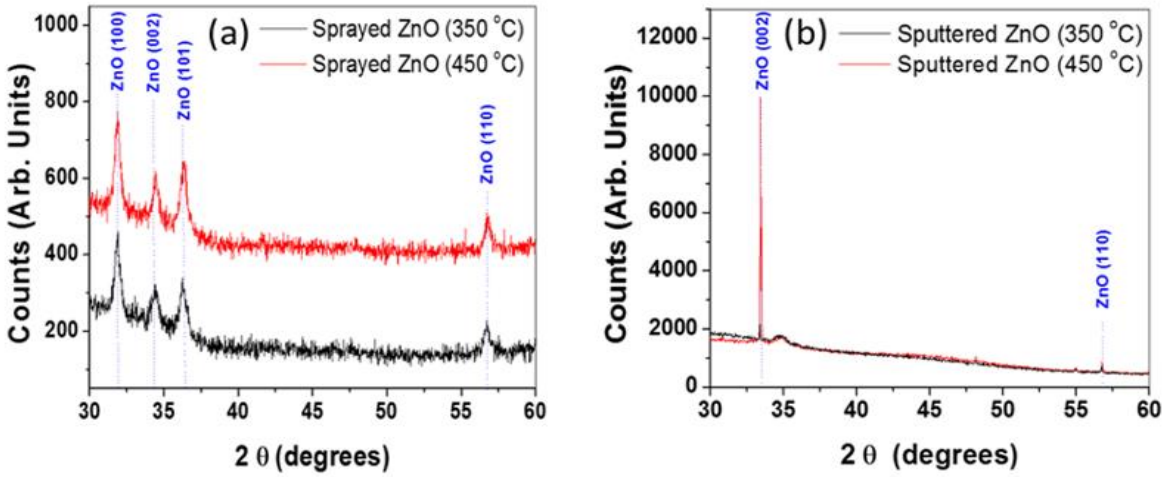


Figure 5.8: (a) Sputtered and (b)sprayed ZnO films diffraction patterns annealed at different temperatures shown above.

For the case of the spray coated films, four diffraction peaks are present which corresponds to the planes (100), (002), (101) and (110), indicating the presence of film crystallites with different orientations. In the case of spray coated samples, the intensity of these peaks increases as the annealing temperature increases, thus indicating that the crystallinity of the film was improved. Average crystallite size obtained using Scherrer equation (5.6) [209] 14.88 nm for 300 $^0$C and 17.32 nm for 450 $^0$C for sprayed samples and 11.67 nm for 300 $^0$C and 13.72 nm for 450 $^0$C for sputtered samples.

$$d = \frac{0.9\lambda}{B\ cos\theta} \qquad \text{Eq. 5.6}$$

Where, λ, θ and B are the X-ray wavelength, Bragg diffraction angle and line of full width at half maximum, respectively.

Transistor devices did not work at lower temperatures such as 200 $^0$C annealing because the crystallisation of ZnO films only takes place at temperatures approximately annealing temperature is greater than 300 $^0$C. Wurtzite structure is the dominant polycrystalline phase when the deposition/annealing temperatures are in the range of 300–450 $^0$C. The rise of (002) peak intensity and shift in the position of (002) peak can be attributed to better crystallinity with greater relaxation caused by annealing. All the diffraction peaks of these XRD patterns are in good agreement with the (JCPDS data Card No. 36-1451).

## 5.7.4 XPS Analysis of the ZnO Films

All sputtered samples used for XPS studies were prepared at Bangor University cleanroom. XPS measurements for sputtered ZnO films were done at Chester University and analysis was performed by Dinesh Kumar, Dr. Jeff Kettle and Prof. G.C Smith.

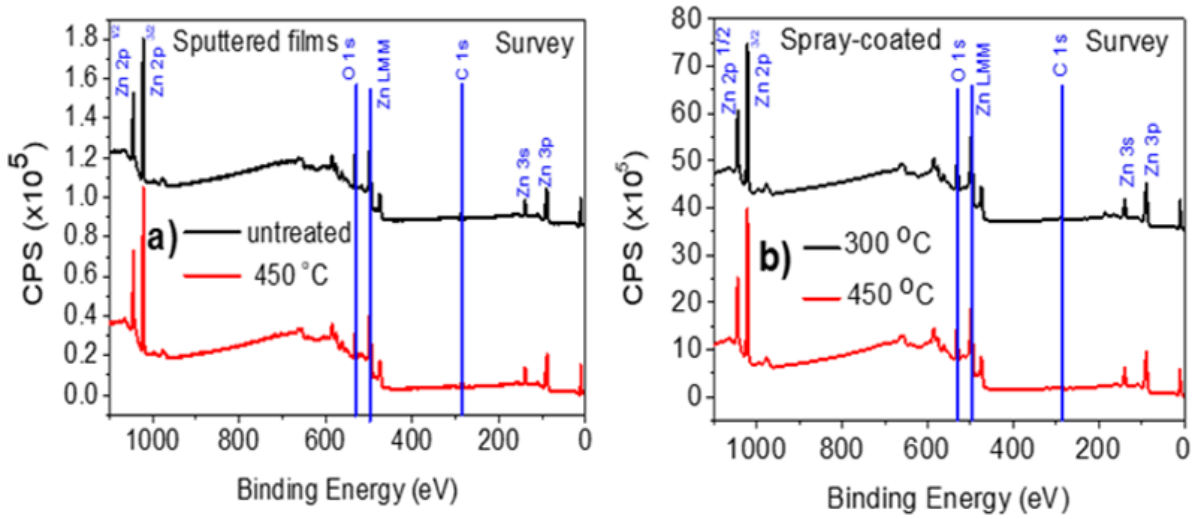


Figure 5.9: XPS survey scans from sputtered (a) and spray-coated ZnO films.

The XPS data from sputtered ZnO films were acquired using a bespoke ultra-high vacuum system fitted with a Specs GmbH Focus 500 monochromated Al Kα X-ray source, Specs GmbH Phoibos 150 mm mean radius hemispherical analyser with 9-channeltron detection, and a Specs GmbH FG20 charge neutralising electron gun. XPS data from spray-coated films were obtained using a K-Alpha, Thermo Scientific spectrometer from National Laboratory for Nanoscience in Campinas, Brazil. Survey spectra were acquired over the binding energy range 1100 – 0eV using a pass energy of 50eV and high-resolution scans were made over the C 1s, O 1s and N 1s photoelectron lines (where detected) using a pass energy of 20 eV. Under these conditions, the full width at half maximum of the Ag $3d^{5/2}$ reference line is < 0.8eV. In each case, the analysis was an area-average over a region approximately 2mm in diameter on the sample surface. The energy scale of the instrument is calibrated according to ISO standard 15472, and the intensity scale is calibrated using an in-house method traceable to the UK National Physical Laboratory. Data were quantified using Scofield cross sections corrected for the energy dependencies of the electron attenuation lengths and the instrument transmission. Data interpretation was carried out using CasaXPS software v2.3.16. The spot area was a 400 x 400 $\mu m^2$ region.

XPS spectra from all samples (both sputtered and sprayed) showed strong Zn and O peaks, with C also present. The annealed sputtered sample also showed a very low level of Cl. As an example, the survey scan for the as-prepared sputtered sample is shown in Figure 5.9 (a) and for the spray-coated films, in Figure 5.9 (b). The results of the quantification of the data are shown in Table 5.12.

Table 5.12: Surface composition for sputtered and spray-coated ZnO films.

| Element and line | Position [eV] | Surface concentration, atom % | | | |
|---|---|---|---|---|---|
| | | Sputtered Films | | Spray-coated films | |
| | | As-prepared | Annealed | 300 [°C] | 450 [°C] |
| C 1s | 284.8 | 39.12 | 27.79 | 22.75 | 22.53 |
| O 1s | 530-532 | 38.59 | 42.33 | 48.07 | 48.69 |
| Zn $2p^{3/2}$ | 1022 | 22.29 | 29.71 | 29.18 | 28.77 |
| Cl 2p | | - | 0.16 | - | - |

Table 5.13: Surface compositions after application of the hydrocarbon contamination overlayer correction (excluding the very minor l contribution in the case of the annealed sample.

| | | As prepared | Annealed |
|---|---|---|---|
| | Hydrocarbon layer thickness (nm): | 1.75 | 1.15 |
| Element and line | O 1s | 52.94 | 51.78 |
| | Zn $2p^{3/2}$ | 47.06 | 48.22 |
| Ratio O/Zn | | 1.13 | 1.07 |

The data shows that annealing of the sputtered films reduced the amount of surface carbon present and also reducing the ratio of oxygen to zinc from ~ 1.7 to ~ 1.4. Stoichiometric ZnO is expected to show a ratio of O/Zn of 1. The difference is probably due to preferential attenuation of the Zn $2p^{3/2}$ signal compared to the O 1s signal by the surface carbonaceous overlayer, as a consequence of the lower kinetic energy of the Zn $2p^{3/2}$ photoelectrons. To correct the measured surface compositions for the effect of the hydrocarbon overlayer, the method of Smith (2005) is applied. In this method, the carbon composition is used to estimate the thickness of the hydrocarbon contamination overlayer, the effect of a layer of this thickness on the attenuation of signals from the underlying material is estimated, and the results are re-normalised to 100 % atoms. The results of applying this correction for sputtered samples are shown in Table 5.13.

The results show a much closer approach to the stoichiometric ZnO, as expected, but a smaller Zn content in the spray coated film, indicating a lower level of C impurities. The slight excess of O is most likely due to the presence of some carbon-bonded oxygen.

Hydrocarbon contamination in spray-coated films was not so significant and the correction procedure was no applied.

### 5.7.5 Surface Chemistry

The Zn 2p spectra from the spray coated samples are shown in Figure 5.10. The Zn 2p spectra present a spin-orbit splitting ($2p^{3/2}$ and $2p^{1/2}$) distancing approximately 23.1 eV, with the low binding energy peak around 1021.2 eV. These peaks are consistent with $Zn^{2+}$ ions in the crystalline lattice, which is the case for ZnO. No significant changes were observed for spray-coated and sputtered samples, irrespective of annealing treatment. Further clear evidence that the observed Zn peaks are associated with the presence of ZnO comes from the intense components of the Auger peaks found at kinetic energies of approximately 988.4 eV (binding energy equivalents of approximately 498.2 eV).

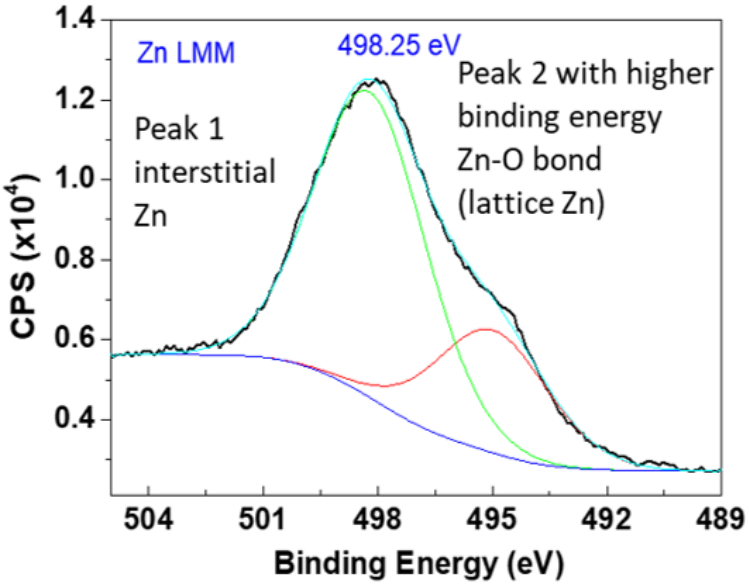


Figure 5.10: Zn $2p^{3/2}$ and LMM X-ray excited Auger spectra for the as-prepared samples.

From these results, the samples consisted of near-pure stoichiometric ZnO with a hydrocarbon overlayer due to absorption from the environment, as is usually seen in XPS analysis of air-exposed samples. Annealing did not appear to change the chemistry or stoichiometry of the ZnO; however, it did result in a reduction in the amount of hydrocarbon contamination. If the hydrocarbon was assumed to be present as a uniform thin overlayer, then its thickness was reduced from approximately 1.75 nm to approximately 1.15 nm on annealing.

For spray-coated films, where hydrocarbon contamination did not play an important role, annealing seems to change slightly the sample chemistry and

stoichiometry, leading to a higher amount of oxygen in metallic bonds in the crystalline lattice and a higher amount of oxygen vacancies. Both cases corroborate the improved electrical properties of the devices, discussed later.

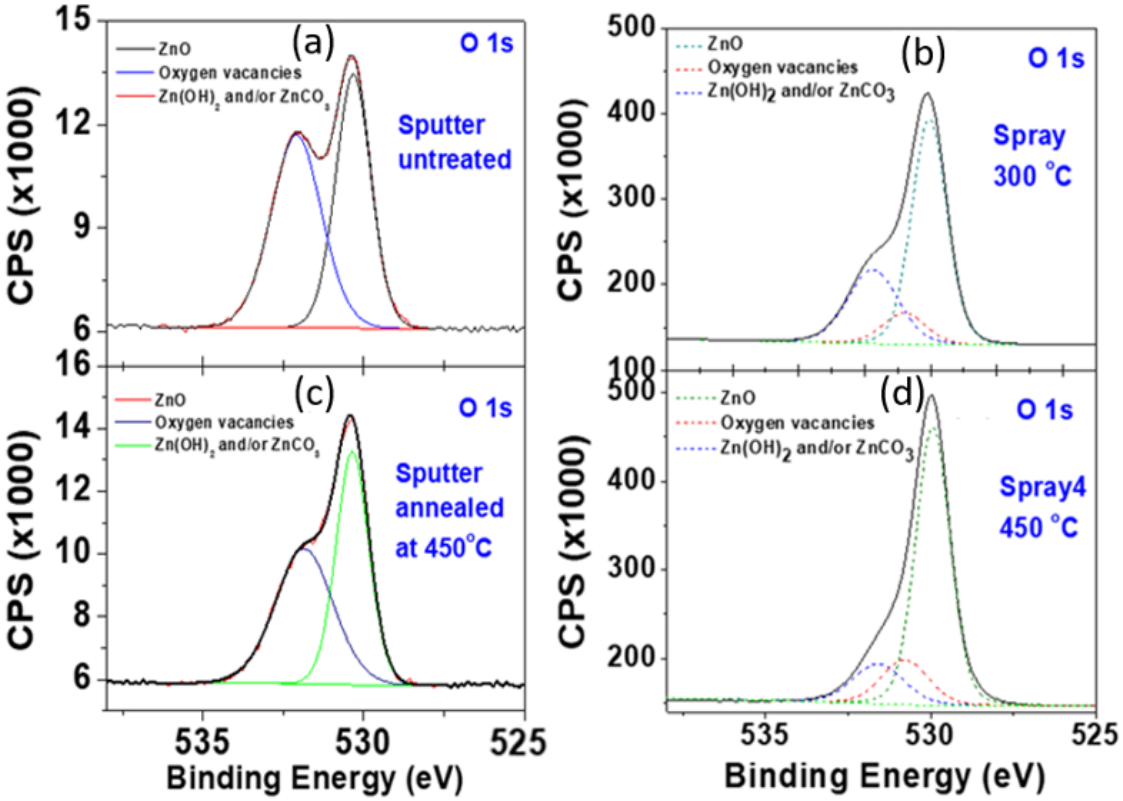


Figure 5.11: (a) sputtered untreated high-resolution spectra for O 1s, (b) sputtered annealed at 450 $^0$C high-resolution spectra for O 1s (c) sprayed at 300 $^0$C high-resolution spectra for O 1s (d) sprayed at 450 $^0$C high-resolution spectra for O 1s.

High resolution scans over the O1s peaks (for sputtered and sprayed samples) are shown in Figure 5.11 also, curve-fitted to known chemical state reference data. The spectra from the sputtered films show a strong component at approximately 530.4 eV and a broader component at approximately 532 eV. The sharper component at lower binding energy is attributed to oxygen in metallic bonds (in ZnO in this case), with the broader component at higher binding energy due to oxygen in a range of unresolved carbon bonding configurations, consistent with those observed in the C 1s peak. The difference between as-prepared and annealed samples is consistent with the reduction in the hydrocarbon contamination layer (and its associated oxygen bonds) on annealing.

High resolution scans over the C 1s peaks from sputtered samples are shown in Figure 5.12, curve-fitted to known chemical state reference data. Both C 1s spectra show strong hydrocarbon peaks at 285.0 eV, with weaker components at approximately 286.5

eV and 289.0 eV due to C-O (hydroxyl) and COO- (surface acid groups). After annealing, there was a small drop in the relative proportion of acid groups compared to the non-annealed samples (11% of the C 1s intensity, compared to 15% of the C 1s intensity as prepared). However, any differences in the chemical state after annealing appear minor. Similar peaks (but less intense) were observed in spray-coated samples (HR scans not shown).

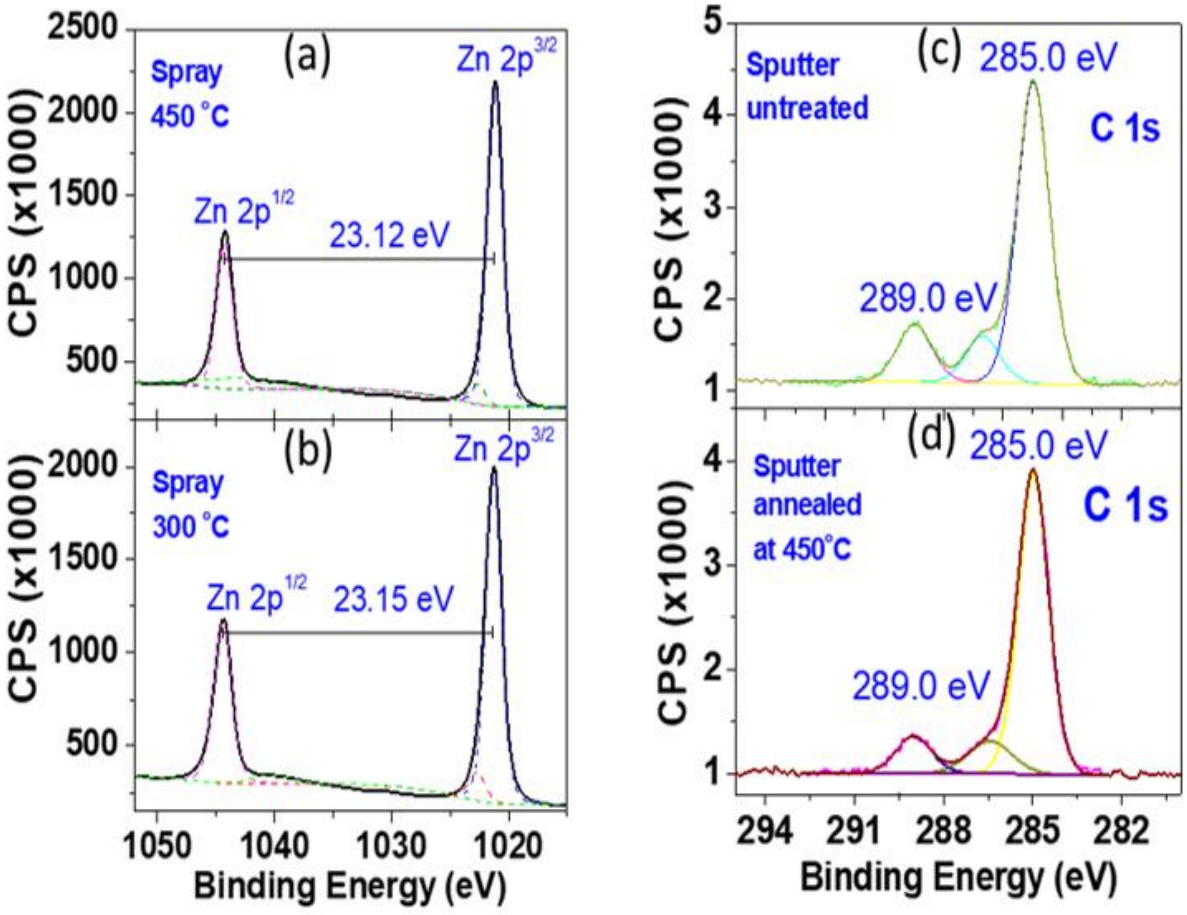


Figure 5.12: (a) Zn 2p spectra for spray-coated films annealed at 450 $^0$C, (b) Zn 2p spectra for spray-coated films annealed at 300 $^0$C, Carbon 1s spectra for sputtered samples (c) untreated, (d) annealed at 450 $^0$C.

Spray-coated films have much narrower O1s spectra, probably due to the longer annealing time (1 hour). The spectra were fitted considering three major contributions, as shown in Table 5.14. The low-energy and more intense component at 530 eV is attributed to oxygen in metallic bonds, forming crystalline ZnO. Two smaller components are observed at 530.8 eV and 531.7 eV. The higher energy component can be attributed to oxygen in ZnOH or $ZnCO_3$ bonds since the spray-coated ZnO films are formed by the pyrolysis of an organic precursor salt, zinc acetate dihydrate. The intermediate

component at 530.8 eV is commonly attributed to oxygen atoms in oxygen deficient regions caused by oxygen vacancies [210]. Table 5.14 shows that the annealing at 450 $^0$C increases the amount of oxygen in the crystalline lattice, simultaneously by the decrease of the amount of oxygen in ZnOH and $ZnCO_3$, which is consistent with the picture of higher conversion from zinc acetate to ZnO. Moreover, the increase of the amount of oxygen related to oxygen vacancies for the annealed sample is in agreement with the observed improvement of the electrical properties of the films, since the n-type conductivity of ZnO can be associated to oxygen vacancies [211].

Table 5.14: Component assignment for the O 1s spectra from the spray-coated samples.

| Component | Spray Annealed at 300 [$^0$C] | | Spray Annealed at 450 [$^0$C] | |
|---|---|---|---|---|
| | Position | %At Concentration | Position | %At Concentration |
| O 1s (a) | 530.04 | 60.81 | 529.93 | 69.69 |
| O 1s (b) | 530.80 | 10.47 | 530.79 | 15.40 |
| O 1s (c) | 531.75 | 28.73 | 531.58 | 14.91 |

Table 5.14 can also be used to correct the surface composition concerning the stoichiometric composition of spray-coated ZnO films. By considering only the amount of oxygen in metallic bonds in the crystalline lattice compared to the Zn 2p peak, we find a stoichiometric O:Zn ratio of 1.00 and 1.18 for the samples annealed at 300 $^0$C and 450 $^0$C, respectively.

Overall, the higher saturation mobility in case of sprayed as compared to sputtered TFTs is attributed to the higher oxygen levels in as prepared as well as annealed samples.

## 5.8 Electrical Characterization of ZnO Thin-Film Transistors Fabricated using Spray and Sputter Deposition

The electrical properties of the sputtered and spray deposited ZnO films were also investigated using optimised bottom-gate, top-contact thin film transistor. A comparative set of the transfer and output characteristics for ZnO TFTs (W/L = 5.55) deposited from spray and sputter processes at various processing temperatures are shown in Figure 5.13 and 5.14 respectively.

As shown in Table 5.15, the sprayed TFTs exhibit excellent operating characteristics with the maximum electron mobility of 15.55 $cm^2V^{-1}S^{-1}$ and current on/off

ratio of $2.1\times10^6$. However, for sputtered TFTs, lower mobility of 1.19 $cm^2V^{-1}S^{-1}$ and on/off ratio of $7.67\times10^3$ is reported. The better performance in case of spray deposition is probably due to the better initial crystal formation of the ZnO active layer, whereas sputtering occurs at room temperature and is subsequently post-annealed, as supported by the XRD data.

Table 5.15: Performance parameters of sprayed and sputtered ZnO TFTs at different annealing temperatures.

| Annealing temperature ($^0C$) | Sprayed performance Parameters | | | Sputtered performance Parameters | | |
|---|---|---|---|---|---|---|
| | $\mu_S$ $[cm^2V^{-1}s^{-1}]$ | $V_T$ [V] | $I_{on}/I_{off}$ [ratio] | $\mu_S$ $[cm^2V^{-1}S^{-1}]$ | $V_T$ [V] | $I_{on}/I_{off}$ ratio |
| 300 | 1.34 | 10.38 | 1.34E+06 | 0.21 | 9.11 | 3.52E+03 |
| 350 | 1.63 | 8.92 | 4.6E+05 | 0.68 | 6.78 | 1.45E+03 |
| 450 | 15.55 | 4.48 | 2.1E+06 | 1.19 | 5.51 | 7.67E+03 |

The ZnO TFT transfer and output curves were stable when measured after 8 week in the dark storage. In Table 5.15, the performance parameters are shown as a function of annealing temperature. For both sputtered and spray coated devices, the threshold voltage ($V_T$) decreases, and the saturation mobility ($\mu_S$) increases with increasing annealing temperature. This is likely to be due to a reduction in impurities at insulator/semiconductor interface and removal of any moisture in device structure which can degrade the device performance. Also, at higher annealing temperatures, more electrons can escape from the localized states and contribute to the free carriers in the conduction band, which causes higher mobility and smaller threshold voltage [212]. Increased mobility after annealing is attributed to increased oxygen levels as confirmed by the XPS analysis. Improved device performance by increasing the annealing temperature might come from better crystallinity (or higher average crystallite size), improving the inter-grain charge transport. Moreover, there would be less influence from defects at the grain boundaries, which can cause charge-trapping and/or scattering. XPS data have also shown an increase in the Zn amount in metallic bounds, which also means that there is more crystalline ZnO at elevated annealing temperatures.

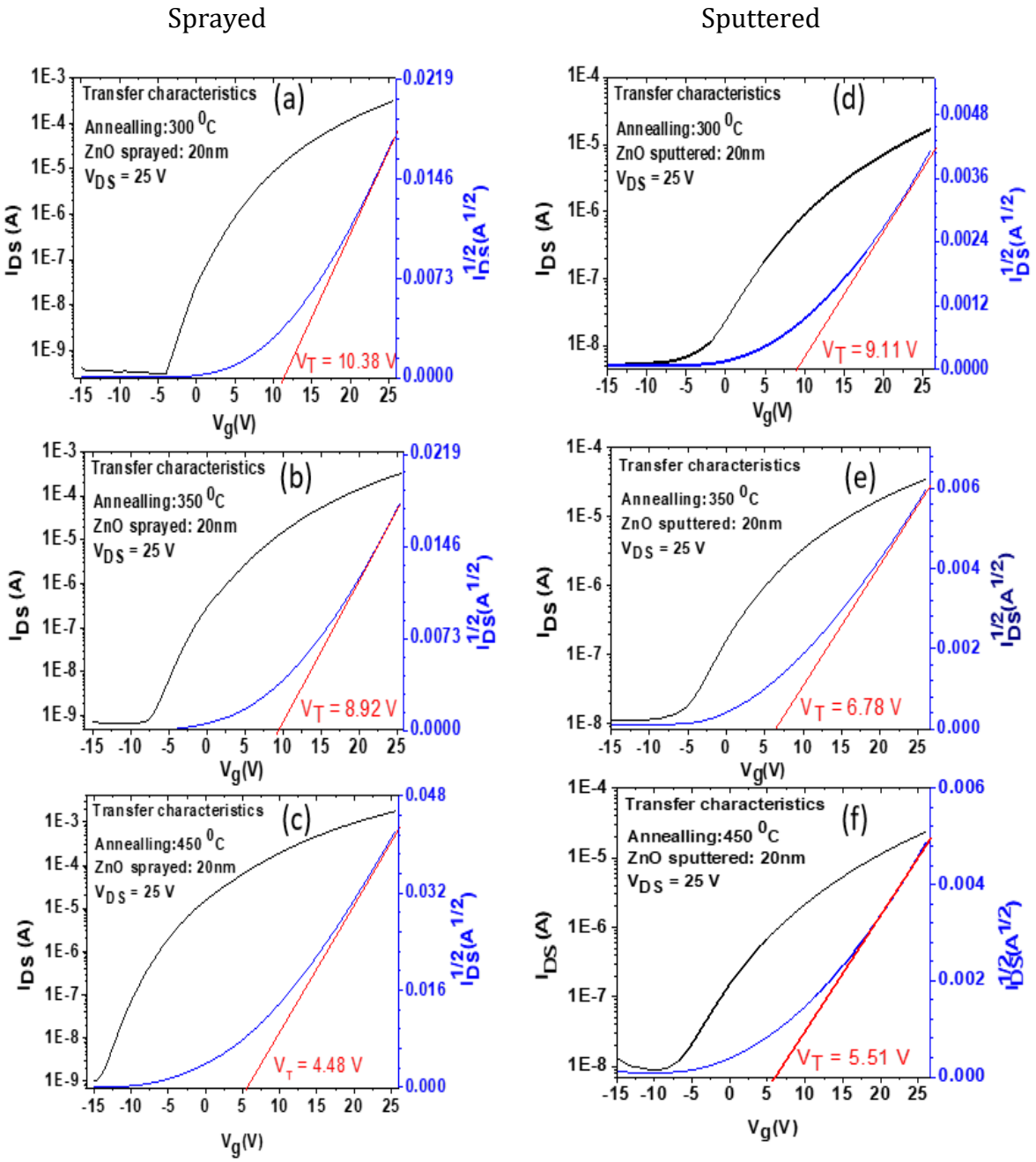


Figure 5.13: Transfer characteristics of sprayed (a) annealing at 300 ˚C, (b) 350 $^0$C, (c) 450 $^0$C and sputtered (d) annealing at 300 $^0$C, (e) 350 $^0$C, (f) 450 $^0$C ZnO TFTs annealed at different temperatures shown above.

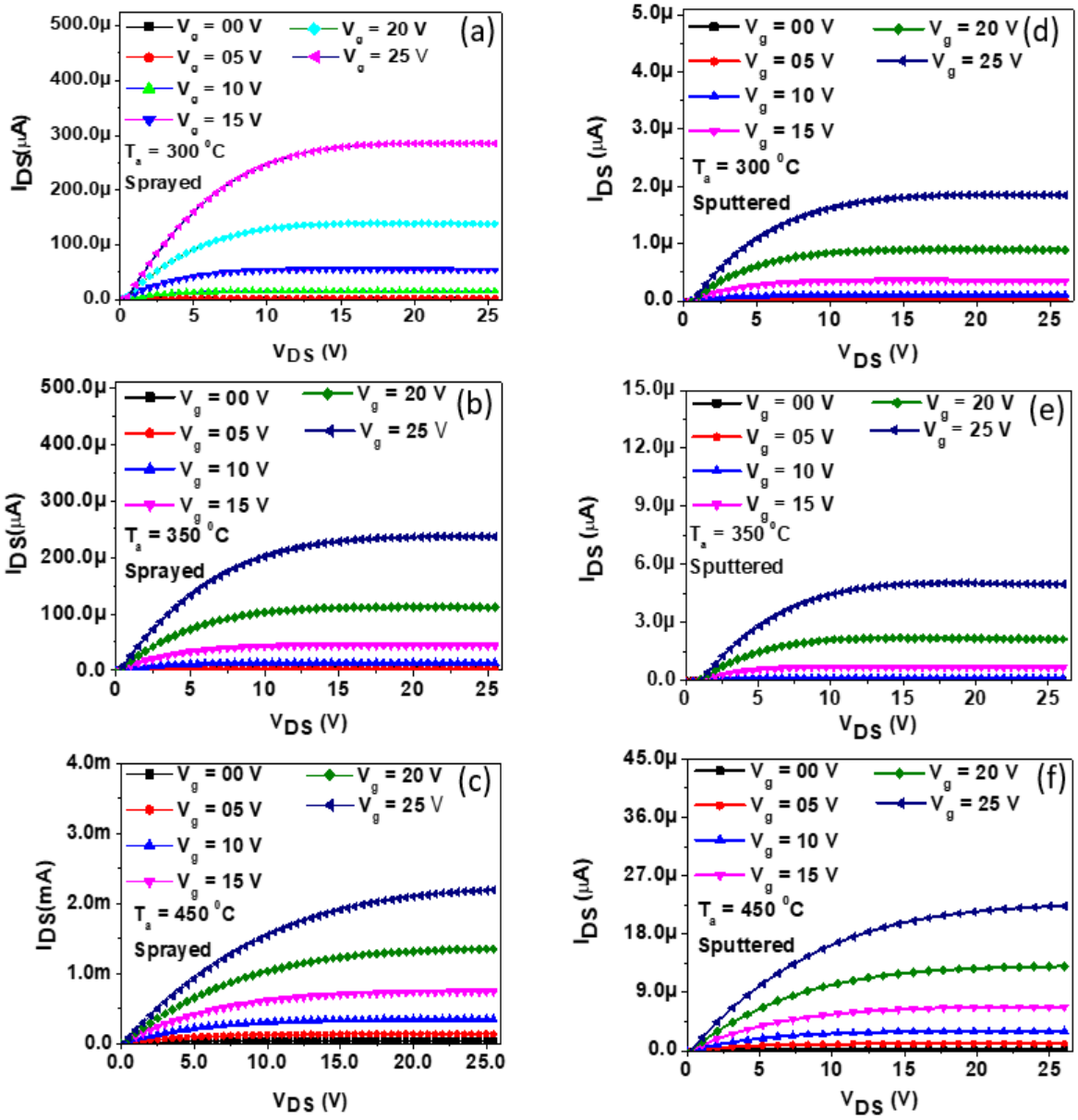


Figure 5.14: Output characteristics of sprayed (a) annealing at 300 ˚C, (b) 350 0C, (c) 450 0C and sputtered (d) annealing at 300 0C, (e) 350 0C, (f) 450 0C ZnO TFTs annealed at different temperatures shown above.

## 5.9 UV Saturation Experiment

UV saturation experiment on ZnO TFTs manufactured using spray, as well as sputtered deposition methods to see the effect of UV light on the TFT characteristics have conducted.

Figure 5.15 (a) shows transfer characteristics of a ZnO TFT manufactured by spray coating and 5.15 (b) sputter coated before (black curve) and after (in blue) exposure to a UV-355 nm LED for 5 minutes at an irradiance of 0.214 mW/mm$^2$. In both

cases, the characteristics changed dramatically and shown is the behaviour after 5 minutes of light exposure, by which time the devices had saturated in terms of their electrical changes. Such behaviour is commonly known as "persistent photoconductivity". The ZnO TFT performance parameters including $\mu_S$, $V_T$ and on-off ratio were evaluated before and after exposure to UV light.

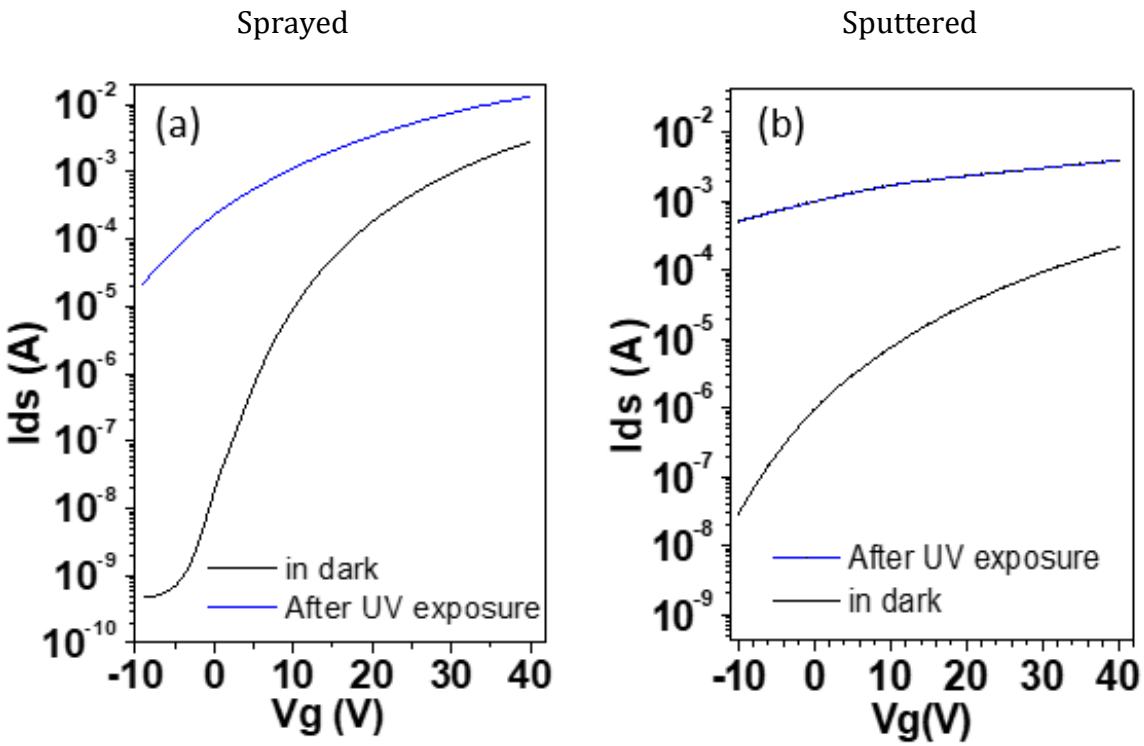


Figure 5.15: Transfer curves for a ZnO TFT with the active layer deposited by (a) spray-coating, (b) sputter coating before and after UV exposure for 5 minutes at an irradiance of 0.214 mW/mm$^2$.

Both types of TFTs show an overall increase in these parameters after UV exposure. However, with a more accentuated effect in the "off-current" region, where the gate bias is smaller than the threshold voltage. The relative change in these performance parameters is higher in the case of sprayed TFTs, suggesting that sprayed TFTs are more sensitive to UV irradiation. This can be attributed to higher surface roughness in case of sprayed TFTs as confirmed by AFM data, increased surface area might be responsible for higher adsorption of molecular oxygen onto the film surface. This increased conductivity effect occurs due to the photo-stimulated desorption of adsorbed oxygen molecules in the ZnO film. In the absence of UV light, oxygen molecules can be adsorbed on the surface as negatively charged ions by capturing the free electrons from the *n*-type semiconductor, thereby create a depletion layer with low conductivity near the surface. When the sample

is exposed to UV light with photon energy in the UV, it generates electron-hole pairs which increase the conductivity.

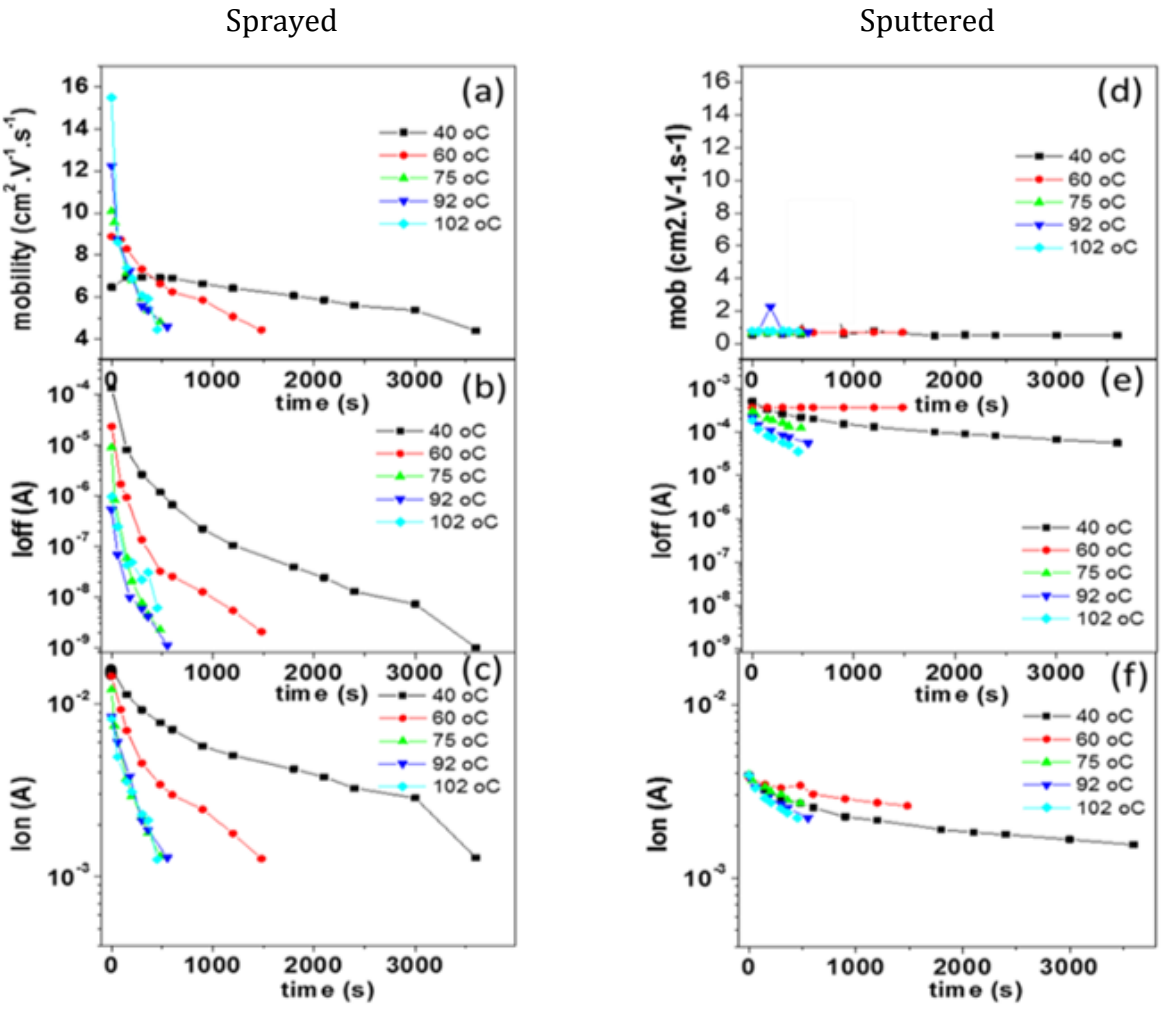


Figure 5.16: Decay time of the sprayed ZnO TFT (a) mobility, (b) OFF-current, (c) Drain on-current and sputtered ZnO TFT (d) mobility, (e) off-current, (f) on-current at different temperatures.

Shown in Figure 5.16 (a), (d) is saturation mobility, (b), (e) TFT OFF-current, and (c), (f) TFT on-current, the decay behaviour of sprayed (left), sputtered (right) the TFT with respect to time elapsed after the UV excitation was switched off for temperatures varying from 40 $^0$C until 102 $^0$C. The mobility for sprayed TFTs increases with temperature and presents a slow decay time at 40 $^0$C. However, the sputtered TFTs show similar mobility values at all temperatures of measurements. By increasing the temperature, the decay of the photo-stimulated mobility becomes faster and nearly no temperature dependence can be observed. The sprayed TFT on-currents Figure 5.14 (c), however, presents a larger variation, with a faster decay than the carrier mobility Figure 5.16 (a) at low temperature (40 $^0$C) and almost invariant behaviour at higher temperatures (above 75 $^0$C), indicating that the on current increase is not only due to the

increase in the carrier mobility by UV illumination but also by the increase in the free charge carrier density in the transistor channel due to elevated temperature excitation energy. The off-current, which is a direct measure of the ZnO film conductivity, presents an even higher variation with temperature and a faster time decay Figure 5.16 (b) at lower temperatures. The initial value of the off-current is strongly dependent on the temperature, however, for temperatures above 75 $^0$C, a temperature dependence cannot be observed for longer times.

From the observed results, it can be confirmed that, even though the increase on the temperature causes an increase on the UV-stimulated carrier mobility, it is also responsible for accelerating the adsorption of the oxygen molecules to the ZnO TFT active layer, which contributes to the decrease in the carrier mobility and the semiconductor conductivity. The TFT off-current has a faster decay time than the on-current because the contribution to the off-current comes from the conductivity of the whole ZnO layer, which has a larger area for oxygen adsorption, whereas the contribution to the on-current comes from the conductivity of the ZnO/dielectric interface, which represents a small portion of the whole ZnO film.

Figure 5.11 shows the temperature dependence of the sprayed TFT mobility (a), off current (c), and of the sputtered ZnO TFT mobility (b), off-current (d) immediately after the UV light was switched off. The TFT mobility increases with temperature, with an activation energy of about 140 meV for sprayed and 53 meV for sputtered TFTs. The OFF-current, as mentioned above, decreases with temperature, due to the adsorption of oxygen molecules from the ZnO film. This adsorption process is thermally activated and has an activation energy of 9.6 meV for sprayed and high activation energy 229.4 meV for sputtered samples. The adsorption process is thermally activated, introducing trapping centers that cause a decrease in the TFT device current. The density of free carriers (proportional to the TFT off current) can be expressed as equation (5.7), where, ΔE is the activation energy of the adsorption process.

$$n = n_0[1 - exp\left(-\frac{\Delta E}{k_B T}\right)] \qquad \text{Eq. 5.7}$$

Figure 5.17 shows that the adsorption process for sprayed samples has a very low thermal activation energy, which causes a strong dependence of the off current on the

temperature. On the other hand, the activation energy for the adsorption process for sputtered devices has higher activation energy, meaning that the off current has little influence on the temperature, as observed in Figure 5.17. Overall the results show that the sputtered samples are less sensitive to UV irradiation because the charge transfer is quicker.

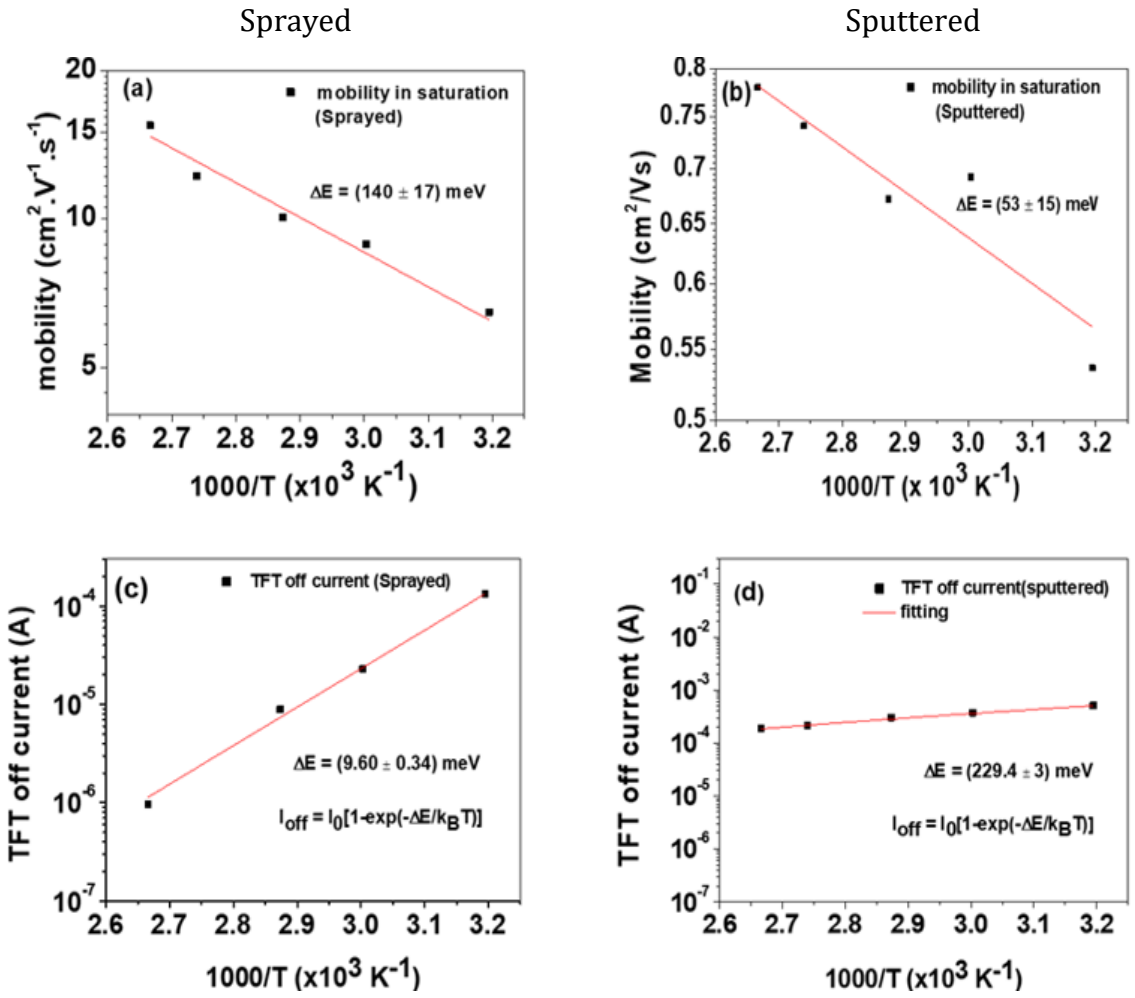


Figure 5.17: Temperature dependence of the sprayed TFT mobility (a), off current (c), and of sputtered ZnO TFT mobility (b), off-current (d) immediately after the UV light was switched off.

## 5.10 Summary

The optimisation of $Al_2O_3$ dielectric and ZnO deposition process using a combinational, DOE approach is reported. Correlations between the manufacturing process parameters and the device characteristics were investigated. An important observation from the results is that the manufacturing parameters of the dielectric layer of the TFTs have a strong influence on the device performance parameters, presenting a comparable effect

(or even higher) on the device characteristics than the variation of the dielectric layer surface treatment parameters, which are commonly investigated in the literature. This procedure is particularly interesting for optimization of other devices in printed/flexible electronics to improve the fabrication process and to speed up the development of new low-cost products.

ZnO TFTs are well suited to UV sensing applications because they absorb predominantly in the UV region due to the wide bandgap ($E_g$ = 3.37 eV). From the perspective of UV sensing, TFT on-current in the saturation region appears to be the best performance parameter in a ZnO TFT for examining differences in UV exposure.

The effect of the substrate temperature during ZnO deposition by spray pyrolysis and annealing temperature after sputtering to the structural, optical, and electrical transport properties has been investigated. Sprayed and sputtered ZnO film structural characterization demonstrated the formation of polycrystalline ZnO only at deposition temperatures above 200 $^0$C. Further increase of the substrate deposition/annealing temperature to 450 $^0$C resulted in films with enlarged crystal size. Consequently, thin-film transistors based on ZnO films grown at substrate temperatures in the range of 300 to 450 $^0$C exhibit the highest electron mobility. It has been shown that the electrical characteristics of both ZnO TFT sprayed and sputtered are altered after their interaction with UV radiation. However, the magnitudes of these changes are larger in sprayed ZnO TFT than sputtered as their surface structure has a greater affinity with the absorption and desorption of oxygen molecules in its surface. The present results demonstrate the possibility of depositing high optical and electronic quality ZnO films onto large area substrates using spray pyrolysis, which is attractive for the electronic industry, since the pyrolysis spray technique is inexpensive; it is not need vacuum steps and is easily applied to large-scale electronics.

# Chapter 6. Effect of Bias Stressing on Indium Gallium Zinc Oxide TFTs and Flexible TFTs

In this chapter, the development of Indium-gallium-zinc-oxide (IGZO) thin film transistors (TFTs) is discussed. IGZO TFTs have advantages of high transparency in the visible range due to being wide bandgap semiconductor, high field-effect mobility and low temperature for device fabrication [213], [214], which are mandatory requirements for high performance display applications [215]. IGZO TFT performance shows great potential for future low power and flexible electronics applications. However, the stability of amorphous oxide semiconductor (AOS) TFT under the various stress has been an issue for practical applications [216]. It is well known that the total trap density affects the behaviour of the threshold voltage shift ($\Delta V_T$) in IGZO TFTs [217], [218]. Therefore, the effects of positive bias stress are investigated in inorganic TFTs based on IGZO as the semiconductor and silicon dioxide as the gate insulator, with measurements carried out over a range of positive bias stress. Bias stressing was performed by applying positive gate bias stress for a particular time, measure output, transfer characteristics, and recover the device to initial state using white light illumination and again applying bias for next period

In this chapter, the effect of positive gate biasing and CYTOP (a fluoropolymer) passivation on TFTs is discussed. An application of gate bias stress leads to a shift in the threshold voltage of IGZO TFTs and after it is removed, the threshold voltage ($V_T$) eventually returns to its original value. The underlying physical mechanisms for the shift in threshold voltage during the application of the bias and after the removal of the bias stress are investigated.

To increase the carrier mobility of the IGZO TFTs, a high dielectric constant (high-k) material has been used as the gate insulator to improve the electrical performance of IGZO TFT[219], [220]. Therefore, the performance of low voltage IGZO TFT devices using high-k dielectric aluminium oxide ($Al_2O_3$) on plastic substrates is described. Moreover, based on AgNW TCEs developed in chapter 4, AgNW film gated IGZO TFTs electrical, optical performance was also investigated and compared with TFTs on incumbent ITO transparent electrodes.

## 6.1 Experimental details

In this work, a flexible Kapton type HN polyimide film (25μm thick) was used as the substrates, which were supplied from RS components ltd, UK. Immediately following cleaning and drying, the samples were transferred to Leybold thermal evaporator and Al metal (80nm) was deposited on these film substrates. E-beam evaporation system was used to deposit gate dielectric. The evaporation source materials were $Al_2O_3$ (1mm to 3mm clear pieces with 99.99% purity). The chamber was then pumped down to a base pressure of $8\times10^{-6}$ torr and the deposition rate was kept below 2 Angstrom/second for uniform layer deposition. The film thickness (168nm) was measured using the Dektak surface profilometer. After manufacturing a 20 nm thick IGZO channel layer by using radio frequency (RF) sputtering technique, TFTs were post annealed at 250 °C for 1 hour and cooled down to room temperature. Post annealing is performed because it removes physical defects, such as sputter damage, and stabilizes the oxygen concentration.

IGZO TFTs with bottom-gate, top-contact structure were fabricated on $SiO_2$ substrates obtained from Micro Chemicals GmbH. All steps of fabrication including sputtering, thermal evaporation and annealing were carried out in the class 100 cleanroom. Firstly, substrates were thoroughly cleaned with solvents followed by drying with a jet flow of nitrogen and oxygen plasma treated for 5 minutes. Thin-film transistors were fabricated by depositing a thin IGZO active layer on top of commercial $SiO_2$/Si substrates using RF sputtering. The dry thermally grown 100 nm thick $SiO_2$ layer acts as the TFT dielectric layer whereas the p-doped (boron) Si substrate (500 μm thick) is used as the TFT gate electrode. A thin layer of aluminium (100 nm thick) was thermally evaporated on the bottom of the Si substrate to assure good contact with the gate electrode. On top of the IGZO active layer, Al contacts were thermally evaporated using a Leybold 250 Univex thermal evaporator through a metallic shadow mask to make drain and source top electrodes. The post-thermal-annealing (450 °C) process is used to repair the interface traps in the IGZO thin film and to reduce the bulk traps/defects in the channel. An organic- passivation layer (CYTOP) was spin coated inside glove box inert environment for the passivating active layer of TFTs and annealed at 160 °C for 30 minutes. CYTOP-organic-passivation has the following characteristic: high transparency, electric insulation, water and oil repellence, chemical resistance, and moisture-proof property-“wettability control”. Passivating IGZO TFTs with CYTOP in the inert environment (Glove box) leads to moisture control over the device. CYTOP is a

hydrophobic material and its passivation minimizes environment-related reactions. Hydrophobic molecules are usually nonpolar, meaning the atoms that make the molecule do not produce a static electric field.

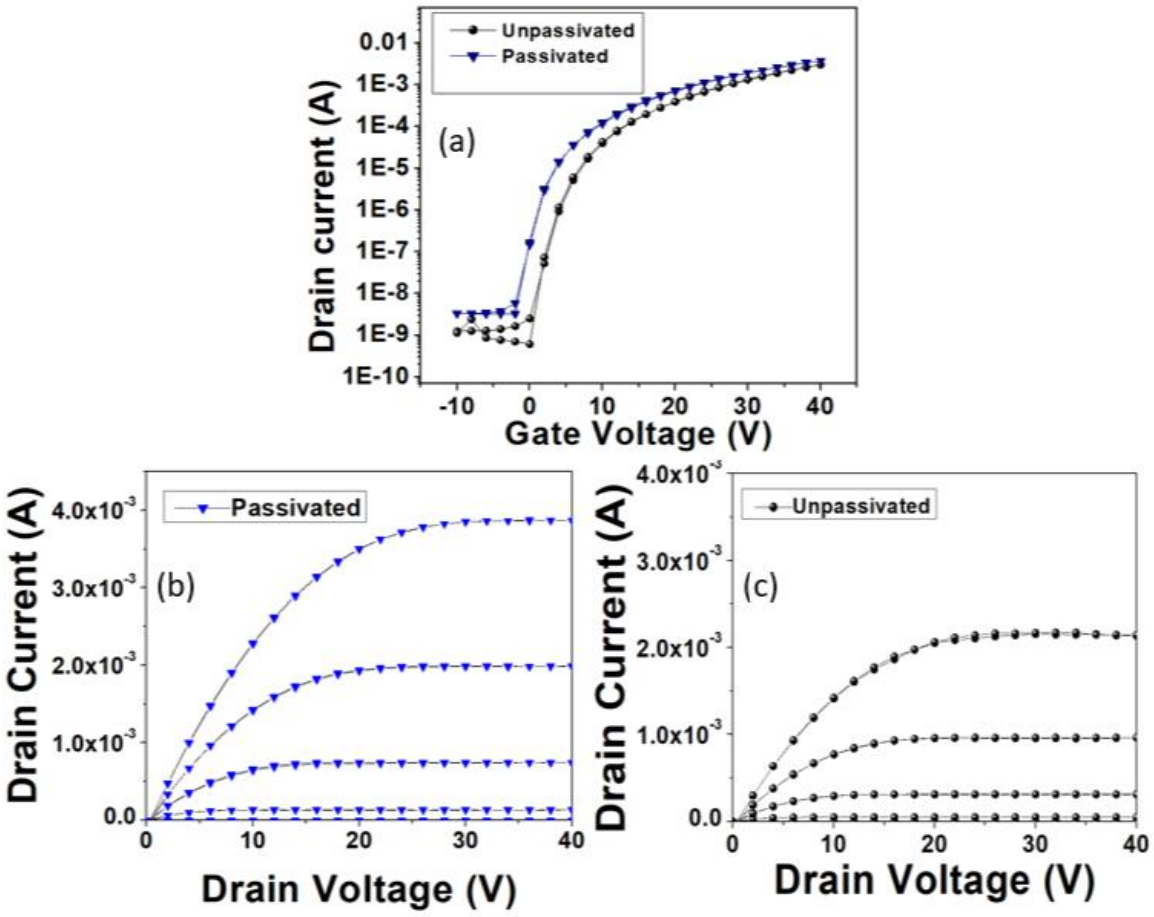


Figure 6.1: (a) Transfer characteristics of unpassivated and CYTOP passivated IGZO TFTs, (b) Output characteristics of CYTOP passivated IGZO TFT and (c) Output characteristics of unpassivated IGZO TFT.

## 6.2 Effect of CYTOP Passivation on Performance of IGZO TFTs

Shown in Figure 6.1 are the output and transfer characteristics of pristine and passivated IGZO TFTs. The TFTs with the CYTOP passivation layer exhibited a relatively good electrical characteristic ($\mu_s$ = 20 $cm^2V^{-1}s^{-1}$) compared with that of the unpassivated TFT ($\mu_s$ = 17 $cm^2V^{-1}s^{-1}$). CYTOP passivation improves electrical characteristics, reduces the threshold voltage and increases mobility. The CYTOP passivation was performed at low annealing temperature (160 $^0$C), and therefore, it is compatible with polymer substrates.

## 6.3 Bias Stressing of IGZO TFTs

In this section, results for fabricated IGZO TFTs employing a organic-passivation layer

(CYTOP) are explained and compared with un-passivated IGZO TFTs. CYTOP is an amorphous fluoropolymer with a high light transmittance of more than 95%.

### 6.3.1 Comparison of Unpassivated Positive Gate Bias Stress

The effect of positive bias stress (PGBS) on the electrical performance of an IGZO TFTs on $SiO_2$ was investigated by measuring the transfer characteristics in the dark before and after stress. In this case, the initial state was achieved by applying the recovery procedure using white light discussed next section. Shown in Figure 6.2 the evolution of transfer characteristics of un-passivated and passivated IGZO TFTs as a function of stress time, demonstrating the time-dependence of the bias stress resulting from applying a constant gate voltage for 11000 seconds, (a) un-passivated $V_G$ = 5 V and drain voltage, $V_D$ of 0V, (b) un-passivated $V_G$ = 20 V, $V_D$ of 0V, (c) un-passivated $V_G$ = 40 V, $V_D$ of 0V,(d) passivated $V_G$ = 5 V and drain voltage, $V_D$ of 0V, (e) passivated $V_G$ = 20 V, $V_D$ of 0V, (f) passivated $V_G$ = 40 V, $V_D$ of 0V, in all cases the characteristics were measured with $V_G$ = 40 V, $V_D$ = 40 V.

As seen in Figure 6.2, the transfer characteristics display a similar pattern i.e. a simple translation along the $V_G$ axis in the direction of the applied positive electric field. There is negligible hysteresis between forward and reverse scans, neither before nor after any applied stress condition. It is observed throughout the stress period, that the subthreshold region continues to shift positively while off-current is reduced in both un-passivated, as well as passivated devices. However, there is a reduction in the magnitude of saturation current, $I_D$, after stressing for un-passivated devices, whereas this reduction in saturation current $I_D$ after stressing for passivated devices is negligible. This is presumably due to low trap levels in passivated devices as compared to un-passivated ones.

To better understand the physics behind the positive bias stress induced threshold voltage shift in RF sputter IGZO TFT, we performed a detail numerical analysis based on the stretched-exponential model. The carrier injection from conducting channel and the subsequent charge trapping plays an important role in the IGZO TFT positive bias instability. The dependence of $\Delta V_T$ on time is generally described by the stretched exponential function given equation 6.1.

$$\Delta V_T(t) = |V_T(\infty) - V_T(0)| \left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \qquad \text{Eq.6.1}$$

Where, $V_T(\infty)$ is the threshold voltage after long stress times, $V_T(0)$ its value prior to bias stress, $\tau$ is a characteristic time constant and $\beta$ the stretching factor describing the distribution in trap times. The solid curves in Figure 6.3 (a) represents the stretched exponential fitting of equation (6.1) to the data using the extracted fitting parameters listed in Table 6.1 zero drain voltage, $V_D$ = 0 V and different gate-bias stress conditions ($V_G$ = 40 V and 10 V).

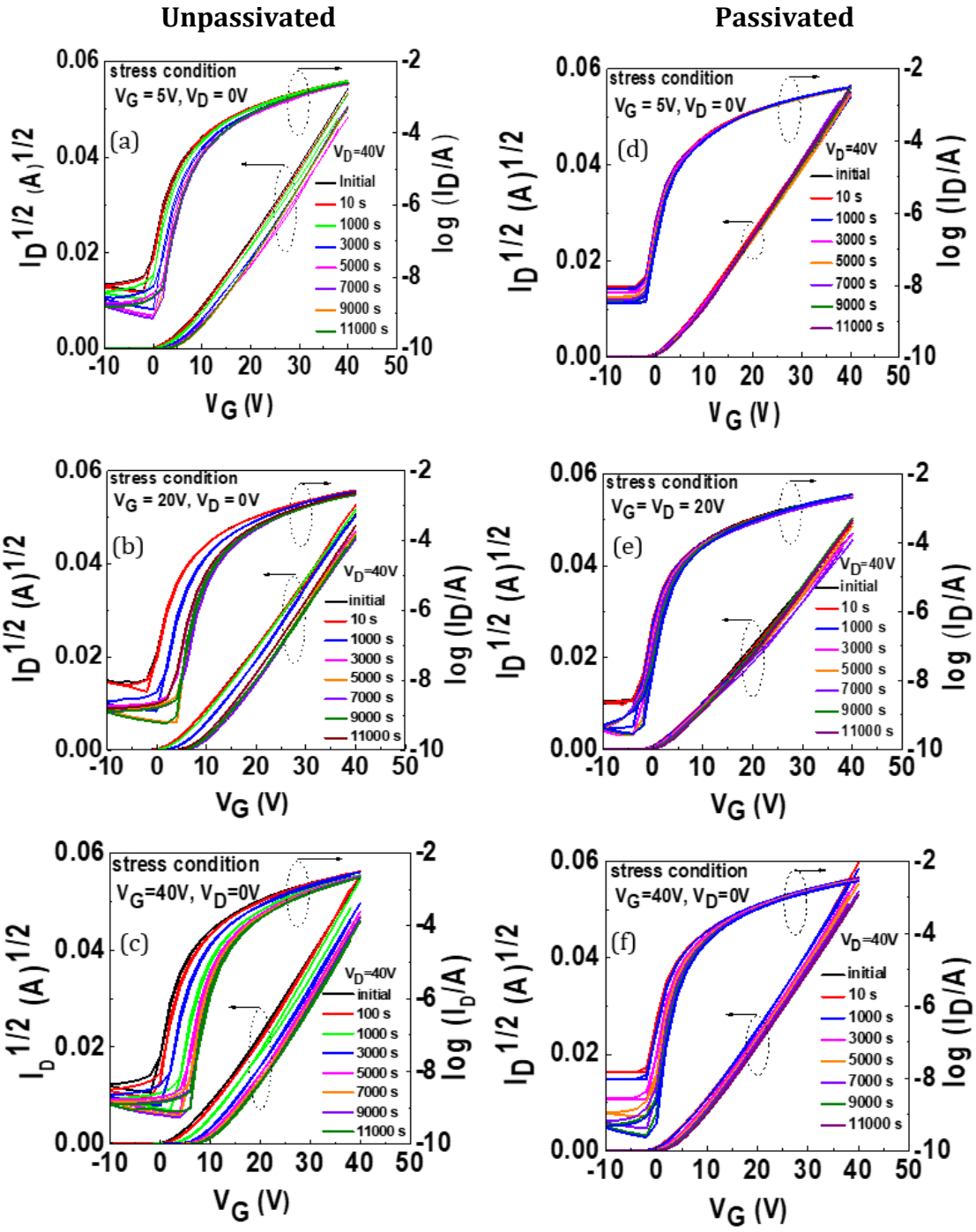


Figure 6.2: Transfer characteristics of un-passivated and passivated TFTs showing the time-dependence of the bias stress resulting from applying a constant gate voltage, (a) Un-passivated $V_G$ = 5 V and drain voltage, $V_D$ of 0V, (b) un-passivated $V_G$ = 20 V, $V_D$ of 0V, (c) un-

passivated $V_G$ = 40 V, $V_D$ of 0V,(d) passivated $V_G$ = 5 V and drain voltage, $V_D$ of 0V, (e) passivated $V_G$ = 20 V, $V_D$ of 0V, (f) passivated $V_G$ = 40 V, $V_D$ of 0V, in all cases the characteristics were measured with $V_G$ = 40 V, $V_D$ = 40 V.

Table 6.1: Parameters obtained by fitting equation (6.1) to the measured bias stress-induced $\Delta V_T$ in Figure 6.3 (a).

| $V_G$ (V) | $\lvert V_T(\infty)-V_T(0)\rvert$ (V) | τ (s) | β |
|---|---|---|---|
| 10 | 3.27 | 8.47 x $10^3$ | 0.36 |
| 40 | 12.66 | 9.08 x $10^3$ | 0.51 |

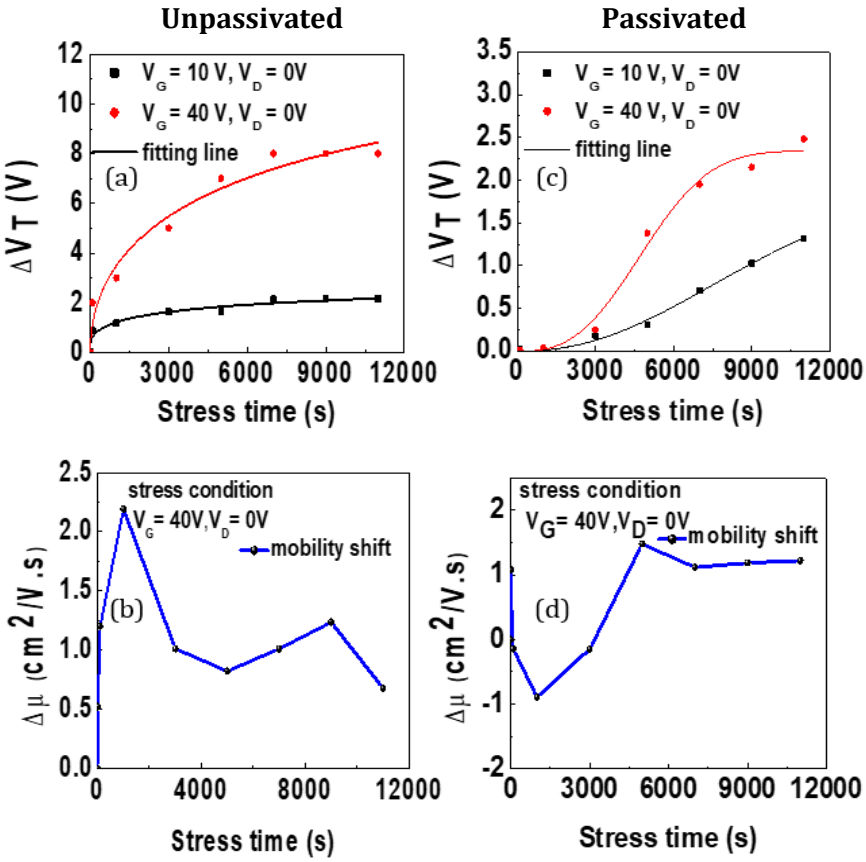


Figure 6.3: Changes in threshold voltage shift and mobility as function of gate bias stress time for gate bias stress (a) un-passivated threshold voltage shift at 10V, 40V (b) un-passivated saturation mobility shift at 10V, 40V, (c) passivated threshold voltage shift at 10V, 40V and (d) passivated saturation mobility shift at 10V, 40V.

Shown in Figure 6.3 are the changes in threshold voltage shift and mobility as function of gate bias stress time for gate bias stress (a) un-passivated threshold voltage shift at 10V, 40V (b) un-passivated saturation mobility shift at 10V, 40V, (c) passivated threshold voltage shift at 10V, 40V and (d) passivated saturation mobility shift at 10V, 40V. The $\Delta V_T$ is highly affected by the stress for un-passivated devices which is caused by electrons trapping at the interface between semiconductor/insulator. However, in the case of passivated TFTs, $\Delta V_T$ is only slightly affected by the positive gate bias stress due

to small electrons trapping at the interface between semiconductor/insulator. This is due to the hydrophobic nature of the CYTOP passivation layer. The red line in Figure 6.3 (a), (c) indicates that the time dependence of $\Delta V_T$ can be described by the stretched-exponential function given by equation (6.1). The gate-voltage dependent saturation mobility decreased for unpassivated TFTs as shown in Figure 6.3 (b), however for passivated initially decreased and then remained unchanged by positive voltage stressing as shown in Figure 6.3 (d).

## 6.4 Recovery Procedure

First gate voltages ($V_G$) ranging from 5V to 40 V were applied with the drain voltage $V_D$=0V. All stress conditions were applied for 11000s in the dark under ambient (uncontrolled) laboratory conditions, typically T=15 $^0$C-25 $^0$C and RH=40%–60%. After completing a bias stress test, selected devices were subjected to a recovery procedure. The recovery was interrupted at fixed times to record the transfer characteristics of the transistor with a drain bias of $V_D$=40V by sweeping the gate bias from 0 to 40V.

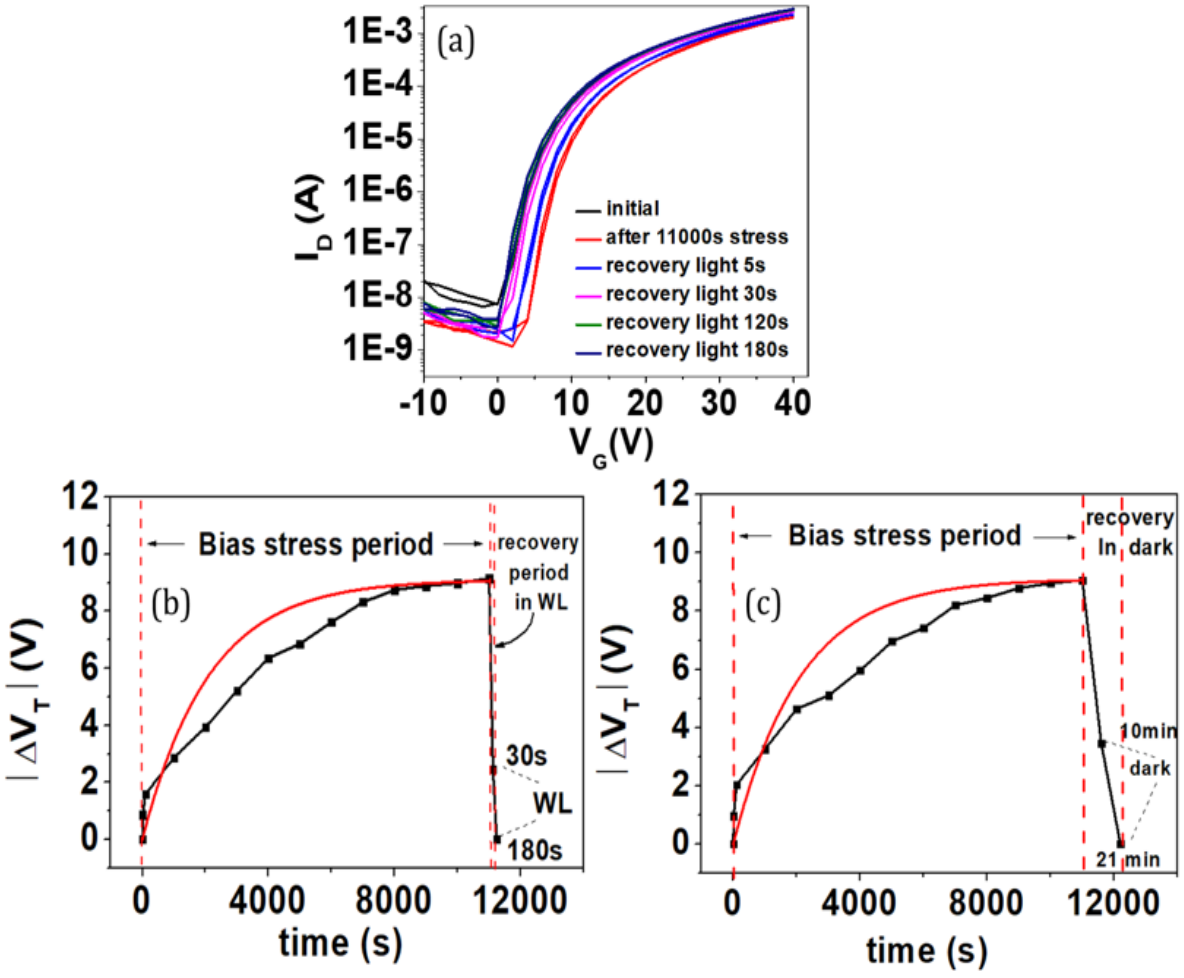

Figure 6.4: (a) Transfer characteristics recorded before, after positive bias stress and recovery at 180s with light, (b) time dependence of $\Delta V_T$, recovery under white light illumination and (c) time dependence of $\Delta V_T$, recovery under dark. The device was subjected to PGBS of $V_G$ = 40V for 11000s.

Before proceeding to the next stress condition, $V_T$ was reset to its initial value by exposing the device to white light for about 180s using white LED (3.2 V White LED 5mm through hole, Nichia NSPW500DS) purchaged fron RS components. Figure 6.4 (a) shows the transfer characteristics recorded before and after positive bias stress and full recovery after illumination 180s with white light, the time dependence of $\Delta V_T$ under white, Figure 6.4 (b) and Figure 6.4 (c) under devices short-circuited condition in the dark. The device was subjected to bias stress $V_G$ = 40 V, $V_D$ = 0 V in the dark for 11000 s. The recovery process was performed in the dark and under white light illumination with $V_G = V_D$ = 0 V. Shown in Figure 6.4 (b) full recovery time 180s under white light and (c) 21 min for full recovery under dark when devices were left short-circuited in the dark.

It can be clearly observed in Figure 6.4(a), that the transfer curves shift back towards the one obtained before stressing. Changes in the threshold voltage ($\Delta V_T$) over time both during stress and under recovery are shown in Figure 6.4 (b), (c). It is observed, that the full recovery of $\Delta V_T$ in the dark took 21 min. However, with white light exposure for a few seconds, $\Delta V_T$ fell to zero and the transfer curve was restored within ~ 180 s to its original value, thus providing a rapid method of re-setting the device ahead of further measurements. Such a fast recovery property is technologically relevant and could be utilized in practical applications such as in a memory device.

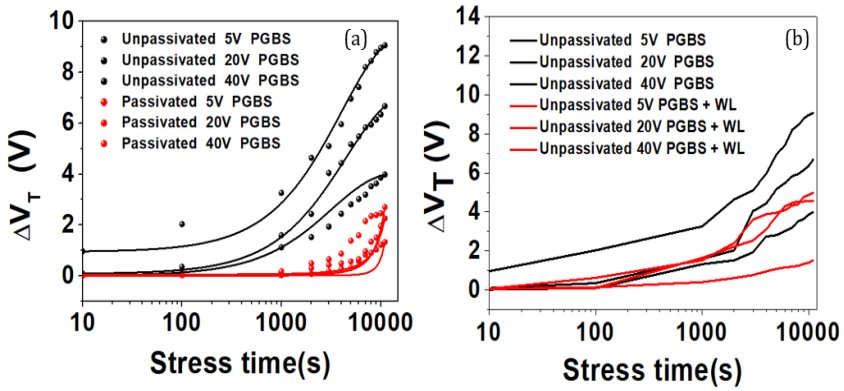


Figure 6.5: Change in threshold voltage, (a) un-passivated and passivated TFTs threshold voltage shift at 5V, 20V, 40V (b) un-passivated TFTs threshold voltage shift at 5V, 20V, 40V with white light (WL) and without white light as a function of gate bias stress for 11000s time.

## 6.5 Effect of CYTOP Passivation, White light (WL) and Positive Gate Bias stress

The influence of CYTOP passivations and white light illumination on the stability of IGZO thin film transistor is investigated in this section. Figure 6.5 shows the change in threshold voltage, change in threshold voltage, (a) un-passivated and passivated TFTs threshold voltage shift at 5V, 20V, 40V (b) un-passivated TFTs threshold voltage shift at 5V, 20V, 40V with white light (WL) and without white light as a function of gate bias stress for 11000s time.

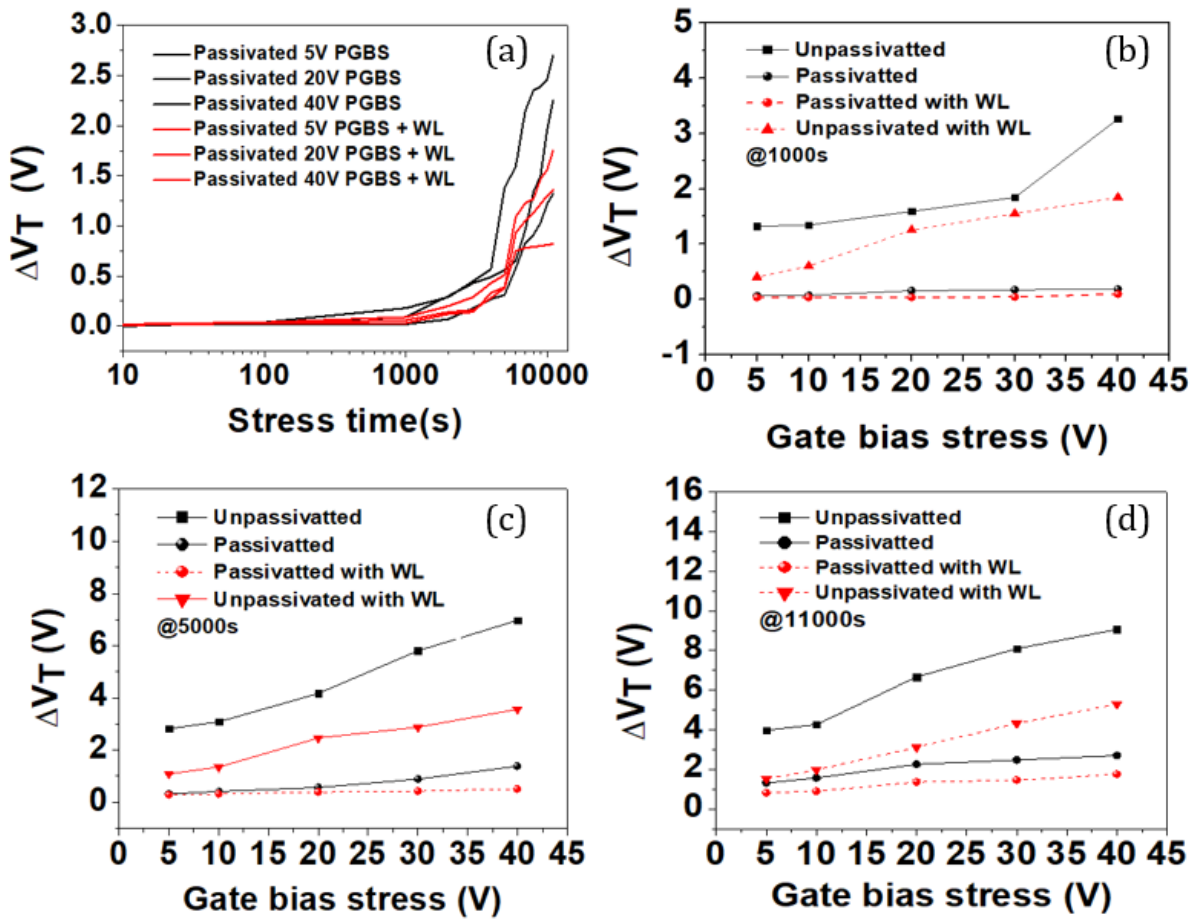


Figure 6.6: The Change in threshold voltage, (a) passivated TFTs threshold voltage shift at 5V, 20V, 40V with white light (WL) and without WL , (b) un-passivated, un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 1000s time, (c) un-passivated, un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 5000s time, (d) un-passivated, un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 11000s time.

Figure 6.6 shows the change in threshold voltage, (a) passivated TFTs threshold voltage shift at 5V, 20V, 40V with white light (WL) and without WL , (b) un-passivated,

un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 1000s time, (c) un-passivated, un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 5000s time, (d) un-passivated, un-passivated with white light, passivated and passivated with white light threshold voltage shift as a function of gate bias stress for 11000s time.

It can be clearly seen from Figure 6.5 (a) that $\Delta V_T$ shift the CYTOP-passivated device exhibited relatively good stability ($\Delta V_T$ = 1V) under positive gate bias stress of 5V while the unpassivated TFTs showed a 4.1V $\Delta V_T$ shift, respectively. The effect of white light on un-passivated TFTs can be seen from Figure 6.5 (b). Under long positive gate bias stress, the device illuminated by white light exhibits smaller positive threshold voltage shift than the device stressed under dark as one can observe from Figure 5.5 (b), 6.6 (a). The reduced threshold voltage shift under WL illumination can be explained by a competition between the bias-induced interface carrier trapping effect and photon-induced carrier de-trapping effect [221].

Overall, it is observed that CYTOP passivation reduces the traps and removes any moisture at the CYTOP/IGZO interface. However, WL illumination on the device reduces the threshold voltage shift due to photon-induced carrier de-trapping at the dielectric/active layer interface.

## 6.6 CV Measurements Before and After Bias Stressing

In the study of metal–oxide–semiconductor (MOS) structures, the capacitance voltage (CV) analysis is one of the simplest approaches for probing defects. To further clarify the instability effect of PGBS on passivated and unpassivated IGZO TFTs, the gate to source capacitance ($C_{GS}$) of IGZO TFTs was investigated. The C-V measurement of IGZO TFT was used to prove the positive effect of the proposed CYTOP passivation layer on reducing the traps at the interface. Whilst this does not quantify the number of trap states (as these will start to decrease as the measurement begins), trends in the data can be identified. The difference of capacitance between unpassivated and passivated TFTs as shown in Figure 6.8 is due to low interfacial traps in passivated ones as compared to unpassivated.

The low frequency TFT CV measurements were done at room temperature before and after PGBS using a Solatron SI 1255 HF frequency response analyser. The DC and the small-signal AC voltages were applied at the gate electrode, while changes to the stored

charges due to the AC signal were detected through the shorted source and drain electrodes. A low frequency was selected to allow the charging current to arrive from the source and drain regions. At higher frequencies, the sub-gap states could potentially be filled in time, and the CV curves would show no distinct accumulation and depletion regions. Shown in Figure 6.7 is the variation in magnitude of capacitance, $C_{GS,}$ with respect to applied gate voltage for unpassivated as well as passivated devices before the application of 40V positive gate bias voltage stress (PGBS). In the $C_{GS}$–$V_G$ measurement, capacitance measurement terminal high is applied to the gate electrode and the source electrode is connected to capacitance measurement low terminal. After 11000 s PGBS stress, $V_T$ variation with no degradation of subthreshold slope (SS) is observed, which is similar to the $I_D$–$V_G$ transfer curves as shown in Figure. 6.2. Shown in Figure 6.7 $\Delta V_{mg}$ is the shift of mid-gap voltage before and after PGBS of 40V for 11000s. It can be noted that this shift for CYTOP passivated is very small (1.5V) due to fewer trap states as compared to unpassivated (5.5V) TFTs for PGBS of 40V after 11000s.

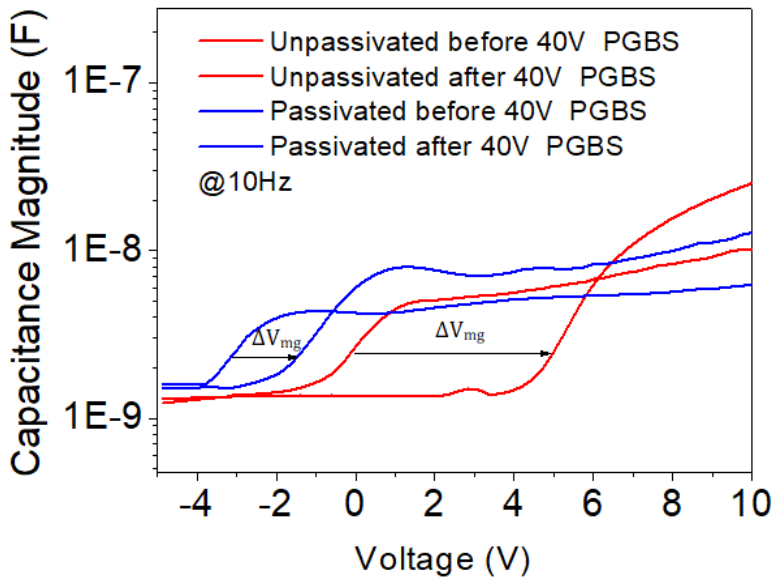


Figure 6.7: C-V curves for sputtered IGZO TFT before and after PGBS. $\Delta V_{mg}$ is the shift of mid-gap voltage before and after PGBS of 40V for 11000s.

## 6.7 Density of States (DOS) Analysis

In this section, Density of States (DOS) analysis is used to understand the difference between unpassivated and passivated IGZO TFT devices under PGBS. In the previous section 6.3, it was suggested that the main effect of PGBS is simply to cause a threshold voltage shift, $\Delta V_T$, arising from electron trapping in IGZO film or at $SiO_2$-IGZO interface. To confirm this, the DoS of the semiconductor was extracted to identify any evidence of

charge trapping within the IGZO bandgap. The DoS spectrum of IGZO was extracted from the transfer characteristics by applying the Grünewald method as outlined in Chapter 3.

Firstly, the relationship between the gate-dependent insulator/semiconductor interface potential, $V_0$, and the effective forward voltage, $V_F = (V_G - V_{ON})$ was obtained from equation (3.4) and plotted as shown in Figures 6.8 (a) and 6.8 (b). It can be observed that as stress time increases, plots of $V_0$ rise rapidly with $V_F$. Then the DoS, N(E) can be obtained with equations (3.5) and (3.6) explained in chapter 3 and plotted as a function of energy relative to the Fermi level, $E_F$, ($V_0 = E - E_F$) as shown in Figures 6.8 (c) and 6.8 (d).

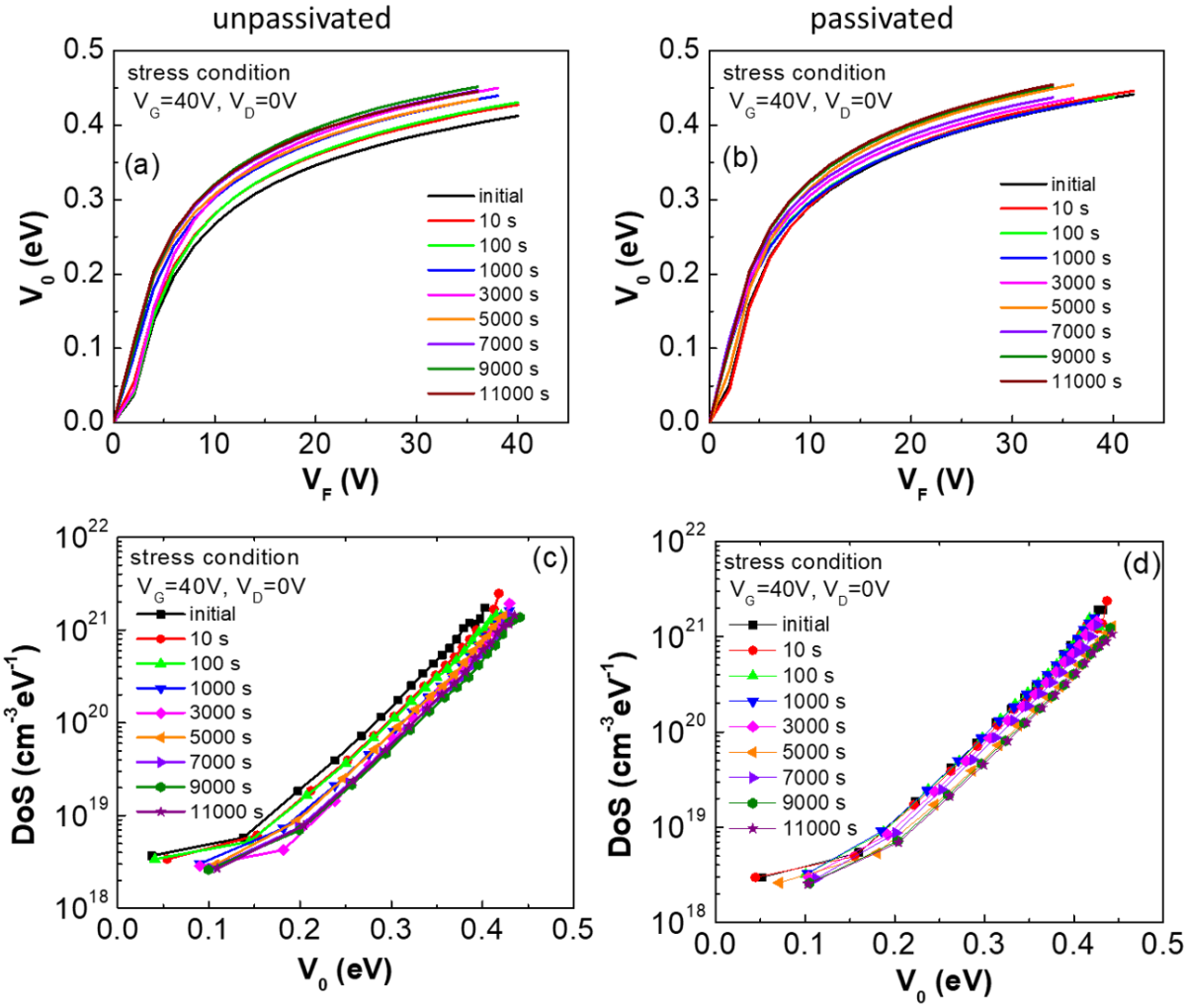


Figure 6.8: Plots of $V_0$ versus $V_F$ showing the effect of zero drain bias, $V_D$ = 0 V and gate bias stresses of (a) $V_G$ = 40 V unpassivated and (b) $V_G$ = 40 V passivated. Density of states for zero drain bias, $V_D$ = 0 V and gate bias stress of (c) $V_G$ = 40 V unpassivated and (d) $V_G$ = 40 V passivated.

From the plot of gate voltage dependent mobility at initial condition, it is assumed that the effective mobility becomes constant at ~10 $cm^2/Vs$ (Figure 6.9 (a). This coincides

with a transport band edge (Figure 6.9 (b)) or $E_C$. Upon evaluating the relevant energy, the DoS may be replotted as a function of ($E$-$E_C$) as shown in Figures 6.10 (a) and (b). Under all bias stress conditions, the initial DoS distribution decreases from 1 x $10^{21}$ $cm^{-3}eV^{-1}$ to 1 x $10^{18}$ $cm^{-3}eV^{-1}$). As can be seen that the effect of gate bias stress is minimal with the plots obtained before and after bias stress coalescing to a single curve.

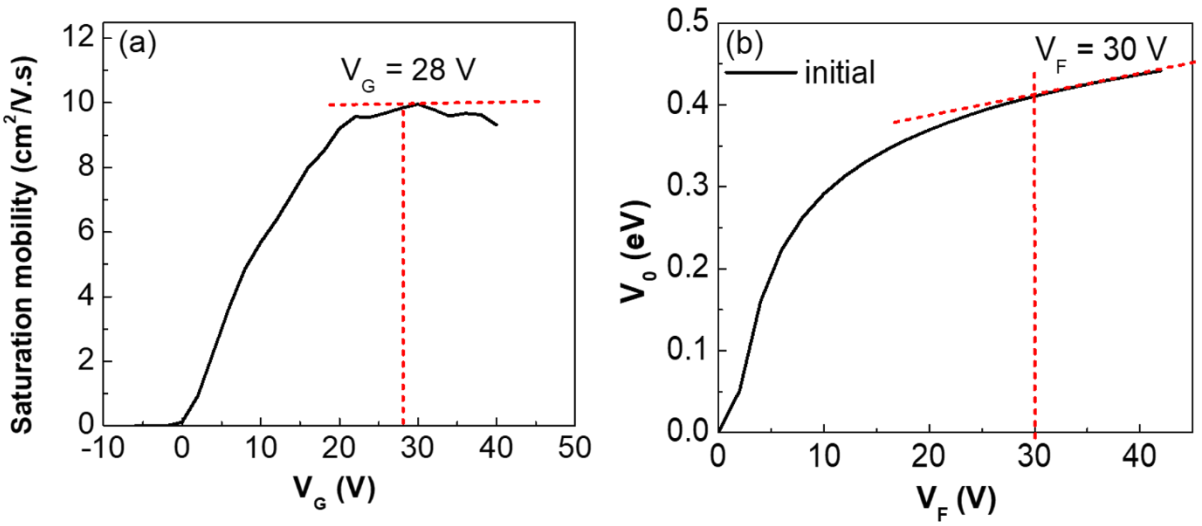


Figure 6.9: Constructions used to estimate the onset of mobility edge. The voltage, $V_G$, at which the tangent departs the experimental curve is noted and corrected for $V_{ON}$ to give $V_F$, i.e $V_F = V_G - V_{ON} = 28-(2) = 30$ V.

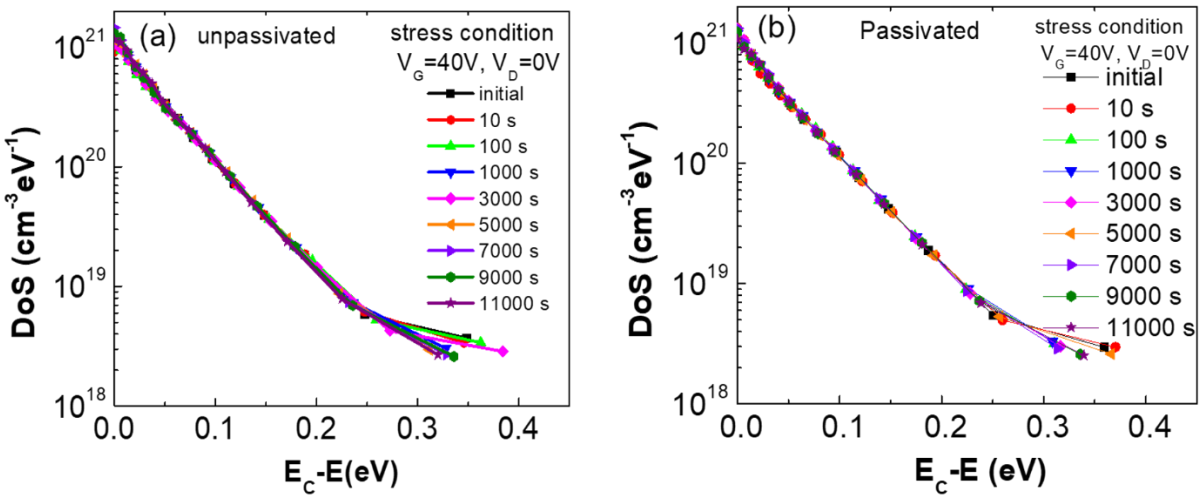


Figure 6.10: Density of states plotted as a function of E-$E_C$ for a zero-drain voltage, following gate bias stress with $V_G$ of (a) 40 V unpassivated and (b) 40 V passivated.

The DoS distribution was fitted with the single exponential function of a localized states DoS according to:

$$N(E) \approx \frac{N_t}{E_t} exp\left(-\frac{E}{E_t}\right) \quad 6.2$$

where $N_t$ is the total trap density while $E_t$ is the characteristic energy decay of the distributions. After stressing passivated devices for 11000 s under bias stress $V_G$ = 40 V, $V_D$ = 0 V, fitting parameters related to the shallow states ≤ 0.1 eV, is $N_t \sim 2.45 \times 10^{22}$ $cm^{-3}$ with $E_t \sim 43.8$ meV. However, for unpassivated devices with same stress level, the total trap density increases slightly to $N_t \sim 3.02 \times 10^{22}$ $cm^{-3}$ with $E_t \sim 40.4$ meV. This supports the view that shift in threshold voltage is due to interfacial traps existence and not from the formation of traps in the bandgap of IGZO

## 6.8 Low Voltage Flexible TFTs

IGZO thin-film transistors gated with E-beam processed thin $Al_2O_3$ have been fabricated on a plastic substrate. One method to achieve a low operating voltage is to decrease the thickness of the gate dielectric layer [222]. However, the gate leakage current can become too large if a conventional gate dielectric layer, e.g., $SiO_2$ is used. Otherwise, high dielectric constant (high-k) materials, such as $HfO_2$, $Al_2O_3$ and $Ta_2O_5$, have been used as a dielectric layer since they can provide a large specific gate capacitance without dramatically increasing the gate leakage current. Among the different types of high-k dielectric materials, $Al_2O_3$ is used because of its advantages such as low cost, low deposition temperature, low leakage current density and good compatibility with oxide semiconductors [223]. Shown in Figure 6.11 (a) a schematic cross-section of IGZO TFT with various device layers, (b) fabricated IGZO TFT device on Kapton film showing the bendability of devices.

Table 6.2: Surface roughness parameters of the dielectric and active layer.

| Sample | $R_q$(nm) | $R_a$(nm) |
|---|---|---|
| $Al_2O_3$ on Kapton | 12.4 | 9.8 |
| IGZO on $AL_2O_3$ | 5.1 | 4.1 |

Atomic force microscopy (AFM) was used to study the surface roughness of the IGZO and $Al_2O_3$ films on Kapton substrates. Shown in Figure 6.11 (c) is the atomic force microscopic (AFM) image of the sputtered IGZO active layer. The important surface

roughness parameters values like RMS roughness ($R_q$), and average roughness ($R_a$) are shown in Table 6.2. The surface roughness of the dielectric and active layer surface affects the performance parameters and it should be low as possible. Roughness values were high, but devices were working after repeated measurements.

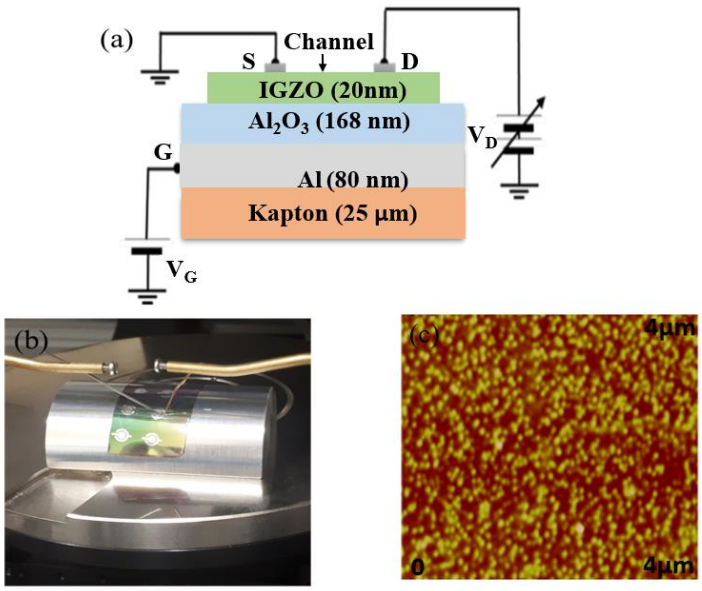


Figure 6.11: (a) A schematic cross-section of IGZO TFT biasing, (b) Fabricated IGZO TFT device on Kapton showing the flexibility and (c) AFM image of sputtered IGZO active layer.

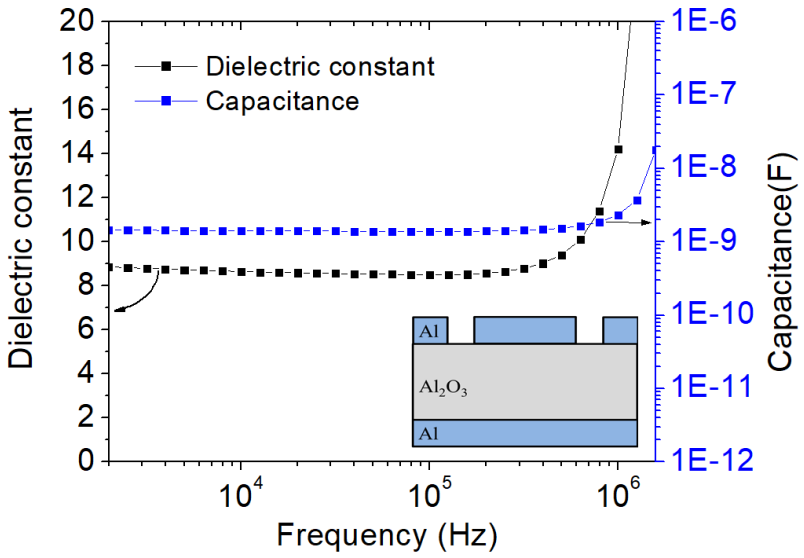


Figure 6.12: Dielectric constant and oxide capacitance (log scale) of E-beam evaporated $Al_2O_3$ versus frequency.

The dielectric performance parameters of the $Al_2O_3$ films were measured in MIM capacitor configuration. Shown in Figure 6.12 is the dielectric constant (k) and the oxide

capacitance versus frequency for a manufactured MIM capacitor. In the inset of Figure 6.13 is shown a schematic of the MIM capacitor. The dielectric constant calculated is found to be around 8.52 and this value is closely matching the value of $Al_2O_3$ dielectric constant (8.32) using E-beam evaporation [224]. As shown in Figure 6.12 the dielectric constant does not change in the frequency range from 2KHz to 100 kHz and start increasing at higher frequencies. It can be clearly observed from Figure 6.13 that oxide capacitance is constant in the frequency range of 500Hz to 250KHz.

The TFT channel length (L) was 400 μm and width (W) was 6300μm. The oxide capacitance density value in a flat band was 5.1 $Fm^{-2}$. The various performance parameters like mobility, threshold voltage and on/off current ratio were extracted from transfer characteristics and are tabulated in Table 6.3.

Table 6.3: Before bending the performance parameters of flexible IGZO TFTs at different bias voltages.

| Operating voltage $V_D$ (V) | $V_T$ (V) | on-off ratio | Mobility $cm^2V^{-1}s^{-1}$ |
|---|---|---|---|
| 0.5 | 0.07 | 0.92E+02 | 12.29 |
| 1 | 0.16 | 1.01E+03 | 28.11 |
| 2 | 0.18 | 0.89E+04 | 31.72 |

The fabricated flexible TFTs were characterized on curved holder, as shown in Figure 6.11 (b), where no considerable performance degradation was observed for curvature radii up to 15mm, as shown in Table 6.4. This result is promising for the use of the demonstrated TFTs in flexible electronics applications and combined with the ultra-low operation voltage (0.5V) these TFTs are suitable for battery-powered applications.

Table 6.4: After bending the performance parameters of flexible IGZO TFTs at different bias voltages.

| Operating voltage $V_D$ (v) | $V_T$ (v) | ON-OFF ratio | Mobility $cm^2V^{-1}s^{-1}$ |
|---|---|---|---|
| 0.5 | 0.08 | 0.90E+02 | 12.27 |
| 1 | 0.17 | 1.03E+03 | 28.09 |
| 2 | 0.19 | 0.88E+04 | 31.71 |

Typical transfer and output IV characteristics of IGZO TFTs measured under dark are shown in Figure 6.13. The leakage current is relatively high for these devices which

do need to be improved in future devices. The leakage current in these devices can be improved by using bi-layer/composite organic-inorganic dielectric.

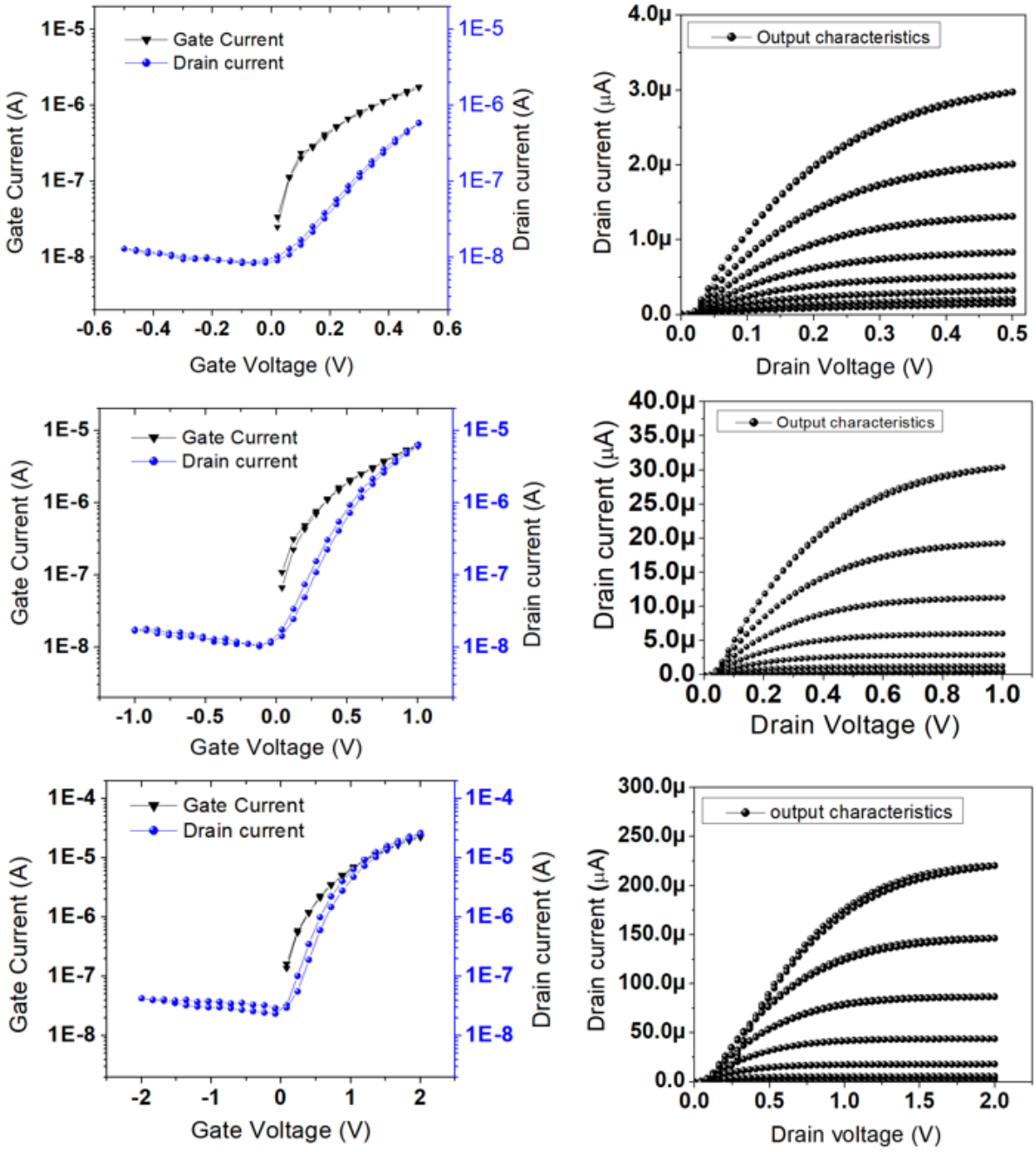


Figure 6.13: Transfer characteristics (a), (b) and (c) and output characteristics (d), (e) and (f) characteristics of IGZO-TFT with operating voltages: $V_D$ =0.5 V, 1V and 2V respectively.

Shown in Figure 6.14 the transfer characteristics of flexible IGZO-TFT before and after bending with operating voltage, $V_D$ of 1V. It can be clearly observed from transfer characteristics that before and after bending there is not considerable degradation in the performance of flexible IGZO TFTs. The manufactured devices show a low operating voltage ($V_D$) of 1 V, a high drain current on-off ratio >$10^3$, threshold voltage $V_T$ of 0.16V,

saturation mobility $\mu_{sat}$ of 28 $cm^2V^{-1}s^{-1}$ and a low subthreshold swing <200 mV/decade. The effects of bending on the gate dielectric in terms of important performance parameters have been studied and it is shown that the devices maintain their high performance even when flexed to a curvature radius of 15 mm. As a result, such devices possess a great potential for low-power, flexible electronics future applications like flexible displays.

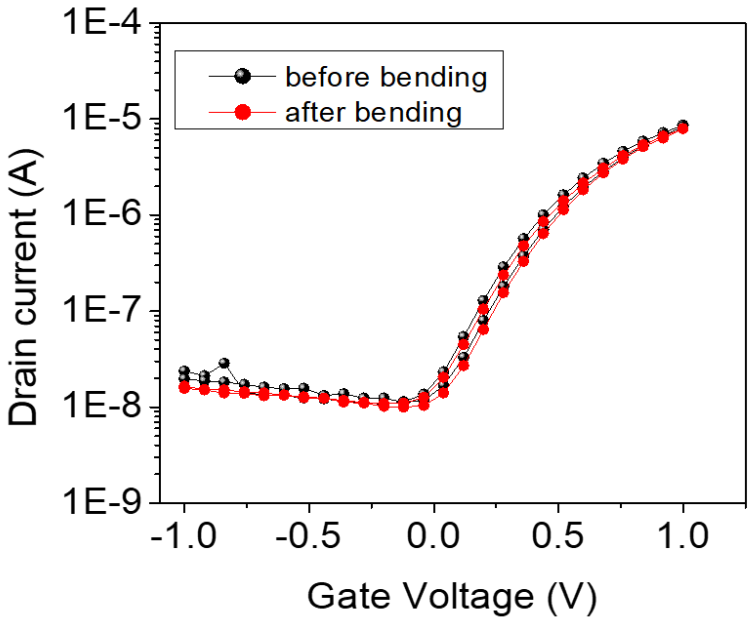


Figure 6.14: The transfer characteristics of flexible IGZO-TFT before and after bending with operating voltage, $V_G = V_D$ of 1V.

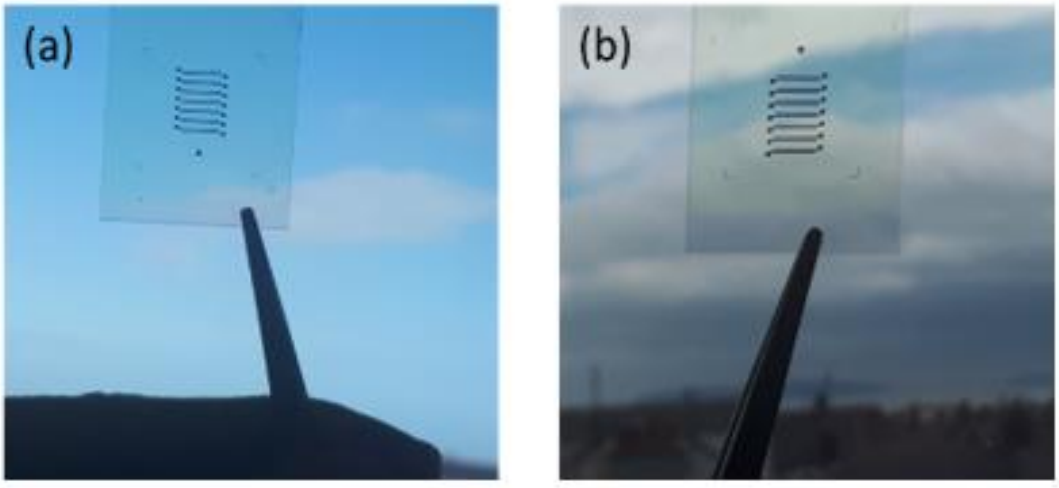


Figure 6.15: (a) Image of manufactured IGZO TFT on ITO substrate, (b) Image of manufactured IGZO TFT on flexible AgNW electrodes.

## 6.9 Transparent IGZO TFTs on AgNW and ITO Electrodes

In this section transparent IGZO TFTs on flexible AgNWs TCEs are presented and their electrical and optical properties are compared to ITO based devices. AgNW TCEs were manufactured and post processed by using the same process as described in Chapter 4.

Shown in figure 6.15 (a) the image of manufactured IGZO TFT on an ITO substrate and figure 6.15 (b) the image of manufactured IGZO TFT on flexible AgNW electrodes. The E-beam evaporated $Al_2O_3$ layer (168nm) was used as the gate dielectric. The channel length of these devices was 90µm and width 5mm.

Table 6.5: Performance parameters of AgNW gated and ITO gated IGZO TFTs.

| Operating voltage $V_D$ (V) | ITO gated Performance Parameters | | | | AgNW gated Performance Parameters | | | |
|---|---|---|---|---|---|---|---|---|
| | $\mu_s$ [$cm^2V^{-1}s^{-1}$] | $V_T$ [V] | $I_{on}/I_{off}$ [ratio] | SS mV/dec | $\mu_s$ [$cm^2V^{-1}s^{-1}$] | $V_T$ [V] | $I_{on}/I_{off}$ ratio | SS mV/dec |
| 2 | 5.04 | 0.57 | 1.04E+03 | 310 | 1.72 | 0.48 | 1.52E+03 | 185 |
| 3 | 10.50 | 0.77 | 1.44E+04 | 388 | 2.3 | 0.91 | 1.34E+04 | 188 |

Both ITO, as well as AgNW TCE, gated IGZO TFTs were working at low operating voltage as low as 2V. Performance parameters of AgNW gated and ITO gated IGZO TFTs are compared in Table 6.5. The devices show high mobility, high on-off ratio, low threshold voltage and small subthreshold slope as can be observed from Table 6.5. K. S. Kim et al, reported IGZO TFT on ITO electrode with mobility of 7.86 $cm^2V^{-1}s^{-1}$, $V_T$ = -0.23 V and SS =340 mV/dec [225].

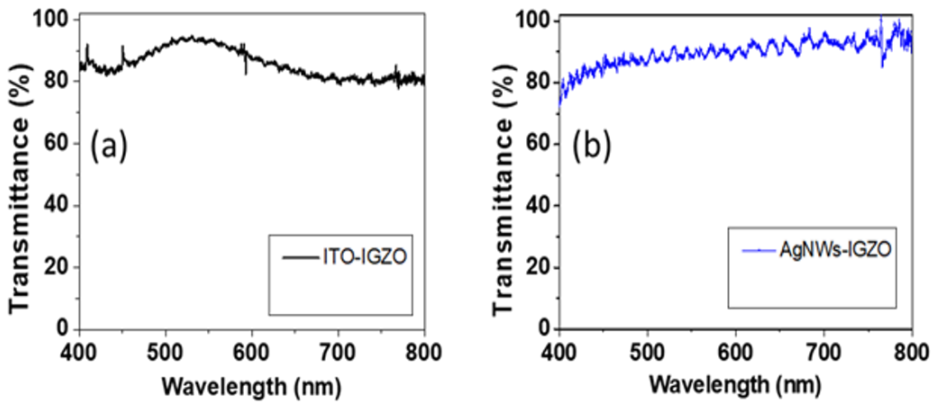


Figure 6.16: Transmittance as a function of wavelength for (a) ITO gated IGZO TFT and (b) AgNW TCE gated IGZO TFT.

Shown in Figure 6.16 the transmittance as a function of wavelength for (a) ITO-IGZO film and (b) AgNWs-IGZO film. The transmittance at 550 nm of 91.2% ($R_{Sh}$ of 60 $\Omega sq^{-1}$) for ITO-IGZO film, however for AgNWs-IGZO film 89.6% ($R_{Sh}$ of 12 $\Omega sq^{-1}$) was measured.

Shown in Figure 6.17 the transfer and output characteristics of IGZO transparent TFTs gated with ITO and AgNW conducting electrodes. It can be clearly observed from the transfer characteristics that ITO gated TFTs shows higher off state current of the order of one decade as compared to AgNW film gated TFTs. However, ON state current is higher of the order of one decade for ITO gated TFTs as compared to AgNW film gated TFTs.

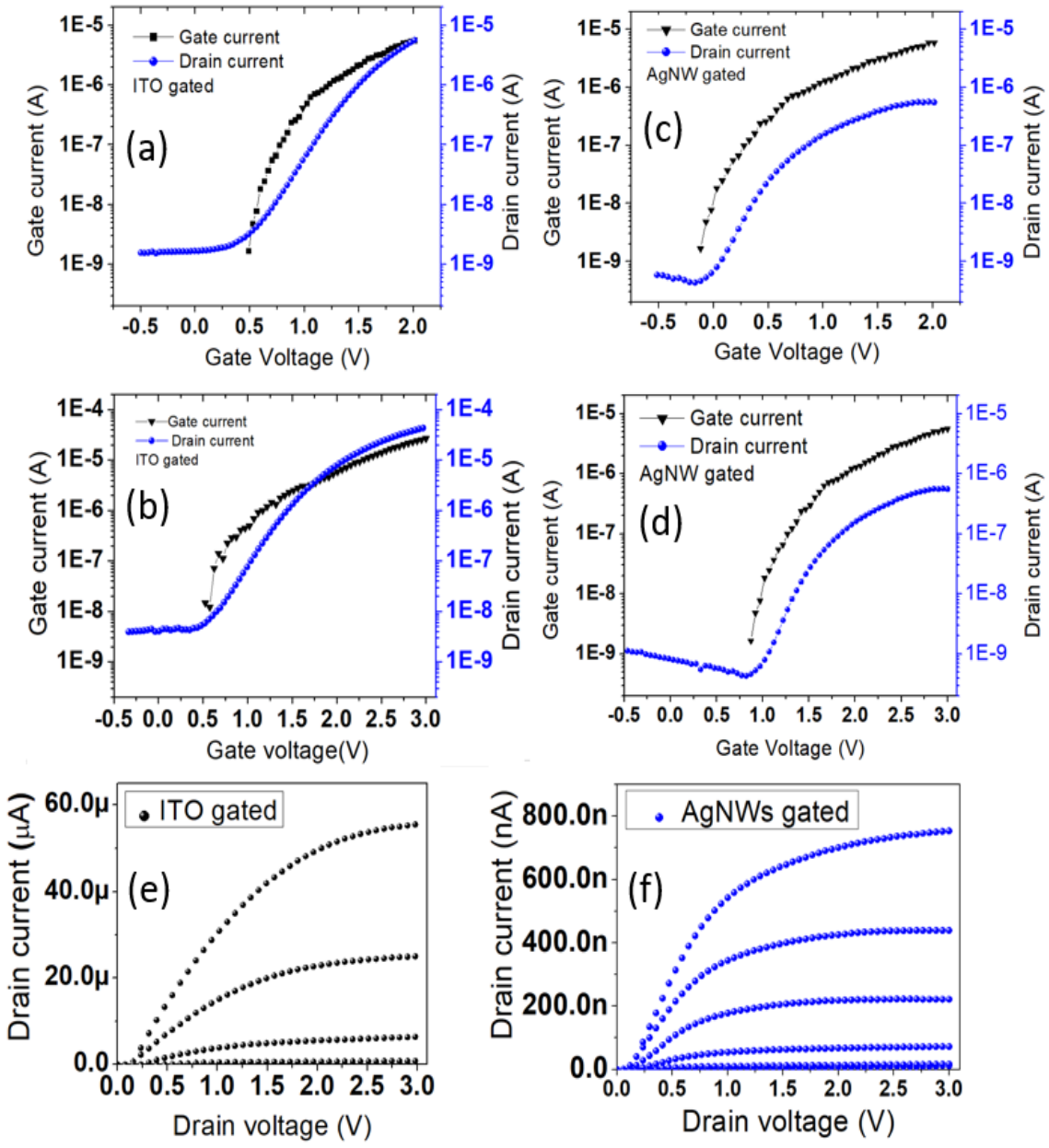


Figure 6.17: Transfer characteristics of ITO gated (black) and AgNWs gated IGZO-TFTs.

## 6.10 Summary

Positive gate bias-induced threshold voltage instability phenomenon of IGZO TFTs is investigated. A combination of device data and DOS analysis is explained in order to observe the difference between passivated and unpassivated TFTs. The influence of CYTOP passivation, white light illumination on the stability of IGZO thin film transistor is also explained. The work reports IGZO TFTs which have been fabricated using E-beam deposited high-k dielectric ($Al_2O_3$) onto a plastic substrate. The devices show a low operating voltage ($V_D$) of 1 V, a high current on-off ratio >$10^3$, threshold voltage $V_T$ of 0.16V, mobility of 28 $cm^2V^{-1}s^{-1}$ and a low subthreshold swing <200 mV/decade. The performance shows great potential for low-power, flexible electronics. The performance of ITO gated and AgNW film gated IGZO TFTs is explained and results are compared.

# Chapter 7. Conclusions and Further Work

## 7.1 Conclusions

The work reported in this thesis is on the development of flexible and transparent conducting electrodes (TCEs) such as silver nanowire (AgNW) TCEs, metal oxide thin film transistors (TFTs) with the aim of improving their stability and performance in real world conditions. This is important as for devices to become commercially viable they must make the transition from laboratory to large area electronics products that can be of real use. In-Depth literature of TCEs and metal oxide TFTs was given, where fundamental properties of AgNWs, metal oxides semiconductors and the basic operation principle of TFTs are explained. TCEs based on various materials, applications and their post processing methods used in literature are discussed. State-of-the-art performances for AgNWs TCEs and metal oxide TFTs were reviewed. Process optimization techniques, Taguchi methods and Plackett-Burman design were also discussed.

At the onset of this Ph.D., an indoor thermal embossing and NIL systems were setups for post processing of AgNW TCEs. This enables AgNW TCEs post processing to improve the electrical and surface properties after thermal embossing. The post processing relied upon three sequential steps; thermal embossing, infrared sintering and a nitrogen plasma treatment. This process leads to the demonstration of AgNWs films with a sheet resistance of 2.5 $\Omega$ $sq^{-1}$and 85% transmittance with world leading FOM = 933, reported FOM is 487.9 using expensive DC magnetron sputtering (Vacuum process). However, our manufacture of AgNW TCEs was based on low-cost spray coating in ambient conditions.

To evaluate the long-term stability of the post processing upon the AgNWs stability, a bespoke accelerated lifetime testing (ALT) system was constructed. For this new circuit, ALT was designed and implemented on the printed circuit board with a switch matrix composed of relays, diodes and BJTs. This allowed high current biasing of the AgNW electrodes and repeated resistance calculations after a regular period, to quantify the degradation of AgNW TCEs in different accelerated real-world environmental conditions. X-ray photoelectron spectroscopy was used to understand the improvement in long-term stability. The thermally embossed and aged samples show low levels of sulphur indicating why these samples remain stable for a long time. A greater proportion of the AgNWs are submerged into the underlying PMMA buffer layer, hence

AgNWs remain less susceptible to environmental ageing. The overall properties of the developed AgNW electrodes show enhanced properties over the incumbent technology; ITO.

The optimisation of high-k dielectric manufacture and ZnO deposition process using a combinational, DOE approach is reported in Chapter 5. Correlation between the manufacturing process parameters and the device characteristics was investigated. An important observation from the results is that the manufacturing parameters of the dielectric layer of the TFTs have a strong influence on the TFT device performance. This procedure can be applied for the optimization of other devices in printed/flexible electronics to improve the fabrication process and to speed up the development of new low-cost products.

Wide bandgap ($E_g$ = 3.37 eV) ZnO material is used for the manufacturing of low voltage TFTs and these TFTs are well suited to UV sensing applications. It was observed that the electrical characteristics of both ZnO TFT sprayed and sputtered are altered after exposure to UV light. However, the magnitudes of these changes are larger in sprayed ZnO TFT than sputtered as their surface structure has a greater affinity with the absorption and desorption of oxygen molecules on its surface. From the perspective of UV sensing, ZnO TFT on-current in the saturation regime appears to be the most suitable performance parameter for examining differences in UV exposure.

The effect of the substrate temperature (during ZnO deposition by spray pyrolysis and annealing temperature after sputtering) on the structural, optical, and electrical transport properties of ZnO TFTs has been investigated. An increase of the substrate deposition/annealing temperature to 450 $^0$C resulted in ZnO films with enlarged crystal size. Therefore, TFTs based on ZnO films grown at substrate temperatures in the range of 300 to 450 $^0$C exhibit the highest electron mobility. The present results demonstrate the possibility of depositing high optical and electronic quality ZnO films onto large area substrates using spray pyrolysis, which is attractive for the electronics industry, since the pyrolysis spray technique is inexpensive, it does not need vacuum steps and is easily applied to large scale electronics.

Understanding the origin of electrical instability in metal oxide TFTs over long periods of time is also essential to realize high performance circuits. Therefore, a positive gate bias-induced threshold voltage instability phenomenon of IGZO TFTs was investigated. The influence of CYTOP passivation and white light illumination on the

stability of IGZO thin film transistors is also reported. A density of states analysis was performed in order to observe the difference between passivated and unpassivated TFTs; demonstrates the trap states at the semiconductor/dielectric interface.

Furthermore, the performance of the flexible IGZO TFTs which have been fabricated using E-beam deposited high-k dielectric ($Al_2O_3$) onto a plastic substrate, demonstrating low operating voltage ($V_D$) of 1 V, a high current on/off ratio >$10^3$, threshold voltage $V_T$ 0.16V, mobility of 28 $cm^2V^{-1}s^{-1}$ and a low subthreshold swing <200 mV/decade are reported. However, the gate leakage current was high and this needs significant improvements. The performance of ITO gated and AgNW film gated IGZO TFTs is reported and results are compared.

Flexible electronics applications are expected to grow substantially over the next 10 years. These types of devices utilise new materials and production processes, which have not been previously used in an industrial context. The need to understand and optimise performance in a rapid manner has become imperative. Given the complexity and challenges of new flexible electronics components, the 'multivariate' approach reported in Chapter 5 could be adopted more widely by the industry to improves the reliability and performances of such devices.

## 7.2 Future Work

It was envisaged that we would fabricate a CMOS inverter using organic p-type and IGZO n-type devices but time imposed a limitation on completing this. Nevertheless, resistive mode inverters are reported. IGZO TFT based N-MOS resistive inverters were fabricated. Photolithography and lift-off process were used to pattern the source/drain metallization as shown in Figure 3.11 in chapter 3. The individual transistors with 5 to 100-μm channel lengths were measured to have the highest saturation mobility of 17 $cm^2V^{-1}s^{-1}$, the subthreshold swing of 388 mV/decade, and current on-off ratios in excess of $10^7$. The basic design of a resistive load inverter is shown in Figure 7.1 (a). Here, IGZO TFT acts as the driver transistor and the load consists of a simple linear resistor $R_L$. The resistive load inverter voltage transfer characteristics were measured using a number of load resistances varying from 100Ω to 1MΩ. Logic operations were satisfactorily demonstrated for a bias voltage of 5 to 25 V.

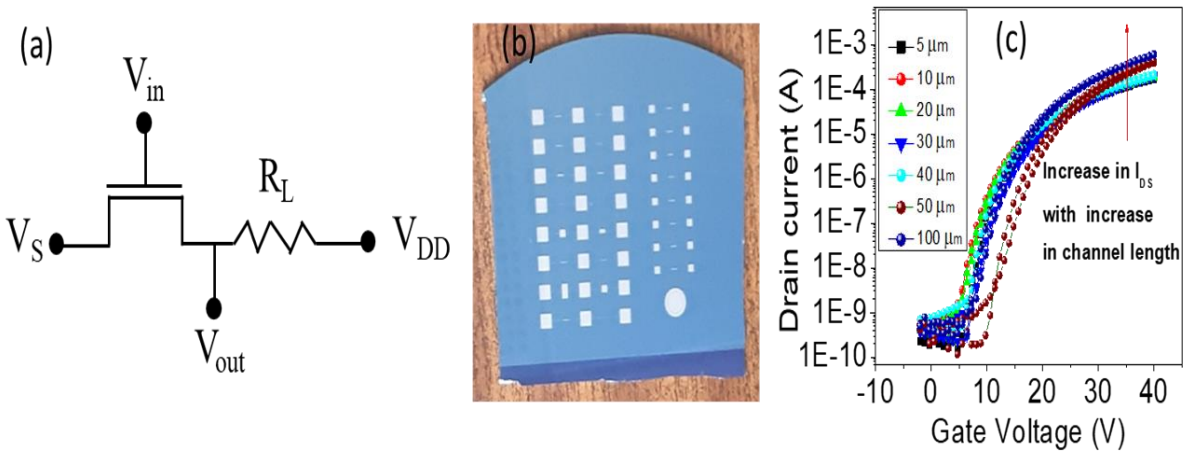


Figure 7.1: (a) Resistive load NMOS inverter biasing circuit, (b) IGZO TFTs on $SiO_2$/Si substrates with different channel lengths, (c) Transfer characteristics of IGZO TFTs with several channel lengths.

Digital inverter quality is often measured using the voltage transfer characteristics (VTC), which is a plot of output voltage as a function of the input voltage. Shown in Table 7.1, the important inverter parameters including noise margin, and operating logic levels obtained from VTC. The two corners of the VTC are very important, as the slope or gain (A) is –1 here and are termed as $V_{IL}$ and $V_{IH}$ points, shown in Figure 7.2 (b). The point at which $V_{in} = V_{out} = V_M$ is the transition point and called the inverter threshold voltage or switching threshold voltage. The noise that may get attached and vary these voltages levels. Noise tolerances for digital circuits are termed as Noise Margin NM (Low, High). Therefore, Noise Margin $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$. The NM should be wide for stable operation of the inverter and high noise immunity.

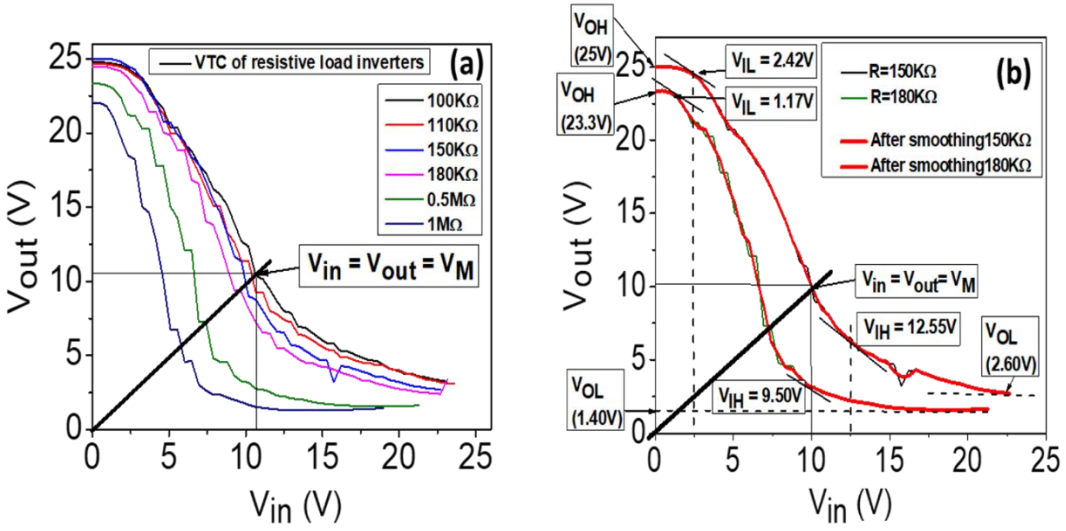


Figure 7.2: (a) Experimentally measured voltage transfer characteristics (VTC) of NMOS resistive inverter with different loads from 100 KΩ to 1 MΩ, (b) VTC of NMOS resistive inverter showing important voltages of the inverter.

Table 7.1: Important inverter parameters obtained from the VTC of resistive load inverter using IGZO TFT.

| Important voltages of Inverter (V) | Resistive loads | | | | | |
|---|---|---|---|---|---|---|
| | 100 KΩ | 110 KΩ | 150 KΩ | 180 KΩ | 0.5MΩ | 1 MΩ |
| $V_{OH}$ | 24.94 | 24.82 | 25 | 24.51 | 23.31 | 22.07 |
| $V_{OL}$ | 3.31 | 3.12 | 2.68 | 2.37 | 1.42 | 1.22 |
| $V_{IL}$ | 2.14 | 2.08 | 2.2 | 1.95 | 1.39 | 0.82 |
| $V_{IH}$ | 13.87 | 13.43 | 12.81 | 12.12 | 8.77 | 7.24 |
| $V_{M}$ | 10.71 | 10.42 | 10.02 | 9.48 | 7.26 | 5.73 |
| $NM_{L}$ | -1.17 | -1.04 | -0.48 | -0.42 | -0.03 | -0.4 |
| $NM_{H}$ | 11.07 | 11.39 | 12.19 | 12.39 | 14.54 | 14.83 |

Shown in Figure 7.3 is experimentally measured NMOS resistive inverter response to square wave input signal, (a) 5V supply voltage, 1MΩ resistance, and 1000pF capacitance (b) 5V supply voltage, 2MΩ resistance, and 1000pF capacitance,(c) 5V supply voltage, 5MΩ resistance, and 1000pF capacitance, (d) 5V supply voltage, 10MΩ resistance, and 1000pF capacitance,(e) 20V supply voltage, 1MΩ resistance, and 1000pF capacitance and (f) 5V supply voltage, 5MΩ resistance, and 1000pF capacitance.

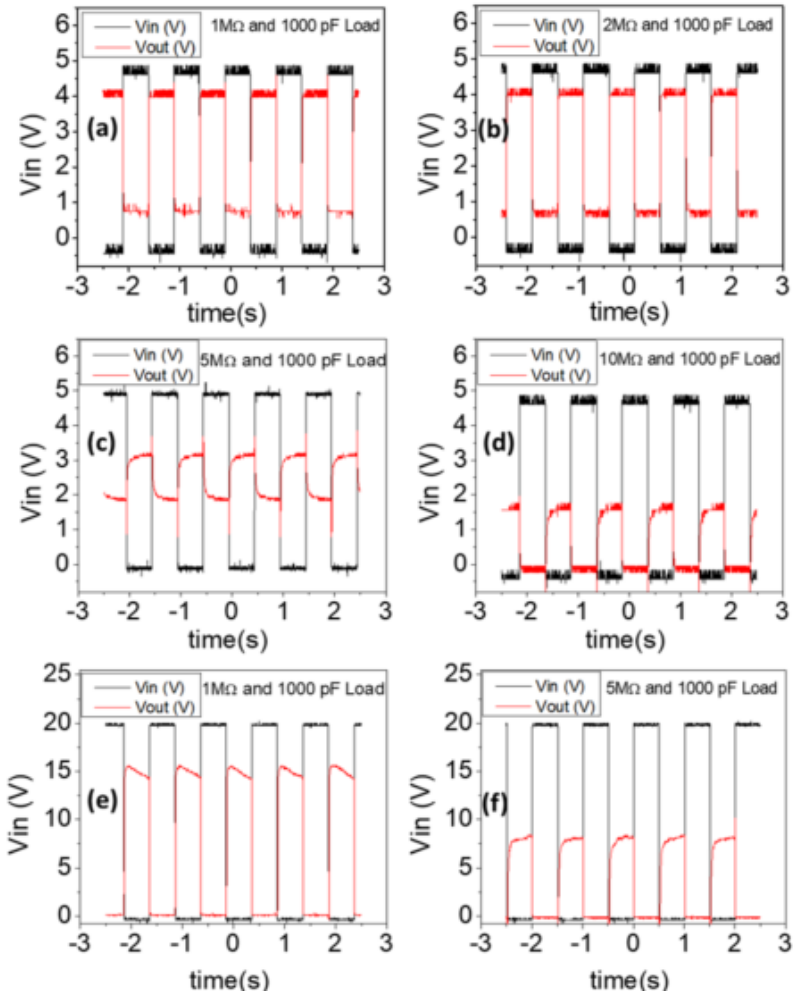


Figure 7.3: Experimentally measured NMOS resistive inverter response to square wave input signal, (a) 5V supply voltage, 1MΩ resistance, and 1000pF capacitance (b) 5V supply voltage, 2MΩ resistance, and 1000pF capacitance,(c) 5V supply voltage, 5MΩ resistance, and 1000pF capacitance, (d) 5V supply voltage, 10MΩ resistance, and 1000pF capacitance,(e) 20V supply voltage, 1MΩ resistance, and 1000pF capacitance and (f) 5V supply voltage, 5MΩ resistance, and 1000pF capacitance.

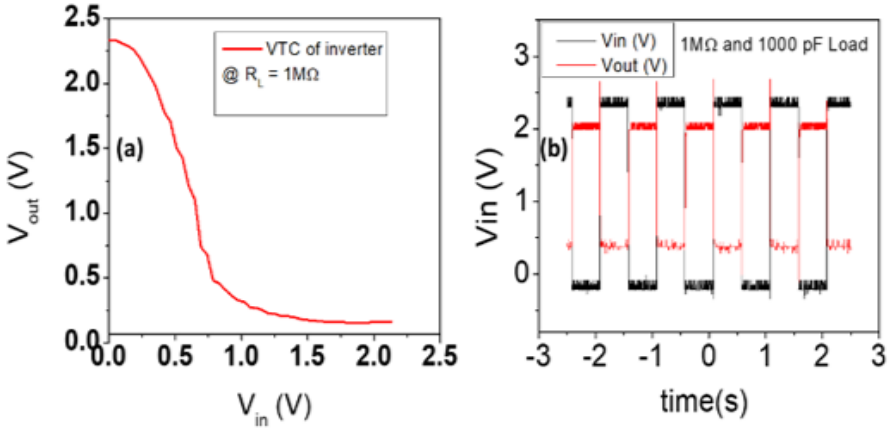


Figure 7.4: (a) Experimentally measured voltage transfer characteristics (VTC) of flexible NMOS resistive inverter (b) Experimentally measured flexible NMOS resistive inverter response to the square wave input signal, 5V supply voltage, 1MΩ resistance, and 1000pF capacitance.

Rise time ($t_r$) is calculated, during the transition, when output switches from 10% to 90% of the maximum value and fall time ($t_f$) when output switches from 90% to 10% of the maximum value. According to our testing oscilloscope accuracy and the constructed circuit using 1MΩ resistance, 1000pF capacitance, the best rise, and fall times were extracted to be ~7.5 ms (Figure 7.3 (a)).

Similarly, using low voltage flexible IGZO TFTs described in earlier section 6.7, VTC and transient response of low voltage resistive inverter was measured using 1MΩ, 1000pF load and shown in Figure 7.4.

Flexible metal oxide TFTs are close to becoming a viable commercial technology, as the obstacles of stability and cost are being overcome. Metal oxides and organic dinaphtho[2,3-b:2′,3′-f]thieno [3,2-b]thiophene (DNTT) both are stable materials, flexible CMOS circuits based on these materials are of importance. As active layer materials become more stable and achieve higher mobilities, the importance of preventing the ingress of water and oxygen by the use of effective encapsulation to reduce interface traps come to the forefront.

To gain more understanding of the trapping mechanisms and finding the origin of the degradation, it would be necessary to investigate the chemical changes in the metal oxide TFTs using techniques such as charge accumulation (CAS) spectroscopy. Access to such equipment would allow changes due to the chemical interaction of the semiconductor with $O_2$ and $H_2O$ to be identified and compared to the results obtained from electrical measurements.

New accelerated life test procedures, for example, time-varying step-stress tests are proposed for testing the stability of AgNW TCEs and metal oxide TFTs. In step-stress accelerated testing, the test devices are subjected to successively higher stress levels in predetermined periods, and thus follow a time-varying stress profile. The devices usually start at a lower stress level at a predetermined time, the stress is increased and the test continues. The test is terminated when all devices have failed or when a certain number of failures are observed. Step-stress testing can substantially reduce the reliability test's duration.

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# Appendix A Surface Roughness Parameters

This appendix (A) details the theory and mathematical equations of surface roughness parameters used to define physical properties of AgNW TCEs, gate dielectric and active layer of TFTs during this PhD research work.

## Roughness

Among height parameters, the roughness average ($R_a$) is the most widely used because it is a simple parameter to obtain when compared to other surface roughness parameters. The roughness average is defined by equation (A.1) given below [226]:

Where Z(x) is the function that defines the surface profile analysed in terms of height (Z) and position (x) of the sample over the evaluation length "L" Thus, the Ra is the arithmetic mean of the absolute values of the height of the surface profile Z(x). Roughness average is also called as the Arithmetic Average (AA), Centre Line Average (CLA) or Arithmetical Mean Deviation of the Profile. The average roughness is just the mean absolute profile and its disadvantage is that it does not make any distinction between peaks and valleys on surface of sample. The average roughness has its own advantages and disadvantages. Advantage is that less sophisticated instrument, for example, a profilometer can provide ($R_a$).

$$R_a = \int_0^L \frac{Z(x)}{L}\, dx \tag{A.1}$$

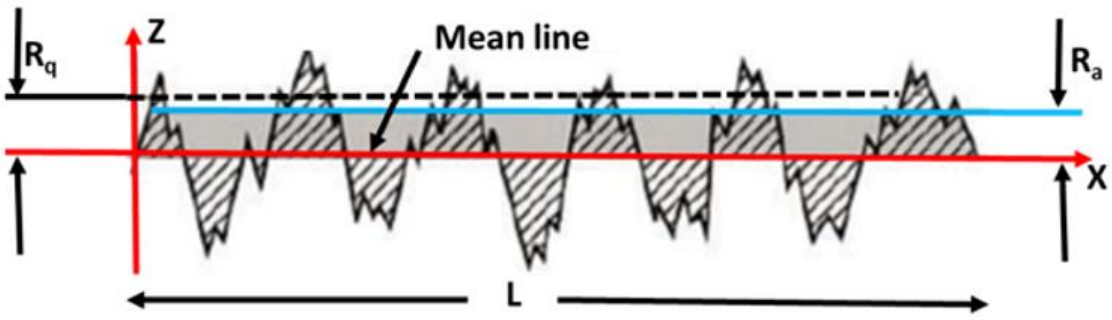


Figure A.1: Profile of a surface (Z). It represents the average roughness Ra and Rq is the RMS roughness based on the mean line (B.C. MacDonald & Co, 2011) [50].

Another surface roughness parameter is root mean square of roughness ($R_q$). The root mean square (RMS) is a statistical measure and is widely used in different fields of science and technology. The root mean square of roughness ($R_q$) is a function that takes the square of the measured values. The RMS roughness of a surface is similar to the roughness average, however the only difference being the mean squared absolute values of surface roughness profile. The advantage of $R_q$ is that it is more sensitive to peaks and valleys than the average roughness $R_a$ due to the squaring of the amplitude in its calculation. The software does not need to be sophisticated in order to measure $R_q$ and for this reason most of the surface analysis equipment provides $R_q$. The function $R_q$ is defined (Gadelmawla et al., 2002) by equation (A.2) as follows:

$$R_q = \left[\int_0^L Z^2(x)/L\, dx\right]^{1/2} \tag{A.2}$$

Ten-point average roughness ($R_z$) is the arithmetic mean of the five highest peaks added to the five deepest valleys over the evaluation length, L measured shown in Figure A.2.

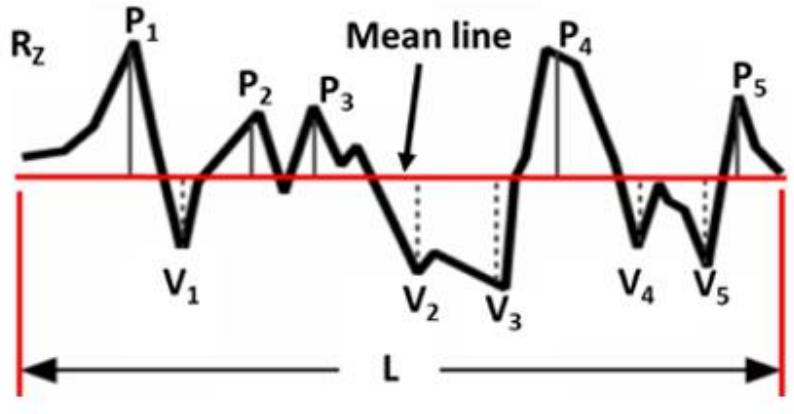


Figure A.2: a) Profile of a surface (Z). It represents the average roughness Ra and Rq is the RMS roughness based on the mean line (B.C. MacDonald & Co, 2011).

# Appendix B Fabrication recipe of AgNWs TCEs

This appendix (B) explains the recipe and details of developed spray technique for fabrication of transparent conducting electrodes (TCEs).

Three types of silver nanowires were used for fabrication of AgNWs TCEs namely *thin-short* nanowire; AgNWs-60S ($d_{mean}$ = 60 nm, $l_{mean}$ = 20-30 µm), *thin-long* nanowire; AgNWs-30L ($d_{mean}$ = 30 nm, $l_{mean}$ = 100-200 µm) and *thick-long* nanowires; AgNWs-100L ($d_{mean}$ = 100 nm, $l_{mean}$ = 100-200 µm). The shorter nanowires are advantageous for achieving high conducting networks at low concentration and the longer nanowires provide higher conductivity performance. The combined advantages of short and long nanowire were exploited by coating them together. Two mixed silver nanowires composition were prepared, one consisted of the type: *thin-short* nanowires (AgNws-60S) with *thin-long* nanowires (AgNWs-30L), denoted as 'AgNWs-M1', and another one consist of the type: *thin-short* nanowires (AgNWs-60S) with *thick-long* nanowires (AgNWs-100L), denoted as AgNWs-M2. The results show a moderate improvement in the electrical/optical performance and in the surface roughness (Shown in chapter 4).

Silver nanowires of the type AgNWs-60S, AgNWs-30L and AgNWs-100L (silver purity 99.5%, concentration 20 mg/mL in ethanol) were purchased from ACS materials. All materials were diluted with ethanol to the concentration of 0.5 mg/mL prior to spray coating. Flexible transparent substrates of planarised polyethylene-napthalate (PEN) with thickness 125 µm were used for this work. PEN was spin coated with poly methyl methacrylate (PMMA) (molecular weight 495K, 8% solution in anisole) purchased from Microchem. For this work, a PMMA buffer layer was employed to reduce the surface roughness of the substrates. HPLC grade isopropyl alcohol (IPA), ethanol (EtOH) and acetone were purchased form Sigma-Aldrich and used as such.

Mixed composite silver nanowires AgNWs-M1 dispersion was prepared by mixing AgNW-60S and AgNWs-30L as supplied in 1:1 volume by volume (V/V) ratios and then diluted with ethanol to 0.5 mg/mL final concentration. "After some initial tests, the ratio of 1:1 was found to be the optimum, so all benchmarking of performances was done at this ratio." Similarly, AgNWs-M2 was prepared with AgNWs-60S and AgNWs-100L. Silver nanowires dispersions in ethanol of each type (0.5 mg/mL) were sonicated for 5 minutes to minimized aggregates before air spray coating. "Ultrasonication and was used prior to spray coating to ensure that the AgNWs were dispersed in the suspension prior

to spray coating. A short duration was used (<5 minutes) at low power in order to ensure no breakage of AgNWs " For air spray coating, a back pressure of air kept at 1 bar using a piston type oil-less airbrush compressor was used for uniform gas/liquid flow rate (0.2 ml/min) at the nozzle. The spray nozzle diameter was 0.5 mm and the fluid cup capacity was 7 $cm^{-3}$ with the air compressor. Substrates PEN of area 15 mm × 18 mm were thoroughly cleaned with DI water, acetone and IPA followed by drying with a jet flow of nitrogen. PMMA (average molecular weight~15,000) was spin coated on cleaned PEN substrates at 2500 rpm for 20 seconds followed by annealed at 100 $^{o}C$ for one minute. The substrates were placed on the substrate heater at 60 $^{o}C$ and the silver nanowires dispersion was air sprayed onto the heated substrates to evaporate the EtOH. The deposition time for preparing electrodes with $R_{Sh} \approx 25\ \Omega\ sq^{-1}$ was found to be approximately 5 mins ±30 seconds. However, using mixed geometry electrodes, the deposition time was approximately 50%. ZnO nanoparticles (diameter < 100) were purchased from sigma Aldrich. Composite ZnO/ AgNWs transparent electrodes were manufactured by spray coating nanoparticles onto post-processed AgNWs.

Three sequential post processing steps namely thermal embossing, $N_2$ plasma treatment and photonic sintering were applied to fresh sprayed TCEs. The AgNW-coated PEN substrates were inserted into a thermal nanoimprint lithography (NIL) system to compress the AgNW on the surface of PEN at different temperatures, times and pressure. The thermal-embossing process was conducted using a 2" nickel shim, formed from a polished silicon wafer to ensure flatness. The anti-sticking layer BGL-GZ-83 was spin coated onto the nickel shims prior to use in the thermal embossing to avoid sticking of the AgNWs and thermoplastic to the nickel shim during the embossing procedure. Pressure, time and temperature of the embossing step were all varied and the process was optimised using the Taguchi method. The optimal conditions found in this way were 5 Bar, 1 minute and 120°C, respectively. All embossing operations were conducted under ambient pressure rather than under vacuum.

The photonic curing was performed using a Novacentrix system to rapidly anneal the surface for enhanced electrical conductivity. Samples were mounted to the system and exposure varied from 450V, 400µs to 750µs with single energy pulse 1488mJ/$cm^2$ to 2712mJ/$cm^2$. The process ensured sintering occurred within the top 1µm of the film surface, rather than the entire thickness of substrate and therefore impacted mostly upon the AgNW film. By concentrating the sintering so close to the surface, flexible and polymeric substrates can be used and surface damage can be minimised. The exposure

time or energy pulse duration was varied to optimise the lowest sheet resistance. The optimal energy was set at 700µs with an energy of 2549mJ/cm$^2$.

A plasma treatment step was also applied to AgNW-coated PEN substrates. The AgNW electrodes were Nitrogen ($N_2$) plasma treated for 2 minutes, which result in reduction of sheet resistance, although no change in transmittance was noted. The treatment process was conducted using a Diener second 'Nano' plasma treatment system at ambient pressure after a 30 seconds nitrogen purge. In this system, a 13.56 MHz RF Generator was used at 100 watts power to generate $N_2$ plasma for 120 seconds.

# Appendix C Aluminum Anodization Process and Transfer Curves

This appendix (C) details the process of the aluminium anodization and transfer curves of ZnO TFTs manufactured using Plackett–Burman designs.

The aluminium anodisation process was carried out by using the Al-coated glass substrate as anode and a stainless-steel sheet (40 mm x 40 mm in area, 1.0 mm thick) as the cathode, both submerged into an electrolytic solution comprising ethylene glycol, deionized water and tartaric acid (0.1 M). The electrodes were kept at a fix distance of 50 mm during the anodisation process, which was carried out in two steps: i) a constant current step and ii) a constant voltage step (using a Keithley SMU model 237). The initial constant current step promotes the growth of an $Al_2O_3$ layer onto metallic Al film. At constant current, the film resistance increases linearly with the thickness, resulting in a linear increase of the applied voltage. The determination of the oxide thickness (t), therefore, depends only on the final voltage (VF) of the constant current step. The oxide thickness follows the relationship t = cVF, where c was empirically determined to be ~ 1.2 nm/V. After the desired final voltage is achieved, the source unit is switched from constant current to constant voltage and an exponential decay of the current is observed. The constant voltage step does not increase the thickness of the $Al_2O_3$ layer but is responsible for eliminating pinholes in the oxide film.

Shown in Figure C.1 and C.2 (please see next page) the transfer curves for ZnO TFTs manufactured using process conditions according to runs # 1 to # 12 used in Plackett–Burman Design (Chapter 5).

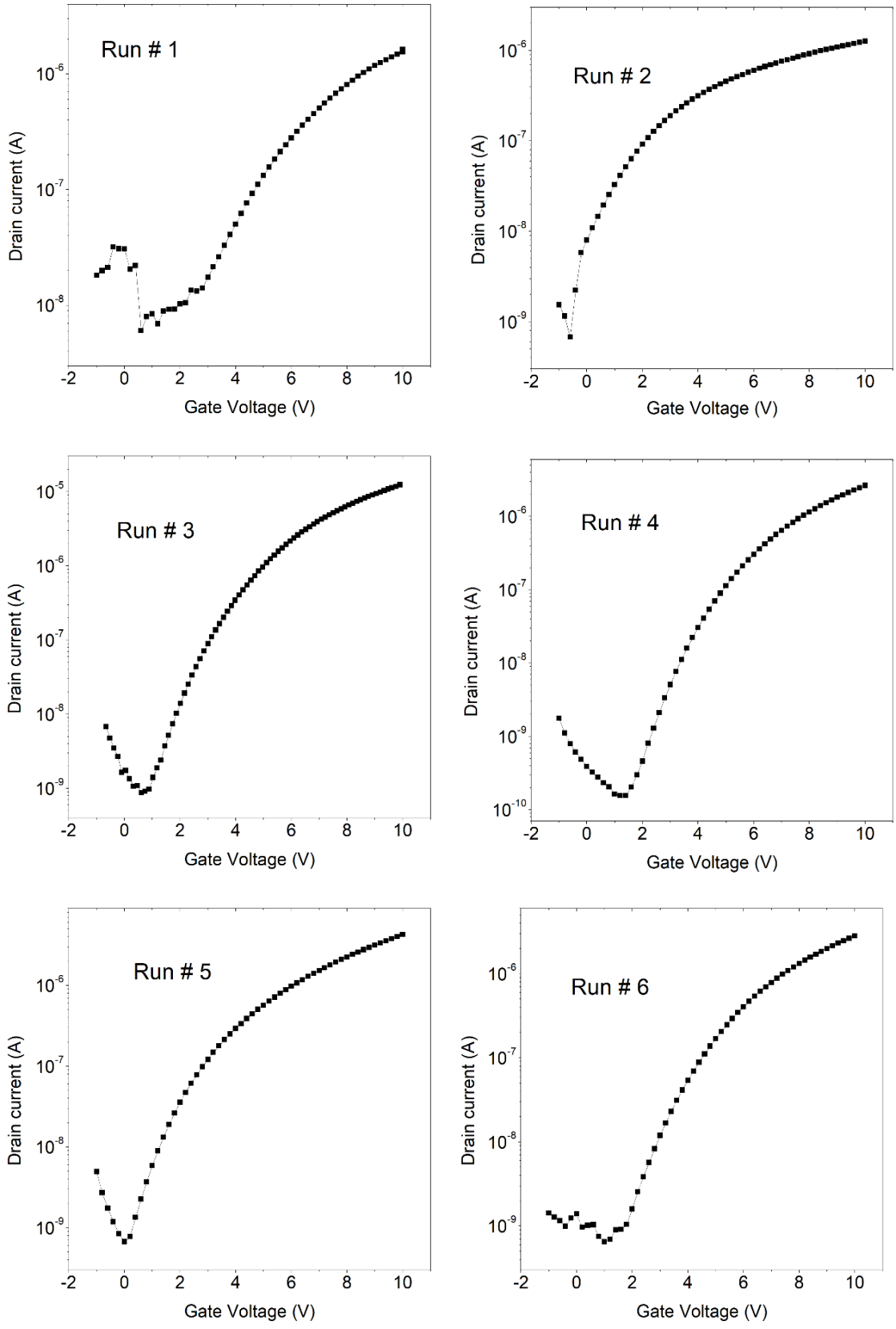


Figure C.1: Transfer curves for transistors built using conditions according to runs # 1 to # 6.

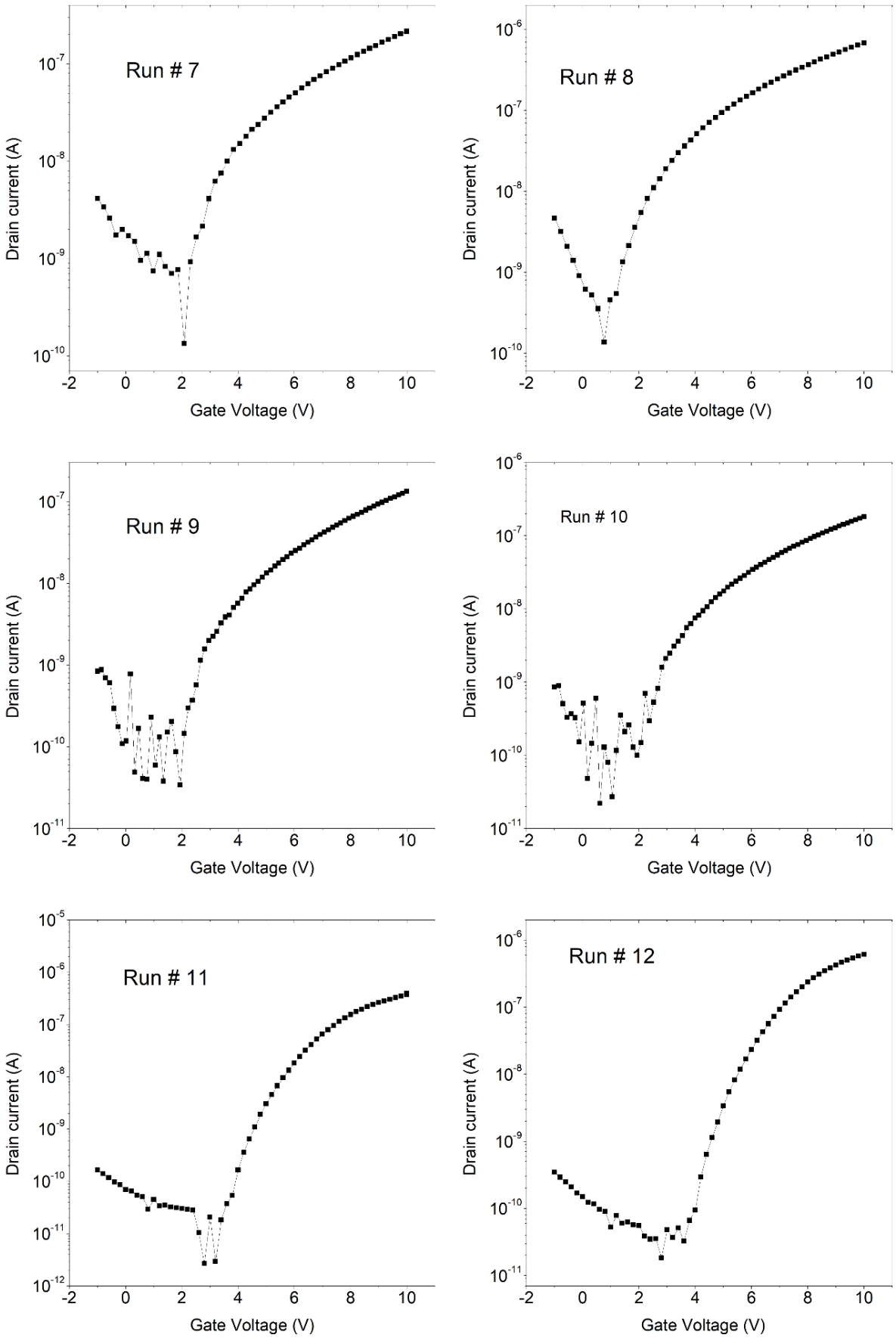


Figure C.2: Transfer curves for transistors built using conditions according to runs # 7 to # 12.