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Enhanced Quasi Type-1 PLL-Based Multi-Functional Control of Single-Phase Dynamic Voltage Restorer

Hafiz Ahmed [1], Samet Biricik [2], Hasan Komurcugil [3] and Mohamed Benbouzid [4,5,*]

[1] Nuclear Futures Institute, Bangor University, Bangor LL57 2DG, UK; hafiz.h.ahmed@ieee.org
[2] Department of Electrical and Electronic Engineering, European University of Lefke, Lefke 99728, Turkey; s.biricik@eul.edu.tr
[3] Department of Computer Engineering, Eastern Mediterranean University, Mersin 10, Famagusta 99628, Turkey; hasan.komurcugil@emu.edu.tr
[4] Institut de Recherche Dupuy de Lôme (UMR CNRS 6027 IRDL), University of Brest, 29238 Brest, France
[5] Logistics Engineering College, Shanghai Maritime University, Shanghai 201306, China
* Correspondence: mohamed.benbouzid@univ-brest.fr; Tel.: +33-2-98018007

Abstract: This paper considers the reference signal generation problem for the multi-functional operation of single-phase dynamic voltage restorers. For this purpose, a single-phase quasi type-1 phase-locked loop (QT1-PLL) is proposed. The pre-loop filter part of this PLL is composed of a frequency-fixed delayed signal cancellation method and a two-stage all-pass filter. Thanks to the frequency-fixed nature, the pre-loop filter is easy to implement and can provide rejection of any measurement offset. Moreover, this PLL benefits from the excellent harmonic robustness property of the conventional QT1-PLL. Small-signal modeling and gain tuning procedures are detailed in this paper. In order to track the reference voltage signals generated by the proposed PLL, a super-twisting sliding mode controller is also presented, which helps to achieve fast dynamic responses. Laboratory-scale prototype-based experimental studies were conducted to validate the developed reference generator and the controller. Experimental results show that the proposed method is fast in detecting and compensating any grid voltage anomalies to maintain constant load voltage despite voltage sag, swell, and harmonic distortions.

Keywords: grid-synchronization; dynamic voltage restorer; converter control system; sliding mode control

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1. Introduction

Power quality problems such as voltage sag, swell, and harmonics can significantly affect the performance of critical loads that are used in hospital, water treatment plant, data center, etc. In addition to harmonics, voltage sag and swells are quite common in power grid and can be caused by many reasons such as lightning strike, accident, short circuit, over loading, switching on or off large electrical loads, etc. In the case of water treatment plant, voltage sag/swell can interrupt the treatment process including dissolved air flotation, filtration, and disinfection. Any interruption in the process can take up to 8 h to resolve, causing one-third production loss for the day. This highlights the importance of mitigating voltage-related power quality problems.

In order to address power quality issues such as voltage sag, swell, and harmonics, the dynamic voltage restorer (DVR) became very popular in recent times [1–4]. DVR can compensate voltage sag, swell, and harmonics to maintain desired constant voltage at the critical load side. In the literature, various topologies of DVR are proposed. However, the most basic DVR topology is made of any dc voltage source such as battery, photovoltaic panel, etc., together with a voltage source inverter with LC filter and a transformer. The transformer provides galvanic isolation between the inverter and its secondary is connected between the grid voltage and the load in series. The control system of DVR constantly monitors grid voltage and injects compensation voltage when it detects any deviation from

the desired voltage. This results in maintaining desired load voltage despite various power quality disturbances at the grid.

The detection of voltage sag, swell, and harmonics plays a vital role in ensuring the effective operation of DVR. Voltage sag and swells are typically short-lived incidents with a time range of few milliseconds to a minute [5]. As such, fast and accurate detection of sag and swell is essential for fast responsive DVR operation. In the ideal case, voltage sag/swell can be detected very quickly by comparing the voltage magnitude with respect to the ideal magnitude. However, calculating the magnitude can be tricky in the presence of nonlinearities such as harmonics.

The first step in compensation voltage calculation is to generate the reference voltage, which should be in-phase with the measured grid voltage. If the grid voltage is ideal, i.e., has a frequency of 50 Hz (or 60 Hz) and contains no harmonics, then generating the reference voltage is straightforward. However, this is not the case in practice. According to the European standard EN 50160 [6], grid voltage can vary between -3 Hz and $+2$ Hz of the nominal frequency. However, the grid frequency has to be within 1% of the nominal value, i.e., ± 0.5 Hz for 99.5% of the time. Moreover, harmonics are almost always present in the grid due to the ever increasing penetration of nonlinear loads and converter-interfaced distributed energy sources. All these factors complicate the reference voltage calculation.

In order to address the non-ideal characteristics of the measured grid voltage, researchers often rely on phase-locked loop (PLL) [7–15] or similar techniques to generate the reference voltage for DVR. Using PLL, first, the instantaneous phase of the grid voltage fundamental component is estimated. This can then be used as the unit template for the reference voltage. By multiplying the unit template with the desired amplitude, the actual reference grid voltage can be calculated. In this study, we are considering a single-phase DVR. However, traditional PLLs in the form of synchronous reference frame (SRF) PLLs work only for three-phase systems. For single-phase systems, an additional orthogonal signal generator (OSG) is required to implement SRF-PLL. In the single-phase DVR literature, various OSGs have already been used. In [16], a second-order generalized integrator (SOGI) is used as the OSG. The effect of DC offset is not considered in [16]. Moreover, despite having band-pass filtering property, traditional SOGI-PLL cannot completely reject the dominant harmonics. Thus, multiple SOGIs need to be placed in parallel in order to reduce the effect of dominant harmonic components. This can make the overall system computationally complex. It is to be noted here that the conventional SRF-PLL can be made robust to harmonics and DC offset by considering a slow loop-filter, i.e., by reducing the bandwidth. This has been considered in [17]. Although this is an interesting practical solution, this strategy is suitable for voltage compensation but not harmonics.

Self-tuning filter (STF) is similar to SOGI; however, in the case of STF, the error feedback is independent of the grid frequency. In [18,19], the authors have applied STF as the reference generator without considering frequency adaptation. As such, the reference generator in [18,19] can be limiting when the grid frequency varies significantly. Quarter-delay is another popular method for generating orthogonal signal. This approach is considered in [20]. However, in off-nominal frequency condition, the required delay would be fractional which increases computational complexity. In [21], an adaptive notch filter (ANF) is used as the reference generator. However, the considered ANF did not use gain normalization. This can make the convergence time slow in the presence of voltage sag.

Based on the literature review, it is clear that there is demand for a reference generator that is robust to harmonics and DC offset while at the same time is computationally simple to implement. For this purpose, in this study, a quasi type-1 PLL [22–24] is considered. This PLL has been selected for several reasons. Firstly, it can provide amplitude normalization without using any low-pass filter unlike conventional SRF-PLL, cf. [25]. Use of additional low-pass filter in the amplitude normalization block will introduce tuning complexity as there is one more gain to tune. Secondly, this PLL provides good harmonic robustness thanks to the use of a moving-average filter. Finally, it has only one gain to tune unlike SRF-PLL where the loop-filter has two tuning parameters. However, this PLL can work only for three-phase system. Thus, a single-phase version of this PLL is proposed in this study.

For this purpose, first, a half-cycle delayed signal cancellation method is applied to reject the DC offset. Then, a frequency-fixed all-pass filter (APF) [26] is applied to generate the orthogonal signal. However, single-stage APFs will generate double frequency oscillations in off-nominal frequency conditions. As such, a two-stage APF is considered that can eliminate the double frequency error. The APF is selected in this study as it can generate orthogonal signals without using any tuning gain unlike other choices available in the literature such as SOGI [16,27], ANF [21], etc. This is beneficial from the tuning simplicity point of view. Finally, the filtered grid voltage signal and its orthogonal component are used as the inputs to the quasi type-1 PLL. A small-signal model of the proposed PLL is developed and validated. Finally, tuning of the PLL gain is also presented. Compared to conventional PLL techniques summarized in [28], our approach is very simple to tune as it has only one tuning gain. All the techniques summarized in [28] have at least three parameters to tune if amplitude normalization is considered. Unlike most of the techniques in [28], our quadrature signal generator is frequency non-adaptive. As such, there is no frequency feedback which may be beneficial from the stability point of view.

Once the reference signal is generated, the role of control system is to follow/track the reference. In the literature, synchronous frame approach in the form of proportional-integral (PI) controllers [29] are widely used. Although this controller can be easily designed and implemented, the dynamic response can be slow. In order to enhance dynamic performance, advanced controllers such as model predictive control (MPC) [7,8], $\mathcal{H}_\infty$ [30], and sliding mode control (SMC) [31–33] are proposed in the literature. MPC can be sensitive to model parameters mismatch. Computational complexity can be an issue for $\mathcal{H}_\infty$ controllers. SMC is often a suitable choice for controlling nonlinear systems in the presence of parameter mismatch and/or external perturbations. As such, this technique has been selected in this study.

The rest of this article is organized as follows: Section 2 explains the operation of the proposed DVR together with the error model for controller development. Development of the proposed reference signal generator is provided in detail in Section 3. Development of the sliding-mode controller is provided in Section 4. Experimental results on a laboratory-scale prototype together with simulation results are provided in Section 5. Finally, Section 6 concludes this paper.

2. DVR Modeling and Problem Formulation

In this study, we consider a single-phase DVR. A connection diagram of the DVR is given in Figure 1. In this configuration, the DVR, which is a full-bridge voltage source inverter, is connected in series through a transformer to the protected load. Isolation between the load the DVR is provided by the transformer. Grid voltage sensor is used to continuously monitor the deviation from the reference voltage, and the appropriate compensation voltage is injected by the DVR to maintain the ideal voltage at the protected load terminal. Filter current and compensation voltage dynamics of the DVR are given by the following:

$$\frac{di_f}{dt} = \frac{1}{L_f}(v_i - v_c), \tag{1}$$

$$\frac{dv_c}{dt} = \frac{1}{C_f}\left(i_f - i_g\right), \tag{2}$$

where v_i, v_g, v_c, i_f, i_g, L_f, and C_f denote the input voltage by the DVR, grid voltage, compensation voltage, filter current, filter inductance, and filter capacitance, respectively. The DVR voltage can be expressed as $v_i = uV_{dc}$ where the DC-link voltage is denoted by V_{dc}, and the control signal is given by u. Moreover, in the ideal case, one can also write the following.

$$v_c = v_g - v_L. \tag{3}$$

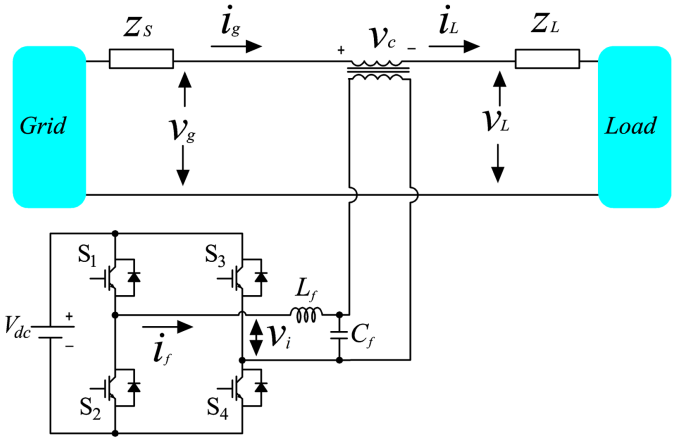

Figure 1. Topology of the considered DVR.

In normal operating condition, the compensation voltage given by (3) will be zero. However, in practice, the grid voltage is never ideal. Various grid anomalies such as voltage sag/swell, harmonics, noise, etc., are present. In this case, (3) can no longer be used for the compensation voltage calculation. In order to ensure that the sensitive load voltage remains as close as possible to the desired voltage, reference voltage needs to be calculated and this voltage should be in-phase with the grid voltage fundamental for the efficient operation by the DVR. Let us consider that the reference voltage is denoted by v_c^{ref}. Then, the tracking error and its derivative are given by the following.

$$\xi_1 = v_c^{\text{ref}} - v_c, \tag{4}$$
$$\xi_2 = \dot{\xi}_1 = \dot{v}_c^{\text{ref}} - \dot{v}_c. \tag{5}$$

Then, by substituting the DVR dynamical Equations (1) and (2) into (4) and (5), the DVR tracking error dynamics can be obtained as follows:

$$\frac{d\xi_1}{dt} = \xi_2, \tag{6}$$
$$\frac{d\xi_2}{dt} = -\delta\xi_1 + \delta u V_{dc} + w, \tag{7}$$

where the coefficient $\delta = 1/\left(L_f C_f\right)$ and the perturbation term $w(t)$ is given by the following.

$$w(t) = -\frac{1}{C_f}\frac{di_g}{dt} - \delta v_c^{\text{ref}} - \dot{v}_c^{\text{ref}}.$$

It is assumed that the perturbation term $w(t)$ has a bounded derivative and is upper bounded by $|\ \frac{dw}{dt}\ | \leq W, W > 0$. Thus, the control of DVR is essentially divided into two parts. In part 1, the problem is to generate the reference voltage v_c^{ref} from the measured grid voltage v_g. In part 2, the problem is to find the control signal u that will ensure that the tracking errors converge asymptotically to zero. These two issues are addressed in the following two sections.

3. Reference Signal Generator

In this Section, reference voltage v_c^{ref} will be generated from the measured grid voltage v_g. For this purpose, let us consider the singe-phase grid voltage signal model in time-domain as provided below:

$$v_g(t) = v_0 + \underbrace{V_p \sin\left(\theta_g\right)}_{v_g^{\varnothing}}, \tag{8}$$

where $|v_0| \geq 0$, V_p, and $\theta_g = \int \omega_g dt, \theta_g(0) = \phi$ are the DC offset, amplitude, and instantaneous phase with ω_g being the grid frequency, and ϕ is the initial phase angle. The frequency is $\omega_g = \omega_n + \delta_\omega$, where $\omega_n = 100\pi$ is the nominal frequency and δ_ω is the deviation from the nominal frequency. For efficient operation of the DVR, the reference voltage should be in phase with the instantaneous phase of the grid voltage θ_g. Thus, the process of extracting θ_g from the measured voltage v_g is considered in this section. For this purpose, a PLL-based approach has been considered in this study. Details are provided below.

3.1. DC Offset Rejection

Measurement offset v_0 causes estimation error in the estimated phase. Thus, rejection of this offset is essential in order to eliminate the steady-state error. For this purpose, the half-cycle delayed signal cancellation (DSC) method is a popular choice in the literature [34,35]. The same approach is considered here. For this purpose, let us consider half-cycle delayed version of the signal v_g as follows:

$$\begin{aligned} v_g^{t_d}(t) &= v_0 + V_p \sin\big(\omega_g(t - t_d) + \phi\big), \\ &= v_0 - V_p \sin\big(\theta_g\big), \end{aligned} \tag{9}$$

where $t_d = \frac{T}{2}$ with $T = \frac{2\pi}{\omega_g}$ being the period of the grid voltage signal. Then, the DC offset can be eliminated by the following operation.

$$\hat{v}_g^{\emptyset} = \frac{1}{2}\Big(v_g - v_g^{t_d}\Big). \tag{10}$$

In implementing Equation (10), the actual period of the grid voltage is required. In the off-nominal frequency condition, the amount of required dely could be a fraction, thereby increasing computational complexity. A potential solution is to use the nominal period; however, this will introduce amplitude and phase attenuation in the off-nominal condition. In this study, only extracting the phase is required. thus, appropriate compensation of the phase delay is necessary to eliminate the error. For this purpose, let us consider the transfer function of the DSC operation (10) as provided by the following:

$$\frac{\hat{v}_g^{\emptyset}}{v_g}(s) = \mathrm{G_{dc}}(s) = \frac{1 - e^{-t_d s}}{2}, \tag{11}$$

where the estimated value is indicated by $\hat{}$. The discrete-time version of the transfer function (11) is given by the following:

$$\mathrm{G_{dc}}(z) = \frac{1 - z^{-N_d}}{2}, \tag{12}$$

where the required delay is given by as $N_d = t_d f_s$ with f_s being the sampling frequency. By substituting $s = j\omega_g$, the phase angle of the transfer function (11) is given by the following.

$$\begin{aligned} \angle \mathrm{G_{dc}}(s) &= \tan^{-1}\left\{\tan\left(\frac{\pi}{2} - \frac{T\omega_g}{4}\right)\right\}, \\ &= \frac{\pi}{2} - \frac{T\omega_g}{4}, \\ &= \frac{\pi}{2} - \frac{T}{4}(\omega_n + \delta_\omega), \\ &= \frac{\pi}{2} - \frac{T}{4}\frac{2\pi}{T} - \frac{T}{4}\delta_\omega, \\ &= \underbrace{-\frac{T}{4}}_{k_{dc}}\delta_\omega. \end{aligned} \tag{13}$$

In calculating (13), it is assumed that $\omega_n = 2\pi/T$. Equation (13) shows that the use of nominal period in (10) causes a phase delay of $-k_{dc}\delta_\omega$ in the off-nominal frequency case. This phase needs to be compensated in the loop-filter to eliminate the phase error in the off-nominal frequency condition.

3.2. Tuning-Free Fixed-Frequency Orthogonal Signal Generator

Once the DC offset is eliminated, the signal $v_g^{\varnothing}$ can be used to generate an orthogonal signal component. In this study, we are considering an all-pass filter (APF) [26,36]. APF is a first-order filter, and it can be used to generate orthogonal signals without any tuning gain. This filter can be used either as frequency-adaptive or non-adaptive configurations. In this study, a frequency-fixed operation is considered same as the DC offset rejection method, as highlighted in Section 3.1. The frequency-fixed APF transfer function is given by the following:

$$\frac{v_g^{\varnothing\perp}}{v_g^{\varnothing}}(s) = \text{APF}(s) = \frac{\omega_n - s}{\omega_n + s}, \tag{14}$$

where superscript $\perp$ indicates orthogonal signals. A time-domain block diagram of APF is provided in Figure 2. Similarly to Section 3.1, the frequency-fixed operation of the APF will introduce amplitude and phase attenuation in the estimated orthogonal signal. As such, characterization of the APF is needed to determine the necessary compensation mechanism. Phase-angle of the transfer function (14) is given by the following.

$$\angle\text{APF}(s) = \tan^{-1}\left(\frac{2\omega_g\omega_n}{(\omega_g - \omega_n)(\omega_g + \omega_n)}\right). \tag{15}$$

For small frequency drift, i.e., $\delta_\omega \approx 0$, it can be assumed that $\omega_g + \omega_n \approx 2\omega_g$. Then, the phase angle (15) can be approximated as follows.

$$\begin{aligned}\angle\text{APF}(s) &\approx \tan^{-1}\left(\frac{1}{\frac{\omega_g}{\omega_n} - 1}\right).\\ &\approx -\frac{\pi}{2} - \tan^{-1}\left(\frac{\omega_g}{\omega_n} - 1\right),\\ &\approx -\frac{\pi}{2} - \left(-\frac{\pi}{4} + \frac{\frac{\omega_g}{\omega_n}}{2} + \frac{\left(\frac{\omega_g}{\omega_n}\right)^2}{2!} + \cdots\right).\end{aligned} \tag{16}$$

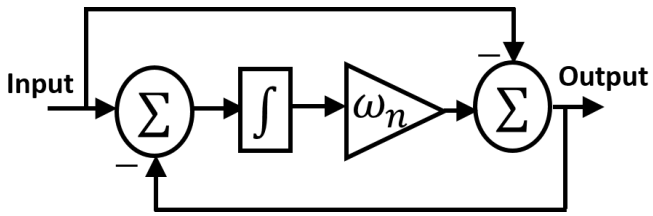

Figure 2. Time-domain implementation of frequency-fixed APF.

By ignoring the high-order (2nd and above) terms from the Taylor series expansion in (16), this equation can be simplified as follows.

$$\begin{aligned}\angle \mathrm{APF}(s) &\approx -\frac{\pi}{2} - \left(-\frac{\pi}{4} + \frac{\omega_g}{2\omega_n}\right),\\ &\approx -\frac{\pi}{4} - \frac{\omega_g}{2\omega_n},\\ &\approx -\frac{\pi}{4} - \frac{(\omega_n + \delta\omega)}{2\omega_n},\\ &\approx -\frac{\pi}{4} - \frac{1}{2} - \frac{\delta_\omega}{2\omega_n}.\end{aligned} \tag{17}$$

As shown in (17), the first two terms are frequency independent while the third term depends on frequency variation. This term, i.e., $k'_\phi = 1/2\omega_n$, needs to compensated.

It is well known that single-phase grid voltage can be represented by an unbalanced two phase-system. It was shown in [36] that single-stage frequency-fixed APF cannot effectively remove the unbalanced component as the bandwidth of the unbalanced component rejection part is very narrow. As such, the unbalanced component will appear as double the fundamental frequency component after Park transformation. Thus, in order to eliminate this error, the double frequency component needs to be rejected. This issue can be solved by increasing the bandwidth of the notch component. In the literature, a two-stage APF has been suggested for this purpose. The two-stage APF effectively increases notch bandwidth and enables frequency-fixed APFs to reject off-nominal frequency unbalanced components. However, the two-stage APF will double the phase delay in the off-nominal frequency condition. As such, the required phase compensation value is computed by $k_\phi = 2k'_\phi = 1/\omega_n$.

3.3. Implementation in PLL

The previous two subsections detailed the procedure for obtaining DC offset eliminated signal $v_g^{\varnothing}$ and its orthogonal component $v_g^{\varnothing\perp}$. These signals can be used as the input to PLL. The overall block diagram of the proposed PLL is provided in Figure 3. This section details the operating principle of this PLL. Before describing the phase detector operation of this PLL in our case, let us consider APF-filtered signals in the steady-state:

$$v_\beta(t) = -V_p \cos(\theta_g + \delta_\phi), \tag{18}$$

$$v_g'^{\varnothing}(t) = -V_p \sin(\theta_g + 2\delta_\phi), \tag{19}$$

where δ_ϕ is the off-nominal frequency phase attenuation by each stage of the APF. As per Figure 3, using the signal $v_g^{\varnothing}(t)$ and $v'_g(t)$, $v_\alpha(t)$ is obtained as follows.

$$\begin{aligned}v_\alpha(t) &= \frac{v_g^{\varnothing}(t) - v_g'^{\varnothing}(t)}{2},\\ &\approx V_p \sin(\theta_g) + \delta_\phi \cos(\theta_g).\end{aligned} \tag{20}$$

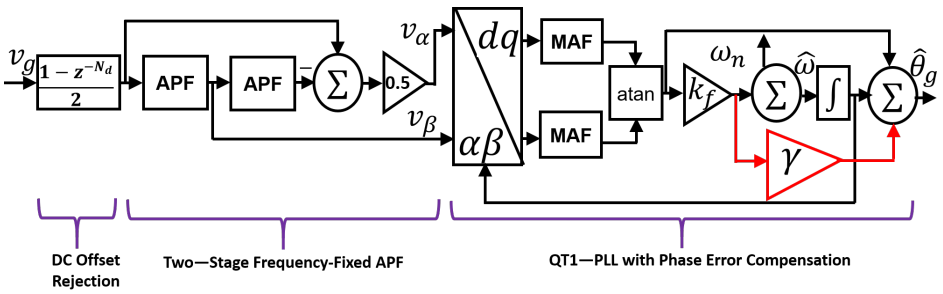

Figure 3. Overall block diagram of the proposed PLL.

The phase detector of the considered PLL is provided by the following.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\omega}t) & \sin(\hat{\omega}t) \\ -\sin(\hat{\omega}t) & \cos(\hat{\omega}t) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix}. \tag{21}$$

Then, direct-axis and quadrature-axis voltages can be obtained directly from (21). By applying a quasi-locked condition, i.e., $\omega - \hat{\omega} \approx 0$, the direct-axis and quadrature-axis voltages can be rewritten as follows.

$$\begin{aligned} v_d &= v_\alpha \cos(\hat{\omega}t) + v_\beta \sin(\hat{\omega}t), \\ &= \frac{V_p}{2}(\sin((\omega+\hat{\omega})t+\phi) + \sin((\omega-\hat{\omega})t+\phi)) + \frac{\delta_\phi}{2}(\cos((\omega-\hat{\omega})t+\phi)) \\ &\quad - \frac{V_p}{2}\big(\sin\big((\omega+\hat{\omega})t+\phi+2\delta_\phi\big) - \sin\big((\omega-\hat{\omega})t+\phi+2\delta_\phi\big)\big) \\ &\quad + \frac{V_p}{2}\frac{\delta_\phi}{2}(\cos((\omega+\hat{\omega})t+\phi)), \\ &\approx \frac{V_p}{2}\big(\sin(\phi) + \sin\big(\phi+\delta_\phi\big)\big) + \frac{V_p}{2}\big(\sin(2\hat{\omega}t+\phi) - \sin\big(2\hat{\omega}t+\phi+\delta_\phi\big)\big) \\ &\quad + \frac{\delta_\phi}{2}\cos(\phi) + \frac{\delta_\phi}{2}(\cos(2\hat{\omega}t+\phi)). \end{aligned} \tag{22}$$

$$\begin{aligned} v_q &= -v_\alpha \sin(\hat{\omega}t) + v_\beta \cos(\hat{\omega}t), \\ &= \frac{V_p}{2}(\cos((\omega+\hat{\omega})t+\phi) + \cos((\omega-\hat{\omega})t+\phi)) - \frac{\delta_\phi}{2}(\sin((\omega+\hat{\omega})t+\phi)) \\ &\quad - \frac{V_p}{2}\big(\cos\big((\omega+\hat{\omega})t+\phi+\delta_\phi\big) - \cos\big((\omega-\hat{\omega})t+\phi+\delta_\phi\big)\big) \\ &\quad + \frac{V_p}{2}\frac{\delta_\phi}{2}(\sin((\omega-\hat{\omega})t+\phi)), \\ &\approx \frac{V_p}{2}\big(\cos(\phi) + \cos\big(\phi+\delta_\phi\big)\big) + \frac{V_p}{2}\big(\cos(2\hat{\omega}t+\phi) - \cos\big(2\hat{\omega}t+\phi+\delta_\phi\big)\big) \\ &\quad + \frac{\delta_\phi}{2}\sin(\phi) + \frac{\delta_\phi}{2}\sin(2\hat{\omega}t+\phi). \end{aligned} \tag{23}$$

Double frequency components in (22) and (23) can easily be filtered by applying moving average filter (MAF) with half-cycle window length. The transfer functions of MAF in continuous and discrete domain are provided by the following.

$$\text{MAF}(s) = \frac{1-e^{-t_d s}}{t_d s}, \tag{24}$$

$$\text{MAF}(z) = \frac{1}{N}\frac{1-z^{-N_d}}{1-z^{-1}}. \tag{25}$$

By applying MAF to (22) and (23) and also assuming negligible off-nominal frequency phase shift, filtered v_d and v_q can be approximated as follows.

$$v'_d = V_p \sin(\phi), \tag{26}$$

$$v'_q = V_p \cos(\phi). \tag{27}$$

Filtered voltages are then fed to the loop-filter of QT1-PLL, as shown in Figure 3.

3.4. Small-Signal Modeling and Tuning

A small-signal model of the proposed PLL can be obtained by considering the signal flow in Figure 3. For this purpose, first, the small-signal model of the pre-loop filters needs to be developed. The first pre-loop filter is the delayed signal cancellation block, which is

given by transfer function (11). This transfer function can be converted into synchronous reference frame by substituting $s = s + j\omega_n$.

$$\mathrm{DSC}_{dq}(s) = \frac{1 + e^{-t_d s}}{2}. \tag{28}$$

The transfer function of the APF in synchronous reference frame can be obtained by applying the Park transformation to single-stage APF and is given by the following Gautam et al. [26].

$$\mathrm{APF}_{dq}(s) = \frac{s + 2\omega_n}{2(s + \omega_n)}. \tag{29}$$

In our study, a two-stage APF is considered. As such, the effective transfer function is given by the following.

$$\mathrm{APF}^2_{dq}(s) = \left(\frac{s + 2\omega_n}{2(s + \omega_n)}\right)^2. \tag{30}$$

Considering the pre-loop filters, the small-signal model is shown in Figure 4, where $\gamma = k_{dc} + k_\phi$ is the overall phase compensation gain.

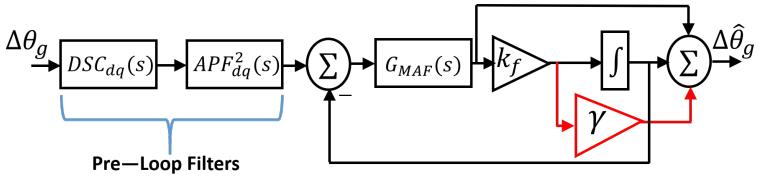

Figure 4. Small-signal model of the proposed PLL.

The proposed PLL has only one parameter to tune, which is the frequency estimation gain k_f. This gain can be tuned in several ways. Two of the popular approaches are based on open-loop phase margin and settling time. The later is considered in this study. In order to tune gain k_f using this method, a +2 Hz frequency step is considered. Considering a 2% settling time, settling time versus the gain k_f is given in Figure 5. From this figure, $k_f = 89$ has been found to provide the fastest settling time. This value has been considered as the optimal gain for k_f. Considering this value of k_f,validation of the small-signal model is provided in Figure 6.

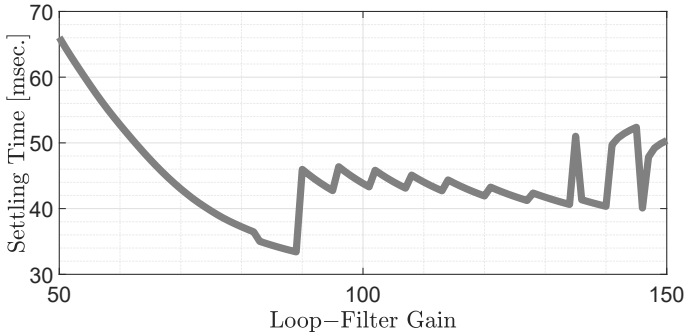

Figure 5. Settling time versus k_f for a +2 Hz frequency step change.

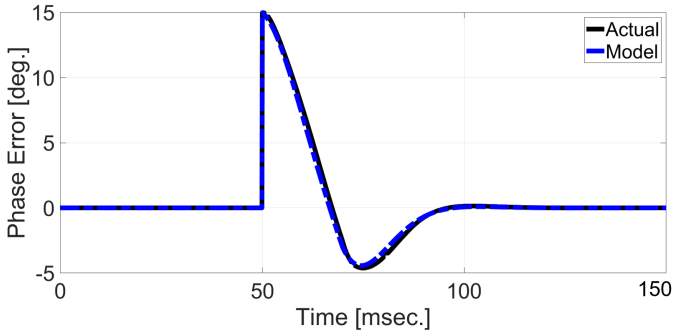

Figure 6. Small-signal model verification of the proposed PLL with $k_f = 89$.

Once the phase of the grid voltage fundamental component is estimated, the reference compensation voltage can be calculated as follows:

$$v_c^{\text{ref}} = V_p^{\text{ref}} \sin(\hat{\theta}_g), \tag{31}$$

where reference magnitude is provided by V_p^{ref}. The design of the control signal u based on the reference grid voltage (31) is detailed in the next section.

4. Super Twisting Sliding Mode Controller Design

In this Section, tracking error dynamics (6) and (7) will be used for the control design. For this purpose, let us consider that the control signal is composed of $u = u_0 + u_n$, where u_0 is the nominal control signal and u_n is the nonlinear part of the control signal. If we consider $u_0 = (1/V_{dc})\xi_1$ and $u_n = u_{ST}/(\delta V_{dc})$, then the total control signal can be written as follows.

$$u = \frac{1}{V_{dc}}\left(\xi_1 + \frac{u_{ST}}{\delta}\right). \tag{32}$$

Then, the tracking error dynamics (6) and (7) can be rewritten as follows.

$$\frac{d\xi_1}{dt} = \xi_2, \tag{33}$$

$$\frac{d\xi_2}{dt} = u_{ST} + w. \tag{34}$$

Tracking error dynamics (33) and (34) can be viewed as a perturbed second-order integrator. Numerous control techniques can be employed to stabilize the error under the presence of perturbation $w(t)$. In this study, we consider a second-order SMC [31,37] in the form of super-twisting SMC [38]. In order to design the super-twisting SMC, let us consider the following sliding surface.

$$\sigma_e = \xi_2 + \lambda_1 \xi_1, \lambda_1 > 0. \tag{35}$$

Then, the controller u_{ST} in (34) can be designed as follows:

$$u_{ST} = -\lambda_1 \xi_2 - \lambda_2 |\sigma_e|^{\frac{1}{2}} \text{sgn}(\sigma_e) - \lambda_3 \int_0^t \text{sgn}(\sigma_e(\tau)) d\tau, \tag{36}$$

where sgn(.) is the conventional signum function and the gains λ_2 and λ_3 are selected as follows.

$$\lambda_3 > W, \lambda_2^2 > 4\lambda_3. \tag{37}$$

In order to analyze the stability of the controller (36), let us consider the derivative of the sliding surface (35) together with (33), (34), and (36) as provided below.

$$\dot{\sigma}_e = -\lambda_2 |\sigma_e|^{\frac{1}{2}} \text{sgn}(\sigma_e) - \lambda_3 \int_0^t \text{sgn}(\sigma_e(\tau)) dt + w(t). \tag{38}$$

Let us consider the following variables.

$$\zeta_1 = \sigma_e, \tag{39}$$

$$\zeta_2 = -\lambda_3 \int_0^t \text{sgn}(\sigma_e(\tau))d\tau + w(t), \tag{40}$$

$$\frac{dw}{dt} = \eta(t). \tag{41}$$

Then, the dynamics of the sliding surface (38) can be rewritten as follows.

$$\frac{d\zeta_1}{dt} = -\lambda_2 |\sigma_e|^{\frac{1}{2}} \text{sgn}(\sigma_e) + \zeta_2, \tag{42}$$

$$\frac{d\zeta_2}{dt} = -\lambda_3 \int_0^t \text{sgn}(\sigma_e(\tau))d\tau + \eta(t). \tag{43}$$

Then, for the selected control gain (37), finite-time convergence of the variables ζ_1 and ζ_2 can easily be established by using the results presented in Levant [37]. In order to implement the super-twisting controller, (32), (35), and (36) are required. An implementation block diagram of the super-twisting sliding-mode controller is provided in Figure 7.

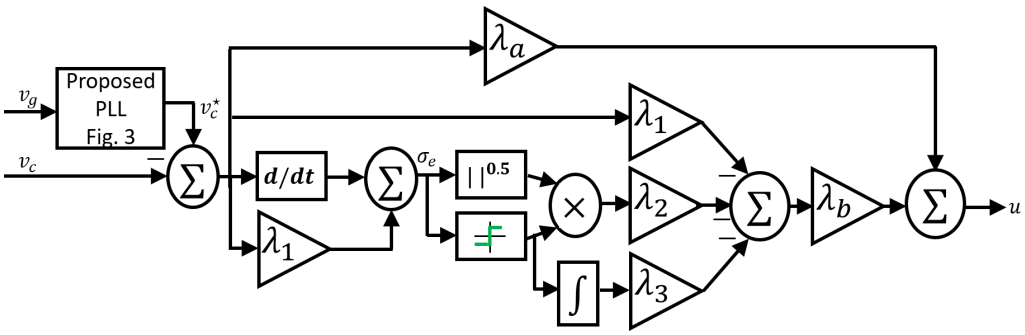

Figure 7. Block diagram of super-twisting sliding-mode controller with $\lambda_a = 1/V_{dc}$ and $\lambda_b = 1/(\delta V_{dc})$.

5. Simulation and Experimental Results

In this Section, simulation and experimental results are reported. The experimental setup used in this study is demonstrated in Figure 8. Here, a Texas Instrument C2000 series micro-controller is used to implement the proposed control and estimation algorithm. Parameters of the setup and control gains are provided in Table 1.

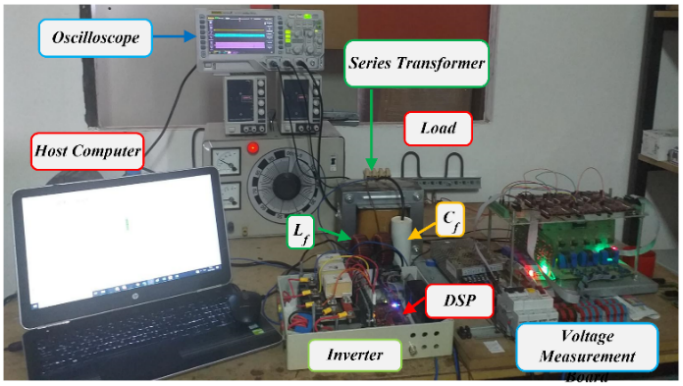

Figure 8. Experimental setup used in this study.

Table 1. Experimental study parameters.

System and Control Parameters	Values
Controller gains	
PLL gain	$k_f = 89$
Grid: voltage and frequency	120 V (rms) 50 Hz
Grid: impedance	$R_g = 1\,\text{m}\Omega$, $L_g = 0.1\,\mu\text{H}$
Transformer turns ratio	1:1
DC link voltage, V_{dc}	120 V
LC filter	$L_f = 0.8$ mH, $C_f = 50\,\mu$F
Sensitive series load	$R = 100\,\Omega$

Numerical simulation using Matlab/Simulink is conducted by considering the same values.

In the first test, the grid voltage suddenly experiences a ≈30% sag. From approximately 170 V (peak), the grid voltage dropped to roughly 120 V (peak). Experimental results are provided in Figure 9. The results show that in order to mitigate the effect of grid voltage sag at the sensitive load side, the DVR was very quick to react and supplied the necessary 50 V in-phase compensation voltage. As a result, constant voltage was maintained at the load side. In the second test, voltage swell was considered, and the results are provided in Figure 10. Here, grid voltage increased to 210 V, which is roughly a 25% change from the nominal value. Unlike the first test, here, out-of-phase compensation voltage needs to be generated in order to reduce the voltage at the sensitive load end. As shown in Figure 10, the proposed enhanced QT1-PLL was very successful in generating the required roughly 40 V out-of-phase compensation voltage, and the sliding mode controller ensured the tracking of the reference compensation voltage by the DVR. These results show that the proposed approach can handle both sag and swell conditions. In the real grid, in addition to voltage sag/swell, harmonics are also a problem. The presence of harmonics will render the sensitive load voltage distorted. As a result, power quality degrades. In order to mitigate this issue, harmonic compensation is also required. In the final test, the grid voltage suddenly became distorted, and the results are provided in Figure 11. The proposed PLL can extract the fundamental component with high harmonic robustness. As a result, quick estimation of the grid harmonics was performed by PLL, and DVR injected the necessary harmonic compensation voltage to ensure very low distortion at the load side. The results in Figure 11 validate the suitability of the proposed PLL in a distorted grid condition.

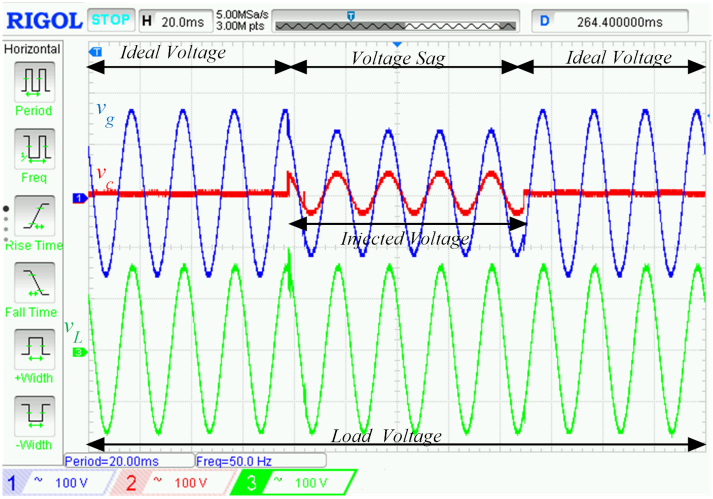

Figure 9. Experimental responses of v_g, v_c, and v_L subject to voltage sag in the grid.

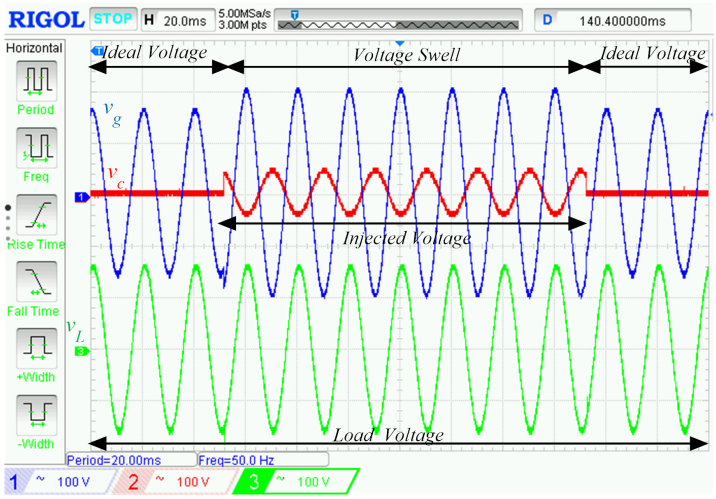

Figure 10. Experimental responses of v_g, v_c, and v_L subject to voltage swell in the grid.

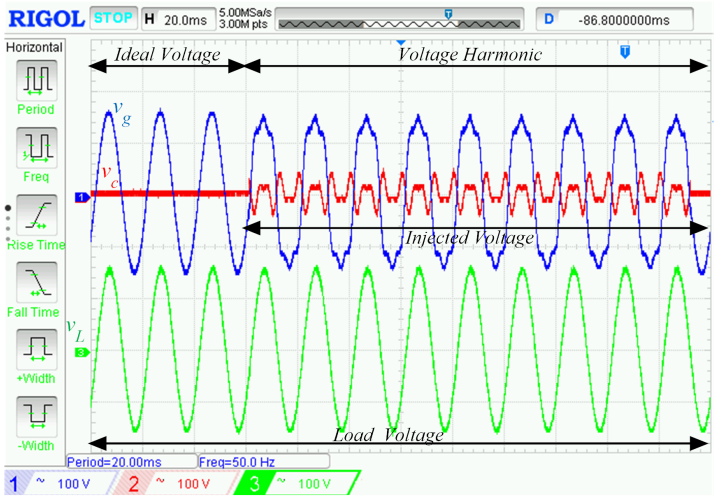

Figure 11. Experimental responses of v_g, v_c, and v_L subject to voltage harmonics in the grid.

In order to check the robustness of the used controller, we have used numerical simulations. In the simulation test, voltage sag and harmonics are considered. The nominal value of the filter inductor is 0.8 mH. This value is used to synthesize the control law. Simulation results with ±25% variation in the filter inductor are provided in Figure 12. The results in Figure 12 show that the response of DVR is very similar when the system parameter experienced a ±25% change from the nominal value. This shows that the sliding mode controller is robust to parameter variations.

Experimental results as shown in Figures 9–11 independently considered voltage sag, swell, and harmonics. In practice, in addition to these characteristics, phase and/or frequency of the grid voltage may also change simultaneously in the worst case scenario. In order to asses the performance of the proposed method, two additional simulation studies were considered. In the first test, grid voltage experienced −0.5 p.u. sag and −25° phase change simultaneously. In the second test, in addition to the sag, the grid voltage also experienced +25° phase change and +1 Hz frequency change. In both cases, the fault cleared after 100 ms and the grid became distorted after fault clearance. Numerical simulation results for the first and second test are provided in Figures 13 and 14. Results show that the proposed control method is very fast (roughly 1 cycle convergence time) despite very abrupt changes in grid voltage parameters. However, it is to be noted here that the load voltage transients are not that smooth compared to the case when only one parameter changed, such as in Figure 12. Smooth transient load voltage scan be obtained by either

freezing the PLL or by using a very slow one [17]. However, this type of solution will not be able to provide efficient harmonic compensation. As such, a trade-off between the dynamic response and smooth transient behavior has to be made in PLL parameter selection.

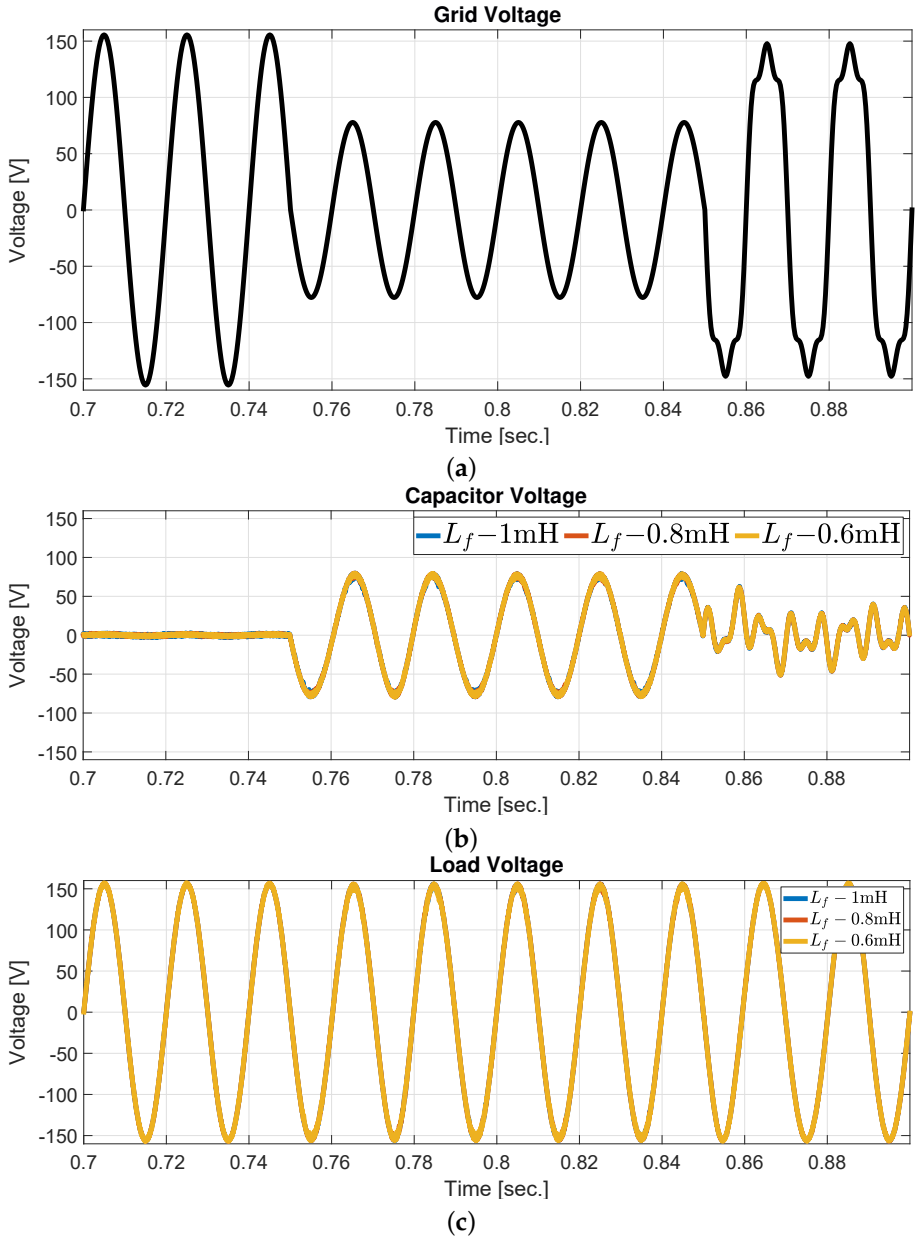

Figure 12. Simulation results for controller robustness check. (**a**) Grid voltage; (**b**) capacitor voltage; (**c**) load voltage.

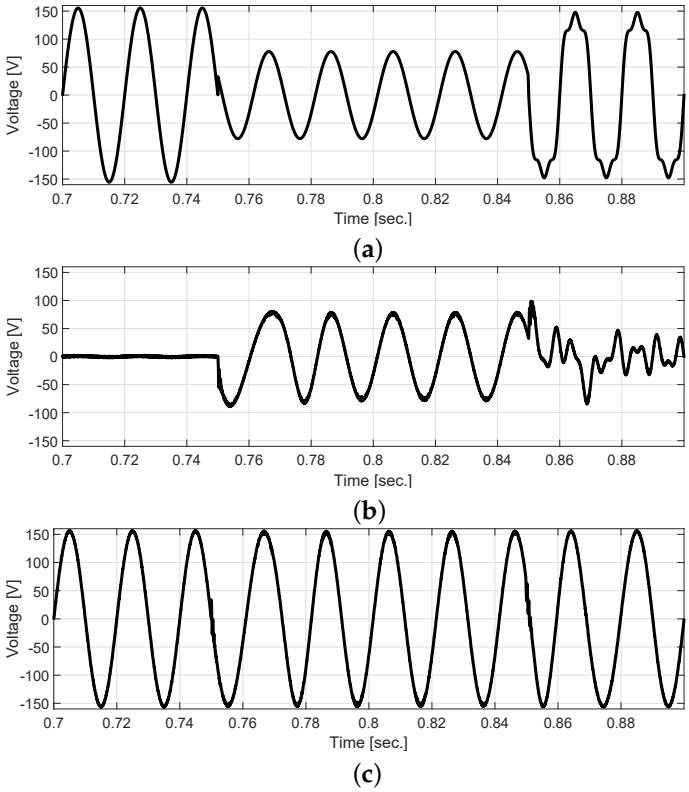

Figure 13. Simulation results for combined voltage sag and phase change at the grid. (**a**) Grid voltage; (**b**) capacitor voltage; (**c**) load voltage.

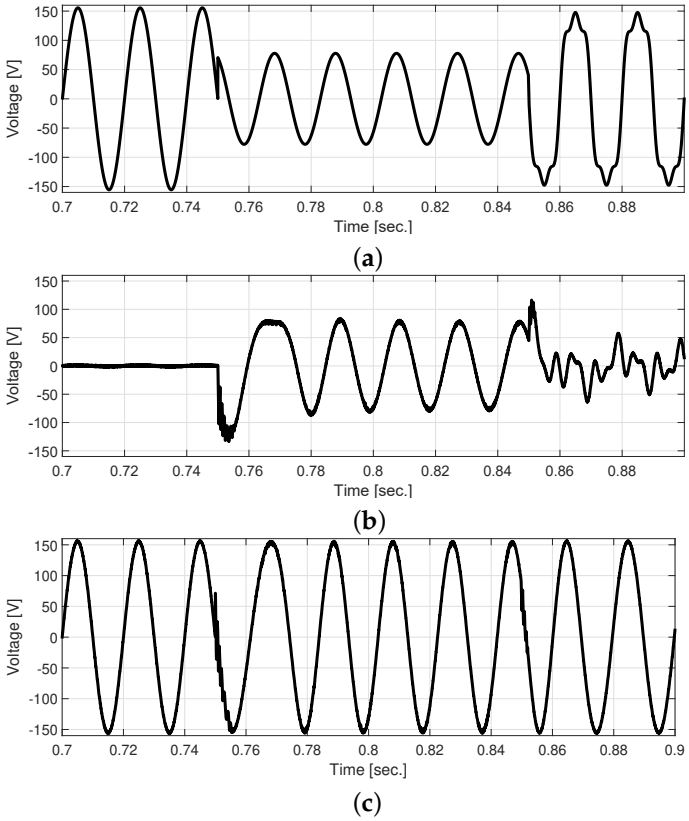

Figure 14. Simulation results for combined voltage sag, frequency, and phase change at the grid. (**a**) Grid voltage; (**b**) capacitor voltage; (**c**) load voltage.

6. Conclusions

In this paper, an enhanced single-phase quasi type-1 PLL was proposed to generate the reference compensation voltage for the multi-functional operation of a single-phase dynamic voltage restorer. A super-twisting sliding-mode controller was also proposed to track the reference voltage. The developed PLL is highly robust to grid voltage harmonics, which resulted in very low total harmonic distortion at the sensitive load-side. Moreover, thanks to a super-twisting controller, fast tracking of the compensation voltage was also achieved. Stability analysis and tuning of the PLL are presented by using small-signal modeling. The developed control method has been validated in a laboratory-scale prototype. The experimental results show that the proposed controller is very effective in compensating any grid voltage abnormalities, which in turn contributes to keeping the voltage at the sensitive load-side to remain very close to the ideal reference voltage.

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References

1. Moghassemi, A.; Padmanaban, S. Dynamic voltage restorer (DVR): A comprehensive review of topologies, power converters, control methods, and modified configurations. *Energies* **2020**, *13*, 4152. [CrossRef]
2. Yáñez-Campos, S.C.; Cerda-Villafaña, G.; Lozano-García, J.M. A Two-Grid Interline Dynamic Voltage Restorer Based on Two Three-Phase Input Matrix Converters. *Appl. Sci.* **2021**, *11*, 561. [CrossRef]
3. Abas, N.; Dilshad, S.; Khalid, A.; Saleem, M.S.; Khan, N. Power quality improvement using dynamic voltage restorer. *IEEE Access* **2020**, *8*, 164325–164339. [CrossRef]
4. Toumi, T.; Allali, A.; Abdelkhalek, O.; Abdelkader, A.B.; Meftouhi, A.; Soumeur, M.A. PV Integrated single-phase dynamic voltage restorer for sag voltage, voltage fluctuations and harmonics compensation. *Int. J. Power Electron. Drive Syst.* **2020**, *11*, 547. [CrossRef]
5. *IEEE Standard 1346-1998*; IEEE Recommended Practice for Evaluating Electric Power System Compatibility with Electronic Process Equipment. IEEE: Piscataway Township, NJ, USA, 1998. [CrossRef]
6. Lucas, A. Single-phase PV power injection limit due to voltage unbalances applied to an urban reference network using real-time simulation. *Appl. Sci.* **2018**, *8*, 1333. [CrossRef]
7. Trabelsi, M.; Komurcugil, H.; Refaat, S.S.; Abu-Rub, H. Model predictive control of packed U cells based transformerless single-phase dynamic voltage restorer. In Proceedings of the 2018 IEEE International Conference on Industrial Technology (ICIT), Lyon, France, 20–22 February 2018; pp. 1926–1931.
8. Kumar, C.; Mishra, M.K. Predictive voltage control of transformerless dynamic voltage restorer. *IEEE Trans. Ind. Electron.* **2015**, *62*, 2693–2697. [CrossRef]
9. Ahmed, H.; Salgado, I.; Chairez, I.; Benbouzid, M. Robust gradient estimator for unknown frequency estimation in noisy environment: Application to grid-synchronization. *IEEE Access* **2020**, *8*, 70693–70702. [CrossRef]
10. Ahmed, H.; Biricik, S.; Benbouzid, M. Enhanced Frequency Adaptive Demodulation Technique For Grid-Connected Converters. *IEEE Trans. Ind. Electron.* **2021**, *68*, 11053–11062. [CrossRef]
11. Remya, V.; Parthiban, P.; Ansal, V.; Nandakumar, A. Single-phase DVR with semi-Z-source inverter for power distribution network. *Arab. J. Sci. Eng.* **2018**, *43*, 3135–3149. [CrossRef]
12. Satputaley, R.J.; Borghate, V.B. Performance analysis of DVR using "new reduced component" multilevel inverter. *Int. Trans. Electr. Energy Syst.* **2017**, *27*, e2288. [CrossRef]
13. Ahmed, H.; Biricik, S.; Benbouzid, M. Linear Kalman Filter-Based Grid Synchronization Technique: An Alternative Implementation. *IEEE Trans. Ind. Inform.* **2021**, *17*, 3847–3856. [CrossRef]
14. Ahmed, H.; Benbouzid, M. Simplified Second-Order Generalized Integrator - Frequency-Locked Loop. *Adv. Electr. Electron. Eng.* **2019**, *17*, 405–412. [CrossRef]
15. Ahmed, H.; Pay, M.L.; Benbouzid, M.; Amirat, Y.; Elbouchikhi, E. Hybrid estimator-based harmonic robust grid synchronization technique. *Electr. Power Syst. Res.* **2019**, *177*, 106013. [CrossRef]

16. Meena, A.; Islam, S.; Anand, S.; Sonawane, Y.; Tungare, S. Design and control of single-phase dynamic voltage restorer. *Sādhanā* **2017**, *42*, 1363–1375. [CrossRef]
17. Nielsen, J.G.; Newman, M.; Nielsen, H.; Blaabjerg, F. Control and testing of a dynamic voltage restorer (DVR) at medium voltage level. *IEEE Trans. Power Electron.* **2004**, *19*, 806–813. [CrossRef]
18. Biricik, S.; Komurcugil, H. Optimized sliding mode control to maximize existence region for single-phase dynamic voltage restorers. *IEEE Trans. Ind. Inform.* **2016**, *12*, 1486–1497. [CrossRef]
19. Biricik, S.; Khadem, S.K.; Redif, S.; Basu, M. Voltage distortion mitigation in a distributed generation-integrated weak utility network via a self-tuning filter-based dynamic voltage restorer. *Electr. Eng.* **2018**, *100*, 1857–1867. [CrossRef]
20. Biricik, S.; Redif, S.; Özerdem, Ö.C.; Khadem, S.K.; Basu, M. Real-time control of shunt active power filter under distorted grid voltage and unbalanced load condition using self-tuning filter. *IET Power Electron.* **2014**, *7*, 1895–1905. [CrossRef]
21. Rajkumar, K.; Parthiban, P. Grid voltage detection method based on a novel adaptive notch filter for control of transformerless dynamic voltage restorer. In Proceedings of the 2020 IEEE First International Conference on Smart Technologies for Power, Energy and Control (STPEC), Nagpur, India, 25–26 September 2020; pp. 1–6.
22. Mellouli, M.S.; Hamouda, M.; Slama, J.B.H.; Al Haddad, K. A Third-order MAF Based QT1-PLL That is Robust against Harmonically Distorted Grid Voltage with Frequency Deviation. *IEEE Trans. Energy Convers.* **2021**, *36*, 1600–1613. [CrossRef]
23. Golestan, S.; Freijedo, F.D.; Vidal, A.; Guerrero, J.M.; Doval-Gandoy, J. A quasi-type-1 phase-locked loop structure. *IEEE Trans. Power Electron.* **2014**, *29*, 6264–6270. [CrossRef]
24. Ahmed, H.; Tir, Z.; Verma, A.K.; Ben Elghali, S.; Benbouzid, M. Quasi Type-1 PLL With Tunable Phase Detector for Unbalanced and Distorted Three-Phase Grid. *IEEE Trans. Energy Convers.* **2021**. [CrossRef]
25. Wu, C.; Xiong, X.; Taul, M.G.; Blaabjerg, F. On the Equilibrium Points in Three-Phase PLL Based on the d-axis Voltage Normalization. *IEEE Trans. Power Electron.* **2021**, *36*, 12146–12150. [CrossRef]
26. Gautam, S.; Xiao, W.; Lu, D.D.C.; Ahmed, H.; Guerrero, J.M. Development of Frequency-Fixed All-Pass Filter based Single-Phase Phase-Locked Loop. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**. [CrossRef]
27. Ahmed, H.; Benbouzid, M. On the enhancement of generalized integrator-based adaptive filter dynamic tuning range. *IEEE Trans. Instrum. Meas.* **2020**, *69*, 7449–7457. [CrossRef]
28. Golestan, S.; Guerrero, J.M.; Vasquez, J.C. Single-Phase PLLs: A Review of Recent Advances. *IEEE Trans. Power Electron.* **2017**, *32*, 9013–9030. [CrossRef]
29. Omar, A.I.; Aleem, S.H.A.; El-Zahab, E.E.; Algablawy, M.; Ali, Z.M. An improved approach for robust control of dynamic voltage restorer and power quality enhancement using grasshopper optimization algorithm. *ISA Trans.* **2019**, *95*, 110–129. [CrossRef]
30. Li, Y.W.; Blaabjerg, F.; Vilathgamuwa, D.M.; Loh, P.C. Design and comparison of high performance stationary-frame controllers for DVR implementation. *IEEE Trans. Power Electron.* **2007**, *22*, 602–612. [CrossRef]
31. Komurcugil, H.; Biricik, S.; Bayhan, S.; Zhang, Z. Sliding Mode Control: Overview of Its Applications in Power Converters. *IEEE Ind. Electron. Mag.* **2021**, *15*, 40–49. [CrossRef]
32. Biricik, S.; Komurcugil, H.; Ahmed, H.; Babaei, E. Super twisting sliding mode control of DVR with frequency-adaptive Brockett oscillator. *IEEE Trans. Ind. Electron.* **2021**, *68*, 10730–10739. [CrossRef]
33. Biricik, S.; Komurcugil, H.; Tuyen, N.D.; Basu, M. Protection of Sensitive Loads Using Sliding Mode Controlled Three-Phase DVR With Adaptive Notch Filter. *IEEE Trans. Ind. Electron.* **2019**, *66*, 5465–5475. [CrossRef]
34. Chedjara, Z.; Massoum, A.; Wira, P.; Safa, A.; Gouichiche, A. A fast and robust reference current generation algorithm for three-phase shunt active power filter. *Int. J. Power Electron. Drive Syst.* **2021**, *12*, 121–129. [CrossRef]
35. Sevilmiş, F.; Karaca, H. A fast hybrid PLL with an adaptive all-pass filter under abnormal grid conditions. *Electr. Power Syst. Res.* **2020**, *184*, 106303. [CrossRef]
36. Ramezani, M.; Golestan, S.; Li, S. Non-frequency sensitive all-pass filter based single-phase PLLs. In Proceedings of the 2016 IEEE/PES Transmission and Distribution Conference and Exposition (T&D), Dallas, TX, USA, 3–5 May 2016; pp. 1–5.
37. Levant, A. Higher-order sliding modes, differentiation and output-feedback control. *Int. J. Control* **2003**, *76*, 924–941. [CrossRef]
38. Derafa, L.; Benallegue, A.; Fridman, L. Super twisting control algorithm for the attitude tracking of a four rotors UAV. *J. Frankl. Inst.* **2012**, *349*, 685–699. [CrossRef]