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High Voltage Nanosecond Pulsed Electric Field (nsPEF) Electroporation Systems

Davies, Ilan

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High Voltage Nanosecond Pulsed Electric Field (nsPEF) Electroporation Systems

Written by

Ilan Wyn Davies

School of Computer Science

and Electronic Engineering

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Thank you to all the friends and colleagues made along this journey that have supported, encouraged and mentored me along the way. Moulding myself to the engineer and professional that I am today. Thank you Chris Hancock, John Bishop, Malcolm White, Patrick Burn, Louis Turner, and Aeron Jones for everything and the memories. A massive thank you to all of you.

Finally, I would like to dedicate this thesis to my family; my late father Bryan, my mother Susan, my sister Teleri, my grandparents and uncle Dylan. Thank you for what I consider, the best upbringing I could have had but their unconditional love, tolerant, and understanding of my workload throughout this PhD and have shown nothing but support for everything I want in life.

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ABSTRACT

The work presented in this thesis contributes to the field of nanosecond electroporation research and has the potential to help address the global issue of cancer. The work focuses on the design and development of two nanosecond pulsed electric field electroporation systems that support the delivery of nanosecond width pulsed electric fields into biological cell line populations (*in-vitro*) and bulk tissue (*in-vivo*). Both the slow and fast electroporation systems have been optimized to deliver high voltages, in excess of 1 kV and nanosecond (10 ns to 300 ns) pulses across 50 Ω load impedance, which is representative of the biological load.

The slow nsPEF electroporation system design is based on the fast-switching of Silicon Carbide power MOSFETs connected in a push-pull configuration with the gates driven by suitable optocoupler gate drivers. This work demonstrates that the system can produce a user-selected number of pulsed electric fields from 100 ns to 300 ns duration, with amplitudes in excess of 1 kV, at a user-selected repetition frequency, from 1 Hz to 50 Hz across a 50 Ω load impedances.

The fast nsPEF electroporation system design uses a combination of relatively slow charging and rapid discharging of a coaxial transmission line with a stack of avalanche transistors operating as a fast-switching element. The system has been demonstrated to produce a user-selected number of positive, negative, or simultaneously generate positive and negative polarity pulsed electric fields, from 10 ns to 300 ns in duration, with amplitudes in excess of 1 kV, at user-selected repetition frequencies across a 50 Ω load impedance.

The nanosecond pulsed electric field electroporation systems developed in this work have the potential for use in cell manipulation and control of cell physiology. Unlike current radiofrequency, microwave and conventional cancer treatment methods of chemotherapy and radiotherapy, the nanosecond pulsed electric field generated provides the possibility to non-thermally irreversibly electroporate cells suspended in a fluid and bulk tissue.

The *in-vitro* and *in-vivo* results obtained from a biological cell line and bulk tissue indicate the nanosecond pulsed electric fields can be used to open cell membranes and allow materials, such as chemotherapy drugs, to be locally introduced into the cells. It has also been shown that cells can be non-thermally ablated without damage to collagen. In this instance porcine liver was used as a representative bulk tissue model.

This work led to the filing of multiple patent applications, thirteen conference papers and one journal paper in the IEEE European Microwave Conference (EuMC). This work has contributed to the field of nanosecond electroporation research and the development of nanosecond electroporation as an alternative non-thermal energy-based therapeutic for cancer treatment.

CONTENTS

CONTRIBUTIONS AND ACHIEVEMENTS

Acknowledged Contributions from Individuals

Caterina Merla, Arianna Casciati, Mirella Tanori and Mariateresa Mancuso providing the set-up and protocols, for the development of the 50 Ω cell suspension buffer solution and culturing of the D283 cell population for the *in-vivo* microbiological investigation work conducted in Chapter 4.

Paul Sibbons, Tahera Ansari and Aaron Southgate help in conducting the pre-clinical and the Haematoxylin & Eosin stain Picro Sirius Red and Miller's providing Elastin slides that resulted in the histology outcome in the preclinical investigation in Chapter 6.

Louis Turner, George Ullrich and Dave Webb for providing mechanical support in the construction of prototype printed circuit boards, adjustment to the election system chassis and adaptation of a vernier calliper for an application for preclinical investigation in Chapter 6.

Contributions and Achievements to the Field

The work presented in this thesis is a direct contribution to the European Union's Horizon 2020 Framework Program FET OPEN funded project called 'Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells' (SUMCASTEC). The overall objective of SUMCASTEC was to explore a radically new approach for real-time isolation (i.e., within minutes vs current 40 days) and neutralization of cancer stem cells. This work contributes to the neutralization section of SUMCASTEC.

The work conducted in developing both the slow and fast nanosecond pulsed electric field electroporation system have contributed to supporting both *in-vitro* and *in-vivo/*pre-clinical research and investigation application of nanosecond electroporation. The design and development of the slow and fast electroporation systems for the neutralisation of cancer stem cells have provided the platform for further development of nanosecond electroporation as an alternative treatment for several cancers, including pancreatic, lung, brain and kidney tumours. Initial findings show the advantage of nsPEF over µsPEF and other traditional thermal ablation treatment energies due to the distinctive selectivity and non-thermal features.

This work has the potential to lead to the development of a new electrosurgical system for use in clinical practice to treat deep-seated tumours in difficult-to-access anatomical locations such as brain, head and neck, colon, lung, pancreatic or breast cancers, whilst exploiting the development of the nanosecond pulsed electric field energy modality and pulsed electric field based electrosurgical applications for use in non-invasive procedures such as therapeutic endoscopy in the gastrointestinal tracks and the lungs.

The Slow Nanosecond Pulsed Electric Field Electroporation System

The slow nanosecond pulsed electric field electroporation system design was operated through the fast-switching of Silicon Carbide power metal-oxide-semiconductor field-effect transistors in a push-pull configuration. The contribution to the field of engineering is the capability of the slow electroporation system to drive a high-power (SiC) MOSFET devices for the generation of high voltage nanosecond pulsed electric fields in a cost-effect and compact manner. This system enabled the ability for a non-thermal targeted approach of neutralization of cancer stem cells, resulting in the increase permeability and reduction in viability of these cells.

Fast Nanosecond Pulsed Electric Field Electroporation System

The fast nanosecond pulsed electric field electroporation system design is based on the relatively slow charging and rapid discharging of an open circuit coaxial transmission line through a stack of avalanche transistors operating as a fast-switching element.

The engineering contribution of the fast electroporation system design is built upon primitive technique and application notes of charged transmission line technique and avalanche transistors from manufacturers such as Motorola, Zetec and Linear Technology. This resulted in a novel circuits and new engineering techniques-based system that can produce a user-specified number of monopolar or simultaneous generation of positive and/or negative polarity nanosecond pulsed electric fields from 10 ns to 300 ns in duration, with amplitudes in excess of 1 kV, at various repetition frequencies, up to 1 kHz (limited by the transmission line length used) across a 50 Ω load impedance. This work showed that a 10 ns pulsed electric field with an amplitude of 2.5 kV can be generated with this technique.

This system was able to non-thermally irreversibly (and possibly reversibly) electroporate *in-vivo* cells, causing associated cellular changes within liver tissue. The electroporated cellular features were well demarcated from normal tissue and regions of cellular apoptosis-related directly to the instrument application sites. Morphologically, the effect of treatment was limited to cells and the collagen within the treated areas was unchanged from normal, therefore indicating non-thermal ablative effects.

Dissemination

The work detailed in this thesis has been presented at thirteen conferences as either a poster or oral presentation. The work has also resulted in several formal publications in engineering/biomedical journals. These contributions were based on the various design, engineering and biological/clinical aspects of the slow and fast nanosecond pulsed electric field (nsPEF) electroporation systems.

Microwave engineering-based conferences where the work was presented include the Asian-Pacific Microwave Conference (APMC), the European Microwave Conference (EuMC) and the International Union of Radio Science General Assembly and Scientific Symposium (URSI – GASS).

Papers were accepted at the Bioelectromagnetics (BioEM) and IEEE International Microwave Biomedical Conference (IMBioC). Finally, four papers were accepted at the 3rd and 4th World Congress on Electroporation conference that covers all aspects of electroporation technology.

The author of this thesis is a named author but is not the primary author of three of the fourteen published work. Contribution to these three publications included the use of the slow and/or the fast nanosecond pulsed electric field electroporation system as part of their research/work and contributed to the result and conclusion of these published work.

The fourteen conference and a journal paper that was submitted and accepted are listed here in chronological order:

Journal

1) I. W. Davies *et al.*, "Push–pull configuration of high-power MOSFETs for generation of nanosecond pulses for electropermeabilization of cells," in *International Journal of Microwave and Wireless Technologies*, vol 11, issue 11, pp. 645-657, April 2019.

European and International Conferences Papers

1) I. W. Davies *et al.*, "Novel and versatile instrumentation for electro-manipulation of cancer stem cells," in *Conf. Bioelectromagnetics (BioEM)*, Piran, Slovenia, 2018, pp. 90
2) I. W. Davies *et al.*, "Electropermeabilization of Isolated Cancer Stem Cells with a Novel and Versatile Nanosecond Pulse Generator," in *Conf. IEEE International Microwave Biomedical Conference (IMBioC)*, Philadelphia, Pennsylvania, USA, 2018, pp. 106-108.
3) I. W. Davies *et al.*, "Push-Pull Configuration of High Power MOSFETs for Generation of Nanosecond Pulses for Electropermeabilization of Isolated Cancer Stem Cells," in *Conf. 48th European Microwave Conference (EuMC)*, Madrid, Spain, 2018, pp.866-869.
4) I. W. Davies *et al.*, "A Novel Ultrashort Electric Field Pulse Generator using Avalanche Breakdown Transistors and the Open Circuit Transmission Line Technique for Nanosecond Electroporation," in *Conf. 3rd World Congress on Electroporation*, Toulouse, France, 2019.
5) Tanori *et al.*, "Ultrashort electric pulses: an effective way to target cancer stem cells," in *Conf. 3rd World Congress on Electroporation*, Toulouse, France, 2019.
6) I. W. Davies and C. P. Hancock, "An Ultrashort Electric Field Pulse Generator using Avalanche Breakdown Transistors and the Open Circuit Transmission Line Technique for Nanosecond Electroporation" in *Conf. IEEE Asia-Pacific Microwave Conference (APMC)*, Singapore, 2019, pp. 1289-1291.
7) I. W. Davies and C. P. Hancock, "Bipolar nanosecond pulse electric field generator using open circuit transmission line technique and avalanche transistors for nanosecond electroporation" in *Conf. Bioelectromagnetics (BioEM)*, Oxford, England, 2020.

8) E. Rampazzo *et al*., "Targeting in vitro 3D models of glioblastoma with sinusoidal EM fields" in *Conf. Bioelectromagnetics (BioEM)*, Oxford, England, 2020.
9) I. W. Davies and C. P. Hancock, "Generating Bipolar nsPulsed Electric Field using Transmission Line & Avalanche Transistors" in *Conf. 50th European Microwave Conference (EuMC)*, Utrecht, The Netherlands, 2021, pp. 1003-1006.
10) *C. Merla et al*., "Ultrashort electric pulses: an effective way to target cancer stem cells" in *Conf. International Union of Radio Science General Assembly and Scientific Symposium (URSI – GASS)*, Rome, Italy, 2021.
11) I. W. Davies *et al*., "Compact Nanosecond Bipolar Pulse Generator for On-chip Modulation of Biological Response" in *Conf. International Union of Radio Science General Assembly and Scientific Symposium (URSI – GASS)*, Rome, Italy, 2021.
12) I. W. Davies, P. Sibbons and C. P. Hancock, "Design of a versatile nanosecond pulsed electric field (nsPEF) system," in *Conf. 4th World Congress on Electroporation*, Copenhagen, Denmark, 2022.
13) I. W. Davies, P. Sibbons and C. P. Hancock, "Histopathology study of nsPEF from a novel electroporator," in *Conf. 4th World Congress on Electroporation*, Copenhagen, Denmark, 2022.

Granted Patents and Pending Patents

The table below provides a list of the various granted and pending patents that are associated with the work presented in the thesis.

Tittle	Jurisdiction	Application No.	Application Date	General Status
ELECTROSURGICAL GENERATOR **Creo Ref: RF/microwave generator with integrated electroporation waveform supply**	Australia	2019245726	08/03/2019	Pending
	Brazil	BR1120200140082	08/03/2019	Pending
	Canada	3088331	08/03/2019	Pending
	China	201980008800.9	08/03/2019	Pending
	European Patent	19709491.5	08/03/2019	Granted
	India	202027042376	08/03/2019	Pending
	Israel	275882	08/03/2019	Pending
	Japan	2020-538809	08/03/2019	Pending
	Russian Federation	2020123242	08/03/2019	Granted
	Singapore	11202006724P	08/03/2019	Pending
	South Korea	2020-7019478	08/03/2019	Pending
	United States of America	16/961149	08/03/2019	Pending
	France	19709491.5	08/03/2019	Granted
	Germany	19709491.5	08/03/2019	Granted
	Ireland	19709491.5	08/03/2019	Granted
	Italy	19709491.5	08/03/2019	Granted

Contributions.

Tittle	Jurisdiction	Application No.	Application Date	General Status
ELECTROSURGICAL GENERATOR **Creo Ref: RF/microwave generator with integrated electroporation waveform supply**	Netherlands	19709491.5	08/03/2019	Granted
	Spain	19709491.5	08/03/2019	Granted
	Switzerland	19709491.5	08/03/2019	Granted
	United Kingdom	19709491.5	08/03/2019	Granted
	Hong Kong	62021023363.6	08/03/2019	Pending

Tittle	Jurisdiction	Application No.	Application Date	General Status
PULSE GENERATING CIRCUIT, AND ELECTROSURGICAL GENERATOR INCORPORATING THE SAME **Creo Ref: Electroporation pulse generator - Bipolar delay line**	Australia	2020395486	30/11/2020	Pending
	Brazil	112022010263-1	30/11/2020	Pending
	Canada	3159846	30/11/2020	Pending
	China	202080083259.0	30/11/2020	Pending
	European Patent	20819658.4	30/11/2020	Pending
	India	202227032664	30/11/2020	Pending
	Israel	293399	30/11/2020	Pending
	Japan	2022-532853	30/11/2020	Pending
	Singapore	11202205696T	30/11/2020	Pending
	South Korea	2022-7017740	30/11/2020	Pending
	United States of America	17/781238	30/11/2020	Pending
	Hong Kong	62022062463.4	30/11/2020	Pending

Tittle	Jurisdiction	Application No.	Application Date	General Status
PULSE GENERATING CIRCUIT, AND ELECTROSURGICAL GENERATOR INCORPORATING THE SAME Creo Ref: Electroporation pulse generator - Stacked transistors	Australia	2020397117	30/11/2020	Pending
	Brazil	BR112022010526-6	30/11/2020	Pending
	Canada	3160062	30/11/2020	Pending
	China	202080083204.X	30/11/2020	Pending
	European Patent	20819659.2	30/11/2020	Pending
	India	202227038281	30/11/2020	Pending
	Israel	293433	30/11/2020	Pending
	Japan	2022-532857	30/11/2020	Pending
	Singapore	11202250060Q	30/11/2020	Pending
	South Korea	2022-7018713	30/11/2020	Pending
	United States of America	17/781505	30/11/2020	Pending
	Hong Kong	62022062464.2	30/11/2020	Pending

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LIST OF EQUATIONS

Chapter	Equation Number	Equation
Chapter 2	(2.1)	$E = \frac{V}{d}$
	(2.2)	$Bandwidth, BW = \frac{0.35}{rise\ time} = \frac{0.35}{t_r}$
Chapter 3	(3.1)	$C_{gate} = C_{input} = C_{iss} = \left(C_{gs} + C_{gd}(1 + g_m Z_L)\right)$
	(3.2)	$i_g = C_{iss} \frac{dV_{gs}}{dt}$
	(3.3)	$V_0 = V_F + R_2 \left(\frac{V_F}{R_1} + I_{Adj}\right)$
	(3.4)	$R2 = \frac{V_0 - V_F}{\frac{V_F}{R_1} + I_{Adj}}$
	(3.5)	$P_{DC} = V_{DC} I_{DC} = \frac{{V_{DC}}^2}{Z_L}$
	(3.6)	$I_{Av} = I_{DC} f t$ $P_{Av} = P_{DC} f t = V_{DC} I_{Av} = V_{DC} I_{DC} f t$
	(3.7)	$V = V_{DC} e^{\frac{t}{\tau}} = V_{DC} e^{\frac{t}{Z_L C}}$
	(3.8)	$C = \frac{t}{Z_L \ln\left(\frac{V}{V_{DC}}\right)}$
Chapter 4	(4.1)	$\Delta T = \frac{E}{c\ m}$
	(4.2)	$\Delta T_{max} = \frac{E}{c\ m} N$
	(4.3)	$E = \frac{V^2}{Z_L} t$
	(4.4)	$\Delta T = \frac{\left(\frac{V^2}{Z_L}\ t\right)}{c\ m} = \frac{\left(\frac{V^2}{Z_L}\ t\right)}{0.23}$
	(4.5)	$\Delta T_{max} = \frac{\left(\frac{V^2}{Z_L}\ t\right)}{c\ m} N = \frac{\left(\frac{V^2}{Z_L}\ t\right)}{0.23} N$
Chapter 5	(5.1)	$T = \frac{l\sqrt{\varepsilon_r}}{c}$
	(5.2)	$C_d = l\ C_l$
	(5.3)	$\tau = R_C C_d$
	(5.4)	Pulse duration $= 2T = \frac{2l\sqrt{\varepsilon_r}}{c}$
	(5.5)	$f = \frac{1}{T} = \frac{1}{5\tau} = \frac{1}{5 R_C C_d} = \frac{1}{5 R_C l C_l}$
	(5.6)	$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC}$

List of Equations.

Chapter	Equation Number	Equation
Chapter 5	(5.7)	$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{V^-}{V^+}$
	(5.8)	$M = \frac{1}{1 - \left(\frac{V}{BV_{CES}}\right)^m}$
	(5.9)	$S = -\frac{g + G}{C_A}$
	(5.10)	$V_L = \frac{Z_L}{Z_L + Z_0} BV_{CES} \approx \frac{Z_L}{Z_L + Z_0} V_{CC}$
	(5.11)	$V_{Line} = \frac{Z_0}{Z_L + Z_0} BV_{CES} \approx \frac{Z_0}{Z_L + Z_0} V_{CC}$
	(5.12)	$I_P = \frac{BV_{CES}}{Z_L + Z_0} \approx \frac{V_{CC}}{Z_L + Z_0}$
	(5.13)	$t_r = t_2 - t_1$
	(5.14)	$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12\left(\frac{H}{W}\right)}} + 0.04\left(1 - \frac{W}{H}\right)^2\right]$
	(5.15)	$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(8\left(\frac{H}{W}\right) + 0.25\left(\frac{W}{H}\right)\right)$
	(5.16)	$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \left[\frac{\varepsilon_r - 1}{2\sqrt{1 + 12\left(\frac{H}{W}\right)}}\right]$
	(5.17)	$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W}{H} + 1.393 + 2/3 \ln\left(\frac{w}{H} + 1.444\right)\right]}$
	(5.18)	$Z_L = Z_0 - nR_{on}$
	(5.19)	$V_L = \left(\frac{Z_L}{Z_L + nR_{on} + Z_0}\right) V_{CC} = \left(\frac{Z_L}{Z_L + n3\Omega + Z_0}\right) V_{CC}$
	(5.20)	$V_L = \frac{Z_L}{Z_L + Z_0} BV_{CES} = \frac{Z_L}{Z_L + Z_0} BV_{CES}(1 - \Gamma) \approx \frac{Z_L}{Z_L + Z_0} V_{CC}(1 - \Gamma)$
	(5.21)	$V_{CC_{max}} = n\, BV_{CES}$
	(5.22)	$V_{Drop} = \frac{V_{CC_{max}}}{n}$
	(5.23)	$P_{diss} = V_{drop}\, \mathrm{I}$
	(5.24)	$V_{L_{max}} = \frac{Z_L}{Z_L + Z_0} nBV_{CES}$
	(5.25)	$V_{CC_{Min}} = n\, V_{CEO}$
	(5.26)	$V_{L_{Min}} = \frac{Z_L}{Z_L + Z_0} nV_{CEO}$
	(5.27)	$C = \frac{L}{Z^2}$
	(5.28)	$C = n\frac{L}{Z^2}$
	(5.29)	$V_{L\Sigma} = \frac{Z_{L\Sigma}}{Z_{L\Sigma} + Z_0} V_{CC} = V_{LPos} + V_{LNeg}$
	(5.30)	$V_{LPos} = \frac{Z_{LPos}}{Z_{LPos} + Z_{LNeg}} V_{L\Sigma} = \frac{Z_{LPos}}{Z_{LPos} + Z_{LNeg} + Z_0} V_{CC} = \frac{Z_{LPos}}{Z_{L\Sigma} + Z_0} V_{CC}$

List of Equations.

Chapter	Equation Number	Equation
Chapter 5	(5.31)	$V_{LNeg} = \frac{Z_{LNeg}}{Z_{LPos} + Z_{LNeg}} V_{L\Sigma} = \frac{Z_{LNeg}}{Z_{LPos} + Z_{LNeg} + Z_0} V_{CC} = \frac{Z_{LNeg}}{Z_{L\Sigma} + Z_0} V_{CC}$
	(5.32)	$\Gamma = \frac{Z_{L\Sigma} - Z_0}{Z_{L\Sigma} + Z_0} = \frac{(Z_{LPos} + Z_{LNeg}) - Z_0}{(Z_{LPos} + Z_{LNeg}) + Z_0}$
	(5.33)	$P_{DC} = V_{DC} I_{DC} = \frac{{V_{DC}}^2}{Z}$
	(5.34)	$P_{Av} = P_{DC} f t = V_{DC} I_{Av} = V_{DC} I_{DC} f t$
	(5.35)	$C = \frac{t}{Z \ln\left(\frac{V}{V_0}\right)}$
	(5.36a)	$Z_0 = 60\sqrt{\frac{\mu}{\varepsilon}} \ln \frac{4b \tanh \frac{\pi a}{b}}{\pi d}$
	(5.36b)	$Z_0 = 138\sqrt{\frac{\mu}{\varepsilon}} \log_{10} \frac{4b \tanh \frac{\pi a}{b}}{\pi d}$
Chapter 6	(6.1)	$N = f\, t_{on} = 200\, t_{on}$
	(6.2)	$E = \frac{V}{d}$
	(6.3)	$Z_L = \frac{\Gamma Z_0 + Z_0}{1 - \Gamma}$
	(6.4)	$\Gamma = \frac{V^-}{V^+}$
	(6.5)	$\bar{P} = PD$
	(6.6)	$E_n = NPt$
	(6.7)	$\Delta T_{Max} = \frac{\Delta T}{T} = \frac{E_n}{cm\, T} = \frac{E_n}{c\, \rho vol\, T} = \frac{E_n}{c\, \rho\, A\, d\, T}$
Appendix I	(I.1)	$T = \frac{l\sqrt{\varepsilon_r}}{c}$
	(I.2)	$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$
	(I.3)	$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC}$
	(I.4)	$Z_0 = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\mu_r \varepsilon_r}} \log\left(\frac{b}{a}\right)$
	(I.5)	$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_L - (Z_{01} + Z_{02})}{Z_L + (Z_{01} + Z_{02})}$
Appendix II	(II.1)	$V_{GS} - V_{GS(th)} > V_{GS} > 0$
	(II.2)	$i_d = \mu_n C_{ox} \frac{W_{gate}}{2L_{channel}} \left(V_{GS} - V_{GS(th)}\right)^2 (1 - \lambda V_{DS})$

LIST OF ABBREVIATIONS

A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z

α β γ δ ε ϵ ζ η θ ϑ ι κ λ μ ν ξ ο π ϖ ρ ϱ σ ς τ υ φ ϕ χ ψ ω

Term		Description
BJT	-	Bipolar Junction Transistor
BoM	-	Bill of Material
Ca	-	Calcium
CE	-	Conformitè Europëenne
CSC	-	Cancer Stem Cell
CTM	-	Calibrated Test and Measure
dc	-	Direct Current
DNA	-	Deoxyribonucleic Acid
ECG	-	Electrocardiography
ECL	-	Emitter-Coupled Logic
ECT	-	Electrochemotherapy
EM	-	Electromagnetic
ENEA	-	Italian National Agency for new technologies, energy and sustainable economic development
EP	-	Electroporation
ESOPE	-	European Standard Operating Procedures on Electrochemotherapy
FDA	-	Food and Drug Administration
FFT	-	Fast Fourier Transform
GaN	-	Gallium Nitride
GUI	-	Graphical User Interface
IGBJT	-	Insulated-Gate Bipolar Junction Transistor
in-vitro	-	Research performed or taking place in a test tube, culture dish, or elsewhere outside a living organism.
in-vivo	-	Research or work is done with or within an entire, living organism
IRE	-	Irreversible Electroporation
K	-	Potassium
LED	-	Light Emitting Diode
MEM	-	Modified Eagle Medium
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor
Na	-	Sodium
NHS	-	National Health Service
NICE	-	National Institute for Health and Care Excellence
nsEP	-	Nanosecond Electroporation
nsPEF	-	Nanosecond Pulsed Electric Field
PCB	-	Printed Circuit Board
PEF	-	Pulsed Electric Field
PSU	-	Power Supply Unit

List of Abbreviations.

Term		Description
RADAR	-	Radio Detection And Ranging
REP	-	Reversible Electroporation
Si	-	Silicon
SiC	-	Silicon Carbide
SOA	-	Safe Operation Area
SUMCASTEC	-	Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells
TTL	-	Transistor–Transistor Logic
UK	-	United Kingdom
VNA	-	Vector Network Analyser
V&V	-	Verification and Validation
WHO	-	World Health Organisation
µsPEF	-	Microsecond Pulsed Electric Field

LIST OF SYMBOLS

A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z

α β γ δ ε ϵ ζ η θ ϑ ι κ λ μ ν ξ ο π ϖ ρ ϱ σ ς τ υ φ ϕ χ ψ ω

Symbol		Description
a	-	Outside radius of inner conductor of the coaxial cable
A	-	Area (mm^2)
b	-	Inside radius of outer conductor of the coaxial cable
BW	-	Bandwidth
BV_{CES}	-	Avalanche breakdown voltage/Collector-emitter breakdown voltage across the transistor's collector-emitter terminals (with the base and emitter terminals shorted together)
BV_{DS}	-	Drain-source breakdown voltage
BV_{EBO}	-	Emitter-base breakdown voltage
c	-	Speed of light ($3x10^8$ m/s)/ specific heat capacity ((J/Kg)/°C)
C	-	Capacitor/Capacitance (F)
C_A	-	Avalanche capacitance
C_d	-	Total capacitance of the delay/transmission line
C_{ds}	-	Drain-source capacitance
C_{gate}	-	Total gate capacitance
C_{gd}	-	Gate-drain capacitance
C_{gs}	-	Gate-source capacitance
C_{iss}	-	Input capacitance
C_l	-	Capacitance per meter of a coaxial line (F/m)
cm	-	Heat capacity
C_{oss}	-	Output capacitance
C_{OX}	-	Capacitance due to the gate oxide layer
C_{rss}	-	Reverse transfer capacitance
d	-	Gap between the two electrodes (m)
D	-	Diode
D	-	Duty cycle
E	-	Electric field (kV/mm)/ Energy
E_n	-	Energy delivered
f	-	Frequency/Repetition frequency/Charging frequency
g	-	Avalanche conductance
G	-	Load conductance
g_m	-	Transfer conductance/Transconductance
H	-	Distance of separation between the line and the ground plane of a microstrip line
I	-	Current
I_{Adj}	-	Adjusting current (2.5 mA)
I_{Av}	-	Average current
I_B	-	Base current
I_{BR}	-	Reverse base current
I_C	-	Collector current

List of Symbols.

Symbol		Description
I_{CB}	-	Collector-base current
i_d	-	Drain current/Current through a load
I_{dc}	-	dc current
I_E	-	Emitter current
i_g	-	Gate current
I_P	-	Peak current
I_{USB}	-	Maximum avalanche current
kV	-	Kilovolt ($1x10^3$ V)
l	-	Length of a charged/transmission line
L	-	Inductor/Inductance (L)
$L_{channel}$	-	MOSFET channel length
m	-	Mass (Kg)
m	-	Empirically determined constant that is dependent on the semiconductor material used for the transistor
M	-	Multiplication factor
ms	-	Millisecond ($1x10^{-3}$ s)
n	-	Number of avalanche transistors that are stacked in series
N	-	Number of pulses
ns	-	Nanosecond ($1x10^{-9}$ s)
$\bar{P}$	-	Mean power
P_{Av}	-	Average power
P_{dc}	-	dc power
P_{dis}	-	Power dissipated across a switching element
P_L	-	Power dissipated across a load
ps	-	Picosecond ($1x10^{-12}$ s)
Q_g	-	Gate charge
R	-	Resistor/Resistance
r_A	-	Avalanche resistance
R_C	-	High impedance charging resistor
$R_{DS(on)}$	-	Drain-source on-resistance
$R_{(on)}$	-	On-resistance of a switching element/transistor
S	-	Switch
S	-	Pole location
t	-	Time constant/Pulse duration (width)
t_{on}	-	Application time of the pulsed fields
T	-	Delay time of a charged/transmission line
T	-	Period or repetition rate of the nsPEFs
T_C	-	Internal storage temperatures
T_J	-	Internal operating junction temperature
t_f	-	Fall Time
t_r	-	Rise Time
V	-	Applied voltage/Pulse amplitude (V)
V_{BE}	-	Base-emitter voltage
V_{CC}	-	dc power supply voltage

List of Symbols.

Symbol		Description
V_{CCmax}	-	Maximum voltage the transmission line can be charged to before transistor breakdown occurs
V_{CCmin}	-	Minimum voltage the transmission line can be charged to before transistor breakdown occurs
V_{CE}	-	Collector-emitter voltage
V_{CEO}	-	Voltage across the transistor's collector-emitter terminals with the transistors base terminal left open-circuit, with 0 A base and emitter currents
V_{dc}	-	dc voltage
V_{drop}	-	Voltage drop across component
V_{DS}	-	Drain-source voltage
V_{DSmax}	-	Maximum drain-source voltage
V_{EBO}	-	Base-emitter voltage
V_F	-	Output voltage rating of the voltage regulator
V_{GS}	-	Gate-source voltage
V_{GSmax}	-	Maximum gate-source voltage
$V_{GS(th)}$	-	Gate-source threshold voltage
V_L	-	Pulse amplitude/Voltage dropped across a load
V_{Lmax}	-	Maximum amplitude across a load
V_{Lmin}	-	Minimum amplitude across a load
V_0	-	Output voltage
vol	-	Volume
V_{th}	-	Gate threshold voltage
$V_{\alpha M}$	-	Collector-emitter breakdown voltage when $\alpha M = 1$
V^+	-	Amplitude of the incident pulse/forward signal
V^-	-	Amplitude of the secondary pulse/reflected signal
W	-	Width of microstrip line
W_{gate}	-	MOSFET gate width
Z_L	-	Load impedance
Z_0	-	Characteristic impedance of a charged/transmission line
Z_Σ	-	Total load impedance
ε_{eff}	-	Effective dielectric constant
ε_r	-	Dielectric constant/ relative permittivity of a dielectric material
μ_n	-	Inversion layer majority carrier mobility
μ_r	-	Relative permeability
μs	-	Microsecond ($1x10^{-6}$ s)
$\boldsymbol{\rho}$	-	Density
Γ	-	Reflection coefficient
τ	-	Time constant (RC)
$\boldsymbol{\lambda}$	-	MOSFET channel length modulation parameter
ρ	-	Density
ΔT	-	Estimated temperature rises per pulse
ΔT_{max}	-	Estimated maximum mean rate of temperature rise

CHAPTER I. INTRODUCTION

1.1. Introduction to Thesis

The slow nsPEF electroporation system produced positive polarity nsPEFs with a wide range of pulse characteristics that were optimised to be delivered across a 50 Ω load impedance. A user-selected number of symmetrical pulsed electric fields (PEFs) were produced with adjustable pulse amplitude, duration and repetition frequency to be generated. The parameters associated with the slow nsPEF electroporation system are highlighted in Table 1.1 below.

Table 1.1. The slow nanosecond pulsed electric field electroporation system pulse parameters

Parameters	Minimum	Maximum	Determined by
Pulse Duration (ns)	80	1,000	the gate driving signal from the microcontroller and driver circuit
Amplitude (V)	250	1,400	the FS40 high voltage power supply unit
Repetition Rate (Hz)	1	50	the gate driving signal from the microcontroller and driver circuit
The Number of Pulses Generated	1	1,000 or continuous	the gate driving signal from the microcontroller and driver circuit
Rise / Fall Time (ns)	35		the MOSFETs rise time and gate-source current

This topology is dependent on the capability of state-of-the-art Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) operating in a push-pull configuration, that was driven by gate-driving optocouplers, and an appropriate microcontroller was used to control the system.

The fast nsPEF electroporation system was designed to generate positive, and negative nsPEFs, or simultaneous generation of both positive and negative PEFs, depending on the positioning of the load with respect to the system ground plane. It has been demonstrated in this work that this system can produce a variety of user-specified symmetrical nsPEF of various pulse widths, amplitudes and repetition frequencies. The system has been optimised such that the pulses are delivered across a 50 Ω load impedance without pulse reflections. The fast nsPEF electroporation system can generate pulse parameters highlighted in Table 1.2. The topology utilises relatively slow charging and ultrafast discharging of a coaxial transmission line in conjunction with a stack of avalanche breakdown transistors, which operate as a fast-switching element, producing PEFs with a transition time less than two nanoseconds. In this work, transition time is defined as the time it takes for a pulse to rise from 10 % to 90 % of its steady value or fall from 90 % to 10 %.

Table 1.2. The fast nanosecond pulsed electric field electroporation system pulse parameters

Parameters	Minimum	Maximum	Incremental increase	Determined by
Pulse Duration (ns)	10	300	10	the transmission line length
Amplitude (V)	100	2,500	100	the number of avalanche transistors stacked
Repetition Rate (Hz)	1	1,000	1	the charging and discharging times associated with the transmission line
The Number of Pulses generated	1	1,000 or continuous	1	the input trigger signal
Polarity	Positive, negative or simultaneous generation of positive and negative pulses			the location of the load between the charged line and the ground plane
Rise / fall time (ns)	< 1			FMMT417 avalanching timing

These electroporation systems were designed to produce a wide range of nanosecond pulsed electric fields. In the design of these electroporation systems, the following parameters were considered: voltage amplitude, pulse ringing and overshoot, pulse duration, pulse repetition frequency and the number of pulses generated. Both systems used different topologies to produce different nsPEF properties for distinct applications. The design of the slow nsPEF electroporation system is best suited to the generation of nsPEF with pulse durations of 100 ns or greater, whilst the fast nsPEF electroporation system is better suited to the generation of short PEFs in the sub-100 ns time regime.

The primarily clinical effect goal of this work was to provide a preliminary cellular, histological and clinical evaluation using the slow and fast pulse generators on biological cell samples in an *in-vitro* and *in-vivo* environment. As part of this evaluation work cell samples consisting predominantly of CSCs were investigated. Cell manipulation and control of cell physiology effects due to the application of nsPEF were pursued through investigating cell permeabilization, viability and thermal effects from *in-vitro* studies, while histological, morphological, collagen effects and thermal effects were investigated using *in-vivo* models. The aim was to prove the concept of such an energy modality before further developing the development of the nanosecond pulsed electric field modules for use in a clinical environment.

1.2. Motivation

Cancer is the leading cause of death worldwide. With a growing and ageing population, with more complex needs, cancer-related deaths continue to rise at an alarming rate (Fig. 1.1). In 2017 there were 17 million cases and 9.6 million deaths associated with cancer worldwide [1]-[2]. The projection of cancer-related cases and deaths is alarming, with the World Health Organisation (WHO) international agency for research on cancer estimating 29.5 million new cases and 16.4 million deaths worldwide, (Fig. 1.2), and 0.26 million death and 0.61 million cases in the United Kingdom alone by 2040 (Fig. 1.3) [2].

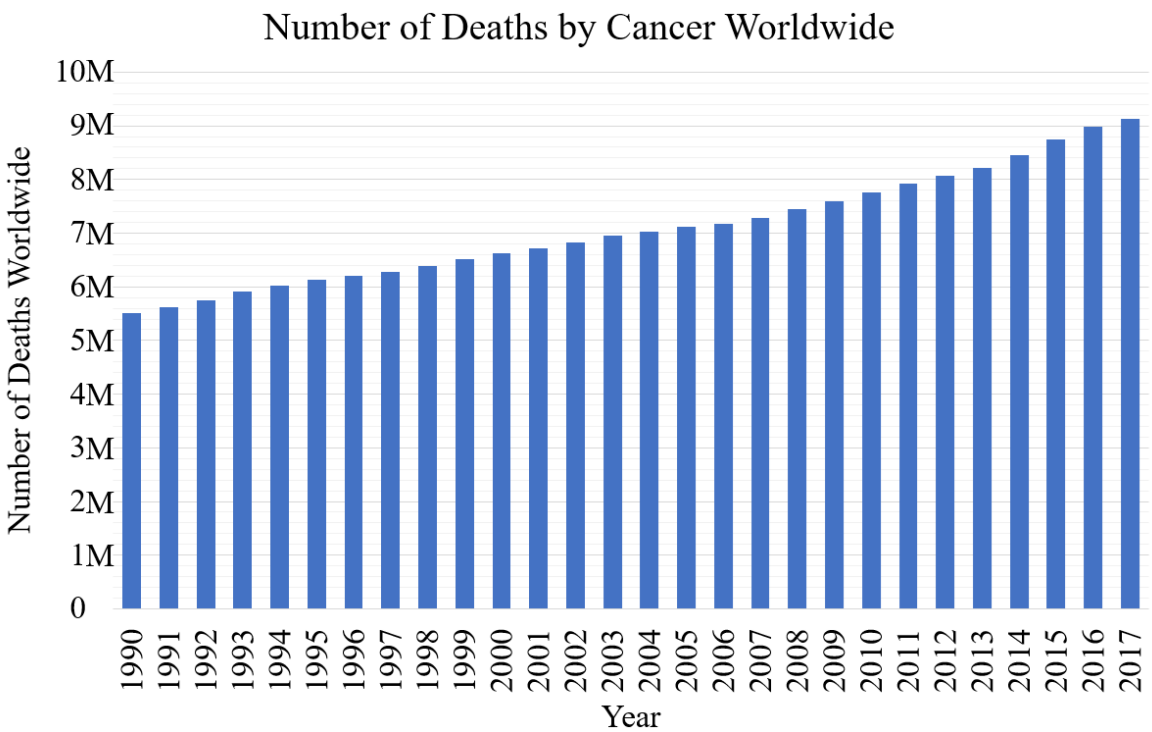

Fig. 1.1. Number of deaths by cancers worldwide (1990 – 2017) [2]

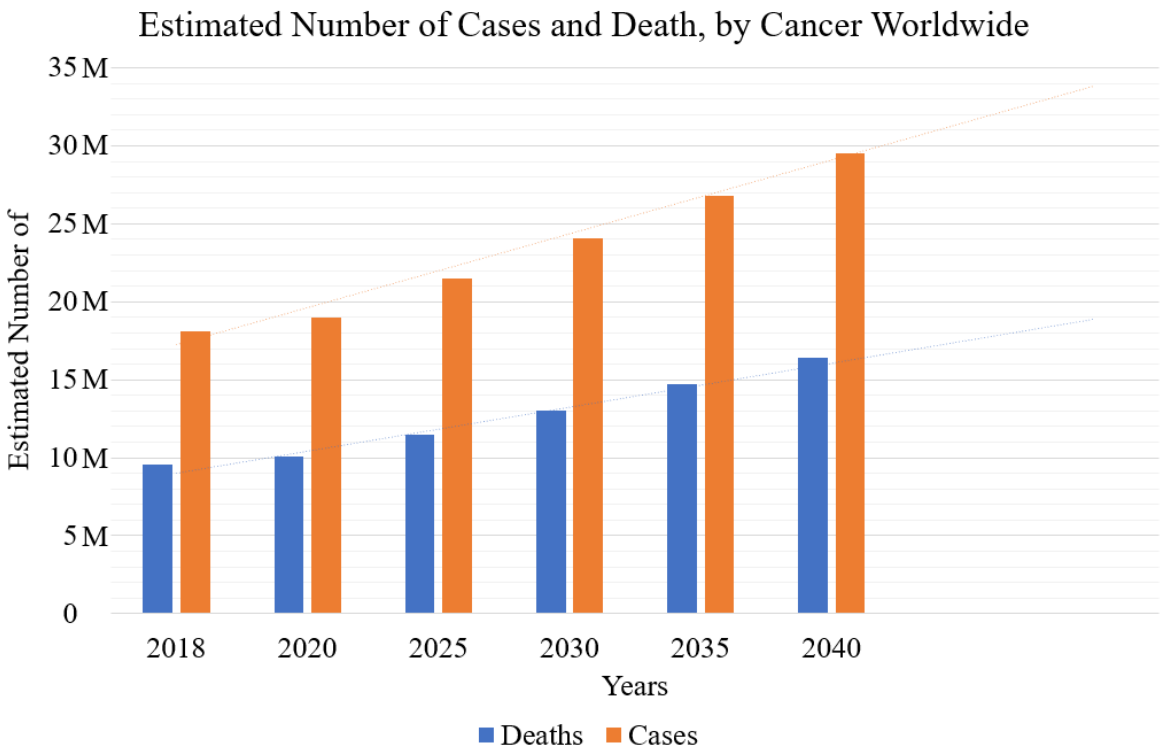

Fig. 1.2. Estimated number of deaths and cases by cancers worldwide (2018 – 2040) [2]

Fig. 1.2 and Fig. 1.3 highlight the increasing and predicted increase of cases and deaths per year associated with cancer [1]-[3]. The increasing number is primarily related to the increase in the ageing population and lifestyle. Developments in medical technology have resulted in increased life expectancy and improved accuracy in earlier detection and diagnosis of diseases, such as cancer. An increase in life expectancy results in a higher percentage of the public living at an age where they have

a higher risk of developing cancer [1]-[5]. Modern medicine and research have increased awareness, accessibility, evaluation, diagnosis and staging of the majority of cancers, resulting in earlier diagnosis [1]-[5].

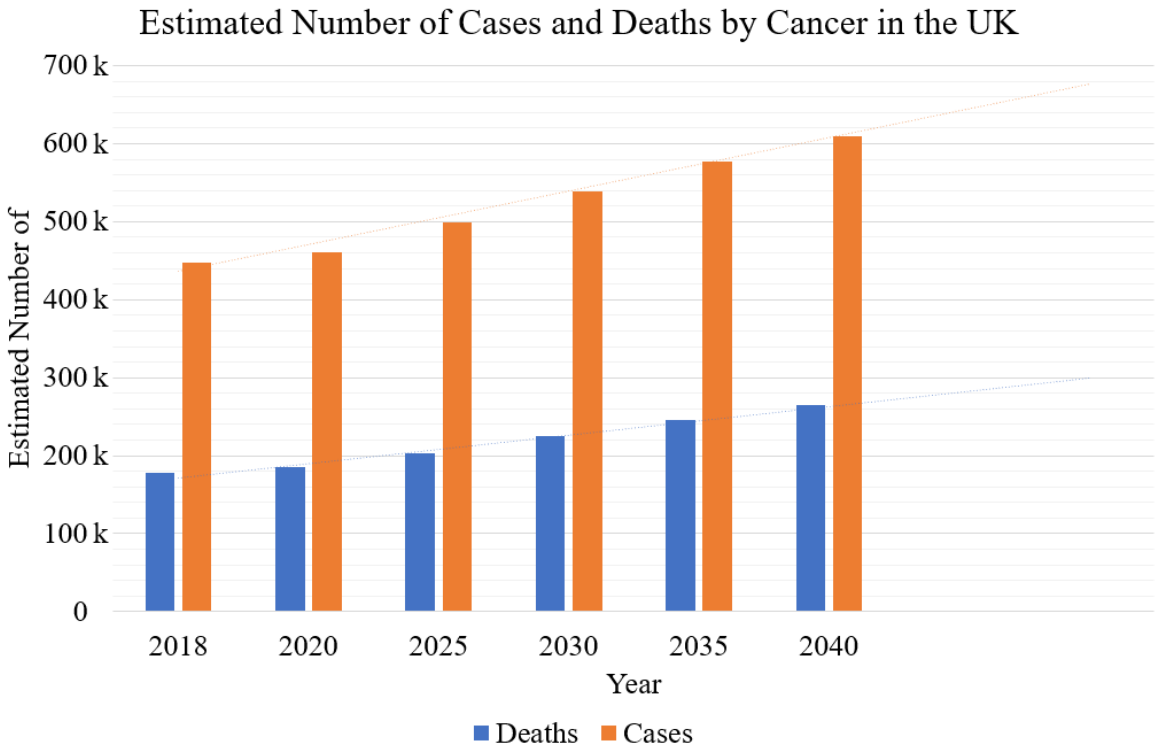

Fig. 1.3. Estimated number of deaths and cases by cancers in the United Kingdom (2018 – 2040) [2]

Conversely, there have been significantly fewer developments in the treatment of cancer in comparison to the diagnosis of the disease. In these modern times, prominent cancer treatment consists of three conventional cancer treatment strategies: chemotherapy, radiotherapy, and surgery. The application of these conventional cancer treatments is on the rise, yet statistics suggest adopting a more rigorous and novel treatment approach to fight this disease is required [6]-[8]. These conventional therapies also have a high associated cost of treatment and patient after-care, in addition to the aggressive side effects associated with the application of ionised ration and poison into the body. Side effects include increased risk of infection, nausea, hair loss/thinning and fatigue to name a few [6]-[8]. These findings lead to a definitive requirement for an alternative treatment, which is safe (with minimum side effects), effective, yet affordable and offers better overall patient outcomes. Such alternatives are non-ionising energy based on non-thermal and thermal ablation. The focus of this work is on the development of a novel non-thermal ablation system.

PEFs application, in the form of electro-pulsation, is a new non-thermal alternative ablation treatment for cancers. The treatment can be administered as a single or combinative energy modality. Electro-pulsation, in the form of classical electroporation in the microsecond (μs) to millisecond (ms) pulse duration regimes has been evaluated clinically as an alternative treatment and is well documented

by the National Institute for Health and Care Excellence (NICE), the Food and Drug Administration (FDA), and PubMed [9]-[10]. Faster duration and higher amplitude pulsed electric fields in the nanosecond (ns) range have been hypothesized by microbiologists to offer advantages over millisecond and microsecond pulsed electric fields.

The development of the versatile slow and fast nanosecond pulsed electric field (nsPEF) electroporation systems introduced in this work will accelerate the clinical evaluation of nsPEF energy as a new energy modality and hopefully provide an alternative cancer treatment to slow down or possibly eliminate cancer in the future.

1.3. Clinical Need

Advancement in cancer research has provided numerous methods and techniques to understand, diagnose and monitor all cancers, hence the increase in the number of cancer cases identified over the last decade and expected cases in the future, (Fig. 1.1 to 1.3) [6]-[7]. Unfortunately, the number of deaths has simultaneously increased with the number of cases detected, indicating that conventional cancer treatments are ineffective and therefore a safe, effective, affordable alternative treatment (with minimum side effects) to eradicate or selectively neutralize various cancers is required.

1.3.1. Cancer Stem Cells (CSCs)

Recent findings indicate that Cancer Stem Cells (CSCs) hold the key to treating and possibly eradicating cancer. Researchers state that targeting CSCs offers the potential to transform the way we confront this disease. CSCs play a key role in the initiation, invasion, and reoccurrence of cancerous tumours [11]-[13]. It may be possible to treat cancers more effectively with a novel alternative therapeutic energy modality or a combination of various energy modalities, such as chemotherapy, radiotherapy, thermal ablation etc, which targets CSCs to potentially halt growth and shrink or neutralize the tumour mass.

1.3.2. Current Clinical Applications

Traditional cancer treatment, such as surgery, chemotherapy and radiotherapy, are the main treatment therapies for many types of cancer. These treatments have been the pinnacle of cancer treatment therapies over the last half a century (Radiotherapy 1895, Chemotherapy 1940’s) [11]-[13]. All of these treatment modalities pose substantial patient side effects [14]. In addition to the side effects associated with each traditional treatment, research indicates that these treatments have no or minimal effect on CSCs [11]-[13].

CSCs are considered resistant to chemotherapy and radiotherapy treatments, and therefore remain after the course of treatment, allowing the tumour to flourish, and spread around the body [11]-[13].

This provides a possible reason why the rate of death due to cancer is increasing each year and highlights the need for new approaches to treat cancer effectively and prevent cancer metastasis and relapse.

1.3.3. Electropulsation

Electroporation is an alternative treatment modality which is gaining traction in the medical world in the fight against cancer. Conventional Electroporation or Irreversible Electroporation is a relatively new procedure, where a cancerous tumour is exposed to pulsed electric fields in the milli-to-microsecond time regime. These pulsed electric fields are applied across the tissue structure to reversibly or irreversibly increase the permeability of the cellular membrane of cells within bulk tissue, allowing chemicals, drugs, or Deoxyribonucleic acid (DNA) to be introduced into the cell by the formation of defects or pores in the cell membrane [9]-[13], [15]-[16]. Electroporation (EP), Irreversible Electroporation (IRE) and Electrochemotherapy (ECT) are becoming accepted treatment methods for specific cancer types such as skin, renal, prostate, liver etc. in the United Kingdom (UK) and already have relevant National Institute for Health and Care Excellence NICE guidelines [9]-[13], [15]-[16].

1.3.4. Nanosecond Electroporation

Nanosecond electroporation (nsEP) is an adaptation of classical electroporation where the pulsed electric fields are generated in the nanoseconds (ns) regime. This therapeutic technique is in its infancy and is thought to have additional potential for cell manipulation and control of cell physiology in comparison to the conventional EP. Literature suggests effects could include increased plasma membrane permeabilization, calcium (Ca^+) release, ion channel activation and apoptosis induction [11]-[13], [17]-[20].

nsEP is in its infancy in practice, but leaders and theorists in the field suggest that this energy modality could hold the key to a wide range of microbiological effects to be induced and revolutionise modern medicine. Possible clinical applications include cancer treatment, regenerative medicine, sterilisation, non-thermal tissue ablation, electro-fusion, gene therapy, and more. The potential applications are dependent on the electrical parameters associated with the nsPEFs generated, and the geometry of the electrode structure used for the delivery of these electric fields into cells and bulk tissue. Parameters that can be controlled are the duration of the pulses (pulse width), the amplitude of the pulses, the repetition frequency of the pulses, rise/fall times of the pulses, pulse ringing or overshoot, and the number of pulses generated.

1.4. Technology as a Key Enabler

Advances in semiconductor materials have made semiconductor transistor technology a viable option for nanosecond switching of high-amplitude electric fields. Recent developments in wide bandgap semiconductor materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) offer

advantages over traditional Silicon (Si) based transistors in terms of use as a fast switch with lower ON-resistance and lower gate-source and gate-drain capacitance [21]-[23].

SiC MOSFETs are viable technology to produce the slow nsPEF electroporation system for the initial concept prototype non-thermal energy modality of nsEP for future applications within a clinical environment. Section 3.2.2. highlights why SiC MOSFETs were preferred over GaN based-MOSFETs.

Also advances in high frequency / high voltage passive components that can be operated in the microwave region of the electromagnetic spectrum (Fig. 1.4), such as well-matched microwave connectors, high voltage microwave capacitors and low loss cable assemblies make it possible to deliver pulses with rise/fall times of less than 300 picoseconds (ps) and peak voltages in excess of 1 kV. Such technological development is a key enabler for nsPEFs production to validate primary research into fast nsPEF, in the few to low tens ns duration and possible picosecond PEF in the future.

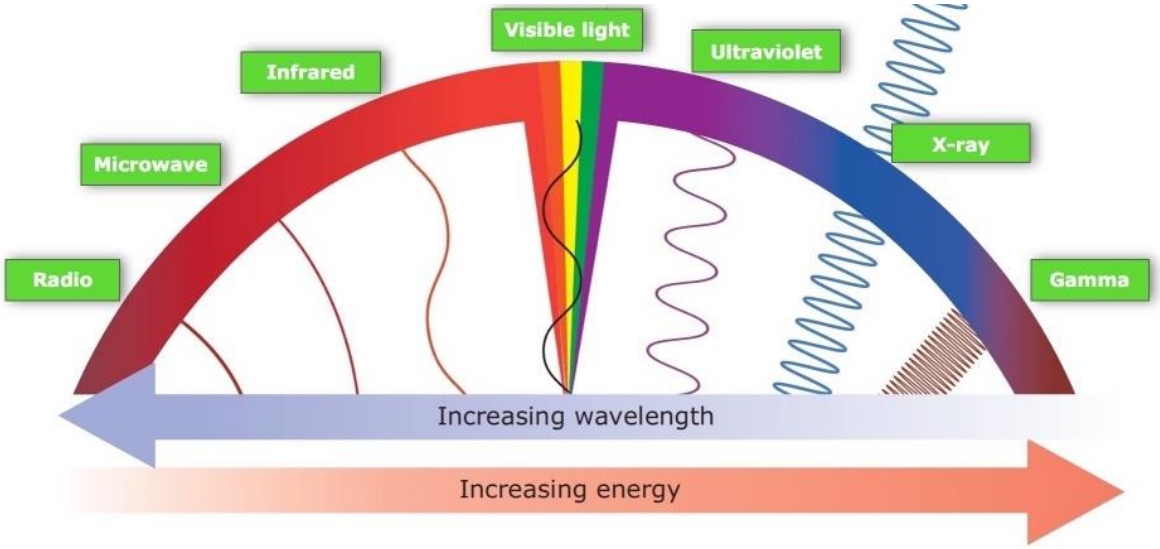

Fig. 1.4. The electromagnetic spectrum showing frequencies of electromagnetic radiation and their associated wavelengths [24]

1.5. Goals and Objectives

The goal of this research is to develop two high voltage nsPEF electroporation systems to open nanopores in biological cells and bulk tissue. The first system is the slow electroporation system that produces pulses of amplitudes in excess of 1 kV and pulse duration of greater than 100 ns. The second system produces fields of similar amplitude, but with pulse widths of less than 100 ns and rise/fall times of less than 1 ns.

The objective of the slow electroporation system was to create a versatile generator that could generate a wide range of high voltage electric fields with pulse widths from 100 ns to 300 ns using state-of-the-art MOSFET based switches. This objective pushes the limits of semiconductor solid-state components in terms of high-speed switching and high voltage capability. In addition to challenging

the possible applications of recent advances in solid-state switches, the goal was to advance and further understand, the effects of nsPEFs within a clinical environment.

The objective of the fast nsPEF electroporation system was again to create a versatile electroporation system that is capable of generating a wide range of high voltage (500 V+ peak) pulses with nanosecond pulse widths and sub-nanosecond rise/fall times. This work aims to further investigate and research the effect of nanosecond pulsed electric fields on biological cells and bulk tissue.

The biological objectives associated with this work were to investigate the effect of various nsPEFs on isolated single-cell population loads in an *in-vitro* environment and bulk porcine liver tissue. These initial investigations provide a proof of concept to determine the effect of nsPEF on cell populations enriched in CSCs and liver tissue in a pre-clinical environment. The successful outcome of this work will lay the groundwork for future feasibility work using nsPEFs on a range of cancer cells and tumours within the human body.

The vision for the nsPEF electroporation systems developed in this work is to achieve targeted non-thermal neutralization of a specified cell population enriched in CSCs, supporting both the *in-vitro* and the *in-vivo* testing to provide the necessary confidence to support further research in biology and medicine.

1.6. Description of Thesis

This research aim was to design and validate a high voltage nsPEF electroporation systems to advance biomedical investigations in the field of nsEP. Two nsPEF electroporation systems were designed, developed, and built from different topologies resulting in a slow and a fast nsPEF electroporation system. The pulsed field systems were validated using predominantly cancerous biological cells enriched in CSCs and bulk tissue (porcine liver). This thesis focuses on several key areas related to the research and development of slow and fast high voltage nsPEF generators for biomedical applications.

Chapter 1 provides a general introduction to the work described in this thesis.

Chapter 2 considers background information on the clinical need and provides a review of current techniques used to generate pulsed electric fields to cells and bulk tissue.

Chapter 3 addresses the technical/engineering strategy, medical/electrical verification, and validation associated with the slow nsPEF electroporation system. Chapter 3 highlights the technological and physical requirements for the overall design, development, and implementation of the slow nsPEF electroporation system.

Chapter 4 focuses on the testing of the slow nsPEF electroporation system on biological cells, bulk tissue, and other tissue structures.

Chapter 5 is focused on the technical/engineering strategy and electrical validation of the fast nsPEF generator. Chapter 5 also highlights the technological and physical requirements for the instrumentation associated with the fast nsPEF electroporation system.

Chapter 6 focuses on investigating the effects of the fast nsPEFs on biological cells within a bulk porcine live tissue.

Chapter 7 summarises the work presented in this thesis. In this chapter future work associated with both the slow and fast electroporation system is also presented.

Chapter 1 References

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CHAPTER II. BACKGROUND AND LITERATURE REVIEW

2.1. Introduction

This chapter introduces electropulsation/electroporation (EP) application, with a focus on Cancer Stem Cells (CSCs), and literature reviews of technology available for the generation of nanosecond electroporation (nsEP).

In the context of this work, nsEP is the cellular and/or tissue effect of nanosecond pulsed electric fields (nsPEFs). Where nsPEFs are symmetrical voltage signals with transition times (rise time (t_r) and fall time (t_f)) less than 50 ns, and pulse widths in the nanosecond regime (nanosecond (ns) to microsecond (µs)). The high voltages associated with the electric fields generated in this work are 500 V and above.

This chapter is divided into four distinct sections. Firstly, a brief clinical description of CSCs and their relevance in terms of cancerous tumours and nsEP. Secondly, a section on the clinical evaluation of electroporation. This includes the parameters associated with electro-pulsation signals, and clinical evaluation and review of classical EP (microsecond (µs) to millisecond (ms) time regime), and nsEP (ns to µs time regime) as advanced electrosurgical techniques. This section includes a background and literature review of work carried out within the field of electroporation. A technical evaluation section of the advances in dielectric materials and semiconductor technology is the third section introduced in this work. Advances in dielectric materials and semiconductor technology are the key enablers in the development of high voltage fast switching instrumentations. The last section consists of a comparative overview of the technologies that can generate high voltage nsPEFs.

2.2. Cancer Stem Cells

Cancer is the leading cause of death worldwide, and the number of new cancer cases and deaths is on the rise globally. The rise in new cases is mainly due to the increasing age of the population and the abundance of cancer-specific screenings available. Fig. 1.1 to Fig. 1.3 reinforces that the number of cancer-related death increase at a similar rate to new cases. This implies that conventional cancer treatments are ineffective and there is a crucial need for an alternative treatment [1]-[2].

Developments in cancer research indicate that CSCs play an integral role in malignant tumours. CSCs and cancerous cells have an intricate relationship, and this relationship was originally identified in leukaemia. Evidence validates that CSCs are found in many solid primary tumour types including breast, prostate, brain, and colon carcinomas [3]-[7].

CSCs are tumour-initiating cells that have stem-like characteristics and possess the capacity for self-renewal and for causing the heterogeneous lineages of cancer cells that comprise the tumour. They have properties that differ from the rest of the tumour population. Their rate of division is at a much slower pace than cancerous cells, which allows them to resist traditional cancer treatment such as radiotherapy and chemotherapy which targets fast-multiplying cells. Traditional cancer treatment only targets the bulk of the tumour but cannot deal with CSCs [3]-[7].

CSCs play a critical role in tumour initiation, invasion, metastasis, and recurrence at or from a primary site. Microbiologists consider CSCs to represent the bad seed of tumours. CSCs have very efficient pathways to draw out drugs, making them highly resistant to chemotherapy and other drug-related therapies. Their amplified deoxyribonucleic acid (DNA) damage repair is an attribute to CSCs resistance to radiation (radiotherapy), although other common mechanisms of resistance can contribute significantly to the insensitivity of CSCs to radiotherapy [3]-[7]. An analogy of CSCs function in a seeded tumour can be described by a weed analogy as illustrated in Fig. 2.1.

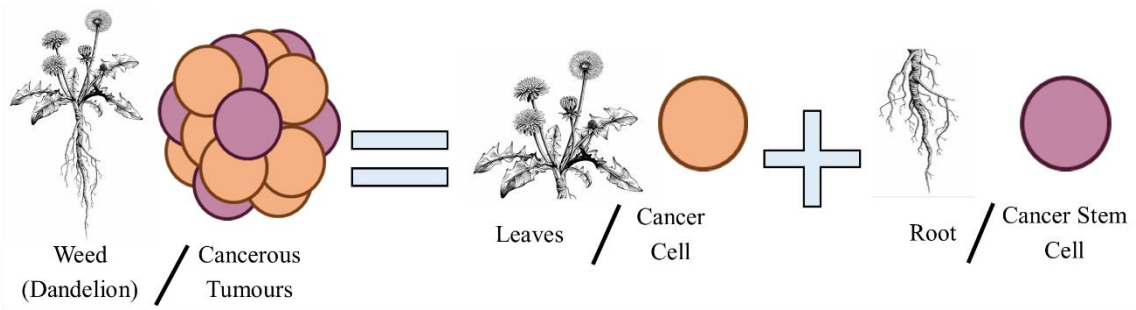


Fig. 2.1. Cancer Stem Cells description as a weed analogy

A cancerous tumour can be compared to a noxious weed, as shown in Fig. 2.1. Noxious weed is a wild plant growing where it is unwanted that competes with cultivated plants (normal cells), as both are unwelcomed growths that are hard to contain or eradicate. A weed is composed of flowery leaves and roots. It is said when tackling weeds (tumours), one must eradicate both root (CSCs) and flower (cancerous cells). Conventional cancer treatment can be thought of as an inexperienced gardener that would pluck/pick the weed on the surface, leaving the roots behind, and so the weed will resurface again in the future.

To successfully diminish a weed, one must eliminate its roots, resulting in the eradication of the weed. This is the same with tumours. For the successful remission of cancerous tumours, one must eliminate both the cancerous cells and cancer stem cells. If CSCs remain at the tumour sight the tumour can reoccur or migrate within the body, resulting in relapse [3]-[7].

Therefore, eliminating CSCs has the potential to eradicate the disease. The targeting of CSCs would represent a shift in treatment focus and requires the identification of novel treatments as shown in Fig. 2.2. Neutralizing CSCs may have the potential to radically change the strategy currently in place

for cancer treatment [6]-[8]. The underlying idea is to refer to cancer as a hierarchical entity, comprising of various cell populations with distinct characteristics.

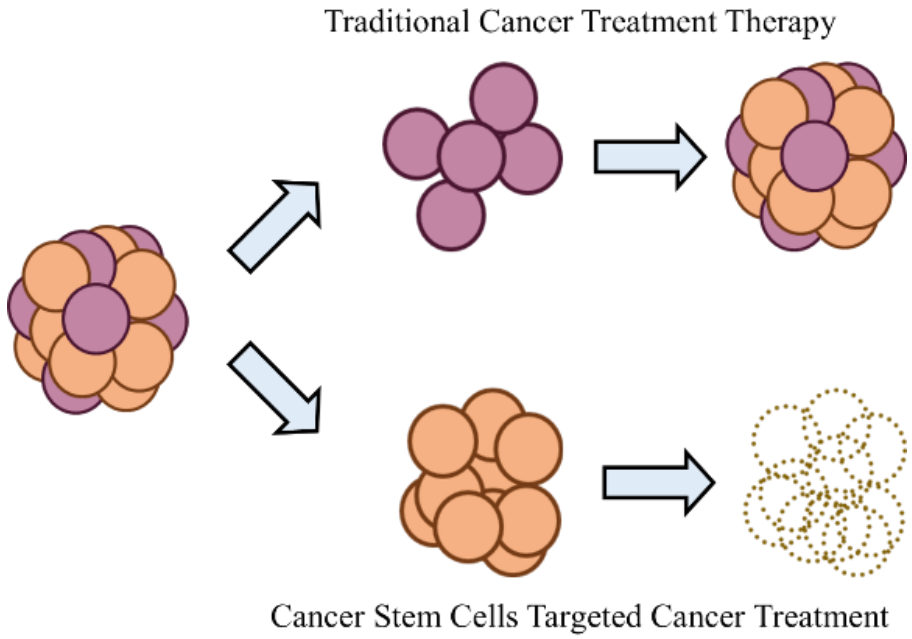


Fig. 2.2. Cancer treatment strategies: Cancer cells (conventional treatment) vs Cancer Stem Cells targeted cancer treatment strategy.

The identification of proliferation and differentiation pathways that are active in CSCs, but not in normal cells, could offer interesting new opportunities for selective therapies in terms of the eradication or promotion of differentiation of CSCs and tumour shrinkage through conventional treatment of targeting cancerous cells [4], [6].

2.3. Clinical Evaluation of Electroporation

2.3.1. Electro-pulsation

As discussed, eliminating CSCs has the potential to eliminate cancer as a disease. Targeted neutralisation of CSCs is a notion that has the potential to radically change the strategy for cancer treatment.

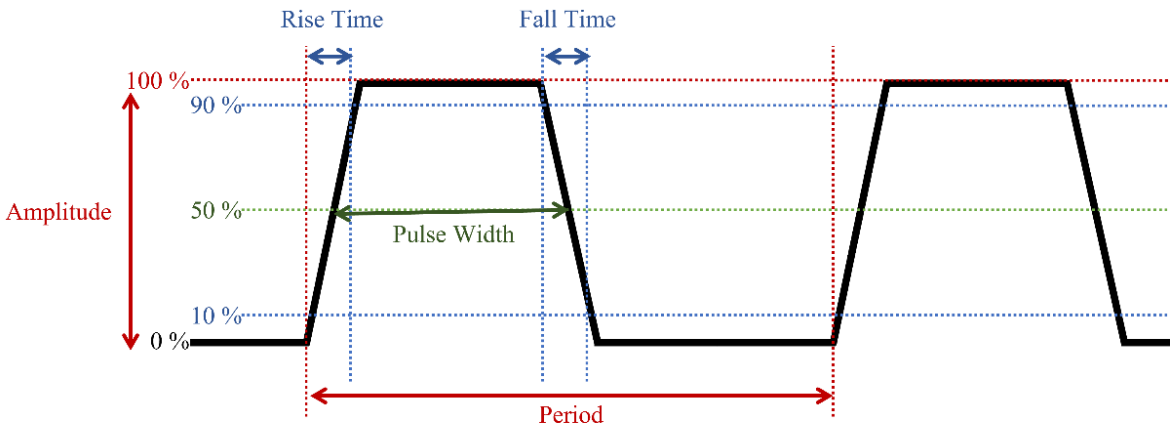
The application of pulsed electric fields (PEFs) or 'electro-pulsation' is considered a novel treatment for CSCs. PEFs has been proven to increased cell plasma membrane permeabilization, thus enabling the introduction of small molecules, ions, and modulation of cell viability. This effect is defined as electroporation. Electroporation is the application of controlled high voltage electrical pulses onto living cells and tissues for a short duration of time. Electro-pulsation technology is based on pulsed power technologies and refocuses cancer treatment from chemical and drugs-based treatment to physics by administering pulses of non-thermal, high-intensity electrical fields, to tumours [3]-[7], [9]. This

constitutes as a high voltage, low-energy impact that is unique and distinct from other medical technologies.

The biological effect of the applied PEFs can be divided into parameters of the electric field parameters [9]-[11]. PEFs parameters include waveform, electric field strength (the pulse amplitude across a specific distance i.e., distance between two electrodes), pulse width (or duration), transition times (rise and fall times), pulse repetition frequency and number of pulses the biological load experiences.

Waveform

Two PEFs waveform formations exist; These are square or exponential decay waveforms. Square waveforms are symmetrical pulses with ideally rapid and identical rise times (t_r) and fall times (t_f) to a set voltage amplitude. Rise/fall times are defined here as the time it takes for the voltage to rise from 10% to 90 % and fall from 90% to 10% of the final value. The pulse amplitude is measured from the highest voltage level of the pulse (100 %) with respect to 0 V (0%). These definitions are shown in Fig. 2.3.



$$Period = \frac{1}{Pulse\ Repetition\ Frequency} \qquad \text{Duty Cycle} = \frac{Pulse\ Width}{Period}$$

Fig. 2.3. Labelled parameters of a square or symmetrical pulsed electric field waveform

Exponential decay is generated by the complete discharge of a capacitor. Square waveforms yield higher efficiencies and visible control of electric field parameters in comparison to an exponential decay wave system [9]-[11]. This work focuses on generating square PEFs.

Electric Field Strength

The electric field strength (E) is measured as the voltage (V), the pulse amplitude, delivered across a distance between two electrodes (d) and can expressed in kV/mm as shown in equation (2.1). It is critical for the electric field strength to surpass the electrical potential of the cell membrane to allow the temporary reversible or irreversible permeation, or “pore formation” to occur on a cell membrane [3]-[5].

$$E = \frac{V}{d} \tag{2.1}$$

Pulse Width

The pulse width, or duration, is the time the sample, or load, is exposed to the electric field per cycle. The time, or pulsed electric field duration, works indirectly with the electric field strength to increase pore formation and associated effects. Pulse width is a key variable that works with voltage amplitude (or electric field) and needs to be considered when optimizing electrical parameters to maximize the results for a given cell and/or tissue type [3]-[5], [9]-[11].

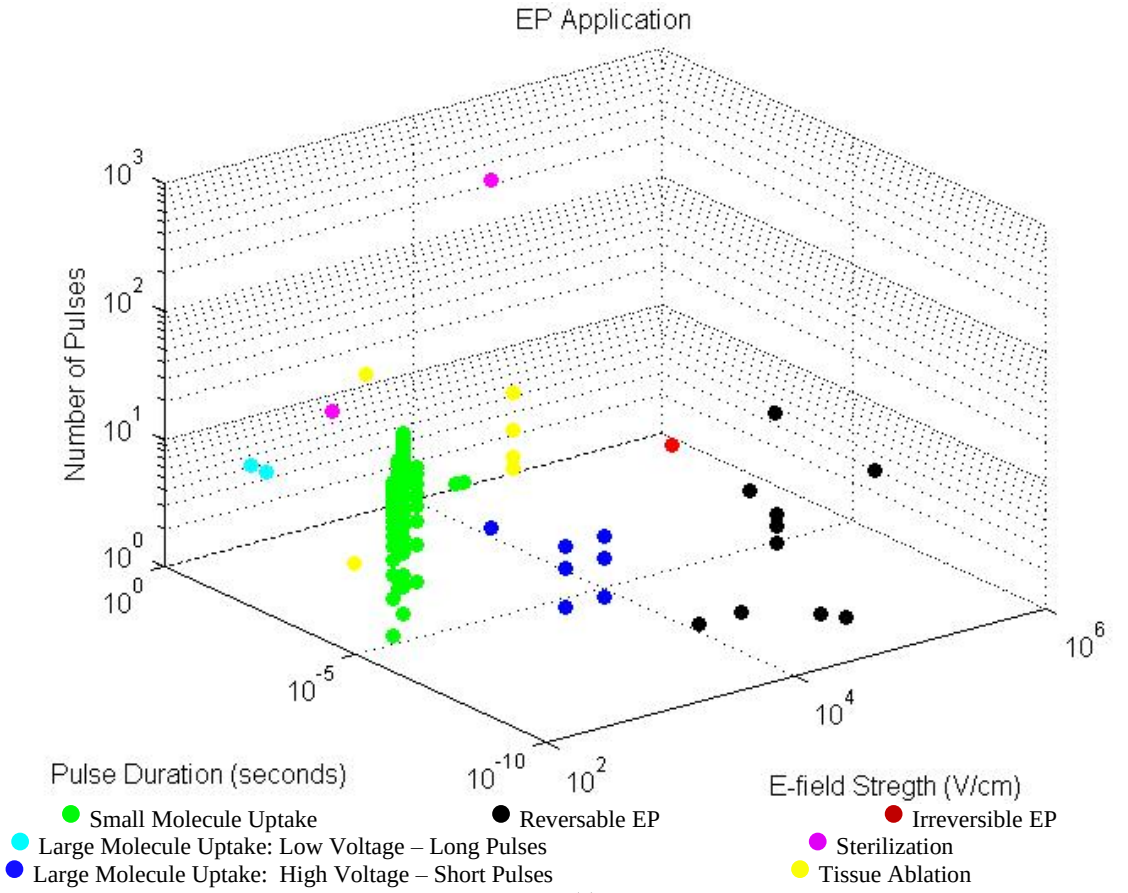
Number of Pulses and Repetition Frequency

Electroporation is typically carried out as a single electric field pulse. However, some cells and tissues may require multiple pulses to achieve electro-permeabilization. The number and repetition frequency of the applied PEFs determine the exposure time that a cell or tissue is exposed. This exposure time has a similar effect to the pulse width, the longer the exposure time the more significant the effect of cell permeabilization. The optimisation of the pulse number and pulse repetition frequency determines the effect the exposure of PEFs has on the biological load. At a point in time, exposure to PEFs can have an adverse effect on cell membranes where permeabilization can become irreversible and the effect becomes thermal ablation [3]-[5], [9]-[12].

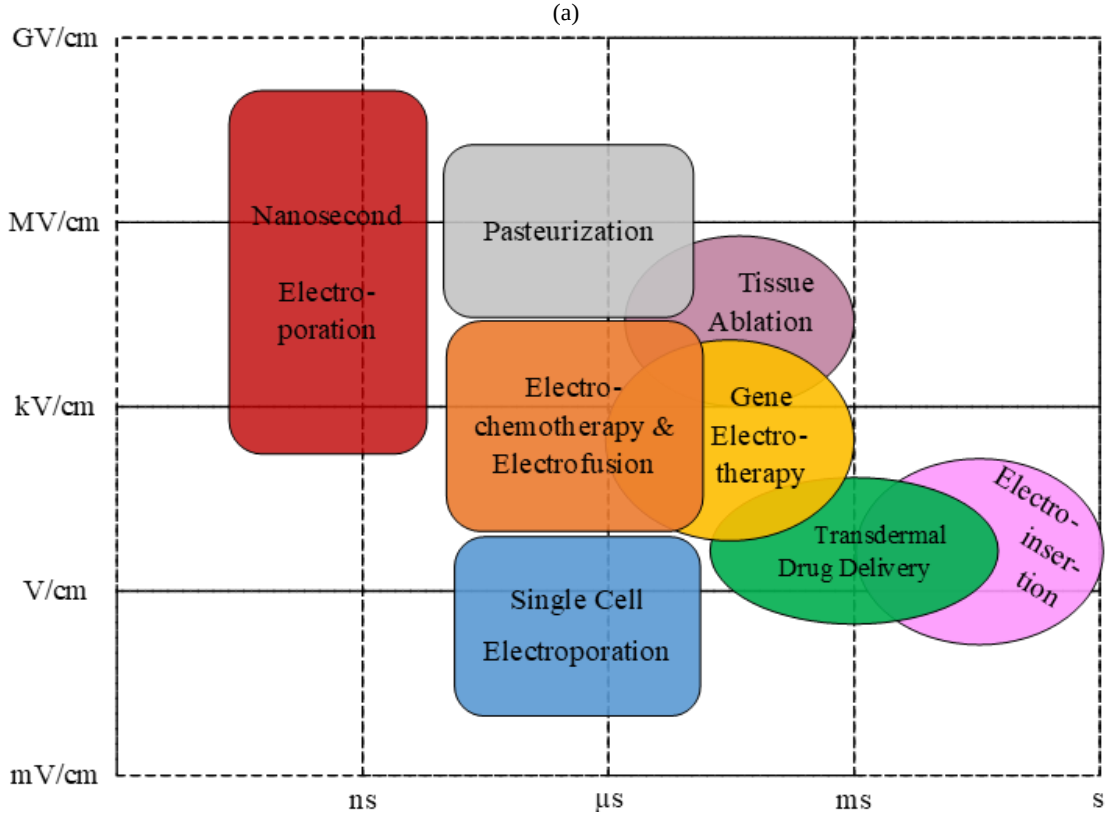
Thermal Effect

The short duration (pulse width), low repetition frequency and the low number of PEFs ensure that the energy delivered into the biological system is non-thermal [3]-[5], [9]-[12]. A non-thermal approach to neutralising CSCs is an appealing treatment approach since it potentially allows for a targeted neutralization of a tumour without heating the cells above body temperature. This would result in predominantly sparing healthy cells, no damage to the extracellular matrix that contains the cells, preservation of nearby vessels and structures whilst allowing tissue regrowth and preventing unwanted damage to patient tissue. The increase in temperature during treatment is proportional to the applied PEFs and is therefore dependent on the electrode configuration utilized at the time. The non-thermal aspects of such energy modality have additional benefits over traditional thermal ablation. Therefore, can be used for the treatment of cancers in regions of the body where the thermal effect is undesirable, such as the: brain, spine, lung, bladder etc. [3]-[5], [9]-[12].

In conclusion, the parameters of the PEFs applied to cells and tissues, such as electric field strength, duration, and the number of applied PEFs determine the biological changes to the tissue structures and the end application. Fig. 2.4 illustrates the generalised versatile representation of PEFs parameters, their effects, and specific clinical applications of the applied electro-pulsation pulse(s).



(a)



(b)

Fig. 2.4. Electroporation application and effect on cells and tissues (a) with various pulsed electric field parameters (pulse duration, Number of pulses and electric field strength) [3]-[7] (b) generalised representation [13]

2.3.2. Classical Electroporation

Classical electroporation is a physical mechanism in which externally controlled PEFs, in the microsecond-to-millisecond time regime (10 µs – 100 ms), are applied to cells. These applied PEFs are known to cause changes in the cellular membrane, resulting in increased plasma membrane permeabilization, thus enabling the introduction of small molecules and modulation of cell viability [6]-[8]. An increase in cell permeability will provide either a reversible or irreversible permeabilization effect. To date, electroporation has been successfully exploited as a medical technique introduced intraoperatively, laparoscopically, and percutaneously [3]-[5], [14]-[16].

An increase in the permeability of the cell membrane is believed to be related to the formation of defects called 'nano pores' in the cell membranes [17]-[18]. The generation of the pores has been demonstrated with molecular dynamic simulations and practically, illustrates the water channels resembling pores that are created in the bilipid membrane under high electric fields.

When an electric field larger than a cell's transmembrane voltage (typically ~ 0.2 V) is applied, ions in the conductive cytoplasm rapidly redistribute. Positive ions move to the membrane to face the negative pole of the electric field and negative ions move to the membrane facing the positive pole, thus creating the pores [6]-[8]. This ion redistribution will charge the capacitance of the plasma membrane generating an equal and opposite field to that applied so that the net field within the cytoplasm is zero. However, this charge redistribution is not instantaneous, and it takes a certain amount of time for nanopores to be produced. Cell membrane permeability is very high during electric field delivery and decreases after delivery, yet membrane permeability can be significantly large for some minutes after. The permeabilization effects, or nanopore generation, can be reversible or irreversible depending on the electric field strength and duration of the field applied [3]-[5], [14]-[18].

Reversable Electroporation

Reversible electroporation (REP) is the application of suitable pulsed electric fields to cells or tissues, inducing reversible permeabilization of cell membranes. This facilitates non-permeant or poorly permeabilised cells resulting in viable cells after the period of increased permeability where nano-pores are formed and then closed. REP can be optimized to introduce small and large molecules, the fusion of cells and the insertion of proteins into the cell membrane and bulk tissue. It is predominantly used for electrochemotherapy (ECT) and gene therapy, allowing delivery of cytotoxic drugs or plasmid DNA into tissues [3]-[5].

The PEF parameters are carefully selected to preserve the viability of cells. An electric field strength of 400 V/cm (40kV/m or 40 V/mm) is considered the threshold for reversible electroporation in tumour tissue. Typically, 8 pulses of the 100 µs, 400 V/cm PEFs with repetition frequencies ranging from 1 Hz (1 second period, 0.0001 % Duty Cycle) to 5 kHz (200 µs, 50 % Duty Cycle) are used for

reversible electroporation. REP pulse parameters are illustrated in Fig. 2.5. Nowadays it is widely used in various biological, medical, and biotechnological applications [3]-[5].

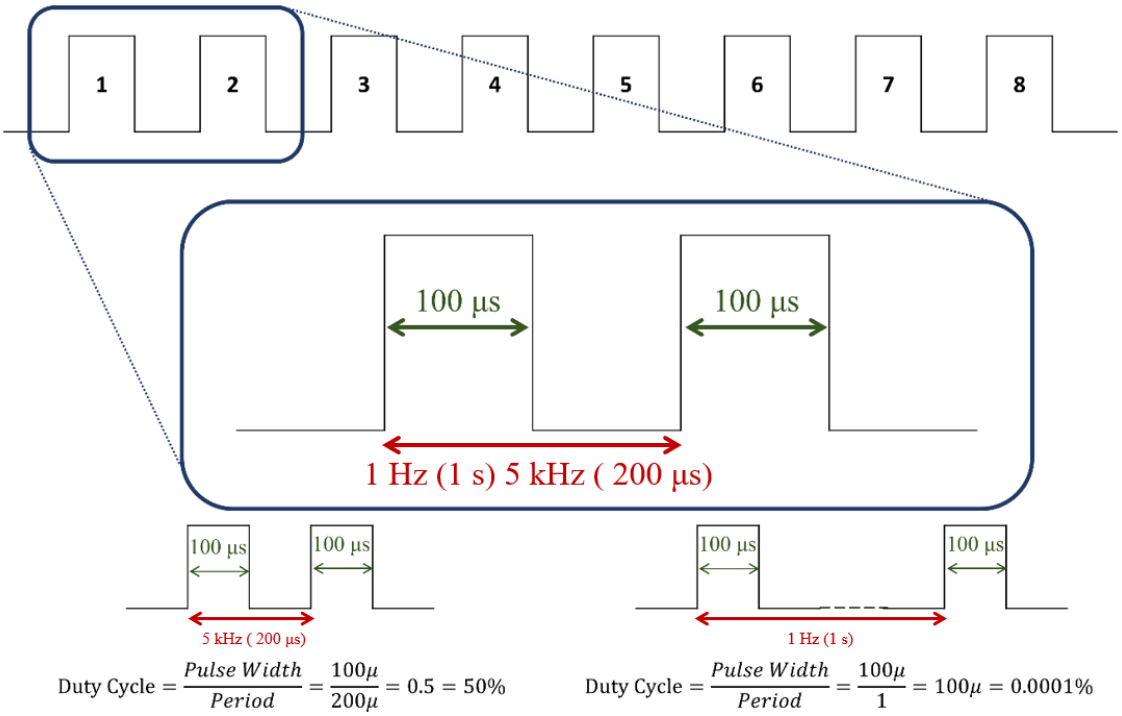


Fig. 2.5. Pulsed electric field parameters for reversable electroporation [4]

Electrochemotherapy

Reversible electroporation can enhance the efficiency of chemotherapy by opening the nanopores of cells to allow substances to locally enter the cells. This process is known Electrochemotherapy [3]-[5], [19]-[20]. Reversible electroporation is now used in ECT clinical procedures and has been approved by the National Institute for Health & Care Excellence (NICE) guidelines [21]-[26]. In practice, low-permeant chemotherapy drugs, such as bleomycin and cisplatin, are administered locally at the site of interest within the human body whilst the site is simultaneously stimulated with reversible electroporation where PEFs are delivered using specific electrode arrays. PEFs of the order of 100 µs duration and 1,000 V/cm amplitude are delivered through electrode arrays which can produce reversibly transient pores that are significant enough to allow normally impermeant molecules, such as bleomycin, to enter the exposed cells. The electric pulses must be applied to the whole tumour volume to ensure that all cells are electroporated and the chemotherapy drug of choice has entered all cells [3]-[4], [19]-[26].

The combined treatment of chemotherapy and reversible electroporation renders cancer stem cells more susceptible to chemotherapy treatment. ECT has been identified as a good evidence-based clinical practice for skin cancer (metastases in the skin and primary basal cell carcinoma) treatment by NICE [21]-[26] and has a European Standard Operating Procedures on Electrochemotherapy (ESOPE) [27].

Its use for deep-seated tumours, such as those in the liver and brain is currently under research. ECT application has been observed on breast, melanoma, liver, pancreatic, head and neck, and other deep-seeded tumours [3]-[4], [19]-[26].

Irreversible Electroporation

Irreversible electroporation (IRE) is the technique whereby electrical pulses are applied to cells causing permeant permeabilization of cellular membranes resulting in permanent cell death [3]-[4], [16], [28]. In recent years, the use of IRE for the treatment of a range of cancers has been intensively researched. It has been demonstrated that this technique produces well-defined borders as the electrical pulse either destroys the cells or leaves them intact without a thermal tissue response. IRE and other electro-pulsation techniques offer significant advantages over thermal ablation techniques. This is mainly due to their non-thermal tissue permeabilization response which enables the cancer cells to be destroyed without damaging the extracellular matrix that the cells 'sit' inside [3]-[4], [16], [28].

IRE is typically delivered by needle-shaped electrodes that are inserted into (or around) the tumour vicinity. Typically, 80 PEFs of 100 µs duration and 1,500 V/cm amplitude are delivered at a repetition frequency range from 1 to 10 kHz is delivered [3]-[4]. Some IRE treatments deliver the 80 pulses in a burst of eight to twenty 100 µs duration and 1,500 V/cm amplitude at a duty cycle of 50 % at a repetition frequency of 0.3 Hz to 10 Hz. These two methods of delivering IRE are demonstrated in Fig. 2.6.

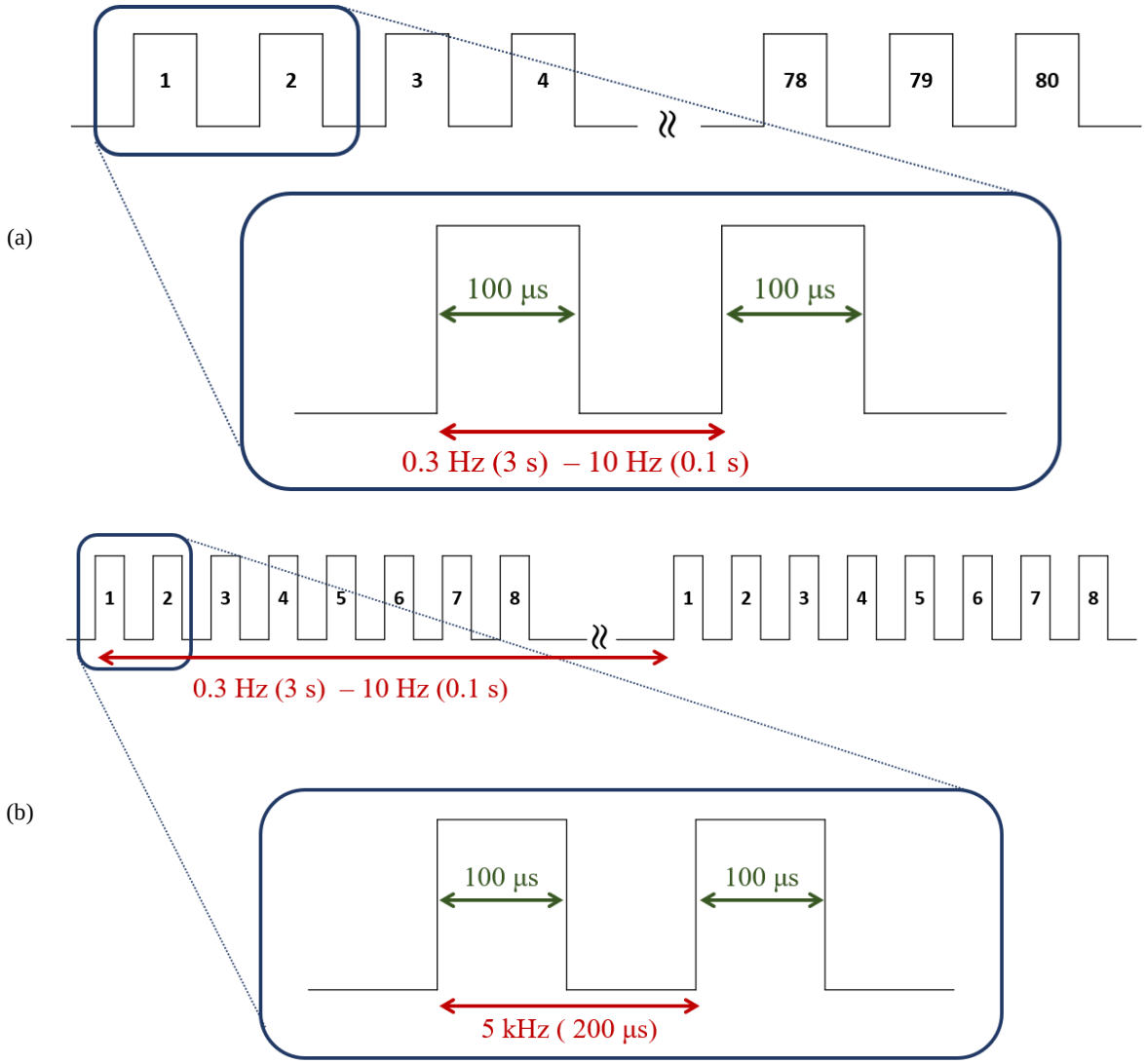
The NICE guidelines provide surgical armamentarium and clinical evidence-based information on IRE ablation of solid tumours in the liver, lungs, pancreas, prostate, and kidneys [29]-[44].

2.3.3. Clinical Evaluation of Electroporation

Classical electroporation in the form of reversible, irreversible, and ECT is accomplished using a high voltage generator capable of controlling PEFs electrical parameters. Electrical parameters such as voltage, current, pulse duration (10 µs to 100 ms), duty cycle, pulse train and burst repetition frequency and overall treatment time could be employed using a range of ablation probes (electrodes). PEFs of specific parameters can increase the permeability of the membrane of the cells, reversibly or irreversibly, which could allow chemicals, drugs, or DNA to be introduced into the cell [3]-[4]. Electroporation probes are placed into tumour tissues under imaging guidance and the procedure is normally undertaken under general anaesthesia as pulsed voltages cause substantial muscle contraction and cardiac arrhythmia due to the associated pulse length, intervals and amplitude of the 100 µs PEFs [3]-[4].

Electrochemotherapy is the only form of electroporation currently available on National Health Service (NHS) treatment as a possible treatment for non-melanoma skin cancer [43]. The procedure involves introducing chemotherapy into the tumour or sometimes directly into a vein (intravenously).

100 µs PEFs are then directed to the tumour using suitable electrodes. The pulses allow the drug(s) to enter the tumour cells more effectively and cause local destruction of the tumour [3]-[4].



$$\text{Duty Cycle} = \frac{Pulse\ Width}{Period} = \frac{100\mu}{200\mu} = 0.5 = 50\%$$

Fig. 2.6. Pulsed electric field parameters for (a) continuous 80 pulse (b) segmented (8 to 20 pulses at a time) methods of delivering irreversible electroporation [4]

Eight guidance and six NICE pathways currently support IRE [44] and five guidance and two NICE pathway documents support ECT [45]. A NICE review of the clinical literature on IRE in 2012 identified four case series studies, two case reports and data from an unpublished registry. In a series of patients with liver, [37], lung [41] and kidney [31] tumours, a complete response rate of 50% was seen when 45 procedures were completed. In this study, no tumour control response was seen in liver metastases less than 5 cm in dimension, and all patients with lower metastases had other lesions which advanced [36]. From their results, it may be stated that it is only a matter of time before classical electroporation will have a dominant presence in the clinical application within the NHS and globally.

There are currently multiple electroporation generators or electroporators available on the market and only one has United States Food and Drug Administration (FDA) approval. This system is the NanoKnife System [46]-[48]. Although systems produced by MIRAI Medicals are now also Conformitè Europëenne (CE) approved [49]-[51]. There are multiple electroporator companies, such as ThermoFisher, Bio-rad and BTX to name a few; that specialise in electroporators, applicators and accessories that are for *in-vitro* and *ex-vivo* application for research purposes only [52]-[54].

Veterinary application of classical electroporation, predominately electrochemotherapy, is now becoming common placed. Tumour treatment in veterinary application consists of the following steps: 1) general anaesthesia; 2) drug injection (cisplatin (1 mg/ml) or bleomycin (1,000 IU/ml)); 3) application of 80 PEFs, in trains of 8 pulses of 100 µs, with a 50 % duty cycle, every 2 ms, as illustrated in Fig. 2.7. These electroporators, applicators and accessories are marketed by companies such as RXVet Biotech and Leroy Biotech [52]-[54].

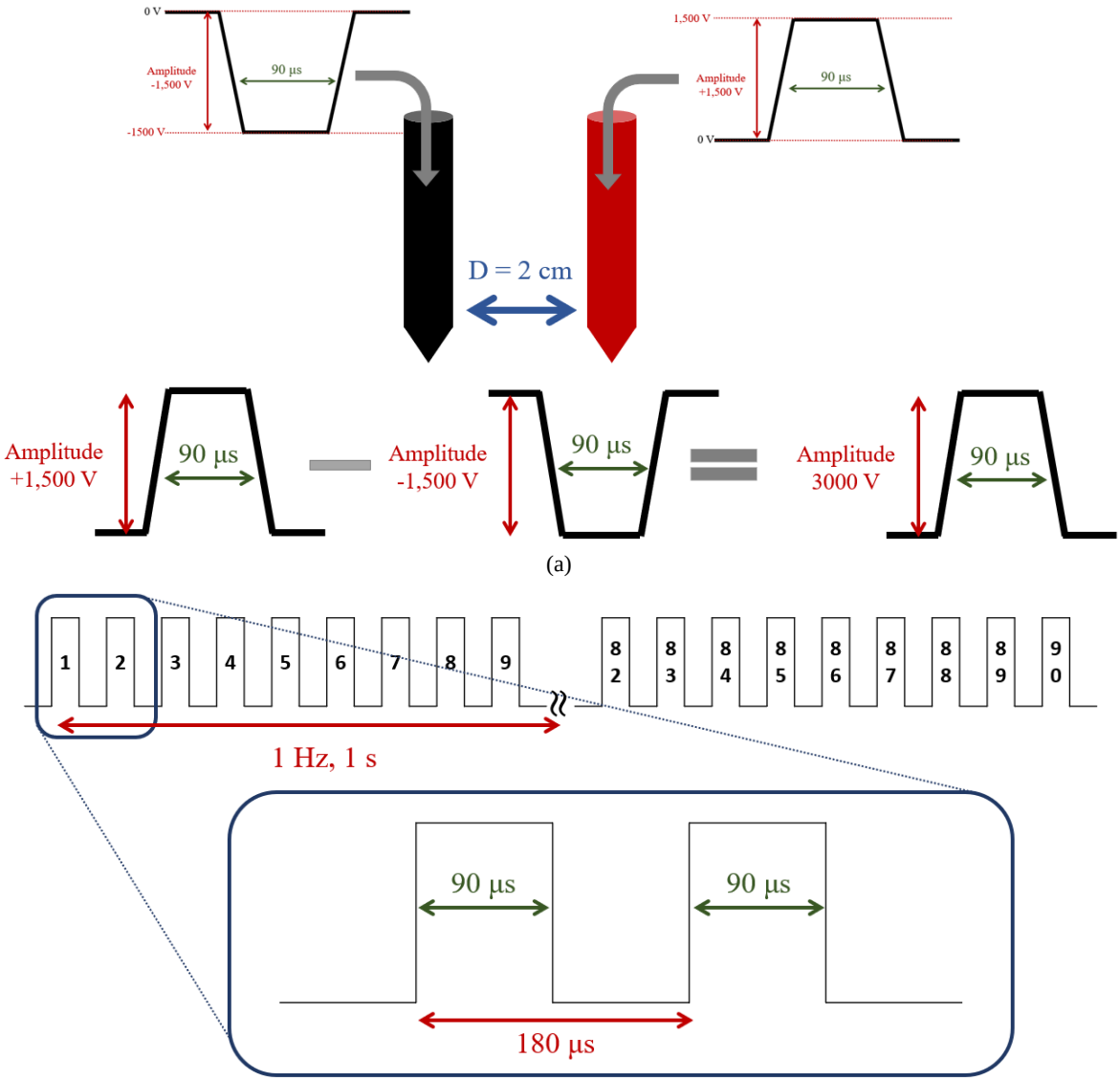
The NanoKnife, by angio dynamics, is an irreversible electroporation soft tissue ablation system to treat prostate cancer. This system is based on 100 µs pulses of electric fields in excess of 3,000 V/cm. NanoKnife therapy is a focal, image-assisted therapy. The clinical results are dependent on the electric field at the point the needle electrodes are located in the tissue [46]-[48].

The NanoKnife pulse application parameters are that one electrode has an electrical positive potential relative to the ground (patient body) and the other electrode a negative potential. The typical electrical potential applied is a 3,000 V (+1,500 V and -1,500 V per needle applicator as shown in Fig. 2.7(a)). 90 PEFs are delivered in a train of 9 pulses of 90 µs duration, of 1,500 V/cm (3,000 V across two electrodes 2 cm apart) with a duty cycle of 50 % and a pulse repetition frequency of 1 Hz between each train of 9 pulses. The PEFs delivered by the NanoKnife are shown in Fig. 2.7(b) [46]-[48].

It is claimed that the NanoKnife induces cell death (apoptosis) with no radiation damage, burning and scarring, which occurs with current standard procedures such as radiotherapy, chemotherapy, surgical resection, or thermal ablation therapies. This demonstrates the application of IRE, where irreversible pore formations are produced on cell's phospholipid membrane [46]-[48].

2.3.4. Nanosecond Electroporation

The predominant application of electroporation uses PEFs between 10 µs and 100 ms in duration. The application of microsecond pulses with low PEF amplitude (< 500V) has dominated the field of electroporation for decades. However, in recent years the number of systems focused on shorter, nsPEF has increased significantly, as shown in Fig. 2.8. This is made possible through the availability and technological developments in high frequency, high voltage semiconductor devices.



$$\text{Duty Cycle} = \frac{Pulse\ Width}{Period} = \frac{90\mu}{180\mu} = 0.5 = 50\%$$

(b)

Fig. 2.7 The NanoKnife (a) electrode arrangement (b) pulsed electric field parameters delivered [47]

The development of nsPEF electroporators and their biological effects are still in their early stage. nsPEFs is a further development of classical electroporation, where a PEF in the nanosecond regime (10 ns – 1 µs) is applied to cells and bulk tissues [3]-[4]. Literature suggests that nsPEFs have additional potential for cell manipulation and control of cell physiology. nsPEFs extend from traditional conventional electroporation permeabilization of cells to effects including calcium release, ion channels activation, and apoptosis induction [3]-[4]. Mechanisms that induce nsPEFs tumour damage and cell death are still not completely understood. While *in-vitro* data for nsPEF induced DNA damage is convincing, evidence for direct DNA damage *in-vivo* is less persuasive [3]-[4].

With the high frequencies associated with the fast nanosecond rise and fall times of the nsPEFs with a higher electric field (kV/mm), the PEFs penetrate deeper into the cell physiology interior and

electroporate the internal membrane and organelles of a cell in addition to the outer plasma membrane, as introduced by conventional electroporation [3]-[4].

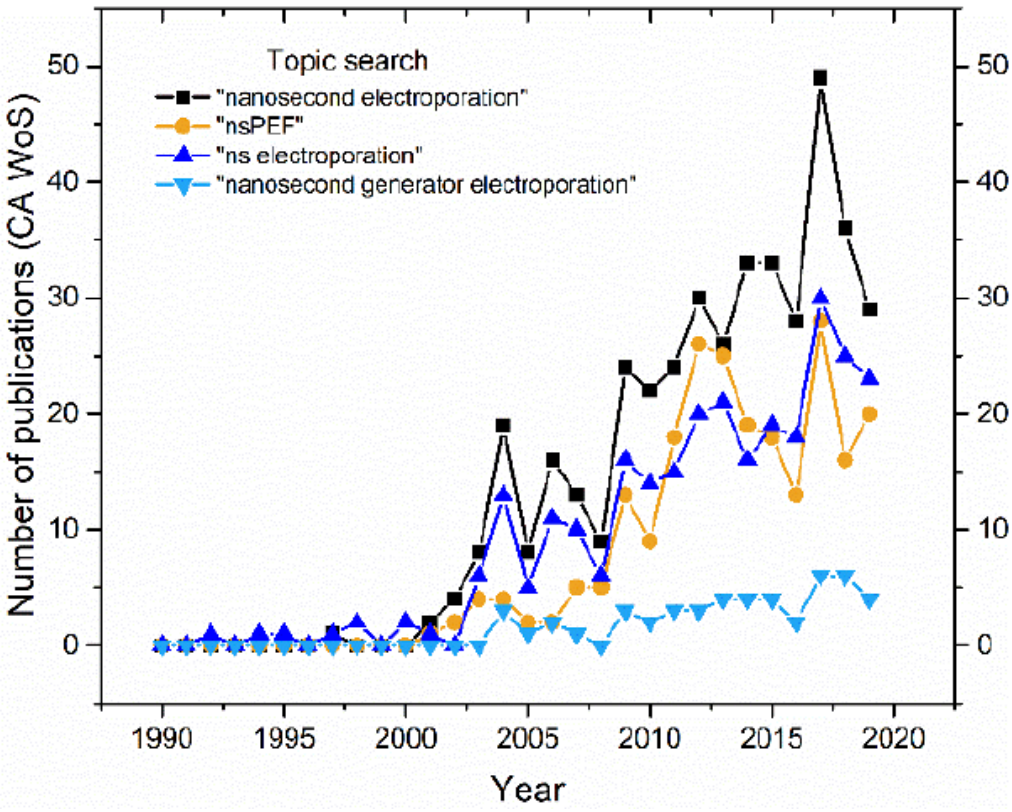


Fig. 2.8. The trends in the number of publications on the topics of nanosecond electroporation / electroporators according to Clarivate Analytics Web of Science [55].

Ablation of cancerous tissue using nsPEF has been demonstrated. In some cases, this technique resulted in complete tumour remission [56]-[60]. This indicates a clear clinical potential for nsPEF in providing effective local cancer treatment. The literature search suggests a representative paradigm shift from chemistry-based medicine and treatment to a physics-based treatment using pulsed energy technology.

The literature recommends that with shorter PEF e.g., nsPEFs, a higher pulse amplitude or electric field strength is required. Initial *in-vitro* evaluation of nsPEFs indicates that good result is obtained with 400 to 2,700 pulses with pulse durations between 100 and 300 ns and electric field strengths of between 30 and 65 kV/cm, depending on the tumour model and electrode design [3]-[4]. Energy transfer into cells and tissues from the application of nsPEFs is relatively low due to their associated short pulse duration and long duration, or repetition frequency between the burst of pulses. These pulse profiles produce a non-thermal ablation and a non-scarring effect on the skin due to the high intensity of the short duration and the longer tissue recovery time (pulse repetition frequency) of the joule heating effects of the PEFs [3]-[4]. Because of the higher voltage amplitude associated with nsPEFs, care must be taken to prevent breakdown / arcing and skin burning when nsPEF are applied *in-vivo*.

Microbiologists are intrigued by the potential of nsPEFs for the treatment of cancer stem cells. Eliminating tumours by regulated cell death mechanisms, including apoptosis [58]-[60] using nsPEFs has been shown to induce a vaccine-like effect in mice and rats [3]-[4]. Other evidence also suggests nsPEFs induce immune responses [3]-[4]. During tumour-regulated cell death, dying cells activate immune mechanisms that can prevent cancer recurrence and may provide protection from recurrent disease and perhaps metastatic, systemic disease [3]-[4].

Recent data suggest that nsPEF treatment stimulates the immune system, thus producing an immunogenic cell death, in addition to ablating primary tumours in a non-thermal capacity. But this has yet to be proven, and ongoing work is being carried out. The activation of the immune system by nsPEF cancer treatment suggests that immune system activation prevents tumour regrowth when a second cancer cell injection was conducted in xenograft in *in-vivo* models, but this has not yet been completely proven and requires additional studies for validation [3]-[4].

Consequently, nsPEF treatment may become a viable approach to immunotherapy that does not involve the delivery of DNA or virus, checkpoint inhibitors, engineered patient immune cells, or molecules of any kind [3]-[4].

It has already been demonstrated that nsPEFs can be used to treat local cancers such as melanoma, basal cell carcinoma, hepatocellular carcinoma, pancreatic and breast cancer in mice and rats, and basal cell carcinoma in humans. This therapy is drug-free and non-thermal and therefore has advantages over other tumour ablation therapies and conventional cancer treatments [3]-[4].

nsPEFs penetrate the interior of cells and trigger the cell's apoptosis pathway to initiate programmed cell death, unlike reversible and irreversible electroporation. It has been theorized that this occurs due to the high frequencies associated with shorter faster pulses associated with PEFs [3]-[4].

The associated frequency spectrum (or Fast Fourier Transform (FFT)) associated with the nsPEFs is higher than the microsecond pulsed electric fields (µsPEFs) or classical electroporation signals. The FFT response of nsPEF encroaches on microwave frequencies because of the nanosecond (ns) to picoseconds (ps) transition times associated with nsPEF. For a nsPEF with a rise and fall time of 1 ns the associated frequency is 350 MHz. This can be calculated by equation (2.2) [61].

$$Bandwidth, BW = \frac{0.35}{rise\ time} = \frac{0.35}{t_r} \tag{2.2}$$

In such a situation, it can be expected that at high frequencies, associated with nsPEF, the creation of nanopores on the subcellular membranes is more likely to be observed than plasma membrane poration. In the time domain, the associated high frequency of nsPEF corresponds to a Fourier spectrum that extends into the high (critical) frequency ranges to permeate membranes of cellular organelles

before pores are observed on the plasma membrane. This has been confirmed in literature through modelling in the time domain [4], [62].

Since nsPEF time domain signals are shorter than the ion redistribution time of cancerous cells the electric field extends through the cell before the cell's ions have time to redistribute. The time and frequency domain content associated with nsPEFs have greater interactions with intracellular structures and provoke additional manipulation and control of cell physiology and induced apoptosis [3]-[4].

Pores generated by nsPEF on the membrane are nanometres (nm) in diameter. These small pores, or openings, will allow water and ions to pass through them but not proteins or DNA. A great deal is known about cell signalling pathways and most involve changes in intracellular calcium levels. Small increases in the local calcium (Ca_2^+) concentrations have been demonstrated to have very strong effects on a variety of cellular functions, such as secretion, cell division, and apoptosis. These observations suggest that nsPEF signalling components lead to key signalling ions, such as calcium, Ca_2^+, that can pass through these nanopores to trigger cellular responses [3]-[4].

As far as we are aware, there are currently no nsPEF electroporators that are utilized on the regular basis in the clinical environment. The majority of nsPEF electroporators are bespoke 'in-house' nsPEF generators built for the application of nsPEF research.

Nanosecond Electroporators

Commercial electroporators have a limited range of pulse parameters that can be set up by researchers as they are purposely used for particular EP applications. In comparison to conventional electroporators, the selection of commercially available high voltage nsPEF electroporators is significantly lower and these systems are for research applications only and no systems are available for clinical use (during the time of write-up). This is also the case regarding available guidelines and recommended applications for nsPEF or nanosecond electroporation i.e., NICE or FDA guidelines for medical research and clinical application [63]-[64].

nsEP is a growing scientific research field and an electroporator that enables a wide range of parameters to be selected by the research is desired to fully investigate the possible applications and clinical effects using nanosecond pulsed electric fields with variable amplitude, duration and shape have on biological cells and bulk tissues. To address the growing scientific demand for nsPEF research, and the lack of commercially available nsPEF electroporators, developing in-house electroporators that can produce nsPEFs with a wide range of PEF parameters could easily be articulated as being beneficial to the PEF research community [11].

Table 2.1 indicates that pulse amplitudes range from mV to several kV and duration from ns ms is desirable for PEF or electroporation research. It would be very difficult to implement an electroporator that can generate such a wide spectre of PEF parameters, within a single generator.

Before designing an electroporation system, it is beneficial to know for what application the electroporator will be used. For example, gene electrotransfer and cell electrofusion require auxiliary signals, multi-needle electrodes require an electrode commutator, organelles require very short pulses and clinical applications that are compliant with clinical safety standards (ISO-14971). Electroporation of single cell or planar lipid bilayer requires low voltage electroporation pulses, whilst *in-vitro* and *in-vivo* applications require high voltage pulses, and organelles such as bacteria and yeasts require even higher voltages. [3]-[4], [11]. A range of pulse parameters associated with known electroporation applications is seen in Table 2.1 bellow:

Table 2.1. Pulsed electric field parameters for specific electroporation applications [11]

Application	***Amplitude***	***Duration***	***Auxiliary Pulses***
Electrochemotherapy	~ kV	µs, 8 x 100 µs	-
Gene Electro-transfer	~ kV	µs – ms	Electrophoretic pulses <500 V, > ms
Electro-insertion	< kV	ms – s	-
Transdermal drug delivery	< kV	ms	-
Electrofusion	~ kV	µs	Dielectrophoretic pulses < 200 V, > s, ~MHz
Pasteurization	>> kV	µs	-
Tissue Ablation	> kV	µs – ms	-
Single cell electroporation	> mV	µs	-
Organelle electroporation	>> kV	ns	-
PEF / Electroporation research	mV - kV	ns – ms	-

The ability to generate pulses with variable parameters is a requirement from microbiologists and clinicians as this enables detailed studies of dose-effect relations to be investigated. It also allows the capability to optimise PEF parameters to maximize the desired biological effects from PEFs exposure.

2.4. Technology as a Key Enabler

The potential applications for nsPEFs exceed micro and millisecond PEFs due to the possibility of inducing apoptosis whilst stimulating the immune response. This could offer a viable contemporary cancer treatment with less to no side-effect in comparison to other standard treatment solutions [3]-[5], [11]. For nsPEFs to be clinically evaluated and viable, the method of generating the nsPEFs must offer controls in terms of being able to easily control the pulse parameters (pulse duration, number of pulses in one burst, duty cycle of burst pulses, repetition frequency, ‘OFF’ times between bursts and amplitude) [3]-[5], [11].

The development of nsPEF electroporation systems with nano- and picosecond transition times requires different designs and technologies from micro- and millisecond PEFs generation. The design implemented is highly dependent on the switching technology transition times (rise time or turn ‘ON’ and fall time or turn ‘OFF’ times). Micro- and millisecond PEF electroporation systems are typically

generated through capacitor discharge for exponential decay PEF, whilst square waves are generated by standard Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) or Bipolar Junction Transistor (BJT) -based switching technologies. Advances in semiconductor material and development in pulsed power technology are the key enabler for the possibility of developing a slow and fast nsPEF electroporation system [5], [11], [14].

Semiconductor pulsed power technology has been used for decades in high-powered applications such as switches mode power supplies and military Radio Detection And Ranging (RADAR) before their use in clinical applications. The development of nsPEF electroporators and their clinical applications is in its infant stage. A versatile nsPEF electroporator capable of producing PEF of variable parameters would be a useful tool for biologists and clinicians alike, as it allows detailed studies of nsPEF dose-effect relations. This would allow the determination of the optimum PEF parameters to achieve desired biological and clinical effects, such as apoptosis, cell regeneration and/or sterilisation, to name a few. Therefore, a technology that would enable and can provide a wide variety of pulse shapes and other parameters, such as amplitude, pulse duration and repetition frequency, in the region of the nanosecond's regime would be useful.

2.4.1. The Ideal Switch

The ideal switch is a device that produces no power loss when switching a current through a load and can change its state ('ON' or 'OFF') instantaneously.

This definition requires the switch to have no voltage drop across its terminals when in the closed position and cuts off all current flow through the load in the open position. The repetitive cycling speed between the switch's position must be infinite, with a zero-time delay between switching from one state to the next ('ON' to 'OFF', and vice versa). This is the characteristics for an ideal switch [14], [65]-[66].

This perfect switch does not exist. Mechanical switches and solenoid relay switches closely meet the open and closed switch criteria of the ideal switch but cannot hope to meet the ideal switching-speed criteria. The concept of square wave generation PEFs consists of a high voltage power supply (V_{CC}) constantly charging a high voltage capacitor (C) and the power switch (S) is capable of fast switching between the 'OFF' to 'ON' and 'ON' to 'OFF' states Fig. 2.9 [65]-[66].

Recent advances in the fields of advanced integrated circuits, material science and semiconductor device fabrication technology have made it possible to generate nsPEFs with pulse amplitudes in excess of 1 kV.

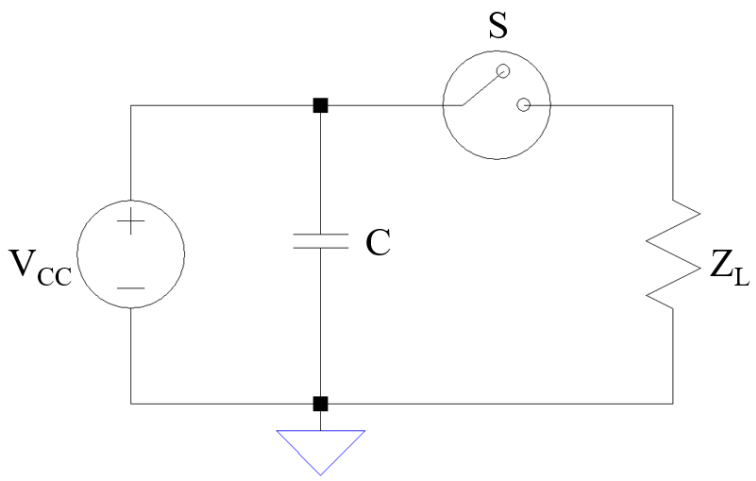


Fig. 2.9. Illustration of an ideal switch (S) for the generation of a high voltage pulse across a load (Z_L) [66].

2.4.2. Pulse Electric Field Requirements

The main requirement of the slow and fast nsPEF electroporation system is to generate pulsed electric field of the following parameters:

- Produce reliable and repeatable symmetrical pulse waveform;
- Produce a pulsed electric field with amplitude in excess of 500 V;
- Produce a symmetrical pulsed electric fields waveform with identical rise-time (t_r) and fall-times (t_f);
- Produces a wide range of PEF duration (pulse width) within the nanosecond regime between 10 ns and 300 ns;
- Adjustable PEF repetition frequency between 1 Hz and 50 Hz;
- Capable of generating a specific number of nsPEF;

2.4.3. Technology as a Key Enabler Overview

Appendices I and II describes the diverse technologies available for the generation of high voltage pulse circuits (Appendix I) and fast switching elements (Appendix II) for the development of electroporation systems. Based on the requirement for the nsPEFs to be generated by the slow and fast nsPEF electroporation, the variously identified switching topologies can be divided into three main groups: capacitor discharge, semiconductor technology and inductive storage discharge. Each group and associated technology are shown in Fig. 2.10. The advantages and disadvantages of each technology are summarized in Table 2.2. Each technology reported here can produce high voltage PEFs with pulse durations in the sub-microsecond range [11], [14], [65]-[71].

Traditionally, transmission line topologies, including Blumlein-type and pulse forming circuits were the dominant technology for the generation of nsPEFs for electroporation applications. The advances in semiconductor technologies BJT, MOSFETs, insulated-gate bipolar junction transistors

(IGBJTs) etc.) and materials (i.e., Silicon Carbide (SiC) and Gallium Nitride (GaN) in recent years have enabled the development of high voltage, fast pulse generators that can produce sub-microsecond pulsed fields with nanosecond or even picosecond transition times [65], [68]. If the development of power semiconductor technology, such as GaN and SiC, continues at the pace it is growing today, then it will be possible to produce pulse amplitudes of 2 kV with picosecond rise and fall times soon [65], [68].

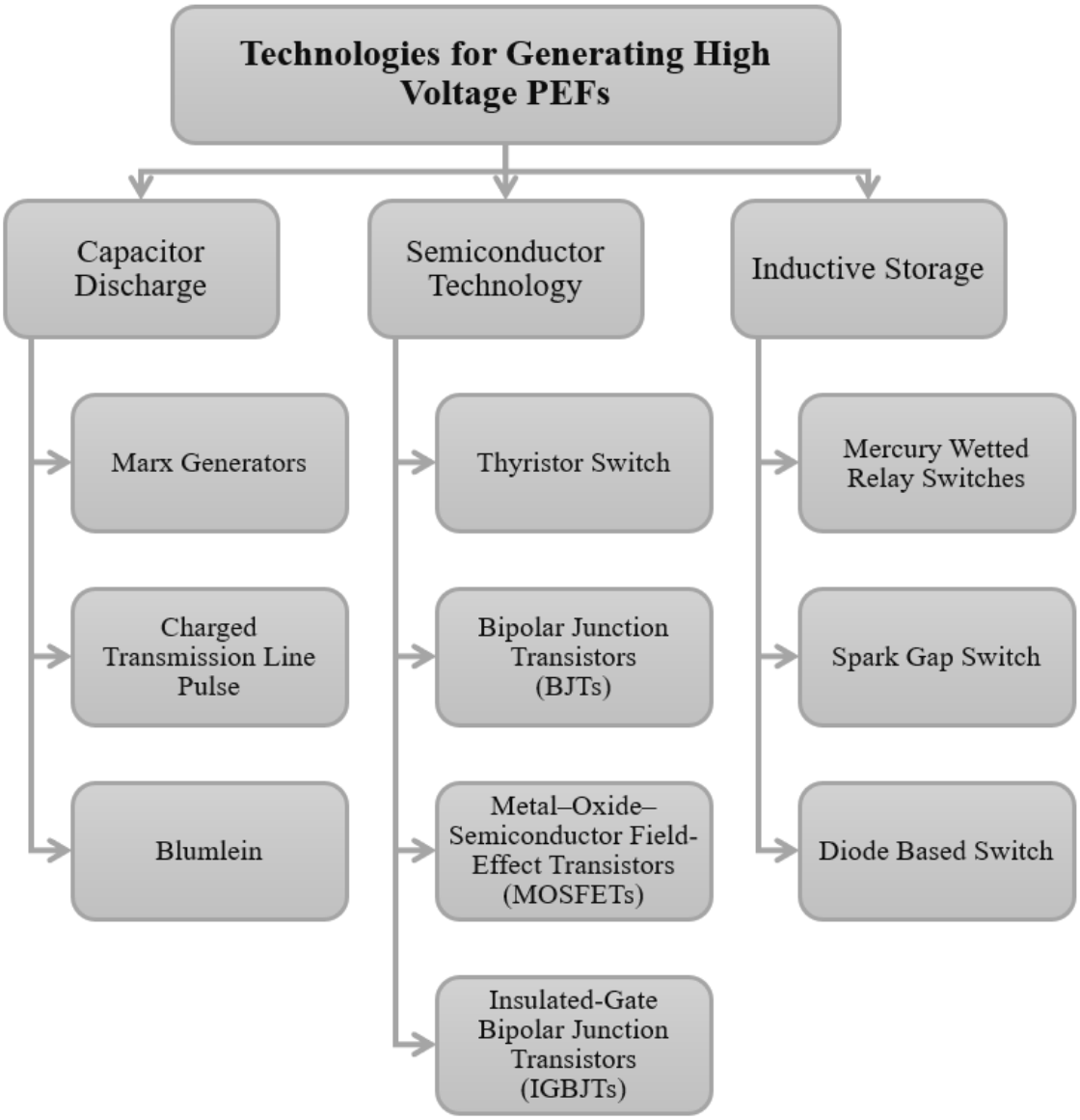


Fig. 2.10. Identified technologies available for the generation of high voltage pulsed electric fields

Table 2.2. Key features and limitations of the identified technologies available for the generation of high voltage sub-microsecond duration pulsed electric fields (Appendix I and II) [11], [14], [65]-[71].

Topology		***Key Features (Advantage)***	***Limitations (Disadvantage)***
Capacitor Discharge	Marx Generators	➢ Can handle high voltages and current, as high as 50 kV to 100 kV, and up to 40 A. The handling capability is dependent on the number of Marx stages implemented; ➢ Low voltage drops across switches as the voltage drop and power are dissipated evenly across each stage. Providing power and load isolation; ➢ Capable of generating short pulses of sub-100 ns duration. The exact nsPEF duration and transition times are determined by the switching element implemented; ➢ Can be adapted for the generation of bipolar pulses using half or full-bridge topology;	➢ Voltage droop is common when high impedance loads are used; ➢ Commonly used for low pulse repetition frequency operation. As the repletion rate is limited to the charging time of the capacitors at each stage of the Marx configuration; ➢ Has a relatively short lifetime. The performance reliability and repeatability of design are dependent on the switching technology implemented i.e., electrode degradation in case of spark gaps. ➢ Commonly used for the generation of capacitance discharge PEF waveform; ➢ Large bulky structure;
	Charged Transmission Lines	➢ High voltage handling capability of 1 kV and above. The voltage and current handling capability are dependent on the breakdown voltage of the switching element implemented and the coaxial transmission line used; ➢ Commonly used to generate a short pulse in the sub-100 ns range; ➢ Simplistic design that consists of two main comments of a transmission line and a switching element; ➢ Can be adapted for the generation of bipolar pulses;	➢ Load impedance matching requirement between the load and characteristic impedance of the charged line. This relationship determines the pulse shape (associated reflection coefficient) and pulse amplitude (voltage divider effect); ➢ Pulse width inflexibility. The pulse width is limited to the associated electrical length or delay time of the transmission line; ➢ Commonly used for low pulse repetition frequency operation between 1 Hz and 50 Hz. The repetition frequency is limited by the time it takes for the charged line to be charged through the high impedance resistor, R_C; ➢ The rise time of the PEF is dependent on the switching element utilised; ➢ The switching elements used with the charged line have a relatively short lifetime;

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Table 2.2. Key features and limitations of the identified technologies available for the generation of high voltage sub-microsecond duration pulsed electric fields (Appendix I and II) [11], [14], [65]-[71].

Topology		***Key Features (Advantage)***	***Limitations (Disadvantage)***
Capacitor Discharge	Blumlein	➢ High voltage handling capability of 1 kV and above. The voltage and current handling capability are dependent on the breakdown voltage of the switching element implemented and the coaxial transmission line used; ➢ Commonly used to generate a short pulse in the sub-100 ns range; ➢ Simplistic design that consists of three main components of two separate identical transmission lines and a switching element; ➢ Can be adapted for the generation of bipolar pulses;	➢ Load impedance matching requirement between the load and characteristic impedance of the charged line. This relationship determines the pulse shape (associated reflection coefficient) and pulse amplitude (voltage divider effect); ➢ Pulse width inflexibility. The pulse width is limited to the associated electrical length or delay time of the transmission line; ➢ Commonly used for low pulse repetition frequency operation between 1 Hz and 50 Hz. The repetition frequency is limited by the time it takes for the charged line to be charged through the high impedance resistor (R_C); ➢ The rise time of the PEF is dependent on the switching element utilised; ➢ The switching elements used with the charged line have a relatively short lifetime;
Semiconductor Technology	Thyristors	➢ Capable of handling high voltages and current of up to 20 kV and 1 kA respectively; ➢ Can produce symmetrical PEFs with identical rise and fall times. Depending on the overall external circuitry implemented with a thyristor; ➢ Can produce produces a wide range of PEFs durations. Depending on the overall external circuitry implemented with a thyristor;	➢ Complexity in the external circuitry surrounding the thyristor for the generation of symmetrical PEFs of various pulse durations; ➢ The repetition frequency of the pulses generated is limited due to the delay time between the trigger signal and the output nsPEF;
	Bipolar Junction Transistors	➢ Can handle semi-high voltage between 200 V to 500 V; ➢ Can produce reliable and repeatable symmetrical pulses; ➢ Have a fast transition time (rise and fall times) of 300 ps (Avalanche mode); ➢ Can be used as a switching element for other nsPEF generation topology such as transmission line, Blumlein or Marx (300 ps rise time in Avalanche mode);	➢ Complex external circuitry; ➢ Complex driving circuit for the operation of an avalanche mode transistor circuit; ➢ Have a slow transition time (rise and fall times) of 500 ns (in Saturation and Current mode);

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Table 2.2. Key features and limitations of the identified technologies available for the generation of high voltage sub-microsecond duration pulsed electric fields (Appendix I and II) [11], [14], [65]-[71].

Topology		***Key Features (Advantage)***	***Limitations (Disadvantage)***
Semiconductor Technology	Insulated-Gate Bipolar Junction Transistors	➢ Can handle high voltage and current of up to 4500 V and 250 A respectively; ➢ Ability to generate well-defined pulses of wide parameters such as pulse duration, and repetition frequency, quickly and flexibly by adjusting the gate drive signal; ➢ Produces reliable and repeatable symmetrical pulse waveform: ➢ Can be adapted for the generation of bipolar pulses;	➢ Commonly used for the generation of a pulse of 150 ns duration and above; ➢ Have relativity slow transition times (rise and fall times) in comparison to other semiconductor switching devices with rise times of 50 ns +; ➢ Complexity in external circuitry surrounding the IGBJT;
	Metal-Oxide-Semiconductor Field-Effect Transistors	➢ Can handle high voltage and current of up to 1700 V and 5+ A respectively; ➢ Ability to generate well-defined pulses of wide parameters such as pulse duration, repetition frequency, and bipolar or monopolar pulses quickly and flexibly by adjusting the gate drive signal; ➢ Reliable and repeatable operation with high life cycles that are determined by the MOSFET circuit topology and gate driver current capacity; ➢ Has a low 'ON' state resistance ($R_{DS(on)}$) as low as 0.05 Ω;	➢ Must consider the switching sequence of the MOSFET and its repetition frequency limitations; ➢ Fast transition times with recorded rise and fall times as fast as 35 ns; ➢ Commonly used for the generation of short pulse generation in the 100 ns + pulse widths regime; ➢ Associated complexity in external circuitry surrounding the MOSFET; ➢ Broadband load sensitivity because of a positive temperature coefficient;
Inductive Storage	Diode Opening Switch	➢ Capable of producing PEF of several kV amplitudes, 1kV to 140kV, with current up to several amps, 15A to 16kA; ➢ The components are easily accessible; ➢ Are commonly used for the generation of short pulse generation in the sub-100 ns regime; ➢ Can produce consistent PEF across variable load impedance;	➢ A complicated design that requires switching synchronization, a complex control system and switching topology; ➢ Limited control of pulse durations; ➢ Produces asymmetrical pulses as the rise time is short, whilst the fall time is dependent on the discharge timing of the CL oscillator;

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Table 2.2. Key features and limitations of the identified technologies available for the generation of high voltage sub-microsecond duration pulsed electric fields (Appendix I and II) [11], [14], [65]-[71].

Topology		***Key Features (Advantage)***	***Limitations (Disadvantage)***
Inductive Storage	Spark Gap	➢ High voltage and current handling capability of up to 30 kV and 100 A respectively; ➢ Produce PEFs with sub-nanoseconds rise and fall times;	➢ Inflexibility regarding dynamic adjusting of PEF duration. This feature is limited by the reliant on the transmission line architecture implemented; ➢ Spark gaps have a relatively short lifetime due to electrode degradation; ➢ Has an unpredictable and unrepeatable characteristic in producing an identical chain of PEFs. Its inability to produce repeatable symmetrical pulse waveforms is due to the unpredictability of the arching aspects of the switch. ➢ Commonly used for low pulse repetition frequency operation of 1 Hz to 50 Hz;
	Mercury Wetted Relay	➢ Fast transition times (rise and fall times) of 0.1 to 0.5 ns can be achieved; ➢ Can be used to generate positive and negative PEF polarities; ➢ Can be used to produce reliable and repeatable symmetrical pulse waveforms; ➢ Produces a wide range of PEF duration within the nanosecond time regime;	➢ Commonly used for low pulse repetition frequency operation between 50 Hz and 500 Hz; ➢ Hard to control and trigger PEFs generation with external trigger signal; ➢ If sealed glass envelope fractures or becomes damaged can cause toxic effects to user from exposure to mercury;

The development of ultra-fast semiconductor switches can generate short pulsed electric fields as fast as 100 ns. Traditional topologies such as transmission lines and pulse forming circuits are commonly used for short pulse generation of pulse widths under 100 ns, with transition times of 5 ns or less. The main advantages of semiconductor technology over traditional topologies are their compact size, flexibility and control of generating PEFs [65], [68]. Flexibility includes the ease of changing the nsPEF parameters, such as the duration, repetition frequency and the number of pulses in a reliable and repeatable manner. In comparison, capacitor-discharge topologies are inflexible due to their reliance on transmission line length and resulting Gaussian pulse shape [65], [68].

For high voltage nsPEFs delivery the switch performance is crucial. The spark gap switches are fast and cost-effective for nsPEF generation, but these switches have a short lifetime due to electrode erosion, and poor pulse duration control and can be frequently associated with turn-on jitter.

In contrast, the semiconductor switches offer a high flexibility of pulse control but are more constrained by high voltage or current withstand limits as well as switch opening and closing times. Connecting such switches in series can overcome the high voltage limitation issues, but this solution increases stray inductance within the circuit which could be a limiting factor regarding the overall switching speed [65], [68].

From the comparison of MOSFETs, IGBJTs and BJTs based switches, all three can offer a breakdown voltage higher than 500 V. However, the BJT switches, are the most cost-effective option, but are slower than both MOSFETs or IGBJTs, and cannot fulfil the nsPEF pulse forming requirements. It is suggested that high-power MOSFETs can be used to generate pulses within the 100 ns to 300 ns PEF range with transition times (rise and fall time) faster than 50 ns [65], [68].

Butkus *et. al* (2020) journal focuses on nsPEF pulse generators and indicates the shift in technology in-house developed electroporation systems' tendency to utilize MOSFET and semiconductor technologies [13]. The increase in the number of developed electroporation systems is due to the lack of commercially available nsPEF electroporation systems [14].

All topologies considered in this work offer a solution to produce high voltage PEFs. However, transmission line-based topologies in conjunction with inductive storage switches (spark gap, diode switches etc.) demonstrate the possibility to produce nsPEFs with a very high amplitude greater than 10 kV with sub-nanosecond transition times. The design of the electroporation system based on these topologies is more complex than solid-state semiconductor switches in regard to the variety of nsPEF parameters that can be generated [11], [13]. Furthermore, for clinical applications, the voltage amplitude would normally be limited to around 1.5 kV to 2 kV maximum due to the breakdown voltage of microwave cable used for non-invasive surgery and associated international standards for medical devices (ISO 13485).

2.5. Conclusion

In recent years the number of systems and research focused on high voltage (>500 V) nsPEFs has increased significantly. Literature suggests that there are currently no nsPEF electroporators that are available for use in a clinical environment. There is a growing need in the scientific and clinical research communities for nsPEF electroporation systems that are capable of producing a wide range of PEFs to quantify and validate the effect of nsPEF on cellular and tissue loads.

Various technologies for the generation of nsPEFs exist and have been reviewed in this chapter. Traditionally transmission line-based topologies can be utilised for the generation of sub-100 ns PEFs. But recent developments in SiC and GaN technologies have resulted in the capability of MOSFETs technology to produce PEFs of 100 ns in duration and various pulse parameters in a flexible manner.

Two 'in-house' nsPEF electroporation systems to obtain preliminary microbiological and pre-clinical effects from the application of nsPEF have been developed in this work. Firstly, a slow nsPEF electroporation system to produce 100 ns to 300 ns PEF with amplitudes in excess of 1 kV utilising power MOSFETs. Secondly, a fast nsPEF electroporation system that combines the traditional method of charged transmission line topology with avalanche transistors for the generation of 10 ns to 100 ns PEF, with sub-nanosecond transition times and amplitudes in excess of 1 kV.

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CHAPTER III. SLOW NSPEF ELECTROPORATION SYSTEM – TECHNICAL DESIGN

3.1. Introduction

This chapter describes the design, development, and evaluation of the slow nanosecond pulsed electric field electroporation system. This system has been evaluated by microbiologists at the Italian National Agency for new technologies, energy and sustainable economic development (ENEA) for preliminary *in-vitro* investigation of nanosecond pulsed electric fields (nsPEFs) effects on Medulloblastoma cell lines. The cell lines were enriched in Cancer Stem Cells (CSCs). This work was a key part of a multidiscipline collaboration supported by the European Union's Horizon 2020 Framework. The particular programme was called the Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells (SUMCASTEC) [1].

This slow nsPEF electroporation system was developed to investigate the effect of nsPEFs, of 100 ns, 200 ns, and 300 ns pulsed electric fields (PEFs), with amplitudes in excess of 1 kV (or electric field strength in excess of 1 kV/mm (1 MV/m)), on Medulloblastoma cell lines that are enriched in CSCs.

Following discussions with microbiologists and clinical researchers, as part of the SUMCASTEC research program, it was highlighted that there is an absence of commercially available nanosecond electroporation systems to investigate the effects of nsPEFs on cancerous bulk tissue and cell lines [2].

The agreed set of requirements for the slow nsPEF electroporation system from the SUMCASTEC consortium was as follows [2]. To deliver a specific number of PEFs of 100 ns to 300 ns in duration, with amplitude in excess of 1 kV across a 50 Ω load impedance with repetition frequencies between 1 Hz and 50 Hz.

The slow nsPEF electroporation system developed in this work utilised fast switching, power metal-oxide-semiconductor field-effect transistors (MOSFETs) connected in a push-pull configuration to produce nsPEFs that meet the above requirements. The push-pull configured MOSFETs were driven by a high current gate driving optocouplers, and the timing and amplitude control of the nsPEFs was managed by a suitable microcontroller. This resulted in the following publications [3]-[7].

3.2. MOSFET Switching Topology

In the second chapter a wide range of technologies that are capable of generating nsPEFs were described. Various topologies for producing nsPEFs were investigated, followed by a comparative study of the possible switching technologies and circuits that could be implemented to produce the nsPEFs that meet the slow nsPEF electroporation system requirements.

3.2.1. Introduction to MOSFETs

MOSFETs technology was identified as a suitable switching technology that is capable of producing the required nsPEF parameters. This technology had been identified as appropriate for producing nanosecond pulses of variable duration, and amplitudes up to, and above 1 kV. The benefits and challenges of using MOSFET technology are highlighted in Table 3.1. bellow.

Table 3.1. The benefit and challenges of power metal-oxide-semiconductor field-effect transistors [8]-[14]

Benefits	***Challenges***
➢ Low ON-resistance ($R_{DS(on)}$);	➢ Packaging challenges to minimise parasitic inductance and temperature;
➢ Small chip size and stray inductance;	➢ Integration of gate driver with high pulsed current rating;
➢ Low capacitances (C_{iss}, C_{gs}, C_{gd});	➢ High heat flux;
➢ Fast switching speeds;	
➢ High operating temperatures;	
➢ High power / voltage capabilities;	

MOSFETs are voltage-controlled current switches that combine the high input impedance of a thyristor with the low power requirement of a semiconductor device. A MOSFET is a majority carrier device that has no difficulty in storing charges in its minority carrier region. Therefore, these devices can be turned ‘ON’ and ‘OFF’ very quickly [8]-[12].

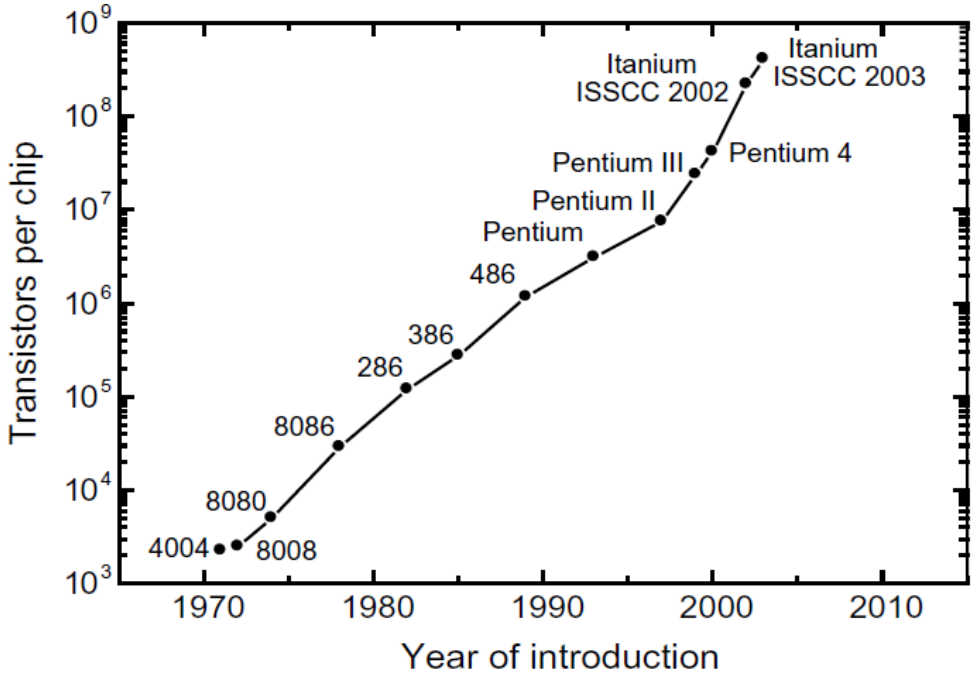
Power MOSFETs are suitable devices for electroporation applications as they provide fast switching speeds and large current and voltage handling capability. Therefore, the generation of nsPEFs with high repetition frequencies can be achieved. Power Gallium Nitride (GaN) transistors and Silicon Carbide (SiC) MOSFETs are now affordably available commercially [12]-[14].

Power MOSFETs are available with high breakdown voltage ratings in excess of 1700 V, and drain current ratings in excess of 70 A, with transition times (rise and fall times) and delay times of less than 40 ns. These features make MOSFETs an attractive option for switching high voltages for the generation of PEFs between 100 ns and 300 ns. Examples of commercially available power MOSFETs are produced by manufacturers such as Wolfspeed [15], Infineon [16] and ON Semi [17]. The n-channel enhancement type MOSFET device was considered in this work because they are the most straightforward device of its kind to control, and the associated driving circuitry design is relatively straightforward.

3.2.2. Si vs SiC vs GaN

Advances in MOSFET technology mimic More’s law, as seen in Fig. 3.1. It can be observed that the number of transistors in a dense integrated circuit (IC) doubles about every two years. This technology scaling effect not only makes the MOSFETs smaller but also much faster, as the speed is inversely proportional to the gate/base length [11].

(a)



(b)

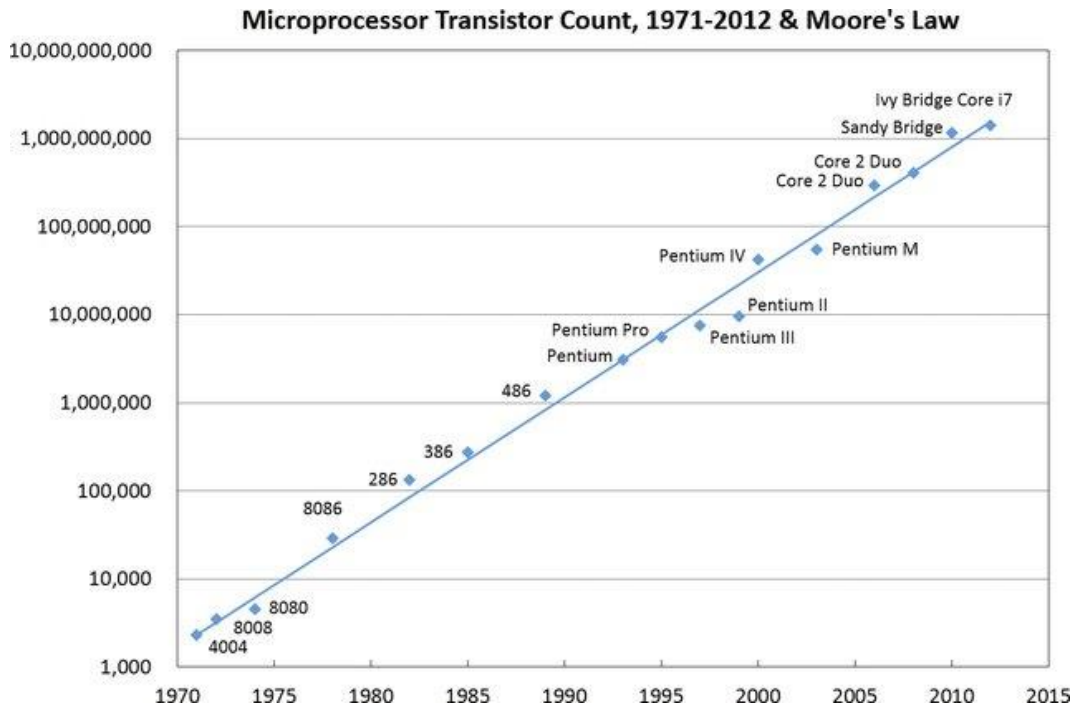


Fig. 3.1. Plot of number of transistors per microprocessors chip against dates of introduction. (a) [11] (b) [18].

The scaling of MOSFETs dimensions in combination with advances in semiconductor materials, such as SiC and GaN, has enabled semiconductor products to evolve rapidly over the past 40 years [11]. GaN and SiC semiconductor materials allow for smaller, faster, more reliable devices to be fabricated with higher efficiency than their silicon-based counterpart. This advancement has produced power MOSFETs with improved features such as better thermal conductivity, larger bandgaps, higher breakdown field strengths and faster electron mobility to name a few. These features are indicated in Fig. 3.2 [19], Fig. 3.3 [20] and Fig. 3.4 [21]. These features enabled the development of higher power

devices capable of handling larger currents and having higher breakdown voltages with faster transition times [8], [11].

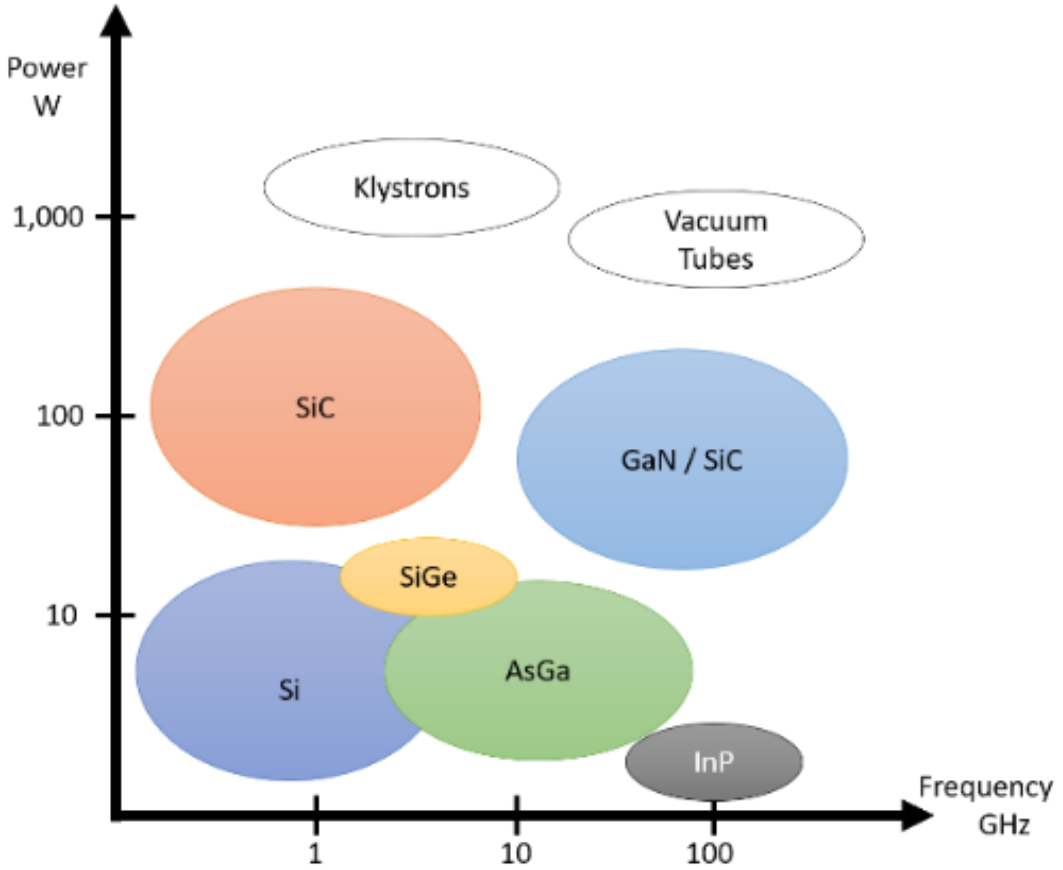


Fig. 3.2. Si, SiC and GaN semiconductor material properties power handling vs operating frequency capabilities [19]

There are particular advantages associated with each semiconductor material of Silicon (Si), SiC and GaN. Silicon is a relatively cheap substrate compared with SiC and GaN, but SiC and GaN devices offer better performance in terms of bandgap and drain-source breakdown voltages [22]-[24].

GaN and SiC are relatively similar with GaN having a bandgap of ~3.2 eV, whilst SiC has a bandgap of 3.4 eV. GaN and SiC's breakdown fields are again relatively similar, with GaN and SiC boasting a breakdown electric field of 3.3 MV/cm and 3.5 MV/cm respectively. Their bandgap and breakdown fields make these compounds significantly better equipped to handle higher voltages to support higher voltage circuits than Si base MOSFETs [22]-[24]. This feature is significant when designing a high voltage nsPEF electroporation system, as is presented in this work.

The most significant difference between GaN and SiC lies in their electron mobility, which indicates how quickly electrons can move through the semiconductor material. Si has an electron mobility of 1500 cm^2/Vs whilst GaN and SiC have an electron mobility value of 2000 cm^2/Vs and 650 cm^2/Vs respectively. This implies that SiC's electrons are slower moving than both GaN and Si. With such elevated electron mobility, GaN is nearly three times more suitable for high-frequency or fast-switching applications [20]-[21].

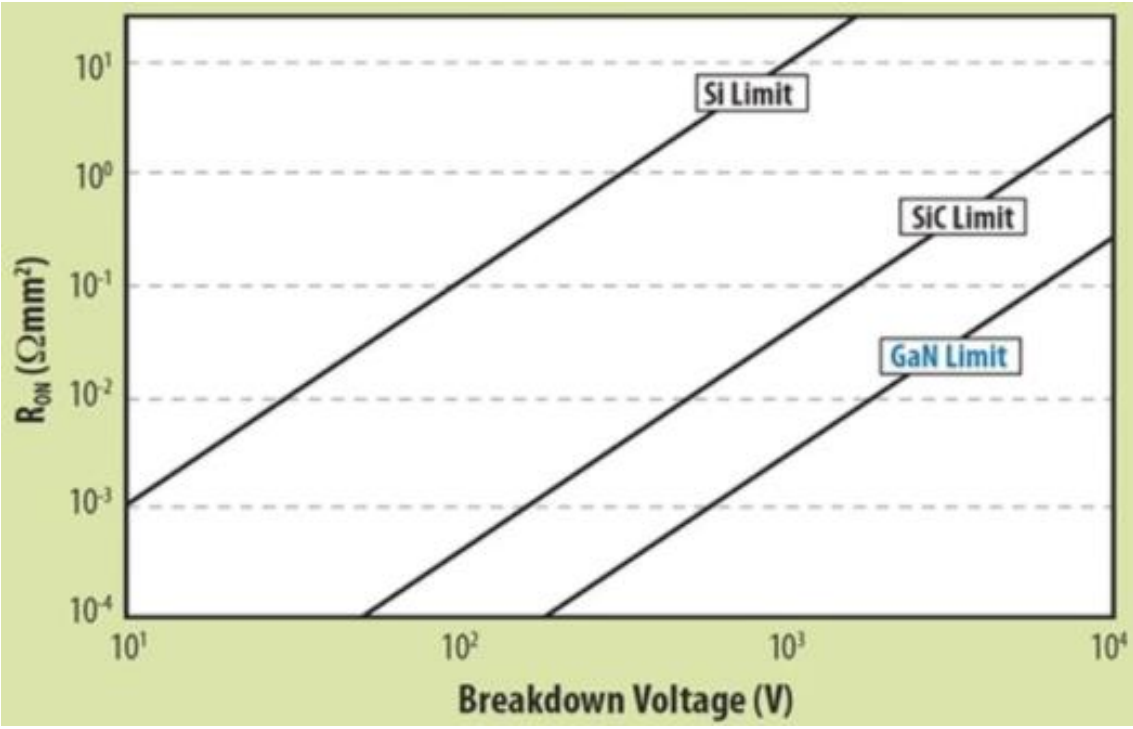


Fig. 3.3. Si, SiC and GaN Semiconductor material breakdown voltage vs ON-resistance characteristics [20]

Thermal conductivity directly influences the material's temperature and its ability to transfer heat through itself. In high-power applications, inefficiencies in materials will create heat, thus increasing the temperature of the material, and subsequently changing its electrical characteristics. GaN has a thermal conductivity value of 1.3 W/cmK in comparison to SiC with a value of 5 W/cmK. This makes SiC almost four times better at heat transfer, which is advantageous in high-power, high-temperature applications [20]-[24].

SiC power devices are far more mature than GaN-based devices in terms of offering breakdown voltages in excess of 1 kV. SiC MOSFET technology is better-suited technology for the high voltage PEFs generation with nanosecond regime rise and fall times required for this work. The primary advantage of SiC transistors is their very low switching losses, at higher-frequency operations. This is due to the positive temperature coefficient that allows the devices to be easily connected in parallel to withstand high operating currents and voltages, in excess of 40 A and 1200 V respectively [22]-[24].

In future, GaN is set to replace SiC power devices since SiC is said to have reached its performance limits regarding speed, temperature, and power handling capabilities. Although for the challenge at hand to produce PEFs of durations 100 ns to 300 ns, with amplitudes in excess of 1 kV, SiC n-channel enhancement type MOSFET devices were the best solution.

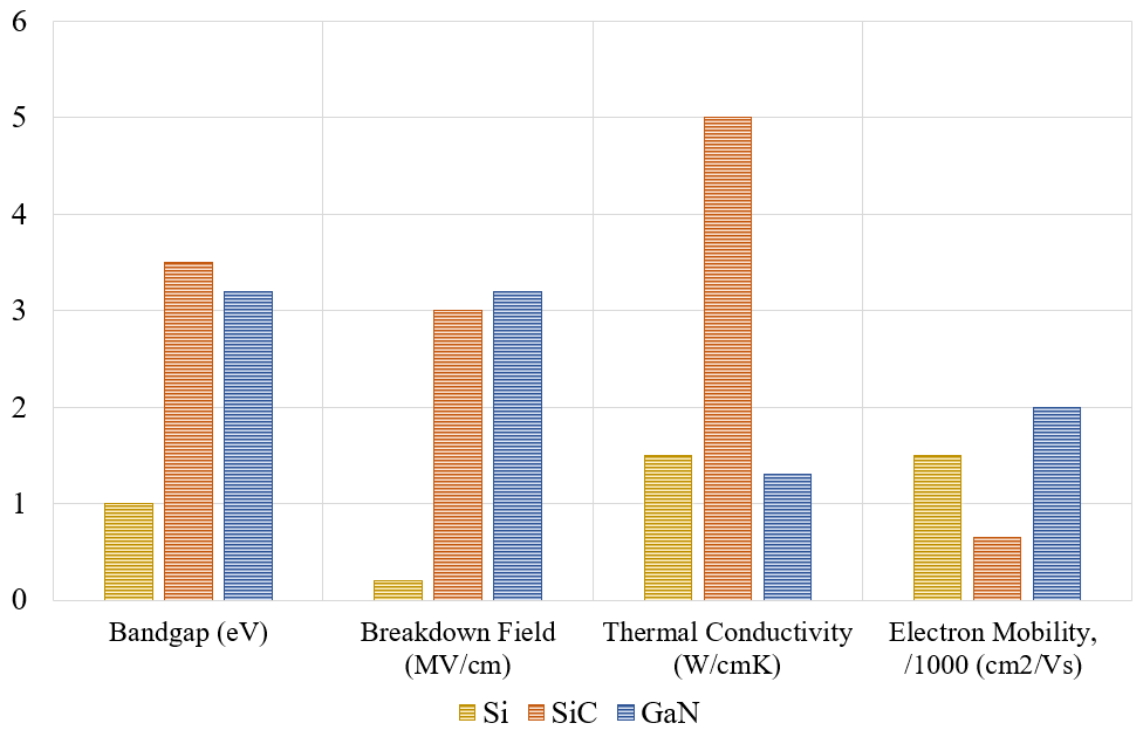


Fig. 3.4. Si, SiC and GaN semiconductor material property comparisons: bandgap, breakdown field, thermal conductivity, and electron mobility [21]

3.2.3. MOSFET Breakdown and Limitation Parameters

SiC Power MOSFETs with breakdown voltages (BV_{DS}) of 1700 V that can be operated with rise times (t_r) of less than 40 ns are commercially available [15]-[17]. These devices are available from suppliers such as RS [25], MOUSER [26], Farnell [27] and to name a few. SiC device developers / manufacturers include Wolfspeed [15] and Infineon [16].

For this application, it was important to choose a power MOSFET with a maximum drain-source voltage above 1 kV and total switching times below 100 ns to generate an electrical pulse of 100 ns duration with amplitudes in excess of 1 kV, into a 50 Ω load impedance. An n-channel enhancement-type MOSFET device was the device of choice, where a positive gate-source voltage (V_{GS}) is used to open the channel and control the drain current (i_d). The transconductance characteristic (i_d as a function of V_{GS}) was also considered carefully when choosing the most appropriate MOSFET for the required application.

Wolfspeed's C2M1000170D SiC n-channel enhancement mode power MOSFET was identified as a suitable component for the generation of nsPEF of 100 ns pulses. The key features of the C2M1000170D (see the datasheet Appendix III [28]) device are as follows:

- High switching speeds (10.5 ns rise-time, 60 ns fall-time) [28];
- High drain-source breakdown voltage (1700 V) [28];
- Low drain-source on-state resistance, $R_{DS(on)}$ (1 Ω) [28];

- Easy to parallel and simple to drive [28];
- Ultra-low drain-gate capacitance / low input capacitances (200 pF) [28];

The maximum gate-source voltage (V_{GSmax}) must not be exceeded. V_{GSmax} is determined by the thickness of the gate oxide layer and the magnitude of the applied electric field. Once the V_{GSmax} value is exceeded, the gate oxide breaks down and the MOSFET is permanently damaged. The C2M1000170D can withstand a V_{GSmax} of up to 25 V before breakdown occurs. Another maximum rating parameter which must not be exceeded is the drain-source voltage (V_{DSmax}) or the breakdown voltage (BV_{DS}). This is the maximum voltage that the device can withstand before the avalanche breakdown of the drain-body PN junction. The BV_{DS} for the C2M1000170D is 1700 V when V_{GS} is 0 V. When designing the gate drive and control circuitry it must be ensured that these MOSFET parameters are not exceeded and the device operates within its Safe Operating Area (SOA), as shown in Fig. 3.5. Three parameters that determine the SOA are the maximum drain current (i_d) the internal operating junction and storage temperatures (T_C or T_J) and the drain-source voltage (V_{DS}).

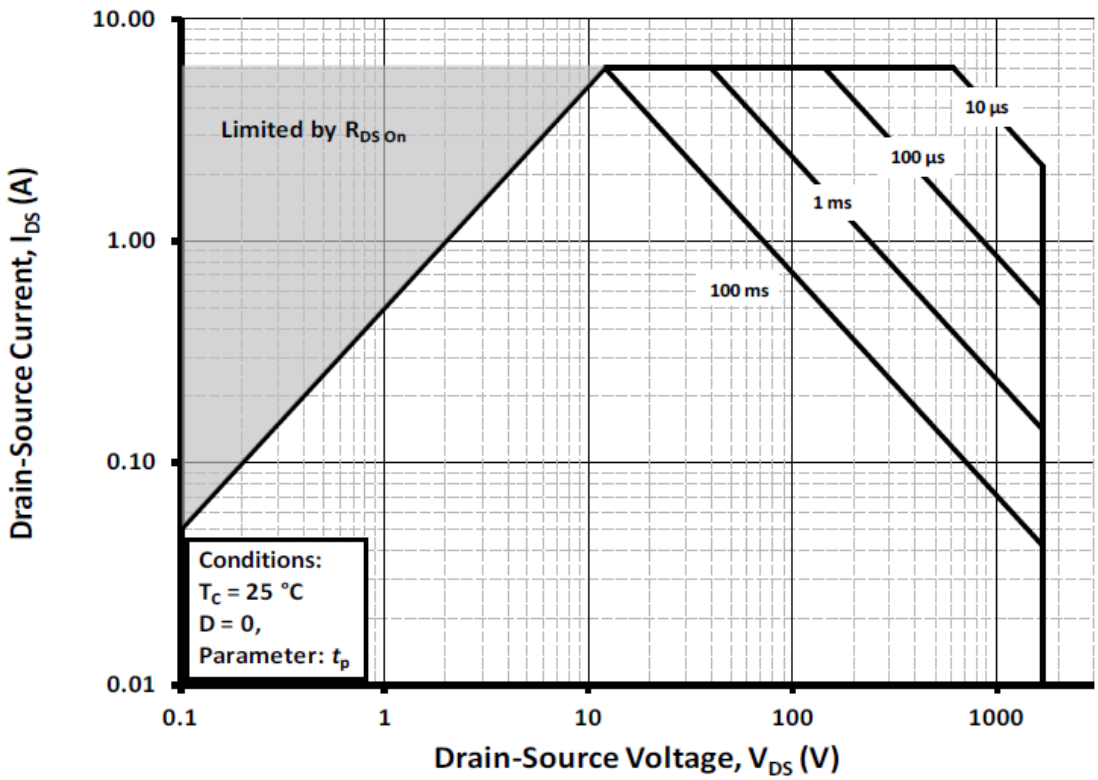


Fig. 3.5. Safe operating area for the C2M1000170D metal-oxide-semiconductor field-effect transistors [28]

To achieve nanosecond switching speed using the C2M1000170D power MOSFET, the maximum rating for the key parameters that determine the upper limit of its switching capabilities should be observed. The effects of the inherited device capacitance and subsequent charge control must be considered.

3.2.4. Gate Drive Requirements and Charge Control

For high voltage switching applications, MOSFETs are faster than bipolar devices i.e., bipolar junction transistors (BJTs) and insulated-gate bipolar junction transistors (IGBJTs). The gate of a MOSFET can be considered as capacitance and can be modelled by the equivalent circuit of a MOSFET as shown in Fig. 3.6.

The gate voltage of a MOSFET does not increase unless its gate input capacitance is charged, and the MOSFET does not turn 'ON' until its gate voltage reaches the gate threshold voltage (V_{th}) [29]. V_{th} of a MOSFET is defined as the minimum gate bias voltage required to open up the channel between the source and drain regions to allow current to flow.

From a typical MOSFET datasheet, the input, output, and reverse transfer capacitance values are usually provided. These capacitances can be calculated from the MOSFET's gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), and the drain-source capacitance (C_{ds}) as indicated below [29]. The drain-source capacitance (C_{ds}) does not effect on any of the MOSFET switching characteristics.

$$\text{Input Capacitance, } C_{iss} = C_{gd} + C_{gs}$$

$$\text{Output Capacitance, } C_{oss} = C_{ds} + C_{gd}$$

$$\text{Reverse Transfer Capacitance, } C_{rss} = C_{gd}$$

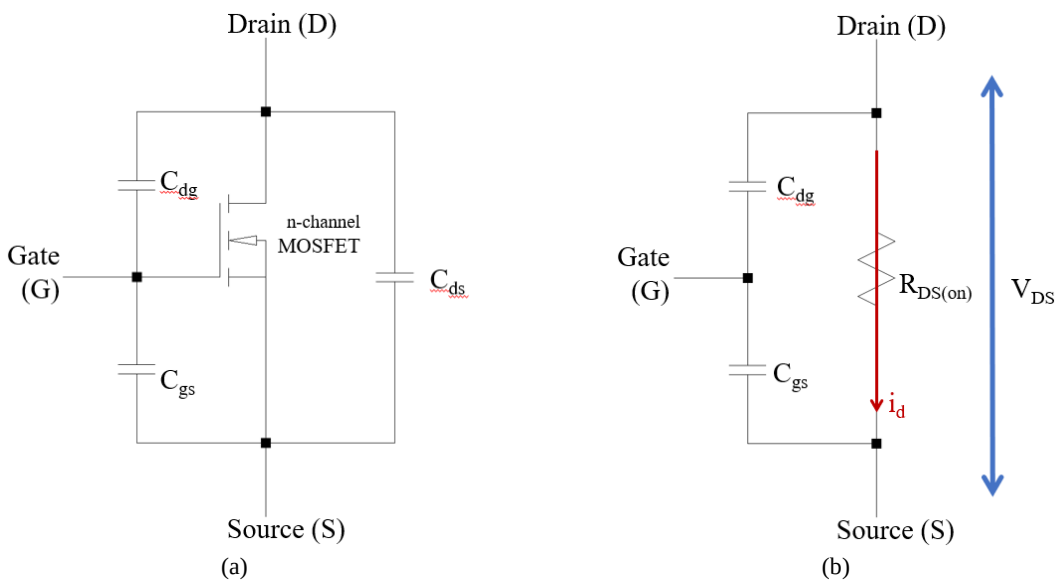


Fig. 3.6. n-channel enhancement power metal-oxide-semiconductor field-effect transistors equivalent (a) capacitance circuit (b) ON-resistance circuit [29]

During the turn 'ON' of a MOSFET, displacement current flows into the gate, charging the gate-source and gate-drain capacitances. The gate voltage-controlled current source can be assumed to be equal to zero when $V_{GS} < V_{th}$ and equal to $g_m(V_{GS} - V_{th})$, where g_m is the transfer conductance or

transconductance $\left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)\left(\frac{\Delta i_d}{V_{GS}}\right)$ when the device is operating in its active region. The device is in its switching mode when $V_{GS} >> V_{th}$ and its ohmic region when $V_{DS} < V_{GS}$. In the ohmic region, the dependent current source is no longer valid because the inversion layer is no longer pinched off at the drain end of the channel but has a spatially uniform thickness since V_{DS} is small. In the equivalent circuit, Fig 3.6(b), the inversion layer shorts the drain to the source, therefore the drain terminal C_{gd} is grounded and $R_{DS(on)}$ accounts for the ohmic losses [29].

As the capacitance is dependent on the depletion layer, the capacitances C_{gs} and C_{gd} vary according to the magnitude of the voltage, V_{DS}. The gate-source capacitance, C_{gs}, is a combination of the electrostatic capacitance of the oxide layer in series with the depletion capacitance. As the voltage across the drain-source is approximately identical to the voltage across the drain-gate, there is a significant change in the value of C_{gd} when a load is being switched, as illustrated in Fig. 3.7. The difference in capacitance ratio when the device is switched 'ON' and 'OF'F can be up to a factor of 10. C_{gd2} is when the device is switched 'ON', and C_{gd1} is when the device is 'OFF' [29].

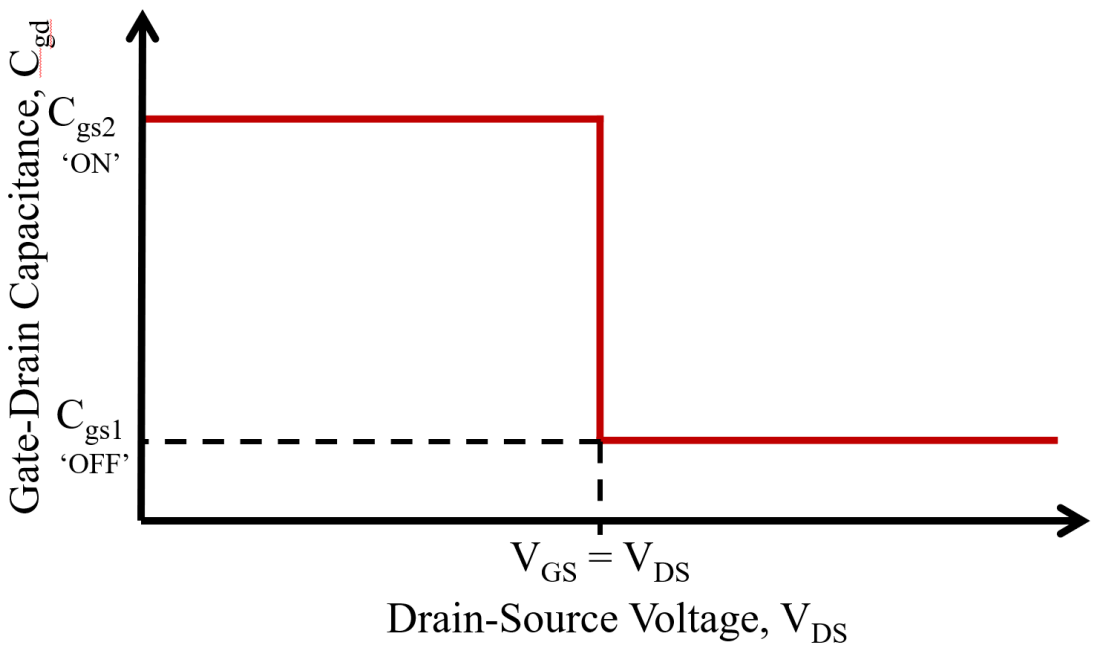


Fig. 3.7. The gate-drain capacitance (C_{gd}) as a function of drain-source voltage (V_{DS}) when the device is switching [29].

Fig. 3.8 shows the gate-source voltage variation over time when a constant current is applied to the gate terminal. As the gate current is constant, the time axis can be expressed in terms of gate charge (Q_g). Gate charge can be expressed by multiplying the gate current (i_g) by the time constant (t). The gate charge is therefore calculated as: $Q_g = i_g\, t$. The C2M1000170D SiC power MOSFET has an input capacitance (C_{iss}) of around 200 pF between the gate and the channel. This capacitance must be charged when the device is tuned 'ON' and discharged to turn the device 'OFF' [28].

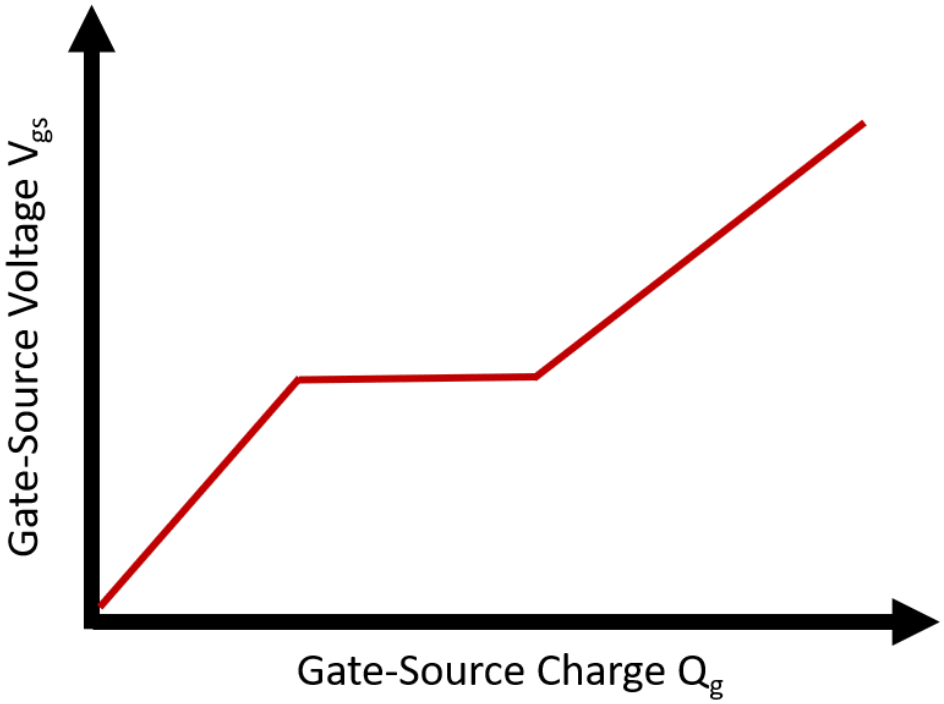


Fig. 3.8. The gate charge waveform expressed as the gate-source voltage (V_{GS}) vs the gate-source charge (Q_g) [29]

To produce pulsed fields with fast switching times in the order of nanoseconds, the charge and discharge times must be as short as possible. A gate driver is necessary to provide enough current to charge the input capacitance of the device to the necessary gate-source voltage, to enable the required current i_d to flow for the generation of pulsed electric fields with ns rise and fall times. The total gate capacitance (C_{gate}) is made up of the gate-source capacitance (C_{gs}) and the gate-drain capacitance (C_{gd}). The driving gate current (i_g) required to charge up the input capacitance (C_{iss}) for the MOSFET to switch high voltage is given by equations 3.1 and 3.2 below [29].

$$C_{gate} = C_{input} = C_{iss} = \left(C_{gs} + C_{gd}(1 + g_m Z_L)\right) \tag{3.1}$$

$$i_g = C_{iss}\frac{dV_{gs}}{dt} \tag{3.2}$$

where g_m is the transconductance $\left(\frac{di_d}{dV_{GS}}\right)$ of the MOSFET and Z_L is the load impedance presented to the circuit by the biological tissue. V_{GS} is the gate-source voltage and t is the pulse duration of the nsPEF generated. Table 3.2. exhibits the necessary current to drive the device of choice, the C2M1000170D MOSFET for the generation of 1 kV nsPEFs of 100 ns to 300 ns duration.

Table 3.2. Gate current required to drive the C2M1000170D to generate 100 ns, 200 ns and 300 ns pulses

Pulse Duration, T (ns)	*Pulse Amplitude, V_L (V)*	*input capacitance, C_{iss} (pF)*	*driving gate current, i_g*	*gate-source voltage, V_{GS} (V)*	*Max rise / fall-times, t_r/t_f (ns)*
100	1000	200	2 A	5	0.5
200	1000	200	1 A	5	1
300	1000	200	667 mA	5	1.5

3.2.5. MOSFET Gate Drive Circuit

For fast switching, the gate driver circuit must provide the MOSFET gate terminal with sufficient gate-source voltage, higher than its threshold voltage (V_{th}) to sufficiently charge its input capacitance (C_{iss}). Table 3.2. indicates the driving current required for the C2M1000170D gate to efficiently drive the MOSFET to generate nsPEF of 100 ns, 200 ns and 300 ns PEF. The gate threshold voltage for the C2M1000170D MOSFET is 2.6 V (V_{DS} = V_{GS}, I_D = 0.5 mA) [28]. The voltage to switch the C2M1000170D MOSFET V_{GS} is +5 V. Therefore, with a 2 A gate driver, one can charge the 200 pF input capacitance in 0.5 ns $dt = C\frac{dV}{i} = \frac{200\text{x}10^{-12}x5}{2}$

Basic Drive Circuit

The total capacitance of a MOSFET needs to be considered in the design of its gate driver circuit. The basic MOSFET driver circuit is illustrated in Fig. 3.9. In Fig. 3.9, R_1 is the MOSFET gate resistor. An appropriate gate resistor value should be selected as it affects the transition time (switching speed) of the MOSFET. Resistor R_2 functions as a pull-down resistor to reduce the gate-source voltage to 0 V when the input signal or trigger signal to the MOSFET gate terminal is open-circuit. The gate voltage or trigger signal needs to be sufficiently higher than the 2.6 V threshold voltage and have the capability to deliver a current of 2 A, to charge the 200 pF input capacitance to turn 'ON' and 'OFF' the C2M1000170D MOSFET in 0.5 ns [29].

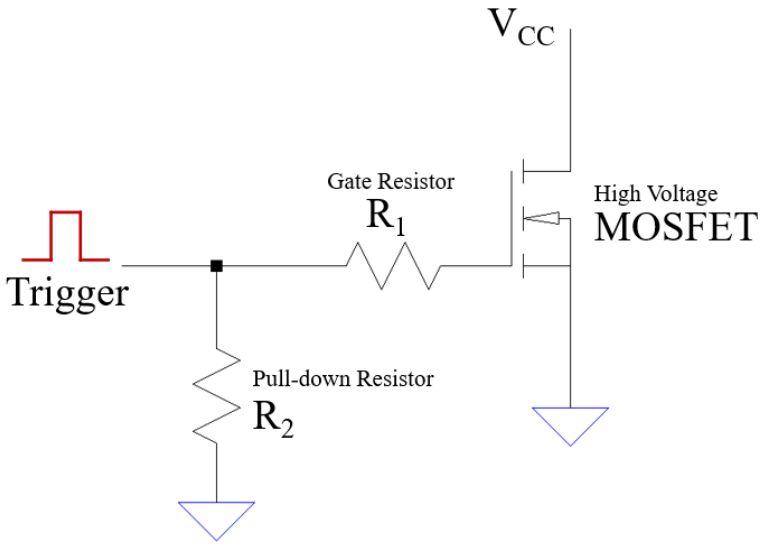


Fig. 3.9. Basic metal-oxide-semiconductor field-effect transistors driving circuit [29]

Logic Driven

Driving a MOSFET with a logic circuit would allow direct control and drive from the output point of a standard microcontroller. One advantage of directly driving a MOSFET using a microcontroller is that it provides a user-configurable method of controlling the pulses generated. From (3.1) and Table 3.2 a current of 2 A is required to efficiently charge the input capacitance, 200 pF, and drive a C2M1000170D MOSFET [33]. The maximum current that can be drawn from a microcontroller is

typically 200 mA. Therefore, it would not be possible to drive a C2M1000170D MOSFET directly without a gate driver if the transition times required and pulse duration is in the nanosecond regime. With the slower turn-on and turn-off times, the required current to charge the input capacitor would be significantly less and the logic method of driving a MOSFET may be applicable for the generation of PEF in the microsecond to second time regime [34].

Direct Drive Voltage Converter

To efficiently drive the C2M1000170D MOSFET the recommended operational value for the gate-source voltage is 20 V. Since a logic driver or micro-controller has insufficient voltage output swing to drive the MOSFET, a voltage converter is required to convert the trigger signal to the necessary driver voltage of 20 V.

Fig. 3.10 shows an example of how to drive a MOSFET with a logic control via a current driver/voltage converter. This converter circuit increases the 5 V logic signal needed to drive a MOSFET above its threshold voltage. In this case, applying a V_{GS} of +20 V from a 5 V logic trigger signal [34].

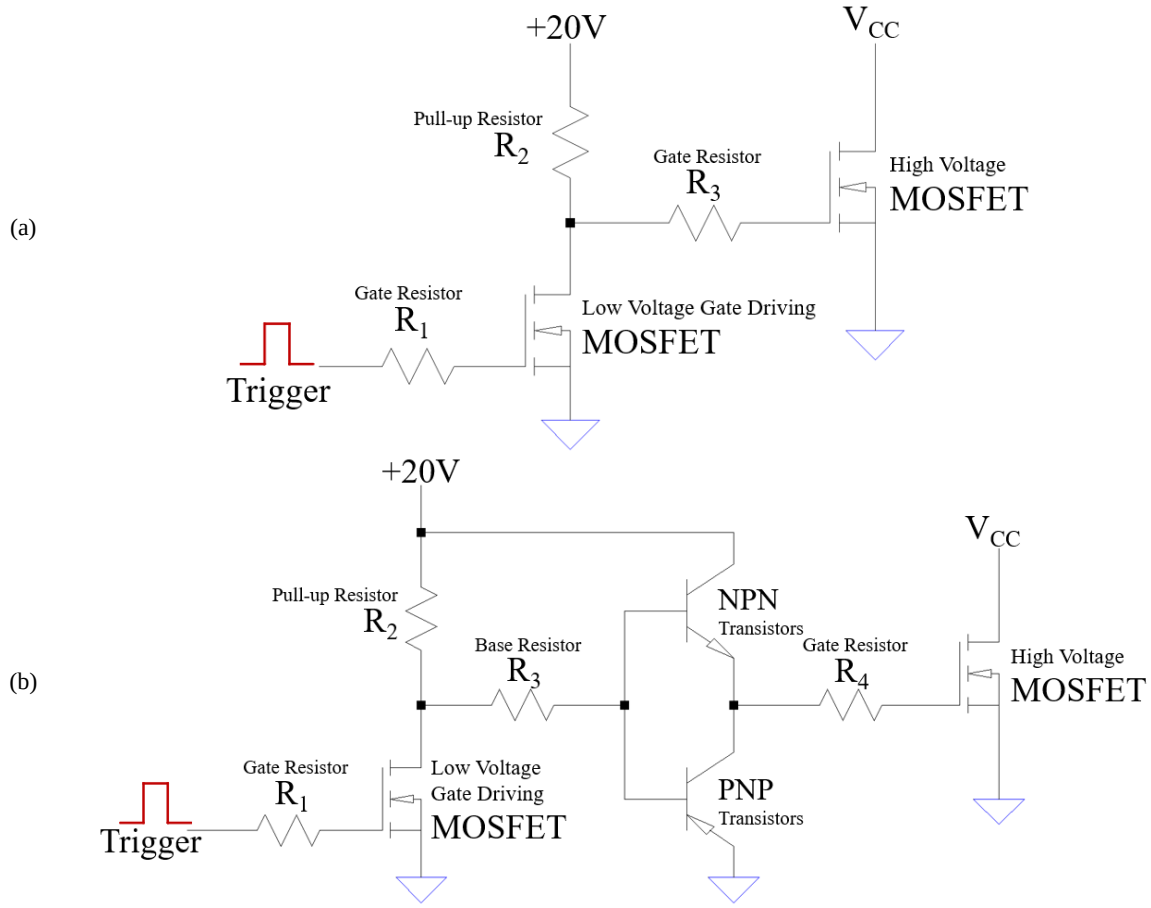


Fig. 3.10. A 20 V drive voltage conversion (a) basic circuit (b) push-pull circuit [29]

In Fig. 3.10, resistor R_2 is connected in series with the gate resistor R_3, and increases the gate drive resistance, making it difficult to drive the MOSFET in saturation mode. This slows the switching speed

of the MOSFET and therefore increases the switching loss. Reducing R_2 causes a large drain current (i_d) to flow to the drive circuit during the turn 'OFF' period of the MOSFET, increasing the power consumption of the drive circuit [34].

The drawback of the circuit shown in Fig. 3.10(a) is that the high voltage MOSFET is driven by another MOSFET. MOSFETs are a voltage-driven/controlled device while BJTs are current-driven devices. By driving the high voltage MOSFET with a push-pull configuration of BJTs as seen in Fig. 3.10(b) they provide sufficient drive current for the high voltage MOSFET providing higher current to charge and discharge the MOSFET input capacitance resulting in fast switching times. Therefore, it is better to drive a high voltage MSOFET for fast switching times, in the nanosecond regime, with a BJTs (Fig. 3.10(a)) than a MOSFET (Fig. 3.10(a)).

Transformer Driver (Insulated Switching)

The use of a pulse transformer eliminates the need for a separate drive power supply as the voltage swing is in the positive and negative directions. As the MOSFET for this application switches a high voltage i.e, 1 kV+, it is recommended that the drive circuit is isolated from the MOSFET by using a transformer, to provide galvanic or magnetic isolation. This is illustrated in Fig. 3.11. This isolation reduces unnecessary noise/interference to be feedback to the driver circuit and any common mode noise is cancelled out [29]. Accurate switching times are essential for this application, particularly for the push-pull configuration of the MOSFETs.

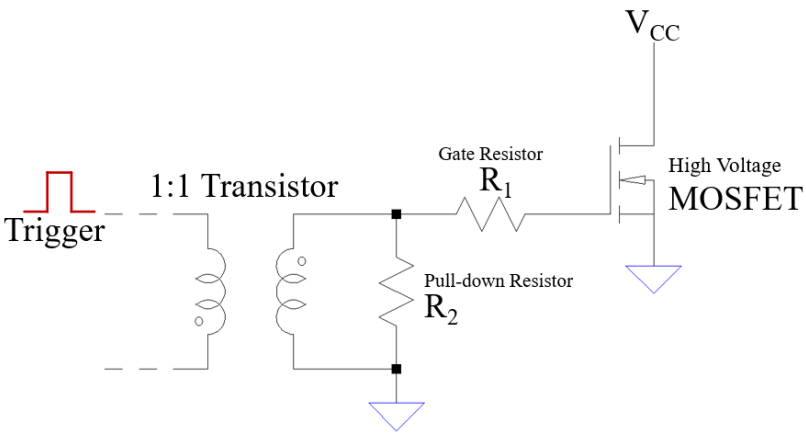


Fig. 3.11. Gate drive transformer circuit [29]

Photocoupler Driver

An optically isolated device, such as a photocoupler, can also be utilised as a MOSFET gate driver, as illustrated in Fig. 3.12. A separate power supply is necessary to establish the amplitude and current of the MOSFET gate driving signal from a photocoupler output. To utilise a photocoupler to drive the high side of a push-pull, half, or full bridge switching circuit, a floating power supply is necessary. Consideration has to be given to the speed and current drive capability of the photocoupler to efficiently drive a specific MOSFET [29].

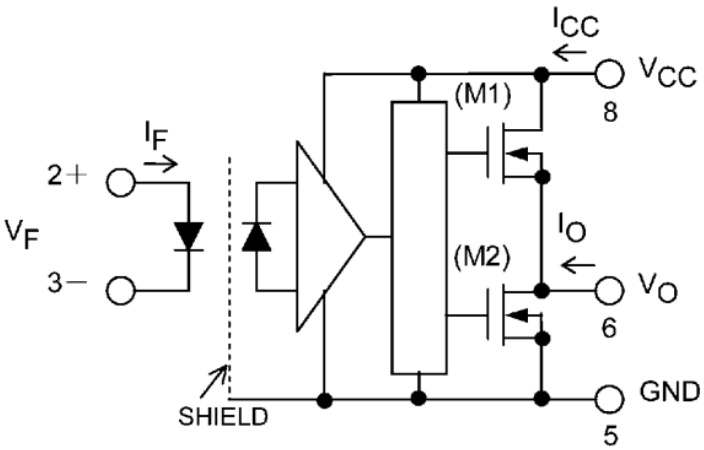


Fig. 3.12. Gate drive photocoupler circuit - TLP352 photocoupler internal circuit [30]

Direct Versus Isolated Gate Driver Circuit

As discussed, the Wolfspeed C2M1000170D SiC n-channel enhancement mode power MOSFET is a device that can be used in circuits to produce nsPEFs with pulse duration of the order of 100 ns [28]. For successful switching of the C2M1000170D MOSFET, a control signal of 20 V (25 V max) and a current capability of 2 A at the gate are required. Because of this requirement, a direct drive voltage converter, or an isolated gate driver is used to convert a +5 V from a digital microcontroller to a voltage level of up to 25 V and delivers up to 2 A to charge up the gate-source capacitance associated with the power MOSFET. This isolated driver circuit may either consist of a transistor to magnetically couple the signal from the microcontroller and the high voltage circuit or an arrangement of photodiodes to provide opto-isolation. Both of these methods isolate the low voltage pulses produced by the microcontroller from the high voltage pulses produced by the high voltage pulses generation circuit.

A driver voltage converter that utilises two transistors in series can be implemented to drive the C2M1000170D MOSFET. The NPN and PNP transistors connected in series operate as a matched switch that provides the fast-switching transition times required in addition to the voltage and current requirement to efficiently drive the C2M1000170D (20 V, 2 A). Combining a PNP transistor with an NPN transistor, as a matched switching element, is a common design used when developing power circuits to drive power MOSFETs. Normally, the PNP and NPN transistors are contained in a single package. A typical gate driver circuit is shown in Fig. 3.13.

As an example of the application of the circuit, a logic gate trigger may be amplified from a transistor–transistor logic (TTL) voltage and current output of 5 V and 200 mA to a gate voltage and current of 20 V and 2 A to charge the input capacitance of the MOSFET $\left(\frac{dV}{dt} = \frac{i}{C}\right)$. The pair of NPN and PNP transistors are used in Class B configuration as a complementary or matched switch, where the PNP transistor conducts for the negative half cycle while the NPN transistor conducts for the

positive half cycle. This implies that a single control signal is required to operate both the NPN and PNP transistor [34].

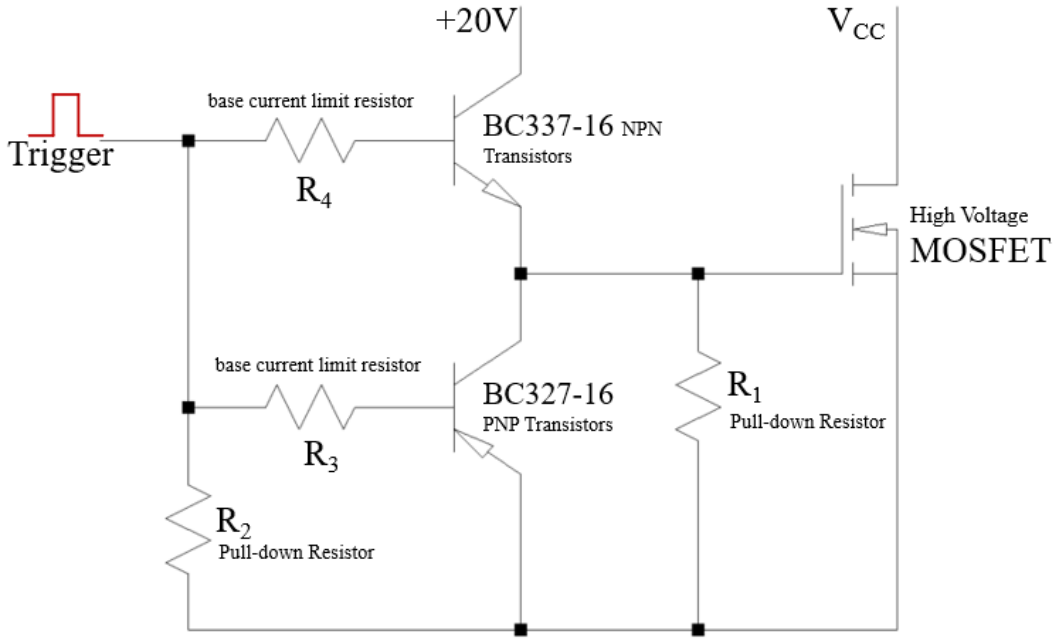


Fig. 3.13. NPN and PNP transistor in a matched switch construct operating as a metal-oxide-semiconductor field-effect transistors gate driver

To drive the C2M1000170D MOSFET [28] a BC327-16 (PNP transistor) [31] and a BC337-16 (NPN transistor) [32] operating in a push-pull were identified as an efficient gate driver circuit. Resistors R_3 and R_4 are base current limit resistors and resistors R_1 and R_2 are pull-down resistors.

An optocoupler or a photocoupler is a semiconductor device that uses a short optical path or link to couple a signal from one electrical circuit to another whilst providing electrical isolation. A Toshiba TLP352 [30] is a suitable photocoupler to drive the C2M1000170D MOSFET as it can produce a gate voltage signal of +15 V to +30 V, and a peak current of 2.5 A.

The TLP352 is specified to provide 3750 V_{rms} of isolation voltage. This factor provides isolation or shields with the low voltage circuitry (microcontroller input control signal input to the optocoupler) and the high voltage circuitry associated with the high voltage switching operation of the MOSFETs. This isolation reduces unnecessary noise/interference to be fed back to the driver circuit and cancels out common mode noise [29]-[30].

The internal circuit of the TLP352 Photocoupler is illustrated in Fig. 3.12 [30]. The internal circuitry is constructed of a totem-pole output that can both sink and source current. This is ideal for driving IGBT and power MOSFET devices.

Considering the drive voltage converter (Fig. 3.13) and photocoupler method (Fig. 3.12) for driving the C2M1000170D MOSFET, the TLP352 Photocoupler was the preferred method as the isolation protects the low voltage microcontroller from the high voltage switch. Both methodologies

produce the necessary gate current, and voltage needed to efficiently drive the C2M1000170D. Unlike the drive voltage converter, the TLP352 Photocoupler provides isolation from voltages of up to 3750 V_{rms} [30].

Without an optoisolators, circuit failure occurred. This failure relates to thermal runaway associated with the high voltage switching and feedback at the high side switching level. The photocoupler overcame this issue as it isolated the low voltage and high voltage floating circuit due to its associated isolation that is rated up to 3750 $V_{rms(min)}$ voltage. In conclusion, a TLP352 Photocoupler [30] was used to efficiently drive the high-power fast switching C2M1000170D MOSFET [28].

3.2.6. MOSFET Switching Topologies

Following discussions with microbiologists and researchers interested in the field of cell electroporation, it was highlighted that there is a need for a nanosecond electroporation system apparatus that can produce symmetrical (identical rise and fall-times) nsPEF with an amplitude that exceeds 1 kV and a range of pulse durations from 100 ns to 300 ns, repetition frequency from 1 Hz to 50 Hz, and generate a specific number of nsPEF.

Because of the agreed specification for the slow nsPEF electroporation system, a push-pull configuration of two MOSFETs as a switching topology was selected to provide the optimal solution. A push-pull configuration switching topology using MOSFETs provides numerous advantages over conventional nsPEF generation topologies such as charged transmission lines, spark gaps and other semiconductor transistors-based switching topologies. The advantages of MOSFET technology over other switching technology for the generation of slow PEFs has been highlighted earlier in this chapter and Chapter 2. Using high voltage, fast switching power MOSFETs configured in a push-pull configuration enabled a well-controlled electro-manipulation technique to be available for microbiologists and researchers in the field of electroporation.

Push-pull Configuration

When a single MOSFET is used to generate high voltage sub-microsecond pulses to be delivered into a fixed low impedance load without reduction in amplitude the gate-source and gate-drain capacitances associated with the MOSFET must be charged and discharged and this can result in unacceptably long switching times. This is particularly true for the discharge of the input capacitance necessary to switch the pulse ‘OFF’. The fall time of the pulse is dictated by the discharge time constant which is determined by the gate-source capacitance of the MOSFET and the impedance load ($t_f = \tau = C_{gs} Z_L$). The majority of MOSFETs available today produce faster rise times in comparison to their fall times. This is true whether a MOSFET is purposely designed to operate in the nanosecond time regime-switching or not. This is seen when looking at the switching times associated with the C2M1000170D device used in this work (10.5 ns rise time and 60 ns fall time) [28].

To overcome this problem, two MOSFETs can be used in a push-pull configuration, as shown in Fig. 3.14 and 3.15. This switching topology means that when the high side MOSFET (S1) is open ('OFF') the low side MOSFET (S2) is closed ('ON'), and vice versa. The relationship between the two MOSFET switching status is synchronized and operated with a single gate control signal as shown in Fig. 3.14, and complementary gate control signals as shown in Fig. 3.15.

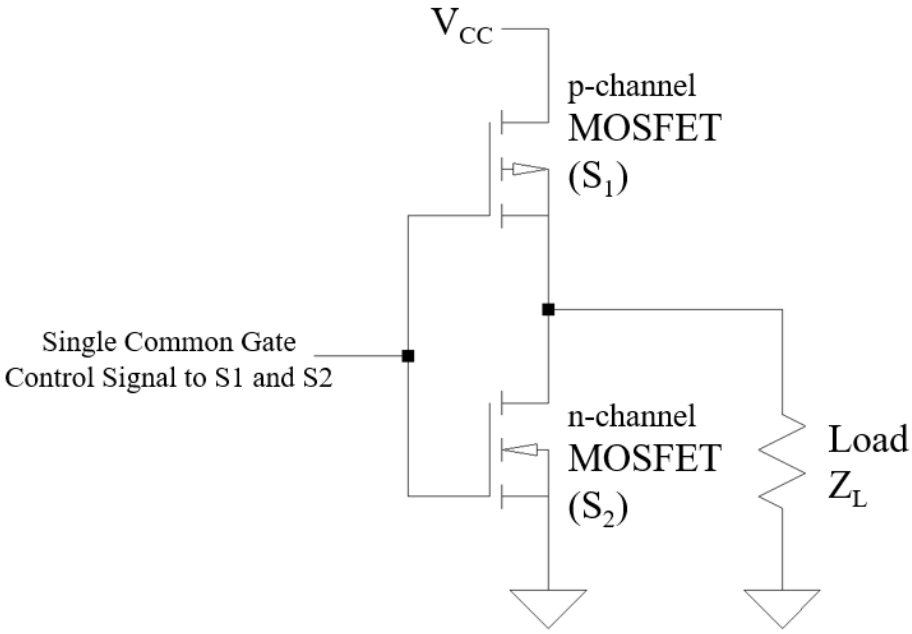


Fig. 3.14. Push-pull configuration for pulse generation with an n and p type metal-oxide-semiconductor field-effect transistors

Fig. 3.14 illustrates a push-pull topology with an n-type and a p-type MOSFET. With this topology, a single signal control (active high) is required to operate the two MOSFETs. A high-level signal input switches the n-type MOSFET 'ON' and the p-type MOSFET 'OFF' and vice versa when a low-level input signal is applied to their gate. The disadvantage of this arrangement is that it is necessary for both the n-type and p-type MOSFET to have the same operational parameters, such as input capacitance, rise-time, breakdown voltages etc. to enable the generation of symmetrical pulses.

Fig. 3.15 on the other hand illustrates the topology for operating two identical n-type MOSFETs overcomes the disadvantages associated with the configuration shown in Fig. 3.14. The downside of this topology is its critical dependency on driving the high side MOSFET (S_1) with an active high (logic level is 1 (5V)) gate signal and an active low gate driving signal (logic level is 0) to operate the low side MOSFET (S_2). Both the active high and active low gate signals in driving/switching both the high side and low side MOSFETs must be carefully controlled and complimentary of one another.

The operation of the equivalent circuit for a push-pull configuration of two MOSFETs connected in series for the generation of symmetrical nsPEFs illustrated in Fig. 3.15 is given in Fig. 3.16. Fig. 3.16(a) illustrates the basic modular design of the MOSFETs operating in a push-pull configuration as

two switches. S1 illustrates the first MOSFET on the high side that is controlled by an active high gate signal, and S2 is the low side second MOSFET that is controlled by an active low gate signal.

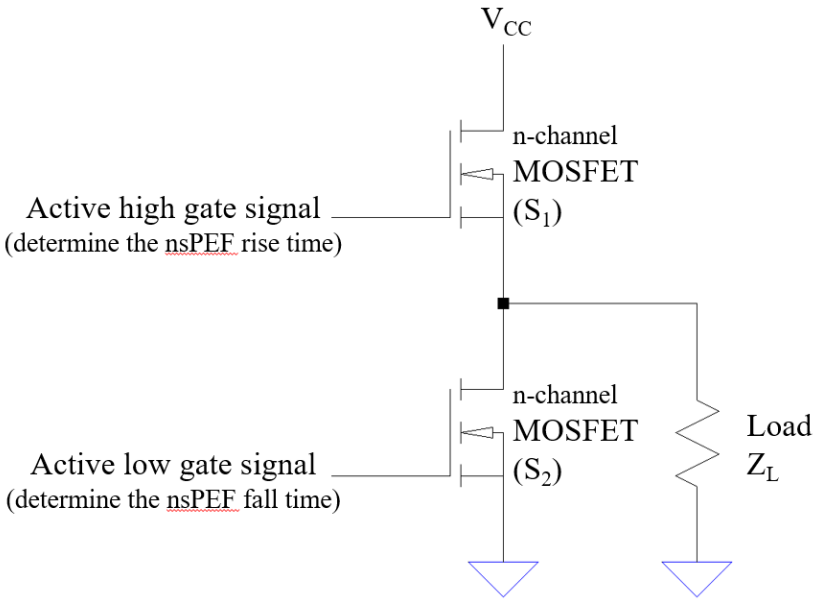


Fig. 3.15. Push-pull configuration of two n-type metal-oxide-semiconductor field-effect transistors with complementary gate control signals for pulsed electric field generation

In this arrangement, nsPEF are generated by the synchronized and complementary operation of both high (S_1) and low-sided (S_2) MOSFETs. When S_1 (the high side MOSFET) is turned 'ON', a high positive voltage is applied to the load. The current flow (red dotted line), from the high voltage source (V_{CC}) and through the load is shown in Fig. 3.16(b). In addition, to applying the high voltage amplitude across the load, the operation of S_1 determines the pulse duration (pulse width) and rise-time of the nsPEF applied across the load.

When S_1 is turned 'OFF', and S_2 is turned 'ON', a second path for the current to flow (blue dotted line) from the load to the ground is cheated, as shown in Fig. 3.16(c). The switching of S_2 creates a low impedance path, which allows the high voltage pulse delivered at the load to discharge to the ground. Therefore, S_2 controls the fall-time of the generated pulse. Implementing the push-pull configuration illustrated in Fig. 3.15 and Fig. 3.16 results in a faster fall time than is possible using a single MOSFET implementation, and leads to symmetrical PEFs across the load, with identical rise and fall times.

It is imperative that both MOSFETs, S_1 and S_2, are not switched 'ON' simultaneously. In such an event, the high voltage supply would be grounded or there would be a short circuit across the load impedance. This situation could result in shorting of the power supply to the ground and a potential temperature rise or breakdown of MOSFETs due to the power dissipation of the drain-source resistance $\left(P = I^2 R_{DS(on)}\right)$.

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impedance. This situation could result in shorting of the power supply to the ground and a potential temperature rise or breakdown of MOSFETs due to the power dissipation of the drain-source resistance $\left(P = I^2 R_{DS(on)}\right)$.

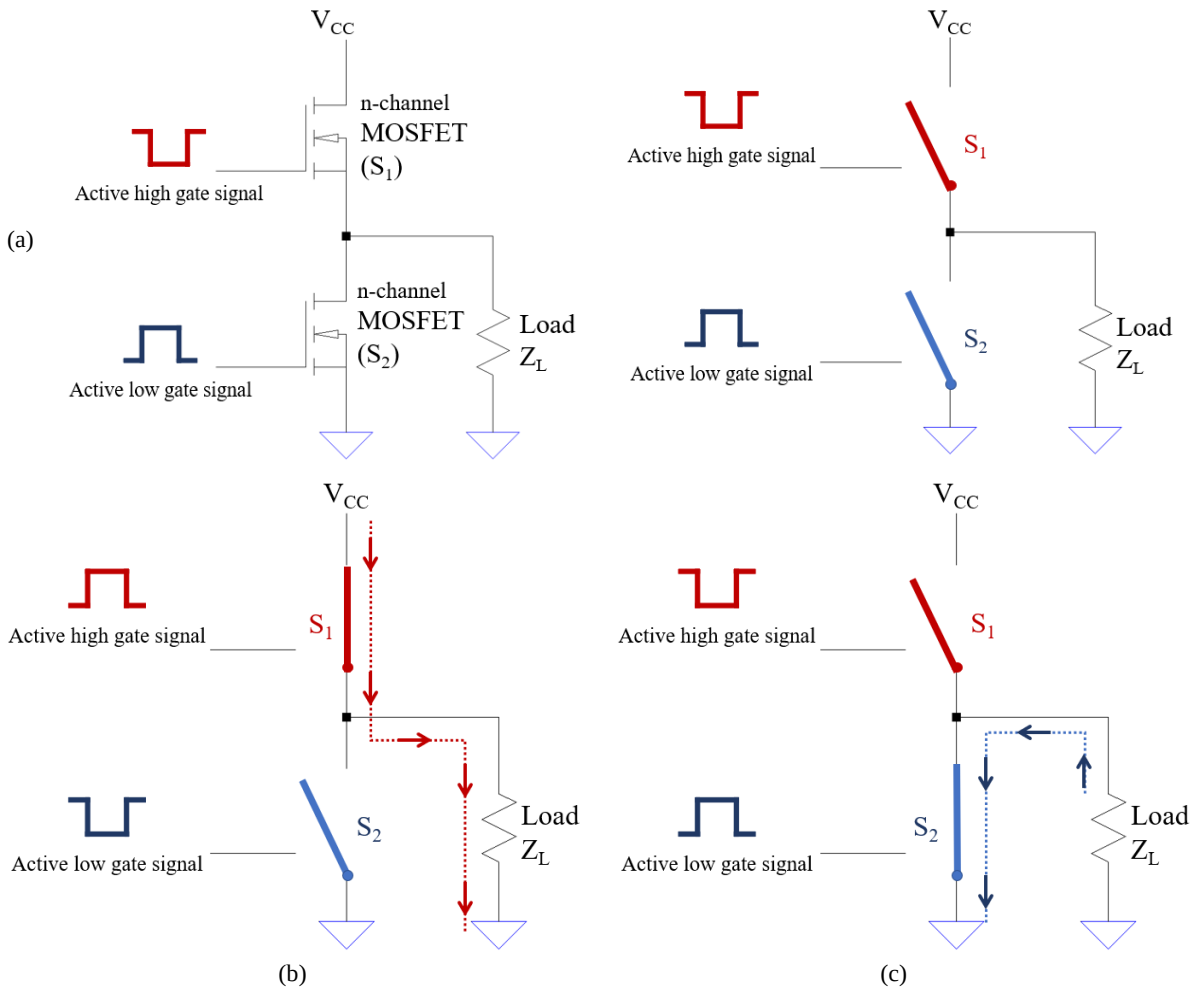


Fig. 3.16. (a) Modular design of the push-pull configuration with two n-type MOSFETs and the circuit simplified as switches (b) current path when S_1 is closed and S_2 open (c) current path when S_1 is open and S_2 is closed.

Full-bridge Configuration

The full-bridge, or H-Bridge topology, consists of four switches where one pair of switches are open, and another is closed in a particular sequence. Full-bridge topology using high-performance MOSFETs can produce nsPEF of either positive and/or negative polarity across a load, using a single dc supply source. As shown in Fig. 3.17(a), the full-bridge topology is a configuration of four MOSFET switches arranged in an H shape. Switches S_1 and S_3 are referred to as the left-hand side of the half-bridge and switches S_2 and S_4 are referred to as the right-hand switching leg [14]. Ideally, both the left side and right sides of the H-bridge configuration are identical so that the currents and losses are balanced [14]. The driving signals need to be taken into careful consideration as these determine the generated pulse characteristics.

As shown in Fig. 3.17, the gate drive signals for all switches (S_1, S_2, S_3 and S_4) are synchronised in such a way to alternate the dc voltage potential across the load impedance. The switch pairs are S_1 and S_4, and S_2 and S_3. When S_1 and S_4 are switched 'ON', and S_2 and S_3 are switched 'OFF' then a positive going pulse is produced across the load, as seen in Fig. 3.17(b). When S_1 and S_4 are turned 'OFF', and S_2 and S_3 are turned 'ON' a negative going pulse is produced across the load, as shown in Fig. 3.17(c).

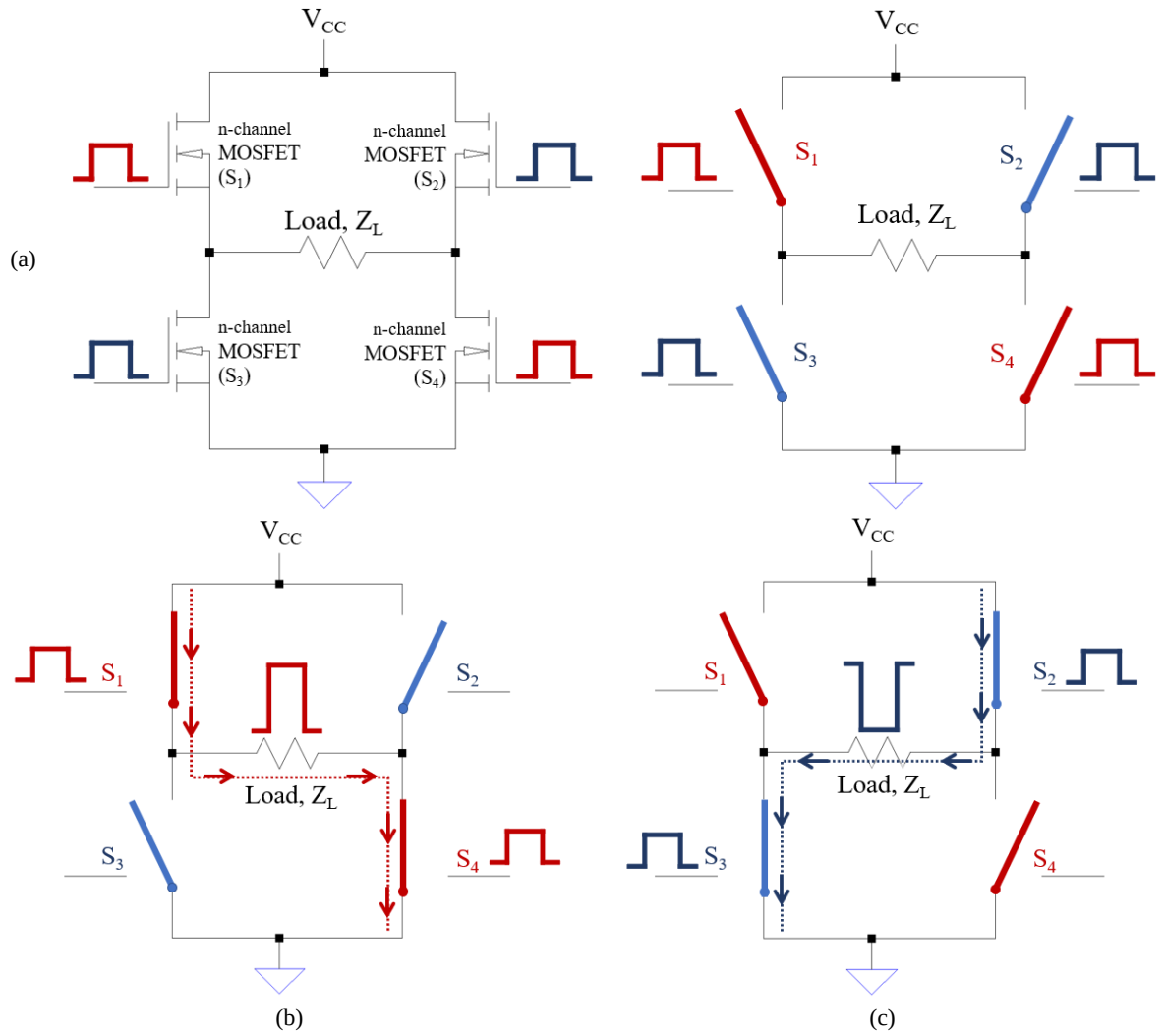


Fig. 3.17. (a) Full-bridge or H-Bridge MOSFET topology (right) and the circuit simplified as switches (left) (b) current path for a positive nanosecond pulsed electric field (S_1 and S_4 is closed) (c) current path for a negative nanosecond pulsed electric field (S_2 and S_3 is closed).

Table 3.3 lists the output states for a single H-bridge stage. This indicates that the synchronous timing between switching the pairs of S_1 and S_4, and S_2 and S_3 could results in a monopolar or bipolar nsPEF generated across the load impedance. A series of positive nsPEFs or negative nsPEFs can be generated across the load, or a series of alternating positive and negative pulses. This highlights the importance of synchronised driving of the gates of the MOSFETs in the H-bridge.

Table 3.3 The output state across a load from a full-bridge topology (Fig. 3.17) [14]

S_1	S_2	S_3	S_4	***nsPEF Polarity at Load***
On	Off	Off	On	Positive
Off	On	On	Off	Negative
On	On	Off	Off	0
Off	Off	On	On	0

If S_1 and S_3 or S_2 and S_4 are turned 'ON' at the same time a shoot-through current is created, in which a failure event occurs when two adjacent switches in a voltage source inverter are 'ON' simultaneously. Therefore, short-circuiting the power supply. High pulsed currents can result in cross-conduction which may exceed the MOSFET maximum drain current specification. Dead-time is introduced between switching devices of each switching leg to mitigate shoot-through currents. High-power full-bridge designs require longer dead-time due to increased parasitic elements [33]-[34]. Most MOSFETs have a high input capacitance and any parasitic inductance can cause an oscillation $\left(f = \frac{1}{2\pi\sqrt{LC}}\right)$. Often adding a series resistor to the MOSFETs gate reduces Q and the overshoot $\left(Q = \frac{1}{R}\sqrt{\frac{L}{C}}\right)$ [33]-[34].

Final MOSFET Switching Topology

As both push-pull and H-bridge topologies would utilise the same power MOSFETs (C2M1000170D), the nsPEFs produced across the load will have the same parameters, in terms of the rise-time, amplitude, pulse width and repetition frequency capability. The H-bridge configuration offers the capability to produce positive or negative monopolar pulses or bipolar pulses, while the push-pull configuration can only produce positive monopolar nsPEFs across the load.

Following discussion with microbiologists [2], [35]-[36], and further literature review [37]-[38], the push-pull topology was developed in this work rather than an H-bridge topology due to the cancellation effect associated with bipolar PEF application within the field of electroporation. In the cancellation effect, the effect of the first PEF is reduced by the second PEF of opposite polarity delivered onto a biological load. The cancellation effect is observed in treatments using high-frequency (ns-regime pulse duration) bipolar pulses. This effect is partially explained by the assisted discharge of the chloride channels associated with biological cells. The overall effect on the cells of bipolar pulses was profoundly reduced in comparison to monopolar pulses, despite delivering twice the energy [37]-[38] .

Cancellation impacts nanosecond electroporation applications in cancer therapy, electrostimulation, and biotechnology, and provides new insights into the effects of more complex waveforms, including pulsed electromagnetic emissions [38]. For the slow nsPEF electroporation system to assist the contribution of microbiologists and clinicians to investigate the effect of nsPEFs

and its possible capability to become an alternative clinical treatment for cancer, a push-pull configuration topology was pursued. The H-bridge topology can be pursued in future to advance and support further nanosecond-pulse-based applications in biology, medicine, and/or biotechnology and will form a part of suggested future work.

3.3. The Developed Slow nsPEF Electroporation System

The requirement for the design and development of the slow nsPEF electroporation system is to produce a specific number of PEFs with pulse durations between 100 ns to 300 ns, with amplitudes in excess of 1kV, delivered across a 50 Ω load impedance with repetition frequencies between 1 Hz to 50 Hz.

With the latest advancements in SiC material technology, it was important to choose a SiC power MOSFET with a minimum drain-source breakdown voltage of 1kV and a rise time below 40 ns, to generate a PEF of 100 ns duration with amplitudes in excess of 1 kV. SiC MOSFETs are voltage-controlled semiconductor devices that efficiently store charge in their minority carrier region, resulting in very rapid turn on (t_r) and turn off (t_f) times. The actual value for this maximum drain-source voltage rating and rise time is 1.7 kV and 10.5 ns respectively [28]. An n-channel enhancement type MOSFET device was chosen, where a positive gate-source voltage (V_{GS}) opens the channel to control the drain current (i_d). The transconductance characteristic (i_d as a function of V_{GS}) was also considered carefully when choosing the most appropriate MOSFET to be utilised.

The modular design developed here is based on a push-pull switch configuration, shown in Fig. 3.16, using two Wolfspeed's C2M1000170D SiC MOSFETs [28] that are directly driven by a Toshiba TLP352 photocoupler [30]. The developed design in this work provides a controllable method of delivering various nsPEFs with the ability to vary the pulse widths, repetition frequency, amplitude and the number of PEFs generated.

Two C2M1000170D SiC power MOSFETs connected in a push-pull configuration is the implemented topology for the generation of symmetrical nsPEFs that meet the requirements set to further support nanosecond-pulse-based applications and research in biology, medicine, and/or biotechnology.

The topology implemented is shown in Fig. 3.18. The configuration is separated into two halves. The high side and the low side circuit. Both the high and the low side hardware circuitry are identical but vary in their gate drive control signal/switching, which compliments each other. The high side circuitry operates the high side MOSFET (S_1), and the low side circuitry operates the low side MOSFET (S_2).

The high side MOSFET (S1) is driven by an active high control signal from a microcontroller that have been amplified via a high side MOSFET driver circuit (TLP352) to supply sufficient gate driving current. Whilst the low side MOSFET (S2) is driven by an active low control signal from a microcontroller that have been amplified via a low side MOSFET driver circuit (TLP352) to supply sufficient gate driving current.

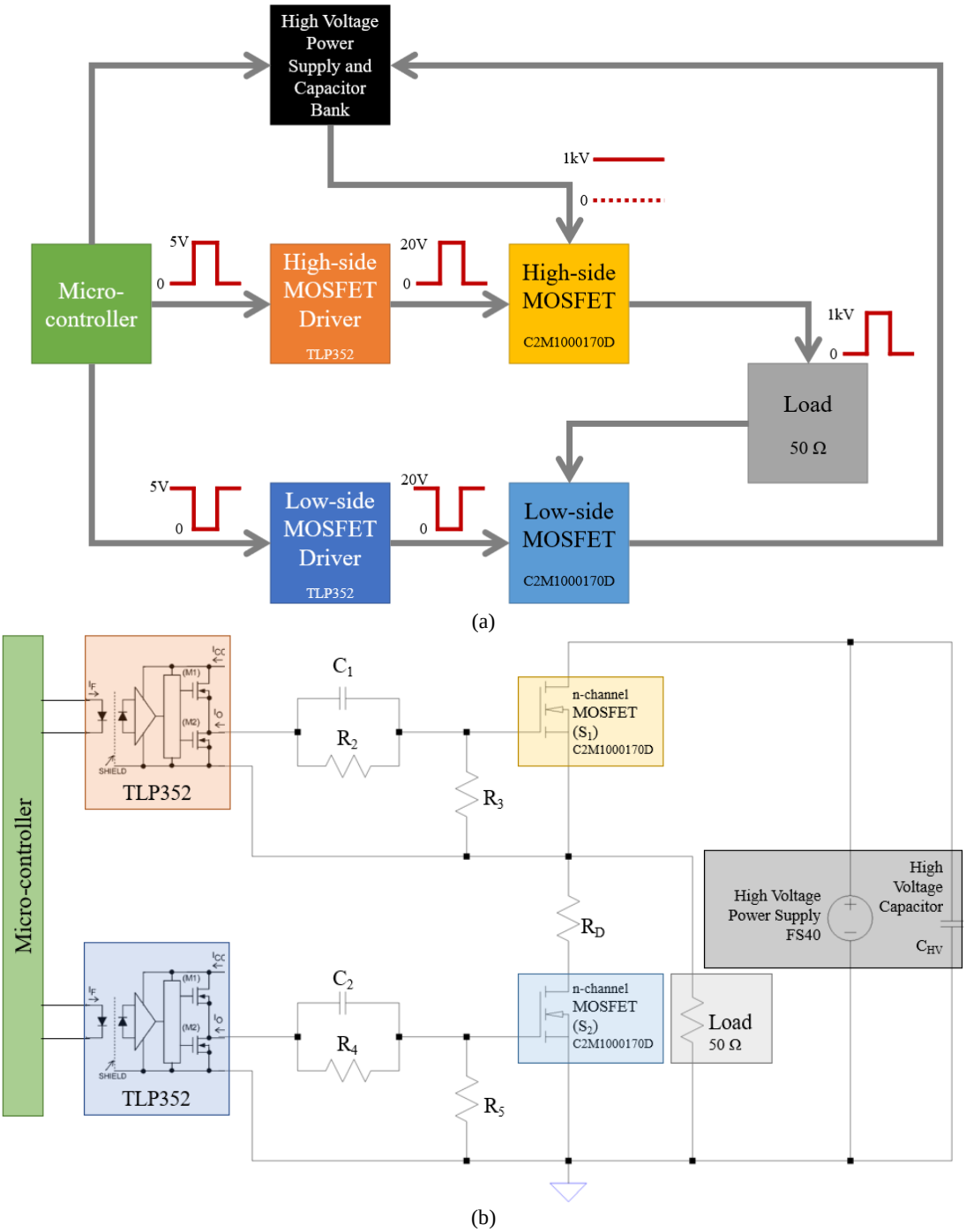


Fig. 3.18. The slow nsPEF electroporation system push-pull configuration (a) block diagram (b) circuit diagram

This switching topology means that when the high side MOSFET (S_1) is open ('OFF') while the low side MOSFET (S_2) is closed ('ON'), and vice versa. The relationship between the two-gate drive

signals to the MOSFETs are synchronized and complementary to one another i.e., active high gate drive signal for the high side MOSFET (S_1) and active low gate drive signal for the low side MOSFET (S_2). Thus, generating high voltage, symmetrical nsPEFs. This arrangement has the potential to produce nsPEFs with a transition time (rise and fall times) of 10.5 ns, as long as the gate drivers can supply sufficient current to charge up the input capacitors of the MOSFETs. This pules current may be in excess of 10 A.

The hardware consists of a C2M1000170D SiC power MOSFET that has an input capacitance (C_{iss}) of 200 pF that must be charged when the device is tuned 'ON' and discharged to turn 'OFF' the device [28]. This power MOSFET was chosen based on the fastest possible switching times, which in turn are determined by the charging and discharging times of the gate-source (C_{gs}) and gate-drain capacitance (C_{gd}) respectively. The charge and discharge times must be as short as possible therefore a gate driver that can provide significant current to charge this capacitance is necessary. Table 3.2. indicate that a 2 A gate current would be required for the efficient switching to produce a nsPEF of 100 ns duration.

For efficient switching, a TOSHIBA TLP352 Photocoupler was selected to operate as a gate driver, that provides the necessary gate current (2.5 A_{max}) to charge and discharge the C_{gs} and C_{gd} efficiently, in addition to providing isolation between the low and high-power circuits [30].

A resistor, R_D, is placed between the high and low side circuitry, as shown in Fig. 3.18. This resistor is inserted to protect the circuits from a failure / open control signal, ensuring a pull-down of the gate signal of the high side MOSFET (S1), turning S1 'OFF', and that the pulse seen at the load is grounded (0V) and not floating. Gate resistors R_2 and R_4 prevent the MOSFETs S_1 and S_2 from high voltage spikes or ringing at the gate-source due to the lead inductance and the input capacitance. R_2 and R_4 reduce the Q of the circuit, where Q is given by $\frac{1}{R}\sqrt{\frac{L}{C}}$. To stop ringing the MOSFET due to the excessive gate-source voltage that may breakdown the gate oxide layer. Capacitors C_1 and C_2 are shunt capacitors at switching and provide a time constant of C_1R_2 and C_2R_4. Resistors R_3 and R_4 are pull-down resistors. In conclusion, implementing a push-pull configuration results in symmetrical shaped PEFs with identical rise and fall times than is possible by implementing a single MOSFET circuit.

Fig. 3.19 is the printed circuit board (PCB) board for the push-pull MOSFET topology and the MOSFET associated gate drive circuitry implemented for the generation of PEFs requirements. In the final configuration, a C2M1000170D, with a maximum drain-source voltage (V_{DSmax}) of 1700 V and a rise time of 10.5 ns, in a push-pull topology was driven by a Toshiba TLP352 photocoupler. The TLP352 photocoupler can produce a gate-source voltage of up to $\pm$ 30 V from a TTL level input signal and can drive a peak current of 2.5 A to efficiently charge and discharge the C2M1000170D input capacitance. Fig. 3.20 shows the high-side and low-side high voltage switching C2M1000170D

MOSFETs and their TLP352 photocoupler driver circuitry. This circuitry is the high voltage PCB circuitry of the slow nsPEF electroporation system for high voltage nsPEF generation.

(a)

(b)

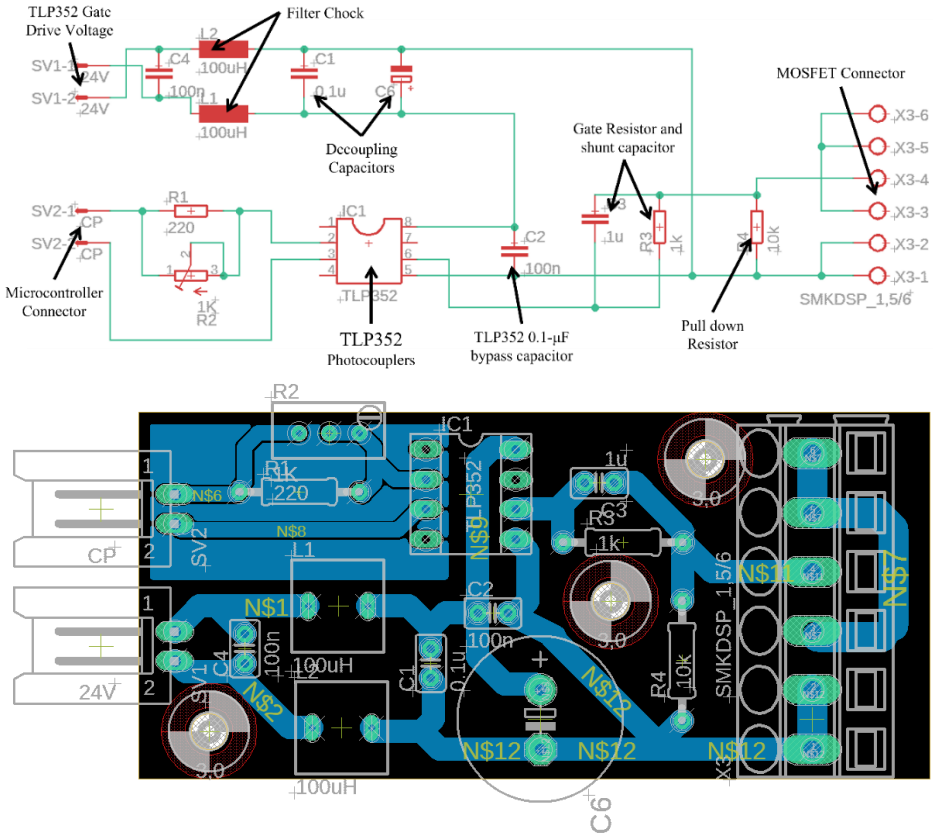


Fig. 3.19. MOSFET and MOSFET driver printed circuit board circuit in Eagle (a) printed circuit board schematic (b) printed circuit board design layout

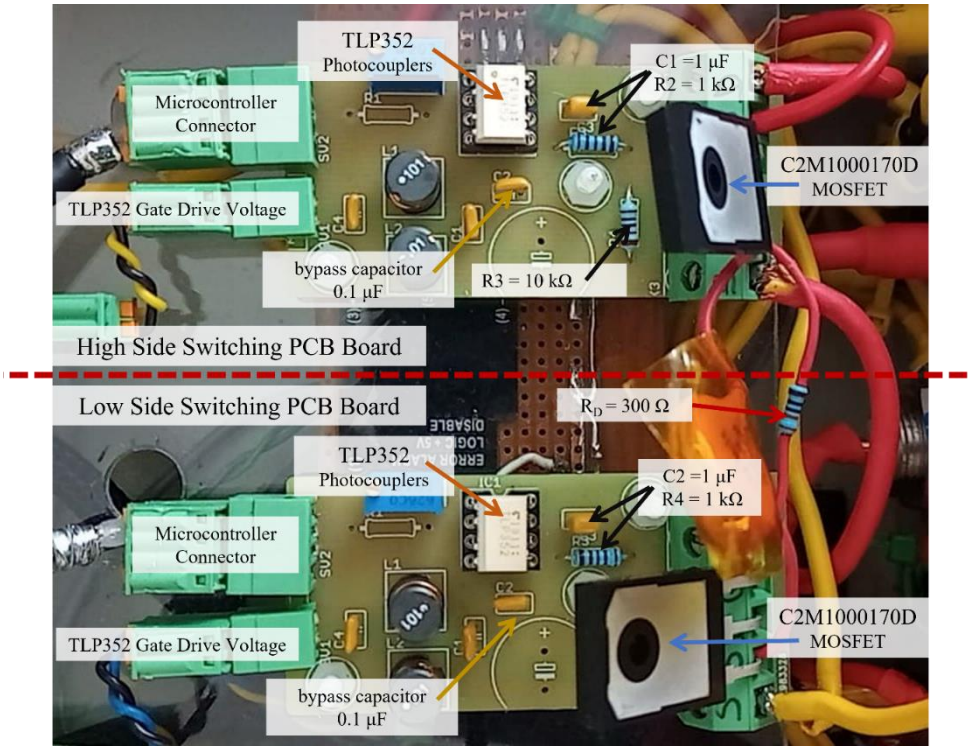


Fig. 3.20. Labelled and populated final high voltage push-pull, high side and low side MOSFET and MOSFET driver printed circuit boards of the slow nsPEF electroporation system

3.4. MOSFET Circuit Power Supply

Gate Drive Power Supply

For a push-pull, half (or full) bridge switching circuit a floating power supply is necessary and the power supplies for the upper and lower driving circuits must be isolated from one another. Fig. 3.21 shows the power supply design used to power the Toshiba optocoupler gate driver to switch the MOSFETs [30]. For the TLP352 photocoupler to successfully drive the C2M1000170D SiC power MOSFET a 20 V to 25 V gate voltage signal is required, and therefore a 20 V to 25 Vdc power supply is required to power the photocoupler.

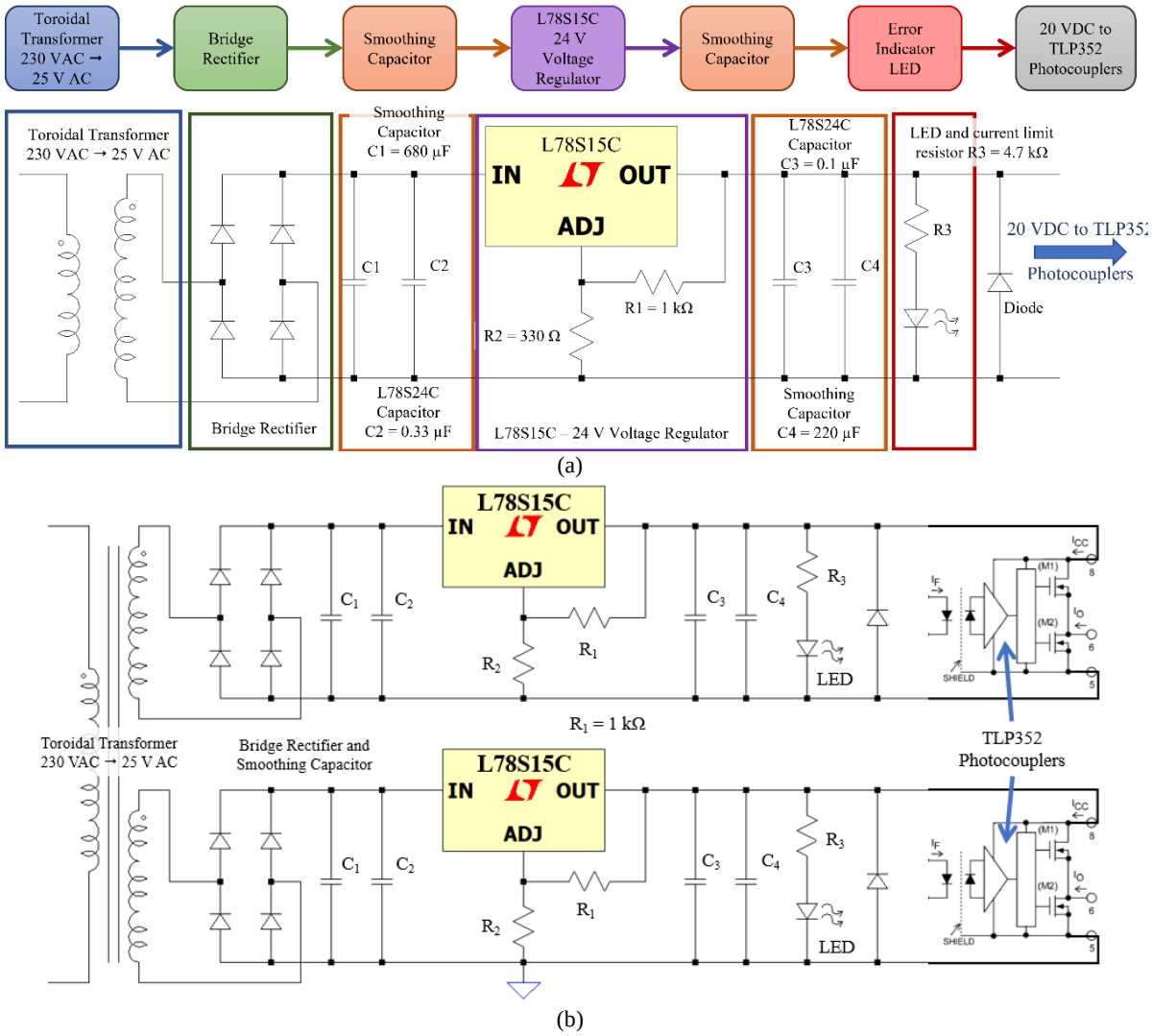


Fig. 3.21. The transformer-isolated power supply design for the TLP352 photocouplers to drive the C2M1000170D MOSFET (a) labelled diagram (b) circuit for high and low side MSOFET diving circuit

The transformer-isolated power supply circuit can be divided into four segments, as shown in Fig. 3.21(a). It compromises of a MOSFET and MOSFET driver, error indicator light-emitting diode (LED), positive voltage regulator and a transformer isolated power supply. The transformer-isolated power supply is based on a forward diode full rectifier and a smoothing capacitor

The gate drive power supply requires to supply a 20 V to 25 V to the TLP352 photocouplers to drive the C2M1000170D SiC power MOSFET. To achieve this a L78S15C regulator [39] was used to regulate the 25 V alternating current (ac) supply from the toroidal transformer with a full bridge rectifier and smoothing capacitor to deliver the necessary dc supply for the TLP352 photocouplers [30]. This circuitry is shown in Fig. 3.21. Although designed primarily as a fixed 24 V voltage regulators, the L78S15C devices can be used with external components to obtain adjustable voltages.

The generator was designed to run from a 230 Vac that is the United Kingdom (UK) mains supply. A toroidal transformer (230 Vac to 25 Vac) followed by a bridge rectifier and smoothing capacitor is used to transform the 230 Vac main input to a 25 Vdc signal with an ac-ripple that has an amplitude determined by the value of capacitors, C_1 as shown in Fig. 3.21. Additionally, it provides isolation between the mains input and the high voltage nsPEF circuitry.

As the L78S15C devices can be used with external components to obtain adjustable voltages and currents through the implementation of two resistors as illustrated in Fig. 3.22. Placing a capacitor on either side of the L78S15C devices improves transient response and is required if the L78S15C regulator is located an appreciable distance from the power supply filter. The recommended capacitor values are 0.33 µF at the device input and a 0.1 µF capacitor at its output [34].

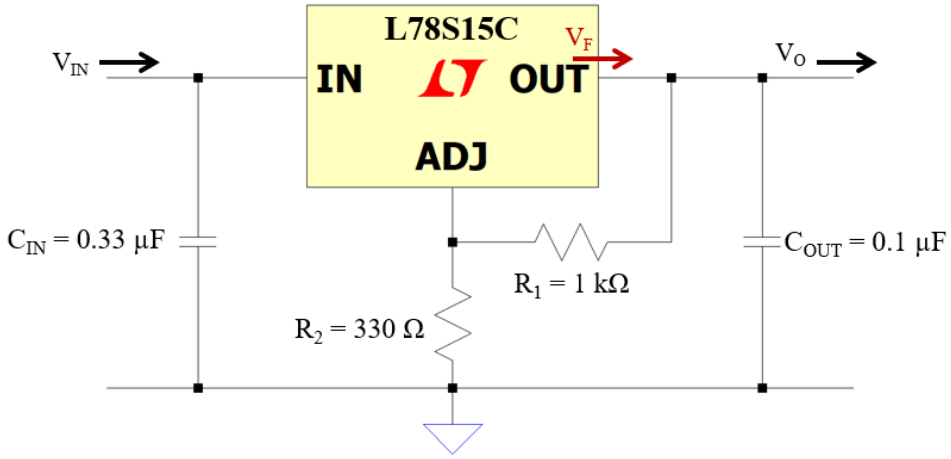


Fig. 3.22 Circuit to adjust the L78S15C voltage output [39]

The relationship between the resistors, R_1 and R_2 in Fig. 3.21 determines the output voltage of the voltage regulator to power the photocoupler to drive the gate MOSFET. The relationship is given by equations (3.3) and (3.4) below:

$$V_0 = V_F + R_2\left(\frac{V_F}{R_1} + I_{Adj}\right) \tag{3.3}$$

$$R_2 = \frac{V_0 - V_F}{\frac{V_F}{R_1} + I_{Adj}} \tag{3.4}$$

where V_0 is the output voltage from the voltage regulator chip and associated circuit, V_F is the output voltage rating of the voltage regulator, that is 15 V from the L78S15C component. I_{Adj} is the adjusting current which is 2.5 mA. For an output voltage (V_0) of 20 V and with R_1 resistor value of 1 kΩ, the required value for R_2 is 330 Ω. Fig. 3.22 shows the circuit for the voltage regulator.

The final section of the gate drive power supply circuit has an error indicator LED with a current limit resistor. For normal operation, the LED is illuminated. If the LED is unlit, it indicates a fault on the MOSFET and MOSFET driver PCB circuit, whether it's the high-side or low-side MOSFET switching circuit PCB (shown in Fig 3.20).

Fig. 3.23 shows the PCB design for the gate drive power supply circuit is shown in Fig. 3.21. This design was also used for the gate drive power supply for the 5 V supply required for the controller and operating the high voltage source of the slow nsPEF electroporation system developed in this work.

The high side driving circuit power supply and the MOSFET driver circuit, shown in Fig. 3.18 and Fig. 3.21 has a 'floating ground'. This floating ground allows the reference voltage between the high side MOSFET gate and source terminal to represent the voltage amplitude of the gate driver signal (20 V to 25 V). If the lower potential side of the high side gate drive power supply was grounded, i.e., not 'floating', the potential between the gate and source terminal of the high side MOSFET would reflect the high voltage amplitude of the generated output pulse. This would result in the breakdown of this MOSFET as its maximum gate-source breakdown voltage would have been exceeded. Therefore, the lower potential side of the high side gate drive power supply is a 'floating ground', and a toroidal transformer is used as illustrated in Fig. 3.21 (b).

5 V Power Supply

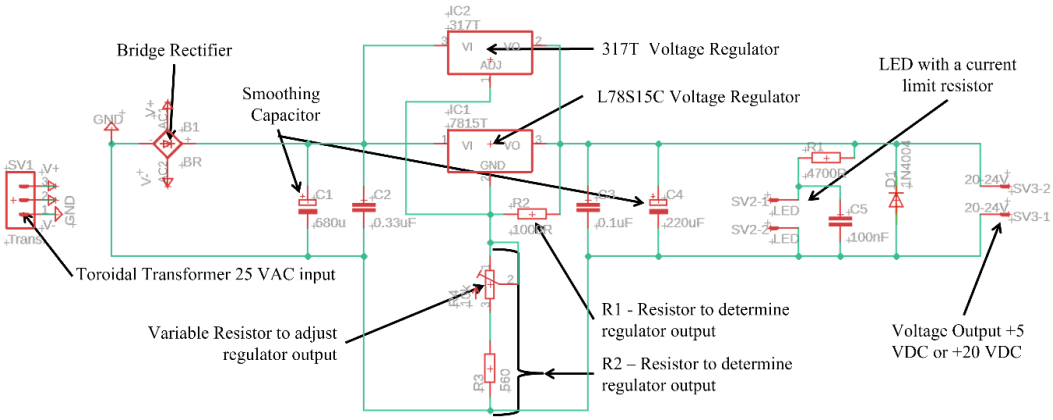
The 5 V power supply powers the microcontroller, the enable/disable and the 5 V input pin for the FS40 isolated, proportional dc to high voltage dc supply. This 5 V power supply PCB uses the same design as the power supply for the gate drive power supply. Its design is a replica of the transformer-isolated power supply design shown in Fig. 3.21 and its PCB circuitry shown in Fig. 3.23. The block diagram for the +5 V supply is given in Fig. 3.24. The same PCB design and circuitry were used here, but the L7805 voltage regulator replaced the L78S15C voltage regulator and alternative capacitor, and resistor values were used for the 5 Vdc supply.

High Voltage Power Supply

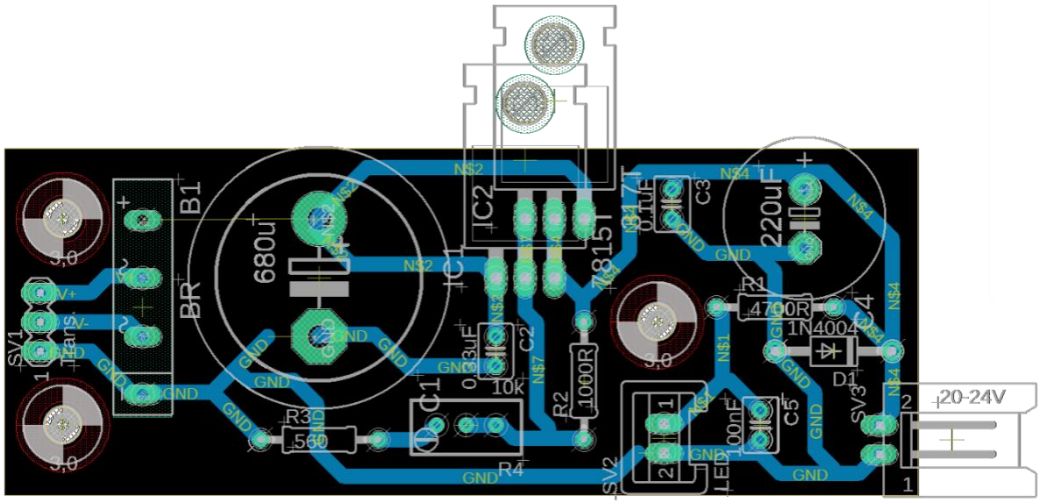
For the generation of high voltage nsPEF the C2M1000170D SiC power MOSFET was configured to switch a high voltage dc source power supply unit with an output that is less than 1700 V. This output voltage was limited to 1700 V because of the C2M1000170D drain-source breakdown voltage rating.

To reduce the possibility of the MOSFET drain-source breakdown voltage being exceeded, the high voltage power supply was limited to 1400 V.

(a)



(b)



(c)

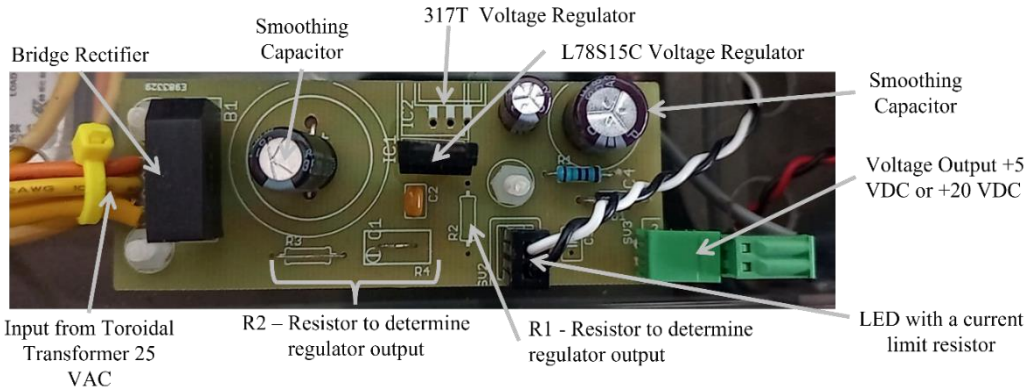


Fig. 3.23. Gate drive power supply circuitry printed circuit board (a) Eagle printed circuit board schematic (b) Eagle printed circuit board design layout (c) populated printed circuit board

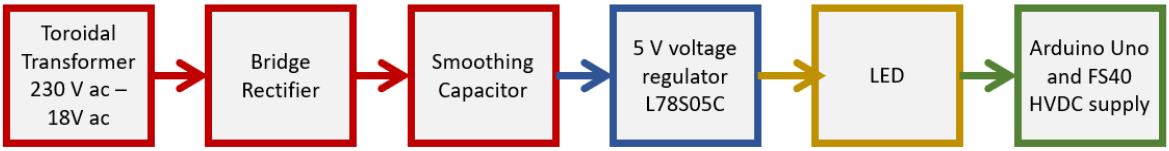


Fig. 3.24. 5 Vdc power supply circuit block diagram

Table 3.4 shows the power supply requirements necessary to provide sufficient current for the nsPEF required for this work to be achieved (generation of fifty 300 ns PEF per second (50 Hz repetition frequency). For the generation of 1400 V nsPEF across a 50 Ω load impedance a dc power supply unit (PSU) of 39.2 kW and 28 A is required (see equation 3.3). The high voltage PSU is pulsed for a maximum duration of 300 ns that is generated every 20 ms seconds (50 Hz). Therefore, we can calculate the power supply requirement by considering the average time the nsPEFs will be generated. Looking at the pulse parameters required, the maximum average time the nsPEFs will be generated is 15 µs per second. This is the maximum pulse width (300 ns) multiplied by the number of pulses generated per second (50 Hz). Therefore, for the generation of 1400 V amplitude pulses across a 50 Ω load impedance a power supply of 0.6 W and 420 µA would suffice.

Table 3.4. High voltage power supply requirements

Power supply parameter		Value	Unit
Direct current (dc)	Voltage, V_{DC}	1400	V
	Current, I_{DC}	$28\ \left(\frac{P_{DC}}{V_{DC}} = \frac{39200}{1400}\right)$	I
	Power, P_{DC}	$39{,}200\ \left(\frac{{V_{DC}}^2}{Z} = \frac{1400^2}{50}\right)$	W
	Load, Z	50	Ω
Pulse width		300	ns
Repetition frequency, f		50	Hz
Average	Voltage, V_{Av}	1400	V
	Current, I_{Av}	420 ($I_{DC}ft = 28$ x 300n x 50)	µA
	Power, P_{Av}	0.6 ($P_{DC}ft =$ 39200 x 300n x 50)	W
Capacitor, C		597	nF

$$P_{DC} = V_{DC}I_{DC} = \frac{{V_{DC}}^2}{Z_L} \quad \text{(dc)} \qquad (3.5)$$

$$I_{Av} = I_{DC}ft$$
$$P_{Av} = P_{DC}ft = V_{DC}I_{Av} = V_{DC}I_{DC}ft \quad \text{(Average)} \qquad (3.6)$$

Where V_{dc} is dc voltage, I_{dc} is dc current, I_{Av} is the average current, P_{dc} is the dc power, P_{Av} is the average power, *f* is repetition frequency, t is the pulse duration/width and Z_L is the load impedance. In this instant Z_L is 50 Ω.

It is required to add a capacitor across the power supply to replenish the power supply or charge it back up to 1400 V in 19.9997 ms. Since the average current available from the power supply is 420 µA, there is a need to replenish to 1400 V in 19.9997 µs. If the maximum drop in the voltage was 1% i.e., 14 V (ΔV). Assuming the voltage drop is exponential as illustrated by the equation below:

$$V = V_{DC}e^{\frac{t}{\tau}} = V_{DC}e^{\frac{t}{Z_L C}} \qquad (3.7)$$

were V_{dc} is the voltage output of the high voltage power supply, in this case, 1400 V. V is 1386 V ($V - \Delta V$) the voltage of the pulse following a 1% voltage drop, t is the nsPEF duration, which is 300 ns in this instance, and τ is the time constant that is the multiplication of the load impedance, Z_L, and the capacitance across the power supply, C. This effect is illustrated in Fig. 3.25. Rearranging equation (3.7) the value of the capacitor to limit the voltage drop to 1 % can be calculated by equation (3.8). $\frac{V}{V_{DC}} = \frac{1386}{1400} = e^{\frac{t}{Z_L C}}$.

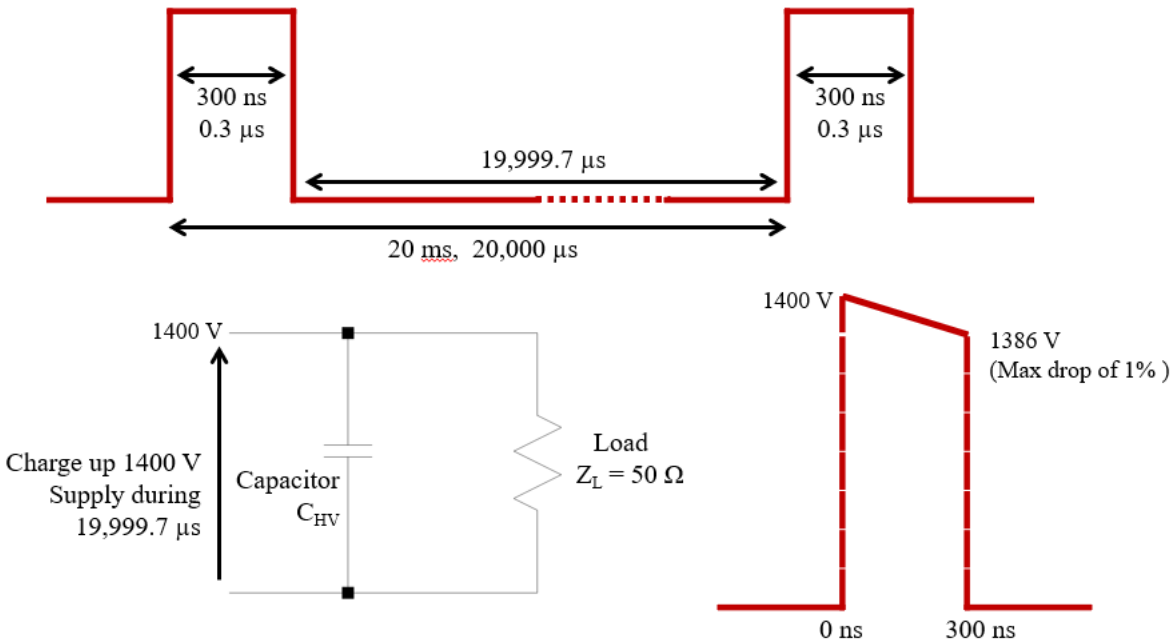


Fig. 3.25. Illustration of the function of a high voltage capacitor across the power supply to replenish the power supply

$$\ln\left(\frac{V}{V_{DC}}\right) = \frac{t}{Z_L C}$$

$$C = \frac{t}{Z_L \ln\left(\frac{V}{V_{DC}}\right)} \quad (3.8)$$

where C capacitance required to limit the voltage drop across the power supply to 1 % and replenish the power supply. The capacitance in this instant is 597 nF.

$$C = \frac{t}{Z_L \ln\left(\frac{V}{V_{DC}}\right)} = \frac{300\text{x}10^{-9}}{50 \ln\left(\frac{1386}{1400}\right)} = 596.99\ nF$$

Following exploration of various high voltage power supplies, the XP-Power 10 W FS40 isolated proportional dc to high voltage dc converter was identified as an acceptable power supply (see the datasheet for FS40 in Appendix IV [40]). The output voltage is proportional to the input voltage, from turn-on to maximum output voltage, enabling easy control of the high voltage supply rail. For this power supply, the maximum output voltage is 4 kV, and the maximum current is 2.5 mA since 2.5 mA is available during the replenishment phase.

The FS40 also has an internal input over-voltage, over-temperature protection, and a TTL enable/disable function. The protection circuits are powered by the +5 V logic input voltage, and a TTL high signal disables the high voltage output [40].

The relationship between the low voltage input and the high voltage output is linear. A 12 V input produces a 4 kV output, and a 6 V input produces a 2 kV output. For the output of the FS40 to be limited to 1.4 kV, the input voltage was limited to 4.2 V.

$$\text{Input voltage } 12\text{ V} = 100\% = 4\text{kV output voltage}$$

$$\frac{1.4\text{kV}}{4\text{kV}} = 35\%, \quad \therefore 12\text{ V} * 0.35 = 4.2\text{ V}$$

The power supply for the FS40 is a replica of the 5 V (Fig. 3.24) and gate drive power supply (Fig. 3.21). The only difference in the circuit is the inclusion of a potentiometer that determines the output voltage of the FS40.

In Fig. 3.26 the value for R_1 is 330 Ω, R_2 is a 1 kΩ potentiometer and R_3 is 91 Ω (made of two 47 Ω resistors). These values were determined using equations (3.5) and (3.6).

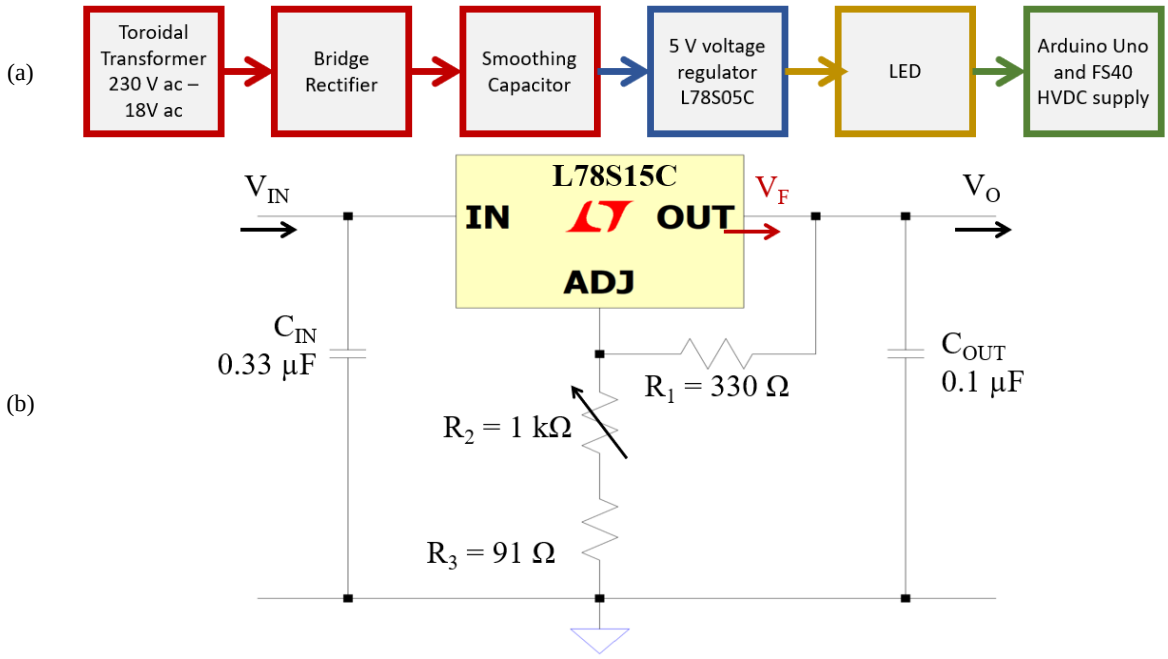


Fig. 3.26. FS40 high voltage power supply input supply circuit to limit the output to 4.3 V (a) block diagram design (b) circuit design

Printed circuit board layouts and designs

The PCBs produced for the slow PEF electroporation system were designed using Eagle PCB layout [41] and the boards were fabricated by Eurocircuits [42]. For high-speed and high-frequency operation, components were placed as close to each other as possible, thus limiting parasitic/stray inductance and capacitance. Surface mounted components were also used wherever possible to reduce parasitic/stray inductance and capacitance as well as electromagnetic (EM) crosstalk [43]-[45]. EM

crosstalk is the interference caused by electromagnetic signals affecting other parts of the systemPower supply rails were decoupled from noise using a combination of low-value ceramic and high-value electrolytic capacitors arranged in parallel. At low frequencies, a large value capacitor offers a low impedance to the ground, but the capacitor's quality diminishes once when self-resonance is reached, and the capacitor becomes inductive. Thus, multiple capacitors maintaining a low impedance path to the ground in a wide range of frequencies were implemented to ensure unwanted noise does not cause interference on control lines [43]-[45].

Effective shielding was also an important consideration to minimise capacitively coupled noise and acts between the high voltage and low voltage sections of the PCB as a Faraday cage to reduce electrical noise from affecting the control signals, and to reduce interference [43]-[45].

3.5. Bill of Material

As discussed, the modular design is based on a push-pull switch configuration using two Wolfspeed's C2M1000170D SiC MOSFET [28] that are directly driven by Toshiba's TLP352 photocoupler [30] to switch a 1.4 kV from a FS40 [40] high voltage power supply unit.

The controllable 0 to 1400 V dc supply was implemented using the XP-Powers FS40 isolated proportional dc to HV dc supply [40]. To assist the high voltage PSU to supply current for the MOSFET switching for the generation of nsPEF a high voltage capacitor with a capacitance of 1 μF was placed in parallel with the high voltage dc supply.

Table 3.5 shows the bill of the material (BoM) for the key components used to implement the final push-pull-based design.

Table 3.5 Bill of material for the final slow nanosecond pulsed electric field electroporation system (at time of design 2017)

Component	***Distributor***	***Stock No.***	***Cost per Unit (£)***	***Quantity***
C2M1000170D SiC n-Channel MOSFET	RS Components	904-7345	4.07	2
Toshiba, TLP352 Opto-coupler	RS Components	796-5190	0.98	2
XPPower FS40 HVdc-voltage Converter	RS Components	123-8405	130.04	1
1μF Polypropylene Capacitor	RS Components	825-1486	2.67	1
			Total Cost	**£ 142.81**

The C2M1000170D power MOSFETs were selected due to their maximum rating to generate the nsPEF required (maximum rating: breakdown voltage of 1.7 kV, capability to produce pulse durations between 100 ns to 300 ns and 10.5 ns rise-time) [28]. Toshiba's TLP352 photocouplers [30] were selected to produce the effective gate voltage swing and high current level for efficient switching of the

C2M1000170D power MOSFETs to produce acceptable transition times. The FS40 power supply was chosen to supply sufficient voltage for the generation of the required nsPEF (100 ns to 300 ns PEFs with amplitude in excess of 1 kV) across a 50 Ω load impedance. A 1µF polypropylene capacitor was connected across the power supply to enable the high pulsed current to be delivered for a selected duration of time, as discussed. All critical components identified in Table 3.5 were selected due to their performance, maximum ratings, availability and cost. Table 3.5 highlights that the overall BoM for the critical electronic components was £142.81. Where 90 % of the cost is accounted for by the XP Power PSU [40].

3.6. Simulation

LTSpice simulation package was used to verify the push-pull design of the slow nsPEF electroporation system [46]-[47]. LTSpice can mathematically predict the behaviour and interaction of the critical components in the circuit by making use of spice models developed by manufacturers [48].

The LTSpice circuit is shown in Fig. 3.27, which is based on the circuit shown in Fig. 3.18. For a more representable simulation of the modular design in Fig. 3.27, a spice model of the C2M1000170D SiC MOSFET was obtained from Wolfspeed's website and utilised [48]. There were no spice models available for Toshiba's TLP352 Photocouplers. Therefore, the outputs generated from the TLP352 were replaced by an LTSpice voltage source with parameters resembling the TLP352 output. These were a 25 V square wave output of a specific duration (100 ns to 300 ns) and period (1 second to 0.02 second, or 1 Hz to 50 Hz).

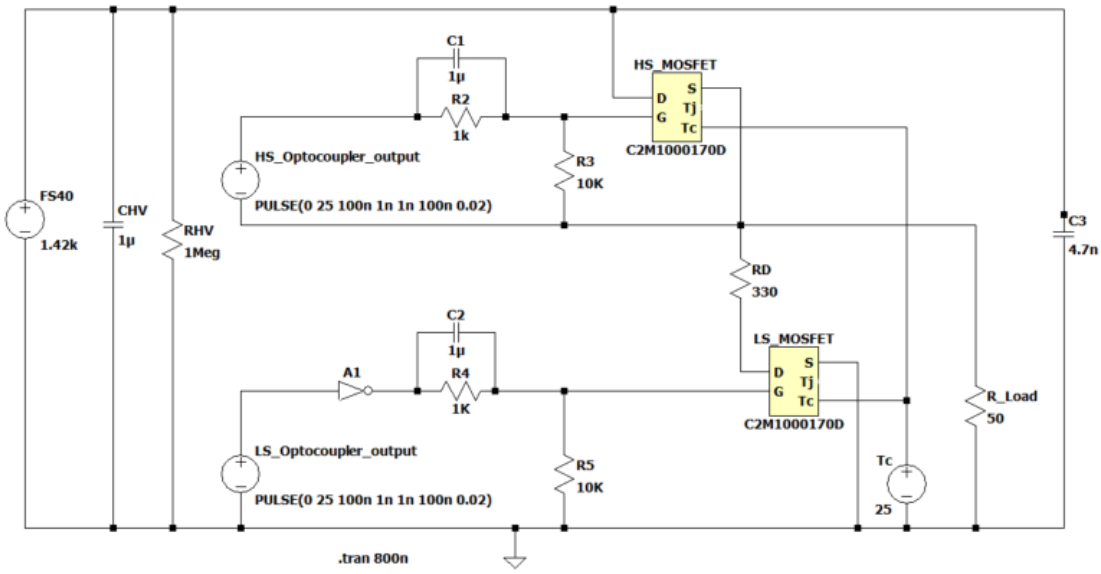


Fig. 3.27. LTSpice circuit of the push-pull design of the slow nanosecond pulsed electric field electroporation system

Fig. 3.28 shows the simulated results of the nsPEF across a 50 Ω load impedance from the circuit shown in Fig. 3.27. The results indicate that this design and using the C2M1000170D SiC MOSFET would generate a nsPEF of 100 ns duration with amplitude in excess of 1 kV. Both the high- and low-level MOSFETs are driven by a complementary 100 ns pulse width control signal of 25 V amplitude

into the MOSFETs gate terminals. This first simulation result indicates that this modular design is capable of delivering the required nsPEF specification for the generator highlighted in Section 3.1.

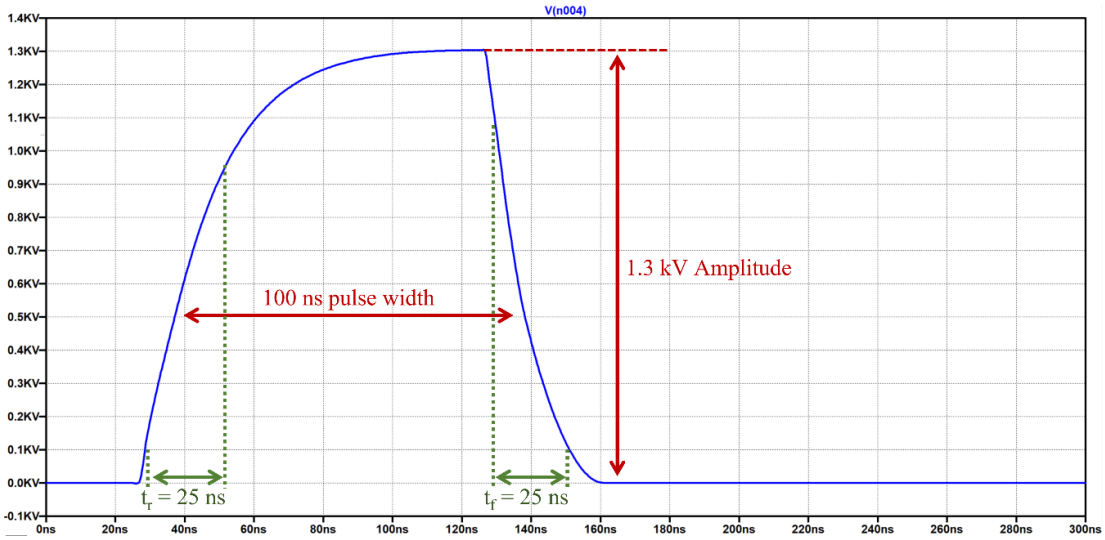


Fig. 3.28. Resulting LTSpice waveform observed of a 100 ns pulsed electric field across a 50 Ω load impedance

The higher the gate signal current the faster the input capacitance of the MOSFET can be charged and discharged $\left(\frac{dV}{dt} = \frac{i}{C}\right)$. This results in faster and more efficient switching of the MOSFET. Fig. 3.29 emphasises this effect. Fig. 3.29(b) and (c) demonstrates that a higher gate drive currents into the high side MOSFET, of 650 mA with a gate-source voltage of 25 V rather than a 400 mA with a gate-source voltage of 15 V, increases the amplitude of the nsPEF across the 50 Ω load impedance by 600 V (Fig. 3.29(a)). With a 650 mA gate drive current a 1.3kV 100 ns PEF across a 50 Ω load impedance was observed in comparison to a 1 kV and 700 V 100 ns PEF across 50 Ω load impedance with a gate drive current of 500 mA and 400 mA respectively.

Fig. 3.30 illustrates the 100 ns PEF measured across various load impedance of 10 Ω, 50 Ω, 100 Ω and 300 Ω. This figure shows that the design is sensitive to load variation as the amplitude of the nsPEF is reduced with lower value load impedances. A low voltage of ~420 V is observed across a 10 Ω load ($R_{\_Load}$) whilst a voltage of 1.4 kV is observed across a 300 Ω load ($R_{\_Load}$). This feature relates to the drain-source on-state resistance of the MOSFET. With a relatively high drain-source on-state resistance, $R_{DS(on)}$, and a low load impedance the effect of $R_{DS(on)}$ is significant since the total resistance is $R_{DS(on)} + R_{\_Load}$. If $R_{DS(on)}$ and $R_{\_Load}$ are the same, then half the voltage will be dropped across $R_{DS(on)}$ and the amplitude of the nsPEF will be halved. This is described as a potential divider, where: nsPEF amplitude, $V_L = \frac{R_{\_Load}}{R_{DS(on)}R_{\_Load}} V_{cc} = \frac{Z_L}{R_{DS(on)}Z_L} V_{cc}$.

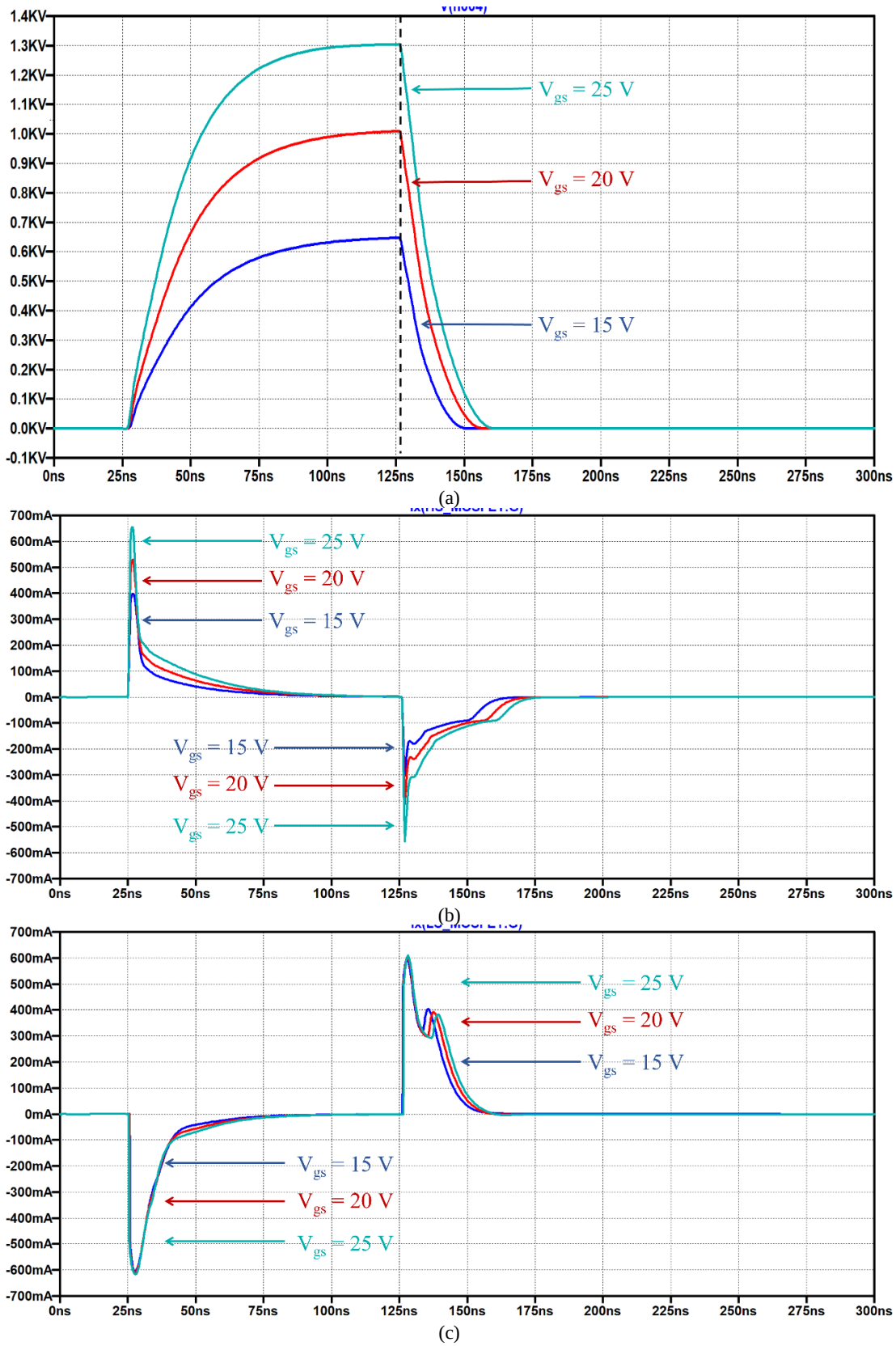


Fig. 3.29. (a) nsPEF across the 50 Ω load impedance (b) Current through the high side MOSFET gate terminal. (c) Current through the low side MOSFET gate terminal, with a gate-source voltage of 15 V (blue), 20 V (red) and 25 V (teal)

The sensitivity to lower impedance load could be solved by selecting a MOSFET with a lower $R_{DS(on)}$. At the time of designing this slow nsPEF electroporation system, the C2M1000170D SiC

MOSFET was the most suitable device available due to its high breakdown voltage (BV_{DS}) of 1700 V and fast rise times of 10.5 ns with relatively low drain-source ON-resistance.

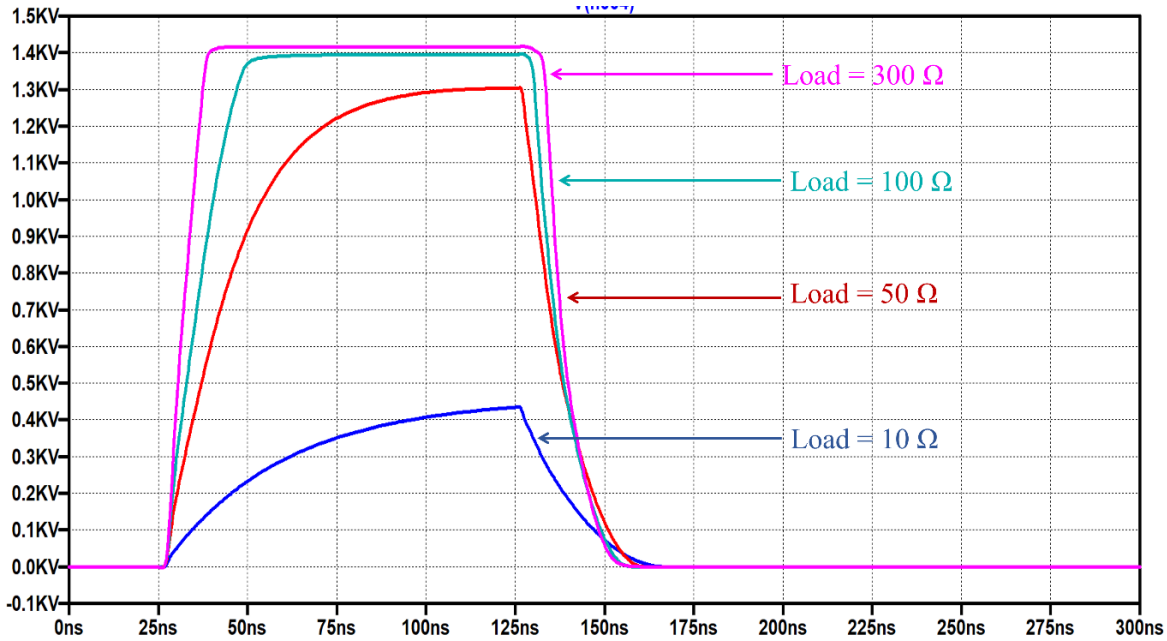


Fig. 3.30. 100 ns pulsed electric field across a load impedance of 10 Ω (blue), 50 Ω (red), 100 Ω (teal) and 300 Ω (pink) with a 1.4 kV high voltage power supply

It should be noted that pulse generation at the highest repetition rates will require a higher value of capacitance across the power supply to enable a high pulse count to be delivered to preserve the pulse amplitude dropping more than 1 %.

In conclusion, the simulation indicates that the design of the slow nsPEF electroporation system could produce 100 ns to 300 ns PEF of amplitude in excess of 1 kV across a 50 Ω load impedance. Thus, meeting the systems requirement. Additionally, the simulation results indicate that the design was optimised to deliver 100 ns to 300 ns PEF of amplitude in excess of 1 kV into bulk tissue (estimated to have an impedance of 300 Ω) at the time of designing and developing the pulser.

Fig. 3.31 shows that the design can produce a wide variety of nsPEF duration pulses across a 50 Ω load impedance from 100 ns to 1 µs duration. All nsPEFs produced have identical rise time and fall times of approximately 25 ns and an amplitude of approximately 1.3 kV. Fig. 3.32 demonstrates that the design can produce identical 1.3 kV 100 ns PEF with identical rise and fall times with a wide range at a pulse repetition frequency from 1 Hz to 1 kHz.

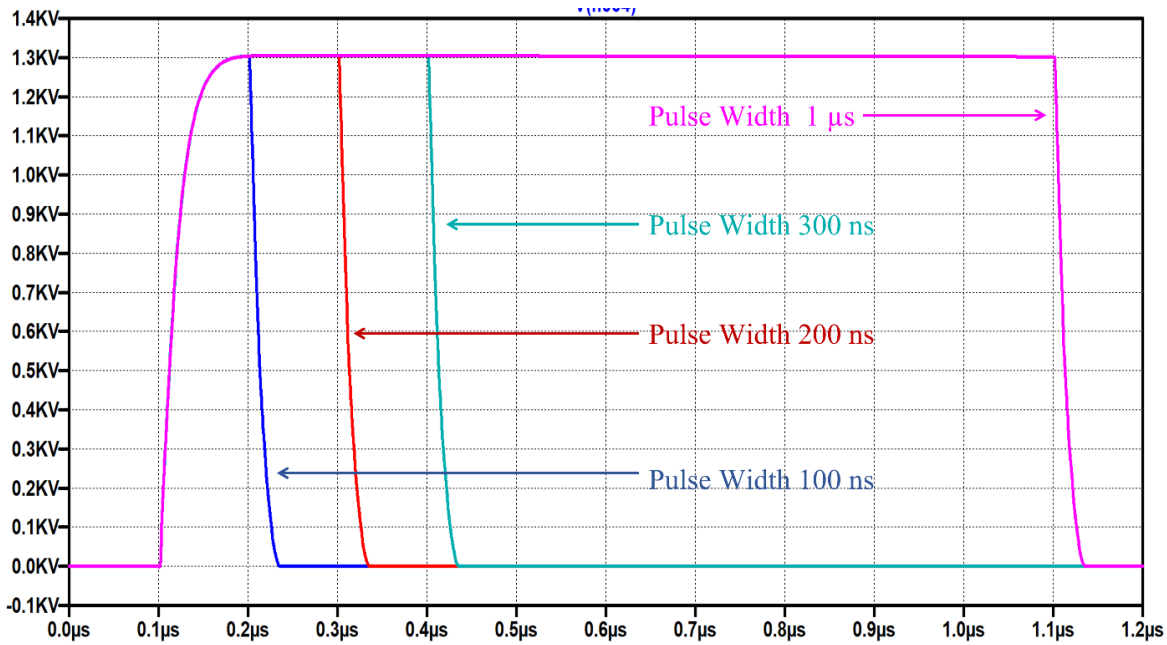


Fig. 3.31. Simulated pulses observed across a 50 Ω load impedance with a gate-source drive signal durations of 100 ns (blue), 200 ns (red), 300 ns (teal) and 1 µs (pink)

The simulation results (Fig. 3.28 to Fig. 3.32) confirm that the design based on two C2M1000170D SiC MOSFET in a push-pull configuration can meet the requirement set for the nanosecond electroporation system. The requirement is the ability to generate a specific number of PEF of 100 ns to 300 ns in duration with amplitude in excess of 1 kV at a repletion frequency of 1 to 50 Hz across a 50 Ω load impedance.

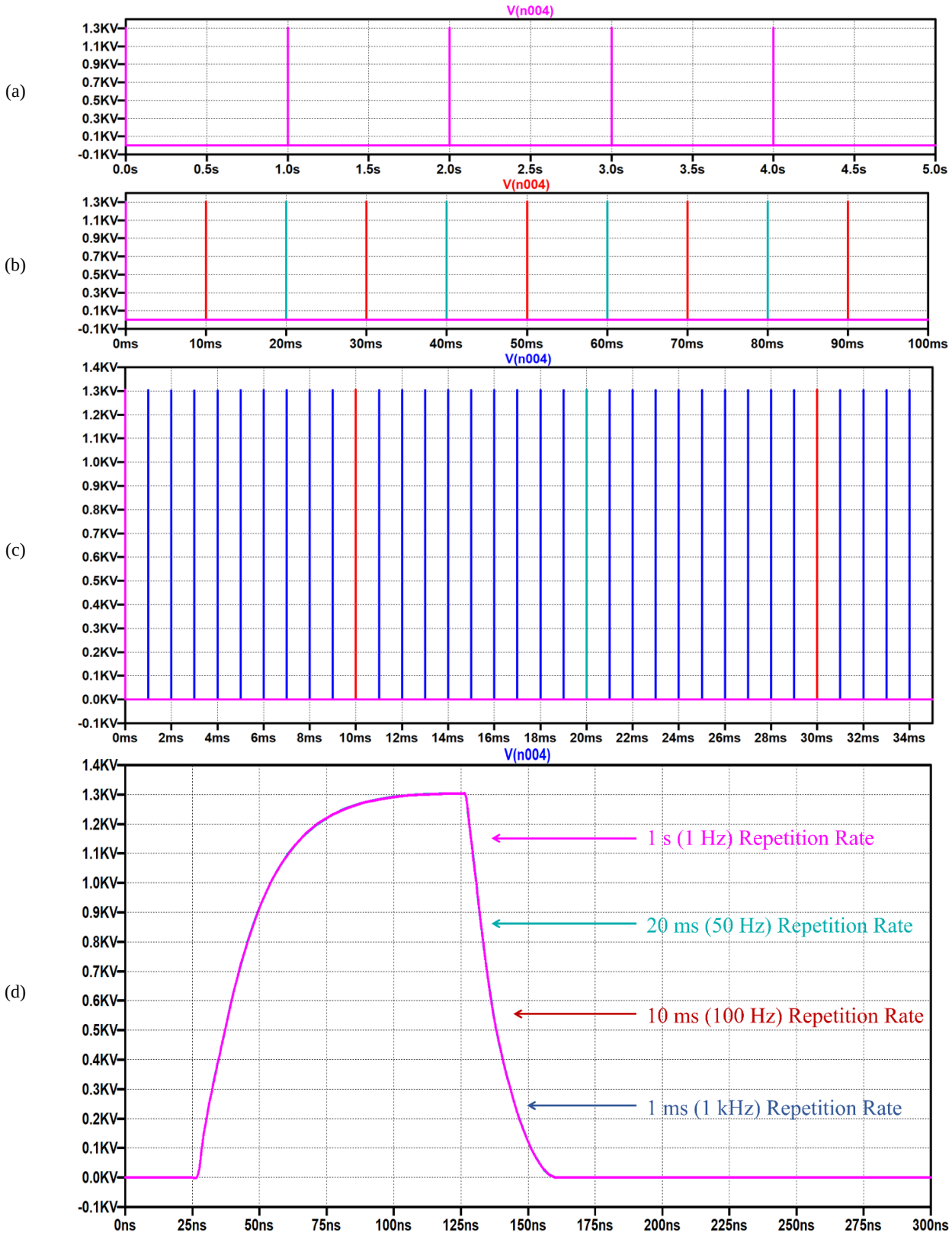


Fig. 3.32. The nanosecond pulsed electric field generated across a 50 Ω load impedance with a repetition rate (frequency) of 1 ms (1 kHz, blue), 10 ms (100 Hz, red) and 20 ms (50 Hz, teal) and 1s (Hz, pink) (a) 0.5 s per division (b) 10 ms per division (c) 2 ms per division (d) 25 ns per division

3.7. Electrical Verification and Validation

Following successful validation of the final circuit design through simulation, the final PCBs and circuitry were assembled, and the slow nsPEF electroporation system was built. The nsPEF generator was constructed of eight separate PCB boards that consisted of the push-pull circuit, the gate driver PCBs for the high and low-side MOSFET, the four voltage power supply PCBs, the microcontroller and high voltage FS40 PCBs, as shown in Fig. 3.33.

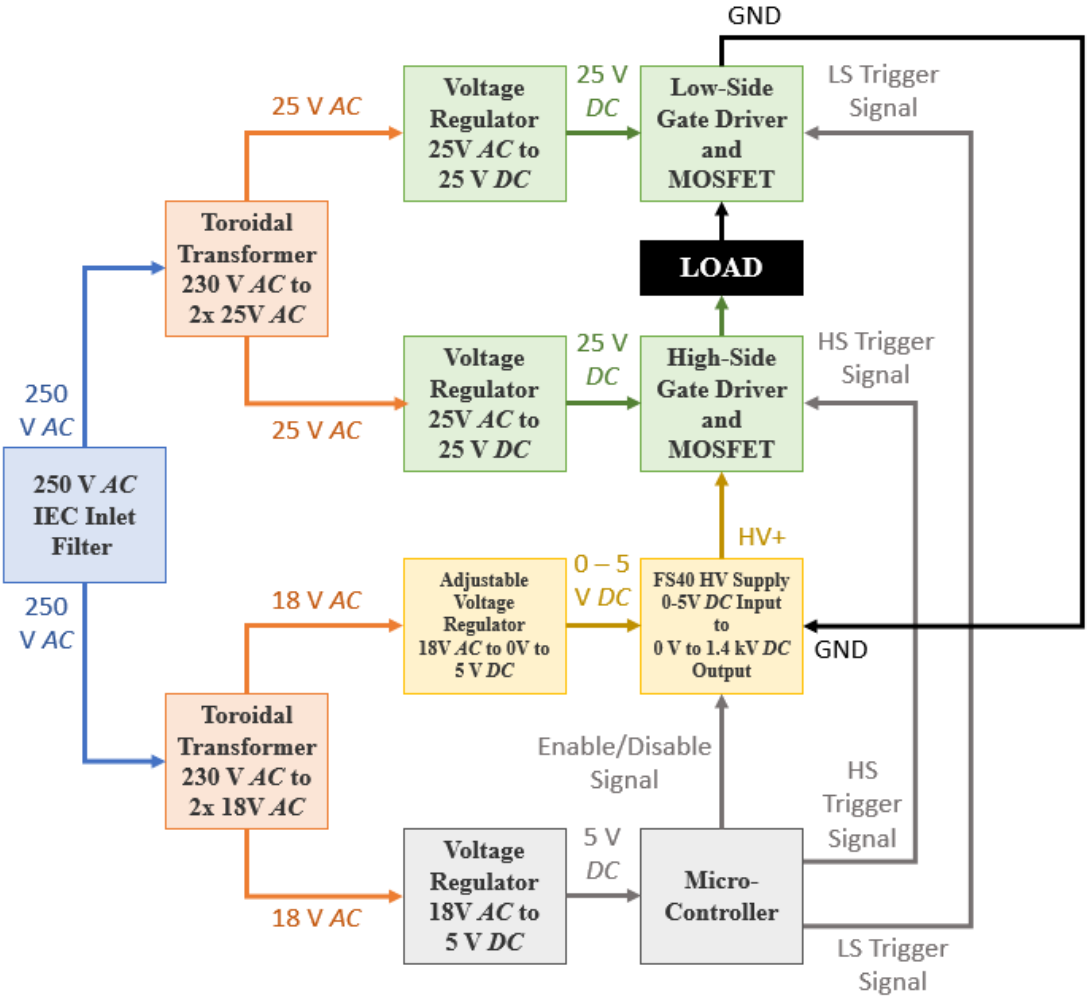


Fig. 3.33. Block diagram of the circuit subsections/printed circuit boards of the slow nsPEF electroporation system

Electrical verification and validation (V&V) were performed to ensure that the developed slow nsPEF electroporation system meets the electrical requirements outlined in Section 3.1. At the highest level, the specification requires the generator to produce a specific number of PEF of 100 ns to 300 ns in duration with amplitude in excess of 1 kV at a repletion frequency of 1 to 50 Hz across a 50 Ω load impedance.

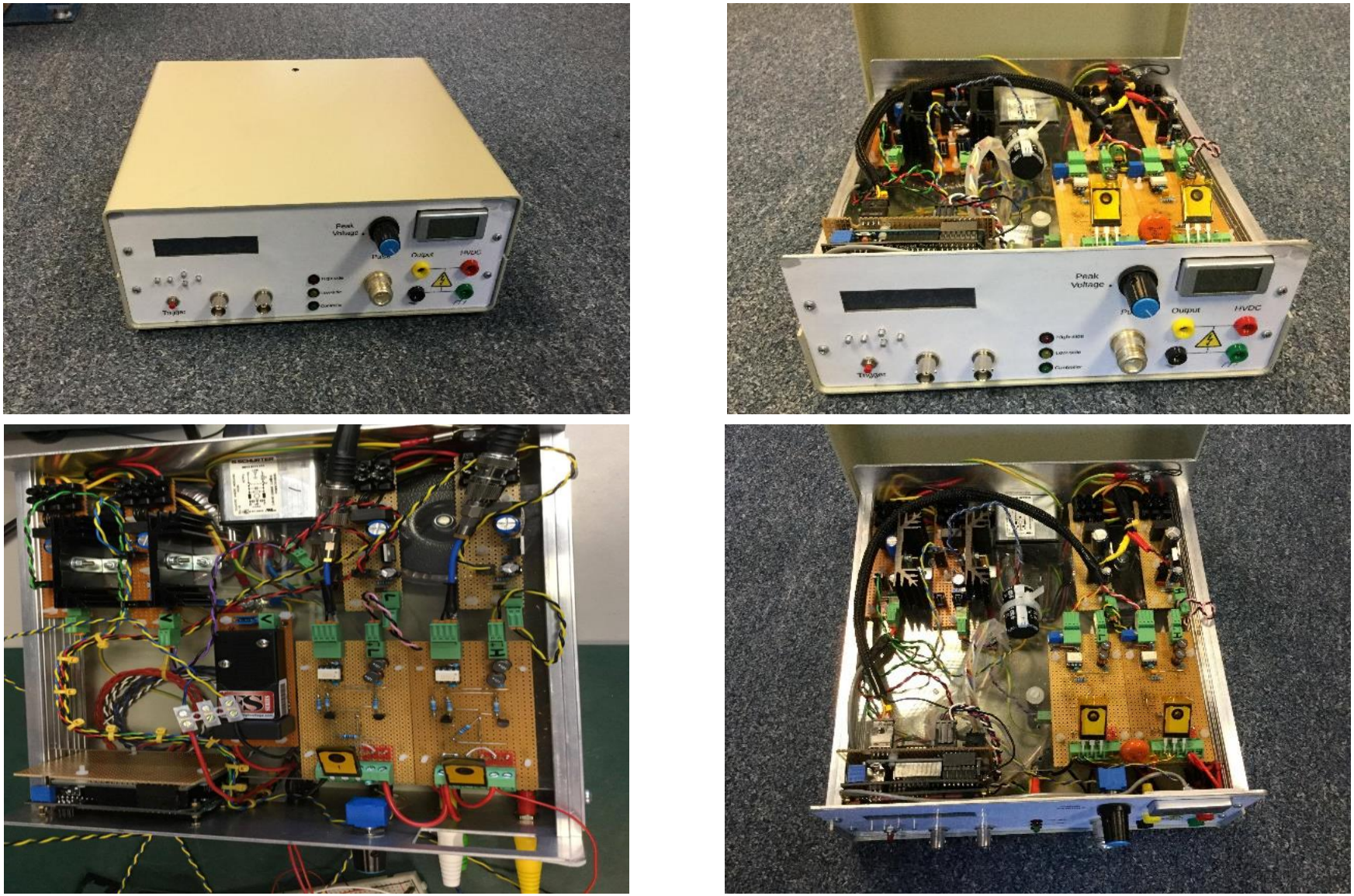


Fig. 3.34 The final comstructed slow nanoseond pulsed electric field electroporation system

3.7.1. Simulation vs Measurements

Following the simulations of a modular design using LTSpice, the slow nsPEF electroporation system was developed, and its performance was compared. The final slow nsPEF electroporation system assembled is shown in Fig. 3.34.

Fig. 3.35(a) demonstrates the assembled nsPEF generator is capable of generating a 1 kV, 100 ns PEF that meet and excels the set pulse parameters set out at the beginning of Section 3.1. Fig. 3.35(b) demonstrates that the constructed nsPEF generator performance exceeds the LTSpice simulation in terms of the pulse rise time when generating a 100 ns PEF across a 50 Ω load impedance. The measured pulse across the 50 Ω resistive load is more symmetrical, in terms of rise and fall times, and has a faster pulse rise-time than predicted in simulation results. This could be the result of a higher gate current in practice, thus, resulting in faster charging of the internal gate capacitance and therefore more efficient switching of said C2M1000170D SiC MOSFETs.

(a)

(b)

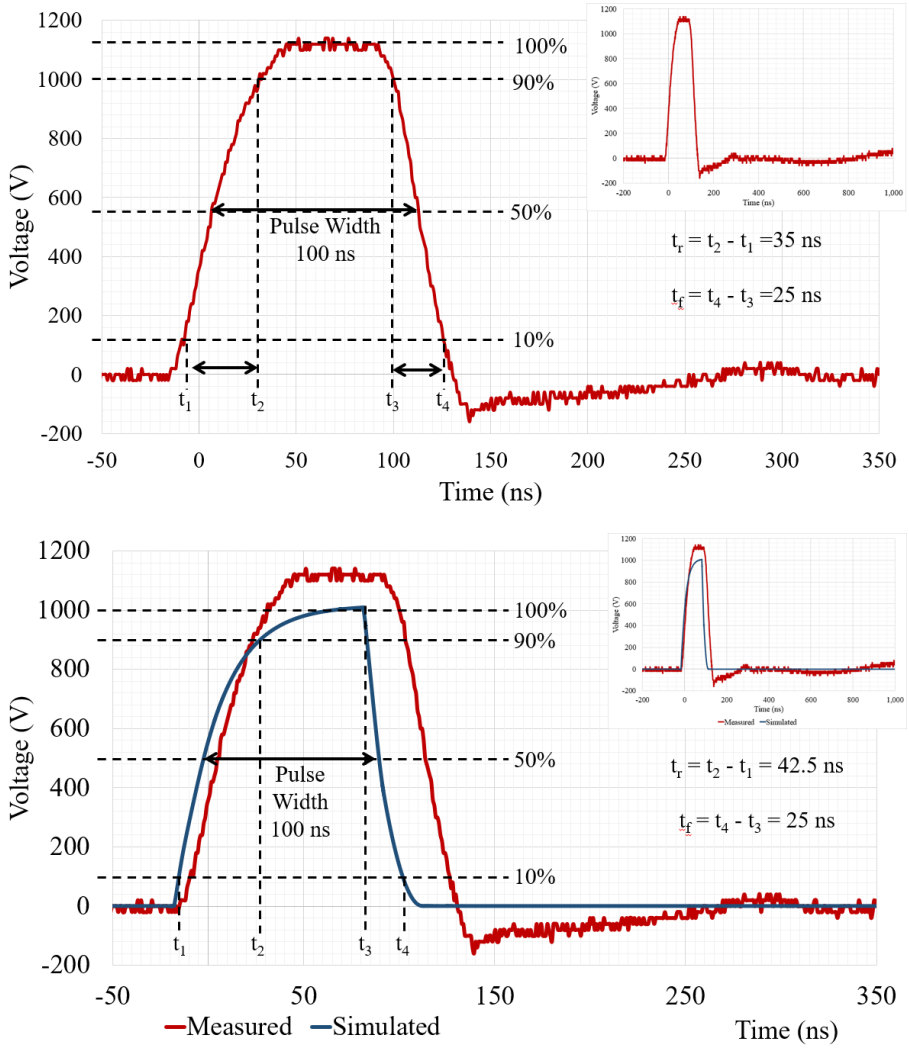
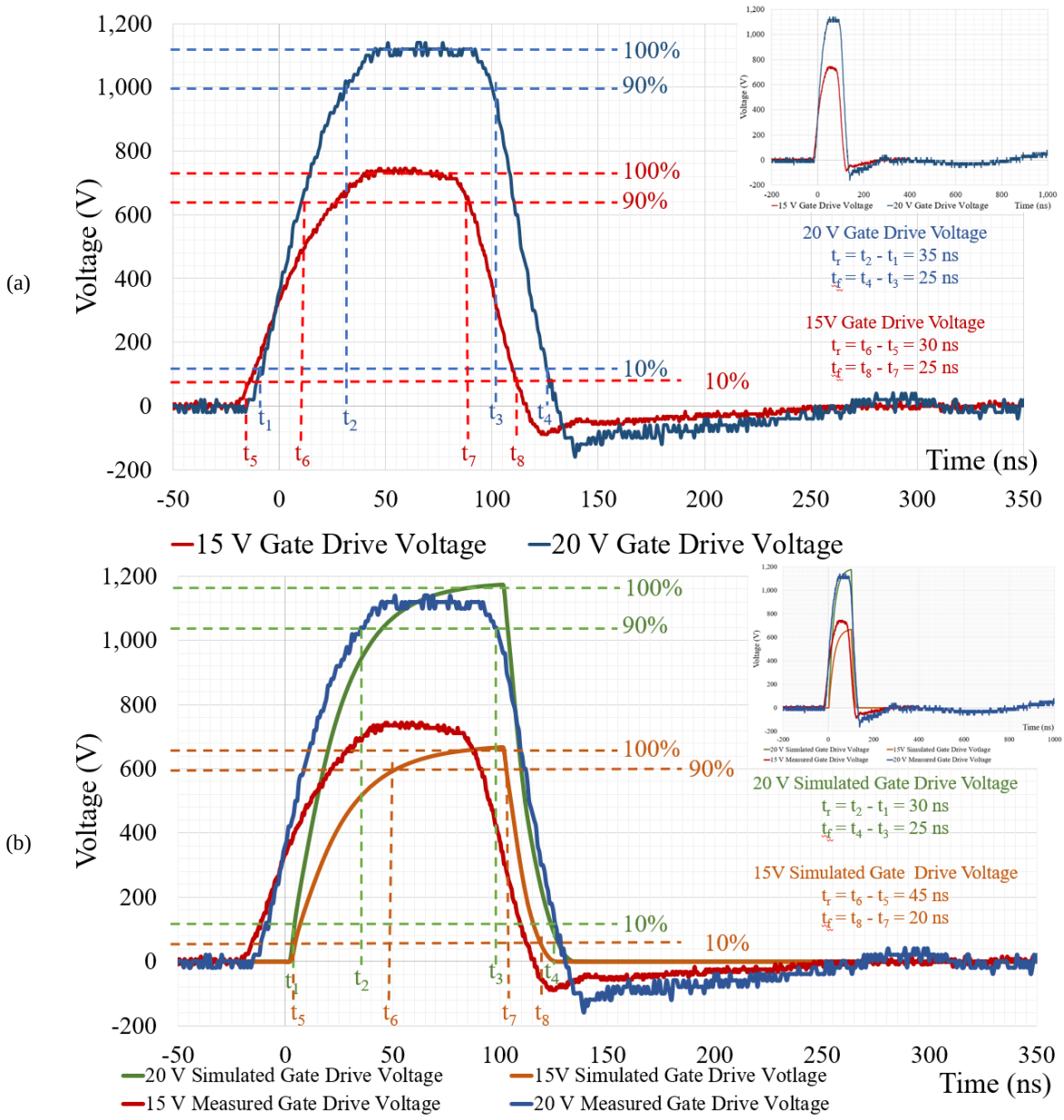


Fig. 3.35. (a) Measured 100 ns pulsed electric field waveform across a 50 Ω load impedance (b) Measured 100 ns pulsed electric field waveform overlayed with the simulation of a 100 ns pulsed electric field LTSpice waveform

3.7.2. Variation in Gate Drive Voltage

Fig. 3.36 indicates that with a higher gate-source voltage, the amplitude of the PEF across the 50 Ω load impedance is increased. This is due to the transconductance characterises of the MOSFET, where the drain current increases with increased gate-source, or gate drive voltage ($i_d \propto V_{GS}$, pulse $= i_d Z_L$). Fig. 3.36(b) demonstrates that the simulated increase in nsPEF amplitude is due to increasing the gate voltage from 15 V to 20 V, similar to the measured pulse. Additionally, in comparing the measured nsPEF with the simulation, the measured pulse across a 50 Ω load impedance is more symmetrical and a squarer in pulse shape, with a faster pulse rise-time.

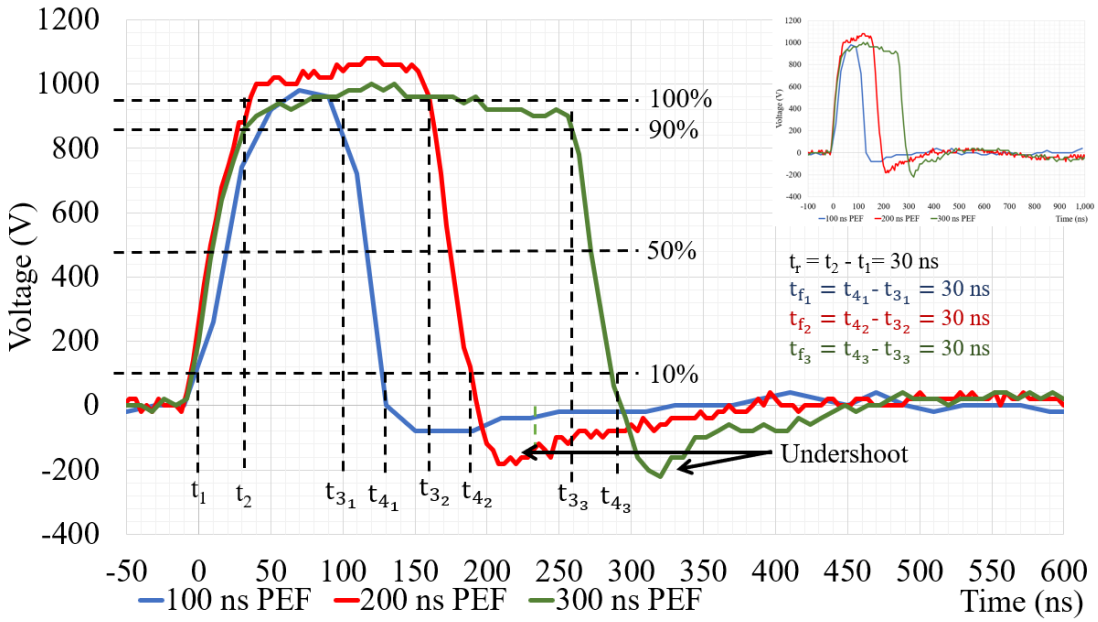


Fig, 3.36. Measured 100 ns pulsed electric field across a 50 Ω load impedance with a 15 V and 20 V gate signal (a) measured waveform (b) measured vs simulated

3.7.3. Function of the Pulse Duration

Fig. 3.37(a) shows that the slow nsPEF electroporation system can produce 1 kV amplitude PEF of 100 ns, 200 ns and 300 ns duration across a 50 Ω load impedance. The rise and fall times of the symmetrical 100 ns, 200 ns and 300 ns are indistinguishable from one another. This confirms that the high side and low side MOSFET's input capacitances are charging and discharging during this $\frac{dV}{dt}$ switching transition.

(a)



(b)

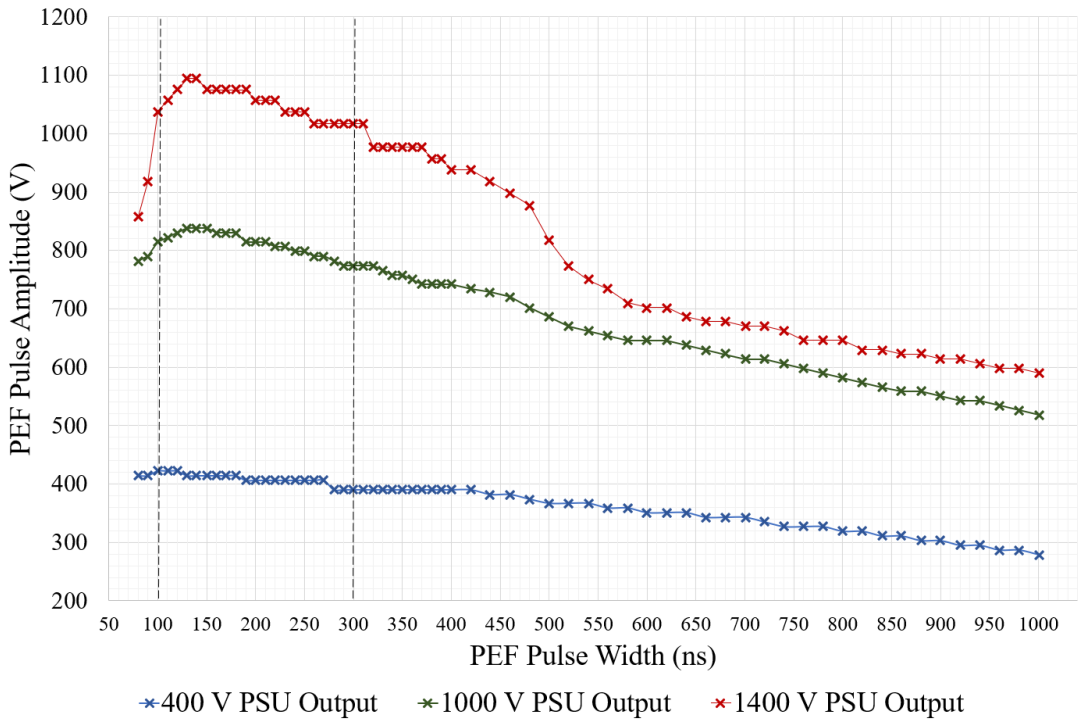


Fig. 3.37. (a) Measured 100 ns, 200 ns, and 300 ns pulsed electric field across a 50 Ω load impedance with a 50 Hz repetition frequency (b) nsPEF amplitude variation over longer pulse durations from 80 ns to 1 µs.

Fig. 3.37(b) shows that the generator can produce PEF duration from 80 ns to 1 µs (1,000 ns) and indicates that the generator's performance is optimized to the intended specifications requirement. This

is because the amplitudes of the PEFs between 100 ns to 300 ns have amplitudes in excess of 1 kV across a 50 Ω load impedance. During these measurements, the high voltage power supply is at its maximum possible programmed output voltage of 1,400 V.

The reduction of pulse amplitude seen in the PEF as the duration increases can be directedly related to the lack of current available from the FS40 power supply and the inability of the capacitor bank to store enough charge. This is due to the increased time associated with the high pulse widths, $\left(C = i\frac{dt}{dV}\right)$. To overcome this issue in future it is suggested a higher-powered power supply unit is used. This is discussed further in detail in Section 3.8.

3.7.4. Function of the Repetition Rate

Fig. 3.38(a) indicates that the pulse amplitude is unaffected throughout the repetition frequency range between 1 Hz and 50 Hz (result obtained with a 100 ns PEF across a 50 Ω load impedance). Therefore Fig. 3.38 also evidences that the chosen MOSFET topology for the slow PEF electroporation system can deliver the required pulse amplitude of 1 kV with a pulse duration ranging from 100 ns to 300 ns with a repetition frequency between 1 Hz and 50 Hz.

Fig. 3.38(b) demonstrates that the amplitude of the PEF is reduced as the repetition frequency of the PEF increases. Fig. 3.38(b) shows that the amplitude of a 100 ns PEF is 1 kV with a repetition rate of 50 Hz as indicated in the requirements for the pulse generator. Also, it can be seen that the pulse amplitude of the 100 ns PEF is reduced to 500 V with a repetition rate of 1 kHz. The reduction in amplitude of the PEFs at a repetition frequency of 1 kHz can be directedly related to the lack of current capacity of the FS40 power supply and associated external capacitor bank. This is due to the increased total time that is associated with a burst of pulses that are generated across a load as the repetition frequency increases. The total time the burst of pulses is generated across a load is a function of the repetition frequency and the pulse width of the burst of PEFs generated. To overcome this issue in future it is suggested that a higher rated voltage-current power supply is used with a higher value capacitor across its output. This is discussed further in detail in Section 3.8.

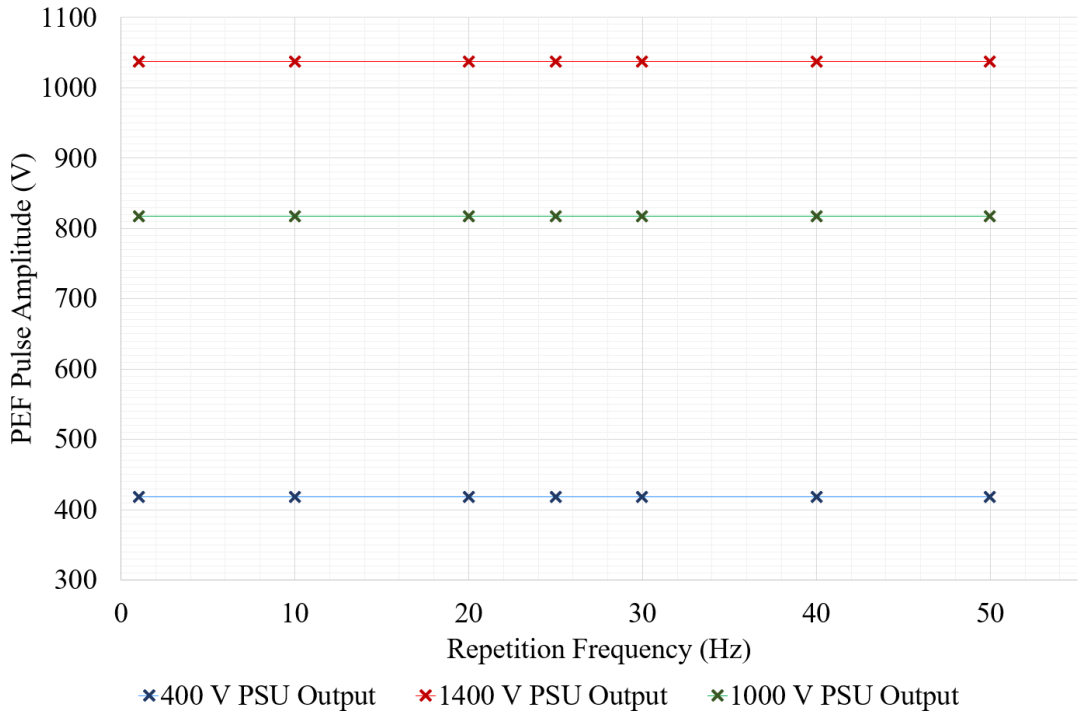
3.7.5. Function of the Load Sensitivity

The load curve shown in Fig. 3.39 was obtained by loading the generator with various resistive loads of low inductance (planar resistors) and measuring the pulse amplitude observed across the load using a high impedance, low capacitance scope probe e.g., 10 MΩ with a 3 pF capacitance.

Fig. 3.39 indicates that the slow nsPEF electroporation system is impedance sensitive. With a load impedance below 500 Ω, the PEF amplitude decreases from 1400 V output from the FS40 high voltage power supply unit. This decrease appears linear (on a log scale) with a load impedance of 100 Ω and less. This effect is due to the internal resistance of the voltage supply source. Fig. 3.39 suggests that the

FS40 power supply used had an internal impedance of approximately 25 Ω. This approximation was made as a 700 V PEF is seen across a ~25 Ω load impedance which is half the 1400 V generated by the FS40 power supply experiences half. Thus, the behaviour of the load and the internal impedance of the power supply acts as a voltage divider. To overcome this issue in future it is suggested a higher-power (voltage and current) dc power supply unit is used. This is discussed in detail in the next subsection.

(a)



(b)

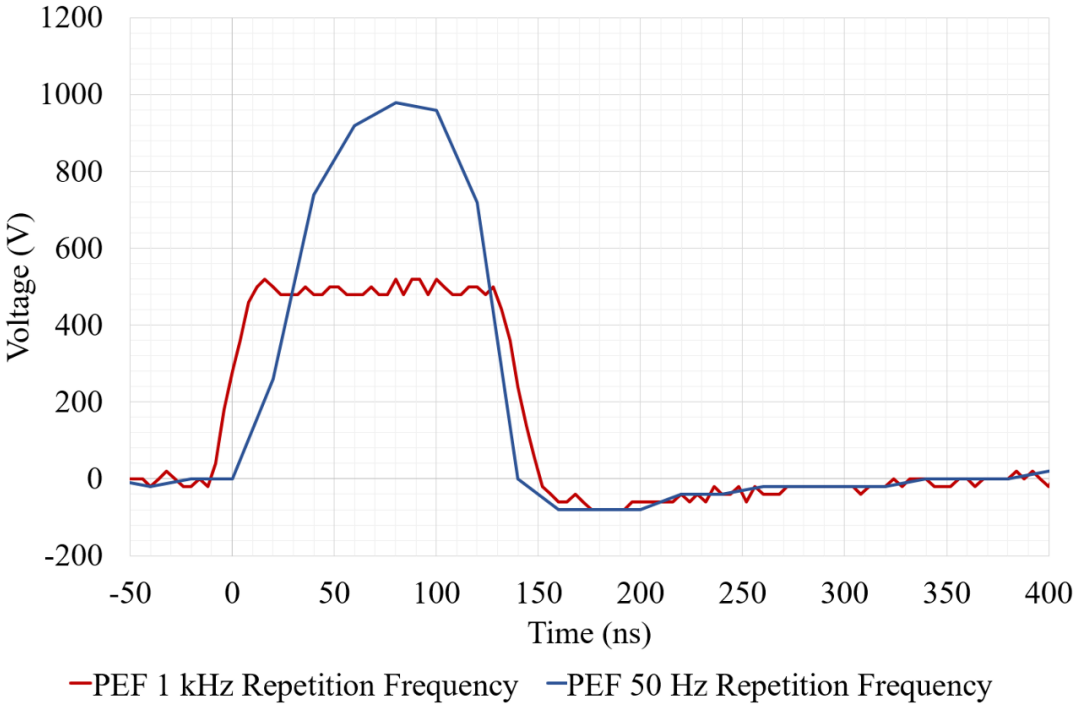
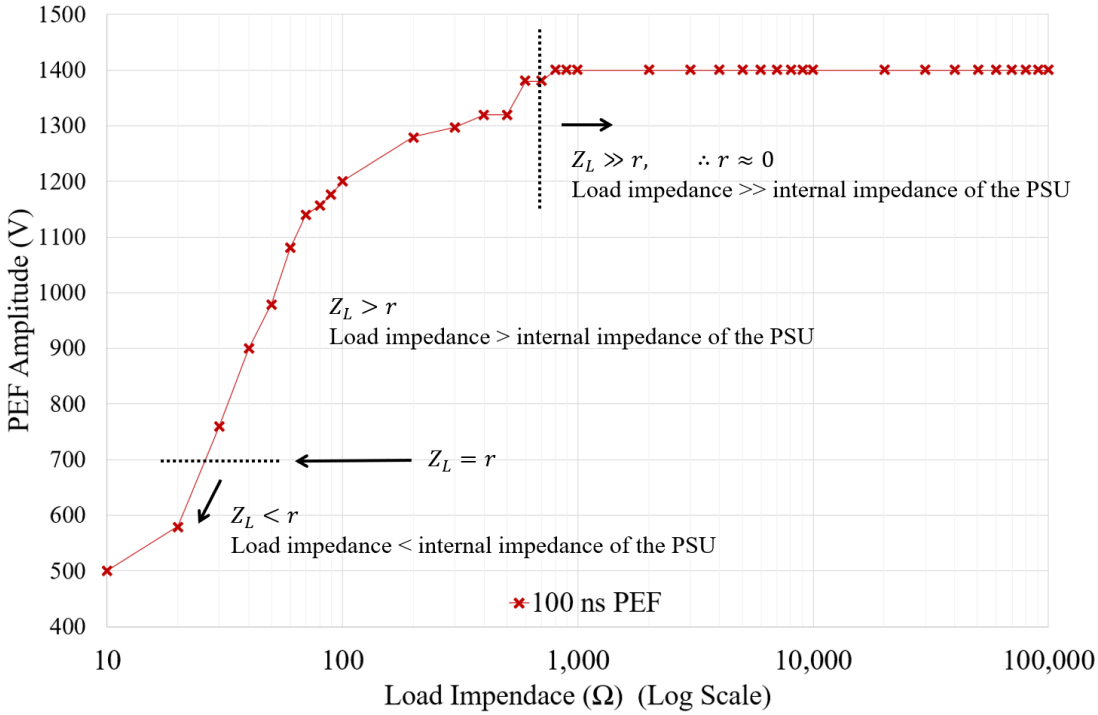


Fig. 3.38. (a) The amplitude of a 100 ns pulsed electric field across a 50 Ω load impedance as a function of repetition frequency of 1 Hz up to 50 Hz. (b) The 100 ns pulsed electric field measured across a 50 Ω load impedance with a repetition frequency of 50 Hz and 1 kHz, with a 1.4 kV power supply unit output.

Fig. 3.39 indicates that the requirement of the slow nsPEF electroporation system to generate 100 ns to 300 nsPEF with amplitudes in excess of 1 kV has been achieved.

(a)



(b)

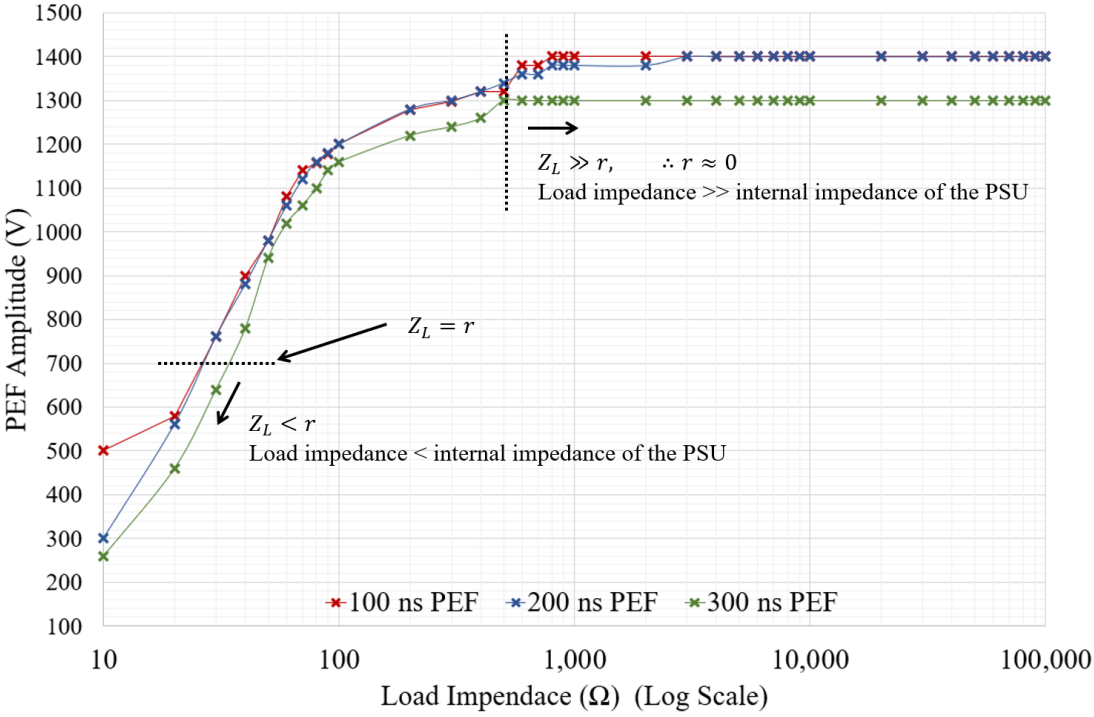


Fig. 3.39. Measured amplitude of (a) 100 ns pulsed electric field as a function of load impedance (b) 100 ns, 200 ns, and 300 ns pulsed electric fields across a wide range of resistive load impedance from 10 Ω to 100 kΩ.

For bulk tissue investigations, this MOSFET-based electroporator would be able to deliver sufficient nsPEF in excess of 1 kV but would not be suitable for cell line investigations. This is because bulk tissue has an estimated impedance of 300 Ω while cell line loads have a highly conductive, low impedance due to the high conductivity fluidic component of cell lines. In conclusion, it is suggested

that the slow nsPEF electroporation system would be suitable for investigating the effects of nsPEF on bulk tissues in an *in-vivo*/pre-clinical study environment. But this system is less suitable for investigating the effect of nsPEF on various cell line populations if their impedance is less than 50 Ω.

3.8. Conclusion and Future Work

A slow nsPEF electroporation system has been designed, developed, and fully characterized in terms of its capability of producing and delivering nsPEF of various amplitudes, durations, and repetition frequencies into a range of load impedances. The agreed set of requirements for the slow pulsed field electroporation system from the first SUMCASTEC consortium was met [2].

Results presented in Fig. 3.37 show that the slow nsPEF electroporation system can produce PEF of durations between 100 ns and 300 ns, with amplitudes in excess of 1 kV, across a 50 Ω load impedance. While Fig. 3.38 shows that the integrity of the nsPEF amplitudes is not affected when the pulses are delivered across a 50 Ω load impedance with a repetition frequency ranging from 1 to 50 Hz. Therefore, the developed slow nsPEF electroporation system has met the set requirements.

The bill of materials in Table 3.5 highlights that the developed electroporation system utilised generic electronic components that are available from non-specialist electronic solutions suppliers. This made the unit cost of developing the slow nsPEF electroporation system cost-effective, with the critical components and the encloser costing approximately £240.00. Additionally, the final system unit is a compact energy module that is approximately 99 mm × 254 mm × 244 mm in dimensions.

Following the verification and validation, the slow nsPEF electroporation system is best optimised to deliver nsPEF into a load impedance of 50 Ω, or greater at low repetition frequencies (1 to 50 Hz). This offers a useful instrument for clinicians and microbiologists to carry out a range of nsPEF experiments and research on bulk tissues or cell lines of 50 Ω impedance or larger, as illustrated in Fig. 3.39. The ability of the system to vary the pulse width, repetition frequency, number of pulses, and amplitude is a key feature to support both *in-vitro* and *in-vivo* investigation of the application of nsPEF-based applications in biology, medicine, and/or biotechnology in a cost-effective manner.

The developed electroporation system operates to the requirement specified. Improvement to the design or alternative components would be required for the system to deliver PEFs that are longer than 300 ns, with higher repetition frequencies, across low impedance loads, with amplitude in excess of 1 kV.

For the generation of the nsPEFs specified in the requirement the XP-Power's FS40 [40] isolated, proportional dc to high voltage dc converter and a capacitor bank of 1 µF across its output was a suitable power supply unit. For the generation of 1 kV PEF with durations varying from 100 ns to 1 µs with a higher repetition frequency of up to 1 kHz a higher rating power supply unit is required. Table 3.6.

highlights the minimum required power rating of a 1.4 kV high voltage power supply unit and associated capacitor bank required for the generation of 100 ns to 100 µs PEF across a load impedance of 10 Ω, 50 Ω, and 300 Ω loads with a repetition frequency of 50 Hz and 1 kHz. The capacitance for the capacitor bank calculated should not allow the voltage of the power supply to drop more than 1% (to 1386 V). The figures in Table 3.6. were calculated by using equations (3.5) to (3.8)

Where V_{dc} is the pulse amplitude, in this case, 1400 V. I_{dc} is the dc current, Z_L is the load impedance of 10 Ω, 50 Ω and 300 Ω, P_{dc} is dc Power ($V_{dc}I_{dc}$ ratio of the power supply), t is the duration of the nsPEF generated (100 ns, 300 ns, 1 µs, 10 µs and 100 µs) and f is the repetition frequency of the nsPEF. I_{AV} is the average current through the load and P_{AV} is the power generated across the load during the total nsPEF exposure time (t *f)*. C is the required capacitance for the capacitor bank and V is the voltage output of the power supply output following the 1% voltage drop ($V_{DC} - \Delta V = 1400 - 14 = 1386$ V).

The load impedance range of 10 Ω, 50 Ω, and 300 Ω was chosen as 10 Ω is an approximation resistive equivalent of cell line culture. 50 Ω because of the current load impedance requirements and 300 Ω as it is an approximated equivalent of bulk tissue impedance. The PEF duration of 100 ns to 100 µs is considered in this analysis as 100 ns is the minimum pulse duration identified in the current requirements. 100 µs is the PEF duration used for the application of classical electroporation for clinical application (electrochemotherapy and irreversible electroporation treatments).The FS40 power supply used in this slow nsPEF electroporation system had a maximum output current rating of 2.5 mA and power rating of 10 W, and a 1 µF capacitor bank was connected across the supply.

Table 3.6 shows the required current (average current, I_{Av}) and power (average power, P_{Av}) of a power supply unit and associated capacitor bank capacitance (C) required to produce PEF of specific parameters. Figures highlighted in green in Table 3.6 indicate that the current power supply (FS40) and associated capacitor bank has the necessary current, power, and/or capacitance rate to generate a 1400 V PEF of specific duration and repetition frequency across the necessary load impedances (10 Ω, 50 Ω, and 300 Ω). If the figures are highlighted in red, it suggests that an alternative power supply would be required to deliver the PEF parameters indicated (load impedance, repetition frequency and pulse duration).

Table 3.6 highlights that the voltage supply selected for this design, and therefore the slow nsPEF electroporation system, can deliver 100 ns to 300 ns PEF at a 50 Hz repetition frequency across the range of load impedances from 50 Ω to 300 Ω (bulk tissue impedance). Additionally, it has the potential of delivering 1400 V PEF of 1 µs in duration across a 300 Ω (bulk tissue impedance).

Table 3.6. Required high voltage power supply unit power rating for the generation of 100 ns, 300 ns, 1 µs, 10 µs and 100 µs pulsed electric fields across a 10 Ω (cell line), 50 Ω and 300 Ω (bulk tissue) load impedance at a repetition frequency of 50 Hz and 1 kHz.

dc power supply requirement			***Load impedance, Z_L (Ω)***	***PEF parameters***			***Required power supply and capacitor bank rating***		
dc Voltage, V_{dc} (V)	dc Current, I_{dc} (A)	dc Power, P_{dc} (W)		Pulse width, t	Repetition frequency, *f*	Total on time *f t*	Average Current, I_{AV} (A)	Average Power, P_{AV} (W)	Capacitance, C (F)
50 Ω load impedance and repetition frequency of 50 Hz									
1,400	28	39,200	50	100 ns	50	5 µs	14 µ	196 m	199 n
1,400	28	39,200	50	300 ns	50	15 µs	42 µ	588 m	597 n
1,400	28	39,200	50	1 µs	50	50 µs	1.4 m	1.96	1.99 µ
1,400	28	39,200	50	10 µs	50	500 µs	14 m	19.6	19.9 µ
1,400	28	39,200	50	100 µs	50	5 ms	140 m	196	199 µ
10 Ω Load and Repetition frequency of 50 Hz									
1,400	140	196,000	10	100 ns	50	5 µs	700 µ	980 m	995 n
1,400	140	196,000	10	300 ns	50	15 µs	2.1 m	2.94	2.98 µ
1,400	140	196,000	10	1 µs	50	50 µs	7 m	9.8	9.95 µ
1,400	140	196,000	10	10 µs	50	500 µs	70 m	98	99.5 µ
1,400	140	196,000	10	100 µs	50	5 ms	700 m	980	995 µ
300 Ω Load and Repetition frequency of 50 Hz									
1,400	4.66	6533.33	300	100 ns	50	5 µs	23.3 µs	32.7 m	33.2 p
1,400	4.66	6533.33	300	300 ns	50	15 µs	70 µs	98 m	99.5 p
1,400	4.66	6533.33	300	1 µs	50	50 µs	233 µs	327 m	332 p
1,400	4.66	6533.33	300	10 µs	50	500 µs	2.33 ms	3.27	3.32 µ
1,400	4.66	6533.33	300	100 µs	50	5 ms	23.3 ms	32.7	33.2 µ

Table continue next page…

Table 3.6. Required high voltage power supply unit power rating for the generation of 100 ns, 300 ns, 1 µs, 10 µs and 100 µs pulsed electric fields across a 10 Ω (cell line), 50 Ω and 300 Ω (bulk tissue) load impedance at a repetition frequency of 50 Hz and 1 kHz.

dc power supply requirement			***Load impedance, Z_L (Ω)***	***PEF parameters***			***Required power supply and capacitor bank rating***		
dc Voltage, V_{dc} (V)	dc Current, I_{dc} (A)	dc Power, P_{dc} (W)		Pulse width, t	Repetition frequency, *f*	Total on time *f t*	Average Current, I_{AV} (A)	Average Power, P_{AV} (W)	Capacitance, C (F)
50 Ω load impedance and Repetition frequency of 1 kHz									
1,400	28	39,200	50	100 ns	1,000	100 µs	2.8 m	3.92	199 n
1,400	28	39,200	50	300 ns	1,000	300 µs	9.4 m	11.8	597 n
1,400	28	39,200	50	1 µs	1,000	1 ms	28 m	39.2	1.99 µ
1,400	28	39,200	50	10 µs	1,000	10 ms	280 m	392	19.9 µ
1,400	28	39,200	50	100 µs	1,000	100 ms	2.8	3.92 k	199 µ
10 Ω Load and Repetition frequency of 1 kHz									
1,400	140	196,000	10	100 ns	1,000	100 µs	14 m	19.6	995 n
1,400	140	196,000	10	300 ns	1,000	300 µs	42 m	58.8	2.98 µ
1,400	140	196,000	10	1 µs	1,000	1 ms	140	196	9.95 µ
1,400	140	196,000	10	10 µs	1,000	10 ms	1.4	1.96 k	99.5 µ
1,400	140	196,000	10	100 µs	1,000	100 ms	14	19.6 k	995 µ
300 Ω Load and Repetition frequency of 1 kHz									
1,400	4.66	6533.33	300	100 ns	1,000	100 µs	467 µs	652 m	33.2 p
1,400	4.66	6533.33	300	300 ns	1,000	300 µs	1.4 m	1.96	99.5 p
1,400	4.66	6533.33	300	1 µs	1,000	1 ms	4.67 m	6.53	332 p
1,400	4.66	6533.33	300	10 µs	1,000	10 ms	46.7 m	65.3	3.32 µ
1,400	4.66	6533.33	300	100 µs	1,000	100 ms	467 m	653	33.2 µ

Utilizing an alternative high voltage power supply to the FS40 [40], such as the HRL3024S1K5P [49] with an output current of 20 mA and power of 30 W, would provide the slow nsPEF electroporation system with the capability to generate a wider variety of PEF. The HRL3024S1K5P power supply unit would provide a means of generating 1.4 kV PEF of 100 ns to 10 µs in durations with a repetition frequency of 50 Hz across a load impedance of 10 Ω or higher. Or it could provide a means to generate a 1 kV PEF of 100 ns to 300 ns in duration, with a repetition frequency of up to 1 kHz across a load impedance of 50 Ω. Or potentially a PEF of 1 µs in duration with a repetition rate of 1 kHz across a bulk tissue of 300 Ω load impedance.

Fig. 3.40 illustrates the relationship between the internal impedance of the power supply unit, r_A, and the load impedance, Z_L, which is similar to a voltage divider circuit. Where the amplitude of the PEF is $V_L = \frac{Z_L}{r_S+Z_L} V_{CC}$. Fig. 3.39 suggest that the FS40 power supply internal impedance is roughly 25 Ω and cell line cultures have an impedance of approximately 10 Ω. With the current power supply, the FS40, to generate a PEF with amplitude in excess of 1 kV across a 10 Ω load impedance a power supply, V_{CC}, of 3.5 kV or above is required $\left(1\text{kV} = \frac{10}{10+25} V_{CC}\right)$. The problem with this is that the 3.5 kV necessary to generate a 1 kV PEF across a 10 Ω load impedance would exceed the C2M1000170D Silicon Carbide Power MOSFET 1.7 kV drain-source breakdown voltage. A method of overcoming this would be to use a MOSFET with a drain-source breakdown voltage of 4 kV or stack and operate multiple C2M1000170D MOSFETs simultaneously.

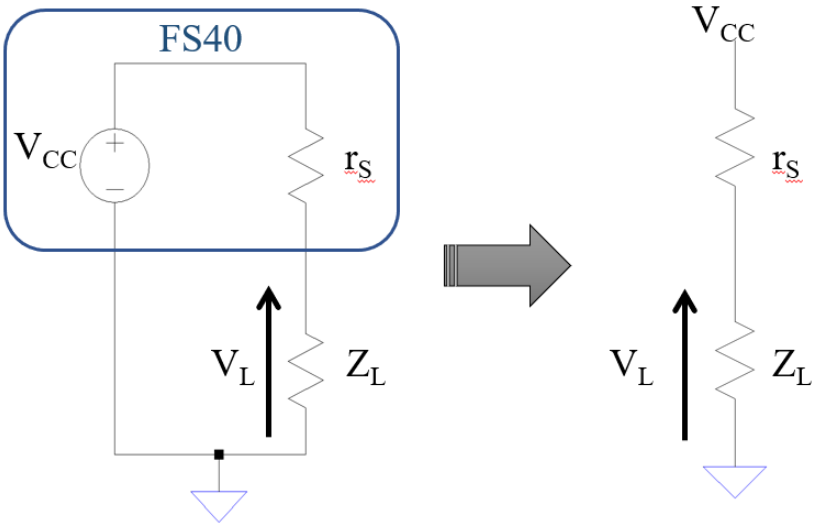


Fig. 3.40. How the relationship between the load impedance (Z_L) and the high voltage power supply unit internal resistance (r_S) resembles a voltage divider

In conclusion, the slow nsPEF electroporation systems topology is based on two C2M1000170D Silicon Carbide Power MOSFET [28] in a push-pull configuration. It is capable of generating a specified number of 100 ns to 300 ns PEF, with amplitude in excess of 1 kV, at a repetition frequency of 1 Hz to 50 Hz. The limitation of the switching speed and therefore the minimum pulse duration is dependent upon the MOSFETs selected for this topology. At the time of implementation, wolfspeeds

C2M1000170D Silicon Carbide Power MOSFETs were the best option. From implementation to write-up there are a wider range of MOSFETs available that are affordable and exhibit faster-switching speeds, lower drain-source on-state resistance, and lower input capacitance.

An example of an alternative MOSFET that could be used in the next iteration of the slow nsPEF electroporation systems is Infineon's IMBF170R650M1 [50]. The IMBF170R650M has a faster transition time and lower drain-source on-state resistance than the C2M1000170D MOSFET. Additionally, the IMBF170R650M1 [50] also has a recommended gate driver to maximise the effectiveness and efficiency of the device switching capabilities. This recommended gate driver is the 1ED3124MU12H Isolated Single Channel EiceDRIVER [51] with its static interlocking function. The 1ED3124MU12H static interlocking function provides a pair of gate driver circuits with cross-connected individual pulse width modulation (PWM) signals to inhibit static turn-on of both MOSFETs simultaneously. A suggested future work would be to exchange the outdated C2M1000170D MOSFETs and FS40 power supply for the identified replacement units to improve the slow nsPEF electroporation systems switching efficiency and capability to generate a wider range of nsPEFs.

Additionally, it would be beneficial to incorporate further monitoring circuits such as a calorimeter to provide an additional modality to the system to calculate the total energy delivered into a load, or bulk tissue, and the maximum thermal effect the energy applied had on said load/bulk tissue. This suggested monitoring circuits that collect such data would be beneficial to support both *in-vitro* and *in-vivo* research of nsPEF-based applications in biology, medicine, and/or biotechnology.

Chapter 3 References

[1] SUMCASTEC. "Home – SUMCASTEC." SUMCASTEC.eu. http://www.sumcastec.eu/. (accessed Aug., 2017)

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CHAPTER IV. SLOW NSPEF ELECTROPORATION SYSTEM – *IN-VITRO* INVESTIGATION

4.1. Introduction

An *in-vitro* investigation of the effect of 1, 5, 10 and 20 pulsed electric fields (PEFs) of 100 ns, 200 ns and 300 ns in duration, with amplitudes in excess of 1 kV on cell population enriched with Cancer Stem Cells (CSCs) was conducted. The cell population enriched with CSCs in question was the D283 medulloblastoma cell line. Investigation into the permeabilization, viability and thermal effects of the applied nanosecond pulsed electric fields (nsPEFs) on the D283 cell line was carried out. One outcome of the *in-vitro* investigation on cell line loads was to understand the operating performance of the nsPEF generator when using complex cell line loads.

The intention was to gain preliminary *in-vitro* data on the application of nsPEF pulses on cell lines that are heavily enriched in cancer stem cells before carrying out pre-clinical investigations on bulk tissue. The results obtained indicate that the generator is capable of achieving well-controlled non-thermal irreversible nanosecond electroporation, or neutralization, of cancerous cell line samples enriched in cancer stem cells.

4.2. *In-vivo* Set-up and Protocols

The D283 medulloblastoma cell line, enriched in CSCs, were exposed to nsPEFs through a Bio-rads commercially available 100 µl electroporation cuvette [1]. The Bio-rad 100 µl electroporation cuvette is a pair of 5 mm x 11 mm parallel plate electrodes with a 1 mm gap, as shown in Fig. 4.1.

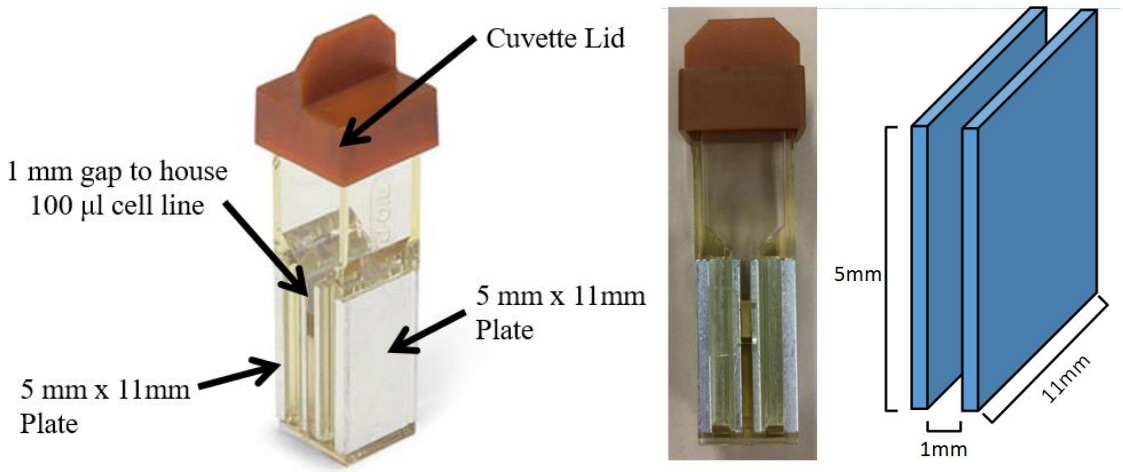


Fig. 4.1 Bio-rads commercially available 100 µl electroporation cuvette [1]

An in-house cuvette housing unit was designed and fabricated to hold the Bio-rad 100 µl electroporation cuvette. This provided a direct and easy standard 50 Ω impedance connector connection between the cuvette and the pulse generator. Thus, allowing the biological load within the cuvette to be

exposed to nsPEF pulses generated by the push-pull configuration electroporation system developed for this microbiological research investigation.

The cuvette housing units, shown in Fig. 4.1, provided a means for real-time monitoring of the applied nsPEF pulses delivered into the biological cells within the electroporation cuvette. The pulse waveforms were captured in real-time using a Tektronix TDS5054B-NV Oscilloscope [2] and a high voltage LeCroy PPE 5 kV probe [3]. The electric field between the cuvette electrodes forms a capacitance load because the biological solution had a homogenous distribution as already suggested in [4]-[5] by numerical simulations.

The complete setup for the preliminary study of the D283 cell line is shown in 3.42. The results of permeabilization, viability and thermal investigations are discussed below.

4.3. Biological Load Protocols

The principal microbiologists from the Italian National Agency for new technologies, energy and sustainable economic development (ENEA) indicated that the electroporation systems required to deliver nsPEFs of 1 kV amplitude into a 50 Ω load impedance. Initially, there was a concern about possible mismatch between the 50 Ω environment of the cuvette, the cuvette housing unit, cables and the connector used for the initial set-up as the estimated impedance for the D283 natural cell line suspension was approximately 10 Ω. Because of these concerns, the D283 cells were suspended in a 50 Ω impedance artificial buffer, developed by ENEA, that provided an overall 50 Ω load impedance in which the D283 cells were suspended whilst maintaining their natural biological characteristics for the duration of the experiment.

In practice, the D283 cell line suspended in a standard culture medium known as Modified Eagle Medium (MEM) had an estimated impedance of approximately 10 Ω. This is due to the high conductivity of the suspending medium of around 1.5 S/m [5]-[6]. Impedance mismatch minimization between the generator, cuvette holder, and the load (cuvette filled with cell solution) is imperative to guarantee the generator can deliver nanosecond electric pulses in excess of 1 kV amplitude. Any impedance mismatch at the interface between the components will cause reflections of the pulse.

To achieve a 50 Ω impedance match for the whole *in-vitro* set-up, the generator with an output n-connector of 50 Ω is connected to a biological load, and the cuvette housing unit that was designed such that the generator 'sees' an impedance of 50 Ω. The D283 cells were suspended in an artificial buffer solution that mimicked a purely resistive load of 50 Ω.

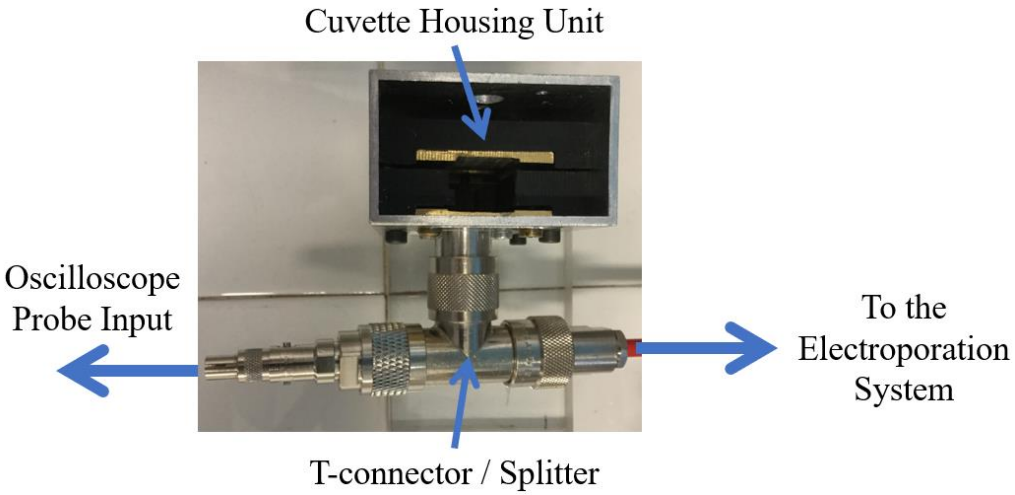
The artificial buffer solution consisted of 100 µl of an artificial buffer solution with 20 ml of phosphate buffer saline (PBS), 80 ml of distilled water, and 8.2 g of sucrose to counteract osmotic pressures of the cells due to the distilled water. The artificial 50 Ω buffer solution had a conductivity of

0.3 S/m [6].The protocol highlighted here [6] details the method undertaken to place the CD283 cells in the artificial buffer solution whilst maintaining their viability when placed in the Bio-rads commercially available 100 µl, 1 mm gap electroporation cuvette to provide the primary permeability, viability and the necessary thermal control.

4.4. Validation of Biological Load Protocols

Before carrying out the *in-vitro* biological investigation, the slow nsPEF electroporation system has been verified and validated on its capability in delivering nsPEF across purely, resistive impedance load. With the protocol highlighted in the previous section, the D283 cells were suspended in an artificial buffer solution that should represent a 50 Ω load impedance. This is to minimise reflection or maximise the matching between the components in the system, as shown in Fig. 4.2. The protocol was developed by the ENEA microbiologists. To verify the integrity of the artificial buffer for the *in-vitro* study a comparison of the measured nsPEFs across a purely resistive 50 Ω load impedance and the artificial 50 Ω buffer was conducted.

(a)



(b)

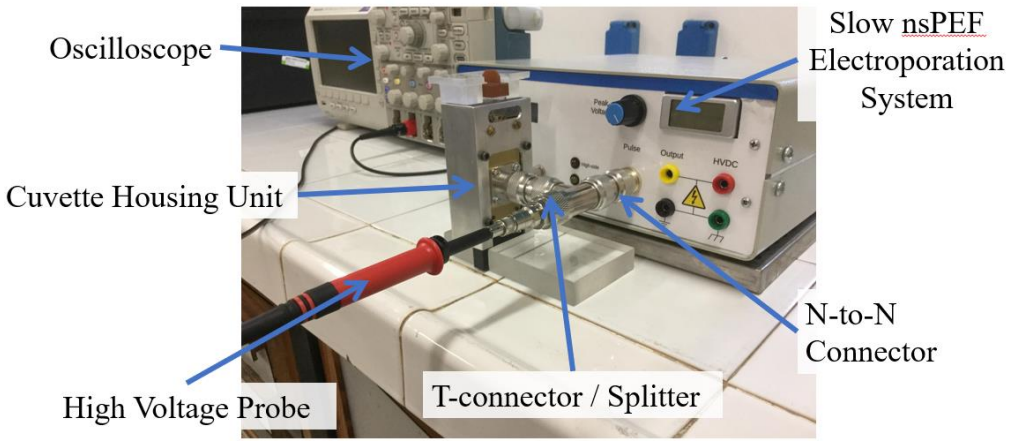


Fig. 4.2. (a) ENEA's in-house cuvette housing unit. (b) The *in-vitro* investigation set-up

Fig. 4.3 illustrates that the artificial buffer is comparable to a purely resistive 50 Ω load impedance, thus validating that the protocol conceived by ENEA for the generation of 100 µl of buffer solutions is

relative to 50 Ω impedance [6]. The 900 V amplitude of the nsPEF observed with ENEA's artificial buffer solution is lower than the 1 kV nsPEF observed across a 50 Ω load impedance. This suggests that the true resistive value of ENEA's artificial buffer solution is approximately 40 Ω when interpreting Fig. 3.39, the measured amplitude of a 100 ns PEF as a function of load impedance.

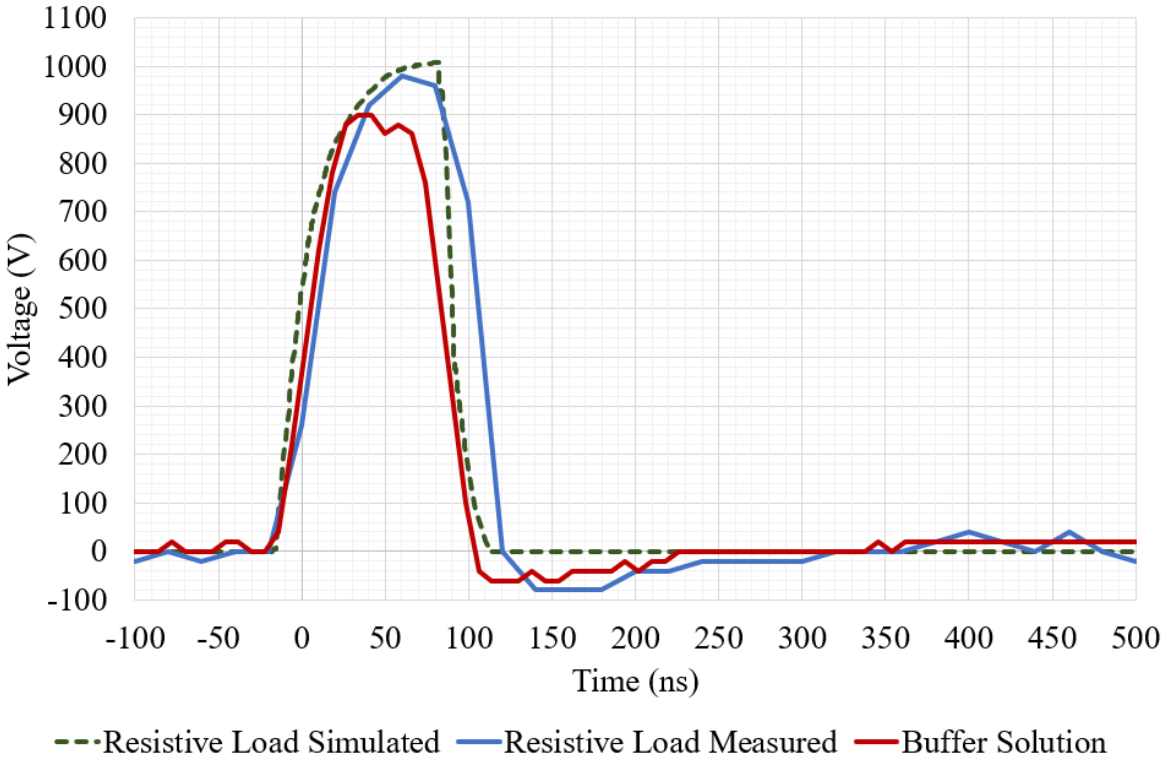


Fig. 4.3. Comparison of the measured 100 ns pulsed electric field observed across a 50 Ω resistive load impedance in simulation (green), in practice (blue), and across the 50 Ω buffer solution developed by ENEA (red)

Furthermore, Fig. 4.4 highlights that the presence of the D283 cells did not affect the electrical properties of the buffer. It can be seen that the addition of the D283 cells has a negligible effect on the nsPEF waveform when compared to the buffer solution without the cells. This implies that the D283 cells represent an extremely small fraction of the global solution volume in comparison to the MEM contained within the cuvette.

Fig. 4.5 shows the 100 ns (blue solid line), 150 ns (red dashed line), and 300 ns (black dotted line) voltage pulse waveforms measured across the electroporation cuvette containing D283 MB cell line suspended with the 50 Ω, 0.3 S/m buffer solution. These waveforms illustrate the pulses electric fields delivered to the cells during the biological investigations (permeabilization and viability tests). The cells are exposed to a symmetrical voltage pulse with a maximum amplitude of ~1.2 kV/mm (~1.2 MV/m), with minimal overshoot and ringing. These results are similar to those obtained through simulations and across a 50 Ω load resistor.

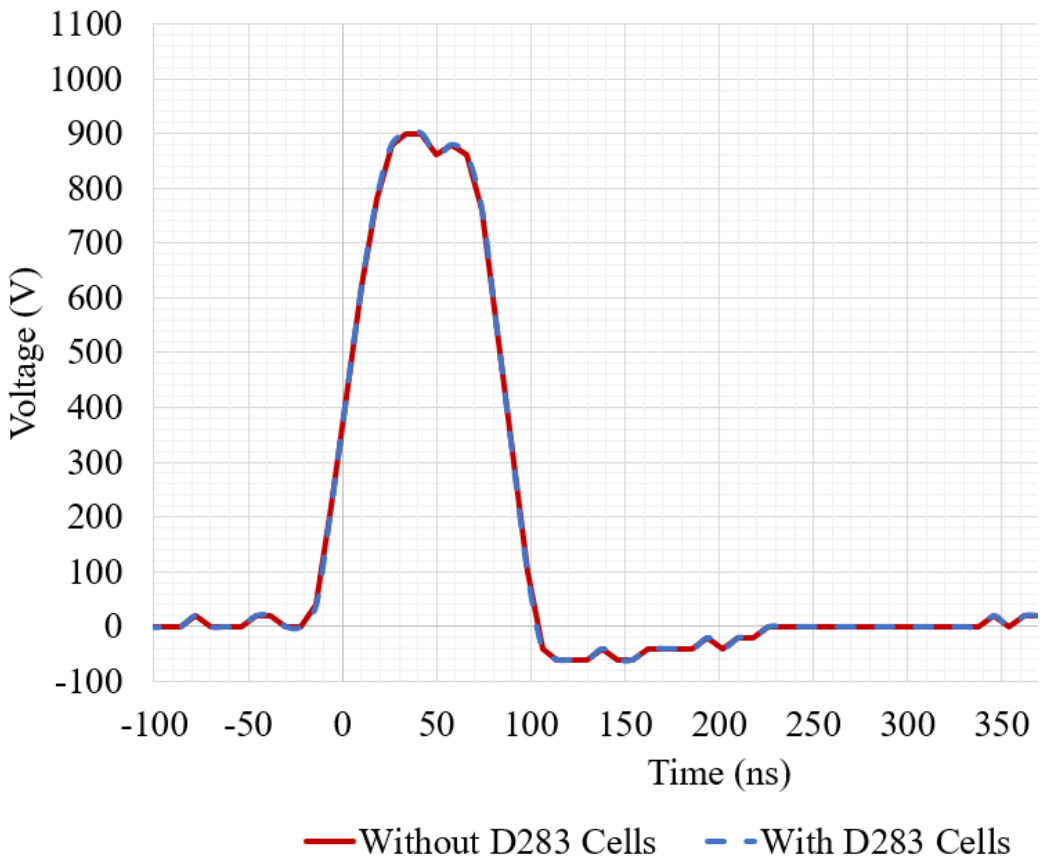


Fig. 4.4. 100 ns pulsed electric field across the buffer solution developed by ENEA [6] with (red) and without (blue) the D283 cell line population.

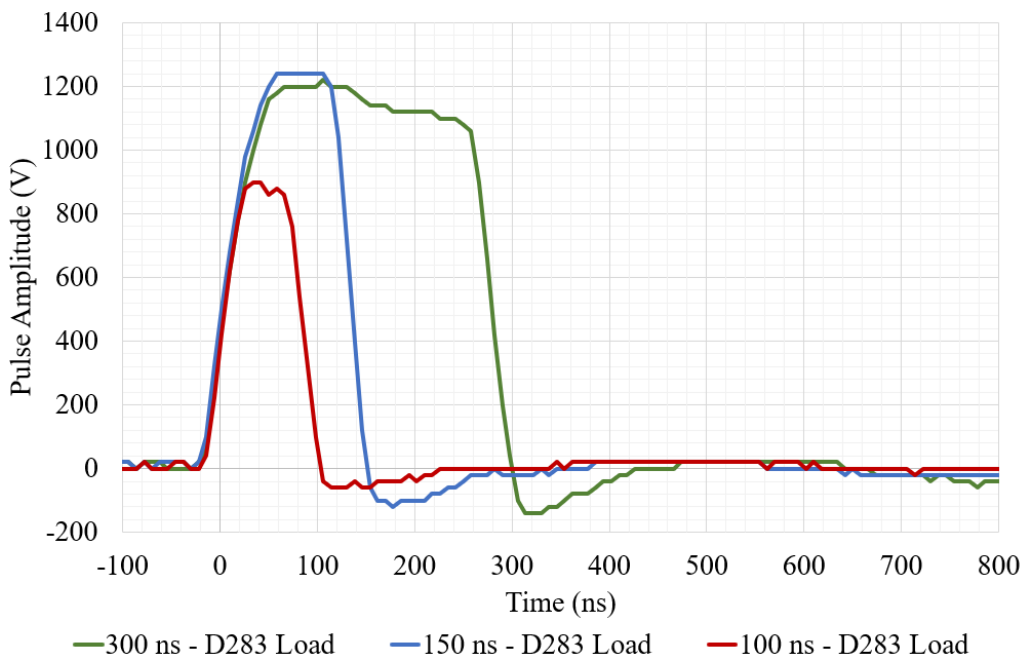


Fig. 4.5. nsPEF of 100 ns (red), 150 ns (blue) and 300 ns (green) pulses observed across the D283 cell line population submerged in the 50 Ω buffer solution

4.5. Permeability Test

For the permeabilization tests, D283 cells were grown in a humidified atmosphere at 37 °C and 5 % CO_2 in MEM supplemented with 10 % fetal bovine serum and 1 % of penicillin-streptomycin. Cells were scraped and centrifuged, suspended in the artificial 50 Ω buffer solution, and Yo-Pro-1 (3 μM) was added 5 minutes before exposure to nsPEFs. This is highlighted in the protocol [6].

To test cell permeabilization, pulses were delivered according to the protocol with PEFs parameters as reported in Table 4.1. A non-pulsed sample called 'Control' or 'Sham' was also included in the analysis where no nsPEFs were applied onto a D283 cell line population.

Table 4.1. Nanosecond pulsed electric field parameters the D282 cell population was exposed to and associated permeabilization rate

Test number	***PEF duration (ns)***	***E-Field Strength (MV/m or kV/mm)***	***Number of Pulses***	***Repetition Frequency (Hz)***	***Permeabilization Rate (%)***
Control	0	0	0	0	5
100a	100	0.9	1	0	5
100b	100	0.9	5	50	30
100c	100	0.9	10	50	27
100d	100	0.9	20	50	35
100e	100	0.9	20	1	5
200a	200	1.2	1	0	4
200b	200	1.2	5	50	74
200c	200	1.2	10	50	80
200d	200	1.2	20	50	82
200e	200	1.2	20	1	73
300a	300	1.2	1	0	18
300b	300	1.2	5	50	80
300c	300	1.2	10	50	81
300d	300	1.2	20	50	80
300e	300	1.2	20	1	90

Fig. 4.6 illustrates the permeabilization rates of the D283 cell line population exposed to various nsPEFs protocols, highlighted in Table 4.1, in terms of pulse width, repetition frequency and the number of pulses. Fig. 4.6 also indicates that exposing D283 cells to at least 5 consecutive 200 ns duration PEFs resulted in greater than 70 % of the cell population being permeabilized while at least 5 consecutive pulses of 300 ns duration PEFs resulted in more than 80 % of the cell population being permeabilized. The best permeabilization results were observed with 20 PEF of 300 ns duration, E-field strength of 1.2 MV/m (1.2 kV/mm) and at repetition frequency of 1 Hz. This nsPEF protocol provided the maximum PEF and energy exposure time onto the cell line population without any thermal injury to the cells.

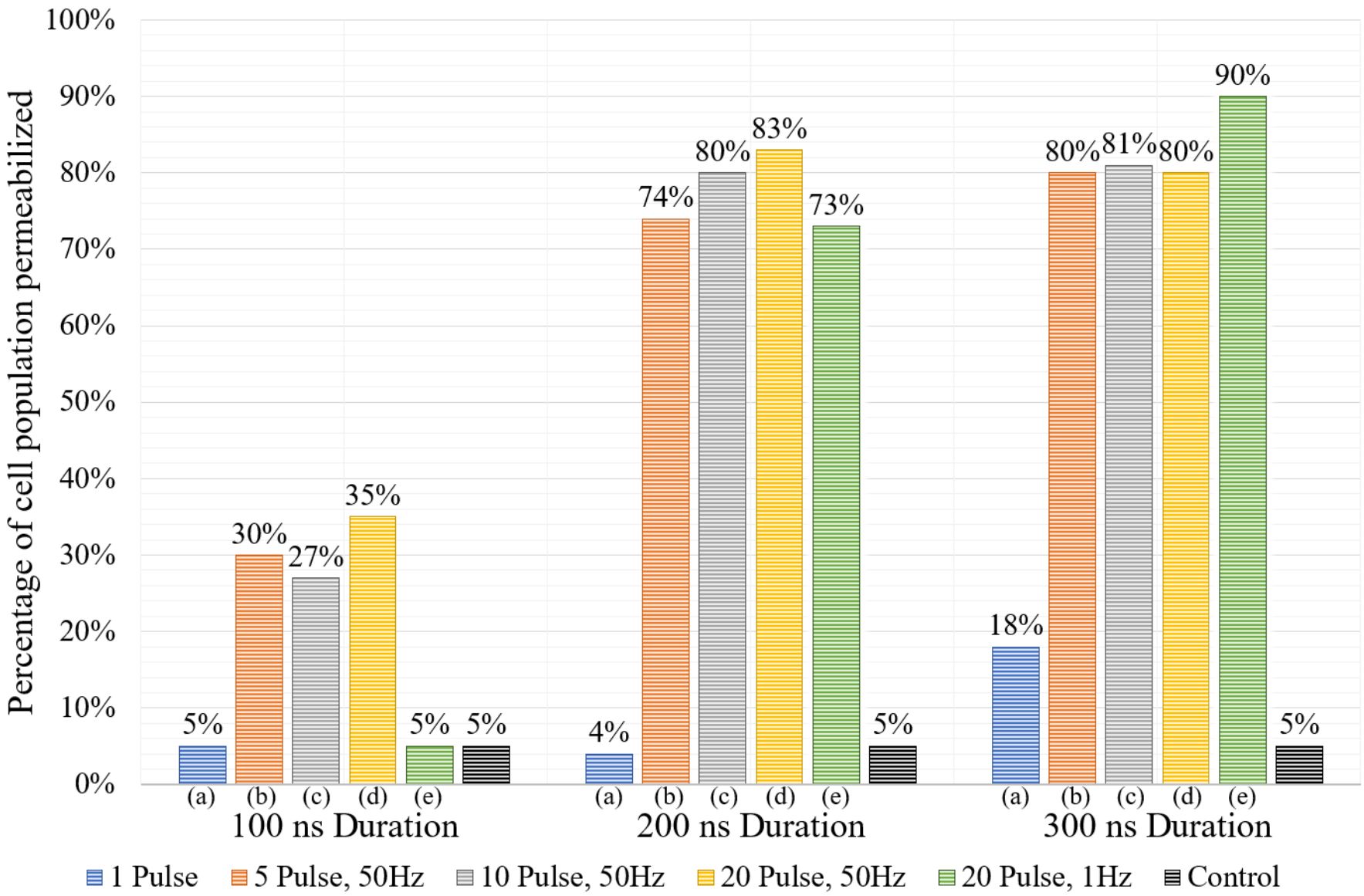
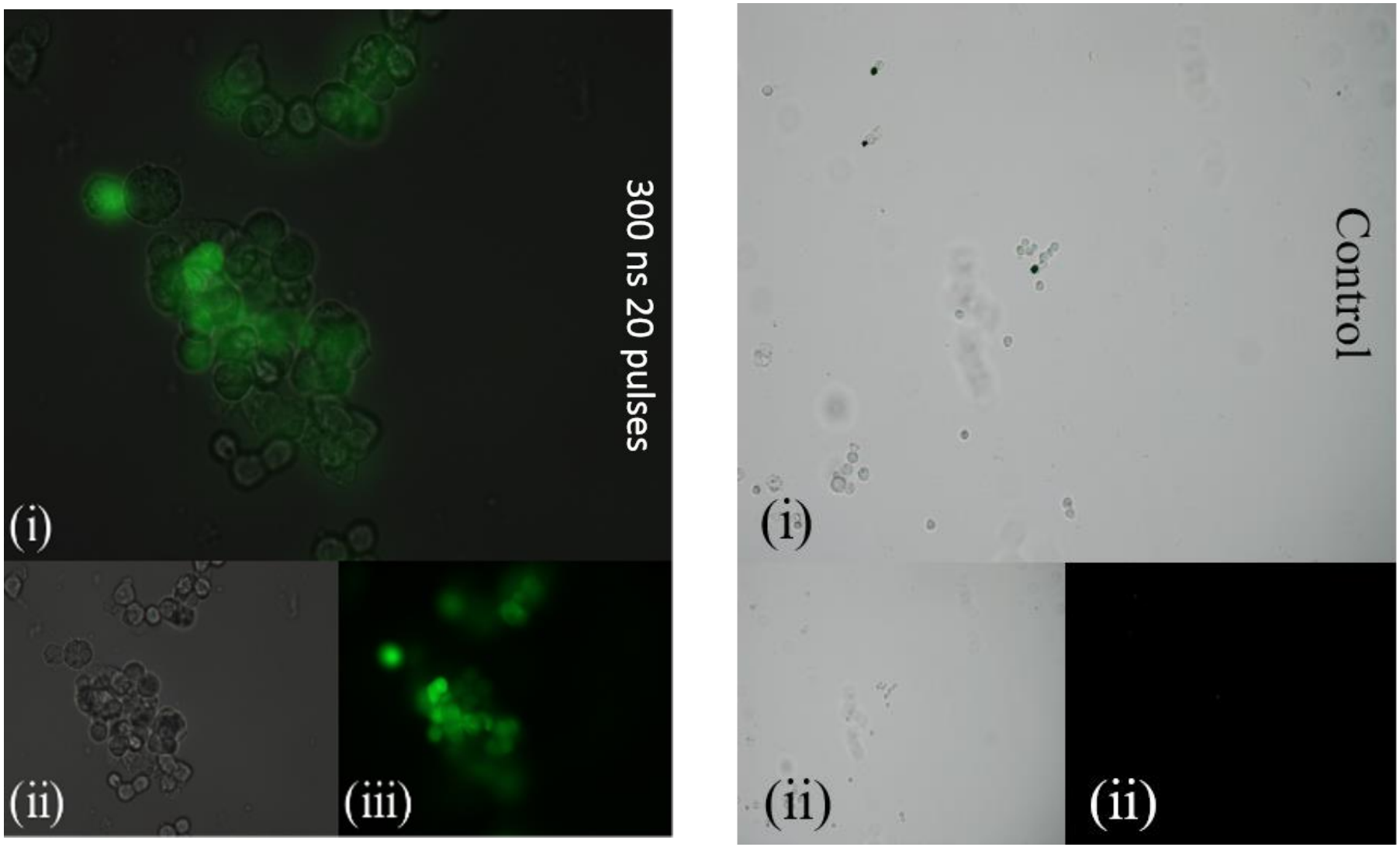


Fig. 4.6. Percentage of D283 cell population permeabilized after exposure to nanosecond pulsed electric field of specific parameters



(a) (b)

Fig. 4.7 The observed fluorescence microscopy YOPRO-1 uptake of the cell line population following exposure to (a) 300e; 20 pulses of 300 ns at 1.2 MV/m (b) Control (i) bright field image overlapped across the fluorescent image (ii) bright field image (iii) fluorescence microscopy YOPRO-1 uptake

These results were confirmed visually through observing electropermeabilized cells under fluorescence microscopy (Yo-Pro-1 λemission = 510 nm), and the percentage of cell permeabilization is computed as the ratio of fluorescent cells divided by the total imaged D283 cells in three different observation areas. This is further confirmed by Fig. 4.7 where images of permeabilized D283 are given. For the same sample and figure, the bright field image is also presented to demonstrate the presence of D283 cells in the reviewed sample.

It can be seen in Fig. 4.6 that 90 % of the cells were permeabilise by applying 20 pulses of 300 ns duration at a pulse repetition rate of 1 Hz (1 pulse per second) with an electric field amplitude of 1.2 MV/m (1.2 kV/mm).

4.6. Viability

Cell viability is a measure of the proportion of live, healthy cells within a population. Cell viability assays are used to determine the overall health of cells in a culture and to measure cell survival following exposure to the delivered nsPEFs. The lower the viability of the cell population, the higher the proportion of the cell population that has been neutralized or irreversibly electroporated.

To assess cell viability, the well-established trypan blue exclusion techniques were carried out after the D283 cell line population were exposed to nsPEF described in Table 4.1. 10 µl of trypan blue was added to the 100 µl of cell solution. Live cells were automatically counted using a commercial system (Luna II by Logos [7]) where the solution containing cells was counted in the disposable counting chambers. The viability of cell populations was evaluated immediately after exposure to the nsPEFs and at 24 hours and 48 hours after exposure. Viability tests were performed using pulses of the following durations: 100, 200, and 300 ns PEFs, with amplitudes of 1 kV/mm and 50 Hz repetition frequency. The number of delivered nsPEFs were: 1, 5, 10 and 20. A sham or control exposure samples were also considered for comparison.

Fig. 4.8, Fig. 4.9, and Fig. 4.10 show the results of the viability tests, where the cell viability percentage is the ratio of the viability of the exposed population to the control sample (cell population not exposed to PEFs). The viability data indicates high cell viability following exposure to 100 ns and 200 ns pulses for the various number of pulses (e.g., 1, 5, 10 and 20) after 24 and 48 hours of observation. The normalized cell population viability is lower when exposed to 300 ns PEFs (Fig. 4.10) in comparison to exposure to 100 ns (Fig. 4.8) and 200 ns PEFs (Fig. 4.9). This is highlighted when the D283 cell is exposed to a higher number of pulses, for example, 10 and 20, and for the long observation time points (e.g., 24 hours and 48 hours after exposure).

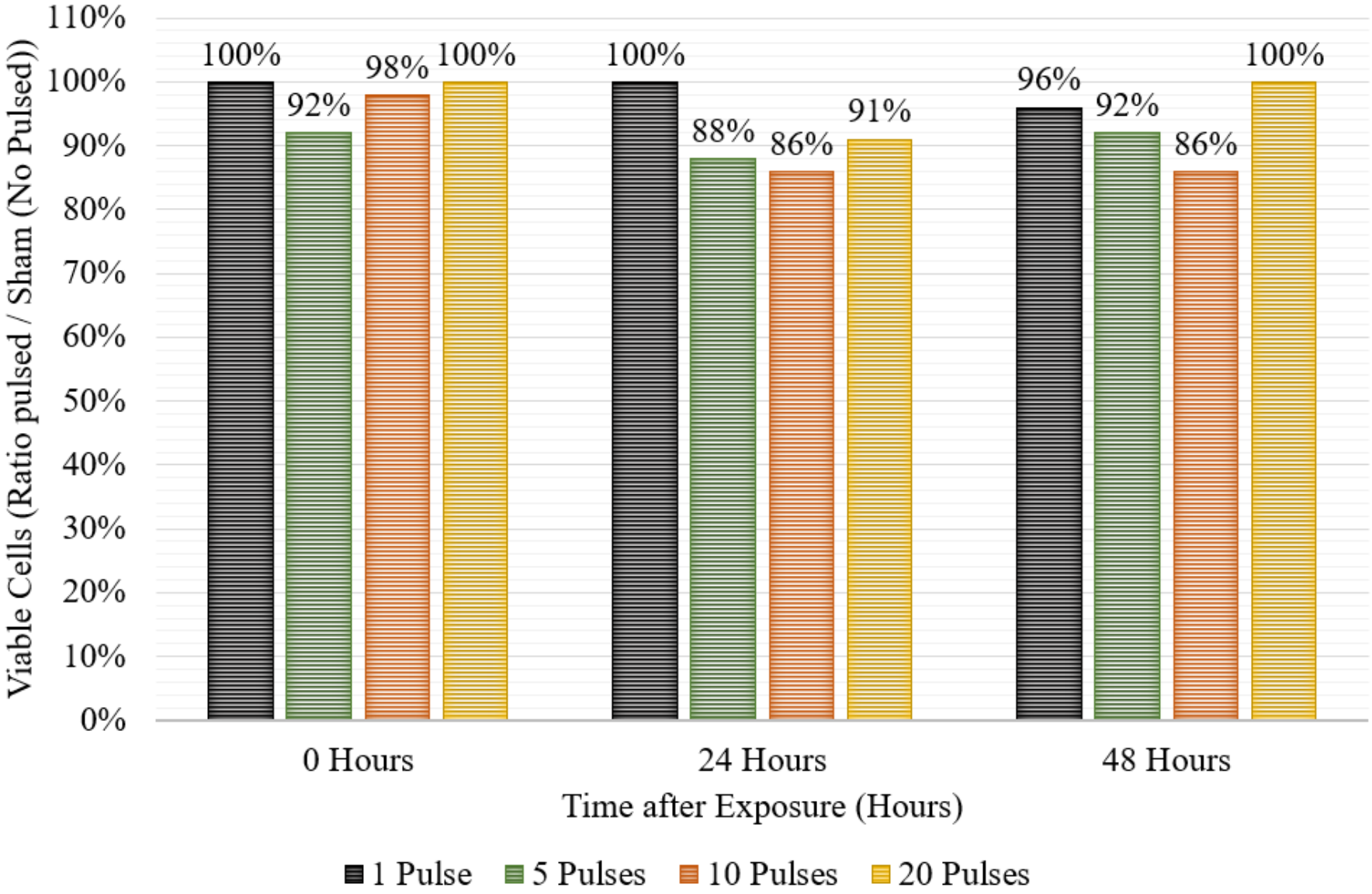


Fig. 4.8. Viability of cells 0, 24 and 48 hours after exposure to 100 ns pulsed electric fields, with 0.9 kV/mm electric field strength and 50 Hz repetition frequency.

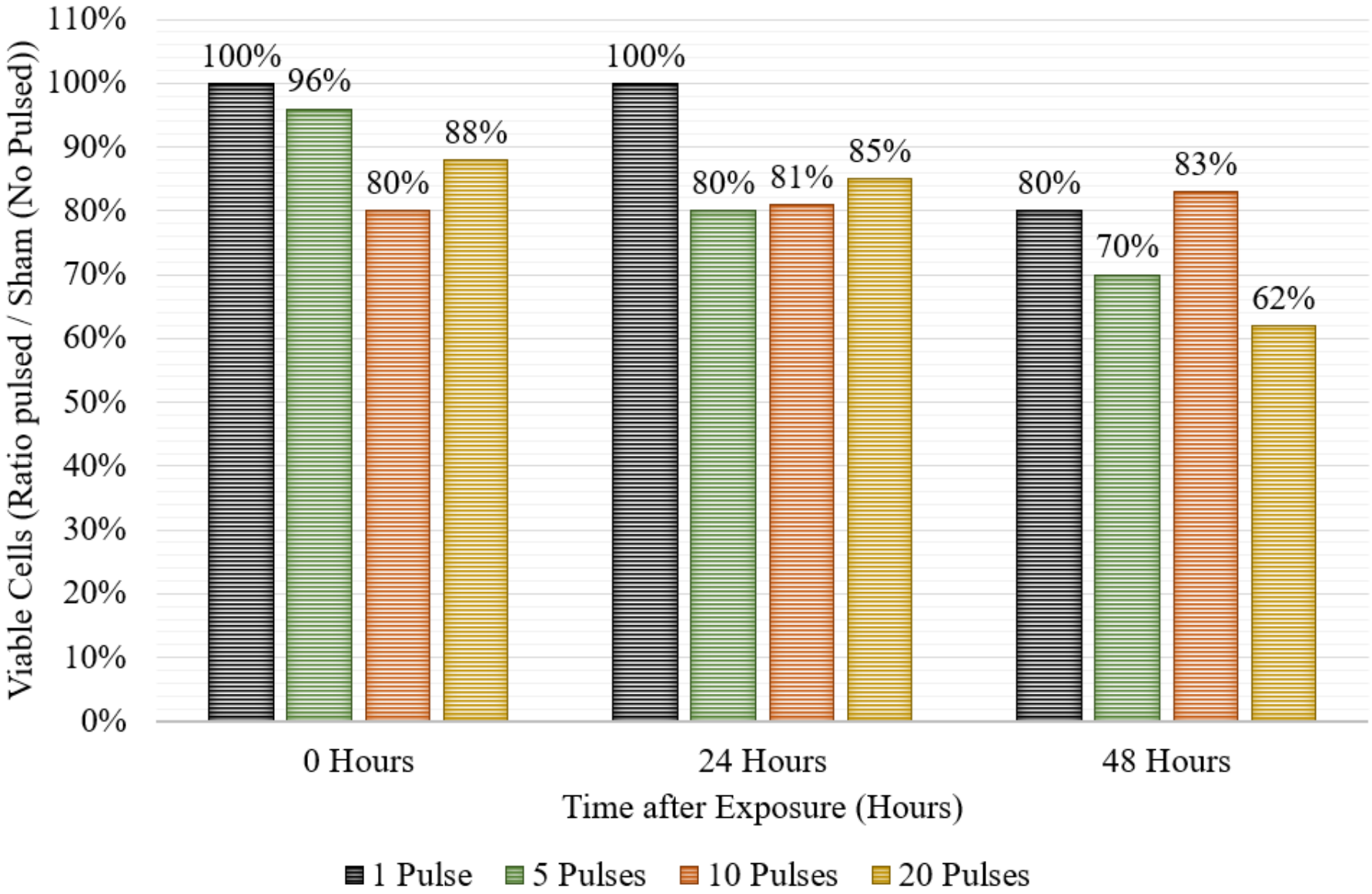


Fig. 4.9. Viability of cells 0, 24 and 48 hours after exposure to 200 ns pulsed electric fields, with 1.2 kV/mm electric field strength and 50 Hz repetition frequency

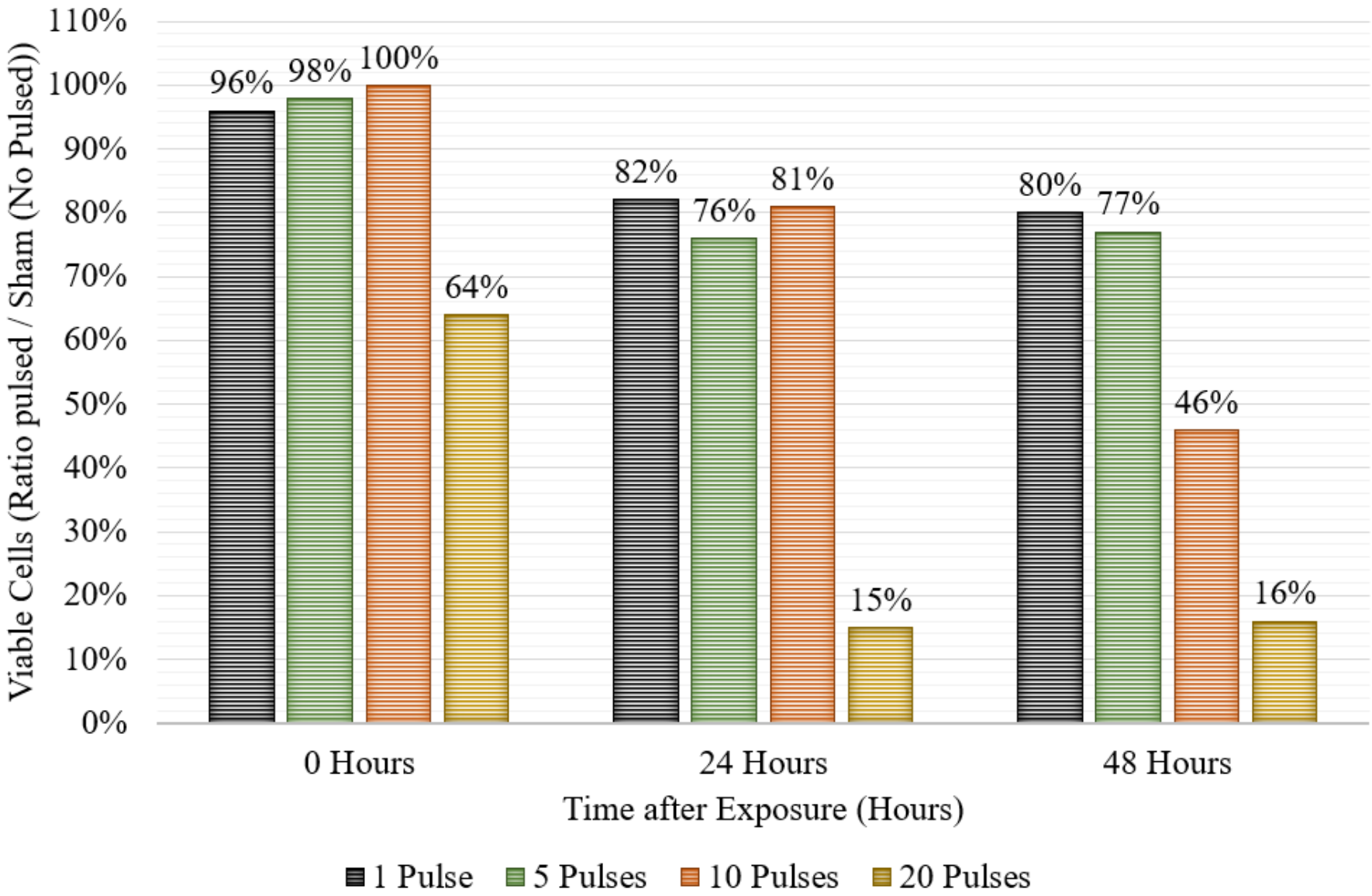


Fig. 4.10. Viability of cells 0, 24 and 48 hours after exposure to 300 ns pulsed electric fields, with 1.2 kV/mm electric field strength and 50 Hz repetition frequency.

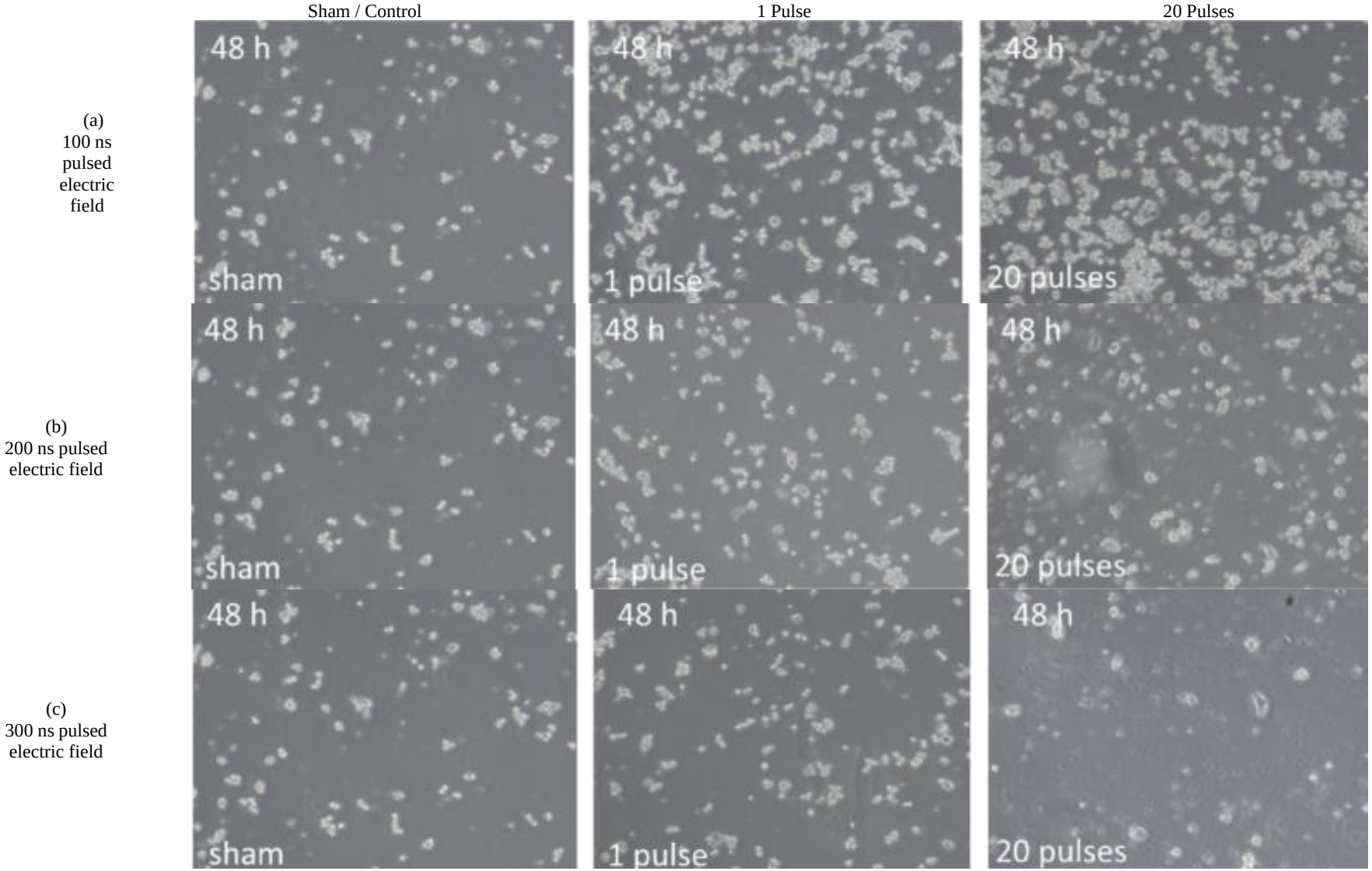


Fig. 4.11. Bright field images of D283 cells 48 hours after exposure to 1 and 20 pulses of (a) 100 ns (b) 200 ns and (c) 300 ns pulsed electric fields in comparison to a bright field image of the D283 cells 'sham' (control) sample.

Bright filed images 48 hours after exposure are shown in Fig. 4.11. These images confirm that the D283 Medulloblastoma enriched in cancer stem cells exposed to 100 ns and 200 ns PEFs are very slightly affected in comparison to the control. Cell viability and morphology appear to be more degraded following exposure to 10 and 20 pulses of 300 ns PEFs.

These observations lead to the hypothesis that D283 cells start to be irreversibly permeabilized when multiple pulses (more than 10) of 300 ns PEF, of electric field strength of 1.2 kV/mm (1.2 kV in amplitude), are delivered.

4.7. Thermal Effects

The short duration (hundreds of nanoseconds) and low repetition frequency (1 Hz to 50 Hz) of the PEFs delivered to the biological load (tissue or cells) were designed to ensure that the microbiological effect is nonthermal [8]-[9]. A non-thermal approach for neutralising or destroying cancer cells and cancer stem cells is an appealing alternative treatment approach as it would allow for targeted neutralization of a tumour without the thermal element of heating the cells above body temperature as seen with conventional ablation methods. More importantly, this effect would result in sparing healthy cells, the extracellular matrix (collagen) and nearby vessels whilst allowing tissue regrowth and preventing unwanted damage to critical patient organs and structures, such as the brain, bladder, and spine [8]-[9].

To verify that the nsPEFs parameters, as seen in Table 4.1, resulted in a nonthermal effect a cuvette heating analysis based on specific heat capacity can be manipulated to estimate the maximum thermal effect the biological system would experience.

The estimated temperature rises per pulse, ΔT, and the maximum mean rate of temperature rise, ΔT_{max}, the D283 cell line experiences with each nsPEFs parameters (Table 4.1) were calculated by equations (4.1) and (4.2). These calculations used the applied nsPEFs parameters (pulse duration, pulse amplitude, number of pulses and repetition rate) and the known parameters of the biological load (impedance, specific heat capacity, and mass).

$$\Delta T = \frac{E}{c\,m} \tag{4.1}$$

$$\Delta T_{max} = \frac{E}{c\,m} N \tag{4.2}$$

where E is the applied energy (Joules, J) that the D283 cell line experiences, c is the specific heat capacity ((J/Kg)/°C), and m is the mass (kg) of the biological load. In equation (4.2), *N* is the number of pulses the buffer solution is exposed to.

Since power is the number of joules of energy (E) per second (t) and power is the sequence of the electric field or voltage divided by the impedance, the energy delivered can be calculated by the parameters of the PEFs delivered and the load impedance as shown in (4.3).

$$E = \frac{V^2}{Z_L} t \tag{4.3}$$

where E is the energy delivered and is dependent on the parameters of the applied nsPEF. V is the nsPEF amplitude (Volts, V), Z_L is the impedance of the biological load (Ω), and t is the pulse duration of an applied nsPEF (seconds, s).

Also, m is the mass of the load that is a multiplication of the density (ρ) and the volume of a substance, therefore: $m = \rho . vol$.

The biological load consists of an impedance of 50 Ω [6] (as indicated in subsection 4.3) and a specific heat capacity of 4.186 (J/g)/°C, i.e., the same specific heat capacity as water. This is a valid approximation as the buffer solution consists mainly of water [6]. In addition to having the same specific heat capacity as water, it is assumed that the buffer solution has an identical density, ρ (kg/m^3), as water. The density of water is 1000 kg/m^3 or 1 g/cc. The volume (vol, m^3) is the volume of biological load that the Bio-rads commercially available 1 mm gap, 100 µl electroporation (EP) cuvettes can hold; this is 55 µm^3 (1 mm x 5 mm x 11 mm) [1]. The heat capacity of the D283 load is 0.23 J/K. This is highlighted in Table 4.2 below.

Table 4.2. Common characteristic parameters relating to the D283 load and cuvette

Equation	***Description***	***Symbol***	***Value***	***Unit***
-	Cuvette Length	*l*	1	mm
-	Cuvette Height	*h*	5	mm
-	Cuvette Width	*w*	11	mm
$\boldsymbol{vol = l\,h\,w}$	Cuvette Volume	*vol*	0.055	mm^3
-	Specific Heat Capacity	*c*	4.186	J/g/K
-	Density	ρ	1	g/cc
$\boldsymbol{m = \rho\, vol}$	Mass	*m*	0.055	G
$\boldsymbol{c\,m}$	Heat Capacity	*c m*	0.23023	J/K
-	impedance	Z	50	Ω

The estimated temperature rise per pulse, ΔT (4.1), and the maximum mean rate of temperature rise, ΔT_{max} (4.2) can be restated as (4.4) and (4.5) respectively. These temperature elevations are directly dependent on the nsPEF parameters.

$$\Delta T = \frac{\left(\frac{V^2}{Z_L}\, t\right)}{c\, m} = \frac{\left(\frac{V^2}{Z_L}\, t\right)}{0.23} \tag{4.4}$$

$$\Delta T_{max} = \frac{\left(\frac{V^2}{Z_L}\, t\right)}{c\, m} N = \frac{\left(\frac{V^2}{Z_L}\, t\right)}{0.23} N \tag{4.5}$$

Since the D283 cell line consists of a small fraction of the global solution volume, it could be assumed that the heating effect on the cell solution is the same as the heating effect on the simple buffer solution. Table 4.3 gives the estimated temperature rise per pulse (4.4) and the maximum mean rate of temperature rise (4.5) associated with the 50 Ω buffer solution when applying a range of pulse parameters (amplitude, pulse width and frequency). Assuming the repetition frequency is kept constant at 1 Hz.

The calculated rise in temperature the D283 biological sample experiences is the maximum temperature the biological sample should experience assuming that no heat, or temperature rise, is dissipated away from the exposure site by thermal conductivity between each pulse delivery. It also assumed that the nsPEF applied are ideal pulses, i.e., symmetrical square pulses with maximum amplitude and pulse duration.

Table 4.3. Estimated heating effect of applied nanosecond pulsed electric field on the buffer solution and D283 cells.

Pulse Width, t (ns)	***Peak Pulse Amplitude, V (V)***	***Impedance, Z_L (Ω)***	***Number of pulses, N***	***Heat Capacity, cm (J/K)***	***Temperature rises per pulse, ΔT (mK or m°C per pulse)***	***Maximum mean rate of temperature rise ΔT_{max} ((mK/s) or (m°C/s))***
100	1,000	50	1	0.23023	8.69	8.69
100	1,000	50	5	0.23023	8.69	43.44
100	1,000	50	10	0.23023	8.69	86.87
100	1,000	50	20	0.23023	8.69	173.74
200	1,200	50	1	0.23023	25.02	25.02
200	1,200	50	5	0.23023	25.02	125.09
200	1,200	50	10	0.23023	25.02	250.18
200	1,200	50	20	0.23023	25.02	500.37
300	1,200	50	1	0.23023	37.53	37.53
300	1,200	50	5	0.23023	37.53	187.64
300	1,200	50	10	0.23023	37.53	375.28
300	1,200	50	20	0.23023	37.53	750.55

This theoretical thermal investigation indicates that the change in the temperature of the biological load is dependent on the properties of the applied pulses. Our computation highlights that the short duration and lower repetition frequency of the nsPEFs delivered ensures nonthermal energy is delivered into the buffer solution, and therefore into the D283 cells [8]-[9]. Table 4.3 indicates that the maximum temperature rise the cells experience within the cuvette is 37.53 m°C. It indicated that the cells experienced a temperature rising of 0.75 °C in a second. This is when the most effective PEFs of 20x 300 ns pulses with 50 Hz repetition frequency are applied thus resulting in non-thermal irreversible

permeabilization of the D283 medulloblastoma cells. Therefore, it can be assumed that no heat is dissipated away from the surrounding environment (air, material, equipment etc.).

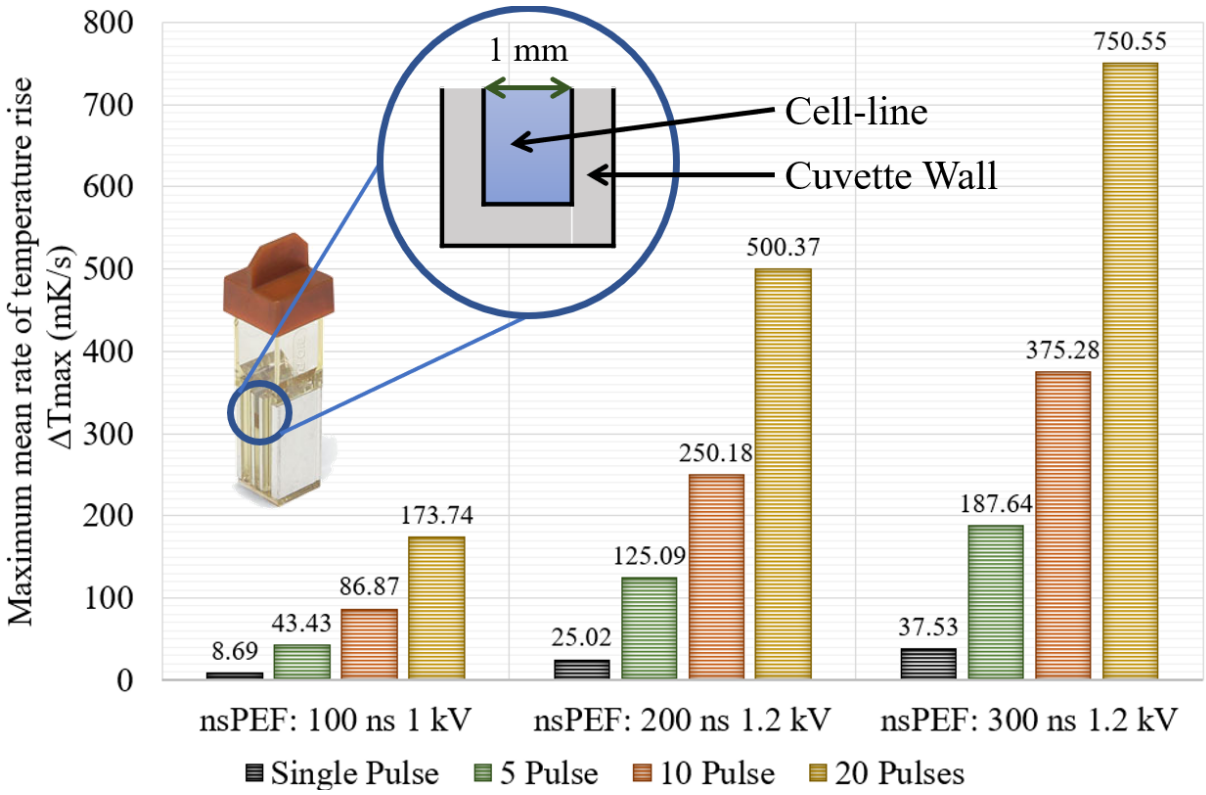


Fig. 4.12. Maximum mean rate of temperature rise ΔT_{max} the cell line load experiences when exposed to 1, 5, 10 and 20 pulsed electric fields of 100 ns, 200 ns and 300 ns in duration

The cuvette is designed to have a characteristic impedance of 50 Ω to absorb all the incident power or minimise reflections of the applied pulsed electric fields. When the peak amplitude of the electric field is 1200 V, and the pulse duration is 300 ns the peak power into a 50 Ω load impedance is 288 kW. If 288 kW is delivered to the cuvette for 300 ns then 8.64 mJ of energy is delivered into the load. The volume of fluid in the cuvette is 55 ml and 8.64 mJ of energy will increase the temperature of 55 ml of the D283 cell line suspended in water by 37.53 mK.

It is assumed the applied PEFs only heat the cell line within the cuvette and not the walls of the cuvette. The surface area of the perspex walls is 142 mm^2 and has a thermal conductivity of 0.21 W/m/K. Therefore, a temperature gradient of 0.07 K/mm would carry away all the heat from one pulse through the walls in a second. The repetition rate of the pulses applied is 50 Hz and therefore the temperature of the load within the cuvette would not increase in the allotted time between each pulse. If the thickness of the walls is 5 mm, then there would be about a third of a degree Kelvin across the walls [1]. All the fluid in the cuvette is less than 0.5 mm from a cuvette wall.

The temperature in the centre of the fluid in the cuvette is unlikely to rise more than one degree Kelvin, and this depends to a large extent on the heat transfer from the cuvette to the surroundings, which is affected by such things as the material of the holding brackets, the contact area and the amount of movement in the surrounding air.

To further demonstrate the absence of thermal effects, the temperature of the buffer contained in the electroporation cuvette was measured using a fibre optic probe (LumaSense OEM Modules, optic fibre dimensions 0.3 mm). The probe was directly placed between the electrodes before (1 min), during and after (1 min) of exposure to the pulsed fields. The worst-case exposure condition in bio-experiments of 20 pulses of 1,200 V field amplitude with 300 ns duration at a pulse repetition frequency of 50 Hz was used for this demonstration. As shown in Fig. 4.13, no macroscopic temperature increase was observed. Over three independent data acquisitions, the temperature measurement result indicated there was no significant increase in the D283 load temperature, thus reinforcing the numerical calculation and heat transfer via the cuvette argument presented previously.

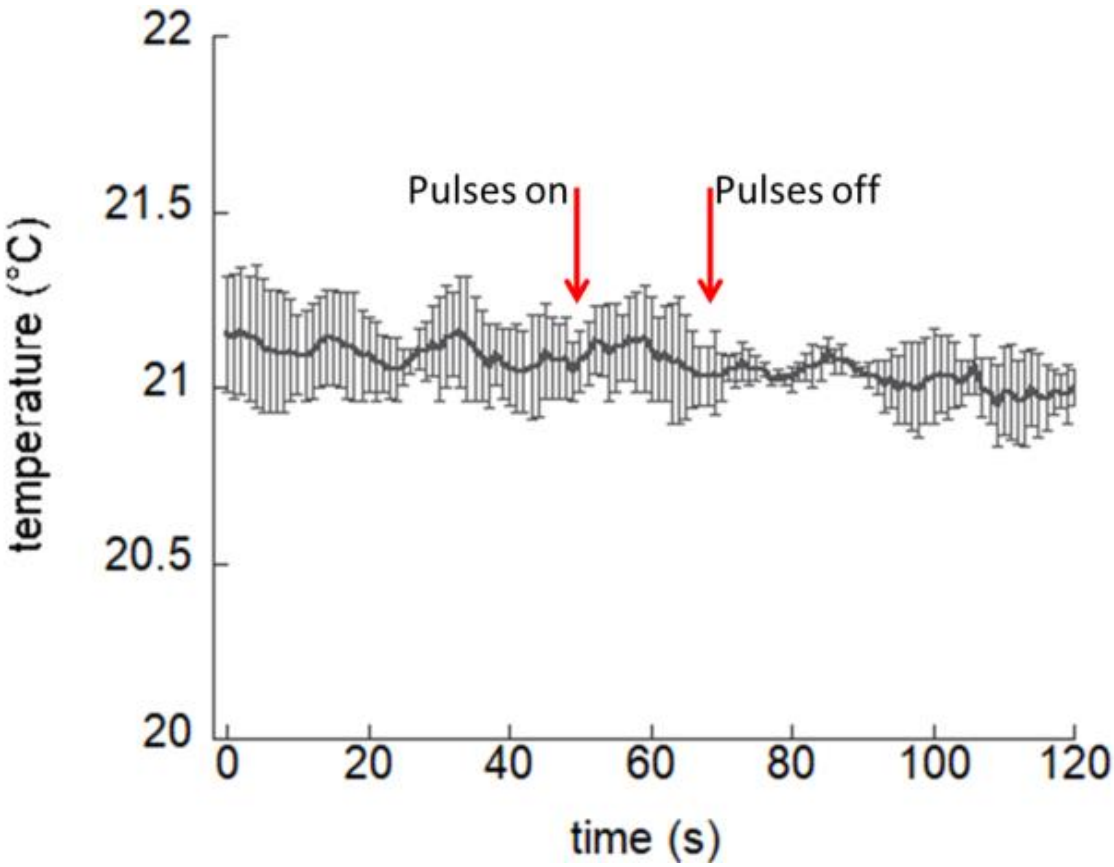


Fig. 4.13. Temperature trend within the electroporation cuvette electrodes before during and after 300 ns pulsed electric fields delivery. Bars represent standard deviation of the measurement over three independent acquisitions.

The thermal investigation of the applied nsPEFs confirms that the irreversible permeabilization (or neutralization) of the D283 Medulloblastoma cells that are enriched in cancer stem cells occurs when exposed to twenty pulsed electric fields of 300 ns in duration PEF with an amplitude of 1,200 V field

amplitude (or electric field strength of 1.2 kV/mm) with a repetition frequency of 50 Hz has no thermal effect on the cell line or would be bulk tissue load.

4.8. Conclusion

This chapter investigated the application of 100 ns to 300 ns PEFs with an amplitude of 1 kV or higher delivered into *in-vitro* loads. Verification and valuation of the ability of the slow nsPEF electroporation system to deliver nsPEFs onto cell lines, enriched in cancer stem cells have also been presented in this chapter.

The initial *in-vivo* investigation intended to gain preliminary data on the application of nsPEFs on cell lines that are heavily enriched in cancer stem cells before to the pre-clinical investigation of nsPEFs on bulk tissue is to be conducted. The results obtained indicate that the push-pull configuration of suitable power metal-oxide-semiconductor field-effect transistors (MOSFETs) for the generation of the nsPEFs is a suitable topology to achieve well-controlled nonthermal irreversible nanosecond electroporation (or neutralization), of cancerous cell line samples enriched in cancer stem cells. This indicates that nanosecond electroporation offers the possibility to become a favourable and novel clinical therapeutic energy source to displace traditional cancer treatment approaches and to shift treatment focus to targeting the cancer stem cells as highlighted in Fig. 2.2. Furthermore, this shift is made possible due to recent advances in semiconductor technology. In particular with the introduction of silicon carbon (SiC) MOSFETs.

The slow nsPEF electroporation system developed in this work was proven to be a very useful instrument that enabled microbiologists to conduct useful research on cancer stem cells. The ability of the electroporation system to provide a wide variety of pulse width, repetition frequencies, number of pulses, and amplitudes that can easily be adjusted by the user is of interest to the microbiologist in the area of cancer cell research. This versatile electroporation system is attractive as it supports a wide range of pulse protocols to determine the optimal PEF parameters for successful nonthermal neutralization of cancer cells and cancer stem cells.

The output from the electroporation system designed and developed in this work was impedance matched to the bulk applicator (cuvette with 50 Ω buffer solution and cuvette holder), delivering symmetrical electric field pulses with minimal ringing and overshoot into the biological load.

The overall system, including the generator, the cuvette housing unit, and buffer solution was used to successfully permeabilise D283 cells. It was demonstrated that more than 70% of the cell population were deemed to be permeabilized when 20 pulses of 200 ns duration (or longer), were delivered into the bulk load. Furthermore, a viability study, following permeabilization indicated that the majority (80%) of the D283 cell line population became irreversibly permeabilized when 20 pulses of 300 ns are delivered.

Further analysis indicated that the initial *in-vitro* investigation based on the application of 20x 300 ns PEFs from the slow nsPEF electroporation system successfully permeabilised 90 % of the cell population and 80 % of the population were irreversible permeabilised in a non-thermal manner. The increase in cell line temperature was measured and calculated to be 751 m°C and the maximum power of 432 mW was delivered into the load for this *in-vitro* nsPEF application. This indicated that even with the longer (300 ns) pulses, the effect was nonthermal.

Therefore, the primary *in-vitro* investigation of nsPEFs resulted in nonthermal neutralization of cancerous cell line, medulloblastoma D282, and this provides confidence that the new slow nsPEF electroporation system will successfully perform nonthermal ablation of bulk tissue, thus offering a viable solution to selectively destroying tumours within the human body.

The vision is that this compact nanosecond electroporation system will be used in clinical practice for targeted nonthermal neutralization of cancer stem cells and treatment of bulk tumours to offer a viable alternative cancer treatment solution, shifting from traditional cancer treatments such as chemotherapy and radiotherapy to an alternative and less traumatic solution.

4.9. Future Work

Before the slow nanosecond pulsed electric field electroporation system can be considered as an alternative cancer treatment for clinical applications, further investigation into the effects this energy has on cells and bulk tissue is required. This includes a portfolio of evidence to showcase safety and efficiency. For this to happen, electrosurgical instruments to harness and deliver this energy in a clinical environment are required. Following a pre-clinical investigation, clinical protocols will be generated to enable clinical use. At this stage, a full design history file will need to be put in place, together with the relevant documentation required for a quality management system that complies with ISO 13485 [10], and Food and Drug Administration (FDA) 510(k) clearance [11].

For this to become a reality and for nanosecond electroporation to be used to improve patient outcomes significant work will require both engineering development and clinical investigation fronts.

4.9.1. Engineering Development

The current electroporation system developed in this work can deliver 100 ns to 300 ns PEFs with amplitude in excess of 1 kV, into a load impedance of 50 Ω. One goal for the future is to develop an electroporation system capable of producing PEFs of amplitude in excess of 1 kV with user programmed in the pulse durations of between 100 ns and 100 µs and repetition frequency from 1 Hz to 50 Hz across a range of impedance loads from 10 Ω to 300 Ω. This would produce an electroporation system that would be capable of opening up the nanopores of cell lines and causing nonthermal ablation of bulk tissue loads in the nanosecond electroporation and microsecond time regime. Traditional

electroporation systems use microsecond pulses, so this system would enable combined ns and µs pulsed electric fields to be delivered.

Since this work, there have been further developments of higher voltage, faster switching MOSFETs that are now available commercially that would be better suited for this application. These new devices also have lower input capacitance and lower drain-source resistance ($R_{DS(on)}$) on values, thus reducing the current required to charge up the input capacitance for faster switching $\left(i = C\frac{dV}{dt}\right)$.

In the future, it may also be necessary to include a dynamic impedance matching circuit to match the energy from the generator into various tissue/bulk tissue loads. This could be a key feature when bulk tissue with a range of impedance is used as the load.

4.9.2. Cell line Investigation

The current slow nsPEF electroporation system is sufficient to further investigate the effect of nsPEFs on the D283 cell line as well as similar cell line populations, provided that the impedance of the load is 50 Ω or higher [6].

The next electroporation systems to be developed based on this topology would need to provide the ability to investigate the effect of nsPEF on various cell line populations that have a range of impedances without the need for a buffer solution. This could significantly advance and support further nsPEF-based investigations into cell line populations that could benefit the fields of regenerative medicine, electrochemotherapy and therapeutics.

One future cell line investigation work is to use an alternative dye to YOPRO-1. YOPRO-1 is a large molecular dye compared to others available and could highlight that electro-permeabilization or generation of nanopores occurs using shorter pulses or using a smaller number of pulses. This could be considered as future cell line investigatory work. Indeed, one interesting possibility highlighted in the literature reviewed in the literature search is that nsPEFs activate ion transport channels allowing for the movement and uptake of small ions. Ions such as Calcium (Ca), Sodium (Na), and potassium (K). These could be investigated using smaller dyes and specific cell markers such as Fluo4 to monitor cellular uptake and activation of ion channels.

Additional work that could be carried out is a verification of the nonthermal aspect of the work. The literature search also suggested that microthermal heating at the cellular level can be maintained by examining the fluorescence of Rhodamine B dye [8]-[9].

4.9.3. Pre-clinical investigation

For nsPEF to be considered as an alternative cancer treatment and part of the Creo medical advance energy platform in the future one must investigate the effect of nsPEFs on bulk tissue in a clinical

environment. As the nanosecond electroporation (nsEP) work carried out in this research has been at a cellular level, future investigation of nsPEF on bulk tissue should be conducted in a pre-clinical environment on bulk tissue. Future work would include repeating this initial investigation on bulk tissue in an *ex-vivo* setting, rather than the current cell line, in an *in-vitro* setting. This would be essential to transition from *in-vitro* to a clinical *in-vivo* environment.

Ongoing pre-clinical investigations including termination and survival studies would be required to fully understand and determine the effectiveness of nsPEFs as a clinical treatment on various organs associated with the human body.

Future work on clinical applications of nsPEF requires to be driven by a clinician, who fully understands the clinical needs and anatomic system. Therefore, a clinical road map for integrating the possible clinical applications of nsPEFs and identifying the clinical needs that will determine the future works. This work can be done to a certain extent using the current electroporation system developed in this research, whilst a more robust electroporation system is being developed.

4.9.4. Summary

In conclusion, the next iteration of the compact nsPEF electroporator could significantly open the field of nsPEF research and the possibility of *in-vitro* and *in-vivo* applications is limitless. A versatile generator is attractive to microbiologists, researchers, and clinicians.

The topology designed and developed in this work provided a versatile nsPEF generator that enabled preliminary microbiological investigation of nsPEF on the D283 Medulloblastoma cell line to be conducted. The conclusion from the microbiological investigation was successful permeabilization of D283 cells with more than 70% of the cell population was permeabilized when 20x 200 ns pulses with an electric field strength of 1.2 kV/mm were delivered. A viability study following the permeabilization investigation indicated that D283 cell lines were irreversibly permeabilized as cell viability and morphology were reduced when 20x 300 ns PEF with an electric field strength of 1.2 kV/mm were delivered. The cell permeabilization and viability investigation demonstrated that 20x 300 ns pulses with an electric field strength of 1.2 kV/mm enable targeted nonthermal ablation or neutralization of cancer stem cells in addition to normal cancer cells.

The vision is that the next development following the future work highlighted above will lead to a commercially available cost-effective compact nanosecond electroporation system unit that can form a part of an advanced energy electrosurgical system to achieve controlled and targeted nonthermal neutralization of cancer stem cells to offer viable alternative cancer treatment.

This initial investigation suggests that the cellular effect of exposure to nsPEFs offers advantages over conventional µs electroporation. This not only includes additional potentials for cell manipulation

and control of cell physiology and clinical effects. It can be concluded that nanosecond-pulse effects include calcium release, ion channel activation, and apoptosis induction on a cellular level [12]-[15]. It is believed that this is due to the shorter pulse duration.

It has also now been demonstrated in a recent pre-clinical, on bulk tissue, that the nanosecond pulses reduce cardiac and muscular impact. These findings were verified though looking at Electrocardiography (ECG) and measuring muscular contraction during pre-clinical trials in Chapter 6.

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CHAPTER V. FAST NSPEF ELECTROPORATION SYSTEM – TECHNICAL DESIGN

5.1. Introduction

This chapter describes the design, development, and evaluation of the fast nanosecond electroporation system that forms the second part of this work. This system was originally intended to be evaluated by microbiologists at the Italian National Agency for new technologies, energy and sustainable economic development (ENEA) for preliminary *in-vitro* investigation of nanosecond pulsed electric field (nsPEF) effects on Medulloblastoma cell lines, which were enriched in Cancer Stem Cells (CSCs). The fast nsPEF electroporation system was a key part of a multidisciplinary collaboration supported by the European Union's Horizon 2020 Framework. This programme was called the Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells (SUMCASTEC) [1].

Because of the restrictions that aroused from the Coronaviruses-19 pandemic and the SUCMASTEC timeline, the Medulloblastoma cell-lines investigation and system evaluation by microbiologists at ENEA did not materialise. Alternatively, the fast nsPEF electroporation system was used to investigate the effects of nsPEFs on bulk tissue in a preclinical environment at the Barcroft pre-clinical investigation facility in Cambridge.

This nanosecond electroporation system was developed for preliminary *in-vitro* investigation studies of nsPEFs, of between 10 ns and 300 ns pulse duration with amplitudes in excess of 1 kV (or electric field strength in excess of 1 kV/mm) and rise time less than 2ns. Ultimately, this system was to be used for preliminary investigation of the effect of nsPEFs on bulk tissue.

Following discussions with microbiologists, clinical researchers, and advisors as part of the SUMCASTEC research program and beyond, it was highlighted that there is an absence of commercially available nanosecond electroporation systems to investigate the effects of nsPEFs on cancerous bulk tissue and cell lines [2].

The agreed set of requirements for the fast nsPEF electroporation system by the SUMCASTEC consortium was as follows [2]:

- Fast Pulsed Electric Field Electroporation system requirements:
- Load impedance: 50 Ω;
- Pulse duration: 10 ns – 100 ns;
- Amplitude: 1 kV+;
- Repetition frequency: 1 Hz – 50 Hz;
- Number of pulses: 1 – 50;

The fast nsPEF electroporation system developed in this work is based on the relatively slow charging and rapid discharging of an open circuit coaxial transmission line (charged line) through a stack of avalanche transistors operating as a fast-switching element. The nsPEF duration is directly dependent on the length of the charged line, whilst the maximum nsPEF amplitude and transition time are dependent on the number of avalanche transistors that are stacked in series. The timing control for the system was managed by an external trigger signal from a commercially available pulse generator. The repetition frequency is limited by the associated charging time of the charged line [3]-[4].

5.2. Charged Line Technique

A charged line can be used as a technique to generate symmetrical rectangular pulses by charging a length of coaxial transmission line, that is open-circuited at the distal end, with a characteristic impedance of Z_0 and an associated time delay of T to a voltage level of V_{CC}, through a high impedance resistor, R_C, and then discharged into a load, Z_L, through a fast-switching element [5]-[6].

This method produces a rectangular pulse with a duration that is equal to twice the associated delay time, 2T, of the transmission line, and an amplitude of half the peak voltage level the transmission line was charged to, $\frac{V_{CC}}{2}$, provided that the load impedance, Z_L, is equal to the transmission lines characteristic impedance, Z_0, ($Z_L = Z_0$), and the high impedance resistor, R_C, is much larger than the transmission lines characteristic impedance ($R_C >> Z_0$). This topology is illustrated in Fig. 5.1 [5]-[6].

The transition times (rise and fall times) of the rectangular pulse generated across Z_L are determined by the switching element. Traditionally, a mechanical relay i.e., a mercury-wetted relay switch or a spark gap switch was used in conjunction with a charged line for pulse generation. Whilst the length of the transmission line determines the pulse duration (or pulse width) and the maximum repetition frequency is determined by how fast the line can be charged through the high impedance resistor, R_C. As $V_0 = V_{CC}\left(1 - e^{\frac{t}{\tau}}\right)$, were $\tau = R_cC_d$. The maximum amplitude of the generated pulsed electric fields (PEFs) is limited by the maximum voltage breakdown of the switching element and the transmission line used [6].

The delay time associated with a transmission line is determined by the relative permittivity, ε_r, of the dielectric material within the coaxial line and its length [5]-[6]. The delay (T) is found using equation (5.1) below:

$$T = \frac{l\sqrt{\varepsilon_r}}{c} \tag{5.1}$$

were T is the delay time associated with the line, l is the length of the line, ε_r is the relative permittivity of the dielectric material of the coaxial transmission line and c is the speed of light in a vacuum (2.99×10^8 m/s).

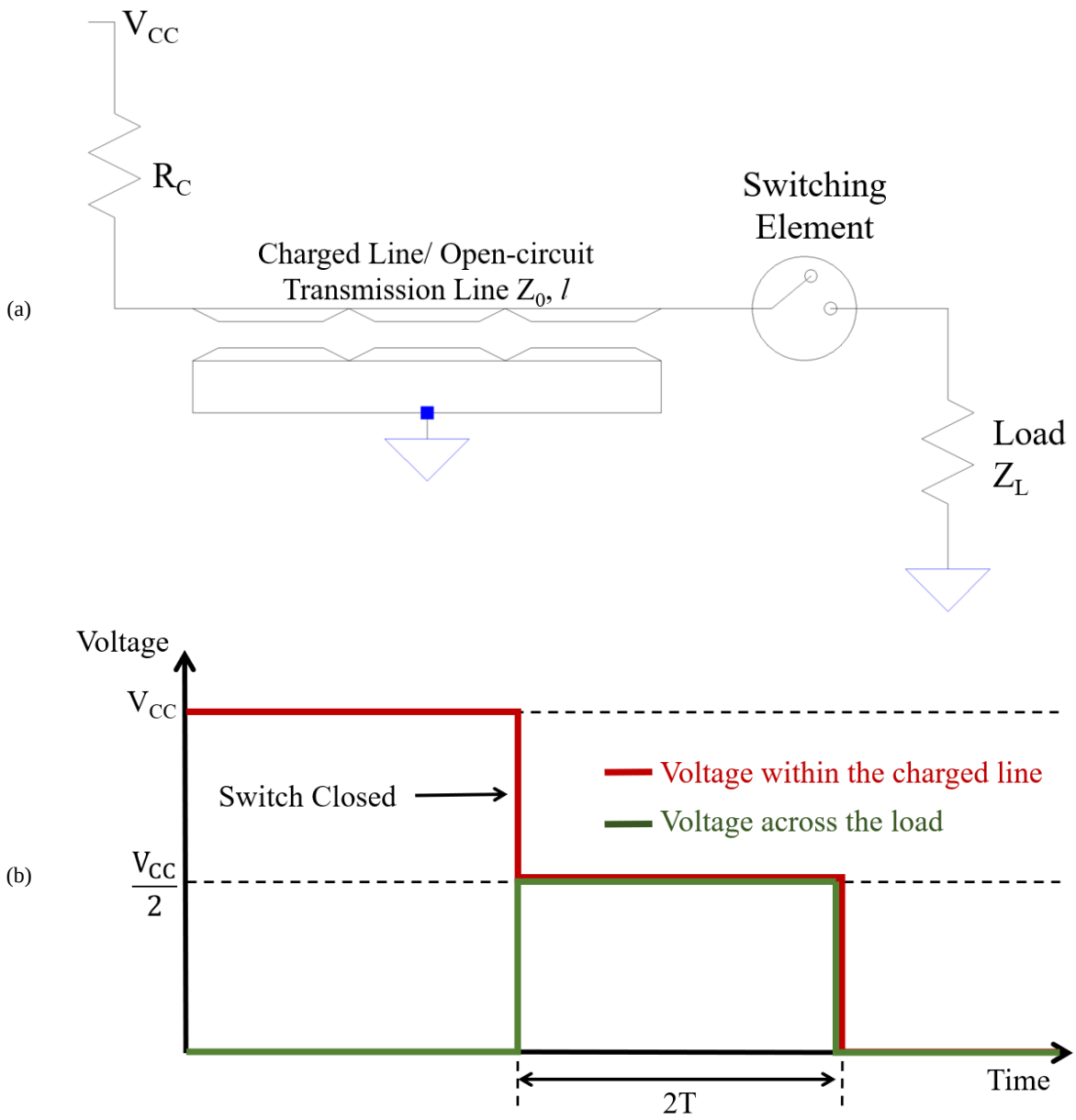


Fig. 5.1. Principle of an open-circuit transmission line technique for the generation of rectangular pulses (a) Basic circuit in principle (b) voltage waveform across the charged line (red) and across the load (Z_L) (green) [6].

The distal end of the transmission line is an open circuit, and the proximal end of the transmission line is connected to a direct current (dc) voltage source, through a high impedance resistor, R_C. The transmission line acts as a charged line (or a capacitor), with a total capacitance of C_d (5.2). When the switching element is open ('OFF'), the line is slowly charged up, from 0 V to the dc voltage level, V_{CC}, through the high impedance resistor R_C. It can be said that the line is fully charged in a time frame that is approximately five times the line charging time constant, $5\tau = 5\, R_C C_d$ (5.3).

$$C_d = l\, C_l \tag{5.2}$$

$$\tau = R_C C_d \tag{5.3}$$

where C_d, is the total capacitance of the delay line (F) and can be calculated by multiplying the length of the line, *l*, by capacitance per meter, C_l (F/m) given on the datasheet of the coaxial line used. τ is the time constant, and R_C is the impedance of the high-value resistor or charging resistor (Ω).

When the switching element is closed ('ON'), the charge stored in the line begins to be discharged through the load (Z_L). At this point, a voltage step travels through the line. As the distal end of the transmission line mimics an open circuit, this voltage step is reflected and travels back down the line towards the load [5]-[6].

This results in a pulse being generated at the load with a duration that is twice the associated time delay (T) of the length of the charged line, thus the duration of the pulse generated across the load is 2T, as indicated by Fig. 5.1 and equation (5.4). The pulse width generated is directly proportional to the length of a transmission or coaxial line used.

$$\text{Pulse duration} = 2T = \frac{2l\sqrt{\varepsilon_r}}{c} \tag{5.4}$$

where T is the delay due to the length of the line, *l* is the length of the line, ε_r is the relative permittivity of the dielectric material of the coaxial transmission line and c is the speed of light in a vacuum (2.99×10^8 m/s).

For efficient application, one end of the transmission line must mimic an open circuit. Producing a reflection coefficient (Γ) of +1 at the distal end of the line. The impedance of the high impedance resistor (R_C) must be substantially greater than the characteristic impedance of the transmission line (Z_0). The length of the line required to generate a specific pulse width can be reduced if the dielectric constant of the dielectric associated with the transmission line is increased (5.4) [6]. This reduction is proportional to the square root of the dielectric material. i.e., $T \propto \sqrt{(\varepsilon_r)}$.

The maximum repetition frequency of the PEF is limited to the time it takes for the open-circuit transmission line to be slowly charged to a voltage level through the high impedance resistor (R_C). To charge the line to 99% of the dc power supply voltage (V_{CC}) the charging time is five times greater than the associated time constant (τ) of the topology. The time constant (τ) is determined by the high impedance resistor (R_C) value and the associated total capacitance of the transmission line (C_d) (5.3) [5]-[7],[9]-[10]. Therefore, the maximum repetition frequency characteristics associated with the PEF generated by this topology are limited to a value of approximately $\frac{1}{5\tau}$:

$$f = \frac{1}{T} = \frac{1}{5\tau} = \frac{1}{5R_C C_d} = \frac{1}{5R_C l C_l} \tag{5.5}$$

where *f* is the repetition frequency, T is the period or repetition rate of the nsPEFs, τ is the associated time constant, R_C is the high impedance resistor value, C_d is the total capacitance of the delay line, C_l is the capacitance per meter of a transmission line and *l* the transmission line length.

5 τ (=$R_C C_d$) is the time constant of the circuit for the line to be charged to 99 % of V_{CC} as $V = V_{CC}\left(1 - e^{-\frac{t}{\tau}}\right) = V_{CC}\left(1 - e^{-\frac{5R_C C_d}{\tau}}\right) = V_{CC}\left(1 - e^{-\frac{5R_C C_d}{R_C C_d}}\right) = V_{CC}(1 - e^{-5}) = V_{CC}(1 - 6m) = V_{CC}0.99$ = 99 % of V_{CC}.

The amplitude and shape/reflection of the incident pulse across a load (Z_L) is determined by the relationship between the characteristic impedance of the transmission line (Z_0) and the impedance of the incident load (Z_L). This phenomenon can be described using low-frequency (circuit theory) and high-frequency microwave theory [5]-[8].

5.2.1. Low Frequency Theory

In low frequency or dc terms, the relationship between the characteristic impedance of the transmission line, Z_0, and the incident load, Z_L, function as a potential divider between the V_{CC} supply voltage and ground and determines the incident PEF amplitude [5]-[6], [11]-[13]. This relationship is demonstrated in Fig. 5.2 and the following equation.

$$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC} \tag{5.6}$$

where Z_0 is the characteristic impedance of the charged line, Z_L is the load impedance, V_{CC} is the supply voltage (and is also the voltage level the charged line is charged to), and V_L is the amplitude of the nsPEF across the load.

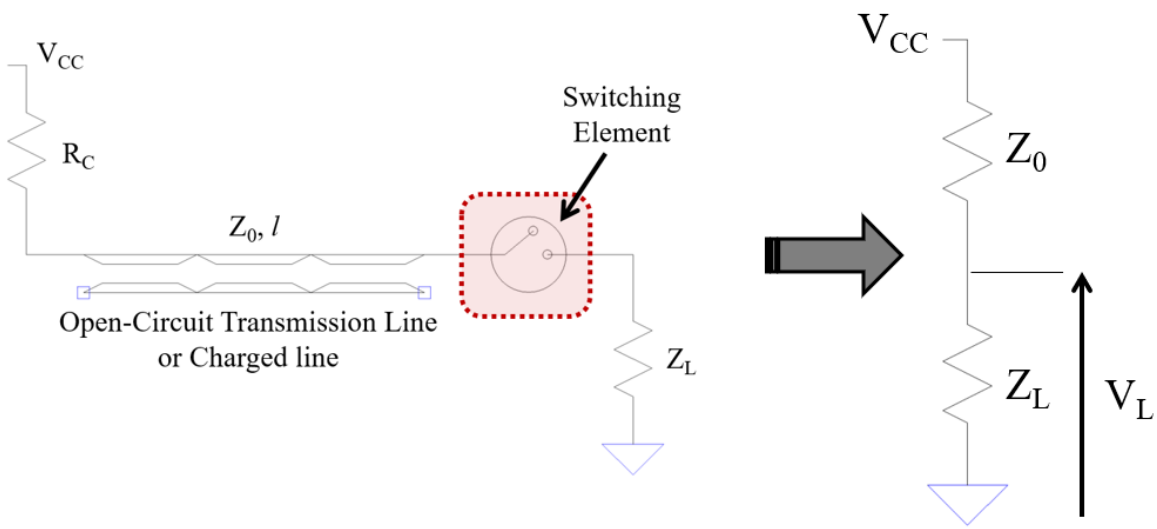


Fig. 5.2. Principle of an open-circuit transmission line technique [6] and its potential divider equivalent circuit

From (5.6), the larger the load impedance is in comparison to the characteristic impedance of the charged line the larger the incident pulse amplitude across the load will be. If Z_L was much larger than Z_0 ($Z_0 << Z_L$) the amplitude of the PEF would be very similar to the voltage level the charged line is charged to, V_{CC}. The issue that arrives when making this the case is that the voltage reflection will occur (this is addressed in the next section).

5.2.2. High Frequency (Transmission Line Theory)

Since the pulsed fields are in the nanosecond time regime, and associated transition times in the sub-nanosecond time regime, high-frequency microwave theory needs to be considered. The relationship between the characteristic impedance of the transmission line (Z_0) and the incident load (Z_L) determines the reflection coefficient (5.7), and therefore the shape of the pulse generated across the load.

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{V^-}{V^+} \tag{5.7}$$

where Γ is the reflection coefficient, Z_0 is the characteristic impedance of the transmission line, and Z_L is the load impedance. V^+ is the incident wave and V^- is the reflected wave.

The reflection coefficient (Γ) is a parameter that describes how much of a wave is reflected by an impedance discontinuity along the transmission line. It is equal to the ratio of the amplitude of the reflected pulse to the incident pulse, as illustrated in Fig. 5.3 [5]-[6].

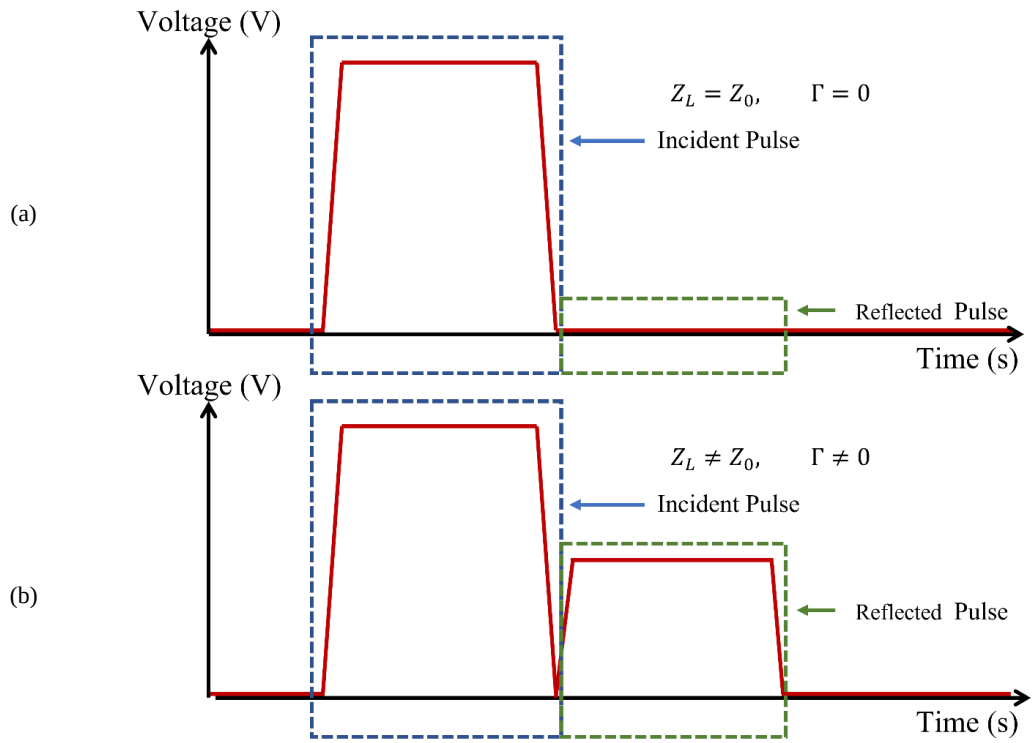


Fig. 5.3. Incident and reflected pulse across a load dependent on the relationship between the load and charged line impedance ratio (a) $Z_L = Z_0$, $\Gamma = 0$ (b) $Z_L \neq Z_0$, $\Gamma \neq 0$

For the generation of a single symmetrical rectangular PEF with no reflection, the load impedance must match the characteristic impedance of the charged line. $\Gamma = 0$ when $Z_L = Z_0$. A reflection coefficient value differing from 0 will cause a second reflected pulse at the load. The extent, or amplitude, of the reflected pulse is dependent on the load impedance and the characteristic impedance of the transmission

line. The closer the load impedance is to the transmission line characteristic impedance the smaller the amplitude of the reflection will be.

5.2.3. Incident Pulsed Electric Fields Across the Load

The shape and amplitude of the PEFs across a load are dependent on the relationship between the characteristic impedance of the transmission line and the load impedance due to the low (5.6), and high (5.7) frequency components within the nsPEF generated and the charged line topology.

For the generation of a single nsPEF, a system reflection coefficient of zero must be achieved. This is achieved when the characteristic impedance of the transmission line is the same as the load impedance at all frequencies, i.e. $Z_L = Z_0$, therefore $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_L - Z_L}{Z_L + Z_L} = \frac{0}{2Z_L} = 0$. The resultant PEF amplitude across a load would be half of the dc power supply voltage (V_{CC}). This is the situation required for the generation of a single incident nsPEF with minimum reflection. i.e., $V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC} = \left(\frac{Z_L}{Z_L + Z_L}\right) V_{CC} = \left(\frac{Z_L}{2Z_L}\right) V_{CC} = \frac{V_{CC}}{2}$.

5.3. Avalanche Mode Transistors

For the generation of fast symmetrical PEFs in the nanosecond regime, avalanche mode transistors were identified as the fast-switching element which could provide a fast transition time (rise time) in the sub-nanosecond range. Literature indicates that transistors operating in avalanche mode, or avalanche transistors, can be used as a high-speed switching element to generate sub-nanosecond rise times down to 300 picoseconds (ps) [9]. Combining avalanche transistors with the operation of the charged line technique discussed is a possible solution for a nsPEF electroporator system that can produce high voltage nsPEFs, with transition times in the sub-nanosecond time regime.

5.3.1. Avalanche Mode Operation

When driving a conventional transistor in its avalanche region the operating voltage/current must be carefully controlled to avoid latch-up. Under some conditions, operating a transistor in the avalanche region can result in permeant damage to the device. However, operating a transistor correctly in its avalanche mode can result in fast high voltage/current switching [6], [10]-[12].

Avalanche mode operation utilises the negative-resistance characteristics of a transistor in its voltage – current (V – I) or collector-emitter voltage (V_{CE}) – collector current (I_C) curve [9]. The V_{CE} – I_C operation curve of a basic avalanche mode operation for an NPN transistor circuit given in Fig. 5.4 was achieved by operating a transistor in its common-emitter circuit topology [6], [10]-[12].

Initially, $I_{BR} = K_1$ is a small reverse current which holds the transistor at operating point B, as shown in Fig. 5.4. If a positive trigger voltage is applied at the trigger input shown in the circuit inset

in Fig. 5.4, the transistor switches 'ON'. The base current is then reduced to zero and the operating point shifts from point B to Point A' on the $I_B = 0$ curve. The rapid speed at which the transistor shifts from point B to A' is the main attraction of utilising avalanche mode operation as a fast-switching element [10]. When the trigger voltage is switched 'OFF', the operating point of the transistor shifts from point A' to A and remains at operation point A [10]. The switching operation of an avalanche mode transistor has two stable states, operation point A and B. To return to operating point B it is necessary to apply a sufficient reverse current to allow only one stable condition. A small negative trigger signal accomplishes this, as indicated by $I_{BR} = K_2$ [10].

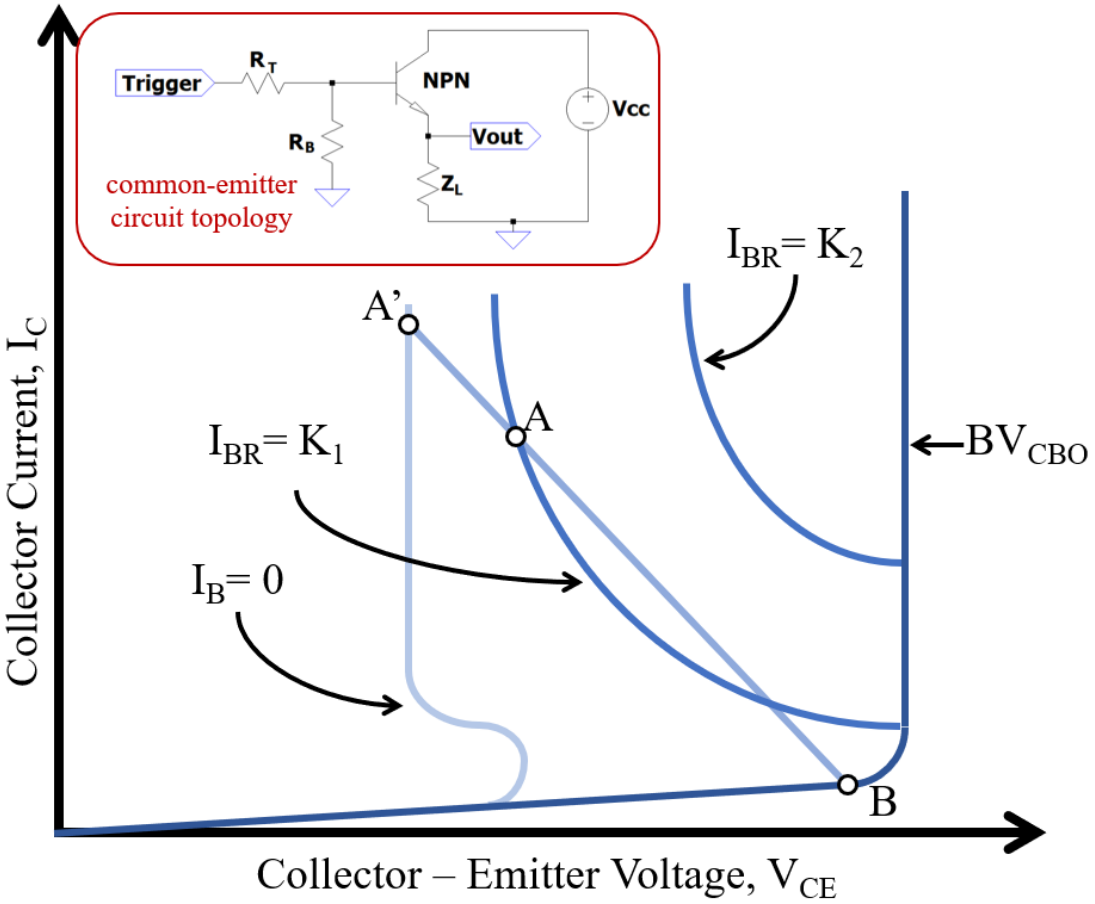


Fig. 5.4. Collector-emitter voltage (V_{CE}) – collector current (I_C) load curve line for an avalanche mode switch operation of an NPN transistor in a common-emitter circuit topology [10]

Because of the instability issues associated with the negative resistance region of a transistor in avalanche mode, avalanche mode circuits are normally alternating current (ac) coupled. A thorough characterisation of a transistor's avalanche region is necessary to properly utilise a transistor operation in avalanche mode for the application as a fast-switching element [10].

5.3.2. Avalanche Breakdown Theory

Avalanche breakdown occurs when a reverse bias is applied to a semiconductor PN junction, which produces a large electric field and accelerates mobile charge carriers through impact ionization within

the crystal lattice. Mobile charges, such as electrons are accelerated by the electric field across the PN junction and move through the crystal lattice in the depletion region of the PN junction. These accelerated electrons gain energy as they eventually collide with atoms within the lattice. If the electrons gain sufficient energy before the collisions, they will disrupt the atomic bonds of the atom they collide with and release electrons. This is known as impact ionization. Upon releasing an electron, a hole is simultaneously generated in the lattice. Now there are freely moving and accelerated particles within the crystal lattice and each freely moving and accelerated particle may participate in the impact ionization process. This creates an 'avalanche' effect of charged particles and results in a large current flowing through the junction [6], [10], [13].

As this effect occurs at high electric fields and high carrier velocities, recombination can be neglected, and the effect is regenerative. This process can be described by a multiplication factor, M. The multiplication factor can be defined as the number of electron-hole pairs produced per carrier entering the depletion layer. Miller [13] described the behaviour of the multiplication factor through the reverse junction voltage (5.8):

$$M = \frac{1}{1 - \left(\frac{V}{BV_{CES}}\right)^{m}} \tag{5.8}$$

Where V is the applied voltage (or reverse junction voltage), *m* is the empirically determined constant that is dependent on the semiconductor material used for the transistor, and BV_{CES} is the avalanche breakdown voltage (or collector-emitter breakdown voltage) of the transistor. The breakdown voltage is the voltage level where the multiplication factor, M becomes infinite [6], [10], [13].

Fast low-current switching can allow voltages up to the avalanche breakdown voltage (BV_{CES}) to be employed with circuits that consists of a capacitive load and delay/charged lines. Circuits using avalanche breakdown transistors should be defined with the worst-case circuit conditions such as high temperatures, minimum turn 'OFF' drive, maximum collector supply voltage, and loads that produce a load line that is inductive in shape.

5.3.3. Operation of a Single Avalanche Mode Transistor Circuit

The operation of a single avalanche mode transistor circuit, shown in the circuit inset in Fig. 5.4, is illustrated by the negative resistance region in the V_{CE} – I_C breakdown curve as shown in Fig. 5.5. This operational mode of a transistor in its avalanche breakdown region is regenerative.

At operating point D in Fig. 5.5, the available reverse base current to the transistor is constant and the collector supply voltage or the collector-emitter voltage (V_{CE}) is in the region of the transistor's breakdown or avalanche breakdown voltage (BV_{CES}) and the emitter junction of the transistor is

reversed biased. As the collector supply voltage (V_{CE}) is close to the avalanche breakdown voltage (BV_{CES}) the multiplication factor (M) is large [10].

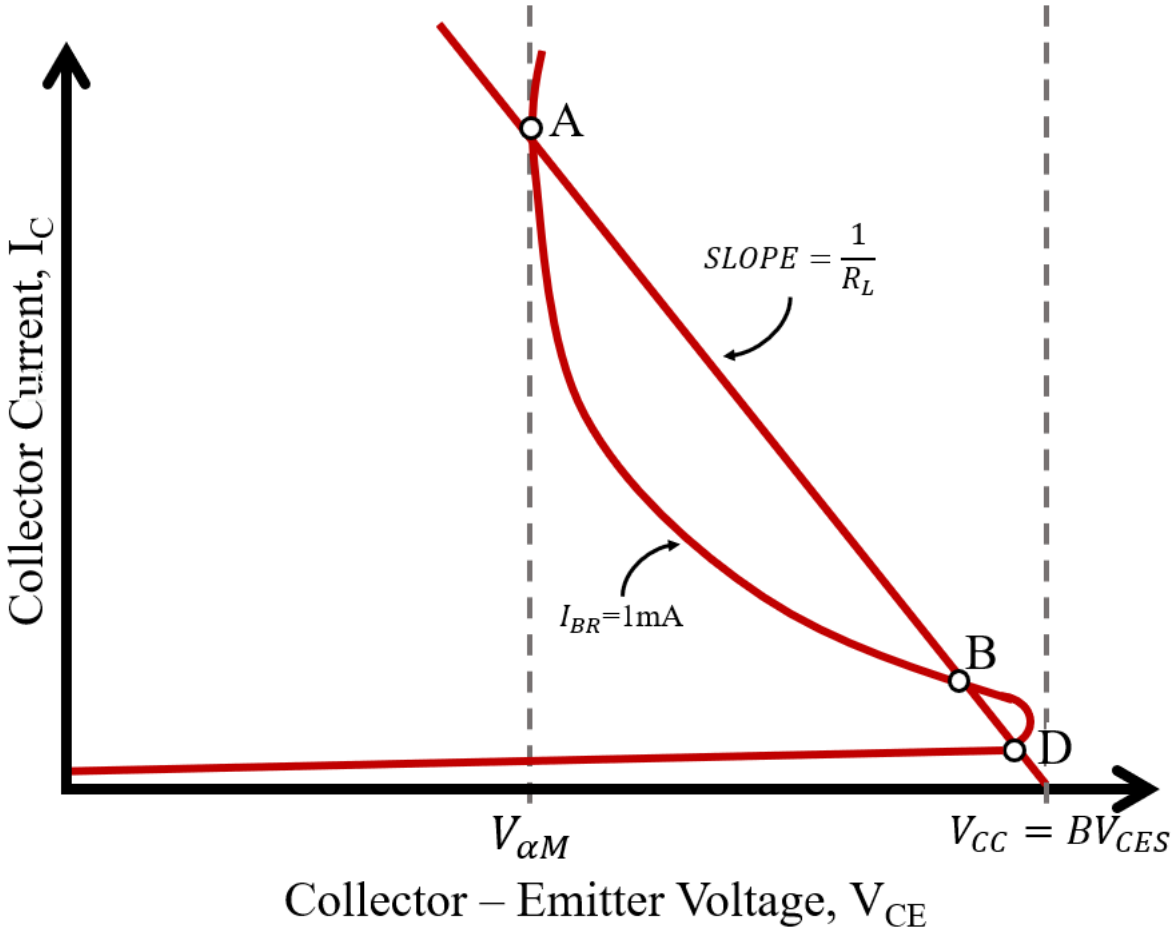


Fig. 5.5. Load line for the operation of a single avalanche mode transistor circuit [10]

In summary, a small current is injected into the emitter terminal, causing the emitter junction to become forward biased. When the injected current reaches the collector junction, it has been multiplied by a factor of M, the multiplication factor. The base current is held at a constant value and therefore the increase of the collector current results in a similar increase of the emitter current as the voltage supply (V_{CC}) cannot store current. This regenerative process continues as the current builds up; the collector voltage decreases, which in turn decreases M. This build-up progresses gradually until an equilibrium condition is reached. This condition is the operating point A, as shown in Fig. 5.5, where regeneration is no longer possible. The operating point of the transistor will remain at point A until an external trigger/signal is applied to cause the operating point to move back to point D. Therefore, the operation of a single avalanche mode transistor circuit exhibits bistable operation, moving regeneratively from operating point D to A, and A to D depending on an applied external trigger signal [10].

The operation of a single avalanche mode transistor circuit can be described in more detail by considering three operating points (A, B and D) intersecting a load line with the transistor characterises shown in Fig. 5.5. Investigating the potential stability of these points is of great importance when

considering the application of the device. The stability of a static operating point can be found by representing the circuits by its equivalent model and finding their natural resonant frequencies. If any frequency corresponds to a growing transient, the operating point is unstable because any disturbing signals will grow in time. This will cause the circuit operation to move in the direction of the disturbing signal until a stable point is found [10].

Using pole-zero theory, the natural resonant frequency of the transistor circuit can be found by inspecting the equivalent circuit. The equivalent circuit consists of three passive components connected in parallel. Two resistors, r_A and Z_L and a capacitor C_A and can be determined by equation (5.9) below.

$$S = -\frac{g + G}{C_A} \tag{5.9}$$

where S pole location determines if the circuit is stable or unstable, C_A is the internal avalanche capacitance, g is the avalanche conductance $\left(g = \frac{1}{r_A}\right)$ and G is the load conductance, $\left(G = \frac{1}{Z_L}\right)$, where r_A is the avalanche resistance and Z_L the load impedance [10].

If the value of S is negative, the pole is on the left-hand side of the complex S plane and the avalanche transistor operation is stable. On the $I_E = 0$ A curve, the operation is stable as the value of both g and C_A are positive. However, in the region where $I_C > M\ I_{CB}$, both g and C_A are negative and to have a stable operation and for S to be a negative value, the load resistance, Z_L, must be larger than the avalanche resistance, r_A ($Z_L > r_A$). The point where $Z_L = r_A$ is the boundary between the stable and unstable operation of the single avalanche mode transistor circuit. At point A in Fig. 5.5, the circuit is stable and $Z_L > r_A$, while on operating point B in Fig. 5.5, $Z_L < r_A$ and the circuit is unstable. These characteristics of the avalanche region are typical of a group of negative resistive devices. These are called open circuit stable devices, which are stable at any point under the condition where $Z_L \rightarrow \infty$ [10].

The switching time of an avalanche mode transistor is independent of the load resistance due to the inter-relationship of the behaviour of the internal avalanche capacitance (C_A) and its $V_{CE} - I_C$ characteristic. The switching time, (or the rise time) is the time it takes to move from point D to point A, as shown in Fig. 5.5. The mathematical expression for the rise time is extremely complex and is not of significant value for a circuit designer and is generally not provided on an avalanche mode transistor datasheet. The fall time is the reverse of the current build-up or the decay of the current which is the time it takes to move from point A to point D, as shown in Fig. 5.5. [10].

5.3.4. Load Lines in the Avalanche Region

The mechanisms of a simple avalanche circuit are expressed in more detail in Fig.5.7 in comparison to Fig. 5.5. The operation of a simple avalanche circuit starts at point A in Fig. 5.6, where $I_{BR} = 1$ mA.

To trigger the circuit, the avalanche resistance is higher than the load impedance ($r_A > Z_L$). This condition can be achieved in two ways [10].

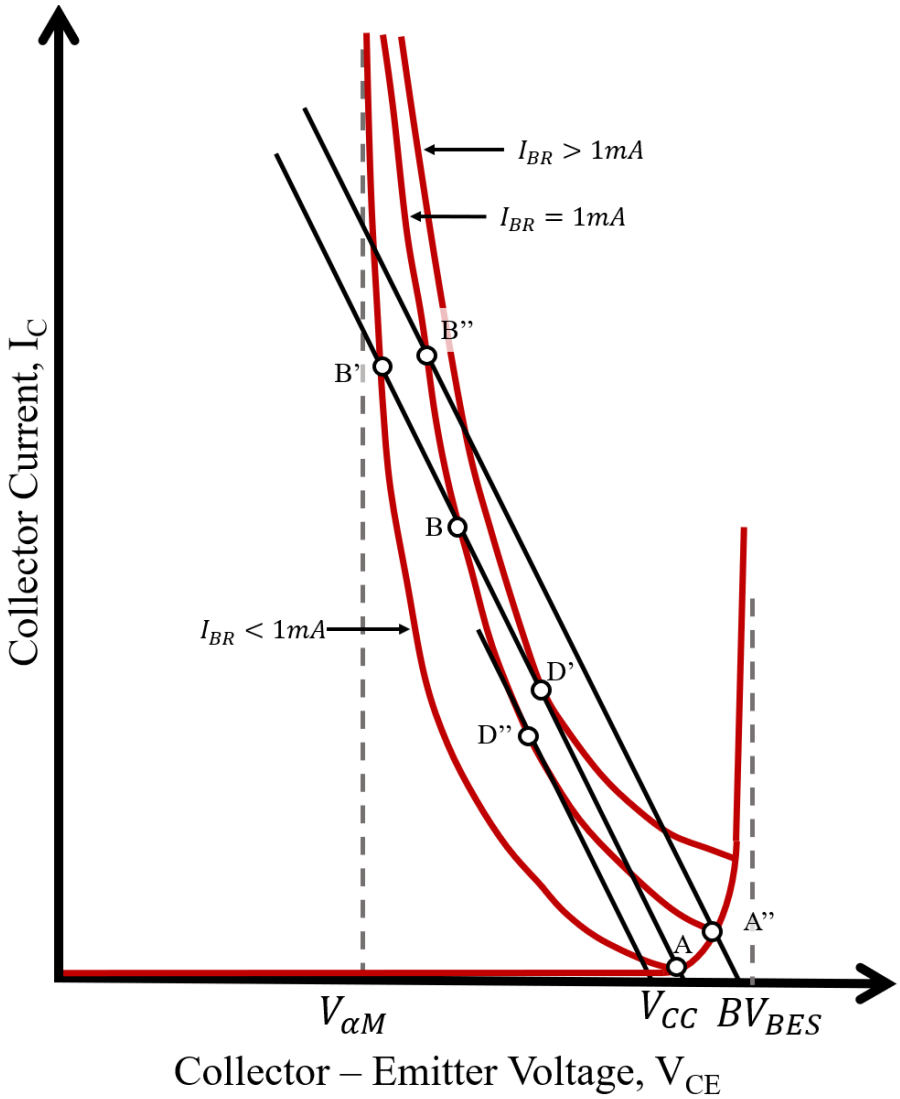


Fig. 5.6. Collector-emitter voltage vs collector current characteristic curves and load lines in the avalanche region [10]

The first condition involves lowering the base current, causing the operating point at point A to become unstable ($Z_L < r_A$). Once the transistor is in its negative resistance region, the base current is restored to 1 mA, where the only stable operating point is at point B, as shown in Fig. 5.6. However, if the trigger is still present at the end of this switching time, the operation will be at point B' [10].

The second condition is when the collector voltage could be increased, causing the load line to shift from point A to A". At this point, $Z_L < r_A$, and the circuit will be triggered. Again, the stable point will be at point B, as seen in Fig. 5.6 when the trigger is removed or at B" with the trigger present [10].

To turn the avalanching transistor 'OFF', or traverse to point A, the condition $Z_L < r_A$ must be met again. This can be met by the inverse of either of the methods described above. This is achieved by increasing I_{BR}, which would move the operating point to D' or V_{CC} could be lowered below the

avalanche breakdown voltage (BV_{CES}), which would move the operating point to point D", as seen in Fig. 5.6. Both D' and D" operating points are unstable points, which would cause the circuit to trigger in the direction of the disturbance and the operation would move back to point A [10].

The operation of the circuit follows must lie on the load line. The analysis assumes that the device can be represented by a single non-linear resistance in parallel with a non-linear capacitance.

5.3.5. Design Considerations

Transistor Selection

When selecting a transistor to operate efficiently and non-destructively in its avalanche region, the characteristics of the transistor must be understood. The primary characteristics are the collector-emitter breakdown voltage, the 'ON' state voltage and the mean power the device can dissipate [9].

Avalanche transistors are bipolar junction transistors that can be operated in the region of their collector-current and collector-to-emitter voltage characteristics beyond their collector-to-emitter breakdown voltage. This is the avalanche breakdown region. Transistors not specifically designed for avalanching can have reasonably consistent avalanche properties. An example of this was found by the inventor Jim Williams in 1991 when operating a 2N2369 transistor in its avalanche breakdown region to produce nsPEF through avalanche breakdown with rise times of 350 ps or less, using a 90V power supply [14].

Avalanche transistors are specifically designed to operate in the avalanche breakdown region to produce avalanche breakdown pulses with rise times in the sub-nanosecond region [15]. Examples of transistors that have been designed and proven to operate in their avalanche region are identified in Table 5.1.

Table 5.1. Avalanche transistors characteristics

Part Number	Max. Collector-Emitter Breakdown Voltage, BV_{CES} (V)	Min. operation Collector-Emitter Voltage, V_{CEO} (V)	Emitter-Base Breakdown Voltage, BV_{EBO} (V)	Max Continuous Collector Current, I_C (mA)	h_{FE}	Transition Frequency (MHz)	References
2N2369	40	15	4.5	200	40-120	>500	[16]
FMMT411	80	15	7	600	100	40	[17]
FMMT413	150	50	6	100	50	150	[18]
FMMT415	260	100	6	500	25	40	[19]
FMMR416	315	100	7	500	100	40	[20]
FMMT417	320	100	6	500	25	40	[19]
ZTX415	260	100	6	500	25	40	[21]

Collector-emitter breakdown voltage or avalanche breakdown voltage (BV_{CES}) is the main transistor characteristic that determines the operation of an avalanche breakdown transistor as a fast switch for the generation of high voltage nsPEFs. To obtain a high voltage pulse, the transistor must

have a high BV_{CES}. If the power supply or the voltage between the collector and the emitter of the transistor exceeds the transistor's avalanche breakdown voltage it would permanently breakdown the transistor to a point where the device could not recover.

Another important parameter to consider is the minimum voltage required for avalanche operation. Below this minimum collector-emitter voltage, V_{CEO}, the device has the switching characteristic of a device operating in a non-avalanche mode. V_{CEO} is measured when the transistor's base terminal is left open circuit, with a base current, $I_B = 0$, and emitter current, $I_E = 0$. This 'starting' voltage is dependent on the external circuitry around the device. For a simple single capacitor arrangement, this point is seen to vary and is shown on an avalanche transistor datasheet as the minimum starting voltage as a function of capacitance.

The datasheet for the particular avalanche transistor can provide the necessary operating circuit and characteristics. This includes the minimum voltage required for avalanche operation as a function of capacitance for different drive currents and the minimum starting voltage as a function of drive current. The rate of change of drive current is relevant to an avalanche transistor operating as a fast-switching element. A lower starting voltage may be achieved by using a faster changing drive current [6], [9]-[10], [16]-[21].

The 'ON'-state characteristic of an avalanche transistor is an important characteristic to consider. This characteristic defines the maximum avalanche current (I_{USB}), or the current passed in the secondary breakdown condition, and it illustrates an avalanche transistor's capability of producing a high avalanche current. The datasheets show the maximum peak current as a function of pulse width for a sinusoidal-like pulse of an avalanche transistor [19]. The curve showing the 'ON'-state characteristic of an avalanche transistor highlights the reliability testing or lifetime test of a Diode Incorporated avalanche transistor.

The lifetime test for a diode-incorporated avalanche transistor FMMT415 indicates the device can produce current pulses of up to 60 A peak and 10ns pulse width for over 4×10^{11} times without failure [19]. Curve 2 and curve 3 also indicate the lifetime or operation till failure. The second curve for the FMMT417 transistor indicates the transistor can operate 10^7 times until failure (curve 2), and 10^3 times until failure, (curve 3) [9]. See datasheet for FMMT417 avalanche transistor in Appendix V [9]. The avalanche current is again illustrated in the datasheet I_{USB} v temperature for a typical device, showing its temperature dependency for specific operating conditions [16]-[21].

5.4. Final Topology

A nsPEFs can be generated by using an avalanche transistor in conjunction with a charged storage method, such as a charged line that is an open circuit at its distal end. This is commonly known as a delay-line pulse generator and is an effective circuit for generating either a positive or negative

symmetrical rectangular pulse with controllable pulse durations. Fig. 5.7 illustrates the basic circuit for such a pulse generator. This circuit can be set up to generate PEFs with a pulse width in the nanosecond regime of positive polarity with respect to the circuit's ground plane. However, a negative pulse can also be obtained by slight modification to the circuit [3]-[4], [6], [9]-[10].

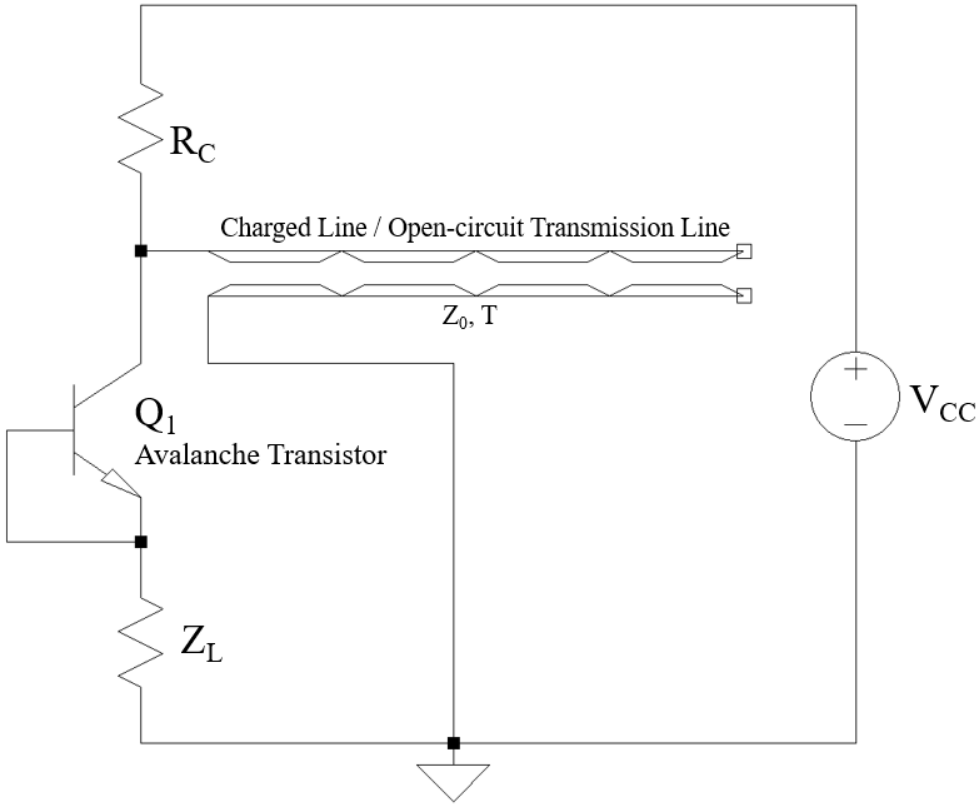


Fig. 5.7. A charged-line pulse generator with a single avalanche transistor as the switching element

5.4.1. Circuit Operation

The circuit shown in Fig. 5.7 utilizes a single avalanche transistor (Q_1) as a fast-switching element in conjunction with an open-circuit transmission line that operates as a delay line. Initially, all supplies to the circuits are 'OFF', (0 V at the voltage power supply (V_{CC})) and the operating point of the transistor and the circuit is at Point A in Fig. 5.8.

When the voltage supply (V_{CC}) is switched 'ON', the high Q storage element (the open circuit transmission line) is charged to V_{CC}, through a high impedance resistor (R_C). When a critical voltage is reached (Point B in Fig. 5.8), where the final bias voltage equals the collector-emitter breakdown voltage of the transistor ($V_{CC} \approx BV_{CES}$), the transistor exhibits a negative resistance which causes the transistor to experience avalanching (electron-hole regeneration). During this period the current through R_C can be neglected and the operating point moves to Point C as shown in Fig. 5.8.

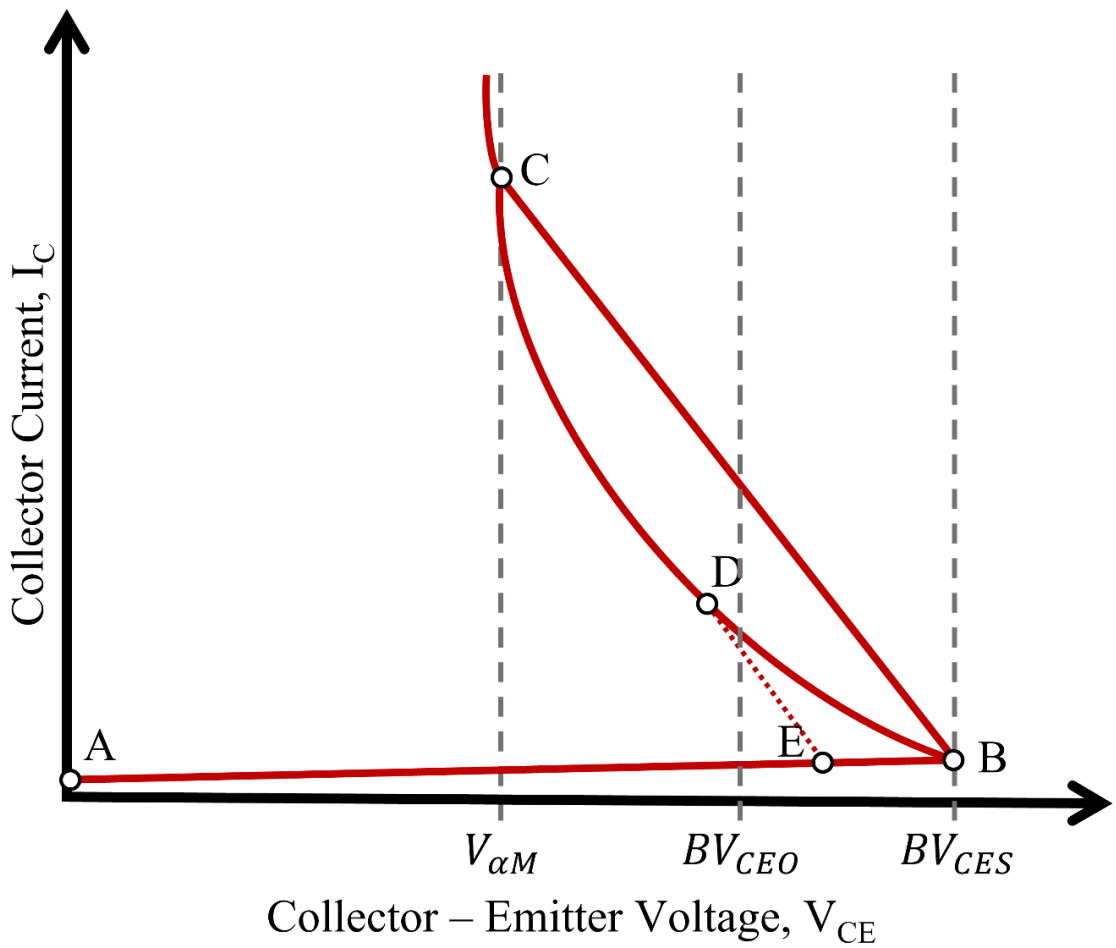


Fig. 5.8. Static characteristic of an avalanche transistor in a delay-line pulse generator [10].

The switching transient from Point B to C in Fig. 5.8 resembles the switching operation of a switching element closing in a charged line technique topology, as seen in Fig. 5.1. During this switching a fall time is observed within the transmission line, from the maximum voltage level ($V_{CC} \approx BV_{CES}$) to half the maximum voltage level $\left(\frac{V_{CC}}{2} \approx \frac{BV_{CES}}{2}\right)$, and a positive rise time is observed across the load as seen in Fig. I.4 and Fig. 5.1.

When this transient reaches the open-circuit end of the line, in time T (the accosted delay time of the transmission line), it is reflected down the line towards the collector of the transistor, giving a total associated delay time of 2T, and a pulse is generated across the load (Z_L) with a width/duration of 2T. This results in the discharge of the charged transmission line, from half the maximum voltage level $\left(\frac{V_{CC}}{2} \approx \frac{BV_{CES}}{2}\right)$ to 0 V after a time of 2T. Following the discharge of the line the operation of the circuit moves from Point C to Point D in Fig. 5.8 [3]-[4], [6], [9]-[10]. This description is illustrated in Fig. I.4 and Fig. 5.1. The amplitude and shape of the pulse depend on the relationship between the load (Z_L) and the characteristic impedance of the transmission line (Z_0).

Point D is an unstable point that causes regeneration and moves the operating point to E. Reflections may occur along the transmission line due to discontinuities along the line and at the load.

The reflection is minimized if the value of Z_L equals Z_0. This operation cycle of the circuit is continuously repeated from Point E→B→C→D→E until the supply voltage V_{CC} is at a level below the transistor collector-emitter breakdown voltage, BV_{CES} [3]-[4], [6], [9]-[10].

5.4.2. Circuit Analysis

The high impedance resistor used to charge the line (R_C) has a value that is significantly larger than the load resistor (Z_L) and the characteristic impedance of the charged line (Z_0). The time it takes for the line to charge to the voltage level V_{CC} depends on the value of R_C and the total capacitance of the delay line (C_d). The higher the value of R_C and/or the C_d the longer the charging time and the lower the possible repetition frequency capability of the circuit. The time constant of the circuit, $5\tau = R_C C_d$ as the line is charged to 99% of V_{CC}. This was previously illustrated by equation (5.5). The repetition frequency is related to the time it takes for the charged transmission line to discharge and then recharge through, R_C, from points E→B→C→D→E, as shown in Fig. 5.8.

The delay time associated with a transmission line is determined by the relative permittivity of the dielectric material (ε_r) of the coaxial line and the length of the line. This was previously illustrated in equation (5.4).

The maximum output voltage is limited by the breakdown voltage of the avalanche transistor, $BV_{CES} - V_{\alpha M}$. Where BV_{CES} is the collector-emitter breakdown voltage of the transistor and $V_{\alpha M}$ is the collector-emitter breakdown voltage when $\alpha M = 1$. The voltage $V_{\alpha M}$ in comparison to BV_{CES} is small and can be neglected. Therefore, the amplitude of the nsPEF across a load (Z_L) can be estimated as:

$$V_L = \frac{Z_L}{Z_L + Z_0} BV_{CES} \approx \frac{Z_L}{Z_L + Z_0} V_{CC} \tag{5.10}$$

Comparing equations (5.6) to (5.10), the collector-emitter breakdown voltage of the transistor, BV_{CES} replaces V_{CC}, in (5.6). The reasoning for this is if the voltage level within the charged line (V_{CC}) over exceeds the collector-emitter breakdown voltage (BV_{CES}) of the transistor will experience a destructive breakdown. If this voltage level is below the collector-emitter breakdown voltage of the transistor, then the circuit will not produce a pulse. For the circuit to operate the voltage across the delay line (V_{CC}) must match the collector-emitter breakdown voltage, (BV_{CES}) of the transistor as illustrated by Fig. 5.8.

This indicates the avalanche transistor switching operation is sensitive to the voltage across the transmission line and that its operation is a balancing act between the destructive and nondistinctive avalanching of the transistor for the generation of nsPEF.

The relationship between the transmission line and load impedance can be modelled as a simple potential divider and so the voltage across the line is given by equation (5.11). The peak current (I_P) across the load during the discharging of the transmission line can be determined by (5.12)

$$V_{Line} = \frac{Z_0}{Z_L + Z_0} BV_{CES} \approx \frac{Z_0}{Z_L + Z_0} V_{CC} \tag{5.11}$$

$$I_P = \frac{BV_{CES}}{Z_L + Z_0} \approx \frac{V_{CC}}{Z_L + Z_0} \tag{5.12}$$

Where I_P is the peak current, BV_{CES} is the collector-emitter breakdown voltage of a transistor, V_{CC} is the voltage level the line is charged to, Z_L is the load resistor and Z_0 is the characteristic impedance of the line.

The extent of the reflections following the incident pulse across the load can be explained using microwave transmission line analysis considering the concept of reflection coefficients.

Table 5.2 demonstrates how the relationship between the load impedance (Z_L) and transmission line characterise impedance (Z_0) influences the reflection coefficient and amplitude of the nsPEFs generated across a load and the discharge waveform seen on the charged transmission line.

Table 5.2. Influences of the load impedance and charged line characterise impedance has on the amplitude and reflection characterise of the generated nsPEF.

Z_L and Z_0 relation	**nsPEF Amplitude**	**Reflection Coefficient, Γ**
$Z_L >> Z_0$	$\sim BV_{CES} - V_{\alpha M}$	1, large, reflected pulse (staircase effect)
$Z_L = Z_0$	$\frac{BV_{CES} - V_{\alpha M}}{2}$	0, no reflection and a single nsPEF is generated.
$Z_L << Z_0$	~ 0	- 1, large, reflected pulses of alternating polarities

This circuit analysis concludes that the amplitude and shape, or associated reflections, of the nsPEFs across a load (Z_L) are influenced by the relationship between the load and the transmission line impedance (Z_0). A nsPEF, with zero reflection, is obtained when $Z_L = Z_0$, and its associated pulse amplitude would be $V_L = \frac{BV_{CES}}{2} \approx \frac{V_{CC}}{2}$.

As discussed, the selected avalanche transistor characteristics determine the generated rise time and the maximum pulse amplitude of the PEF that can be generated. A key component in determining the amplitude is the collector-emitter breakdown voltage (BV_{CES}) of the transistor.

5.4.3. Operation Cycle Control

Operating continuously from Point E→B→C→D→E, as shown in Fig. 5.8, will happen if the transmission line is charged to the transistor's collector-emitter breakdown voltage (BV_{CES}). This voltage level is a specific level that varies slightly from one transistor to the next.

The repetition frequency of the nsPEFs generated is associated with the time taken for the charged transmission line to reach its final voltage (V_{CC}) which is also the transistor's collector-emitter breakdown voltage (BV_{CES}), $V_{CC} \approx BV_{CES}$. If the final bias voltage exceeds the transistor's collector-emitter breakdown voltage the transistor can be damaged permanently, and no more pulses will be generated.

The current operation implies that there is very limited control over when, how many and the repetition frequency between each nsPEF generated by this circuit. The only method of control is by charging the transmission line to the specific 'biting point' voltage which is the transistor's collector-emitter breakdown voltage (BV_{CES}).

5.4.4. Component Selection

From the circuit analysis and operation cycle, it's clear that the selection of critical components used, such as the avalanche transistor and the transmission line dictate the operation of the circuit and therefore the parameters of the nsPEFs generated.

The transmission line is a crucial component to the successful operation of this topology to generate nsPEFs of 10 ns to 100 ns duration, with amplitudes in excess of 1 kV. In the embodiments discussed in this work, a coaxial cable is used as a transmission line. Three key parameters were required for a coaxial cable to perform as a charged transmission line for this application. These were: breakdown voltage of > 10 kV, attenuations of < 0.2 dB/m at the highest frequency within the pulse (1 GHz+) and a characteristic impedance of 50 Ω.

The characteristic impedance of the line is an important parameter considered in the development of the fast nsPEF electroporation system since it was required to apply the nsPEF across a cell-line population with an impedance of approximately 50 Ω. The circuit operation and analysis indicate that to generate a nsPEF with minimum reflection, the characteristic impedance of the transmission line should match the load impedance (5.7). Therefore, a coaxial line with a characteristic impedance of 50 Ω must be utilised. Additionally, (5.6) suggests that if this condition is met, the amplitude across the load will be half the collector-emitter breakdown voltage of the transistor. For the generation of nsPEFs with amplitudes in excess of 1 kV, the charged transmission line will therefore contain voltages in excess of 2 kV. Therefore, the higher the coaxial cable breakdown voltage the better.

A coaxial transmission line with acceptable attenuation at high frequency, in the GHz range is also required. This is because of the high-frequency components associated with the nsPEF. The frequency content within the pulse can be represented in the frequency domain as a sine function. The maximum frequency content within the nsPEF is related to the rise time of the nsPEF.

Rise time (t_r) is the time required for a pulse to rise from 10 per cent (0.1) to 90 per cent (0.9) of its steady value or amplitude. Rise time can be defined as

$$t_r = t_2 - t_1 \tag{5.13}$$

where t_1 is the time at which the output of the system under analysis is at 10 % ($0.1V_L$) of the steady-state value, and t_2 is the time at which the output is at 90 % ($0.9V_L$) of the steady-state value. This is illustrated in Fig. 5.1.

A rise time of 350 ps has been achieved from avalanche transistors. Which holds a frequency component/ bandwidth of 1 GHz.

In this topology, an avalanche transistor is used as a switching element, in conjunction with a charged transmission line, the components and circuit layout must consider frequency components of 1 GHz and above, which is in the microwave frequency region (300 MHz to 300 GHz). Therefore, microwave circuit design techniques need to be considered [5], [7], [22].

Transmission Line

In addition to the key requirement of the voltage and frequency capability of a transmission line, the dielectric constant and the capacitance per unit meter of the line are important parameters that determine the characteristics of the nsPEFs. The pulse width is determined by the transmission line dielectric constant and the length (5.4), and the total capacitance of the line determines the repetition frequency of the nsPEFs (5.5). The higher the dielectric constant of the material separates the two conductors that make up the transmission line, the short the physical transmission line length that is required [5], [7], [22].

There are several transmission line geometries including coaxial lines, planar lines, microstrip, strip line, coplanar lines and suspended strip lines [5], [7], [22]. For fast prototyping of the fast nsPEF electroporation system, a coaxial transmission line was implemented.

A wide range of coaxial transmission lines was investigated for implementation and a flexible RG214 coaxial double shielded with black PVC jacket cable was selected as the transmission line of choice with the following electrical specifications: nominal impedance of 50, capacitance of 101 pF/m, a maximum operating frequency range of 11 GHz, attenuation of 24.5 dB/100m (0.245 dB/m) at 1 GHz, 66 % velocity of propagation, and maximum operating voltage of 3.7 kV_{RMS}, and can withstand voltages of up to 10 kV_{RMS}.

Considering the RG214 coaxial cable electrical characteristics and the equations (5.4) and (5.5), the length of the RG214 cable required to generate the required width of nsPEF and the maximum repetition frequency (Hz) can be determined. Table 5.3 illustrates the estimated figures for an RG214 coaxial cable.

Table 5.3. Estimated nsPEF parameters calculated from the RG214 cable specifications

Required Pulse Width, 2T (ns)	***Line Length, l (m)***	***Impedance, Z_0 (Ω)***	***Total Capacitance, C_{line} (pF)***	***Max Repetition, frequency $5R_CC_D$***	***Max Repetition frequency, f (Hz)***	***Dielectric Constant ε_r***
10	1	50	100.98	504.90 µs	1980.59	2.25
50	5	50	504.90	2.52 ms	396.12	2.25
100	10	50	1,009.80	5.05 ms	198.06	2.25
…	…	…	…	…	…	…
170	17	50	1,716.66	8.58 ms	116.50	2.25
…	…	…	…	…	…	…
200	19.98	50	2,019.60	10.10 ms	99.03	2.25
300	29.98	50	3,029.40	15.15 ms	66.02	2.25

To verify the estimated nsPEF that will be produced with an RG214 cable, a vector network analyser (VNA) was used. The VNA is capable of using inverse Fourier transforms to convert swept frequency measurements for the device under test (the RG214 coaxial cable) into the time domain.

Fig. 5.9. shows the experimental set-up that includes a VNA to measure the associated delay time within a coaxial cable. The time difference between the two peaks shown in the time domain display of the VNA, shown in Fig. 5.10, indicates the duration of the nsPEF that would be generated, which is twice the associated time delay of the length of the RG214 cable. The distance between these peaks is the associated delay for a signal to travel from the distal end of the calibrated test and measure (CTM) cable connector to the VNA's S_{11} port (the calibration plane) to the distal end of the open-ended coaxial line and back to the distal end of the CTM cable. This indicates the pulse duration of the nsPEF generated with the associated coaxial cable.

The first peak, indicated by Δ1 in Fig. 5.10, indicates the connection between the S11 measurement port of the test and measurement cable and the coaxial cable. This indicates one end of the coaxial cable that is connected to the distal end of the calibrated CTM cable. The second peak seen, indicated as Δ2 in Fig. 5.10, is the reflected signal the VNA records at is after the signal has travelled along the coaxial cable and reflected back at the open distal end (impedance = ∞). Subtracting the largest time stamp from the smallest (Δ2 – Δ1 in Fig. 5.10) gives twice the associated delay (2T) of the line under test. 2T indicates the pulse width of the nsPEF that would be generated by implementing a charged line in conjunction with an avalanche transistor as the switching element.

Fig. 5.10(a) shows that a PEF of approximately 13.6 ns in duration (Δ2 – Δ1 = 13.768 ns – 200 ps = 13.568 ns) would be generated with a 1 m length of an RG214 cable. Fig. 5.10(b) shows that a PEF of 203.12 ns in duration would be generated with a 20 m length of RG214 cable. From these results, the associated pulse width using RG214 cable can be estimated as 10 ns per meter length of cable.

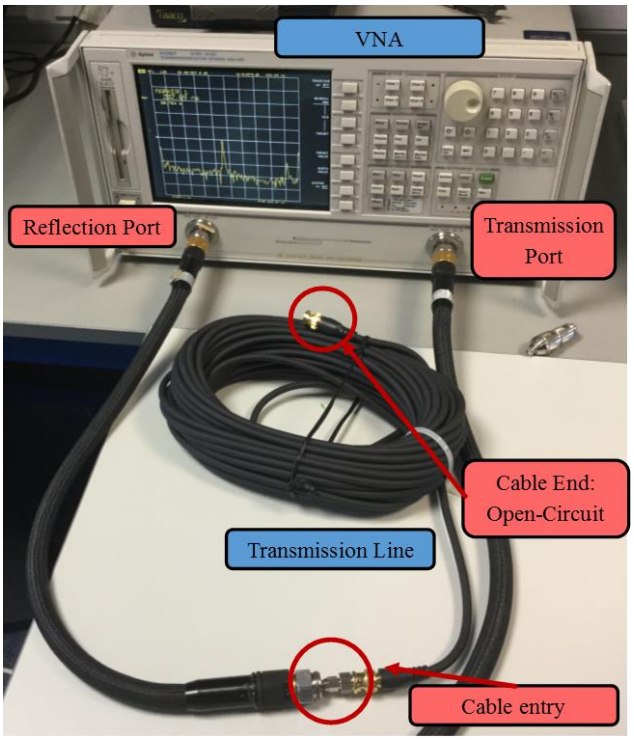
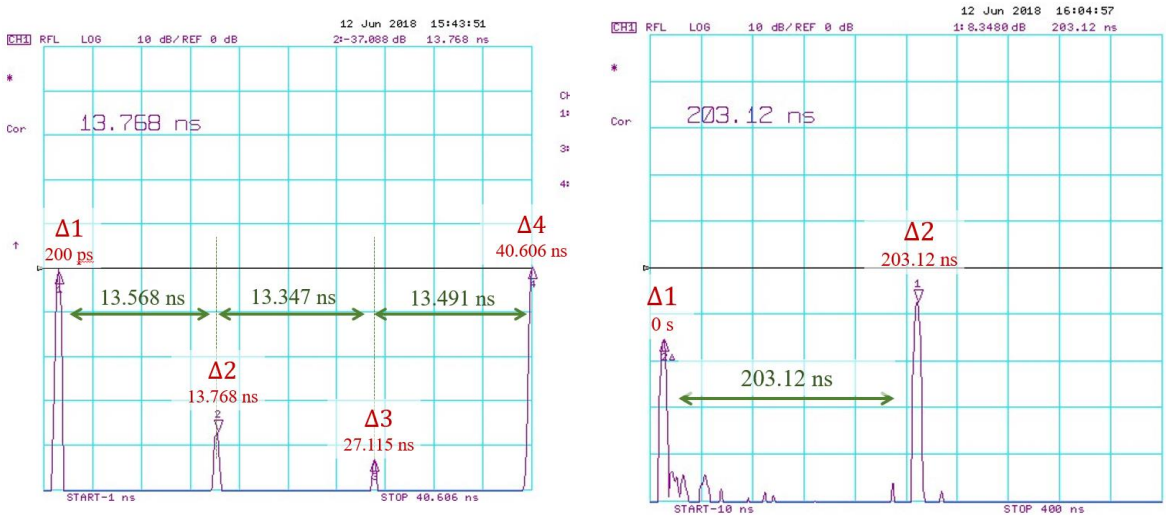


Fig. 5.9. Vector network analyser set-up to measure the associated delay time and pulse width of a coaxial cable.



(a) (b)

Fig. 5.10. Vector network analyser measurement of the electrical length, or twice the associated delay time (2T) of a RG214 coaxial cable of (a) 1 m and (b) 20 m in length.

Avalanche Transistor as a Fast Switch

Selecting a suitable avalanche transistor is crucial for the successful implementation of a nsPEFs generator that can produce an amplitude in excess of 1 kV and pulse duration in the order of 10 ns to 100 ns. For this to be achieved an avalanche transistor with sub-nanosecond rise times and collector-emitter breakdown voltage in excess of 1 kV is required.

Table 5.1. catalogues transistors that are purposely manufactured to operate in their avalanche mode of operation. The three transistors considered to be the most appropriate candidates were: 2N2369, FMMT415 and the FMMT417 devices. These three-avalanche transistors were investigated

with the following lengths of RG214 coaxial cable: 1 m, 5 m, and 17 m that produced associated pulse durations (2T) of 10 ns, 50 ns and 170 ns respectively.

Fig. 5.7 illustrates the test circuit used to test the performance of the three avalanche transistors and determine the breakdown voltage for the devices to avalanche. Thus, verifying the topology of combining an open circuit coaxial transmission line technique, as a charge line, with an avalanche transistor as a fast-switching element to produce nsPEFs in the range of 10 ns to 100 ns and above, with transition times less than a nanosecond across a 50 Ω load.

The value of the resistor used to charge the line (R_C) was 1 MΩ [34] and the voltage supply used was a Fluke 410B dc power supply [35]. The power supply (V_{CC}) was increased to slowly charge the open circuit coaxial transmission line through R_C until the transistor's avalanche breakdown voltage (BV_{CES}) was achieved.

Fig. 5.11. illustrates the nsPEF generated across a 50 Ω load by implementing the three aforementioned avalanche transistors (FMMT417, FMM415 and 2N2369) with a length of RG214 coaxial transmission of 17 m, where the distal end was an open circuit. This figure shows that the three transistors have a collector-emitter breakdown voltage, BV_{CES}, greater than specified in their respective datasheet (Table 5.1).

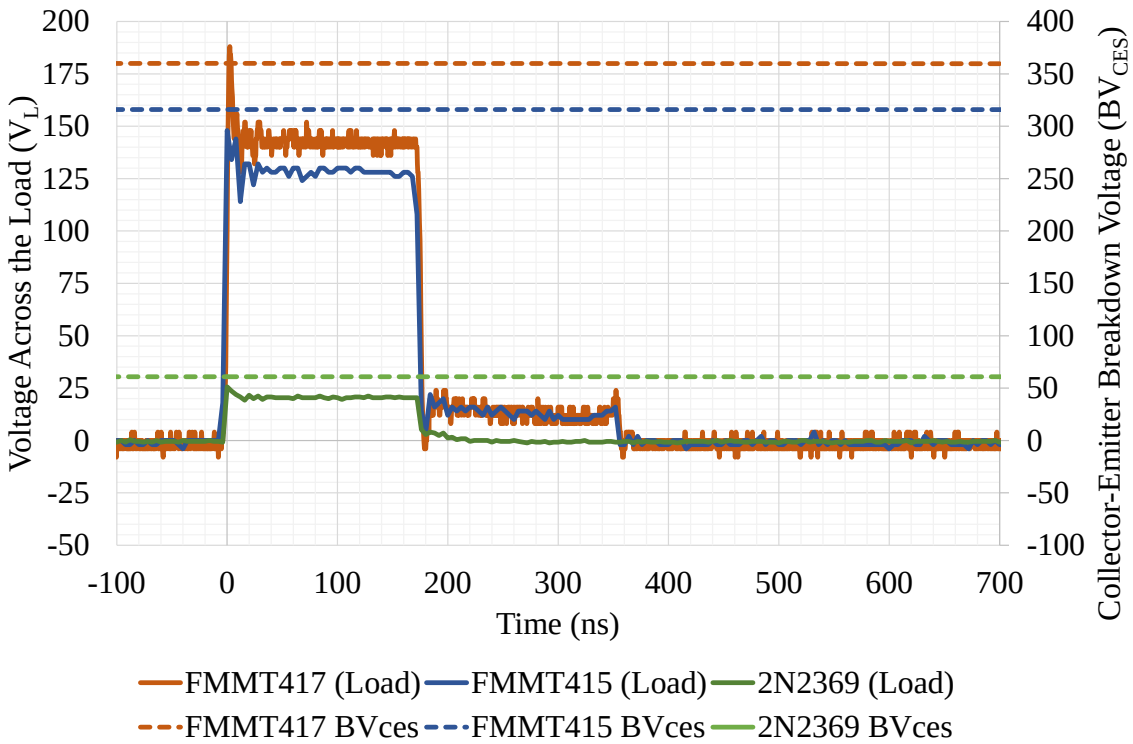


Fig. 5.11. Measured pulsed across a 50 Ω load by implementing a transmission line length of 17 m in conjunction with a FMMT417, FMMT415 and 2N2369 avalanche transistor (left-hand y-axis) and the charged line voltage to cause collector-emitter breakdown of the transistors (dotted line, right-hand y-axis)

Fig. 5.11. indicate that the FMMT417 avalanche transistor has the highest collector-emitter breakdown voltage (BV_{CES}) of around 360 V. As the FMMT417 has the highest collector-emitter breakdown voltage and produced a nsPEF with the highest amplitude of ~ 140 V. This figure also suggests that the FMMT417 has a faster transition time (rise and fall times) in comparison to the FMMT415 and 2N2369 avalanche transistors. It is also demonstrated that a 17 m length of charged line produced a 170 ns pulse width which aligns with the theory presented.

The measured pulses shown in Fig. 5.11 indicate minimum pulse reflection. A small neglectable reflection following the incident pulse can be observed, but this would not affect the result. The amplitude of the nsPEFs was approximately half the voltage level required to avalanche the transistors.

In conclusion, the FMMT417 avalanche transistor is the best-suited avalanche transistor to operate as the fast-switching element with a charged line for the application of generating nsPEFs. This is because of their high collector-emitter breakdown voltage in comparison to the other avalanche transistors investigated in this work. Additionally, their SOT-23 surface mount package enables very low inductance, which reduces pulse ringing and oscillation designed circuit [9].

Microstrip Lines

Due to the high-frequency component associated with the fast pulses microwave circuit design techniques were used in the layout of the generator. A microstrip line was used to develop the circuits associated with the fast pulse generator. A microstrip circuit design enables components in the high-frequency path, such as the FMMT417 transistors, and connectors, to be connected without reflections using 50 Ω microstrip lines fabricated along a microwave substrate [5], [7], [22].

This ensures a 50 Ω impedance is maintained from the charged coaxial transmission line through the analogue circuit of an avalanche transistor, or stack of avalanche transistors, to the 50 Ω load. This design technique is seen in high-speed digital circuits such as fast emitter-coupled logic (ECL) or ECL in picoseconds (ECL-ps).

Microstrip lines are fabricated where a conductor is separated from a ground plane by a dielectric layer, known as the substrate, as shown in Fig. 5.12. In microstrip lines, the width of the line (W), the distance of separation between the line and the ground plane (H), the dielectric constant of the substrate material (ε_r) and to a lesser degree the thickness of the line determine the characteristic impedance (Z_0) of this transmission line. Therefore, the impedance of the microstrip circuit can be determined by adjusting the width of the strip line and the height of the dielectric substrate (H).

For a microstrip line, the electromagnetic field exists and propagates both through the substrate material and, to a lesser degree the surrounding air, as seen in Fig. 5.13. This gives rise to a principle known as an effective dielectric constant. This slightly alters the required geometry for a given

microstrip line as would be calculated using the dielectric constant given in the datasheet for the material [5], [7], [22].

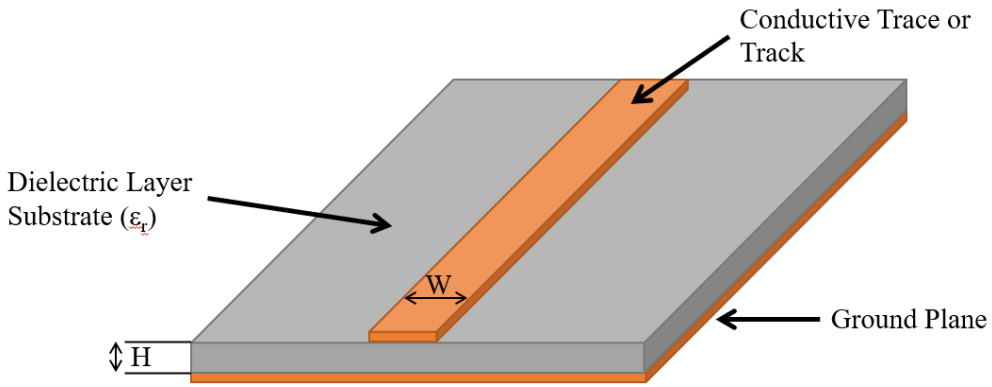
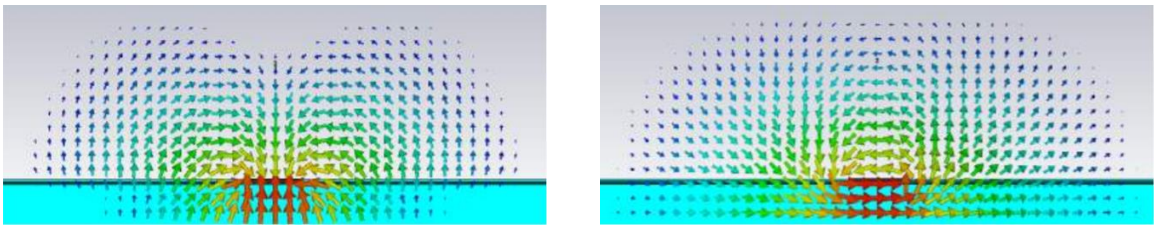


Fig. 5.12. A microstrip line printed circuit board structure [7]



(a) (b)

Fig. 5.13. Simulation of a microstrip structure showing its (a) Electric-Field and (b) Magnetic-Field lines [7]

The microstrip line circuits for this work were designed and built on an FR-4 (standard printed circuit board (PCB)) substrate. The dielectric constant (ε_r) for FR4 ranges from 3.8 to 4.8. Calculation of the effective dielectric constant (ε_{eff}) and characteristic impedance (Z_0) of the microstrip lines have been considered in many publications and are discussed in detail in [23], where a homogeneous medium which represents air, and the substrate regions are calculated. The effective dielectric constant is usually somewhere between the dielectric constant of air and that of the substrate material. These calculations slightly vary depending on the ratio of the line width (W) and the substrate thickness (H) as shown in equations (5.14) to (5.17).

$$if\ \left(\frac{W}{H}\right) < 1;$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12\left(\frac{H}{W}\right)}} + 0.04\left(1 - \frac{W}{H}\right)^2\right] \tag{5.14}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}}\ \ln\left(8\left(\frac{H}{W}\right) + 0.25\left(\frac{W}{H}\right)\right) \tag{5.15}$$

$$If\ \left(\frac{W}{H}\right) > 1;$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \left[\frac{\varepsilon_r - 1}{2\sqrt{1 + 12\left(\frac{H}{W}\right)}}\right] \tag{5.16}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W}{H} + 1.393 + 2/3\ln\left(\frac{w}{H} + 1.444\right)\right]} \tag{5.17}$$

Considering equations (5.14) and (5.17) W is the width of the microstrip line, H is the separation distance between the line and the ground plane, ε_{eff} is the effective dielectric constant of the structure, ε_r is the dielectric constant of the substrate material, and Z_0 is the impedance of the structure.

Fig. 5.14 presents a plot of the effective dielectric constant (ε_{reff}) and characteristics impedance (Z_0) against line width (W) for a substrate thickness (H) of 1.50 mm and a dielectric constant (ε_r) using equations (5.14) to (5.17). It can be seen that the ratio H/W changes the effective dielectric constant, εeff, and the impedance of the microstrip structure, Z_0. The microstrip line for the boards developed in this work uses an FR4 substrate that has a dielectric constant of 4.7, and the separation between the line and the ground plane is 1.5 mm [24]. The graph given in Fig. 5.14 indicates that a microstrip line width of 2.75 mm would produce a microstrip line of 50 Ω characteristic impedance.

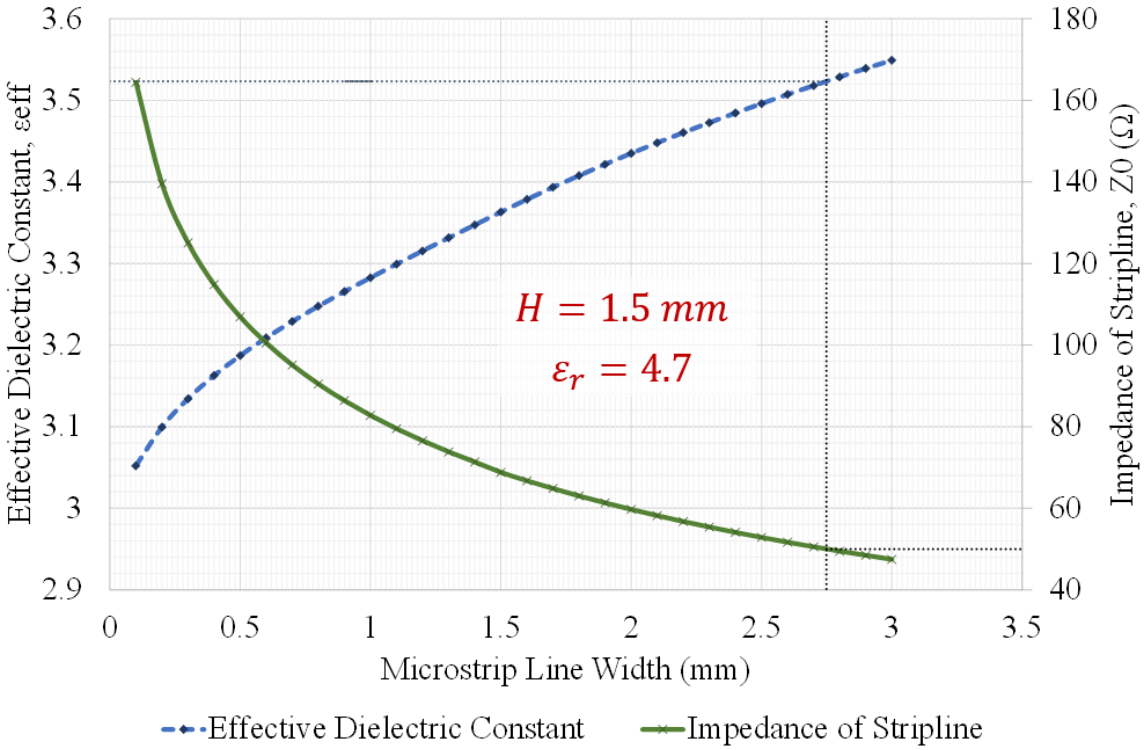


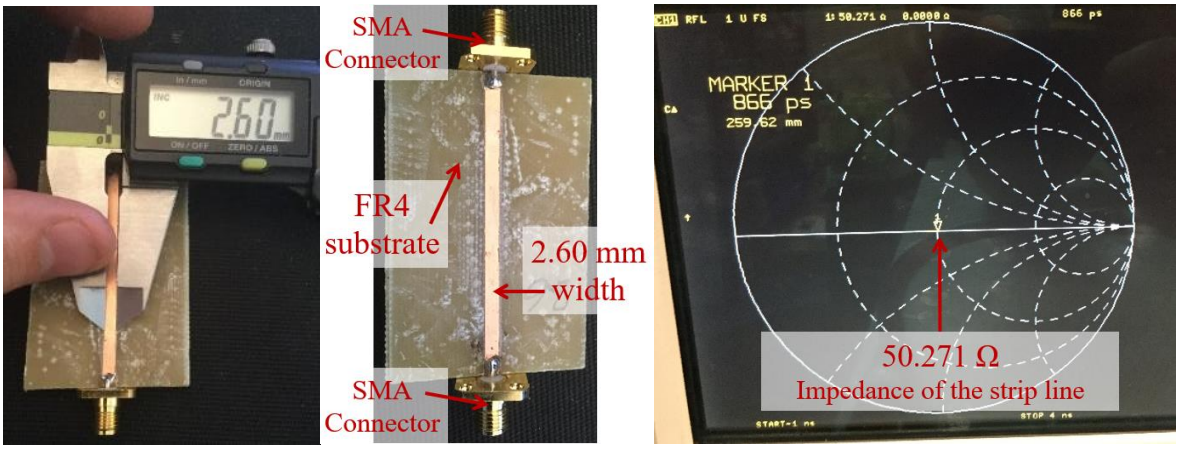
Fig. 5.14. Characteristic impedance and effective dielectric constant variation with line width for structure where H = 1.50 mm and ε_r =4.7.

Equations (5.14) to (5.17) and Fig. 5.15 show theoretically and practically that a microstrip line width of 2.60 mm on a substrate with a dielectric constant of 4.7 and separation between the line and the ground plane of 1.5 mm will produce a microstrip line of 51.56 Ω. This was verified by fabricating the line and testing using a VNA.

The performance of the circuit can be hindered by inadequate PCB layout. The underside of the board was a full ground plane and the SMA connectors were carefully soldered to the board with a gap of ≤ 0.25 mm gap between the tab of the SMA connector and the start of the microstrip line (this prevents breakdown). The use of surface-mount packaged components, such as the FMMT417 SOT-23

package, minimises stray inductance. This enables low inductance designs with minimum reflection and minimum risk of oscillation to be implemented [9].

Therefore, the circuit design for generating fast nanosecond pulsed electric fields using an open-circuit coaxial transmission line in conjunction with an avalanche transistor, or stack of transistors, was populated on a microstrip line-based PCB. A microstrip line of 2.75 mm width was implemented to ensure 50 Ω impedance is maintained from the charged coaxial transmission line through the analogue circuit, to the 50 Ω load.



(a) (b)

Fig. 5.15. (a) Fabricated microstrip line on a FR4 substrate material (b) corresponding vector network analyser Smith Chart result

5.5. Simulation

LTSpice simulation package was used to verify the slow charging and rapid discharging of an open circuit coaxial transmission line through a stack of avalanche transistors operating as a fast-switching element for the generation of the nsPEF. LTSpice simulation package can mathematically predict the behaviour of the circuit if an appropriate spice model for the transistor (or other critical components) is available [25].

5.5.1. FMMT417 Avalanche Transistor

A third-party spice netlist file that contains the subcircuit definitions for the FMMT417 avalanche transistors was found [26]. It is possible in LTSpice IV to implement a component from a third-party spice netlist file [27]-[28]. This netlist was used in the LTSpice simulations as the FMMT417 avalanche transistor used in the simulation schematic for the generation of high voltage nsPEFs.

LTSpice is a SPICE-based analogy electronic circuit simulator known to simulate components in their linear operation, while avalanche transistors operate in a non-linear fashion in practice. To fully understand and appreciate the complexity of the netlist Spice model of the FMMT417 from Diodes Incorporated there is a need to simulate the netlist Spice model [25].

Through studying the netlist Spice model for the FMMT417, shown in Fig. 5.16(a), an equivalent circuit for this Spice model was created. The equivalent circuit for this device model is illustrated in Fig. 5.16(b). From studying the netlist file and its equivalent circuits, it can be determined that sub-components within the Spice model are modelled, or mathematically interpreted, to behave in a linear fashion. This is indicated in the netlist Spice file with the code lines starting with '.model'. These lines suggest that the FMMT417 operates with different characteristics under four different collector-emitter or breakdown voltage ('Bv') conditions. These are indicated below:

- '**.model DZ20** D Is=1E-15 **Bv=20** Ibv=100u'
- '**.model DZ200** D Is=1E-15 **Bv=200** Ibv=100u'
- '**.model DZ350** D Is=1E-15 Rs=0.1 **Bv=350** Ibv=100u'
- '**.model DZ500** D Is=1E-15 N=10 **Bv=500** Ibv=100u'

This netlist model for the FMMT417 gives a collector-emitter ON-resistance (R_{on}) of 3 Ω when the FMMT417 operates as a switch in simulation. This is indicated by the $R_{(on)}$ values of the switches, and R6 in the FMMT417 equivalent model. The $R_{(on)}$ for the FMMT417 can be neglected when operating in the avalanche breakdown mode.

- '.**model SMOD1** VSWITCH Roff=1e10 **Ron=0.1** Voff=4.3 Von=4.6'
- '.**model SMOD2** VSWITCH Roff=1e3 **Ron=1.0** Voff=4.5 Von=9'
- '.**model SMOD3** VSWITCH Roff=1e10 **Ron=0.1** Voff=20 Von=25'
- '**R_R6** 10 11 **2**'

From the net file list file for the FMMT417, it can be seen that the Spice model will operate as a fast-switching element with a transition time of 1.3 ns, as indicated by the spice statement: '**+TF =1.3E-9**'.

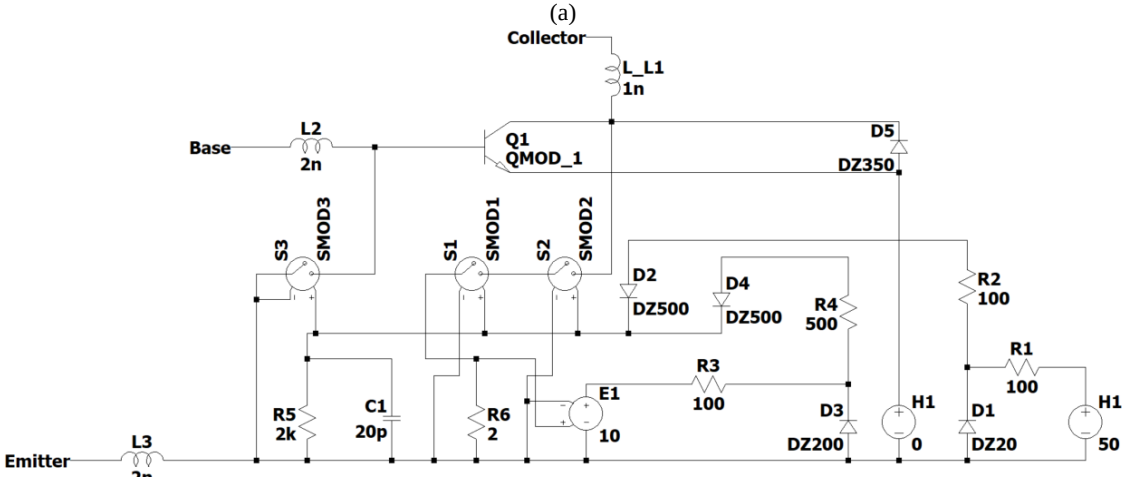
To verify these assumptions made from the FMMT417 netlist file, the Spice model was simulated to investigate the LTSpice operation and linear collector-emitter voltage (V_{CE}) vs collector current (I_C) characteristic. Fig. 5.17(a) illustrates the LTSpice simulation schematic used to gain the FMMT417 V_{CE} vs I_C curves that are shown in Fig. 5.17(b), and Fig. 5.17(c). Fig. 5.17(c) illustrates the complete FMMT417 collector-emitter voltage (V_{CE}) vs collector current (I_C) curves, which include its saturation, active, and its breakdown region. Fig. 5.17(b) highlights the breakdown characteristic region of the simulated FMMT417.

The FMMT417 LTSpice Spice V_{CE} vs I_C, characteristic curves shown here demonstrate that the FMMT417 spice model can be modelled mathematically in a piecewise linear fashion. In reality, the avalanche region of a transistor behaves in a non-linear manner. In this model, it shows that the collector-emitter breakdown voltage for the FMMT417 is 350 V. At V_{CE} = 350 V the collector current increases with a rapid change in current from a minimum change in voltage along the current y-axis

plane to a collector current value of ∞ A. In reality, if the voltage drop across the FMMT417 exceeds that of the FMMT417 collector-emitter breakdown voltage, the transistor will undergo destructive avalanche breakdown and permanently damage the transistor.

```
*ZETEX FMMT417 Spice Model v2.0 Last Revised 23/03/07
*
.SUBCKT FMMT417 16 15 14
*Pins_____________C__B__E
Q_Q1          9  8  7 QMOD_1
R_R1          5  6  100
R_R2          5  4  100
R_R3          12  3  100
R_R4          3  1  500
R_R5          10  2  2k
R_R6          10  11  2
D_D1          10  5 DZ20
D_D2          4  2 DZ500
D_D3          10  3 DZ200
D_D4          1  2 DZ500
D_D5          7  9 DZ350
C_C1          10  2  20p
S_S1         13  11  2  10  SMOD1
S_S2          9  13  2  10  SMOD2
S_S3          8  10  2  10  SMOD3
V_H1          7  10  0
H1 6 10  V_H1 50
E1 12 10 11 10 10
L_L1          9  16  1nH
L_L2          15  8  2nH
L_L3          10  14  2nH
.model QMOD_1 NPN IS =3E-14 NF =1 BF =110 IKF=0.4
+VAF=1900 ISE=1E-12 NE =1.6
+NR =1 BR =7 IKR=0.2 VAR=75 ISC=1e-10 NC =1.9
+RB =0.4 RE =0.1 RC =0.1
+CJC=10.9E-12 MJC=0.347 VJC=0.476 CJE=82.6E-12
+TF =1.3E-9 TR =2.3e-7
.model DZ20 D Is=1E-15  Bv=20 Ibv=100u
.model DZ200 D Is=1E-15  Bv=200 Ibv=100u
.model DZ350 D Is=1E-15 Rs=0.1 Bv=350 Ibv=100u
.model DZ500 D Is=1E-15 N=10 Bv=500 Ibv=100u
.model SMOD1 VSWITCH Roff=1e10 Ron=0.1 Voff=4.3 Von=4.6
.model SMOD2 VSWITCH Roff=1e3 Ron=1.0 Voff=4.5 Von=9
.model SMOD3 VSWITCH Roff=1e10 Ron=0.1 Voff=20 Von=25
.ENDS FMMT417
*
```

(a)



(b)

Fig. 5.16. (a) FMMT417 netlist file [26] (b) and its netlist equivalent circuit

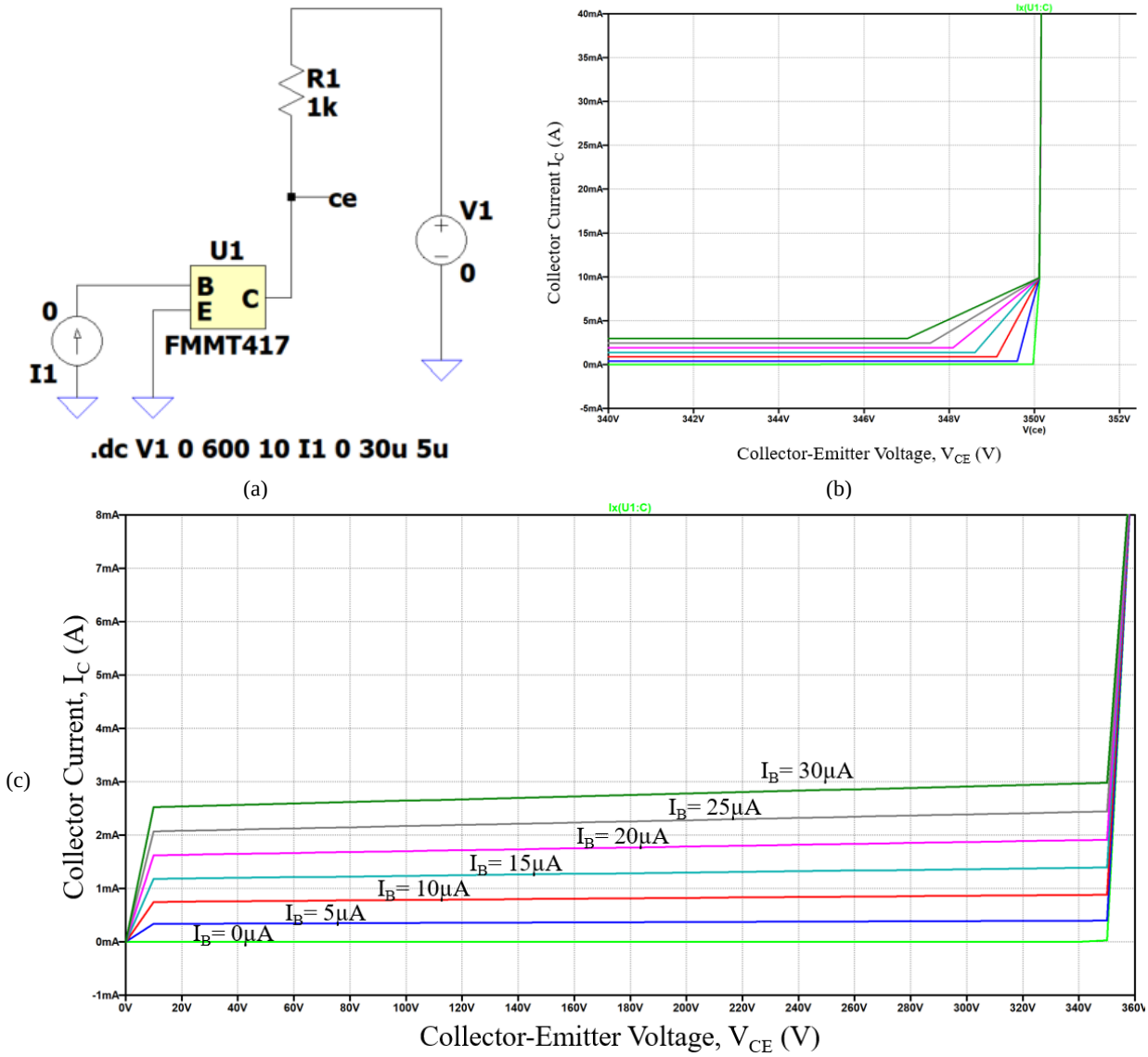


Fig. 5.17. FMMT417 LTSpice spice collector-emitter voltage vs collector current characteristic (a) schematic (b) avalanche breakdown region of the characteristic curve for the range of collector-emitter voltage from 340 V to 352 V (c) complete characteristic curve collector-emitter voltage from 0 V to 360 V

5.5.2. Final Simulated Designated Design

The final simulation topology includes the charged line and the FMMT417 transistor as a fast nanosecond switching element. Fig. 5.18 shows the LTSpice schematic for the operation of the relatively slow charging and rapid discharging of the open-circuited transmission line section with a single FMMT417 avalanche transistor operating as a fast-switching element for the generation of nsPEFs. The simulation used a model for a transmission line with a characteristic impedance of 50 Ω and an associated time delay (T) of 50 ns.

Fig. 5.19 shows the simulated voltage waveforms across the load (Z_L) (blue) and the voltage along the charged line (red) for the circuit given in Fig. 5.18. Fig. 5.19 illustrates the 100 ns PEF generated across a 50 Ω load, which is twice the 50 ns associated delay time (T) of the transmission line. These

simulations are for a single avalanche transistor switch. The amplitude of the nsPEF is approximately 170 V, which is approximately half the voltage of the fully charged line. This demonstrates that the FMMT417 avalanche transistor switch does not affect the pulse duration. The number of nsPEFs generated and their repetition frequency is determined by the trigger signal across the base-emitter of the FMMT417, which uses a 1:1 pulse transformer, as seen in Fig. 5.18. The 1:1 high-frequency pulse transformer is an important component in the fast nanosecond pulse circuit.

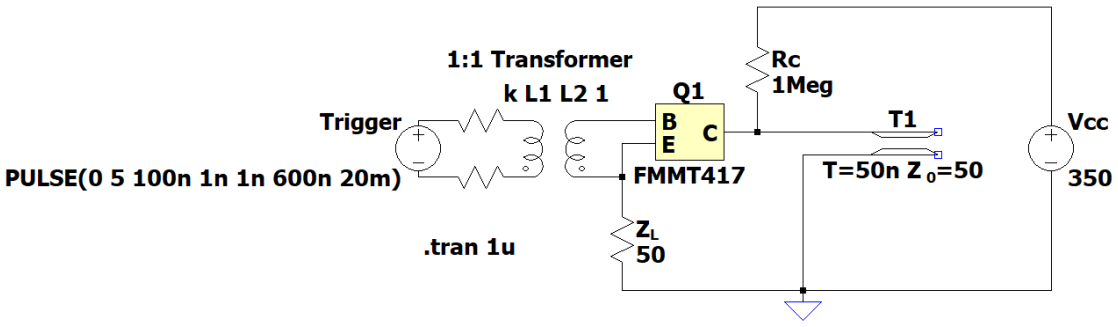


Fig. 5.18. LTSpice simulation schematic for the final topology with a single FMMT417 transistor

Following a closer look at Fig. 5.19(a), a small reflection following the incident pulse is observed when along the line. From the analysis of the spice model for the FMMT417, it was observed that the FMMT417 has an ON-resistance of 3 Ω. Therefore, from a reflection coefficient standpoint, there is a mismatch as the total impedance at the load side is 53 Ω (Z_L (50 Ω) + $R_{(on)}$ (3 Ω))) in comparison to the 50 Ω characteristic impedance of the transmission line. For a reflection coefficient of 0, the total impedance at the load would need to be 47 Ω. This is validated in Fig. 5.19(b) by the symmetrical nsPEF with no reflection along the line when load impedance Z_L is 47 Ω.

For a microwave circuit to have a zero reflection coefficient (Γ = 0) to prevent reflected voltages (and currents) at the boundary between two impedances, the total load impedance (Z_L) must be the same as the characteristic impedance of the transmission line (Z_0). In this circuit, Z_0 = 50 Ω and Z_L must take into account the ON-resistance of the avalanche transistors i.e., $Z_L = Z_L'$ where $Z_L'=Z_0 - R_{on}$. When a number of avalanche transistors (n) are stacked together to increase the overall breakdown voltage of the circuit (or the amplitude of the fast nsPEF), the total value of $R_{(on)}$ must be taken into account. Therefore, the load impedance for a circuit with zero reflection coefficient can be calculated by the below equation.

$$Z_L = Z_0 - nR_{(on)} \tag{5.18}$$

Where Z_L is the load impedance required for a circuit with a zero reflection coefficient (Γ = 0), Z_0 is the characteristic impedance of the transmission line, n is the number of avalanche transistors that are stacked in series, and $R_{(on)}$ is the ON-resistance of a single transistor used.

Because of the effects of the ON-resistance of the FMMT417 and the adjustment required to the load impedance for zero reflection, this affects the amplitude of the nsPEF. Therefore, the amplitude of the nsPEF is reduced due to the additional impedance of $nR_{(on)}$. This can be thought of as an additional

resistor in a potential divider network of three resistors. These resistors are the load impedance, (Z_L), the characteristic impedance of the charged line (Z_0) and the total ON-resistance of the stacked transistors, $nR_{(on)}$. Thus, the amplitude of the nsPEF in simulation can be calculated by (5.19).

$$V_L = \left(\frac{Z_L}{Z_L + nR_{on} + Z_0}\right)V_{CC} \quad = \left(\frac{Z_L}{Z_L + n3\Omega + Z_0}\right)V_{CC} \tag{5.19}$$

Where V_L is the amplitude of the nsPEF across the load, Z_L is the load impedance, Z_0 is the characteristic impedance of the transmission line, n is the number of avalanche transistors that are stacked in series, $R_{(on)}$ is the ON-resistance of a single transistor used, n is the number of avalanche transistors that are stacked in series, and V_{CC} is the voltage across the charged coaxial transmission line.

This demonstrated that in simulation the value of the load impedance needs to be reduced by a factor of 3 times the number of FMMT417 transistors that are stacked in simulated as the value of their $R_{(on)}$ is 3 Ω. In practice, this value may be smaller (see the datasheet Appendix IV [19]). The amplitude of the nsPEF is less than the theoretical value of $\frac{VCC}{2}$ the more FMMT417 transistors that are stacked. This observation is reflected in Table 5.4.

Because of the linear spice model of the FMMT417, its avalanche occurs at exactly 350 V, with an infinite collector current. Fig. 5.19(c) shows that the avalanche transistor does not experience a destructive breakdown in simulation, even when a 1,000 V is placed across its collector and emitter terminal.

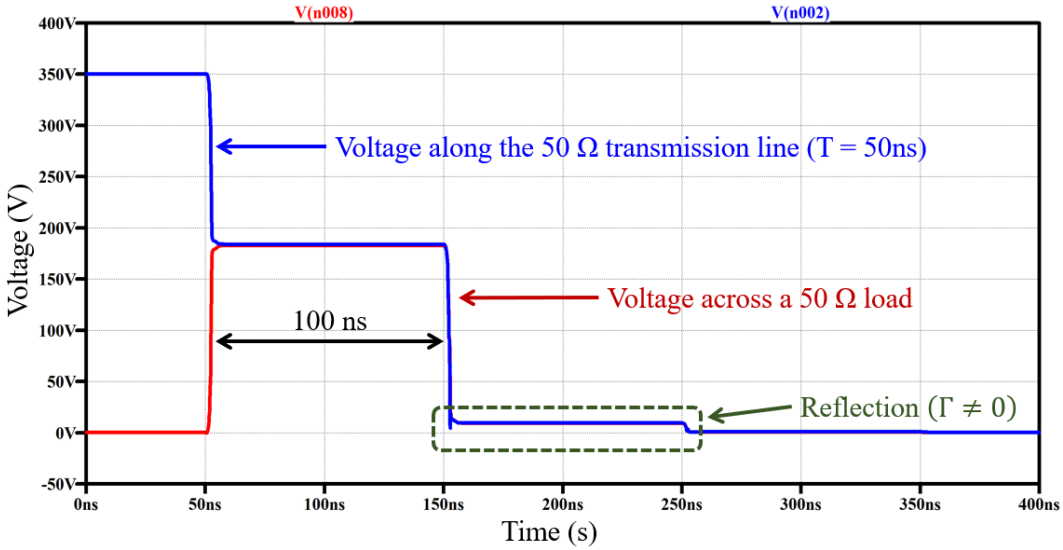
Table 5.4. nsPEF calculated amplitude due to $R_{(on)}$ of the FMMT4717 spice model

Number of stacked transistors, n	Voltage along the charged line, n350	Total impedance of the stacked transistors, $nR_{(on)}$ (Ω)	Impedance of the load for **Γ = 0** (Ω)	characteristic impedance of charged line, Z_0 (Ω)	nsPEF amplitude with $R_{(on)}$=3 Ω (V)	nsPEF amplitude if $R_{(on)}$ = 0 Ω (V)
1	350	3	47	50	164.5	175
2	700	6	44	50	308.0	350
3	1050	9	41	50	430.5	525
4	1400	12	38	50	532.0	700
5	1750	15	35	50	612.5	875

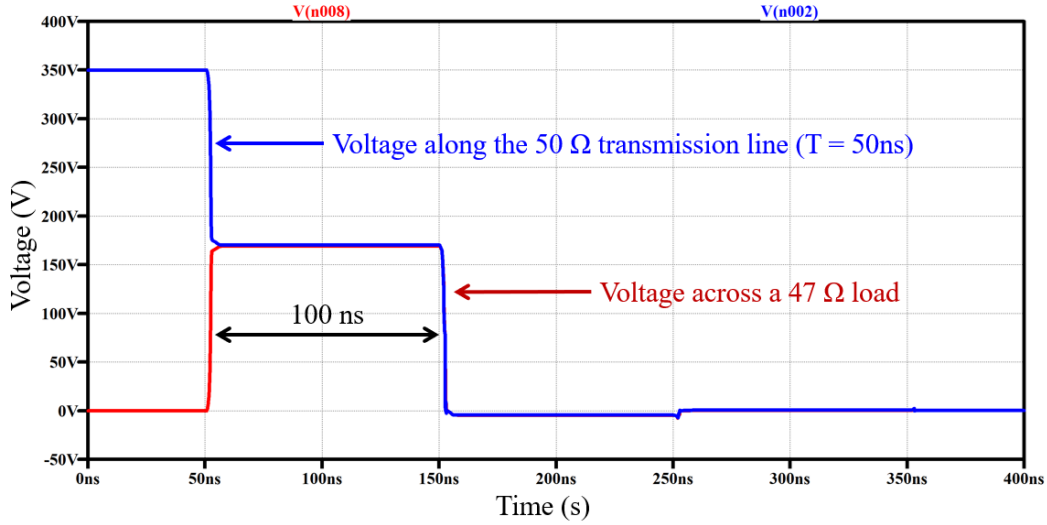
In reality, if the collector-emitter voltage exceeds the FMMT417 breakdown voltage, to an extreme such as 1,000 V, the transistor would experience a destructive breakdown. The LTSpice model for the FMMT417 limits the maximum voltage drop across the device to 350 V. Therefore, the transistor does not experience a destructive breakdown in simulation. Because of this piecewise linear model for the FMMT417, the Spice model is not realistic. However, the FMMT417 spice model provides a basic model for the transistor and enables the rest of the circuit to be modelled to provide a first order understanding of the operation of the overall circuit, which includes the relatively slow charging and

rapid discharging of a transmission line through a stack of avalanche transistors operating as a fast-switching element for the generation of nsPEF.

(a)



(b)



(c)

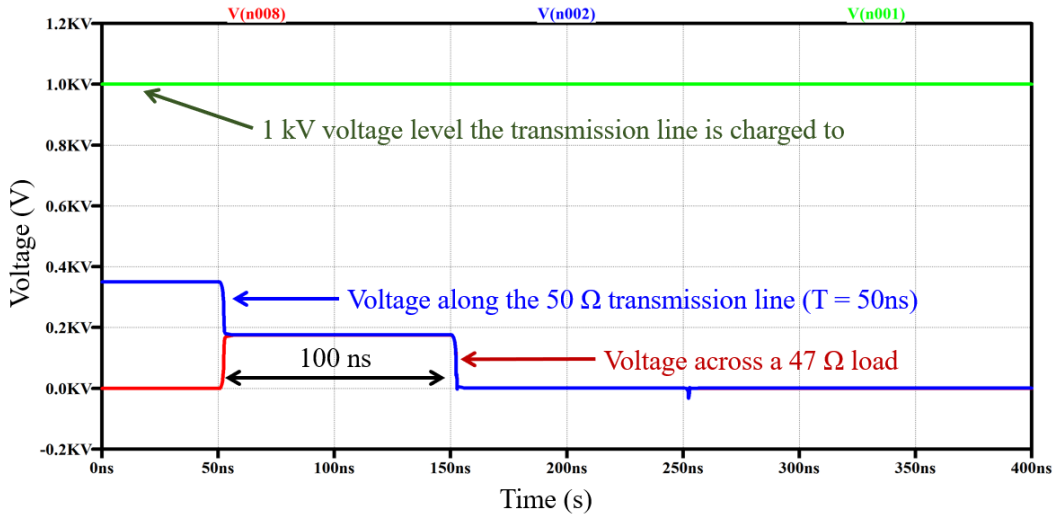
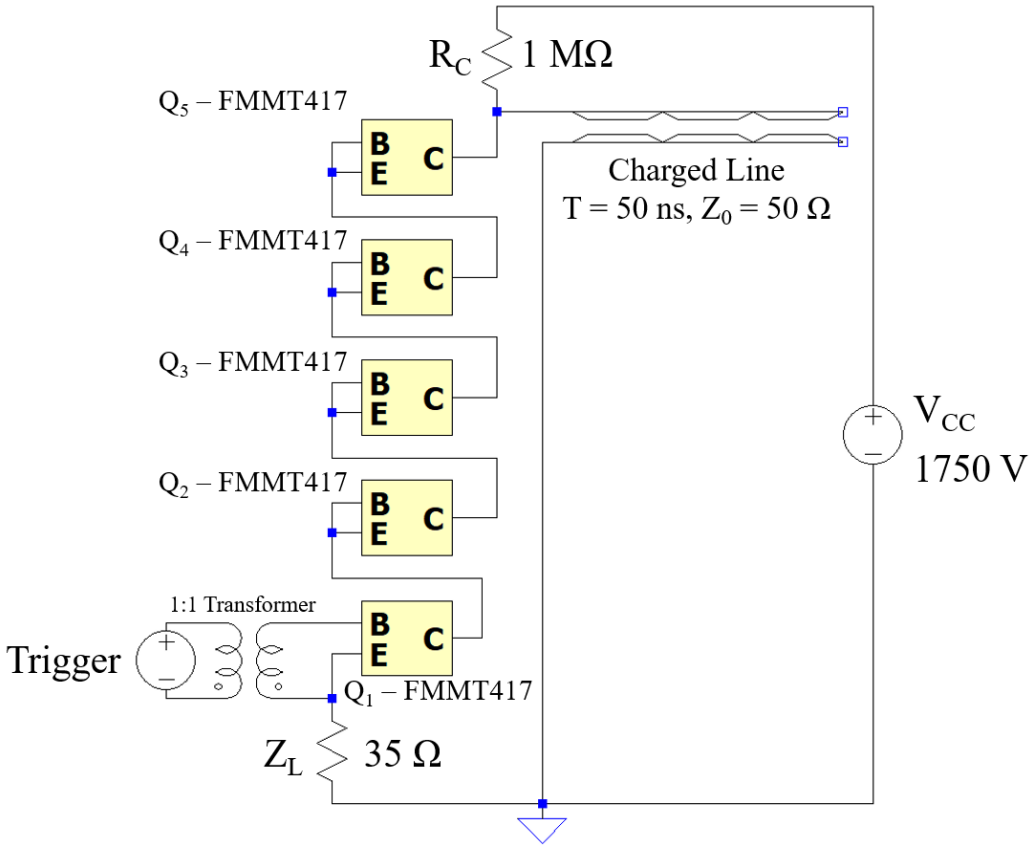


Fig. 5.19. Simulated voltage along the 50 Ω charged line (blue waveform) and across the load (red waveform) with a load impedance (Z_L) of (a) 50 Ω (b) 47 Ω and (c) 50 Ω load with additional measured voltage level along the charged line increased from 350 V to 1 kV (green waveform).

Fig. 5.20. illustrates the operation of stacking five FMMT417 avalanche transistors to form the fast-switching elements to increase the nsPEF amplitude across the load (Z_L). Because of the 3 Ω ON-resistance associated with the FMMT417 spice model a 35 Ω load impedance (50 Ω – (5 x 3 Ω)) provides a reflection coefficient of zero. The resultant waveforms observed in Fig. 60(b) supports equation (5.18) and in LTSpice simulation a 35 Ω load produces a system with no reflection.

(a)



(b)

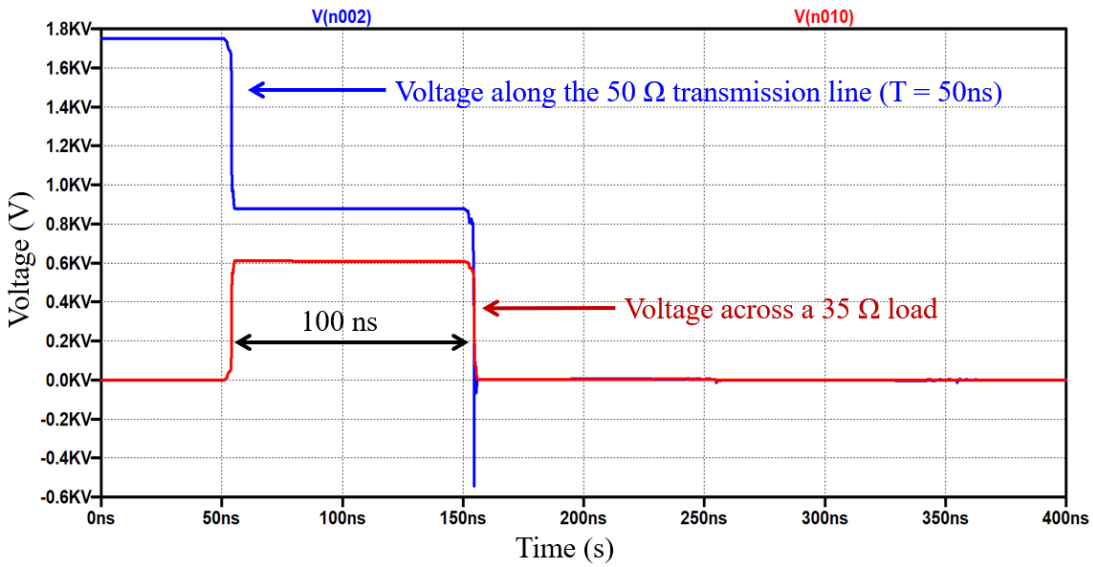


Fig. 5.20. (a). LTSpice simulation schematic the charged line technique with a stack of five FMMT417 transistors operating as a fast-switching element. (b) measure simulation voltage signal along the transmission line (blue waveform) and across the 35 Ω load (red waveform)

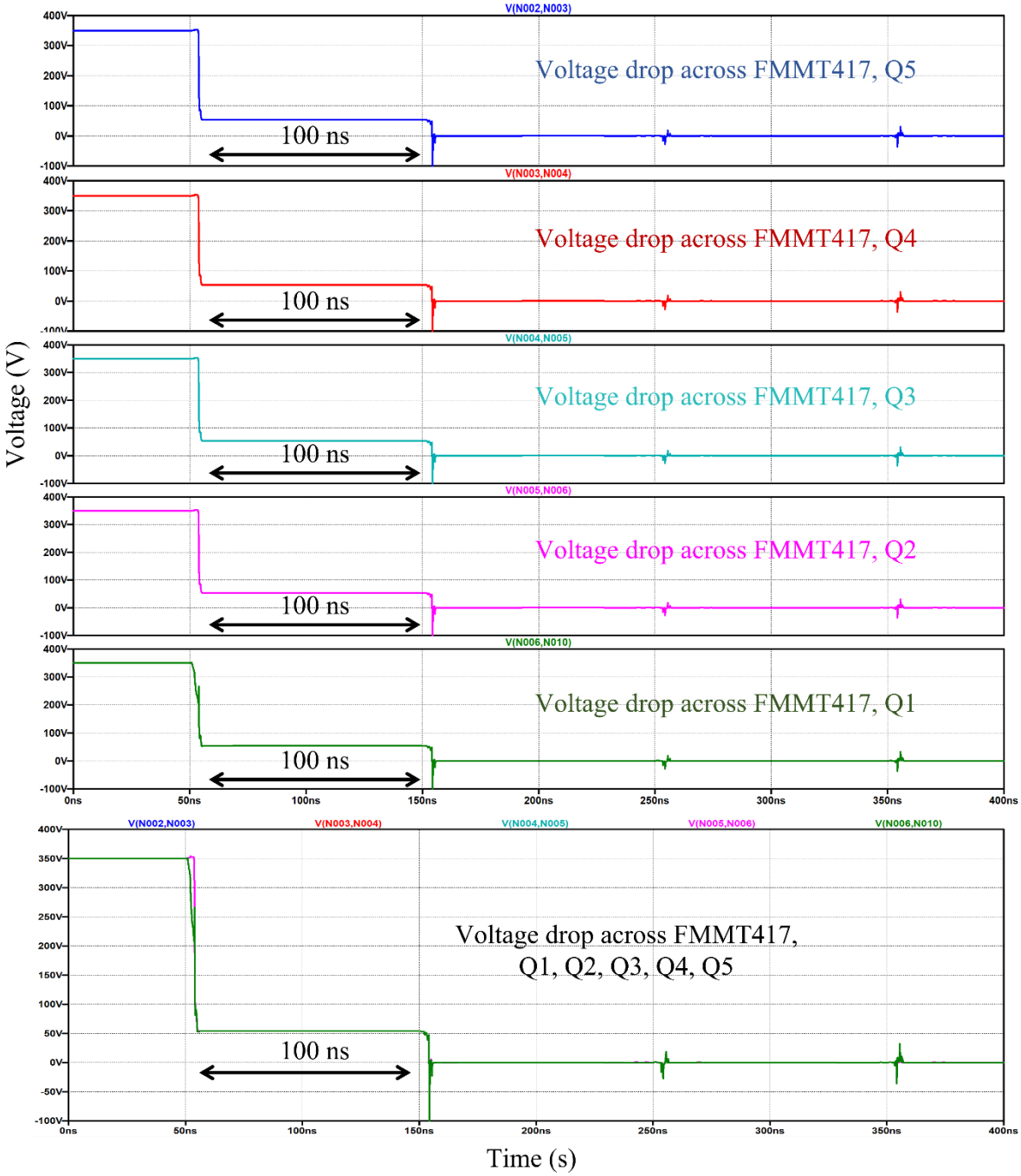


Fig. 5.21. Voltage drop across the lowest stack transistor (Q_1) (bottom – pink waveform) to the highest stacked transistor (Q_5) (top-green waveform) in a switching element consisting of five avalanche transistors.

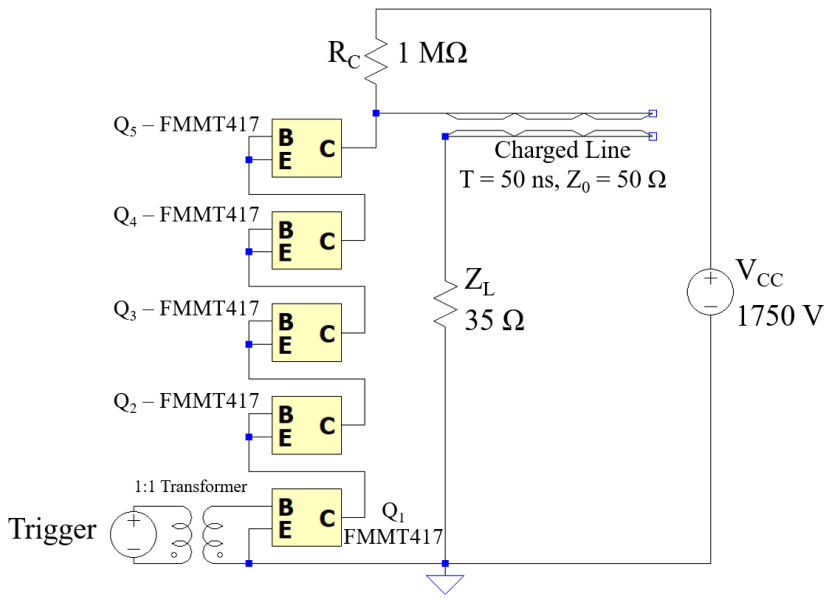
Comparing the amplitude of the nsPEF across the load (Z_L) from Fig. 5.19(b) and Fig. 5.20(b) demonstrates that by increasing the number of FMMT417, that are stacked as a switching element, the amplitude of nsPEF generated is increased as one would expect.

Fig. 5.21 illustrates that the voltage across the charged line is dropped evenly across each of the stacked FMMT417 transistors. The waveform and the amplitude of the voltage drop across each transistor collector and emitter terminals in the stack are identical. This is illustrated in Fig. 5.21. from the voltage drop across the bottom transistor in the stack (Q_1) to the voltage across the highest stacked

transistor in the stack (Q_5) in a switching element consisting of five avalanche transistors as shown in Fig. 5.20(a).Fig. 5.22(a) is an alternative schematic of Fig. 5.20(a), where the load within the schematic has been relocated. The 35 Ω load has been relocated from being placed between the lowest FMMT417 transistor, Q_1, in the stack, and the ground plane (as shown in Fig. 5.20(a)), to be between the outer conductor of the transmission line and ground plane of the system, as shown in Fig. 5.22(a).

The resultant nsPEF generated in Fig. 5.22(b) is identical to the nsPEF waveform seen in Fig. 5.20(b) with regards to the amplitude, duration and waveform. The only difference is the polarity of the pulse, where it can be seen that the polarity is negative. This demonstrates that by moving the location of the load from across the emitter of Q_1 and ground to across the proximal end (outer conductor) of the transmission line to ground the polarity of the nsPEF is changed from a positive to a negative polarity nsPEFs.

(a)



(b)

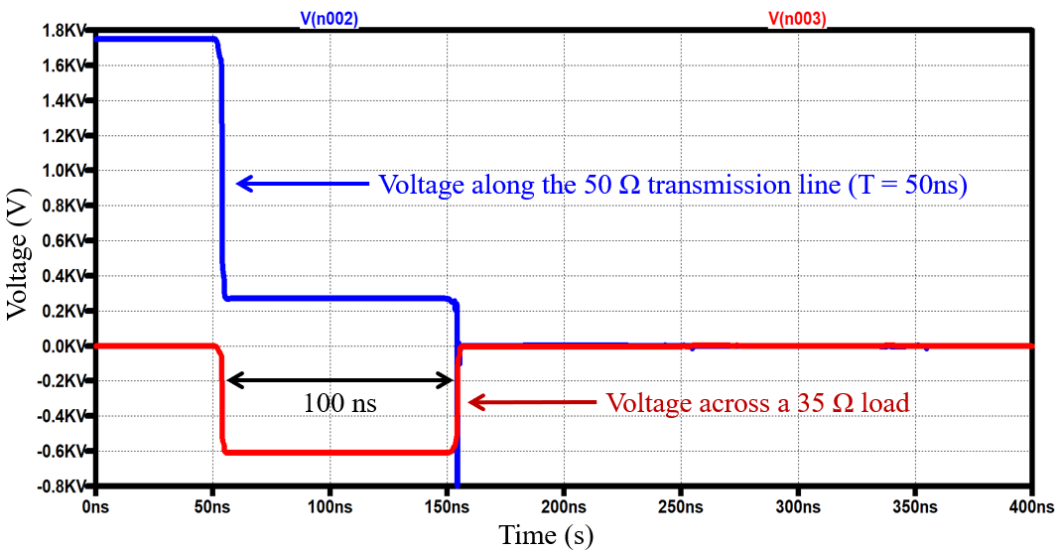


Fig. 5.22. (a) LTSpice simulation schematic of a charged line technique with five stacked FMMT417 avalanche transistors operating as a fast-switching element to producing a negative pulsed electric field (b) measure simulation voltage signal along the transmission line (blue waveform) and across the load (red waveform)

Summary

This simulation work confirms that stacking avalanche transistors as a switching element along with a charged transmission line that is an open circuit at the distal end can generate fast nsPEFs with a wide range of amplitude, duration, and polarity. This simulation work validates that the pulse duration of the nsPEFs produced is determined by the length of the transmission line. The amplitude of the nsPEF and associated reflection coefficient of the circuit is determined by the impedance relationship between the transmission line's characteristic impedance (Z_0) and the load impedance (Z_L), which must take into account the ON-resistance of each device stacked ($R_{(on)}$). The amplitude of the nsPEF is limited by the collective collector-emitter breakdown voltage of a single device (BV_{CES}) But the transistors can be stacked to produce an amplitude of nBV_{CES}, where 'n' is the number of transistors in the stack.

The rise times of the nsPEFs are determined by the characteristics of the switching element and therefore by the avalanche breakdown characteristics. The transition times for the nsPEFs are identical regardless of the number of transistors that are stacked. A trigger, or a control signal, determines when the pulses are produced. The duration of the trigger, or the control signal, must be longer in duration than the duration of the nsPEF generated to allow the charged line to be fully discharged.

A positive nsPEF can be generated when the load is placed between the lowest stacked transistor, Q_1, emitter terminal and ground plane. A negative nsPEF can be generated when the load is placed at the proximal end of the transmission line between its outer conductor and the ground plane of the circuit.

This LTSpice simulation work supports the topology for generating high voltage fast nsPEF using avalanche transistors and an open circuit transmission line meets the requirement for the fast nsPEF electroporation system given in Section 5.1. The results presented from this simulation subsection are comparable with the true measured nsPEF and operation of the circuit in practice.

It must be emphasised that these simulation results do not truly represent the practical operation of the avalanche transistor but provide a first-order representation of the operation of the circuit developed for the fast nsPEF electroporation system. This is mainly because of the mathematical spice model representation used for the FMMT417 provided by the manufacturers and its operation within the LTSpice simulation software.

5.6. Verification and Validation of the final Topology

The goal is to build and test the fast nsPEF electroporation circuit simulated in the previous section that can deliver nsPEFs of durations between 10 ns and 100 ns, and amplitude in excess of 1kV, across a 50 Ω load. The design is based on the slow charging and rapid discharging of a coaxial transmission line, through a stack of avalanche transistors that operate as a fast-switching element. This circuit has been discussed in the previous section.

For this work, FMMT417 avalanche transistors are used as a fast-switching element. The FMMT417 has a collector-emitter breakdown voltage (BV_{CES}) of 320 V, and collector-emitter voltages (V_{CEO}) of 100 V, with literature reporting that these devices can produce transient times of 300 ps when avalanched [14]. By controlling the voltage drop across the FMMT417 device to be between its collector-emitter voltages of BV_{CES} and V_{CEO}, it is possible to dictate when the transistor experiences non-destructive avalanching. Where BV_{CES} is the breakdown voltage across the transistor's collector-emitter terminals with the base and emitter terminals shorted together, and V_{CEO} is the voltage across the transistor's collector-emitter terminals with the transistors base terminal left open-circuit, with 0 A base and emitter currents (I_B and I_E) [3]-[4], [9]-[10].

The circuit illustrated in Fig. 5.7 is the final topology with a 1 MΩ resistor used as the high impedance charging resistor (R_C) [29]. An RG214 coaxial cable of specific lengths is used as the open-circuited coaxial transmission line with a characteristic impedance (Z_0) of 50 Ω and a dielectric constant (ε_r) of 2.3 [30]. A single FMMT417 avalanche transistor with its base and emitter terminals connected and no external control trigger signal applied to the base terminal is used as the fast-switching element.

The results reported in this verification and validation section have been conducted on a resistive load (Z_L) of 50 Ω unless stated otherwise. The measured voltage waveforms presented in this work were captured in real-time using a Tektronix TDS5054B-NV Oscilloscope [31] with a bandwidth of 1 GHz and a LeCory PPE 5 kV high voltage probe with a bandwidth of 400 MHz and a pulse input capacitance of < 6 pF [32]. To minimize pulse reflection all the circuits were constructed using a 50 Ω microstrip line fabricated using FR4 board [24]. The voltage supply used was a Fluke 410B dc power supply [33].

5.6.1. Single FMMT417 Operation

The avalanche transistors breakdown curve given in Fig. 5.8 can be used to help describe the operation of the design given in Fig. 5.7.

Initially, the fast switch is 'open' and is 'OFF'. This is Point A in Fig. 5.8. When the high voltage dc supply is applied, the high-Q transmission line is charged to the high voltage level (V_{CC}) through the high impedance 1 MΩ resistor (R_C). This slowly charges the charged coaxial transmission line exponentially, at a rate determined by the CR time constant of the circuit $\left(V_{max} = \left(1 - e^{-\frac{t}{\tau}}\right)\right)$. At a time of 5 CR (5τ), the line is charged to 99 % value of V_{CC}. Time constant CR is determined by the total capacitance of the charged line (C_d) and the 1 MΩ value of R_C.

When the transmission line is charged to the critical voltage, Point B in 5.16., which is the collector-emitter breakdown voltage (BV_{CES}) for the FMMT417 avalanche transistor, $V_{CC} \approx BV_{CES} \approx$ 320 V, the transistor exhibits negative resistance. This causes the transistor to experience avalanching

(electron-hole regeneration). During this period, the current through R_C can be neglected, and the operation point moves from Point B to Point C in Fig. 5.8.

This moves the operating point from Point B to C on the FMMT417 avalanche transistor breakdown curve (Fig. 5.8). At this point, a fall time is observed at the transmission line non-open circuit distal end. This occurs as the voltage held on the line is quickly discharged through the avalanching FMMT417 transistor switch. At this point, a positive rise time is also observed at the load, as previously illustrated in Fig. 5.1.

The transient on the line reaches the open-circuit distal end of the transmission line in a time T (5.1). When the transient reaches the open-circuit distal end of the line, it is reflected back down the line with the same polarity towards the collector of the transistor. The time it takes for the transient to propagate down the line and back is 2T, as a pulse of width 2T is produced across the load (Z_L). The amplitude and shape of the nsPEF depend on the relationship between the characteristic impedance of the transmission line (Z_0) and the load impedance (Z_L) as shown in equations (5.6) and (5.7), as discussed.

In this example, both the load and the transmission line have an impendence of 50 Ω. This should generate a symmetrical pulse of duration 2T with an amplitude that is approximately half the voltage level of the charged line, where the charged line is charged to a voltage equal to the collector-emitter breakdown voltage, ($V_{CC} = BV_{CES}$). Therefore, the amplitude of the nsPEF generated should be half the collector-emitter breakdown voltage (BV_{CES}) of the FMMT417, $V_L = \frac{V_{CC}}{2} = \frac{BV_{CES}}{2} \approx 160$ V. Generating a nsPEFs will result in the discharge of the charged line from its voltage level V_{CC} of $BV_{CES} \approx 320$ V to half its voltage level for a time of 2T and then to a lower voltage level that is dependent on when the line is charged, i.e., when the switch is re-opened. This will change the operating point of the circuit from Point C to Point D in Fig. 5.8.

Point D is an unstable operating point that causes regeneration as a negative resistance is experienced by the avalanche transistors. This would push the operation point of the transistor from D to Point E, where the switch can be said to be in the 'OFF' state and no nsPEF is observed. If the high voltage power supply unit (PSU) is still on, and unadjusted, then the charged line is slowly re-charged to a voltage level V_{CC} of $BV_{CES} \approx 320$ V. Once the charged line is recharged to BV_{CES}, then the operation cycle of the circuit can be repeated from Point E→B→C→D→E, in Fig. 5.8, based on the voltage level across the charged line.

This cycle is repeated until the voltage level across the charged line (V_{CC}) falls below the FMMT417 transistors collector-emitter breakdown voltage ($BV_{CES} \approx 320$ V). When this occurs, no nsPEF is produced and the circuit is 'OFF'.

In conclusion, this circuit operation would result in the generation of a nsPEF across a load with a duration of twice the delay time, 2T, with minimal pulse reflections. The amplitude is approximately half the avalanche collector-emitter breakdown voltage of the transistor $\left(\frac{BV_{CES}}{2} \approx \frac{320}{2} \approx 160\ V\right)$. The number of nsPEFs generated will be continuous until the voltage on the line drops to a voltage level that is below the collector-emitter breakdown voltage (BV_{CES}) of the transistor. The repetition frequency associated with the nsPEFs is dependent on the total capacitance of the charged line and its length. The longer the transmission line, the longer the nsPEF duration will be, and the longer the associated charging time of the transmission line and the lower the repetition frequency, or greater the time between pulse generation.

Fig. 5.23. shows the measured nsPEF across a 50 Ω load with a length of RG214 of 1 m, 5 m, and 17 m, with associated delay time (T) of 5 ns, 25 ns and 85 ns respectively. A charged line length of 1 m, 5 m, and 17 m produced nsPEFs of 10 ns, 50 ns and 170 ns respectively.

All three pulses generated across the 50 Ω load, in Fig. 5.23 have identical sub-nanosecond rise times. This emphasizes that the characteristic of the avalanche transistor defines the transition times of the topology and that sub-nanosecond rise times are achievable. It is known that the avalanche transistors can switch with a transition time of 300 ps and associated bandwidth of 1 GHz. The LeCroy PPE 5 kV high voltage probe has an associated system bandwidth of 400 Mz (2.5 ns) and this limits what can be measured in practice [39].

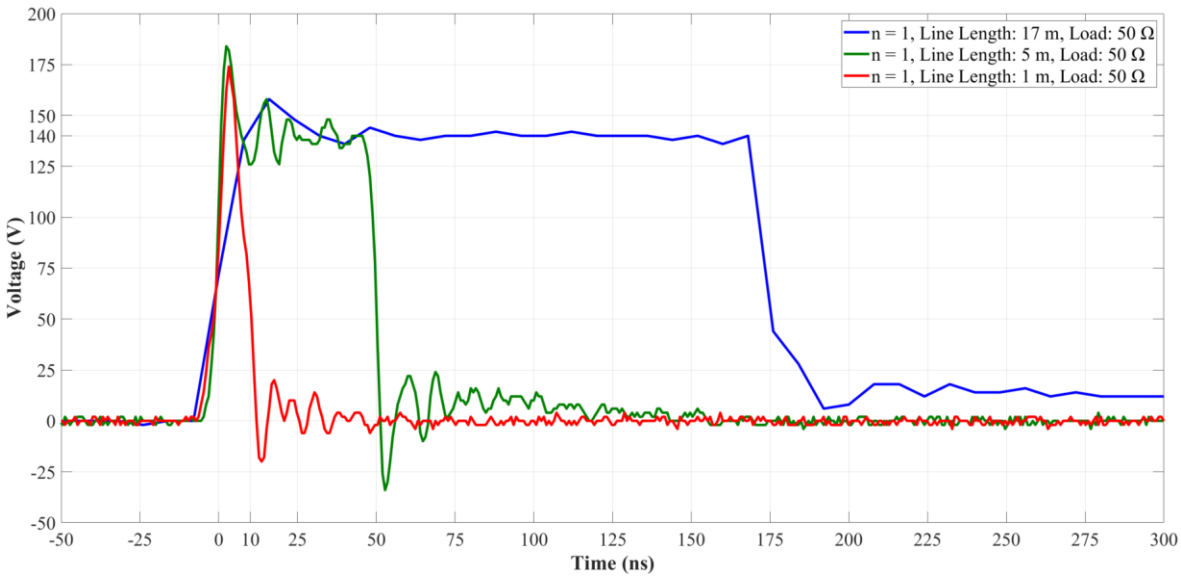


Fig. 5.23. Measured pulsed electric field across a 50 Ω load, by implementing a 17 m (blue), 5 m (green) and 1 m (red) line length with a single FMMT417 avalanche transistor.

The amplitude of the nsPEFs is limited by the FMMT417 transistor's collector-emitter breakdown voltage (BV_{CES}). When the charged line is charged to the approximate value of the FMMT417 transistor collector-emitter breakdown voltage (BV_{CES}), of around 320 V, the transistor experiences avalanching.

If the charged line voltage level exceeds the transistor's BV_{CES} value, it can inflict permanent damage on the transistor. This provides an approximate voltage level that the RG214 cable can be charged up to in practice to initiate avalanching and nsPEF generation using this circuit.

Fig. 5.24. demonstrates the voltage level V_{CC} across the charged line. A supply voltage of ~340 V initiates avalanching and the generation of the nsPEFs. As discussed, Fig. 5.23 show that nsPEFs of ~140 V amplitude are observed across the 50 Ω load with all three-line lengths. This amplitude is almost half the voltage that initiates the avalanche breakdown of the transistor of ~340 V. The relationship between Fig. 5.23 and Fig. 5.24 illustrates the basic operation of a charged/delay line generator shown in Fig. 5.1.

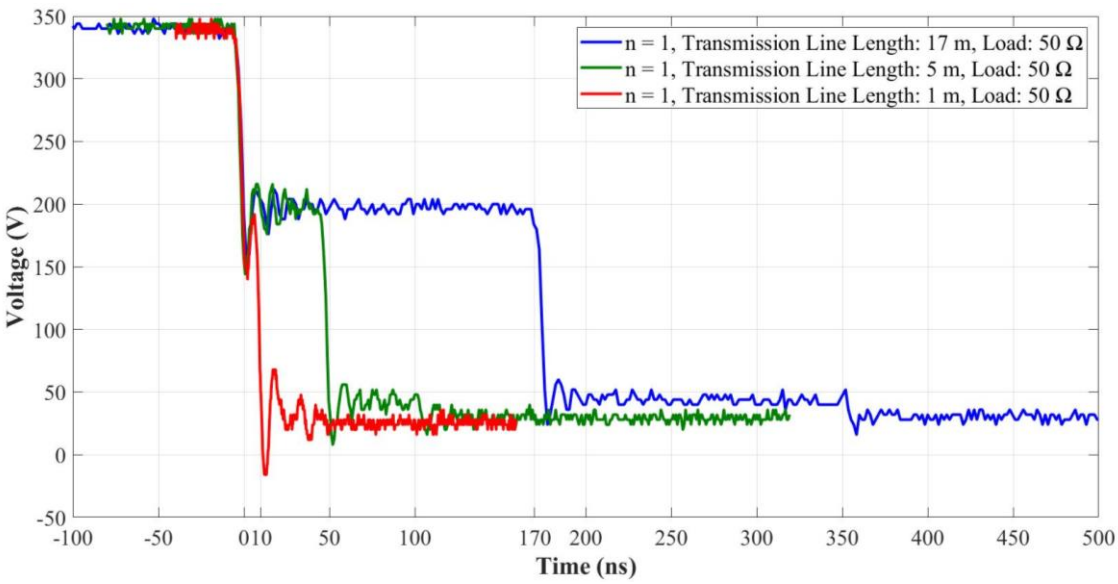


Fig. 5.24. Measured result of the fall time or discharge of the charged line with various charged line lengths of 17 m (blue), 5 m (green) and 1 m (red) with a single FMMT417 avalanche transistor delivered into a 50 Ω load.

Considering the 170 ns PEF shown in Fig. 5.23, a reflected pulse of approximately 20 V of identical duration (170 ns) directly follows the initial 140 V, 170 ns PEF. In theory, as both the transmission line and load have an impedance are 50 Ω the reflection coefficient is expected to be 0 and no pulse reflection should be observed following the initial pulse. The amplitude of the reflected pulse is 20 V, this follows the initial 140 V amplitude PEF. This implies that a reflection coefficient (Γ) of 0.14 $\left(\frac{V^-}{V^+} = \frac{20}{140}\right)$ is produced. Because of the 0.14 voltage reflection coefficient associated with the circuit, a nsPEF with an amplitude of 140 V is observed rather than the predicted amplitude of 170 V $\left(\frac{BV_{CES}}{2} = \frac{340}{2}\right)$. This can be analysed by adapting equations (5.6) and (5.10) to contain the reflection coefficient (Γ) as indicated below.

$$V_L = \frac{Z_L}{Z_L + Z_0} BV_{CES} = \frac{Z_L}{Z_L + Z_0} BV_{CES}(1 - \Gamma) \approx \frac{Z_L}{Z_L + Z_0} V_{CC}(1 - \Gamma) \tag{5.20}$$

$$V_L = \frac{BV_{CES}}{2}(1-\Gamma) = \frac{340}{2}(1-0.14) = 170 \text{ x } 0.86 = 146.2 \text{ V}$$

Where $\frac{BV_{CES}}{2}$ is the estimated nsPEF amplitude if the transmission line (Z_0) and the load impedance (Z_L) are identical, and Γ is the reflection coefficient. Appling (5.20) to the result observed in Fig. 5.23, an estimated nsPEF amplitude of 140 V is produced. It should be noted that this is the same as the amplitude of the incident nsPEF observed in Fig. 5.23.

Figures 5.25, 5.26 and 5.27 show the measured voltage level/signal across the charged line or across the collector-emitter of the FMMT417 avalanche transistors, when the nsPEFs were produced.

Fig. 5.24 shows that the voltage level along the charged line falls from the transistor's collector-emitter breakdown voltage, 360 V, to a voltage level of 200 V over a period of 2T. This voltage occurs when a nsPEF is delivered across a representative load. This is highlighted further in Fig. 5.26. After a time period of 2T, the voltage level across the charged line and the load drops to a voltage level of ~ 0V.

Following this, the charged line is slowly recharged to the transistor's collector-emitter breakdown voltage (Vcc = BV_{CES}). This is indicated in Fig. 5.25. This switching operation is then repeated (Point E→B→C→D→E in Fig. 5.8). The cycle of charging and discharging the coaxial transmission line is demonstrated in Fig. 5.25. The repetition frequency of the nsPEF is proportional to the time elapsed between successive avalanching of the FMMT417, and this is dependent on the time to charge the line.

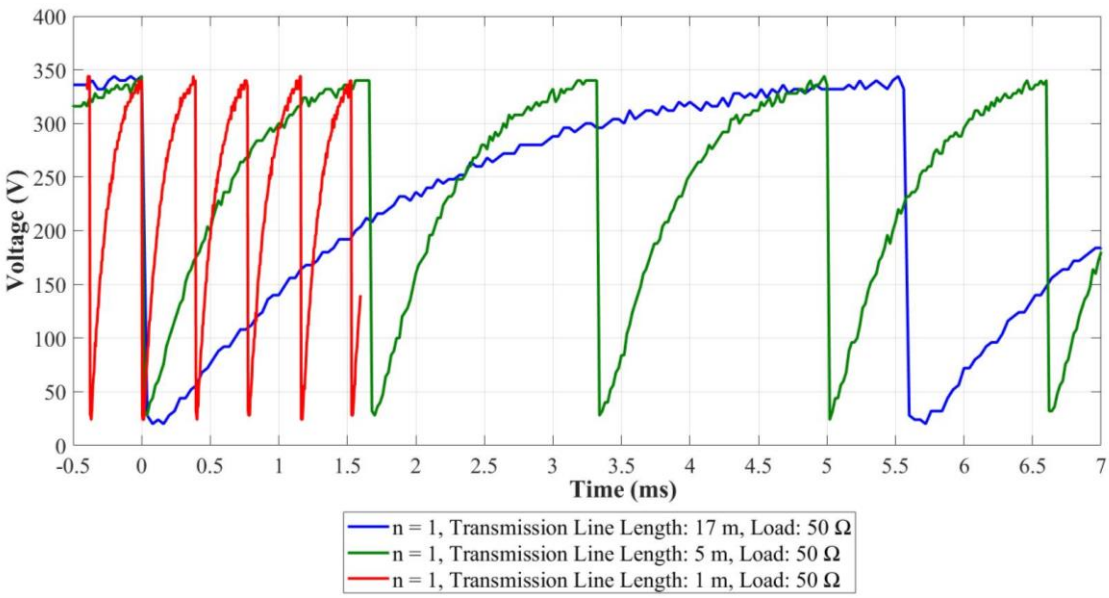


Fig. 5.25. Measured voltage level across a charged line of 17 m (blue), 5 m (green) and 1 m (red) in length with a single FMMT417 avalanche transistor and a 50 Ω as a load.

The capacitance of the RG214 coaxial cable used in the design is 100.98 pF per meter. Since the velocity of propagation in RG214 cable is 66% of the speed of light (c = $3x10^8$ m/s), the velocity of the wave propagation along the cable will be 1.98x108 m/s. Therefore, the length of RG214 required to

produce a 10 ns pulse is $\frac{10x10^{-9}s \text{ x } 1.98x10^{8}m/s}{2}$ = 0.99 m. This means that the capacitance (Cd) will be 0.99 m x 100.98 pF/m = 100 pF. Therefore, the time to charge the line through a 1 MΩ resistor will be 100 pF x 1 MΩ x 5 = 0.5 ms. Therefore, the maximum pulse repetition frequency will be approximately 2 kHz. This will reduce as the length of the pulse increases.

Fig. 5.25 shows the voltage across a 1 m, 5 m and 17 m transmission line with a 1 MΩ charging resistor. This corresponds to repetition frequencies of 2.5 kHz (0.4 ms), 588 Hz (1.7 ms) and 179 Hz (5.6 ms) respectively. Fig. 5.26 confirms that using an avalanche transistor with a charged line is a stable technique to produce nsPEFs with sub-nanosecond rise times.

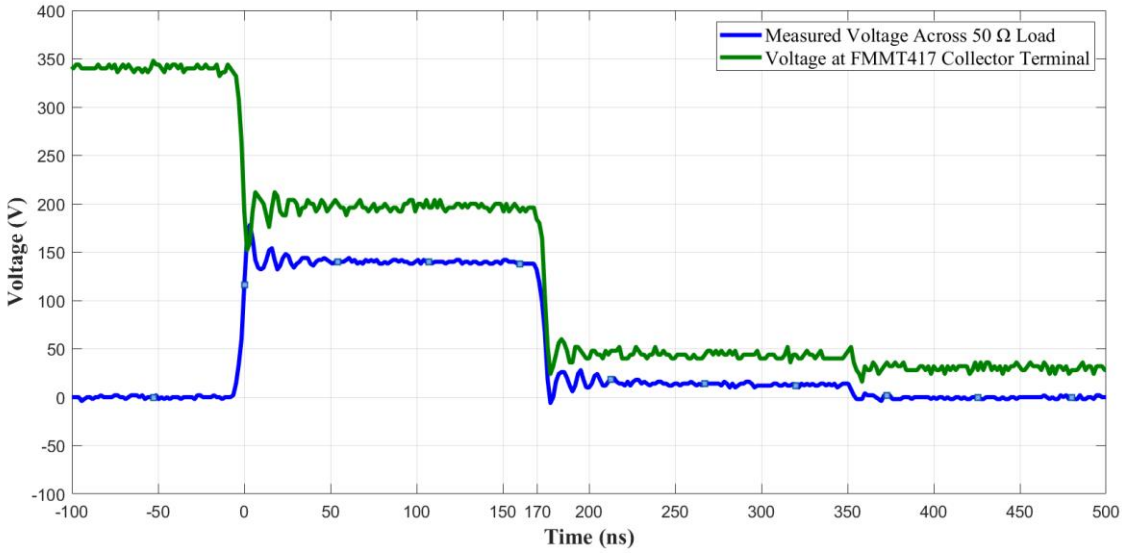


Fig. 5.26. Principle of charged line technique for the generation of rectangular pulsed electric fields with an avalanche transistor as the switching element. Showing the voltage across the FMM7417 transistor (green) and across the 50 Ω load (blue)

Summary

It has been shown that a fast pulse can be implemented based on an FMMT417 avalanche transistor and an open-circuit coaxial transmission line of various lengths. Pulses of 10 ns, 50 ns and 170 ns duration can be generated with an amplitude of up to 140 V using one transistor.

Adaptation of this topology was required to meet the requirement for a fast nsPEF electroporation system. An increase in the amplitude of the nsPEFs and control of when the number and the repetition frequency between the nsPEFs was needed. Once these features were implemented, this made this topology a viable and desirable nsPEF electroporation system circuit for use in biomedical applications. This work justifies the adaptations required to this topology for the development of a high voltage fast nsPEF electroporation system.

5.6.2. Stacking FMMT417 transistors to Produce Higher Voltage Pulses

It is possible to arrange avalanche transistors in series to enable higher voltage PEFs to be generated. This is shown in Fig. 5.27.

This involves stacking multiple FMMT417 avalanche transistors in series to generate a total voltage step of more than a kilovolt. A system to generate a pulse with a high current can be configured by stacking the avalanche transistors in parallel, but this is not a requirement for the pulses developed in this work. Using this arrangement, an increase in the voltage amplitude is observed [3]-[4], [9]-[10], [14].

Each transistor in the stack has its base and emitter terminal connected and is linked to the collector terminal of the next transistor in the stack. The base-emitter terminals of the lowest transistor (Q_1) in the stack are connected via a 1:1 pulse transformer. This is also illustrated in Fig. 5.27. The emitter terminal of the lowest transistor in the stack (Q_1) is connected to the load (Z_L). The transformer supplies the trigger or control signal to the base terminal of Q_1. The significance of the transformer is described in a later subsection, '5.3.3. Triggering Control'. The collector of the highest transistor in the stack (Q_n) is connected to the charged line at the proximal end.

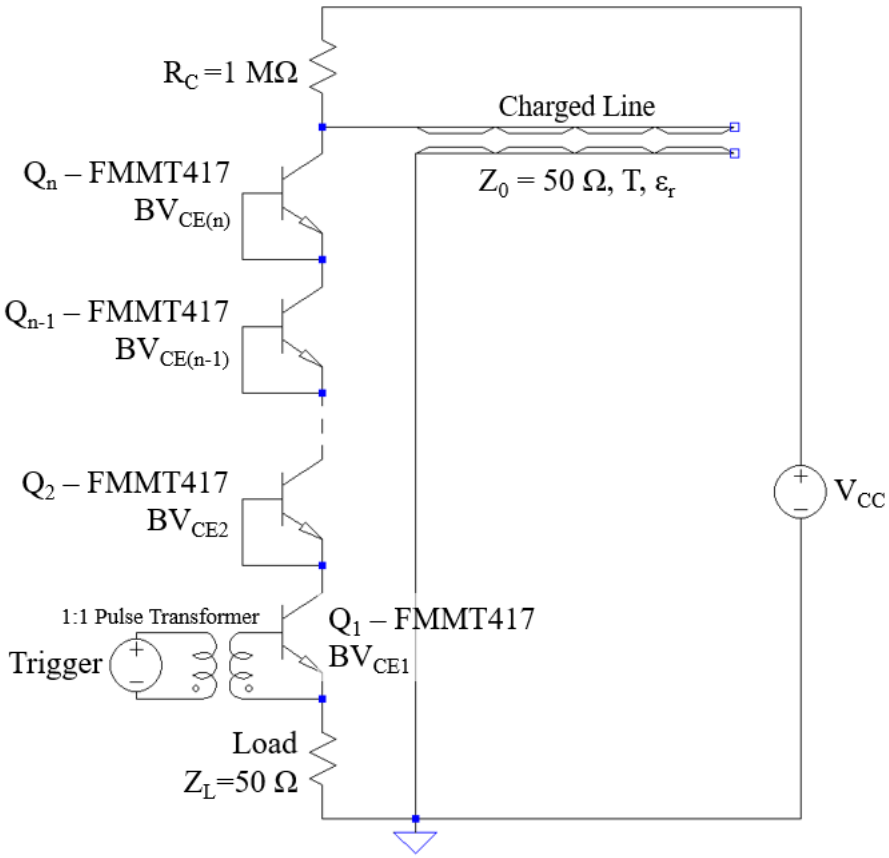


Fig. 5.27. Pulsed electric field circuit utilizing a charged line technique using a stack of avalanche transistors as the fast-switching element and controlled by an external trigger signal across the base-emitter of Q_1 using a 1:1 pulse transformer.

In theory, the amplitude of the pulse across the load increases linearly with each additional transistor in the stack. The maximum voltage level that can be placed across the charged line before a transistor or transistors in the stack experience permeant breakdown is V_{CCmax}

$$V_{CC_{max}} = n\, BV_{CES} \tag{5.21}$$

And the voltage drop across each transistor can be calculated by

$$V_{drop} = \frac{V_{CC_{max}}}{n} \tag{5.22}$$

where V_{CCmax} is the maximum voltage the transmission line can be charged to before transistor breakdown occurs, BV_{CES} is the breakdown voltage of each transistor, V_{drop} is the voltage dropped across a transistor in the series stack, and n is the number of transistors that are stacked. As the transistors are stacked in series, the current through each transistor is identical. The power is dissipated evenly across each transistor:

$$P_{dis} = V_{drop}\, \mathrm{I} \tag{5.23}$$

where P_{dis} is the power that is dissipated by each transistor in the stack, and I is the current flowing through the transistors.

If the transistors are matched the voltage drop is shared equally across each of the transistors in the stack. This voltage drop should not exceed the collector-emitter breakdown voltage for the transistor. Therefore $V_{drop} = BV_{CES}$. The maximum voltage that a stacked FMMT417 transistor arrangement can withstand is given by equation (5.21), and the maximum amplitude of the nsPEFs generated is given by equation (5.24).

$$V_{L_{max}} = \frac{Z_L}{Z_L + Z_0} nBV_{CES} \tag{5.24}$$

where *n* is the number of transistors that are stacked in series, BV_{CES} is the collector-emitter breakdown voltage of each transistor, and V_{Lmax} is the maximum amplitude of the nsPEF that can be generated across the load (Z_L). Z_0 is the transmission line characteristic impedance and Z_L is the load impedance.

Through stacking avalanche transistors, the voltage level across the transmission line (V_{CC}) and the maximum pulse amplitude that can be generated across a load (V_{Lmax}) is dependent on the number of avalanche transistors that are stacked in series (n), and the collector-emitter breakdown voltage of the selected transistor (BV_{CES}). This is assuming that the transistors that are stacked are matched. It should be noted that the maximum amplitude of the PEF is also dependent on the breakdown voltage of the coaxial cable used.

It is known that an avalanche transistor can be operated and controlled in a precise manner if the voltage drop across each transistor is between the BV_{CES} and V_{CEO} collector-emitter voltages for the transistor. Where BV_{CES} is the breakdown voltage, with the base and emitter terminals shorted together (the maximum collector-emitter operating voltage for avalanche). V_{CEO} is with the transistors base terminal left open-circuit, with 0 A base and emitter currents (I_B and I_E) (the minimum collector-emitter operating voltage for avalanche). [3]-[4], [9]-[10].

The minimum voltage level a charged line needs to reach in a stacked avalanche transistor topology for a controlled non-destructive avalanche switching (V_{CCmin}) can be found using equation (5.25). The minimum nsPEF amplitude that can be generated from a stacked transistor topology (V_{Lmin}) is given by equation (5.26).

$$V_{CC_{Min}} = n\, V_{CEO} \tag{5.25}$$

$$V_{L_{Min}} = \frac{Z_L}{Z_L + Z_0} n V_{CEO} \tag{5.26}$$

where V_{CCmin} is the recommended minimum voltage level for a charged line to successfully control the non-destructive avalanching of an avalanche transistor following exposure to a trigger signal. V_{Lmin} is the minimum amplitude of a nsPEF that can be generated across a load, n is the number of transistors that are stacked in series, and V_{CEO} is the collector-emitter breakdown voltage (with the base of the transistor left in an open-circuit).

The amplitude of nsPEF is dependent on the relationship between the transmission line characteristic impedance (Z_0) and the load impedance (Z_L) of the load voltage is $V_L = \frac{Z_L}{Z_L+Z_0} V_{CC}$. The estimated amplitude of the nsPEF for the overall system with no reflection occurring is when $Z_0 = Z_L$ and the resulting pulse amplitude across the load V_L is $\frac{50}{50+50} V_{CC} = \frac{V_{CC}}{2}$.

For the FMMT417 transistor to operate as a controlled switching element, the voltage drop across its collector-emitter junction should lie between its avalanche breakdown voltages BV_{CES} and the collector-emitter voltage V_{CEO}.

So, $BV_{CEO} < V_{CC} > V_{CES}$ $\quad$ $100 < V_{CC} > 32$

For a stack of FMMT417 avalanche transistors to operate as a controlled switch the voltage across the charged line, or charged voltage, should not exceed VCCmin or VCCmax. The value of VCCmin and VCCmax voltages for FMMT417 transistors are as follows:

$$V_{CC_{max}} = nBV_{CES} = n\,320 \qquad V_{CC_{min}} = nV_{CEO} = n\,100$$

$$V_{CC_{min}} < V_{CC} > V_{CC_{max}}\,, \qquad nV_{CEO} < V_{CC} > n\,BV_{CES}\,, \qquad n\,100 < V_{CC} > n\,320$$

If the charged line is charged to a voltage level that exceeds V_{CCmax}, then the voltage drop across each transistor would exceed the collector-emitter breakdown voltage (BV_{CES}) and causes destructive avalanching of the transistors in the stack. Resulting in the permeant destruction of the FMMT417 devices.

If the charged voltage is below V_{CCmin} then the voltage drop across each transistor is below its V_{CEO}, and non-destructive avalanching of the transistors in the stack will not occur, with or without a trigger signal.

If the voltage along the charged line is between the V_{CCmin} and V_{CCmax}, the voltage drop across each transistor is between their BV_{CES} and V_{CEO} values. These voltage levels would allow the transistors to avalanche non-destructively by applying a trigger control signal to the lowest transistor in the stack (Q_1). This would provide an ideal condition for the trigger signal to initiate the generation of the nsPEFs and control the repetition frequency between each nsPEF generated.

The estimated maximum and minimum amplitudes of the pulsed electric fields are:

$$V_{L_{max}} = n\frac{BV_{CES}}{2} = n\frac{320}{2} = n160 \qquad V_{L_{min}} = n\frac{BV_{CEO}}{2} = n\frac{100}{2} = n50$$

This assumes that the transmission line characteristic impedance (Z_0) is equal to the load impedance (Z_L) i.e., zero reflection voltage ($\Gamma = 0$).

Table 5.5. exemplifies the maximum and minimum voltage limits for controlled non-destructive avalanching of stacked transistors, and the associated nsPEF amplitude that would be generated across a load with a specific number of stacked transistors.

Table 5.5. The maximum and minimum charged line voltage level and pulse amplitude that could be achieved with a specific number of transistors stacked as a switching element. Assuming that $Z_0 = Z_L$.

Number of transistors	V_{CCmax} (V)	V_{CCmin} (V)	V_{Lmax} (V)	V_{Lmin} (V)
$\boldsymbol{n}$	nBV_{CES}	nBV_{CEO}	$n160$	$n50$
1	320	100	160	50
2	640	200	320	100
3	960	300	480	150
5	1,600	500	800	250
…	…	…	…	…
7	2,240	700	1,120	350
…	…	…	…	…
10	3,200	1,000	1,600	500
20	6,400	2,000	3,200	1,000

Example: if $Z_L = Z_0 = 50\ \Omega$, BV_{CES} (V_{CES}) for a typical FMMT417 is 320 V and V_{CEO} is 100 V (from the datasheet for a FMMT417 [27]) and n = 10;

$$V_{L_{max}} = \frac{Z_L}{Z_L + Z_0} nBV_{CES} = \frac{50\ \Omega}{50\ \Omega + 50\ \Omega} \text{ x 10 x 320 V} = \frac{50 \text{ x 10 x 320}}{100} = 1{,}600 \text{ V}$$

$$V_{L_{Min}} = \frac{Z_L}{Z_L + Z_0} nV_{CEO} = \frac{50\ \Omega}{50\ \Omega + 50\ \Omega} \text{ x 10 x 100 V} = \frac{50 \text{ x 10 x 100}}{100} = 500 \text{ V}$$

The circuit shown in Fig. 5.27 operates as follows. Initially, all the stacked avalanche transistors are in their 'OFF' state. When a positive trigger signal is applied to the base of Q_1, via a pulse transformer, Q_1 is turned 'ON' and places its collector voltage near ground potential. Q_1 essentially acts as a short circuit and the collector current flows through the transistor collector and the load (Z_L) which is grounded. This then results in a voltage drop across the second lowest avalanche transistor in the stacked (Q_2). Thus, creating the desired condition for the overvolting of Q_2, which causes Q_2 to avalanche in a non-destructive manner. This enables the transistor to turn 'ON', and places Q_2's collector terminal near ground potential.

This creates a sequential 'knock-on' effect on the next transistor in the chain (Q_3) resulting in its overvolting. Each stage (or transistor) in turn switches 'ON' and "sees" an even greater over voltage that exceeds its avalanche transistor breakdown voltage (BV_{CES}). This 'knock-on' effect causes all of the transistors in the chain to avalanche in a non-destructive manner, from the lowest avalanche transistor in the chain (Q_1) to the final avalanche transistor in the series chain (Q_n). Q_n's collector terminal is connected to the proximal end of the coaxial delay line.

When Q_n is turned 'ON' and experiences non-destructive avalanching, a fast rise time is produced at the load (Point B to C in Fig. 5.8, avalanche transistor V_{CE}–I_C breakdown curve) allowing the charged line to discharge through the chain of stacked avalanche transistors and across the load (Z_L). This results in a pulse with a width of 2T and a maximum pulse amplitude of $\frac{nBV_{CES}}{2}$ to be generated across the load (Z_L) if Z_0=Z_L.

If the voltage across the charged line matches, or slightly exceeds the value of V_{CCmax}, then the voltage drop across each of the transistors matches their breakdown voltage (BV_{CES}). This causes all the avalanche transistors in the chain to experience destructive avalanching. The result is the generation of a nsPEF across the load of 2T in duration and amplitude of V_{Lmax}, in a continuous circuit operation. Where the pulse repetition frequency timing characteristic will not be dictated by the trigger signal into Q_1 but by the associated charging time of the transmission line used (5.5). This operation is identical to the operation described in subsection 5.5.1.

Fig. 5.28 demonstrates that stacking multiple avalanche transistors in series produces the desired pulse amplitude across the load (Z_L). The measured nsPEF across a 50 Ω load is shown in Fig. 5.29. The set-up used an RG214 transmission line with a characterised impedance of 50 Ω with line lengths of 1 m, 5 m and 170 m. With every FMMT417 avalanche transistor added to the stack, the measured

amplitude of the nsPEF across the load increased by an estimated voltage of 140 V. As discussed, this is approximately half the value of the FMMT417 breakdown voltage $\left(\frac{V_{CES}}{2}\right)$.

(a)

(b)

(c)

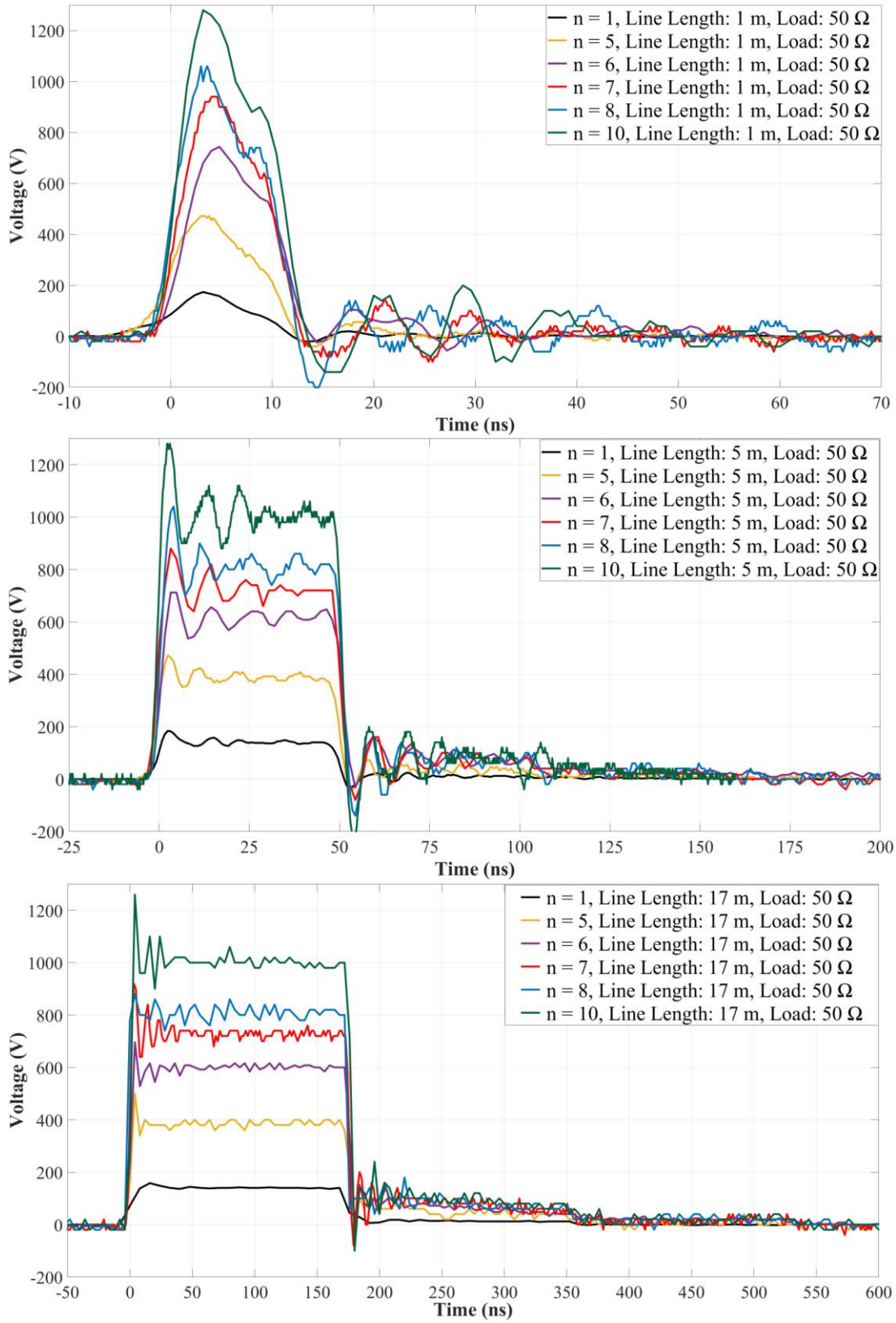


Fig. 5.28. Measured pulsed electric fields across a 50 Ω load with a single (1), 5, 6, 7, 8 and 10 avalanche transistors stacked as the switching element and a transmission line length of (a) 1 m (2T = 10 ns), (b) 5m (2T = 50 ns), and (c) 17 m (2T = 170 ns).

The nsPEFs measured across the 50 Ω load shown in Fig. 5.28 have comparable rise and fall times regardless of the duration of the pulse and the number of transistors stacked to create the fast-switching element.

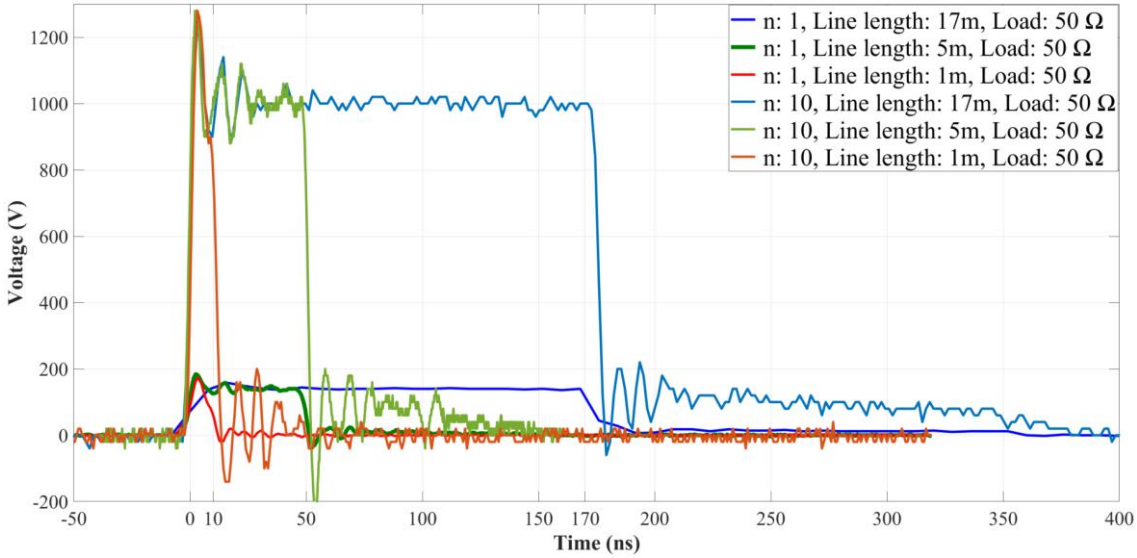


Fig. 5.29. Measured pulsed electric fields across a 50 Ω load with a single and 10 avalanche transistors stacked as the switching element accompanied by a transmission line length of 1 m (2T = 10 ns), 5m (2T = 50 ns), and 17 m (2T = 170 ns).

Fig. 5.30 also shows the pulses produced by a single and 10 transistors as a switching element. Except for some variation in amplitude, overshoot and ringing the pulses are the same.

Fig. 5.31. illustrates that stacking 20 FMMT417 avalanche transistors with a 1 m length of RG214 transmission line produces a 10 ns PEF with an amplitude of 2,500 V and a transition time of less than one nanosecond, across a 50 Ω load. With each additional transistor added to the stack, the stray inductance present in the circuit increases. Stray inductance can slow the rise time of the nsPEF.

The rationale for selecting the FMMT417 transistor was due to the high collector-emitter breakdown voltage of 320 V, its low inductance of 2.5 nH and the availability in a surface mount SOT23 package [27]. Additionally, the surface mount SOT23 package and microstrip PCB layout adopted allow for a compact stacking layout, which further reduces unwanted stray inductance. The use of microstrip PCB and surface mount avalanche transistors was purposely employed to reduce stray capacitance and inductance to maximise the number of transistors that could be used to create the fast switch without pulse degradation.

Nevertheless, there will be a point where the rise time of the nsPEF generated from this topology will be greater than a nanosecond because of the influence of additional stray inductance presented with each transistor added. Future design considerations to overcome this drawback could be to place a capacitor in parallel with each transistor, or a set of transistors to add capacitance to each stage(s) to counteract the effect of FMMT417 2.5 nH inductance effect.

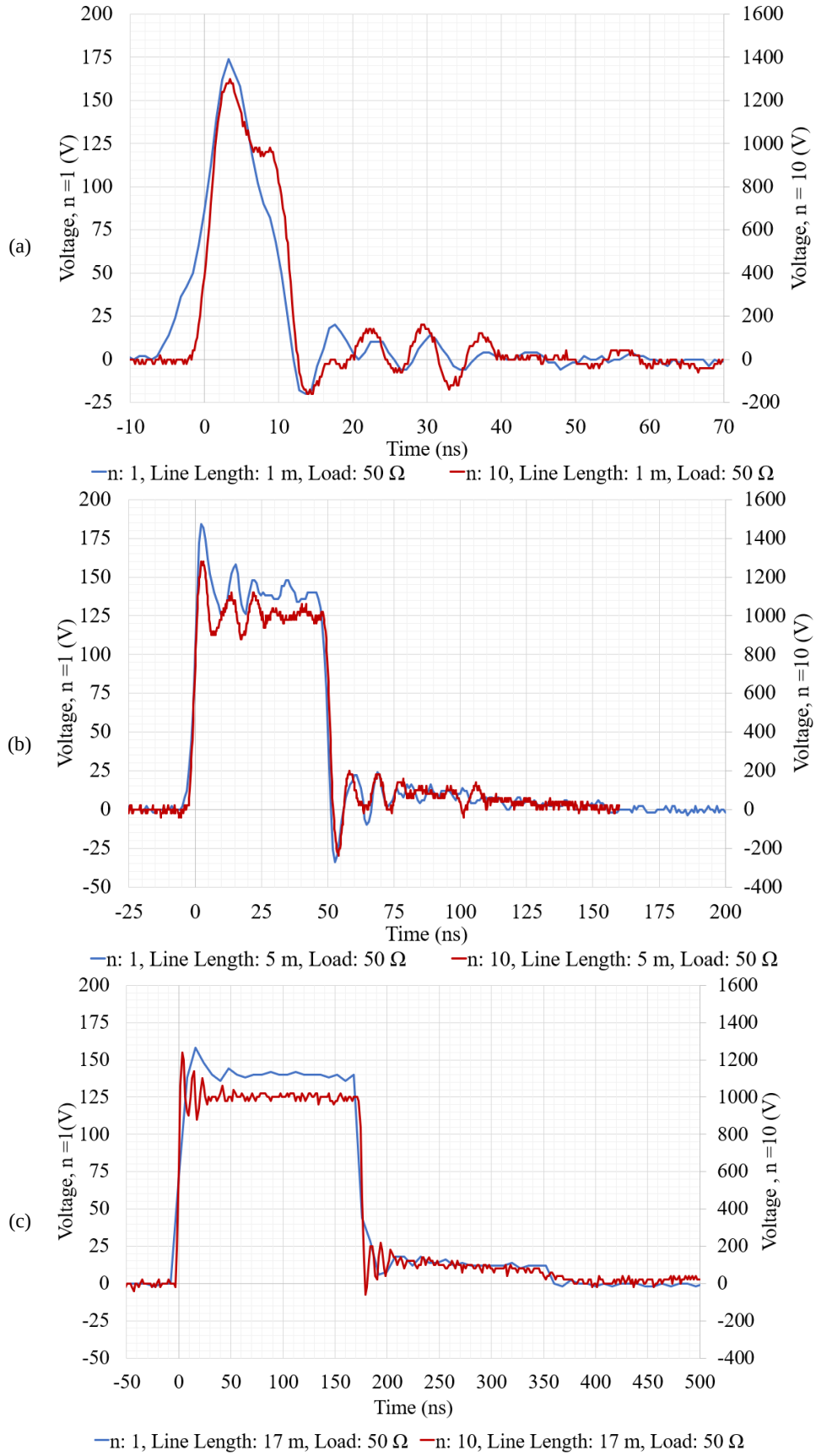


Fig. 5.30. Overlayed Measured pulsed electric fields across a 50 Ω load with a single transistor (blue waveform) and 10 avalanche transistors stacked (red waveform) as a switching element accompanied by a transmission line length of (a) 1 m (2T = 10 ns) (b) 5m (2T = 50 ns), and (c) 17 m (2T = 170 ns)

Nevertheless, there will be a point where the rise time of the nsPEF generated from this topology will be greater than a nanosecond because of the influence of additional stray inductance presented with each transistor added. Future design considerations to overcome this drawback could be to place a capacitor in parallel with each transistor, or a set of transistors to add capacitance to each stage(s) to counteract the effect of FMMT417 2.5 nH inductance effect.

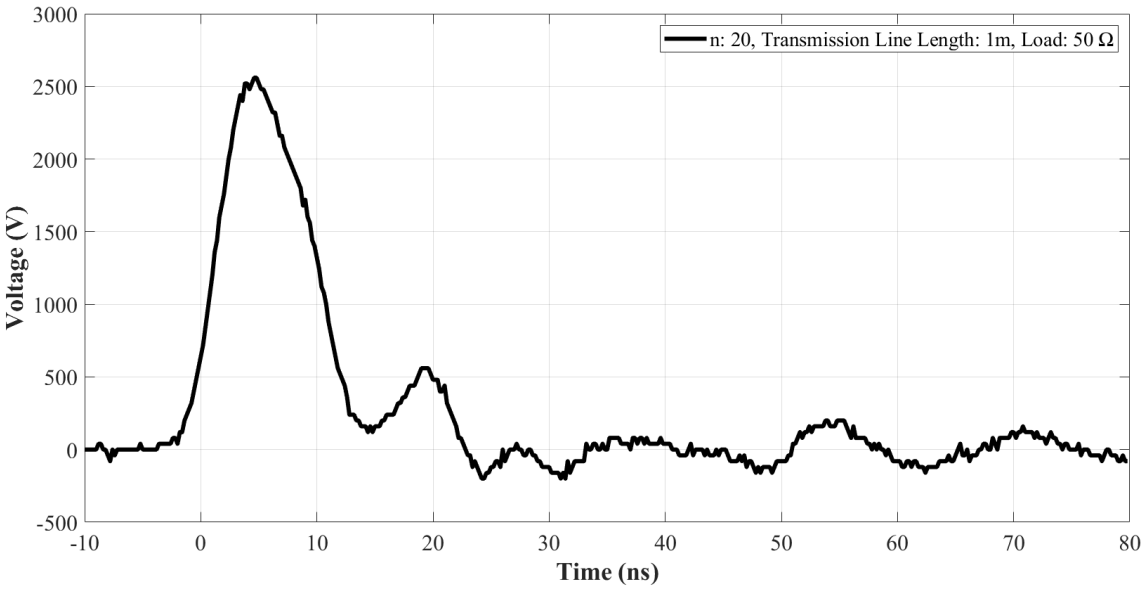


Fig. 5.31. Measured pulsed electric field across a 50 Ω load with 20 avalanche transistors stacked as the switching element accompanied by a transmission line length of 1m (2T = 10 ns)

The value of the capacitor that can be placed in parallel with each transistor to compensate for its stray inductance can be found by

$$C = \frac{L}{Z^2} \tag{5.27}$$

L is the collector-emitter inductance of an avalanche transistor and Z is the impedance requirement of the microstrip PCB.

In this situation, a 50 Ω impedance (Z) must be maintained throughout the circuit from the characteristic impedance of the charged line (Z_0) through the microstrip PCB to the 50 Ω load (ZL). The collector-emitter inductance of the FMMT417 avalanche transistor is 2.5 nH. Therefore, a capacitor of 1 pF, $C = \frac{L}{Z^2} = \frac{2.5n}{50^2} = 1pF$, in parallel with each stacked transistor would counteract the 2.5 nH collector-emitter inductance of the FMMT417 avalanche transistor. A capacitor can be placed across a specified number of transistors and the value of this capacitor can be calculated by

$$C = n\frac{L}{Z^2} \tag{5.28}$$

where n is the number of avalanche transistors the capacitor will be placed in parallel across.

This subsection investigated the possibility of stacking avalanche transistors to increase the amplitude of the nsPEF. It showed that it is possible to generate a nsPEF with amplitude in excess of 1 kV by stacking seven avalanche transistors. A switching element designed with 20 transistors stacked in series can produce a nsPEF with an amplitude of 2.5 kV.

The nsPEFs produced with multiple transistors had similar timing characteristics, including transition times and pulse width. The transition times achieved were below a nanosecond, suggesting that the total impedance of the multiple transistors does not affect the transition time of the nsPEFs. Additional capacitors were not used in the design to counteract the stray inductance created by the FMMT417 surface mount packages.

For future pre-clinical and clinical applications (Chapter 6), the voltage amplitude is limited to 1,500 V due to the breakdown voltage of microwave cables, such as the SUCOFROM_86_CT [43] for non-invasive surgery and associated international standards for medical devices (ISO 13485). The SUCOFROM_86_CT and its associated connectors have a maximum operating voltage of 1,500 V and this sets the maximum pulse amplitude that can be produced. Because of this limitation, ten avalanche transistors are the best implemented in the final nsPEF system. This is because a stack of ten transistors (n=10) can provide the necessary nsPEFs amplitude in excess of 1 kV with a range of pulse widths from 10 ns to 170 ns as illustrated in Fig. 5.28, Fig. 5.29 and Fig. 5.30.

5.6.3. Triggering Control

The circuit implemented in Fig. 5.7 operates through the relatively slow charging and rapid discharging of an open circuit coaxial transmission and has no means of controlling the timing characterises. Timing characterises such as when the pulses will be produced, the number of pulses in a burst, and the repetition frequency. The only timing characterises that could be controlled was the duration of the nsPEF. When the voltage on the charged line reached the collector-emitter breakdown voltage (nBV_{CES}) the generation of nsPEF began. This operation was continuous until the voltage level of the charged line was below the avalanche transistor's breakdown voltage, or when the voltage exceeded the transistor’s breakdown voltage.

During this continuous cycle of operation, the repetition frequency of the nsPEFs is associated with the time constant it takes for the charge line to charge to the transistor BV_{CES} level following the avalanche transistor’s non-destructive avalanching. The associated repetition frequency or charging time is associated with the total capacitance of the line and the resistor in the charging circuit (R_C). This provides a limitation in the current circuit, in that the repetition frequency is dependent on the time constant, or charging time, of the cable implemented. This implies that a unique repetition frequency is given for a specific length of transmission line and associated nsPEF duration. This is highlighted in Fig. 5.25. The operation of this circuit as it stands requires a precise ‘biting point’ relationship between

the voltage level across the transmission line and the breakdown voltage of the avalanche transistor to switch the system 'ON'. This is highlighted in Table 5.6.

Table 5.6. 'Single FMMT417 Operation' circuit operation depending on the voltage across the coaxial transmission line (V_{CC}) relationship with the collector-emitter breakdown voltage of an avalanche transistors (BV_{CES})

V_{CC} and BV_{CES} Relationship	Descriptive comment
$V_{CC} \approx BV_{CES}$	Non-destructive avalanching of transistors. Continuous avalanching of transistor and nsPEF generation. (Point E→B→C→D→E in Fig. 5.8) across a load, at a repetition frequency that is dependent on the charged line charging time.
$V_{CC} < BV_{CES}$	No nsPEF will be generated. Avalanche breakdown voltage not reached
$V_{CC} > BV_{CES}$	Avalanche transistor will experience a destructive avalanching. Transistor permanently destroyed and no further nsPEF is produced.

For a fast nsPEF electroporation system to support nanosecond electroporation, and other nsPEF-related research, there is a need for a system that can be controlled to deliver a specific number of nsPEFs at a required repetition frequency when required.

Triggering the base terminal of the lowest stacked transistor, as shown in Fig. 5.27, is a technique to control the switching characterises of a transistor and the time characteristics of the generated nsPEF [3]-[4], [9]-[10].

Applying a voltage signal, or trigger signal, directly to the base terminal of a transistor allows the transistor to operate like a switch. When sufficient base-emitter voltage (V_{EBO}) is applied, the transistor is switched 'ON'. This causes a non-destructive avalanche breakdown between the collector and emitter terminal of an avalanche transistor, driving the collector to emitter voltage to 0 V. The maximum V_{EBO} or emitter-base breakdown voltage (BV_{EBO}) rating of the FMMT417 avalanche transistor is 6 V [19]. When the collector-emitter voltage is driven to 0 V, the transistor acts as a short circuit, or a closed switch and the current flows through the transistor to the load.

Applying this external trigger signal drives the FMMT417 transistor into a non-destructive avalanche mode, resulting in a fast rise time in the collector current which produces a pulse across the load with a sub-nanosecond rise time. This triggering signal makes it possible to control when the transistor is switched 'ON' and therefore dictates the number of pulses produced, and the repetition frequency of the pulses. The amplitude, duration, and shape (reflection) parameters of the pulses are determined by the length of the line and the relationship between the transmission line characteristic impedance (Z_0) and load impedance (Z_L) [3]-[4], [9]-[10].

The repetition frequency and the number of nsPEFs produced would be identical to the repetition frequency and the number of trigger control signals across the base and emitter terminals of the first transistor (Q_1).

For the successfully controlled triggering and non-destructive avalanching of a transistor, and the generation of nsPEF, certain conditions must be met. The first condition is that the maximum emitter-base voltage (V_{EBO}) rating of the FMMT417 avalanche transistor must not be exceeded [19]. The V_{EBO} rating of the FMMT417 is 6 V. Therefore, a 5 V trigger signal or a transistor-transistor logic (TTL) signal would be sufficient to trigger non-destructive avalanching of the transistor.

The voltage level across the charged line must be between the collective collector-emitter breakdown voltages of the transistors $nBV_{CEO} < V_{CC} > nBV_{CES}$ [3]-[4], [9]-[10].

The pulse duration of the triggering pulse must be longer in duration than the duration of the nsPEF generated, and therefore longer than twice the associated delay time of the charged line used (2T). This switching condition provides sufficient time for the charged line to fully discharge [3]-[4], [9]-[10]. The maximum nsPEF duration of the fast nsPEF electroporation system aims to deliver is 300 ns. To meet this condition, the duration of the trigger control signal should be longer than the incident pulse across the load. A 600 ns will be sufficient to allow substantial time for the charged line to fully discharge whilst the avalanche transistor experiences non-destructive avalanching.

The repetition frequency of the trigger signal is limited to the repetition frequency that is associated with the charging time of the line (5.5), which is approximately $\frac{1}{5\tau}$. This condition will allow sufficient time for the charged line to charge to the high voltage PSU voltage level (V_{CC}). This will allow for the nsPEFs with the maximum possible pulse amplitude to be generated.

Fig. 5.32 illustrates how a trigger signal is applied to the system to initiate nsPEFs generation. The trigger signal is applied to the transistor via a 1:1 transformer, with the secondary coil output of the transformer between the base and emitter terminals of the transistor. This isolates the voltage between the trigger signal source and the potentially high voltage nsPEF circuit. Additionally, it reduces unnecessary noise/interference that could be feedback without distorting the signal shape of the trigger signal. With the inclusion of the transformer, the 5 V TTL trigger signal applied between the transistor's base and emitter terminals will be floating and not affected by the current through the transistor during switching.

Considering the requirement to trigger non-destructive avalanching within the fast nsPEF electroporation system, the amplitude of the trigger signal is limited to 5 V. This is because of the 6 V maximum V_{EBO} rating of the FMMT417. For a 300 ns PEF, a 30 m RG214 cable would be required, and in combination with a 1 MΩ charging resistor (R_C) the charging time of the cable is estimated to be ~15 ms (66 Hz). Therefore, a nsPEF with a repetition frequency from 1 Hz to 50 Hz can be generated efficiently by the system without compromising the charging time of the open circuit transmission line.

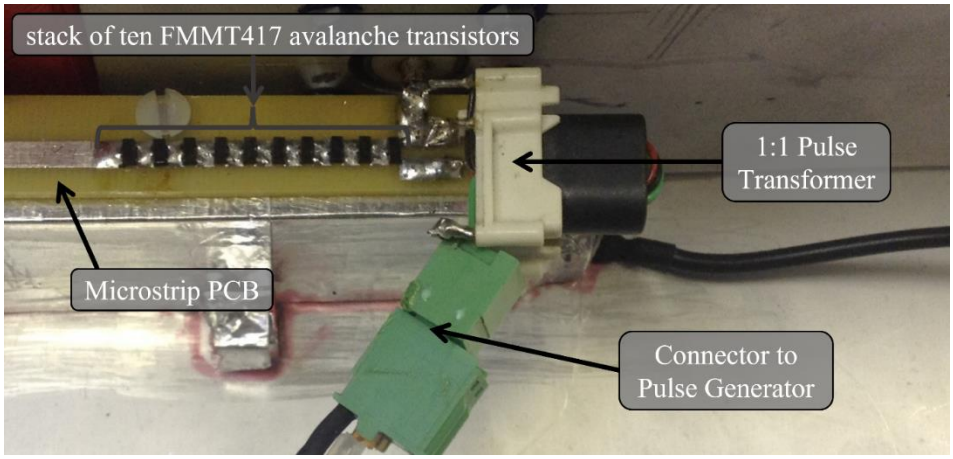


Fig. 5.32. Developed switching element consisting of a stack of ten (n=10) avalanche transistors operating as a fast-switching element with a 1:1 pulse transformer

The timing characteristics of the nsPEF generated from the fast nsPEF electroporation system will be synchronised and identical to the timing characteristics of the trigger pulse. This trigger signal will govern when, how many and the repetition frequency of the nsPEFs generated. This trigger signal was produced by using a 'Quantum Composers 9520 Series Pulse Generator' [34].

For the implementation, a 1:1 pulse transformer was placed between the base and emitter terminal of Q1 (as shown in Fig. 5.27), and the PCB is shown in Fig. 5.32 to mount the stack of avalanche breakdown transistors to minimise external inductance.

Fig. 5.33. and Fig. 5.34 show the measured voltage signal across the charged line or the voltage level at the highest stacked transistor (Q_n) collector terminal. These figures illustrate the slow charging and rapid discharging that occurs across the charged line. The rapid discharge seen in these figures (Fig. 5.33 and Fig. 5.34) indicates when a nsPEF is generated across the load. The time between these discharges indicates the repetition rate/frequency of the nsPEF generated, which is T. The repetition frequency is the inverse of this repetition rate, $f = \frac{1}{T}$.

Fig. 5.25 illustrates that nsPEFs are produced when the breakdown voltage of the transistor is reached without a trigger signal.

Fig. 5.33 demonstrates that a trigger signal can effectively manipulate the operation of the system and the triggering of an avalanche transistor, or a stack of avalanche transistors as a fast-switching element. The discharge of the charged lines occurred at a repetition rate of 20 ms, or a repetition frequency of 50 Hz, with a wide variety of charged line lengths and nsPEF durations. Therefore, the nsPEF are generated with a repetition frequency of 50 Hz that emulates the trigger control signal repetition frequency. This triggering effect is identical no matter the number of transistors that are stacked to form the switching element. Therefore, it has been shown that by implementing a trigger

signal under certain circuit parameters the number and the repetition frequency of the PEFs can be controlled.

Fig. 5.25 and Fig. 5.33. show the comparison of the nsPEF generated across a 50 Ω load with a single FMMT417 transistor operating as the switching element in a self-generating operational mode and a stack of ten FMMT417 as a switching element, operating with a trigger signal with a repetition frequency from 50 Hz (20 ms) to 1 kHz respectively.

(a)

(b)

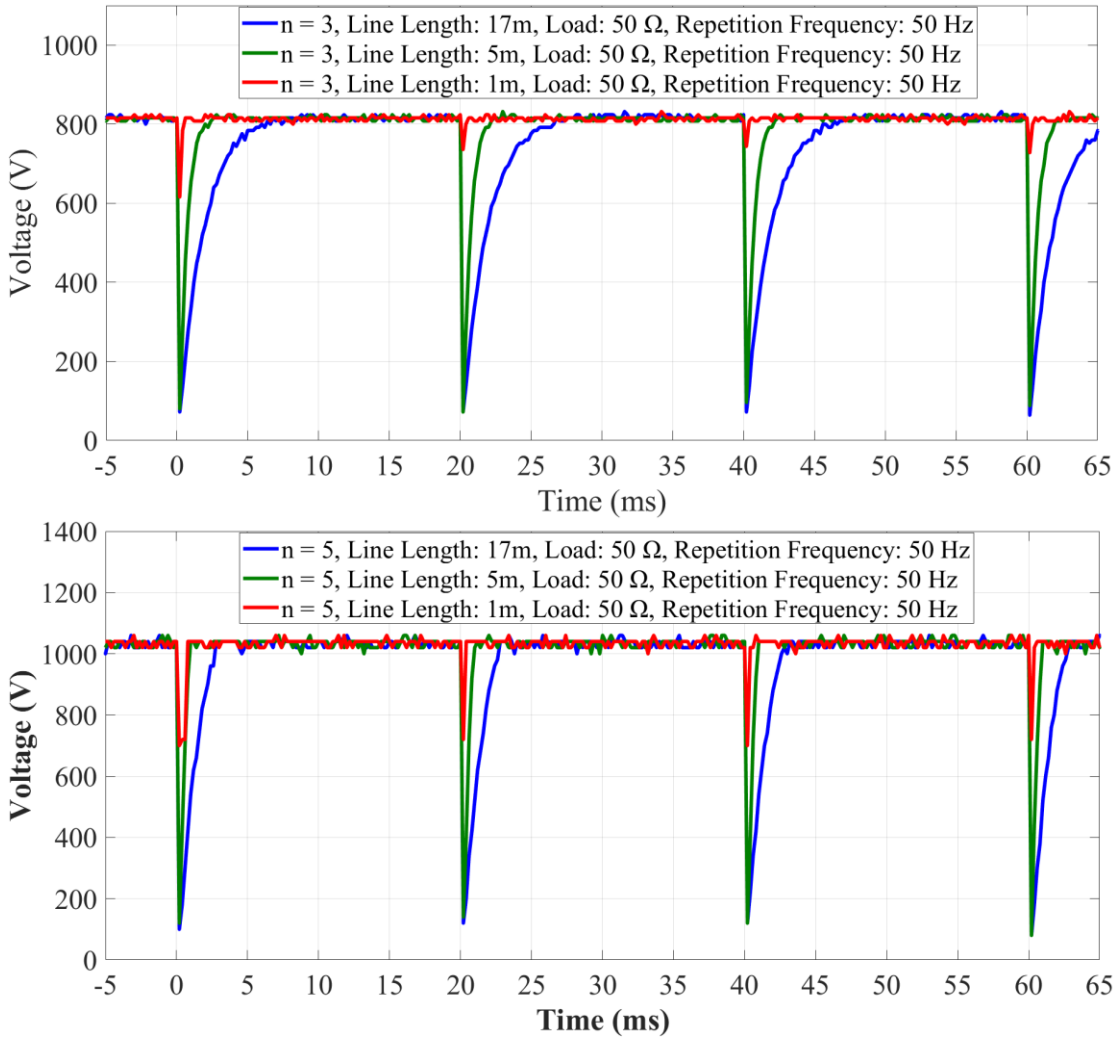
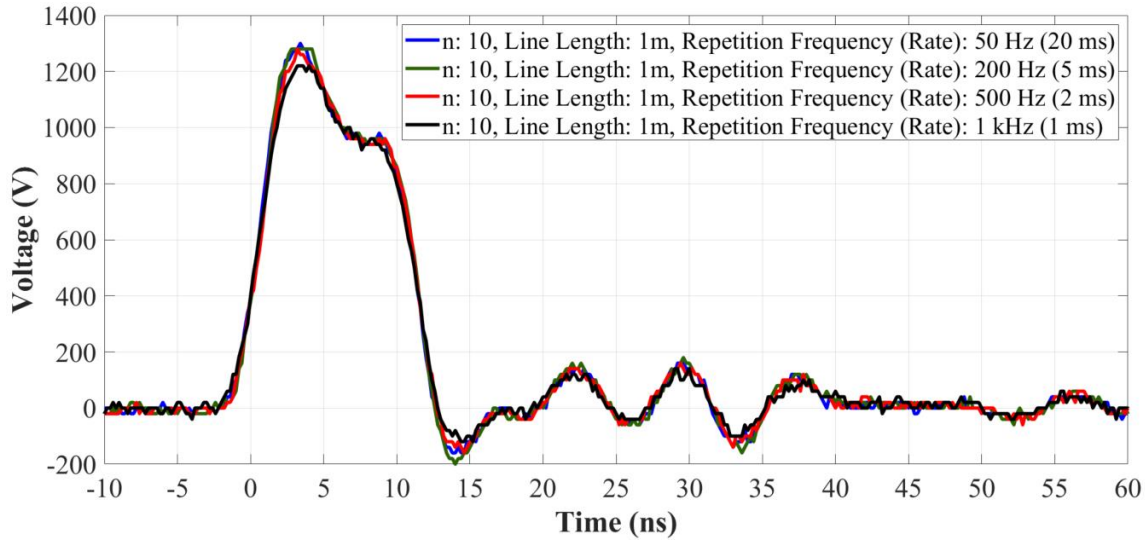
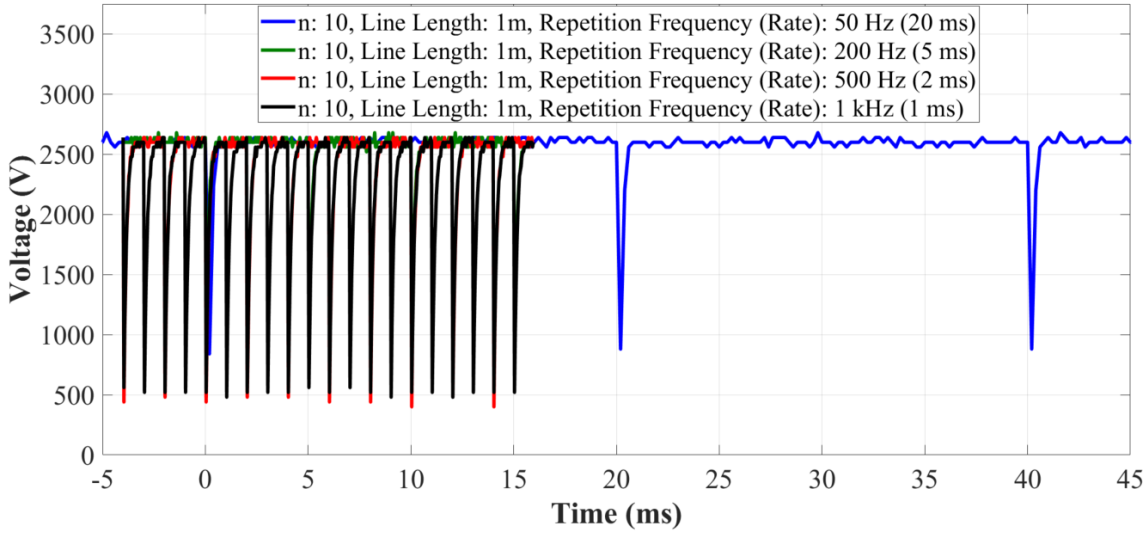


Fig. 5.33. Measured voltages across the charged line with a length of 1 m, 5 m, and 17 m with a stack of (a) three (n = 3) and (b) five (n =5) FMMT417 transistors operating under non-destructive avalanche mode ($V_{CEO} < V_{CC} > BV_{CES}$) with a trigger signal of 5 V, 600 ns pulse width with a repetition frequency of 50 Hz (period: 20 ms) across a 50 Ω.

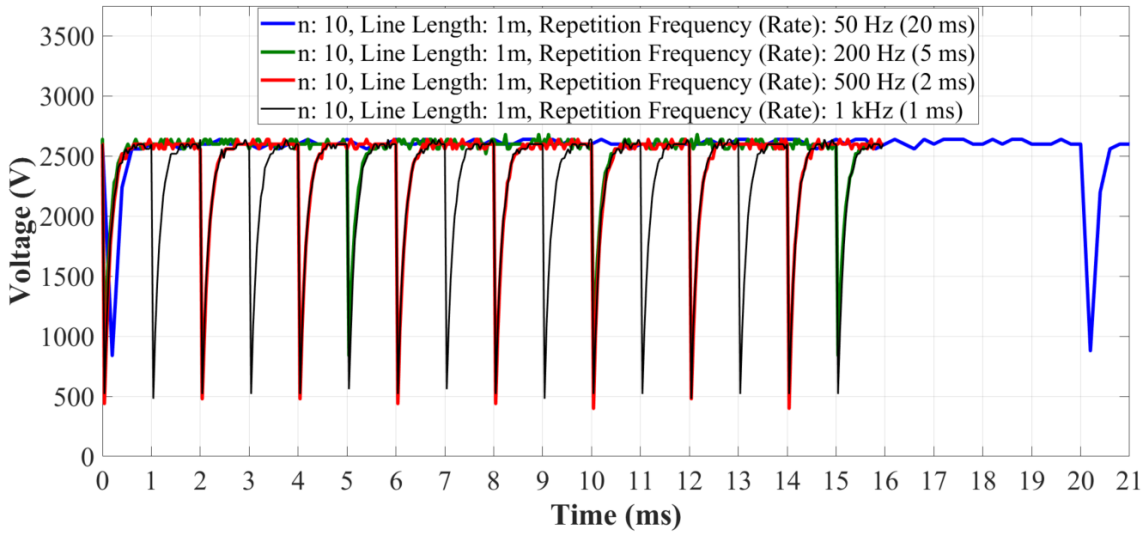
Fig. 5.33 and Fig. 5.34 verify that a trigger signal, which complies with the non-destructive avalanching previously mentioned, allows for a method of controlling when, how many and the repetition frequency of the nsPEF generated. It also reinforces that the number of transistors stacked dictates the nsPEFs amplitude and the length of the charge lines determines the nsPEFs duration.



(a)



(b.i)



(b.ii)

Fig. 5.34. Measured voltages from the fast electroporation system with a stack of ten (n=10) FMMT417 operating under non-destructive avalanche mode with a charged line length of 1 m and a trigger control signal with a repetition frequency (rate/period) of 50 Hz (20 ms), 200 Hz (5 ms), 500 Hz (2 ms) and 1 kHz (1 ms) (a) across a 50 Ω load (b) across the charged line with a x-axis scale of (i) 5 ms per division (ii) 1 ms per division.

Fig. 5.34(a) illustrates the measured 10 ns PEFs across a 50 Ω load that was generated with a stack of ten avalanche transistors in conjunction with a 1 m charged line that is operating with a trigger control signal with repetition frequencies of a 50 Hz (20 ms), 200 Hz (5 ms), 500 Hz (2 ms) and 1 kHz (1 ms). This figure demonstrates that an identical 1 kV nsPEFs of 10 ns duration is generated across a 50 Ω load when the fast nsPEF electrorotation system is driven with various trigger repetition frequencies. These repetition frequencies are 50 Hz (20 ms), 200 Hz (5 ms), 500 Hz (2 ms) and 1 kHz (1 ms).

Fig. 5.34(b) illustrate the measured voltage across the charged line. The discharging of the line in these waveforms corresponds to when a nsPEF is generated and the associated repetition frequency. It suggests that the repetition frequency of the nsPEF (or the rate at which the charged line can be charged and discharged) is identical to the repetition frequency of the trigger signal connected between the base and emitter terminals of the lowest stacked FMMT417 (Q_1).

The charging time of a 1 m charged line is ~0.4 ms as demonstrated in Fig. 5.25, Fig. 5.34, and Fig. 5.35. This is independent of the repetition rate of the trigger signal. This charging time corresponds to the time it takes for the voltage to rise from the discharged state back to the ~2600 V. The trigger signal repetition rate/frequency should not exceed the charging time of the charged line. As the charging time of the 1 m line is 0.4 ms, it was possible to generate a 1.2 kV, 10 ns PEF at a repetition rate of 1 ms, or a repetition frequency of 1 kHz. This is evidenced in Fig. 5.34.

In conclusion, Fig. 5.33 and Fig. 5.34 demonstrate that the trigger signal and its repetition frequency do not affect the charging time of the charged line, the amplitude or the duration of the nsPEFs generated. The trigger signal only dictates when, the number of pulses, and the repetition rate/frequency of the nsPEFs generated.

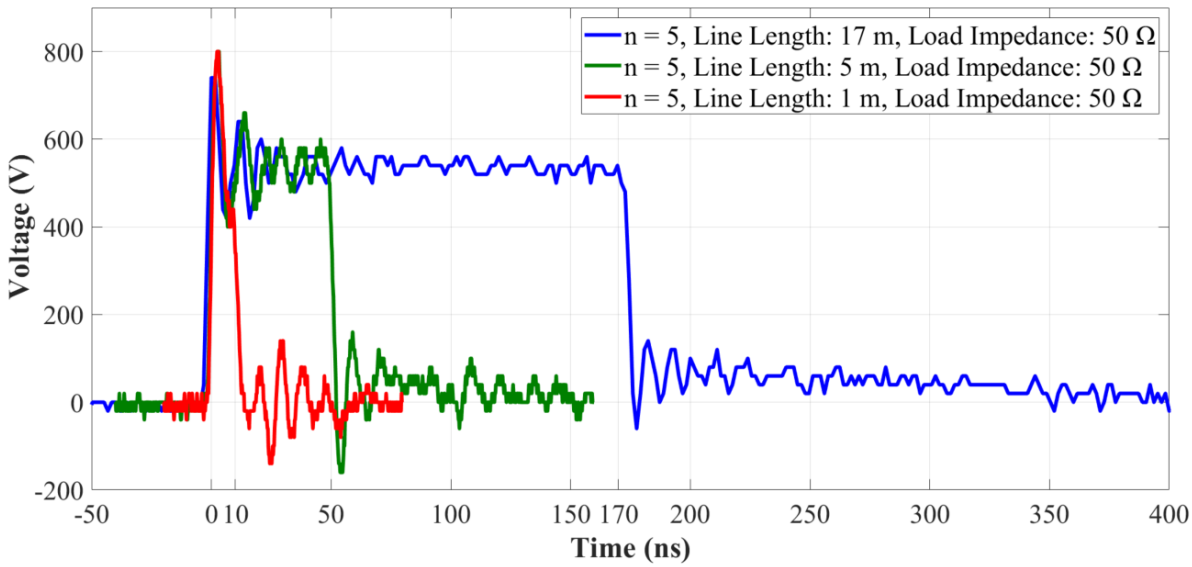
This is true if the following four conditions are met. Firstly, the base-emitter voltage of the transistor is not exceeded (BV_{EBO}). Secondly that the voltage drop across each transistor is between its collector-emitter voltage of V_{CEO} and BV_{CES}. Thirdly, the duration of the trigger signal is larger than the duration of the nsPEF that will be generated. Finally, the trigger signal repetition rate is less than the charging time (5τ) of the charged line in question.

For the developed fast nsPEF electroporation system developed in this work a trigger signal of 5 V amplitude and duration of 600 ns was sufficient to trigger avalanche switching of the stack of ten FMMT417 transistors. A 1 kV nsPEFs with durations ranging between 10 ns to 300 ns can be generated with a repetition frequency range between 1 Hz and 50 Hz. For the generation of nsPEFs, in excess of 1 kV in amplitude, with repetition frequencies in excess of 50 Hz, the charging time of the line used must be carefully considered.

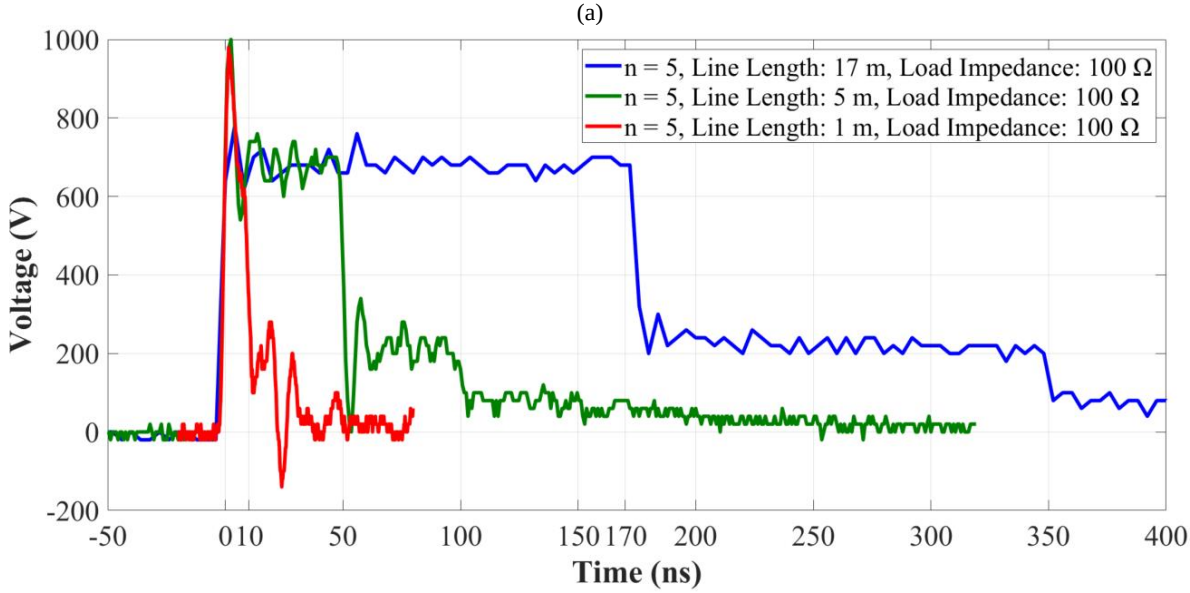
5.6.4. Pulse Formation and Reflections

Figure 5.36 and 5.37 demonstrates the effect the relationship between the load impedance (Z_L) and the charged line characteristic impedance (Z_0) has on the nsPEF generated. Fig. 5.36 compares the nsPEFs generated across a 50 Ω and a 100 Ω load with an RG214 transmission line with a characteristic impedance of 50 Ω.

The amplitude and reflection of the PEFs observed across a 50 Ω load are lower in companion to the nsPEFs measured across a 100 Ω load. With a 50 Ω load, the nsPEFs have neglectable reflection, since the reflection coefficient associated with the system is zero, as $Z_L = Z_0$. This is because $\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_L - Z_L}{Z_L + Z_L} = \frac{0}{2Z_L} = 0$.



(a)



(b)

Fig. 5.35. Measured pulsed electric fields with five (n=5) stacked avalanche transistors with a 50 Ω charged line of 1 m, 5m and 17 m in length with a load impedance of (a) 50 Ω (b) 100 Ω

The amplitude of the nsPEFs seen in Fig. 5.35(a) are identically at an amplitude of 533 V. This amplitude is approximately half the voltage level of the charged line before triggering since $Z_L = Z_0$. This is because $V_L = \left(\frac{Z_L}{Z_L+Z_0}\right)V_{CC} = \left(\frac{Z_L}{2Z_L}\right)V_{CC} = \frac{V_{CC}}{2} = \sim\frac{1100}{2} = \sim 550 \approx 533$.

In comparison, the amplitude of the nsPEFs across a higher load impedance of 100 Ω is higher, at 700 V. A ~200 V secondary nsPEF of identical duration is observed following this initial pulse. The amplitude of the nsPEFs seen in Fig. 5.36(a) is higher because of $Z_L > Z_0$. This is because $V_L = \left(\frac{Z_L}{Z_L+Z_0}\right)V_{CC} = \left(\frac{100}{100+50}\right)V_{CC} = \frac{2}{3}V_{CC} = \sim\frac{2}{3}1100 = \sim 733 \approx 700$. And the reflection coefficient of this system in this scenario is $\frac{1}{3}$. This secondary nsPEF is a reflection of the incident pulse a since $Z_L \neq Z_0$, with a reflection coefficient of 1/3. $\Gamma = \frac{Z_L-Z_0}{Z_L+Z_0} = \frac{100-50}{100+50} = \frac{1}{3}$ causing a voltage of ~200 V to be reflected back along the charged line. The reflected secondary pulse is approximately ~233 V, $\frac{1}{3}$ the amplitude of the 700 V incident pulse $\left(700 \text{ x } \frac{1}{3} \approx 233\right)$. This is observed in Fig. 5.35 and Fig. 5.36.

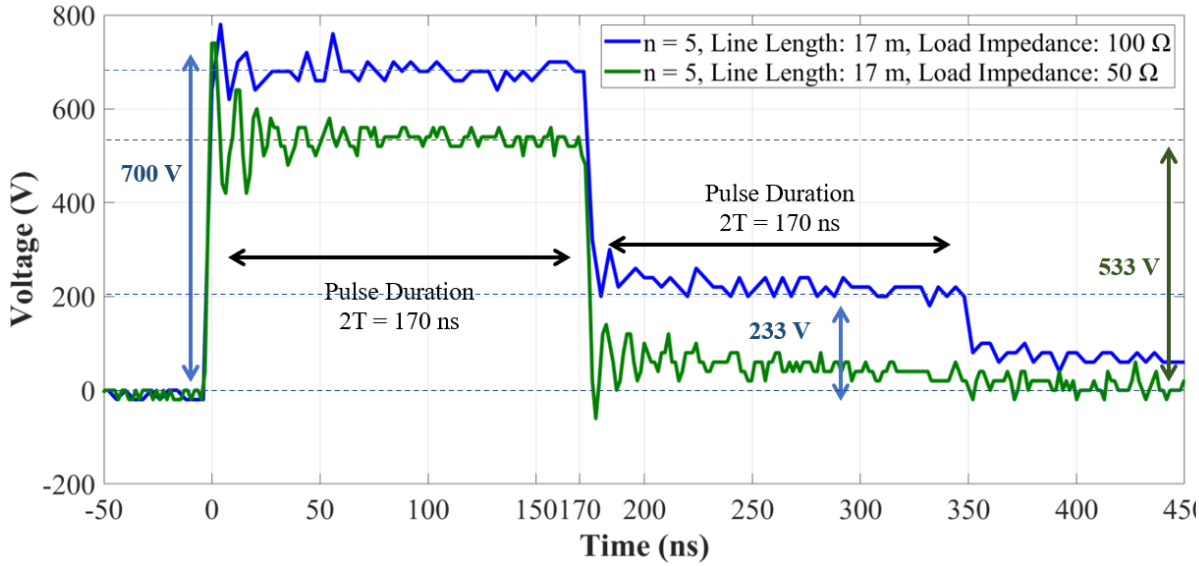


Fig. 5.36. Comparison of the measured pulsed electric field waveform with a charged line of 17 m and a stack of 5 avalanche transistors as the switching element with a load impedance of 50 Ω (green) and 100 Ω (blue)

These waveforms validate the theory in terms of the main/incident pulse and the reflected pulse produced as a function of time. The theory is highlighted in Table 5.7.

In conclusion, this section illustrated that the system design is load impedance sensitive and confirms the microwave theory associated with the design [5]. For the generation of nsPEFs with zero reflection, in future, it is best to attempt to use impedance matching techniques to match the impedance of the charged line to the impedance of the load due to the nature of the pulses. Broadband matching networks will be required.

Table 5.7. Effect of the load and charged line impedance relationship has on the pulsed electric fields amplitude and the systems reflection coefficient

Figure	Load Impedance, Z_L (Ω)	Characteristic impedance of charged line, Z_0 (Ω)	Reflection coefficient, **Γ**	nsPEF amplitude in respect to the voltage level of charged line, V_L (V)
Equation	Z_L	Z_0	$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$	$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC}$
5.38(a)	50	50	0	0.5 V_{CC} $\left(\frac{1}{2} V_{CC}\right)$
5.38(b)	100	50	0.333, $\left(\frac{1}{3}\right)$	0.666 V_{CC}, $\left(\frac{2}{3} V_{CC}\right)$

5.6.5. Pulse Polarity

Revisiting the fundamental topology for generating nsPEFs that there are two current loops present within the circuit design, as shown in Fig. 5.37. The placement of the load within a current loop, current loop two, results in the generation of nsPEFs of either a positive or negative polarity.

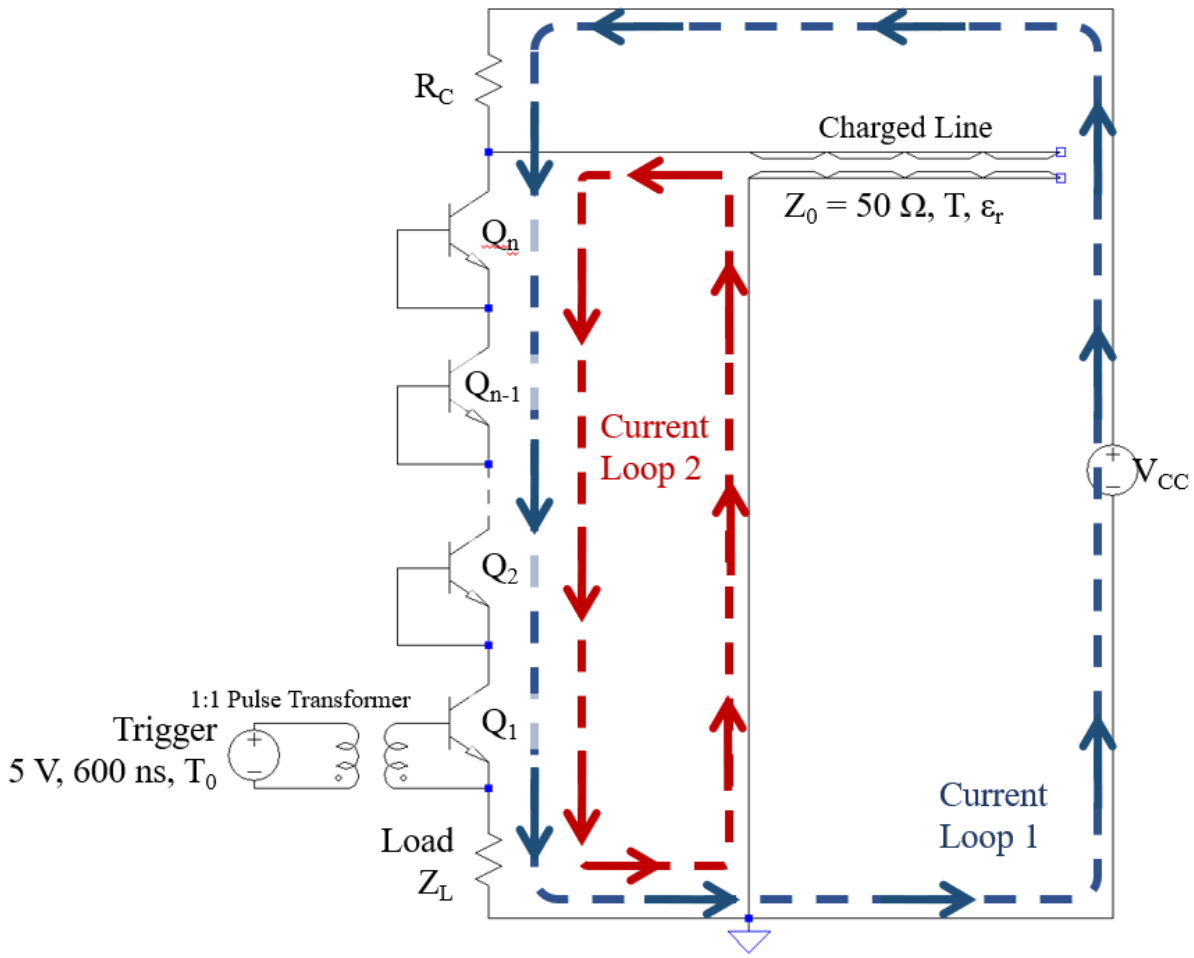


Fig. 5.37. Analysis of two current loops. Using current loop 1 (blue) and current loop 2 (red) associated with the charged line in conjunction with a stack of avalanche transistors implemented as the fast-switching element.

Fig. 5.37 illustrates the two current loops within the circuit. The first current loop, current loop one, will be a small current flow that charges the transmission/charged line via the high impedance

resistor (R_C). When the transistor stack is switched 'ON' by the triggering pulse, the energy stored in the charged line is released as a high current around the current loop two and generates a nsPEF across a load (Z_L). Up to this point, the load has been positioned between the lowest transistor (Q_1) emitter terminal and the ground plane of the system. This has produced a nsPEF with a positive polarity [3]-[4], [9]-[10].

By manipulating the high current flow, that is current loop two, and repositioning load (Z_L) from being placed between the lowest transistor (Q_1) emitter terminal and ground to a new position between the outer conductor of the charged line and ground. In this situation, the polarity of the nsPEF is reversed. The placement of the load within the second current loop changes the polarity of the nsPEF. A negative nsPEF is generated when the load is placed within the loop as illustrated in Fig. 5.38.

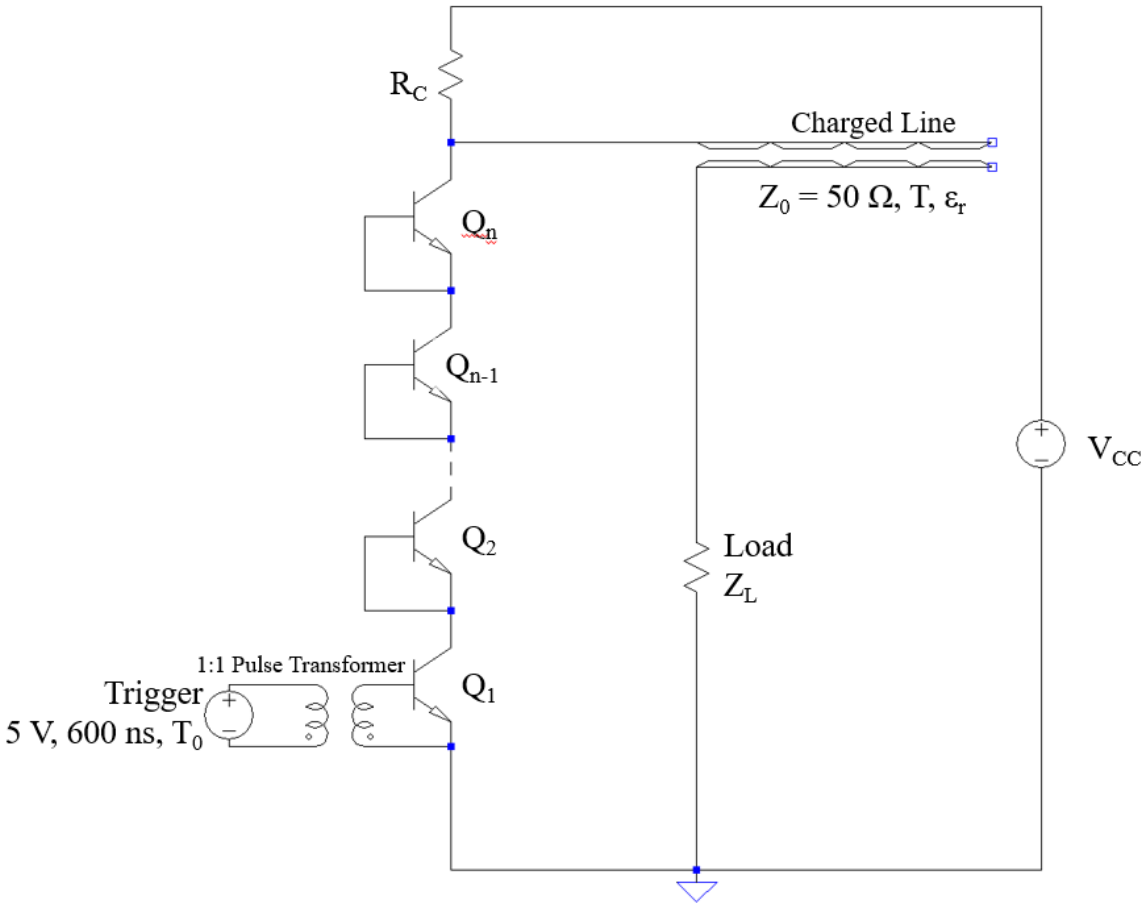


Fig. 5.38. Circuit for the generation of a negative polarity pulsed electric fields

The general characterises of the nsPEF produced across the load in figures 5.38 and 5.39 are identical, except for the pulse polarity of the pulses. These characteristics include pulse duration, transition times (rise and fall time), repetition frequency and amplitude. This is because these characteristics are determined by the external factors already discussed [3]-[4], [9]-[10].

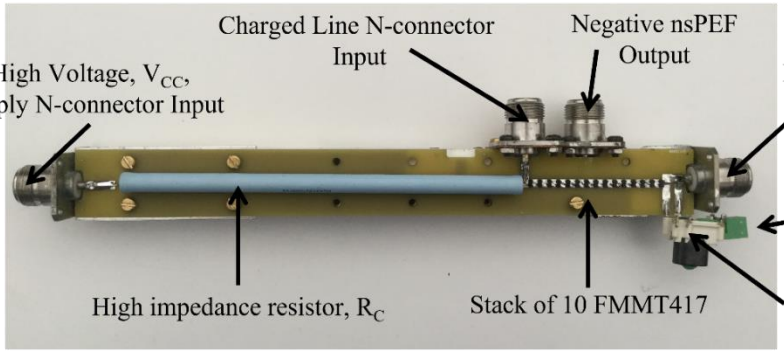
The duration of the nsPEFs is determined by the line length (l) and dielectric constant (ε_r) for the line (5.4). The amplitude and the reflection associated with the incident pulse are determined by the

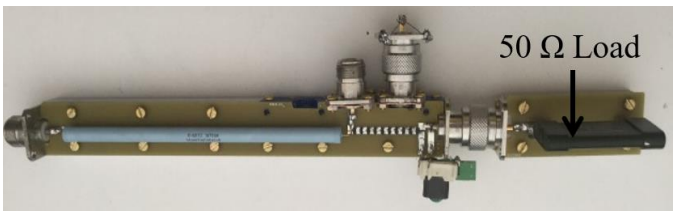
values of the load impedance (Z_L) and the characteristic impedance of the transmission line (Z_0) and the voltage level the line is charged to (V_{CC}) as shown in equations (5.6) and (5.7). The higher the number of transistors stacked the higher the amplitude of the pulse generated.

The control over when the nsPEFs are generated, the number of PEFs generated and the repetition frequency between each pulse is determined by the trigger signal applied across the base-emitter terminals of Q_1, via a 1:1 pulse transformer. This can only occur when the voltage level across the charged line is between the voltage levels of nV_{CEO} and nBV_{CES}.

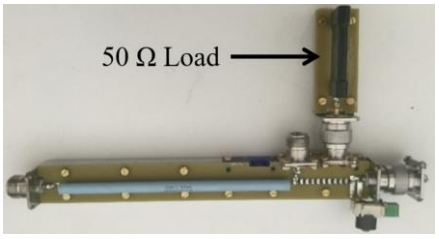
Fig. 5.39 shows the bench test circuit implemented for the fast nsPEF electroporation system. A stack of ten avalanche transistors operates as the fast-switching element to produce a nsPEF with amplitudes in excess of 1 kV. The polarity of the nsPEFs is dependent on which output connector the load is connected to. This can be seen in Fig. 5.39. For positive nsPEFs, the load is connected as shown in Fig. 5.39(b). For negative nsPEFs, the load is connected as shown in Fig. 5.39(c).

(a)





(b)

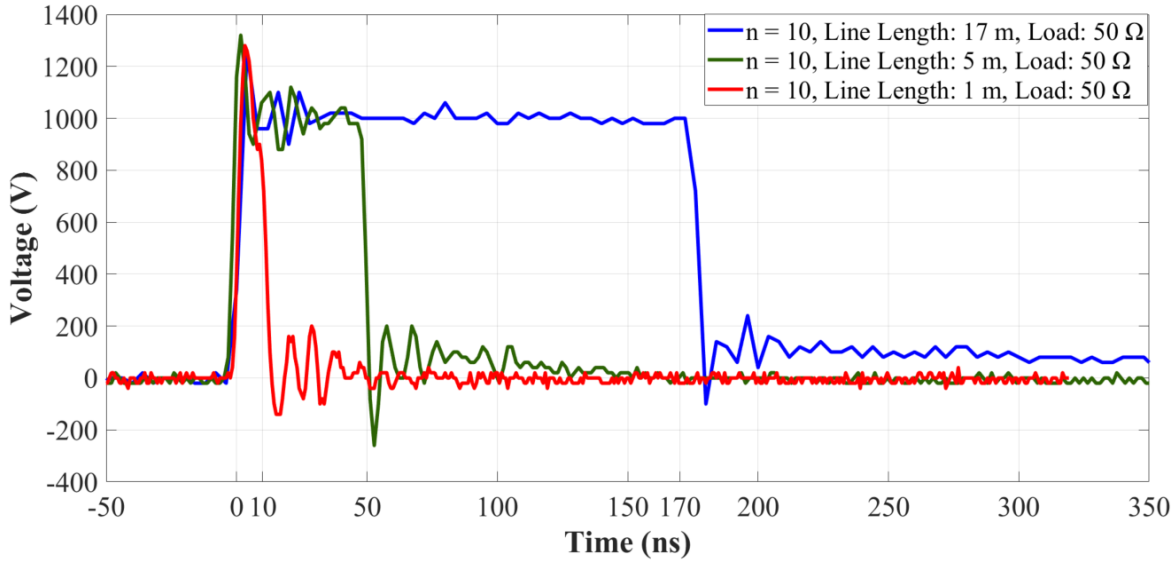


(c)

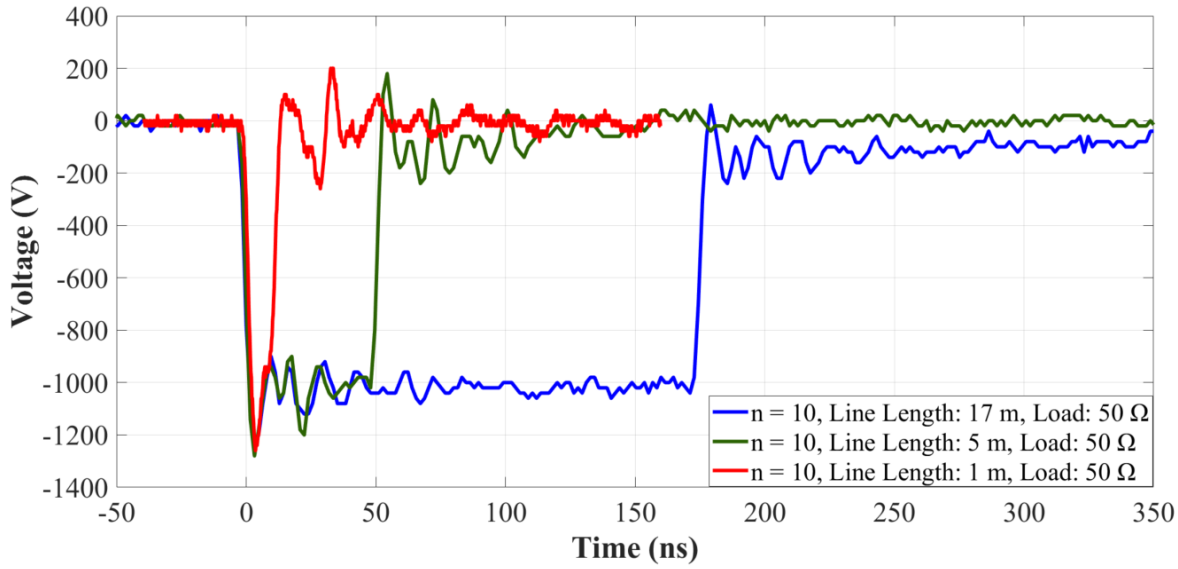
Fig. 5.39. The bench testing circuit showing the stack of ten (n = 10) avalanche transistors to generate pulsed electric fields (a) The modular design of the avalanche switch methodology (b) with a load located to generate a positive nsPEF (c) with a load located to generate a negative nsPEF.

Fig. 5.40 demonstrates that the placement of the load within the circuit that forms as part of the high current loop two determines the pulse polarity of the nsPEF. Fig. 5.40(a) shows the measured nsPEFs across the load (Z_L) in the circuit shown in Fig. 5.37. Fig. 5.40(b) shows the measured nsPEFs across the load (Z_L) in the circuit shown in Fig. 5.38. Comparing the nsPEFs shown in Fig. 5.40, it can be seen that the pulses have identical characteristics except for the polarities of the pulses generated. It is seen that the nsPEFs in Fig. 5.40(b) is the mirror image of nsPEF in Fig. 4.43(a). This is created solely by changing the location of the load within the second current loop. In conclusion, it has been

demonstrated that the placement of the load within the circuit current loop two only affects the polarity of the nsPEF.



(a)



(b)

Fig. 5.40. Measured pulsed electric fields across a 50 Ω load with a stack of ten transistors with a 1 m, 5 m and 17 m charged lines and the 50 Ω load located to generate a (a) positive (Fig. 5.37) or (b) negative polarity pulses (Fig. 5.38)

5.6.6. Simultaneous Generation of Positive and Negative Going Pulses.

The current loops within the design illustrated in Fig. 5.37 can be further manipulated to create a nsPEF system that can produce positive and negative polarity pulses simultaneously. The operation of this circuit is identical to the unipolar designs for generating a negative or a positive polarity nsPEFs. This section describes the generation of a pulse between negative and positive voltages so that the pulse may be split into positive and negative going parts relative to earth. None of the voltage steps is larger than the step available with the normal pulse.

The basic topology for this operation is shown in Fig. 5.41(a). It consists of a switch (S), which is the stack of avalanche transistors, a load ($Z_{L\Sigma}$) that has positive and negative going parts relative to the earth (Z_{LPos} and Z_{LNeg}), a charged/transmission line, a charging resistor (R_C) and power supply (V_{CC}) that does not necessarily need an earth/ground to work. The earth can be placed anywhere within the circuit, but in this design, the earth placement is shown in Fig. 5.41(b). The earth has been added in the middle of the load in Fig. 5.41(a), with positive (Z_{LPos}) and negative (Z_{LNeg}) going parts relative to the earth of the power supply (V_{CC}). This essentially splits the load impedance ($Z_{L\Sigma}$) into two load impedances that are labelled as Z_{LPos} and Z_{LNeg} for the simultaneous generation of positive and negative polarity nsPEFs across Z_{LPos} and Z_{LNeg} respectively.

The load $Z_{L\Sigma}$ in Fig. 5.41(a) is the sum of the loads Z_{LPos} and Z_{LNeg} ($Z_{L\Sigma} = Z_{LPos} + Z_{LNeg}$). A positive polarity PEFs is observed across load Z_{LPos} that is located between the emitter terminal of the lowest stacked transistor (Q_1) and the ground plane. Z_{LPos} is the positive going part relative to earth. A negative polarity PEFs is observed across load Z_{LNeg} that is located between the outer conductor of the transmission line and the ground. Z_{LNeg} is the negative going part relative to earth.

The three potential differences within the circuit can be identified as V_{LPos}, V_{LNeg} and $V_{L\Sigma}$ ($V_{L\Sigma} = V_{LPos} + V_{LNeg}$). This results in three possible nsPEFs that can be obtained from this topology simultaneously. A positive nsPEF with an amplitude of V_{LPos} is observed across the load Z_{LPos} (positive going part relative to earth). A negative nsPEF with an amplitude of V_{LNeg} is observed across the load Z_{LNeg} (negative going part relative to earth). A nsPEF with an amplitude of $V_{L\Sigma}$ is observed across the total load of the system ($Z_{L\Sigma}$) between the lowest stacked transistor (Q_1) emitter terminal and the outer conductor of the transmission line. The potential differences within the circuit for the three nsPEF to be observed across the loads ($Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg}) as described are shown in Fig. 5.42. Therefore if $Z_{LPos} = Z_{LNeg}$ then $V_{LPos} = V_{LNeg} = V_L$ and $V_{L\Sigma} = V_{LPos} - -V_{LNeg} = 2V_L$.

Equation (5.6) can be adapted to calculate the amplitude of nsPEF observed across the three potential differences across the whole load, the positive and negative parts within the circuit that are $V_{L\Sigma}$, V_{LPos}, and V_{LNeg} and as shown in Fig. 5.42.

$$V_{L\Sigma} = \frac{Z_{L\Sigma}}{Z_{L\Sigma} + Z_0} V_{CC} = V_{LPos} + V_{LNeg} \tag{5.29}$$

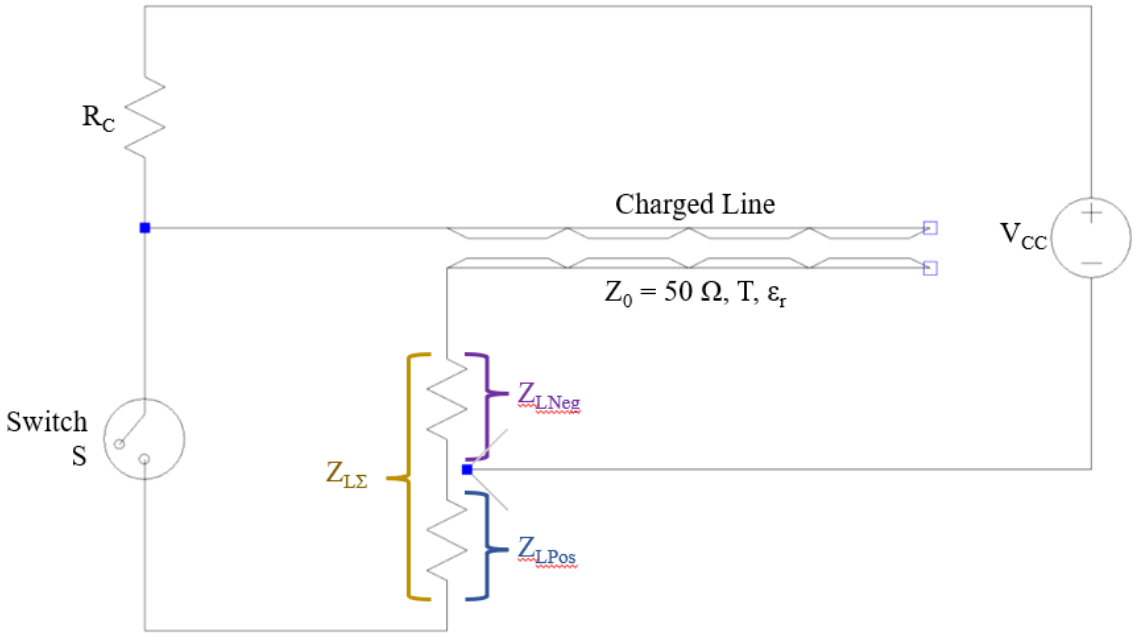
$$V_{LPos} = \frac{Z_{LPos}}{Z_{LPos} + Z_{LNeg}} V_{L\Sigma} = \frac{Z_{LPos}}{Z_{LPos} + Z_{LNeg} + Z_0} V_{CC} = \frac{Z_{LPos}}{Z_{L\Sigma} + Z_0} V_{CC} \tag{5.30}$$

$$V_{LNeg} = \frac{Z_{LNeg}}{Z_{LPos} + Z_{LNeg}} V_{L\Sigma} = \frac{Z_{LNeg}}{Z_{LPos} + Z_{LNeg} + Z_0} V_{CC} = \frac{Z_{LNeg}}{Z_{L\Sigma} + Z_0} V_{CC} \tag{5.31}$$

The total load impedance of the circuit ($Z_{L\Sigma}$) is the sum of the positive load (Z_{LPos}) and negative load (Z_{LNeg}), $Z_{L\Sigma} = Z_{LPos} + Z_{LNeg}$. The reflection coefficient (Γ) in equation (5.7) can be rewritten as (5.32) for this system for the generation of positive and negative polarity nsPEFs simultaneously.

$$\Gamma = \frac{Z_{L\Sigma} - Z_0}{Z_{L\Sigma} + Z_0} = \frac{(Z_{LPos} + Z_{LNeg}) - Z_0}{(Z_{LPos} + Z_{LNeg}) + Z_0} \tag{5.32}$$

(a)



(b)

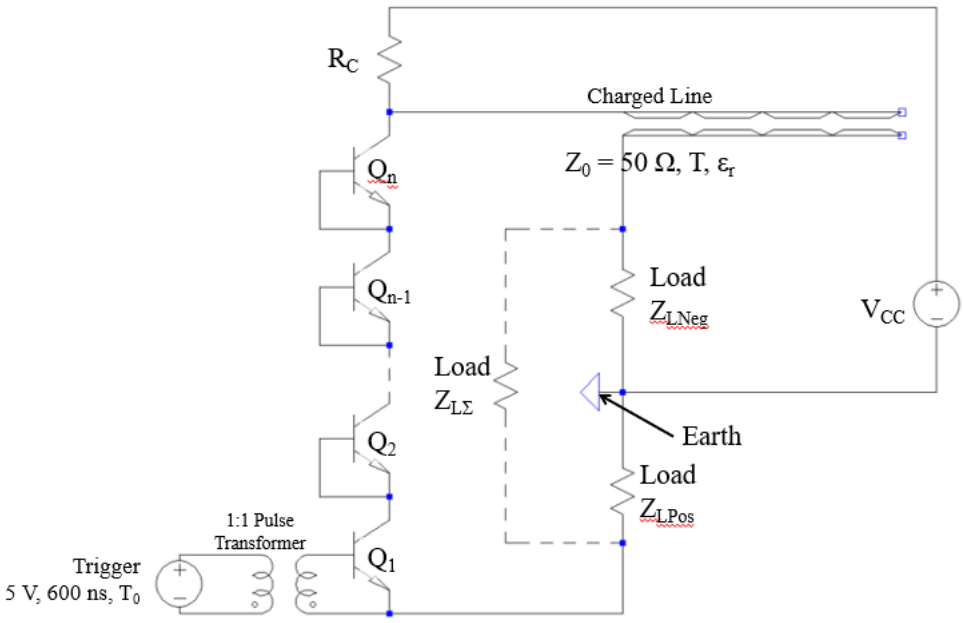


Fig. 5.41. Circuit design for the simultaneous generation of nsPEF of positive and negative polarity pulse (a) basic topology as a switch and a potentiometer load ($Z_{L\Sigma}$) that made of a postie and negative going parts (Z_{LPos} and Z_{LNeg}) and no earth/ground plane (b) with three loads ($Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg}) and an earth/ ground.

Essentially $Z_{L\Sigma}$ and $V_{L\Sigma}$ are identical to Z_L and V_L seen in the unipolar pulse circuits generated previously. Considering equations (5.29) to (5.32), three nsPEFs could be outputted from this circuit design. This depends on the potential difference taken across the system. For the generation of nsPEFs with zero reflection, the total load impedance ($Z_{L\Sigma}$) across the system should equal the characteristic impedance of the charged line (Z_0). If $Z_{L\Sigma} = Z_0$ then $\Gamma = \frac{Z_{L\Sigma}-Z_0}{Z_{L\Sigma}+Z_0} == \frac{Z_0-Z_0}{Z_0+Z_0} = \frac{0}{2Z_0} = 0$. This would result in the amplitude of the nsPEFs across the load ($Z_{L\Sigma}$) being half the voltage level the line is charged to (V_{CC}). If $Z_{L\Sigma} = Z_0$ then $V_{L\Sigma} = \frac{Z_{L\Sigma}}{Z_{L\Sigma}+Z_0}V_{CC} = \frac{Z_0}{Z_0+Z_0}V_{CC} = \frac{V_{CC}}{2}$. The operation and characters of the nsPEFs measured across the load $Z_{L\Sigma}$, between the emitter terminal of Q_1 and the outer conductor of the charged line, is identical to the generation of nsPEF with the circuit shown in Fig. 5.27.

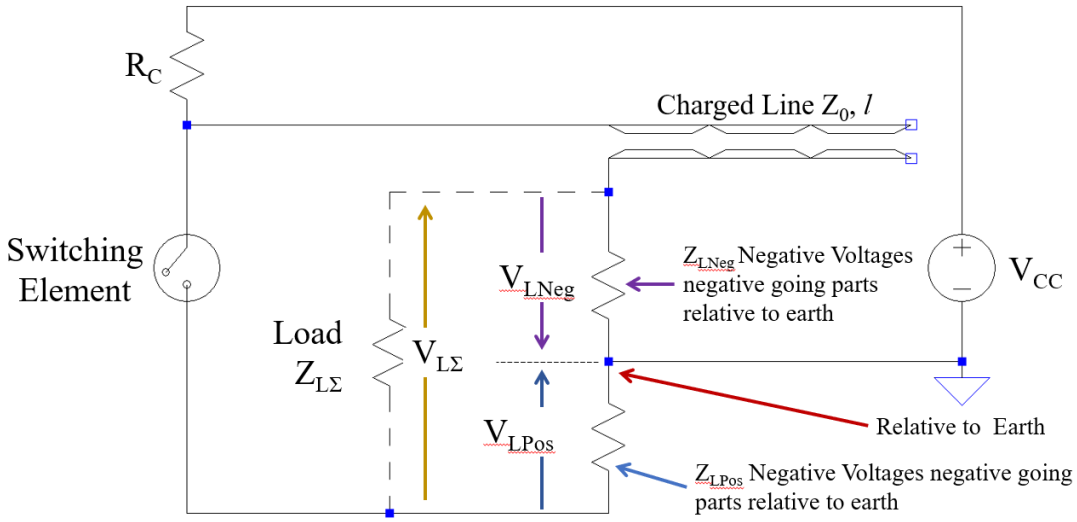


Fig. 5.42. The potential differences V_{LPos}, V_{LNeg} and $V_{L\Sigma}$ across the loads Z_{LPos}, Z_{LNeg} and $Z_{L\Sigma}$.

If the load impedance of Z_{LPos} and Z_{LNeg} are identical ($Z_{LPos} = Z_{LNeg}$), and the total load ($Z_{L\Sigma}$) matches the characteristic impedance of the charged line (Z_0), i.e., $Z_{L\Sigma} = Z_0$, the reflection coefficient (Γ) of the circuit will be 0. The amplitude of the nsPEFs across Z_{LPos} and Z_{LNeg} will be identical and is calculated to be a quarter of the voltage level the line is charged to (V_{CC}) or half the amplitude of the nsPEF across $Z_{L\Sigma}$.

If $Z_{L\Sigma} = Z_0$ and $Z_{LPos} = Z_{LNeg} = \frac{Z_{L\Sigma}}{2} = \frac{Z_0}{2}$. Therefore $V_{L\Sigma} = \frac{Z_{L\Sigma}}{Z_{L\Sigma}+Z_0}V_{CC} = \frac{V_{CC}}{2}$, $V_{LPos} = \frac{Z_{LPos}}{Z_{L\Sigma}+Z_0}V_{CC} = \frac{\frac{Z_0}{2}}{Z_0+Z_0}V_{CC} = \frac{V_{CC}}{4}$, and $V_{LNeg} = \frac{Z_{LNeg}}{Z_{L\Sigma}+Z_0}V_{CC} = \frac{\frac{Z_0}{2}}{Z_0+Z_0}V_{CC} = \frac{V_{CC}}{4}$. This reinforces that the amplitude of the nsPEFs across $Z_{L\Sigma}$ ($V_{L\Sigma}$) is the sum of the amplitude of the nsPEFs across both loads Z_{LPos} and Z_{LNeg}. $V_{L\Sigma} = V_{LPos} + V_{LNeg} = \frac{V_{CC}}{4} + \frac{V_{CC}}{4} = \frac{V_{CC}}{2}$.

The difference between the amplitude of V_{LPos} and V_{LNeg} is dependent on the impedance ratio between Z_{LPos} and Z_{LNeg}. The relationship between these two load impedances (Z_{LPos} and Z_{LNeg}) behaves

as a potential divider or two halves of a potentiometer across the total load impedances ($V_{L\Sigma}$). This is illustrated in Fig. 5.43.

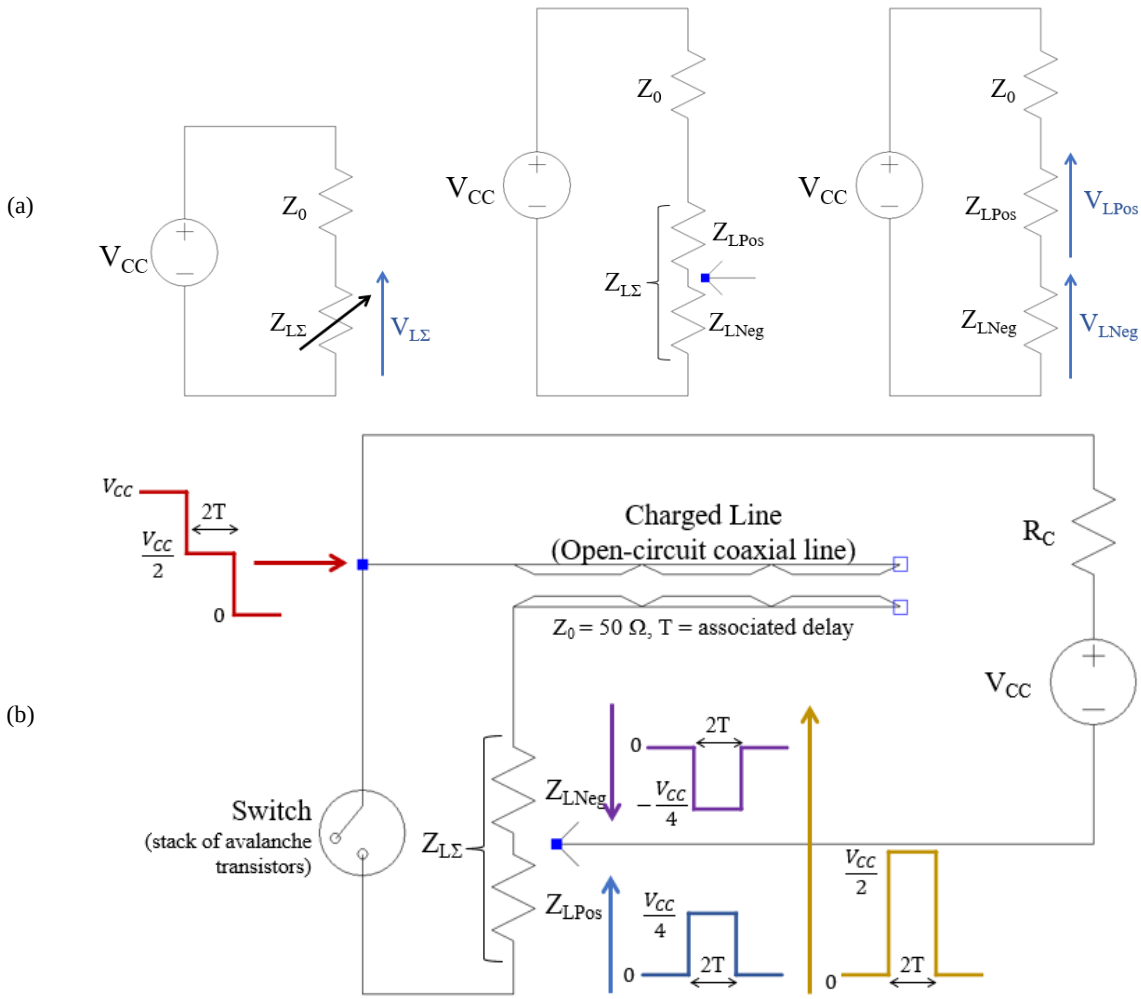


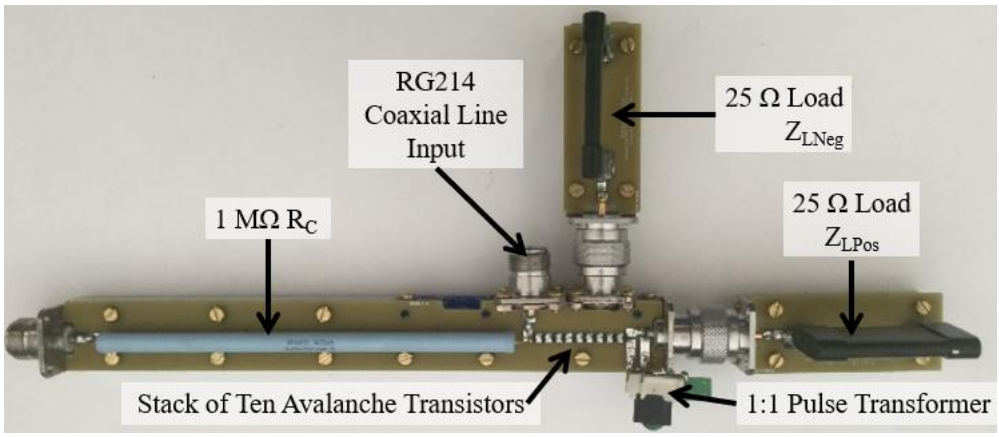
Fig. 5.43. Equivalent circuit of the topology of generating a positive and negative polarity pulsed electric fields as a (a) potential divider with a transmission line characteristic impedance (Z_0), the total load impedance, ($Z_{L\Sigma}$) and the loads Z_{LPos} and Z_{LNeg}. (b) example when $Z_{L\Sigma} = Z_0$ and $Z_{LPos} = Z_{LNeg} = \frac{Z_{L\Sigma}}{2}$

Fig. 5.44. shows the developed bench test circuit for the fast nsPEF electroporation system with a board mount power supply unit (the FS40) and capacitor bank for the charging of the charged line for the simultaneous generation of a positive and negative polarity nsPEFs across two loads Z_{LPos} and Z_{LNeg}. The stack of ten avalanche transistors operates as the fast-switching element that can produce nsPEFs in excess of 1 kV across the total load ($Z_{L\Sigma}$, between the emitter terminal of Q_1 and the outer conductor of the charged line) or the simultaneous generation of a positive and negative nsPEF across loads Z_{LPos} and Z_{LNeg} respectively with an amplitude in excess of 500 V in amplitude.

Fig. 5.45 shows the three nsPEFs that can be generated simultaneously from the circuit in Fig. 5.42. These three nsPEFs are taken from specific potential differences within the current loop or potential difference/probing location within the circuit, as shown in Fig. 5.43. This figure shows the measured nsPEFs generated across the loads $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} with a 50 Ω RG214 transmission line

of 17 m, 5 m and 1 m in length. The impedances of loads Z_{LPos} and Z_{LNeg} were 25 Ω and therefore the impedance of $Z_{L\Sigma}$ was 50 Ω ($Z_{L\Sigma} = Z_{LPos} + Z_{LNeg} = 25\ \Omega + 25\ \Omega$).

(a)



(b)

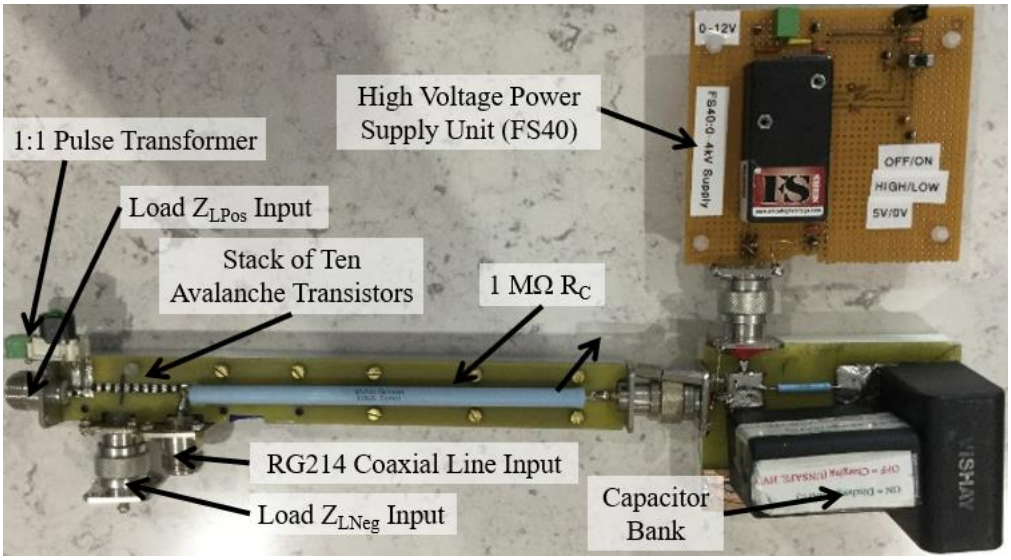


Fig. 5.44. The bench testing circuit of the fast electroporation system circuit (a) Switching circuit with two 25 Ω loads Z_{LPos} and Z_{LNeg} (b) Switching circuit with the high voltage power supply unit (FS40) and capacitor bank printed circuit board.

Fig. 5.45 validates the theory shown in Fig. 5.43(b) from equations (5.29) to (5.32) as the three nsPEFs observed across $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} have identical timing characteristics (pulse widths and transition times). This is because the charged line length determines the pulse width and the stack avalanche transistors operating as a switch determine the transition times.

Secondly, there is a minimal reflection of the three incident pulses measured across $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} as the impedance of $Z_{L\Sigma}$ and the characteristic impedance of the transmission line (Z_0) are the same, thus the reflection coefficient of the circuit/system is zero ($\Gamma = 0$). i.e., $Z_0 = Z_{L\Sigma} = Z_{LPos} + Z_{LNeg}$, $50\ \Omega = 50\ \Omega = 25\ \Omega + 25\ \Omega$.

(a)

(b)

(c)

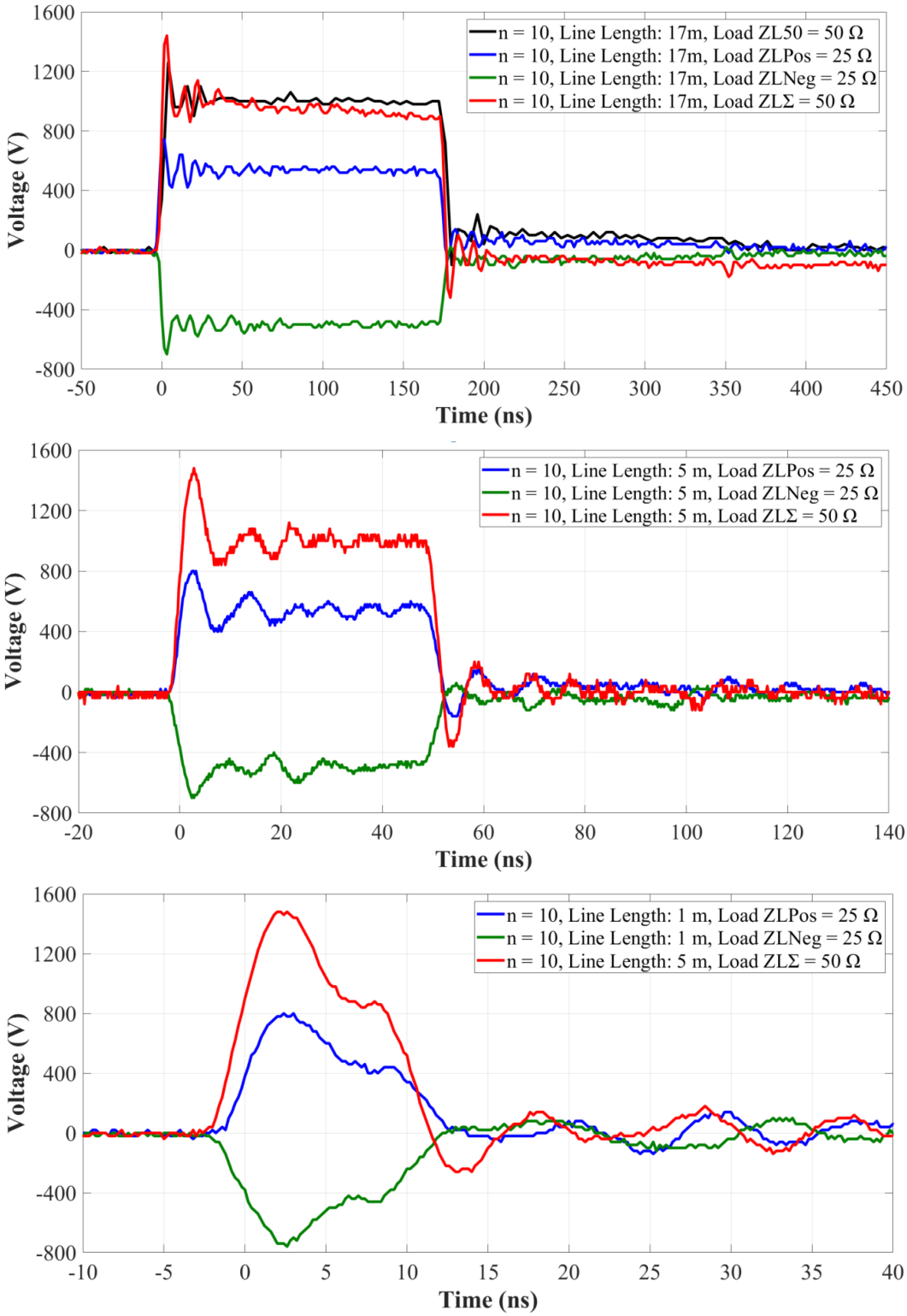


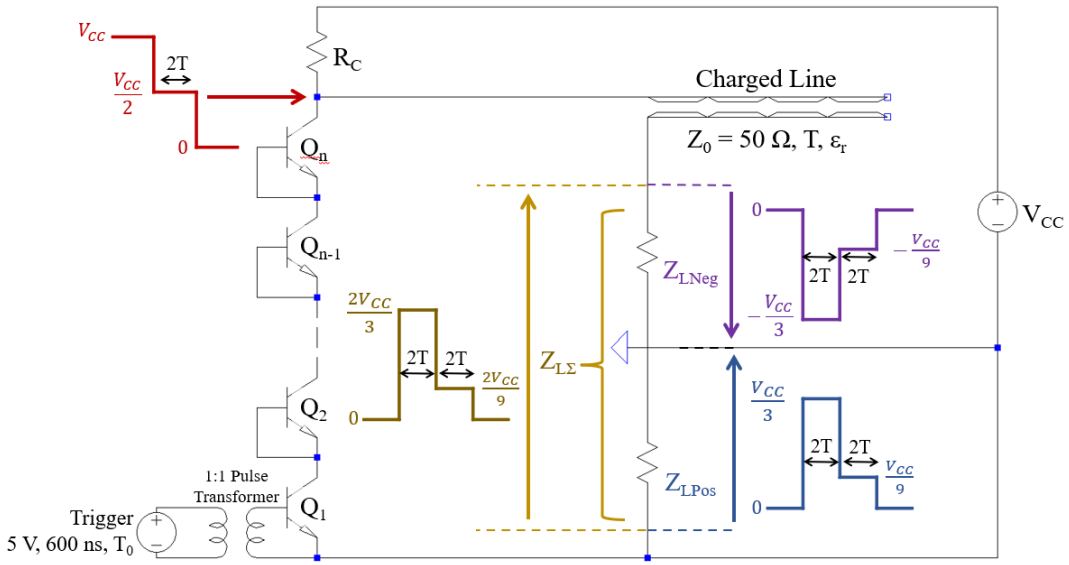
Fig. 5.45. Measured pulsed electric fields across the three different potential difference within the circuit shown in Fig. 5.42. With load values of $Z_{L\Sigma}$ = 50 Ω (red), Z_{LPos} = 25 Ω (blue), and Z_{LNeg} = 25 Ω (green) overlayed with the measured nsPEF across a 50 Ω load in circuit shown in Fig. 5.27 (black) with a stack of ten (n =10) avalanche transistors and a 50 Ω transmission line of (a) 17 m, (b) 5 m and (c) 1 m in length.

Finally, Fig. 5.45(a) shows that the nsPEF measured across $V_{L\Sigma}$ (between the emitter terminal of Q_1 and the outer conductor of the transmission line) in Fig. 5.42 is identical to the nsPEF measured

across a single load Z_L of 50 Ω, implemented between the emitter terminal of Q_1 and the ground, to generate a single positive polarity nsPEF across the load, as seen in Fig. 5.27. Additionally, the amplitude across Z_{LPos} and Z_{LNeg} are identical but of opposite polarity, and the potential difference of the circuit ($V_{L\Sigma}$) or amplitude across $Z_{L\Sigma}$ is equivalent to $V_{LPos} - - V_{LNeg}$ ($V_{LPos} + V_{LNeg}$), or twice the amplitude of the V_{LPos} and V_{LNeg}.

Fig. 5.46 compares shows the measured nsPEFs generated across the loads $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} with a 50 Ω RG214 transmission line 17 m in length. The impedances of loads Z_{LPos} and Z_{LNeg} in this figure were 50 Ω and the impedance of $Z_{L\Sigma}$ was 100 Ω ($Z_{L\Sigma} = Z_{LPos} + Z_{LNeg} = 50\ \Omega + 50\ \Omega$). The timing characteristics of the nsPEFs in Fig. 5.46, the duration and transition times of the nsPEF and their amplitudes across both Z_{LPos} and Z_{LNeg} are identical.

(a)



(b)

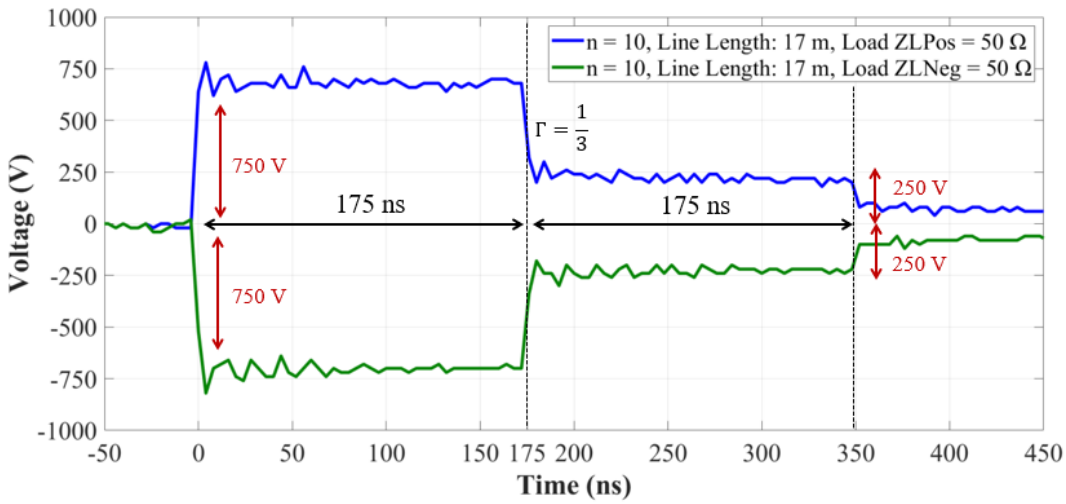


Fig. 5.46. Three load values of $Z_{L\Sigma}$ = 100 Ω (red), Z_{LPos} = 50 Ω and Z_{LNeg} = 50 Ω with a stack of ten (n =10) avalanche transistors and a 50 Ω transmission line of 17 m (a) the circuit and theoretical pulsed electric field waveforms across the loads (b) measured pulsed electric field across Z_{LPos} (blue) and Z_{LNeg} (green) in practice

Comparing the nsPEF shown in Fig. 5.46 with Fig. 5.45 there is a reflection associated with the nsPEFs in Fig. 5.46. This reflection is seen as the reflection coefficient (Γ) in this circuit is $\frac{1}{3}$, because the impedance of $Z_{L\Sigma}$ is 100 Ω and the characteristic impedance of the transmission line (Z_0) is 50 Ω. $\Gamma = \frac{Z_{L\Sigma}-Z_0}{Z_{L\Sigma}+Z_0} = \frac{100-50}{50+50} = \frac{50}{150} = \frac{1}{3}$.

The amplitude of the nsPEF measured across both Z_{LPos} and Z_{LNeg} are higher in Fig. 5.46 than in Fig. 5.45 because their load impedance value is higher (50 Ω > 25 Ω) within the same circuit (identical 50 Ω coaxial transmission line, charged voltage (V_{CC} = 2000 V) and the number of stacked transistors). For the nsPEF measured in Fig. 5.45 the value of Z_{LPos} and Z_{LNeg} is 25 Ω and the value for $Z_{L\Sigma}$ is 50 Ω and their associated nsPEFs amplitudes were 500 V across Z_{LPos} and Z_{LNeg}, and 1000 V across $Z_{L\Sigma}$. For the nsPEF measured in Fig. 5.45 the value of Z_{LPos} and Z_{LNeg} is 50 Ω and the value for $Z_{L\Sigma}$ is 100 Ω and their associated nsPEFs amplitudes were 750 V across Z_{LPos} and Z_{LNeg}, and 1500 V across $V_{L\Sigma}$.

In conclusion, the nsPEF electroporation system developed is capable of generating three nsPEFs simultaneously. These three nsPEFs are taken from specific potential differences within the current loop of the topology as shown in Fig. 5.42. The identified potential differences or 'loads' within the circuit are $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg}. The load $Z_{L\Sigma}$ can be thought of as a load or a potentiometer between the emitter terminal of Q_1 and the outer conductor of the transmission line that is composed of a positive and negative parts that are Z_{LPos} and Z_{LNeg}. Its impedance is the combined impedance of both Z_{LPos} and Z_{LNeg} i.e., $Z_{L\Sigma} = Z_{LPos} + Z_{LNeg}$. Z_{LPos} is the impedance/load between the emitter terminal of Q_1 and the ground of the system and Z_{LNeg} is the impedance/load between the outer conductor of the transmission line and the ground of the system.

The timing characteristics of the nsPEF across $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} are identical. The pulse width is determined by the transmission line length and transition times by the switching characters of the stack of avalanche transistors. The reflection coefficient and the amplitude of the nsPEFs that are measured across $Z_{L\Sigma}$, Z_{LPos} and Z_{LNeg} of the system are dependent on the value of the characteristic impedance of the transmission line (Z_0) and $Z_{L\Sigma}$. These are highlighted in Table 5.8.

Future work is required to progress this design for the system to apply a burst of positive polarity nsPEFs followed by a negative polarity nsPEFs, with a specified predetermined intermission between the positive and negative polarity pulses across a load, bulk tissue or cuvette of cell line population. These would be defined as bipolar pulses. A possible solution to generate bipolar pulses is to implement a transmission line of specific time delay that determines the intermission time between the application of a positive and negative polarity PEF as both pulses are currently generated simultaneously in this current topology.

Table 5.8. The principle of simultaneous generating three nanosecond pulsed electric fields

	$\boldsymbol{Z_{L\Sigma}}$	Reflection Coefficient of the circuit, Γ	Amplitude of nsPEF across $\boldsymbol{Z_{LPos}}$ (V)	Amplitude of nsPEF across $\boldsymbol{Z_{LPNeg}}$ (V)	Amplitude of nsPEF across $\boldsymbol{Z_{L\Sigma}}$ (V)
Equation	$Z_{LPos} + Z_{LNeg}$	$\Gamma = \frac{Z_{L\Sigma} - Z_0}{Z_{L\Sigma} + Z_0}$	$\frac{Z_{LNeg}}{Z_{L\Sigma} + Z_0} V_{CC}$	$\frac{Z_{LNeg}}{Z_{L\Sigma} + Z_0} V_{CC}$	$\frac{Z_{L\Sigma}}{Z_{L\Sigma} + Z_0} V_{CC} = V_{LPos} + V_{LNeg}$
$\boldsymbol{Z_{LPos} = 25\,\Omega}$, $\boldsymbol{Z_{LNeg} = 25\,\Omega}$	$25\,\Omega + 25\,\Omega = 50\,\Omega$,	$\frac{50-50}{50+50} = 0$	$\frac{25}{50+50} V_{CC} = \frac{V_{CC}}{4}$	$\frac{25}{50+50} V_{CC} = \frac{V_{CC}}{4}$	$\frac{50}{50+50} V_{CC} = \frac{V_{CC}}{2}$
$\boldsymbol{Z_{LPos} = 50\,\Omega}$, $\boldsymbol{Z_{LNeg} = 50\,\Omega}$	$50\,\Omega + 50\,\Omega = 100\,\Omega$,	$\frac{100-50}{50+50} = \frac{1}{3}$	$\frac{50}{100+50} V_{CC} = \frac{V_{CC}}{3}$	$\frac{50}{100+50} V_{CC} = \frac{V_{CC}}{3}$	$\frac{100}{100+50} V_{CC} = \frac{2V_{CC}}{3}$
$\boldsymbol{Z_{LPos} = 12.5\Omega}$ $\boldsymbol{Z_{LNeg} = 12.5\Omega}$	$12.5\,\Omega + 12.5\,\Omega = 25\,\Omega$,	$\frac{25-50}{25+50} = -\frac{1}{3}$	$\frac{12.5}{25+50} V_{CC} = \frac{V_{CC}}{6}$	$\frac{12.5}{25+50} V_{CC} = \frac{V_{CC}}{6}$	$\frac{50}{50+50} V_{CC} = \frac{V_{CC}}{3}$

5.7. The Fast Electroporation System

This final architecture comprises the slow charging of an RG214 coaxial cable, through a 1 MΩ resistor (R_C) that is rapidly discharging through a stack of ten FMMT417 avalanche transistors operating as a fast-switching element. This final constructed fast nsPEF electroporation system meets the agreed set of requirements given by the SUMCASTEC consortium outlined in section 5.1. The unit can generate a specified number of nsPEFs of duration between 10 ns and 100 ns, with a range of repetition frequency from 1 Hz to 50 Hz, with amplitudes in excess of 1kV, across a 50 Ω load. It was demonstrated from bench testing that stacking twenty (n = 20) FMMT417 avalanche transistors in series can produce 10ns PEF with amplitudes as high as 2.5 kV

This final system generates symmetrical nsPEFs by charging a 50 Ω RG214 coaxial transmission line, of a specific length, which is an open circuit at its distal end, through a high impedance 1 MΩ, to a specified voltage level (V_{CC}) between the voltage levels nV_{CEO} and nBV_{CES}. The length of the RG214 line determines the pulse width of the nsPEF. An RG214 coaxial line-based generator produces a pulse of approximately 10 ns per 1 m of line length. The charged line is then rapidly discharged through a stack of ten (n =10) FMMT417 avalanche transistors to generate a nsPEF with sub-nanosecond transition times across the load. A nsPEF is generated when a 5 V, 600 ns trigger signal is applied to the lowest stacked transistor base terminal via an isolated 1:1 pulse transformer. This trigger signal dictates when the pulse is generated, the number of pulses and the repetition frequency of the high voltage nsPEFs generated from the fast nsPEF electroporation system.

5.7.1. Avalanche Switching Microstrip Circuit Module

The stacking of ten (n = 10) FMMT417 avalanche transistors was implemented for the implementation of the final fast nsPEF electroporation system. The estimated amplitude of the PEF across the load (V_L) is given by:

$$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC} \approx \left(\frac{Z_L}{Z_L + Z_0}\right) nBV_{CES}$$

For the stack of ten avalanche transistors to operate as a controlled switch the voltage across the charged line must be between the values of $nV_{CEO} < V_{CC} > nB_{VCES}$. For a stack of ten (n = 10) FMMT417 avalanche transistors to operate as a controlled switch must be between the values of 1000 V < V_{CC} > 3200 V. The maximum amplitude of nsPEF that can be produced across a 50 Ω load (V_{LMax}) is given by:

$$V_{LMax} = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC} = \left(\frac{50}{50 + 50}\right) 3200 = \frac{3200}{2} = 1600\ V$$

The RG214 coaxial cable used for the delay line has a high operating voltage of 4 kV and attenuation of 0.245 dB/m (24.5 dB/100m) at 1 GHz) [33]. The RG214 cable uses Polyethylene (PE) as the dielectric with a dielectric constant of 2.25. This conveniently provides an approximate pulse duration of 10 ns per meter. Cutting a length of open circuit RG214 cable to generate a nsPEF of specific duration can be found by:

$$\text{pusle width} = 2T = 2\frac{l\sqrt{\varepsilon_r}}{c} = \frac{l\sqrt{2.25}}{3\text{x}10^8}\left(\frac{m}{m/s}\right) \approx l\ 1\text{x}10^{-8}s$$

where l is the length of the line. For a 10 ns pulse, l = 1 m.

The FMMT417 transistor, RG214 coaxial cable and a 1:1 gate pulse transformer are the critical components for the generation of the fast nsPEF electroporation system. Because of the microwave frequency components associated with the transition times of the nsPEFs generated and the importance of impedance matching between the 50 Ω transmission line characteristic impedance (Z_0) and the load (Z_L) the components were mounted on a 50 Ω microstrip line PCB design developed for the avalanche switching circuit module.

The avalanche switching microstrip circuit module is designed with a ground-plane technique with the distance between each stacked FMMT417 component kept as short as possible. SOT23 packages were used to minimise stray inductance.

All the PCB circuit modules for the fast nsPEF electroporation system were fabricated by Euro Circuits [35]. 'FR-4 Improved' dielectric material with a dielectric constant of 4.04 and thickness of

1.55 mm was used to fabricate the circuit [36]-[37]. From the equations given in section 5.4.5.3, a microstrip line of width 3.04 mm was used to produce a 50 Ω line.

Fig. 5.47 illustrates the microstrip PCB design for the avalanche switching module for the fast nsPEF electroporation system. The dimension of the microstrip pads to enable the devices to be connected are designed to minimise the distances between each transistor in the stacked line. These dimensions were selected after studying the FMMT417 datasheet [19], in particular, its SOT23 package outline dimensions and suggested pad layout. The distance between each solder pad is 1.20 mm, which is the outline dimension of the SO23 package body and the distance between the collector, emitter and base terminals. The microstrip line width of 3.04 mm, produced a microstrip line with a characteristic impedance of 50 Ω, which was marginally larger than the FMMT417 SOT23 package width of 3.00 mm (max). These dimensions are illustrated in Fig. 5.47(d).

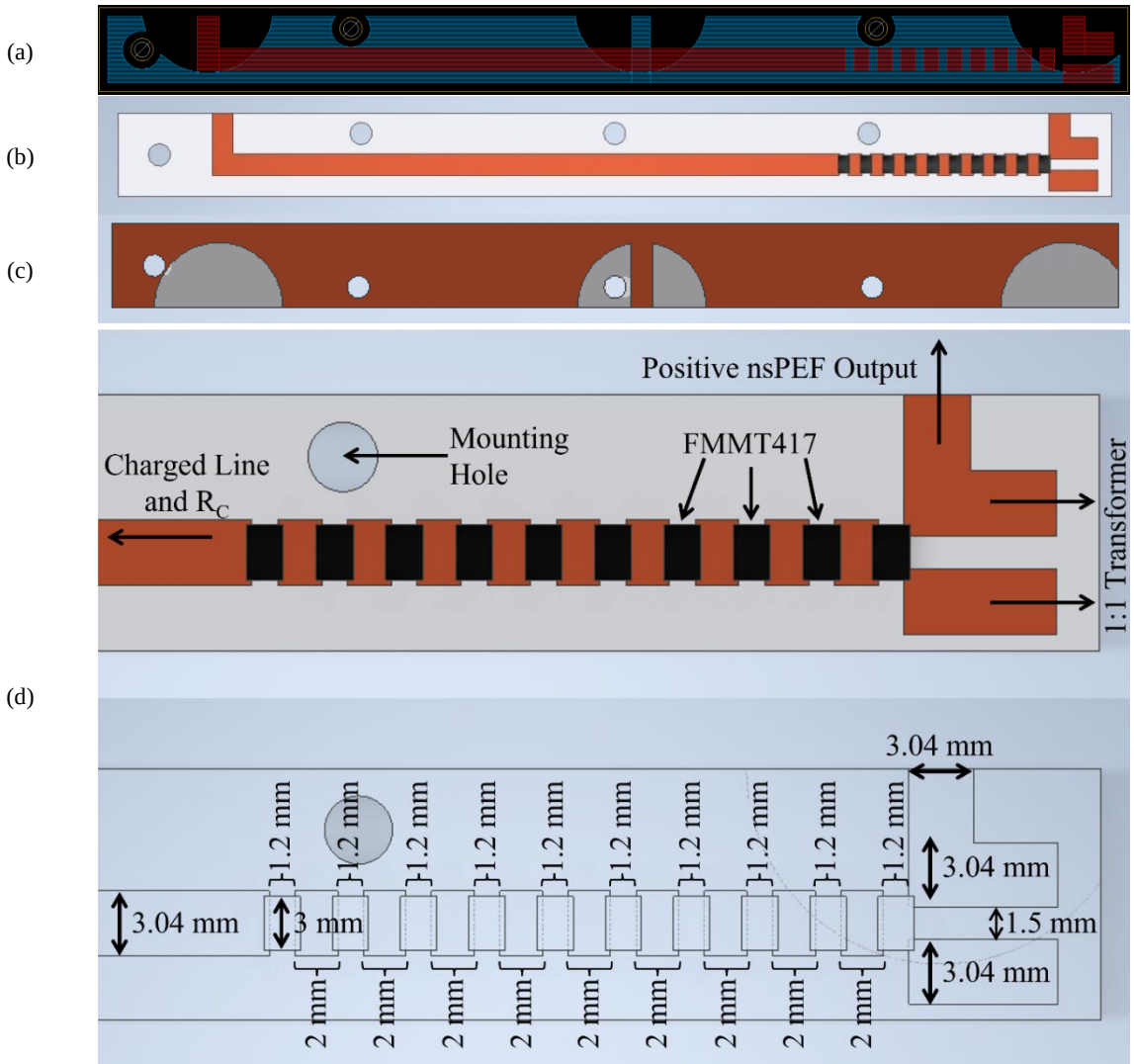


Fig. 5.47. The avalanche switching microstrip layout (a) Eagle printed circuit board software board design - red top layer, blue bottom layer (b) computer aided design model of the top layer of the printed circuit board design populated with the FMMT417s devices (c) computer aided design model of the bottom layer of the printed circuit board (d) labelled computer aided design model and dimensions of the printed circuit board top layer.

For the circuit to be capable of producing a voltage amplitude in excess of 1.5 kV, HN-connectors were used as their operating and breakdown voltage is sufficiently higher than N-connectors (up to 5 kV) [55]-[56]. The left HN-connector port is an input port for the user to connect an RG214 coaxial line of a specific length to the fast nsPEF electroporation system. This provides flexibility for the user to select the desired nsPEF duration.

The two other HN-connector ports (centre and right-hand connectors) are output ports. The middle flange HN-connector in Fig. 5.48 is the output port, where a negative nsPEF is generated and the remaining port is where a positive nsPEF is generated. The outer conductor of the HN-connectors for the charged line input and negative nsPEF output (left and centre ports) are connected and isolated away from the ground plane/chassis of the system.

The inner conductor of the centre HN-connector port, for the generation of a negative nsPEF, and the outer conductor of the right HN-connector port, for the generation of positive nsPEF are connected to the ground plane of the system and the chassis of the module. The inner conductor of the third port is where the positive nsPEF is output and is soldered to the microstrip line connected to the emitter of the lowest stacked transistor, Q_1. This is shown in Fig. 5.48.

Fig. 5.48 illustrates how the avalanche switching microstrip circuits module appears when populated with the relevant HN-connectors, gate drive transformer and stack of FMMT417 transistors.

As seen in Fig. 5.48, the output from the secondary coil of a 1:1 isolated pulse transformer is soldered onto the microstrip line across the lowest stacked transformer (Q_1) base and emitter terminals. The primary coil of the 1:1 gate drive transformer is attached to a two-pin edge connector. This allows for an easy connection to be made to an external pulse generator that can provide the necessary 5 V, 600 ns trigger signal to control the switching circuit and the operation of the fast nsPEF electroporation system.

5.7.2. High Voltage Circuit Module

For the generation of the nsPEFs with amplitudes in excess of 1 kV, the charged line needs to be charged to a voltage level that is in excess of 2,000 V. The maximum voltage the transmission line can be charged to is 3,200 V. If the voltage level exceeds 3,200 V, the voltage drops across each of the ten FMMT417 would exceed their collector-emitter breakdown voltage (BV_{CES}) value of 320 V. If this occurs, the stack transistors will experience a permanent breakdown. For the trigger signal to be effective in manipulating the 'ON'/'OFF' timing of the nsPEFs, the voltage drop across each transistor should not exceed their collector-emitter breakdown voltage value of BV_{CES} and V_{CEO}. Therefore, the maximum and minimum voltage level the transmission lines can be charged to are nBV_{CES} (10 x 320 = 3200 V) and nV_{CEO} (10 x 100 = 1000 V), for the generation of a 10 ns to 300 ns PEFs with a maximum amplitude of 1600 V and a repetition frequency of 50 Hz onto a 50 Ω load.

(a)

(b)

(c)

(d)

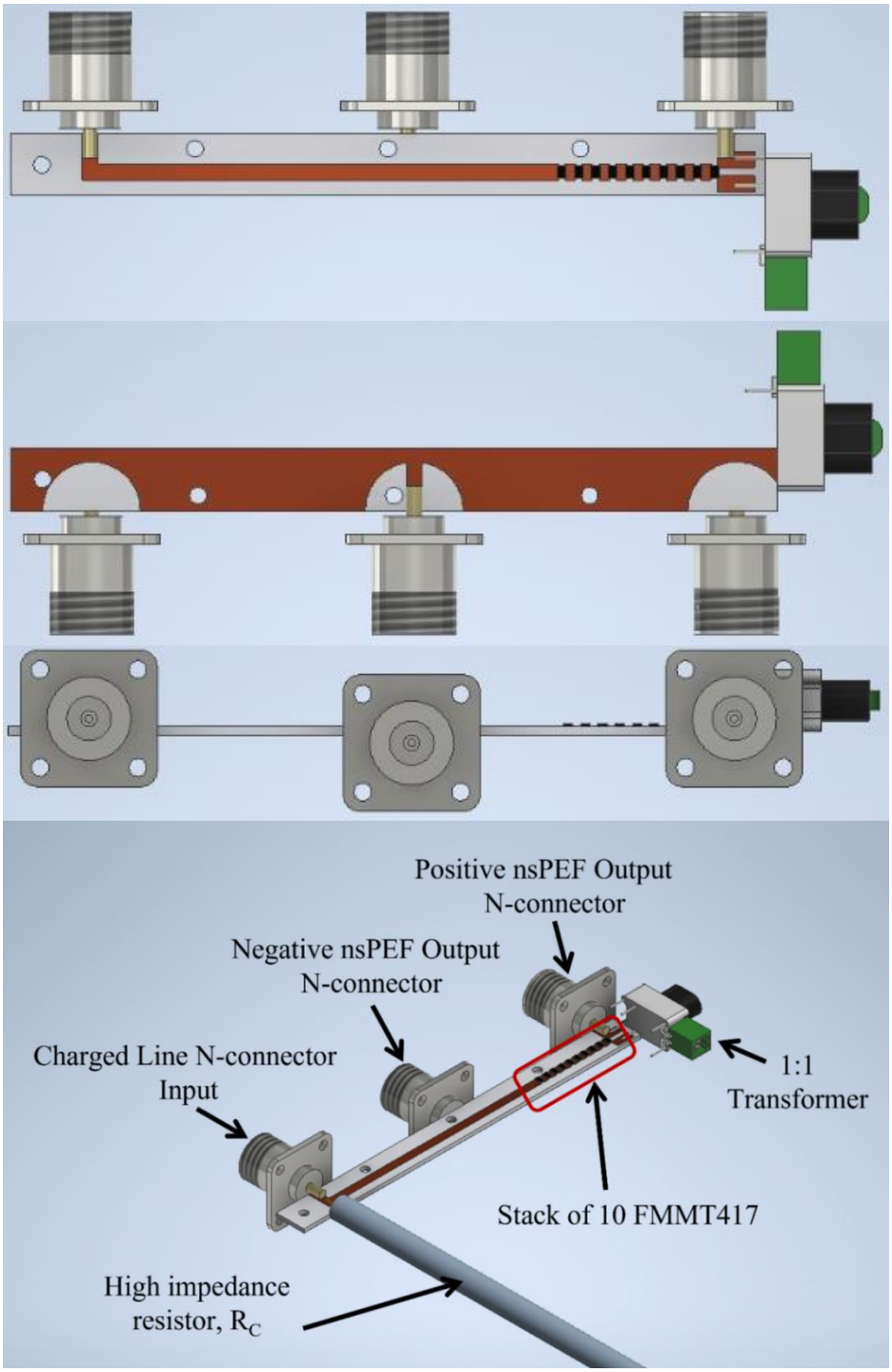


Fig. 5.48. computer aided design model of the avalanche switching microstrip circuit printed circuit board module fully populated (a) top layer view (b) bottom layer view (c) side view (d) Labelled diagram of the populated avalanche switching microstrip circuits.

Table 5.9. shows the power supply requirements necessary to maintain the nsPEFs required for this work. In terms of the dc voltage required for the generation of 1600 V across a 50 Ω load, a power supply of 3200 V, 204 kW and 64 A is required (see equation 5.36). But the nsPEFs are pulsed for a maximum duration of 300 ns and these pulses are generated every 20 ms seconds (50 Hz). Therefore, we can calculate the power supply requirement by taking into account the average time the nsPEFs will

be generated. Looking at these pulse parameters the maximum average time the nsPEFs will be generated each second is 15 µs. This is the maximum pulse width (300 ns) multiplied by the number of pulses per second (50). Therefore, for the generation of 1,600 V amplitude pulses across the 50 Ω load, a power supply of 3,200 V, 3.07 W and 960 µA would suffice.

Table 5.9. High voltage power supply maximum requirements for the fast nsPEF electroporation system

Maximum Power supply parameter		Value	Unit
DC	Voltage, V	3,200	V
	Current, I	64	I
	Power, P	204,800	W
Load impedance, $\boldsymbol{Z_L}$		50	Ω
Pulse width, t		300	ns
Repetition frequency, *f*		50	Hz
maximum average 'ON' time, *t*		15	µs
Average	Voltage, V	3,200	V
	Current, I_{Av}	960	µI
	Power, P_{Av}	3.07	W
Capacitance bank, C		597	nF

$$P_{DC} = VI_{dc} = \frac{V^2}{Z_L} \tag{5.33}$$

$$P_{Av} = P_{dc}ft = VI_{Av} = VI_{dc}ft \tag{5.34}$$

Where V is dc voltage, I_{dc} is dc current, I_{Av} is the average current, P_{dc} is dc power, P_{Av} is the average power, f is repetition frequency, t is the pulse duration and Z_L is the load impedance (50 Ω).

It is required to add a capacitor across the power supply to charge back up to 3200 V in 19.9997 ms (20 ms). If the maximum drop in the voltage across the generation of the 300 ns pulses i.e., 32 V (ΔV) then the capacitance required can be found using equation (5.35). Where the capacitance required to replenish or recharge the power supply is 597 nF.

$$C = \frac{t}{Z_L \ln\left(\frac{V}{V_0}\right)} \tag{5.35}$$

where V_0 (3200 V) is the voltage output from the high voltage power supply unit, V is the voltage after a 1% drop (3168 V, $V_0 - \Delta V$, 3200 V – 32 V), t is the pulse duration and Z_L is the load impedance (Z_0).

$$C = \frac{t}{Z \ln\left(\frac{V}{V_0}\right)} = \frac{300\text{x}10^{-9}}{50 \ln\left(\frac{3168}{3200}\right)} = 596.99\ nF$$

Following a review of various high voltage power supplies, the XP-Power 10 W FS40 isolated proportional dc to high voltage dc converter was identified as the best option (see the datasheet for FS40 in Appendix IV [38]). The output voltage is proportional to the input voltage, from turn-on to maximum output voltage, enabling easy control of the high voltage supply rail. The maximum output voltage is 4 kV, and the maximum current is 2.5 mA. This satisfies the requirement of 960 mA to replenish the charge in the 597 nF capacitor.

The relationship between the low voltage input and the high voltage output associated with the FS40 unit is linear. A 12 V input produces a 4 kV output, and a 6 V input produces a 2 kV output.For the output of the FS40 to be limited to 3.2 kV, the input voltage was limited to 4.2 V.

$$\text{Input } 12\,V = 100\% = 4kV$$

$$\frac{3.2kV}{4kV} = 80\%, \quad \therefore 12\,V * 0.8 = 9.6\,V$$

Additional features of the FS40 PSU include an internal input over-voltage and over-temperature protection and an enable/disable function. The protection circuits are powered by the +5 V logic input voltage terminal. A +5 V (TTL) signal to the control terminal of the device will disable the high voltage output [38].

Two 1 μF capacitors are connected across the FS40 high voltage PSU. The role of this capacitor bank is to maintain a constant dc value by removing the power supply ripple. A high impedance resistor, of value 3.3 MΩ, is placed across each of the 1 μF capacitors. The role of these resistors is to discharge the capacitors when the power supply is turned ‘OFF’ i.e., remove the electric charge stored in the power supply 1 μF capacitors when the PSU is disabled/turned ‘OFF’. This eliminates the possibility of residue charge within the capacitors causing an electric shock.

The two-pin edge connector intends to provide a connection for the input control voltage, 0 V to 9.6 V, to control the isolated output voltage of 0 V to 3.2 kV.

The three-pin edge connector provides the input and output signals to control the FS40. This includes a +5 V logic input to the FS40 for the PSU to operate a 5 V/0 V switch signal to control the PSU ‘OFF’ and ‘ON’ on demand, and a 5 V for ‘OFF’ and a 0 V for ‘ON’ operation. Error output from the FS40 sixth pin can indicate when an over-temperature and/or shutdown error occurs when a high TTL (5 V) signal is present at this terminal.

5.7.3. Construction Build

The completed build of the fast nsPEF electroporation system is shown in Fig. 5.49. HN connectors HN_1, HN_2 and HN_3 are the outputs from the system. HN_1 is the input port for the RG214 coaxial

transmission line of a specific length. HN_2 delivers negative going pulses and HN_3 delivers the positive going pulses.

For the completion of a fast nsPEF electroporation system, the modular design in Fig. 5.49 needs to be housed in a chassis. This will produce a complete fast nsPEF electroporation system to be used for *in-vitro* and *in-vivo* investigations. The final developed fast nsPEF electroporation prototype system is demonstrated in Fig. 5.53.

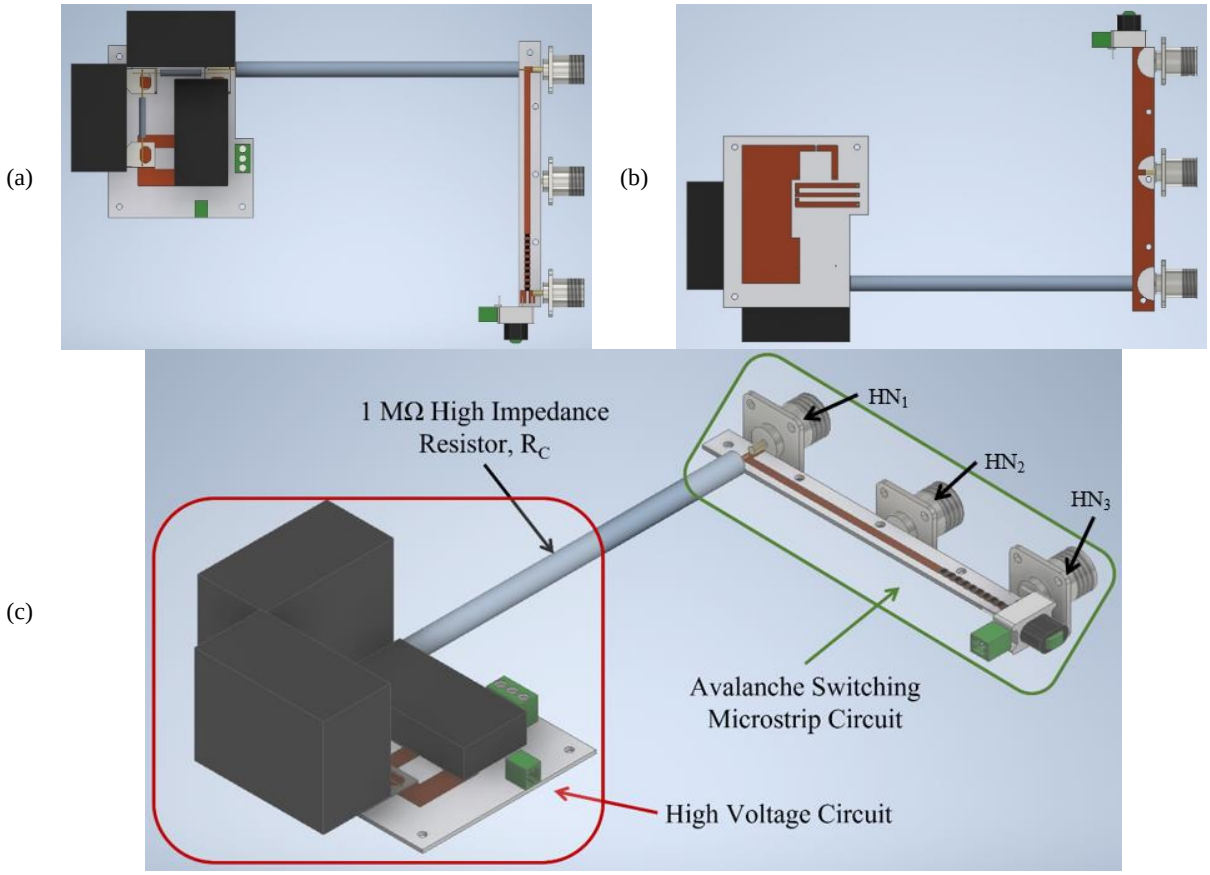


Fig. 5.49. The complete fast electroporation system modular designs printed circuit board computer aided design (a) top view (b) bottom view (c) labelled diagram

Front Panel

The front panel of the fast nsPEF electroporation system consists of three HN-connector ports, the negative and positive nsPEFs output and the charged line input port, as is shown in Fig. 5.50. The outer conductor of both the charged line input and negative nsPEF output ports is connected with a conductive copper plate and isolated from the chassis and the ground plane of the system. This isolation is provided by a 3D-printed plastic structure, thus making the outer conductors of this two HN-connector (HN_1 and HN_2) at a floating potential. The relevance of this floating potential to the rest of the system determines whether a negative nsPEF is generated in a unipolar or simultaneously with a positive polarity pulse format. To protect the user from this floating potential, a 3D insulated housing surrounds the negative nsPEF output and charged line input ports.

Fig. 5.50(b) shows the arrangement of the front panel for the generation of positive nsPEFs from the system in retrospect to the ground plane. In Fig. 5.50(b), a short-circuit compatible HN-connector is placed at the negative nsPEF port (HN_2). This connects the outer conductor of the negative nsPEF output and charged line input to the ground plane of the system.

(a)

(b)

(c)

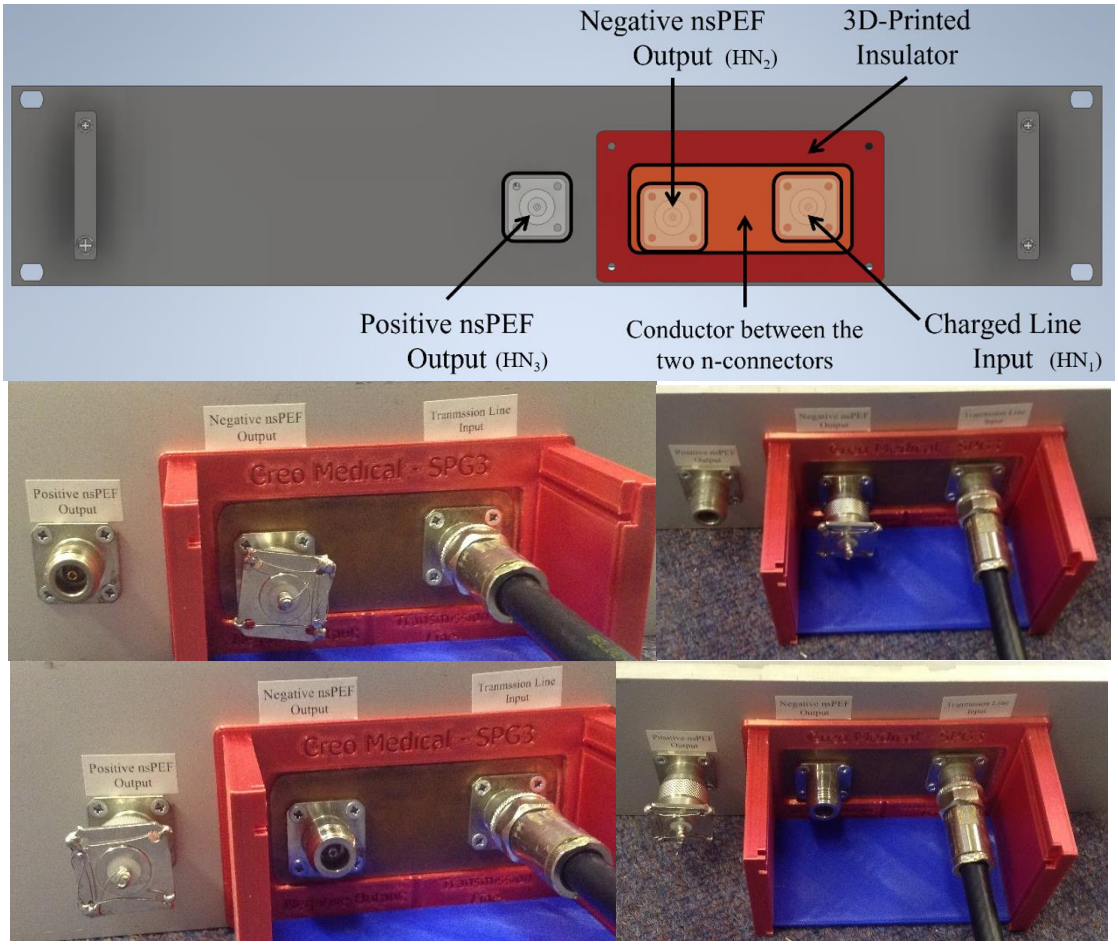


Fig. 5.50. The front panel of the fast electroporation system (a) annotated computer aided design (b) orientation to produce a positive polarity pulsed electric field (c) orientation to produce a negative polarity pulsed electric field

Fig. 5.50(c) shows the arrangement of the front panel for the generation of negative nsPEFs from the system in retrospect to the ground plane. In Fig. 5.50(c), a short-circuit compatible HN-connector is placed at the positive nsPEF port (HN_3). This connects the inner conductor of the positive nsPEF output to the ground plane of the system. Fig. 5.51 shows how each HN-connector on the front panel is connected.

Back Panel

The back panel design of the fast nsPEF electroporation system is shown in Fig. 5.52. The purpose of the system's back panel is to feed the necessary control signals to operate the fast nsPEF electroporation system.

The first pair of red and black banana connectors, on the left-hand side of the back panel in Fig. 5.52, is connected to the 0 to 12 V two-pin edge connectors on the high voltage supply PCB. The input voltage into this port should be limited to 9.6 V. This input voltage controls and selects the high voltage dc output from the FS40 power supply/high voltage supply PCB within the system.

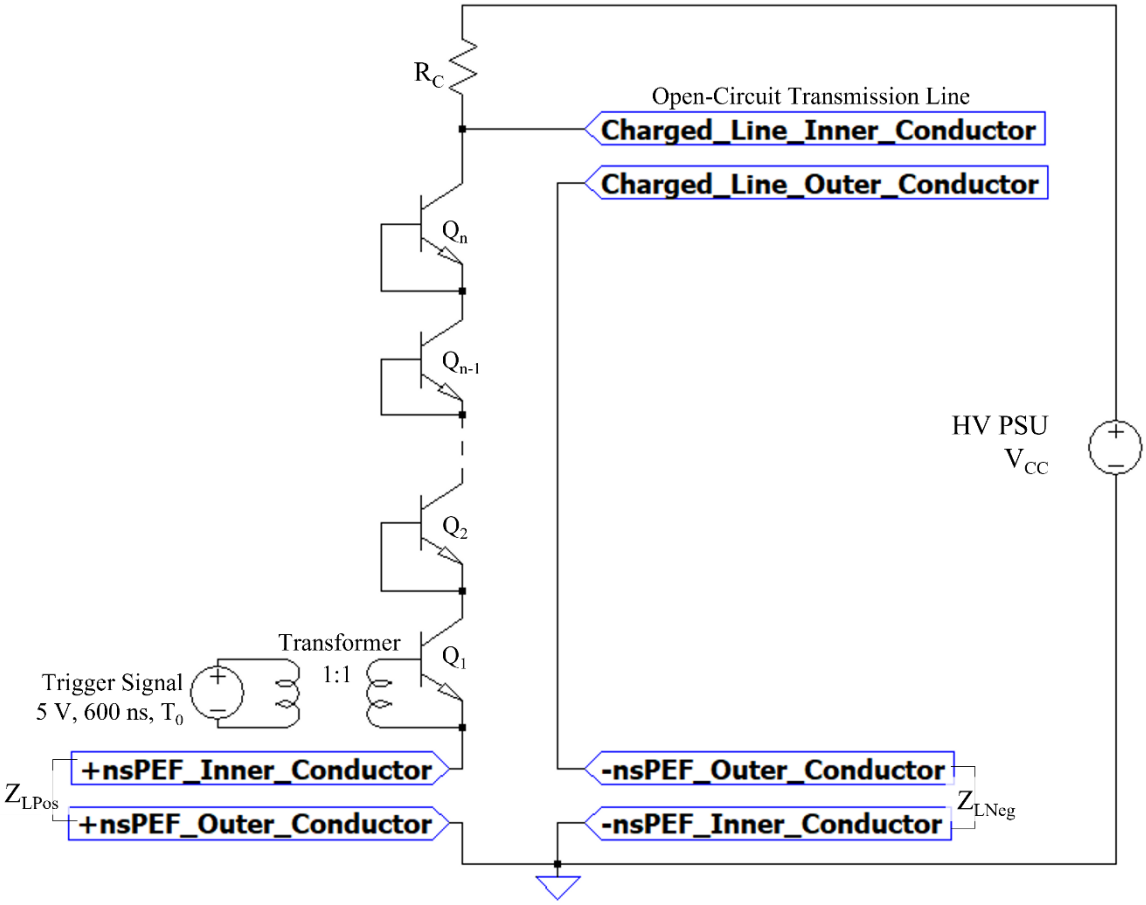


Fig. 5.51. Circuit for the fast electroporation system showing indicating the output connections on its front panel.

The ‘OFF’/‘ON’ button operates the ‘OFF’/‘ON’ operation of the system. When the button is switched into the ‘OFF’ position, a 5 V / TTL high signal is applied to the FS40 and disables the high voltage output.

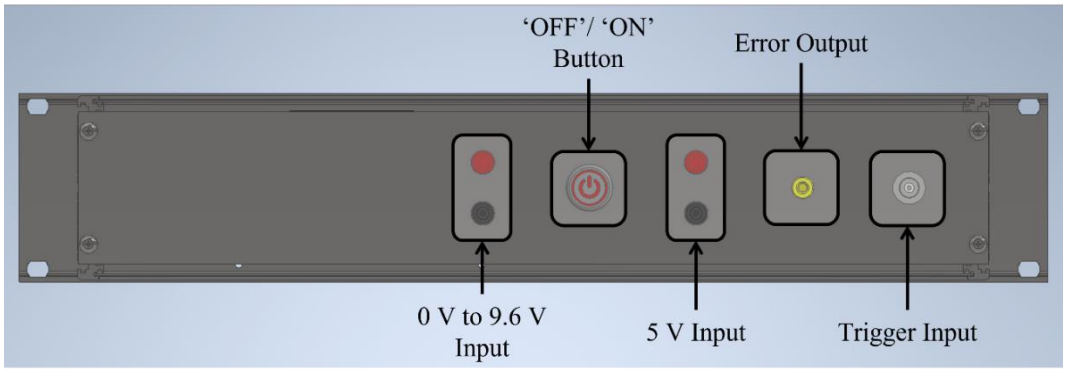


Fig. 5.52. The back panel computer aided design of the fast electroporation system

The second pair of red and black banana connectors requires a 5 V input. This 5 V supply provides 5 V to the FS40 for operation and powers the fault monitor circuit within the FS40 high voltage PSU. This 5 V also prides 5 V to the enable/disable terminal used to switch 'OFF' the unit. The yellow port is the error output pin from the system. If a high TTL signal is measured from this port, it indicates an error on the FS40 module. This error signal shuts down the FS40 module and the overall system.

The final input port is labelled the trigger input. This port is connected to the primary winding of the input isolation 1:1 pulse transformer. This input terminal allows an external control signal of 5V, 600 ns in duration with a specific repetition frequency to trigger the lowest stacked avalanche transistor (Q_1) into a controlled non-destructive avalanching.

Bill of Materials

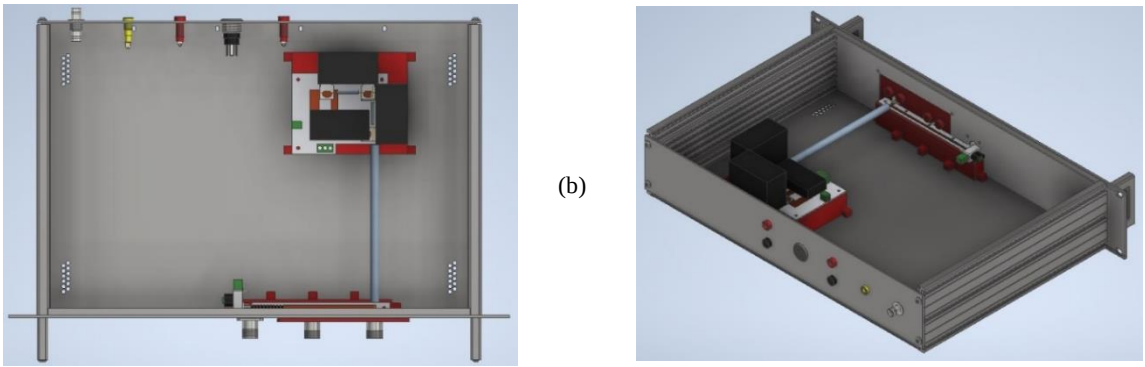
Table 5.10 gives the bill of the material (BoM) for the key components required to implement and build the fast nsPEF electroporation system shown in Fig. 5.53. Table 5.10 highlights that the overall cost of the critical components required to build the system is £693.76. The charged line and the ten avalanche transistors account for approximately 50% of the overall cost. The cost of the RG214 cable is £10.19 per meter. The two custom-designed PCBs account for approximately 10 % of the total cost.

Table 5.10. Bill of material of the fast nanosecond pulsed electric field electroporation system critical components (at time of design 2019)

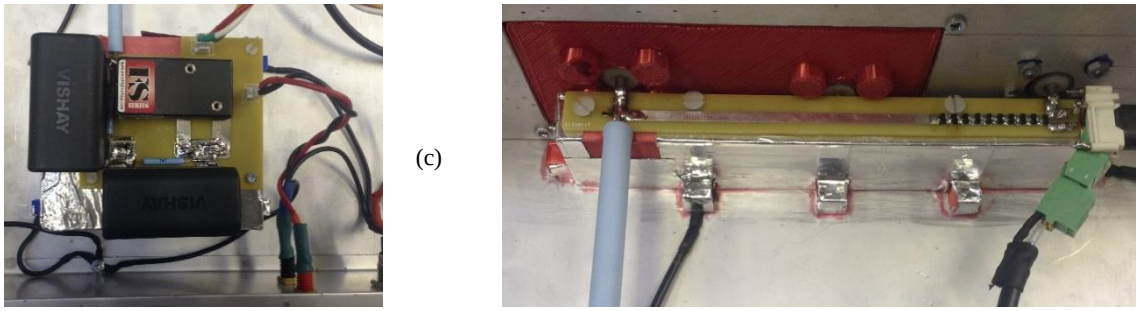
Component	Distributor	Stock No.	Cost per Unit (£)	Quantity
2U Rack Chassis	Farnell	1816035	104.29	1
MOX97021004FVE - High Voltage 1 MΩ, 20W, Resistor	Farnell	1551410	50.73	1
XPPower FS40 HVDC-voltage Converter	RS Components	123-8405	130.04	1
FMMT417TD Avalanche Transistor	Mouser	522-FMMT417TD	7.85	10
Belden Coaxial Cable, RG214/U, 50 Ω, 25m	RS Components	521-8391	254.75	1
Avalanche switching microstrip printed circuit board	Euro Circuits	-	33.78	1
High voltage supply printed circuit board	Euro Circuits	-	41.67	1
			Total Cost	£ 693.76

The user manual for operating and maintaining the fast nsPEF electroporation system is given in Appendix VII. This appendix provides information on mechanical and electrical specifications, instruction for use, and safety considerations surrounding the fast nsPEF electroporation system.

(a) (b)



(c) (c)



(d)

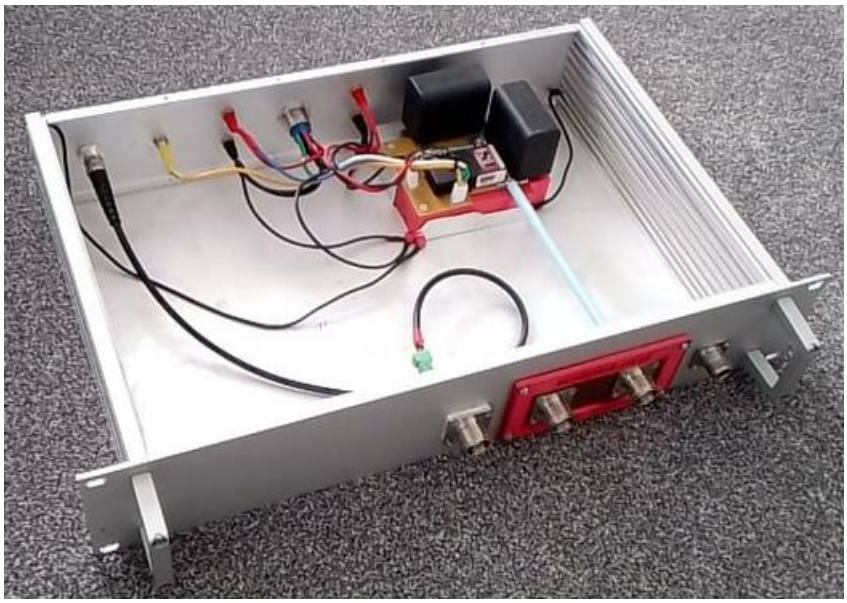


Fig. 5.53. The developed fast nanosecond pulsed electric field electroporation system (a) Top view computer aided design (b) Top-left computer aided design view (c) the built high voltage printed circuit board module (d) The built avalanche switching printed circuit board module (e) the final built system

5.7.4. Verification and Validation of the Fast nsPEF Electroporation System

Setup

The setup for the verification and validation of the system is illustrated in Fig. 5.54. A Quantum Composers 9520 Series Pulse Generator is used to produce the trigger signal. The 9520 unit generates a specific number of 5 V, 600 ns trigger pulse, of specified repetition frequency, which triggers the non-destructive avalanching of the avalanche switching. For a commercial system, the number of pulses and

the repetition frequency of the high voltage pulses generated across the load will be generated using an integrated microcontroller.

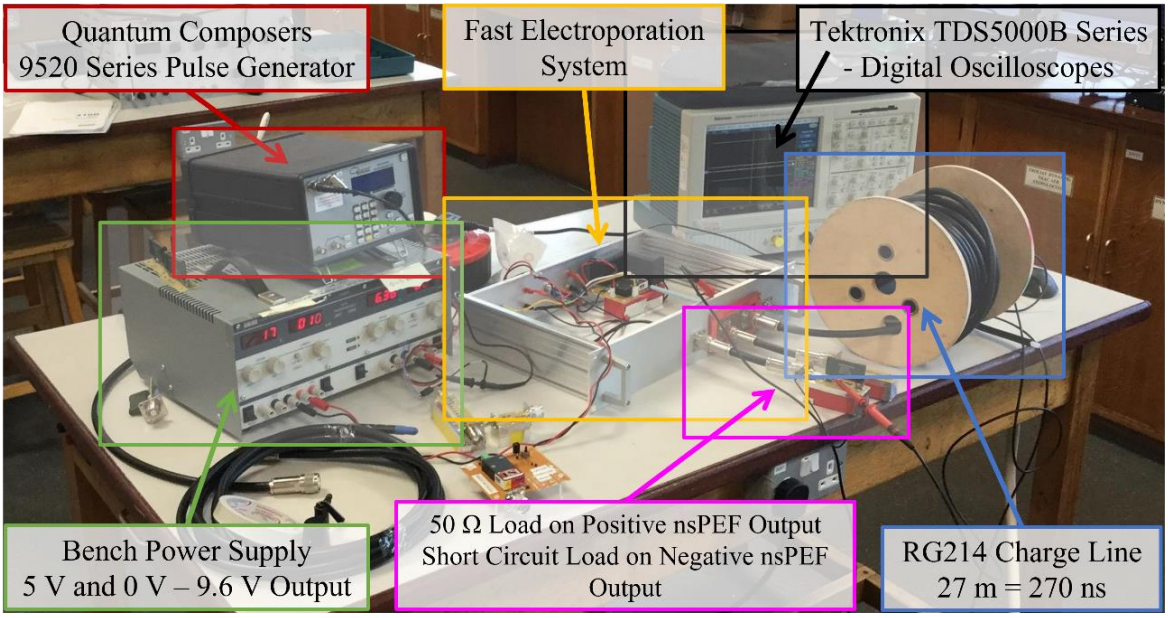


Fig. 5.54. Fast nanosecond pulsed electric field electroporation system verification and validation set-up

In this setup, a dual-channel bench PSU provides the necessary input voltages. One of the bench PSU outputs provides the 5 V, 1.25 A necessary to power the fast nsPEF electroporation system to operate the FS40 and its features. The second bench PSU channel provides the variable voltage input into the fast nsPEF electroporation system to control and select the high voltage level output from the FS40, which is the voltage level at the coaxial line that is charged. This provides flexibility in adjusting and selecting the amplitude of the nsPEFs generated.

A Tektronix TDS5054B-NV oscilloscope [31] with relevant high voltage probes [32] was used to capture, measure, and monitor the nsPEFs generated across the load. The TDS5054B-NV scope was also used to monitor the charging and discharging characteristics of the charge line. The verification and validation work investigates the nsPEF generated by the fast nsPEF electroporation system across a fixed load of 50 Ω as this is representative of the planned *in-vitro* investigation with this system, where the load is made up of D283 cells suspended in a 100 µl artificial buffer whilst maintaining their natural biological characteristics. This is identical to the biological load protocols described in section 4.3. as the bulk impedance of this load is 50 Ω.

Positive nsPEF Generation

The first validation of the system is its capability to generate positive nsPEFs of various durations and with various repetition frequencies. For the fast nsPEF electroporation system to generate positive nsPEFs, a coaxial transmission line of a specific length needs to be attached to the charged line input.

A short circuit connector is attached to the negative nsPEF HN-connector output. This is illustrated in Fig. 5.50(b).

Fig. 5.55 shows the positive polarity nsPEFs measured across a 50 Ω load and along the charged line. In this setup, a 7.5 V input signal was applied to the high voltage FS40 module to produce a 2500 Vdc at the output. A continuous trigger signal with a repetition frequency of 50 Hz (20 ms) was also applied. Fig. 5.55(a) shows that with a charged line of 1 m, 5 m and 17 m pulses electric fields of 10 ns, 50 ns, and 170 ns in duration with amplitudes of 1 kV are generated. This represents the performance of this modular design under bench testing conditions as illustrated in Fig. 5.41 (a).

Fig. 5.55(b) illustrates the voltage across the charged line. The rapid discharge indicates when a nsPEF is generated. This discharge of the 1 m, 5 m, and 17 m lines occurs at a repetition rate of 20 ms (50 Hz).

(a)

(b)

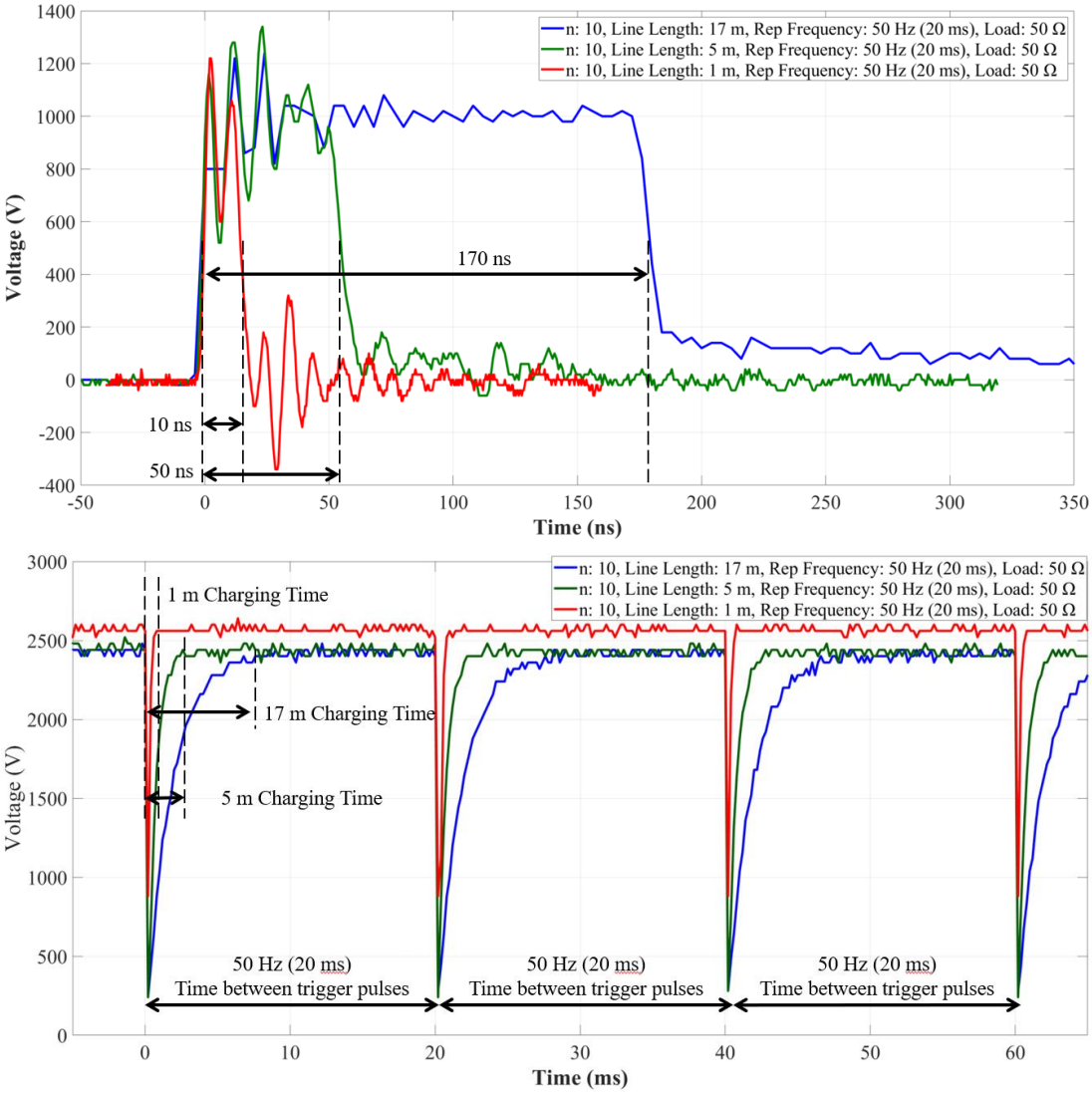
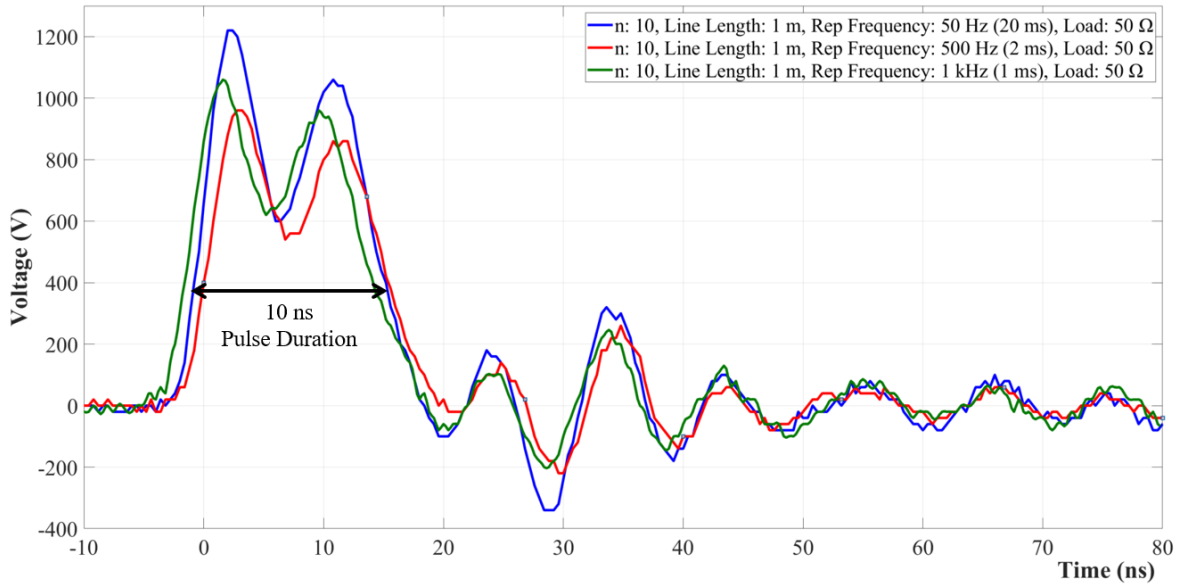
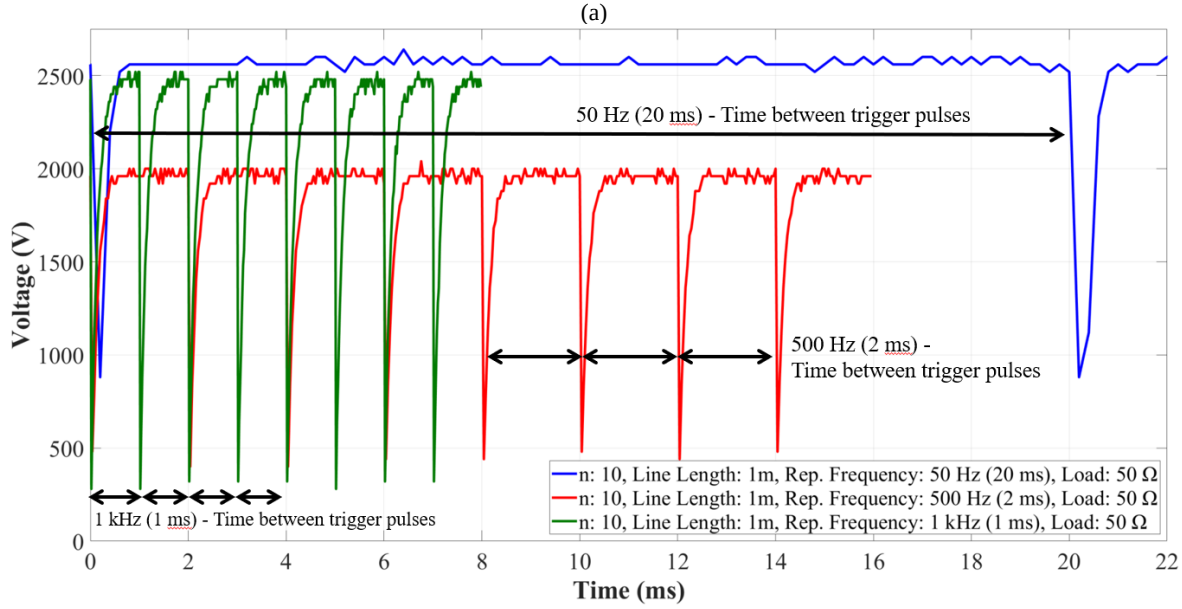


Fig. 5.55. Measured voltage waveform from the fast nanosecond pulsed electric field electroporation system, in positive nanosecond pulsed electric field mode, with various charged line lengths, 1 m, 5 m and 17 m lines with a repetition frequency of 50 Hz (20ms) (a) Across a 50 Ω load (b) along the charged line.

Fig. 5.56(a) demonstrates that the fast nsPEF electroporation system can produce comparable nsPEFs of specific duration with a trigger signal input of 5 V, 600 ns duration with a range repetition frequency. This figure shows the fast nsPEF electroporation system can produce high voltage nsPEFs of 10 ns, with a charged line length of 1m using a range of repetition frequencies from 50 Hz (20ms) to 1,000 Hz (1 ms). The nsPEFs and the voltage across the charged line were captured simultaneously. This is shown in Fig. 5.56.



(a)



(b)

Fig. 5.56. Measured voltage waveform from the fast nanosecond pulsed electric field electroporation system, in positive nanosecond pulsed electric field generation mode, with a 1 m charged line and repetition frequencies of 50 Hz (20ms), 500 Hz (2 ms) and 1,000 Hz (1 ms) (a) across a 50 Ω load (b) across the charged line.

Negative nsPEF Generation

The second point of the validation work was to verify that the system can generate negative nsPEFs of various durations and repetition frequencies. For the fast nsPEF electroporation system to generate

negative nsPEFs a coaxial transmission line of a specific length needs to be attached to the charged line input. Additionally, a short circuit is made at the positive nsPEF HN-connector output. This is illustrated in Fig. 5.50(c).

Fig. 5.57 shows the negative polarity nsPEFs delivered across a 50 Ω load and the voltage across the charged line. For this measurement, the control voltage on the FS40 high voltage power supply was 7.5 V and this produced a 2500 V output from the high voltage FS40 module. Fig. 5.57(a) shows that with a charged line of 1 m, 5 m, and 17 m in length pulses of duration of 10 ns, 50 ns and 170 ns, with amplitude of 1 kV (peak-to-peak of 1 kV) were generated.

(a)

(b)

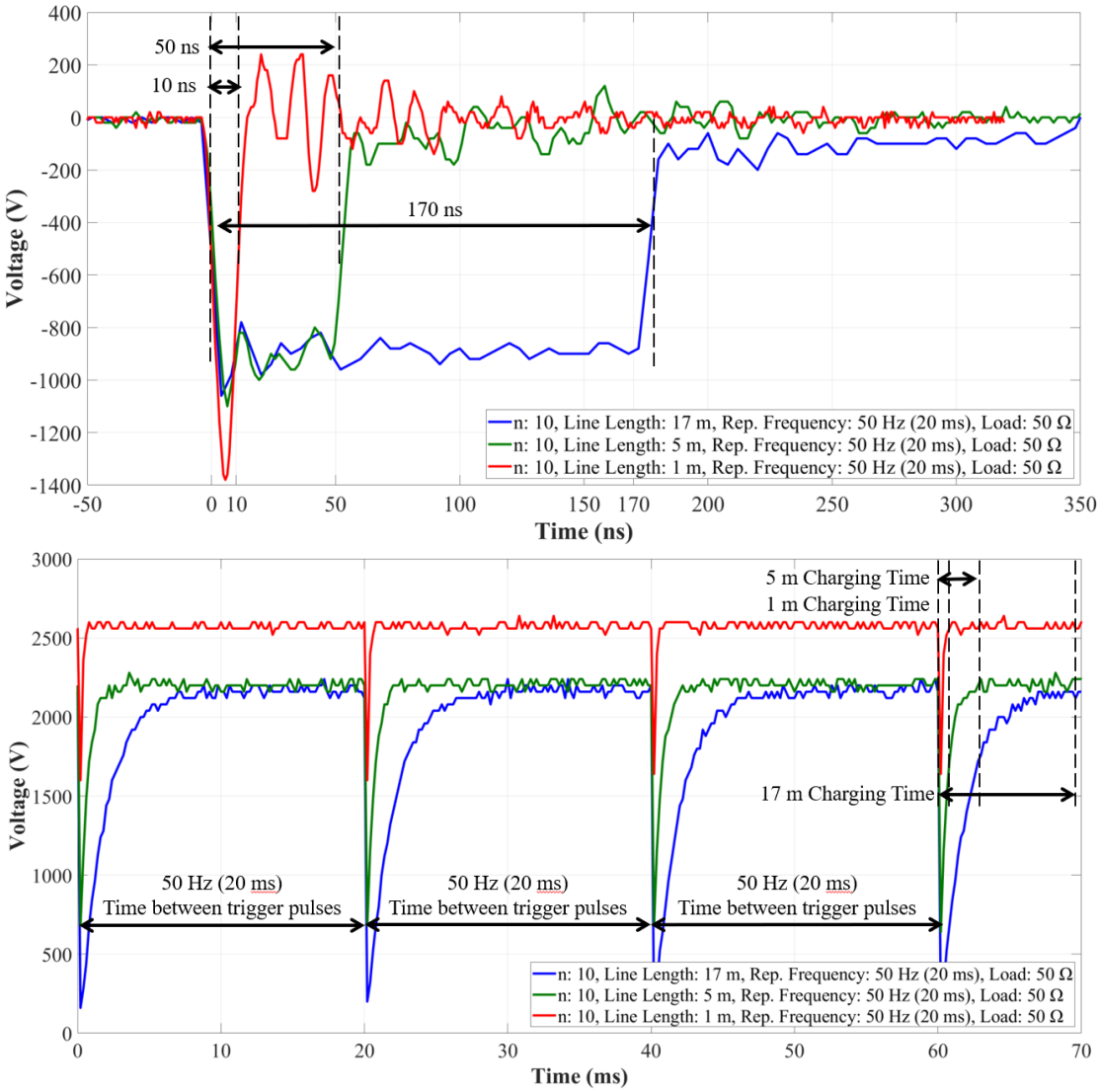


Fig. 5.57. Measured voltage waveform for the fast nanosecond pulsed electric field electroporation system, producing negative pulses with line lengths of 1 m, 5 m and 17 m and a repetition frequency of 50 Hz (20ms) (a) across a 50 Ω load (b) across the charged line

Fig. 5.57(b) illustrates the voltage level across the charged line. This demonstrates the rapid discharging of the line, which indicates when a nsPEF is generated and its associated repetition

frequency. The discharging of the 1 m, 5 m, and 17 m lines, and therefore the generation of the 10 ns, 50 ns, and 170 ns PEFs respectively occur at a repetition rate of 20 ms (50 Hz).

Fig. 5.58(a) illustrates that the fast nsPEF electroporation system can produce nsPEFs of selected duration with a trigger signal input of 5 V, 600 ns duration and repetition frequencies of 50 Hz, 500 Hz and 1 kHz. This figure shows that the fast nsPEF electroporation system can produce high voltage negative nsPEFs of 10 ns, with a charged line length of 1m at a range of trigger repetition frequencies from 50 Hz (20 ms) to 1,000 Hz (1 ms). The nsPEFs were captured simultaneously to the voltage across the charged line in Fig. 5.58(b). This confirms that the triggering (generation of the nsPEFs) is operating correctly.

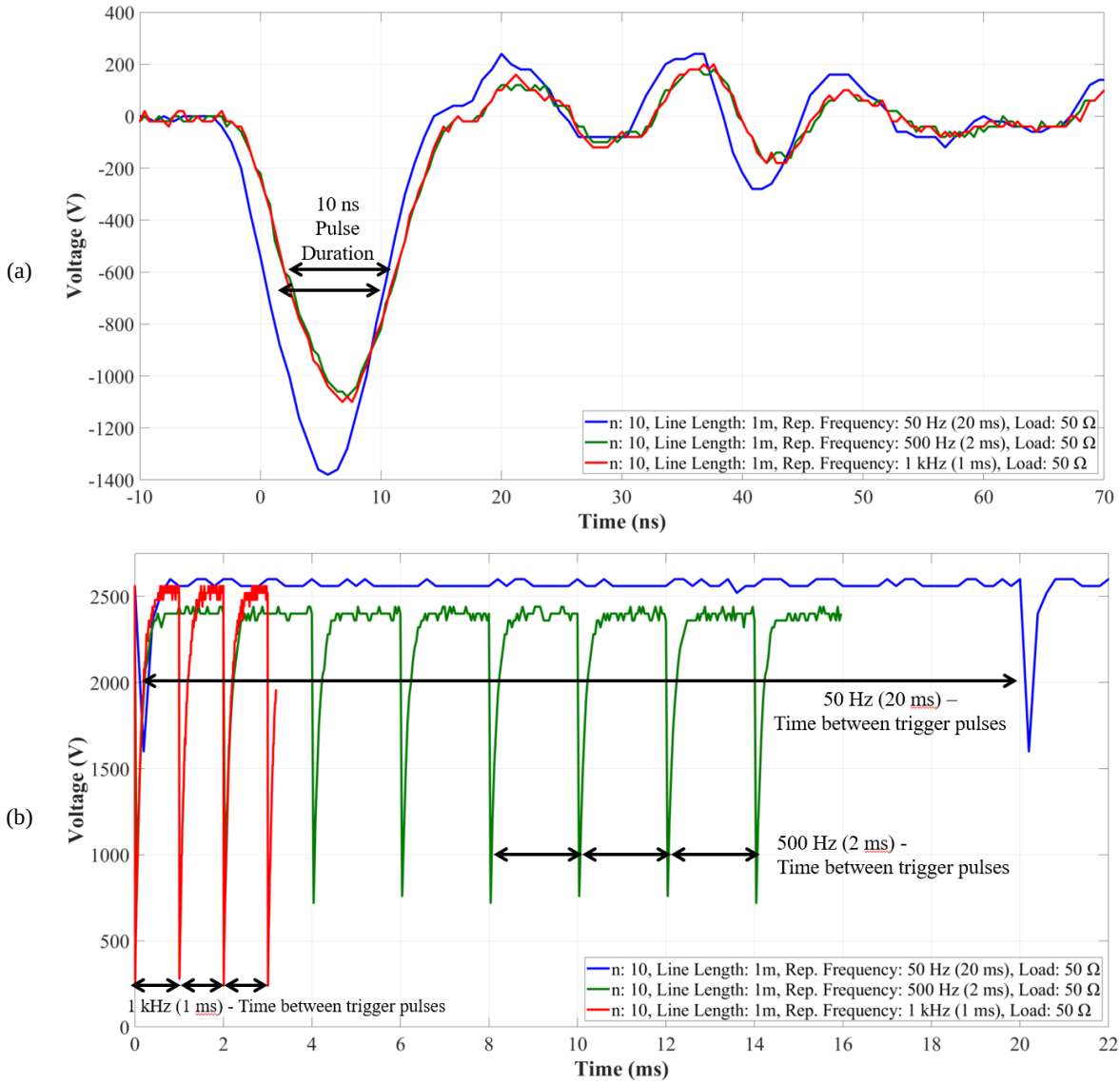


Fig. 5.58. Measured voltage waveforms for the fast nanosecond pulsed electric field electroporation system generating negative pulsed electric fields using a 1 m charged line and repetition frequencies of 50 Hz (20ms), 500 Hz (2 ms) and 1,000 Hz (1 ms) (a) across a 50 Ω load (b) voltage across the charged line

The results shown in Fig. 5.57 and Fig. 5.58 show that the generation of nsPEFs with negative polarity is comparable to the results given in Fig. 5.55 and Fig. 5.56 for the generation and characteristics of positive nsPEFs.

5.8. Conclusion

This chapter describes the design and development of the developed fast nsPEF electroporation system to generate unipolar 10 ns to 300 ns PEF in excess of 1 kV in amplitude, of either positive or negative polarity, with a rise time of less than one nanosecond. The topology chosen is a combination of relatively slow charging and rapid discharging of a coaxial line through a stack of ten avalanche transistors, which operates as a fast-switching element. Additionally, the system can be configured to generate positive and negative polarised pulses simultaneously with amplitudes of more than 500 V. The final system is illustrated in Fig. 5.53.

The fast nsPEF electroporation system has been verified and validated for its ability to generate nsPEFs of various amplitudes, duration, and repetition frequencies across a 50 Ω load. It has been shown that this fast nsPEF electroporation system meets the requirements outlined in Table 5.11.

Table 5.11. Fast nanosecond pulsed electric field electroporation system requirement agreed vs achieved

nsPEF Characteristic Requirement	Agreed	Achieved
Load impedance	50 Ω	50 Ω
Pulse Duration	10 ns – 100 ns	10 ns – 300 ns+;
Amplitude	1 kV+	Up to 2.5 kV
Repetition Frequency (Rate)	1 Hz (1 s) – 50 Hz (20 ms)	1 Hz (1 s) – 1 kHz (1 ms);
Number of pulses	1 – 50	1 – continuous pulses;
Polarity	Unipolar positive PEF	Unipolar positive or negative PEF individually or simultaneously

The system is impedance sensitive in its operation. This is because the amplitude and the reflection coefficient of the system are dependent on the relationship of the total load impedance (Z_L) across the system with the characteristic impedance of the coaxial line used (Z_0). This has been proven in theory by (5.6) and (5.7). The amplitude of the nsPEFs generated is restricted by the number of avalanche transistors that are stacked in series and their collective collector-emitter breakdown voltage (nBV_{CES}). This has been demonstrated in theory by (5.24). This work concludes that stacking twenty transistors can produce a PEF of 10 ns in duration, with an amplitude of 2.5 kV, as shown in Fig. 5.31.

The rise and fall times of the pulses are determined by the avalanche transistors operating as the fast-switching element. It has been discovered from a literature search that 300 ps rise/fall time can be achieved by avalanche transistors. The transition times captured in this work are of the order of one nanosecond and this is due to the frequency response limitation of the LeCroy PPE5KV 400 MHz high voltage probe used for the measurements [32].

Through manipulating the current loop within the circuit and placing a fixed resistor across the emitter and ground of avalanche transistor Q_1 and the outer conductor of the coaxial line and ground a unipolar or simultaneous generation of negative and positive nsPEFs can be generated.

In conclusion, the fast nsPEF electroporation system shown in Fig. 5.53 can generate well-defined symmetrical high voltage nsPEFs, of various polarities, with rise and fall times less than a nanosecond, and with a wide variety of pulse lengths and repetition frequencies. The nsPEF parameters and associated limitations of the fast nsPEF electroporation system are highlighted in Table 5.12.

Table 5.12. Nanosecond pulsed electric field parameters and limitation associated with the fast nanosecond pulsed electric field electroporation system.

nsPEF parameters	Minimum	Maximum	Limitation
Pulse Amplitude (V)	500	1,500	Determined by the number of avalanche transistors stacked and their collective breakdown voltage and the relationship between Z_L and Z_0
	$V_{LMin} = \left(\frac{Z_L}{Z_L + Z_0}\right) nBV_{CEO}$	$V_{LMax} = \left(\frac{Z_L}{Z_L + Z_0}\right) nBV_{CES}$	$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC}$
Pulse Duration (ns)	10	300 +	Determined by the co-axal charged line dielectric constant and length
		$pulse\ width = 2T = 2\frac{l\sqrt{\varepsilon_r}}{c}$	
Repetition Frequency (Hz)	1	50 +	Limited by the charging time of the charged line used
		$f = \frac{1}{5\tau} = \frac{1}{5R_C C} = \frac{1}{5R_C l C_{line}}$	
Rise Time		300 ps, as illustrated in literature	
Reflection Coefficient of the system, **Γ**	0	-1 or 1	Determined by the relationship between Z_L and Z_0
		$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$	

This electroporation system is an instrument to enable clinicians and microbiologists to carry out a range of experiments and research studies. The intention of this system is to be used to investigate the effect of nsPEF on the D283 medulloblastoma cell population, where cells are suspended in a 50 Ω impedance artificial buffer. This planned investigation is identical to the investigation conducted in 'Chapter 4'. The planned investigations are part of the SUMCASTEC programme. Furthermore, the system could support future *in-vitro*, *ex-vivo* and *in-vivo* investigations of nanosecond pulsed electric field-based applications in biology and medicine.

5.9. Future Work

This fast nsPEF electroporation system achieved the agreed set of requirements from the SUMCASTEC consortium for a system capable of producing nanosecond rise/fall times high voltage electric fields. The chosen topology of combining a charged line technique with an avalanche transistor-based switch has been proven as a suitable methodology for the generation of high voltage nsPEF with transition time in the picosecond regime.

This system requires future work to become a stand-alone unit with an integrated microcontroller and dc power supplies. Further future development for the fast nsPEF electroporation system includes the adaptation to be a standalone energy module and a potential alternative charged line for a variable length of an open-circuit transmission line to change the pulse width.

5.9.1. Alternative Charged Lines Structures

Fixed Delay Coaxial Line Structures

The duration of the pulses is determined by the delay time associated with the charged line. This delay is proportional to the physical and electrical length of the transmission line. For the concept to work the distal end of the line is an open circuit. For future work, an alternative transmission line structure(s) could be used.

When a specific nsPEF duration is identified that results in a beneficial clinical effect the length of the transmission line can be fixed. The duration of the nsPEF generated will be fixed and determined by the dielectric constant and length of the coaxial transmission line (5.4).

This inbuilt fixed transmission line with a specific associated delay time can be in the form of a coaxial or microstrip line. Both have their associated advantages and disadvantages. Using a dielectric material, in a coaxial or microstrip line structure, with a larger dielectric constant (ε_r) would result in the need for a shorter physical and more compact structure.

Microstrip transmission lines can easily be fabricated to a specific impedance and integrated onto the avalanche-switching microstrip circuit. The impedance of a microstrip transmission line is dependent on the microstrip width and the thickness of the dielectric material. This is highlighted in equations (5.14) to (5.17). Mechanically, a microstrip line can take up less space than a coaxial line as it could be implemented as any pattern fabricated on the microstrip i.e., spiral, zigzag, lines around the board.

Helical Line

A helical line could be employed to enable the associated delay time within the structure to be adjusted [6], [38]. A helical line is illustrated in Fig. 5.59, where the inner conductor is placed in a rectangular channel or trough transmission line structure that is milled onto a rotary metal cylinder.

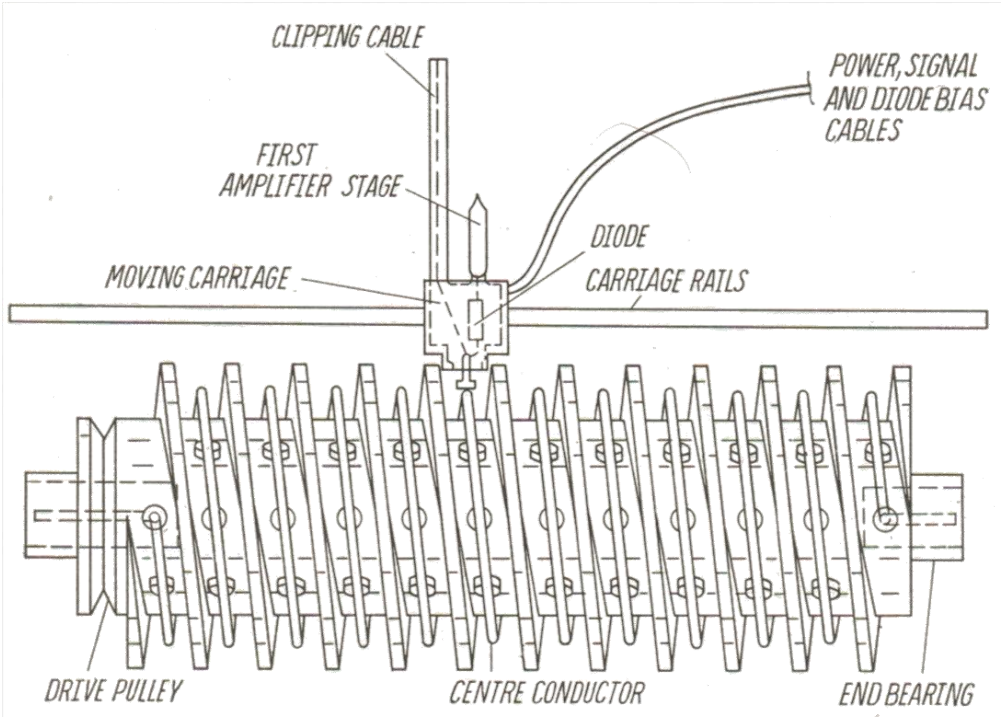


Fig. 5.59. Helical delay line structure design [6]

The characteristic impedance of the rectangular through transmission line is determined by the dimensions of the line, as indicated by equation (5.36). Equation (5.36) can be used to calculate the characteristic impedance (Z_0) of the line.

$$\text{If d} \ll \text{a}, \qquad Z_0 = 60\sqrt{\frac{\mu}{\varepsilon}}\ln\frac{4b\tanh\frac{\pi a}{b}}{\pi d} \tag{5.36a}$$

$$\text{b} << \text{a}, \qquad Z_0 = 138\sqrt{\frac{\mu}{\varepsilon}}\log_{10}\frac{4b\tanh\frac{\pi a}{b}}{\pi d} \tag{5.36b}$$

Where a is the distance between the centre point of the cylindrical inner conductor to the inner wall of the rectangular-shaped outer conductor, b is the length of the inner wall of the rectangular-shaped outer conductor and d is the diameter of the cylindrical inner conductor. These dimensions are illustrated in Fig. 5.60.

A sliding contact can be used, that is fastened to a moving section to determine the delay associated with the line and therefore the pulse duration. Because of the large winding diameter of the structure, the behaviour of the delay line is like a homogenous line structure. For the structure shown in Fig. 5.59, air is used as the dielectric material, but this does not need to be the case. The main attenuation factor

associated with this structure is the radiation loss of the open rectangular line. Shielding the entire helical line will afford some reduction in the loss [6]. The design of the structure is more complex than a standard open-ended coaxial cable. An advantage of the helical line is the ability to adjust the electrical length of the line.

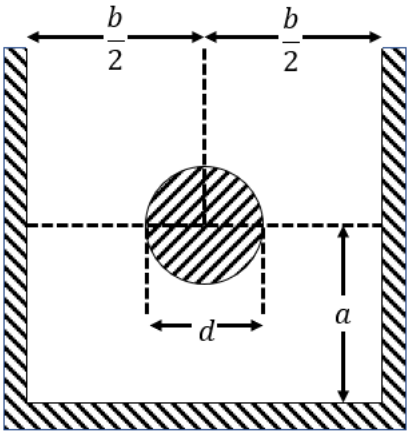


Fig. 5.60. Wire-in semi-infinite rectangular trough transmission line design [6]

Trombone Line

A trombone or extendable line is another variable line design. It can be used to achieve a controllable time delay more conveniently and simplistically than the helical line. It consists of a length of coaxial lines or microstrip lines that can be physically extended.

Fig. 5.61 illustrates a coaxial trombone line. The delay is determined by the expansion or compression of the transmission line. A microstrip trombone structure is a relatively simple structure. Sliding one microstrip across another adjusts the overall electrical length and therefore the associated delay of charged line.

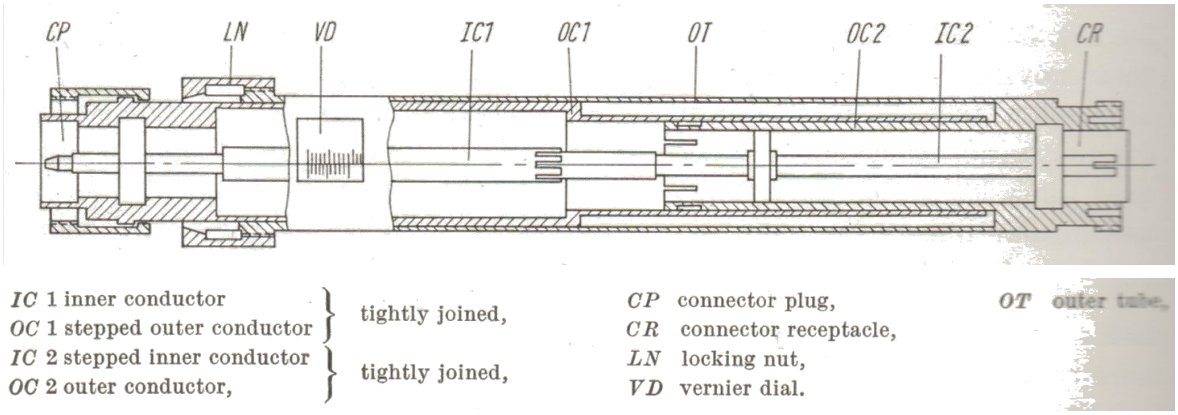


Fig. 5.61. Decimetre extension line or trombone-type delay line [6]

Fig. 5.62 shows the application of a trombone line to adjust the associated delay within a charge line from its minimum to maximum length/associated delay [6].

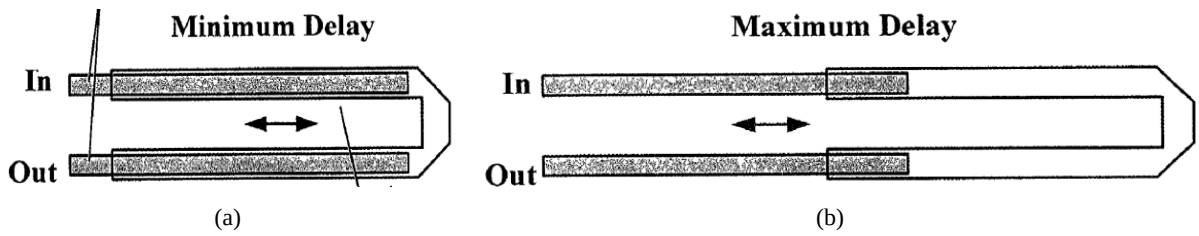


Fig. 5.62. The concept of a trombone line to adjust the delay or electrical length of a charged line. (a) for minimum delay time (b) maximum delay time [6]

Ferrite Lines

Ferrite transmission lines are another method of producing a variable delay. These structures are influenced by the loss of the magnitude of the bias magnetising current which changes the time location of the leading edge of the incident pulse [6]. An example of this can be seen with a cable of 20 m length in which its associated delay time can be altered by 100 ns with a current alteration of 1 A. The drawback of a ferrite line is the temperature coefficient associated with a high current level, which leads to delay time instability.

Summary

An alternative transmission line structure needs to be investigated in future if a commercial fast nsPEF electroporation system is to be developed. This would reduce the need for an external input port and an external coaxial line. This alternative transmission line can have a variable or fixed associated delay time, depending on the end application of the system.

5.9.2. Bipolar Pulse Generator

The fast nsPEF electroporation system topology can be adapted into a system that can generate monopolar and bipolar pulsed electric fields. Examples of three potential topologies of utilising a transmission line with fast-switching elements to produce a bipolar nsPEF electroporation system are described below. The fast-switching elements in these examples would be a stack of avalanche transistors as described in this work.

Fig. 5.63. shows a circuit to generate bipolar pulses with three identical transmission lines with a characteristic impedance (Z_0) and associated delay time, or propagation time of T and two fast switching elements S_1 and S_2 [40]-[41]. The load (Z_L) in this example would need to be twice the characteristic impedance (Z_0) of the transmission lines for a system with zero reflection coefficient (Γ). The duration of the nsPEF generated across the load would be four times the associated delay time of the transmission lines (4T). The amplitude of the PEF is equal to the turn-on voltage. Theoretically, the ideal bipolar pulse waveforms are obtained when the second switching element (S_2) is closed at the time of 2T after the first switching element (S_1) is closed.

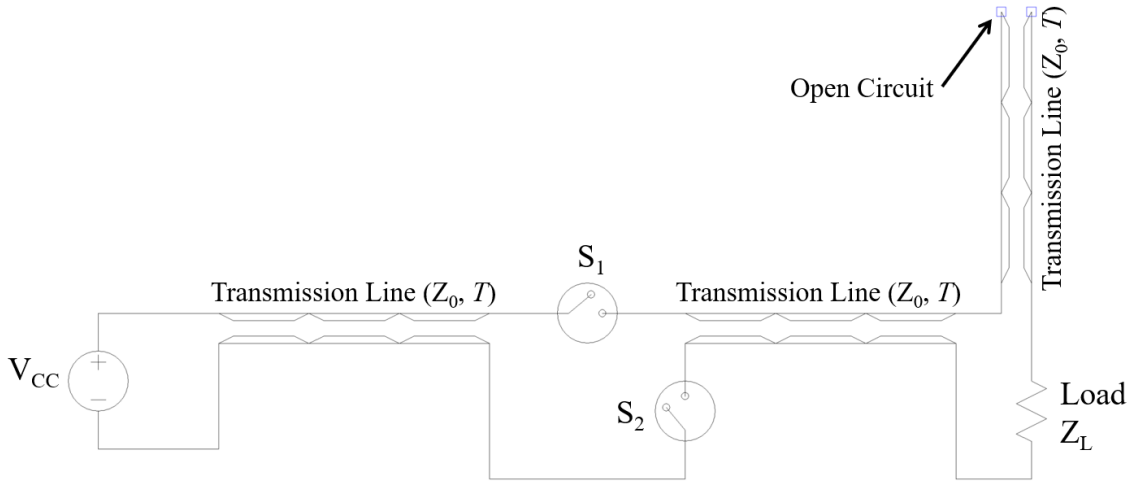


Fig. 5.63. Bipolar pulse generator with three transmission lines and two switching elements presented in [40] and [41]

Fig. 5.64 shows a bipolar pulse generator consisting of a single transmission line and two switches [64]. Here the load impedance (Z_L) is the same as the characteristic impedance (Z_0) of the transmission line with a one-way delay/propagation time of T.

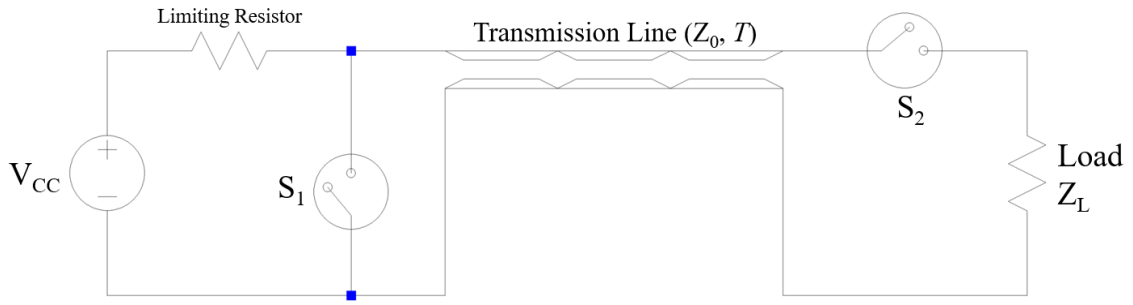


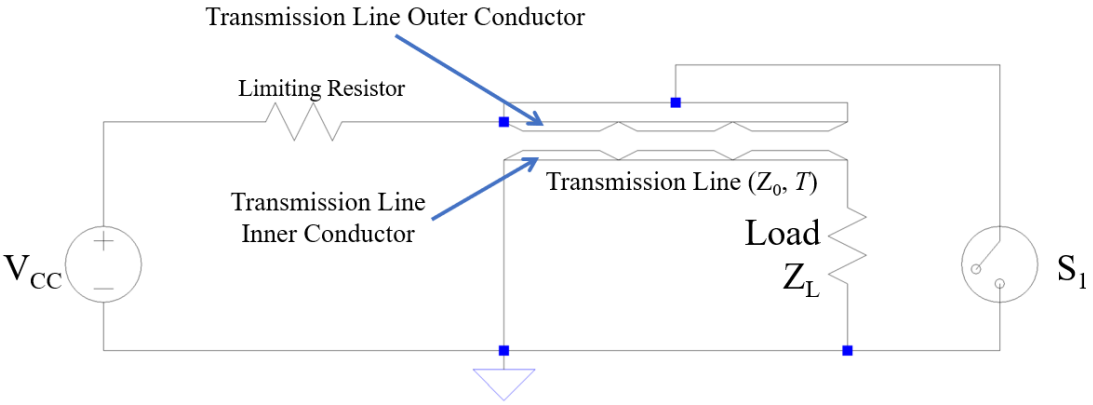
Fig. 5.64. Bipolar pulse generator with a single transmission line and two switching elements presented in [42]

Before the operation, the transmission line is charged to an amplitude of V_{CC} as both switches (S_1 and S_2) are closed. When the two switches are closed a step wave is generated from each of the switches. The first wave generated from S_1 has an amplitude of $-V_{CC}$ and propagates to the right. The second wave generated from S_2 has an amplitude of $-\frac{V_{CC}}{2}$ and propagates to the left. When the two waves pass the midpoint of the transmission line, a potential distribution occurs. The first wave with an amplitude of $-\frac{V_{CC}}{2}$ is absorbed by the load (Z_L) because of Z_L=Z_0 of the transmission line. The second wave is reflected from the S_1 after a time T with an amplitude of $\frac{V_{CC}}{2}$ as a short circuit is seen at S_1 as the switch is now closed ($\Gamma = -1$).

The generated pulse has a bipolar pulse width of 2T. The peak-to-peak voltage of the bipolar pulse is equal to the V_{CC}. Theoretically, the ideal bipolar pulse waveforms are obtained when the two switches S_1 and S_2 are closed simultaneously.

Fig. 5.65 shows a topology for the generation of a bipolar nsPEF electroporation system that utilises a single transmission line and a single switching element [43]. The switching element is located between the two ends of the transmission line outers and the ground plane. For a system with zero reflection coefficient, the load impedance (Z_L) matches the characteristic impedance of the transmission line (Z_0) with an associated delay/propagation time of T. When the switch is closed, the left end of the coaxial line becomes a short circuit ($\Gamma = -1$) and the right side of the transmission line is connected to the load. Therefore, this circuit is equivalent to the circuit shown in Fig. 5.64. The generated pulse has a bipolar pulse width of 2T with a peak-to-peak voltage of V_{CC}.

(a)



(b)

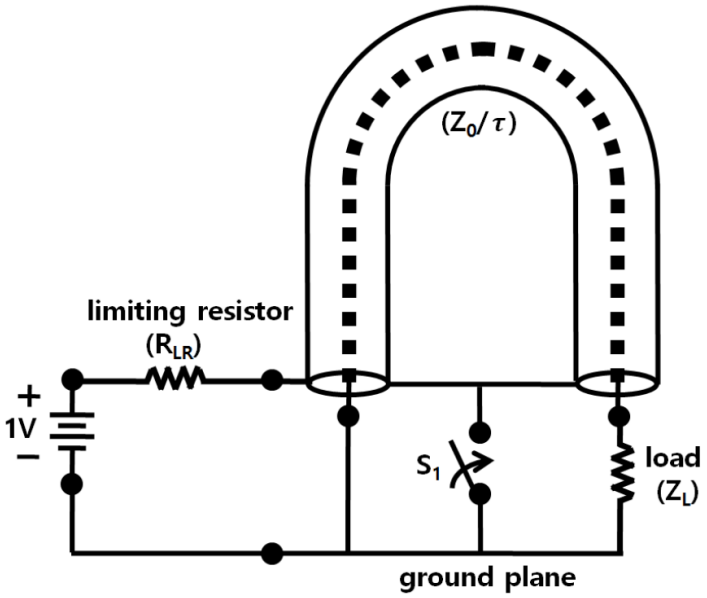


Fig. 5.65. Single switch bipolar pulse generator circuits (b) presented in [43]

5.9.3. Future Standalone Energy Module Development

The current method of selecting the nsPEFs provides a flexible and responsive system for research purposes. The next stage is to understand the operation on *in-vivo* bulk tissue. Once operation on bulk tissue is optimised, a standardised standalone electroporation energy module can be developed.

This future iteration of the system would be a standalone module that includes an integrated PSU, a variable-length transmission line that can automatically be adjusted using an arrangement of coaxial switches, a microcontroller, and a graphical user interface (GUI).

Microcontroller and Graphical User Interface

The current fast nsPEF electroporation system timing characteristics are controlled by using a Quantum Composers 9520 series pulse generator [34].

The addition of a microcontroller would provide an embedded application to integrate a GUI and control the system to enable automatic control of the high voltage generator, the width of the pulses and the repetition frequency. The basic abstract description of the behaviour of a future microcontroller within the next iteration of the fast nsPEF electrorotation system is shown in Fig. 5.66 and Fig. 5.67. With an integrated microcontroller incorporated into the system, a user of the fast nsPEF electroporation system can interact with a GUI.

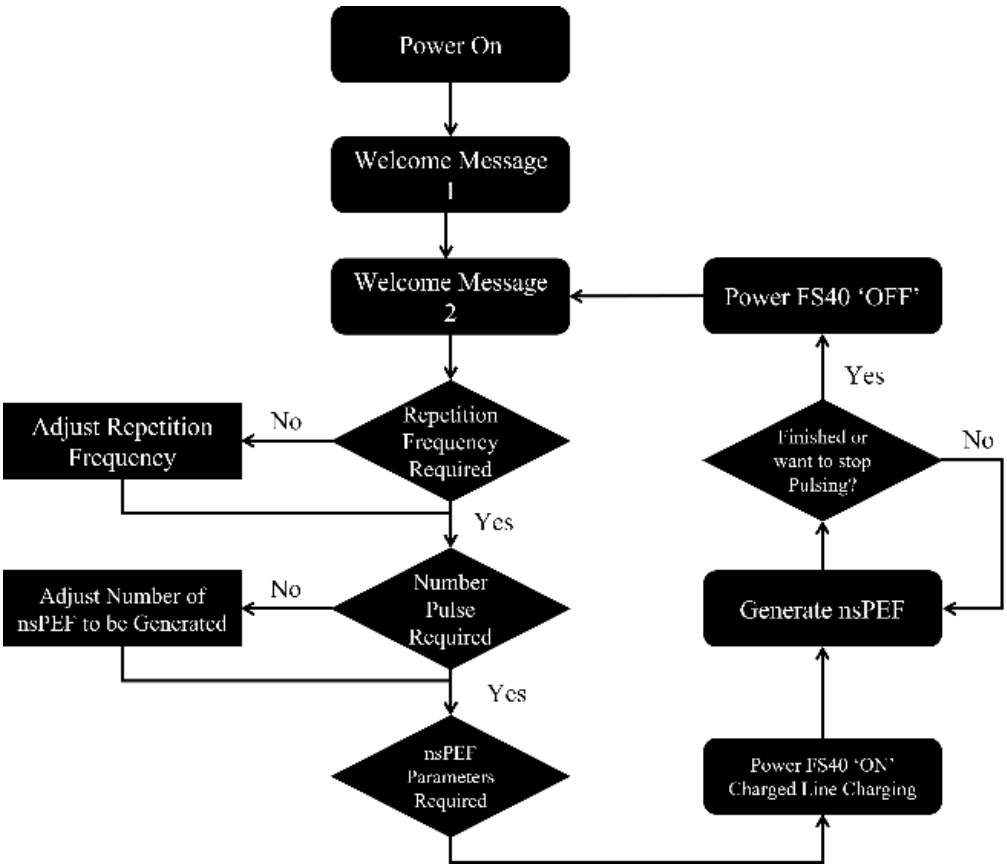


Fig. 5.66. The potential state event diagram of the future microcontroller flow chart

Power Supply

Currently, a 5 V bench power supply is required for the FS40 high voltage supply. A second variable bench power supply that can be varied between 0 V to 9.6 V is used to adjust the dc voltage level on the transmission line. A future improvement would be to have a board or chassis-mounted

PSUs within the fast nsPEF electroporation system to eliminate the need for a bench power supply to operate the system.

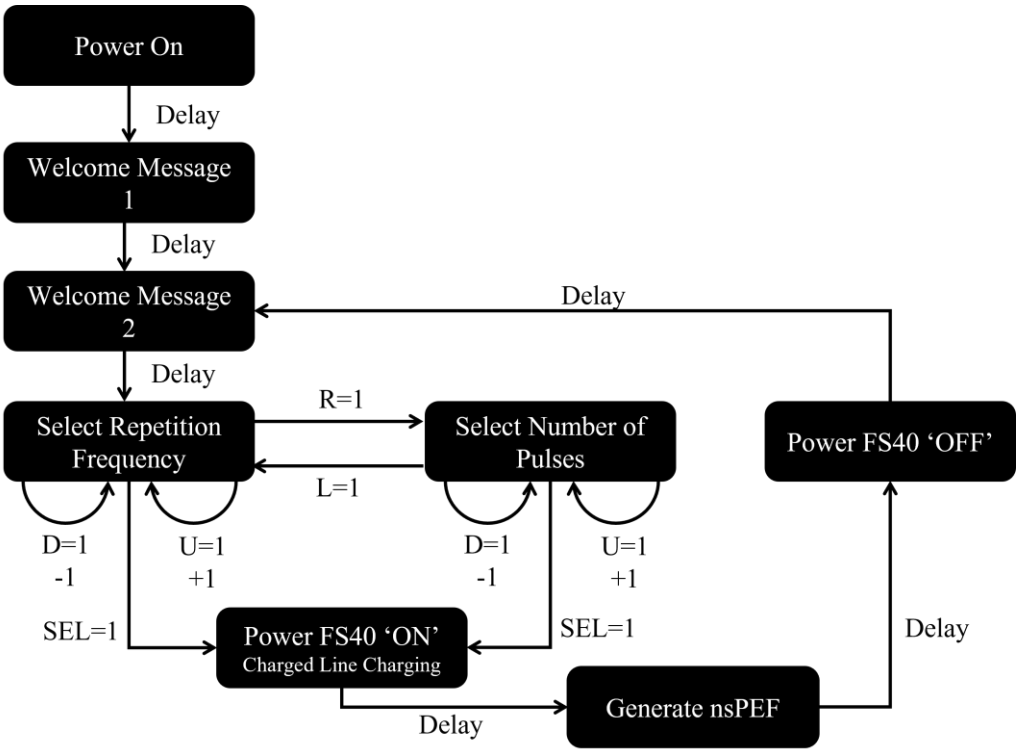


Fig. 5.67. The potential state event diagram of the future microcontroller state machine

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CHAPTER VI. FAST NSPEF ELECTROPORATION SYSTEM – PRE-CLINICAL INVESTIGATION

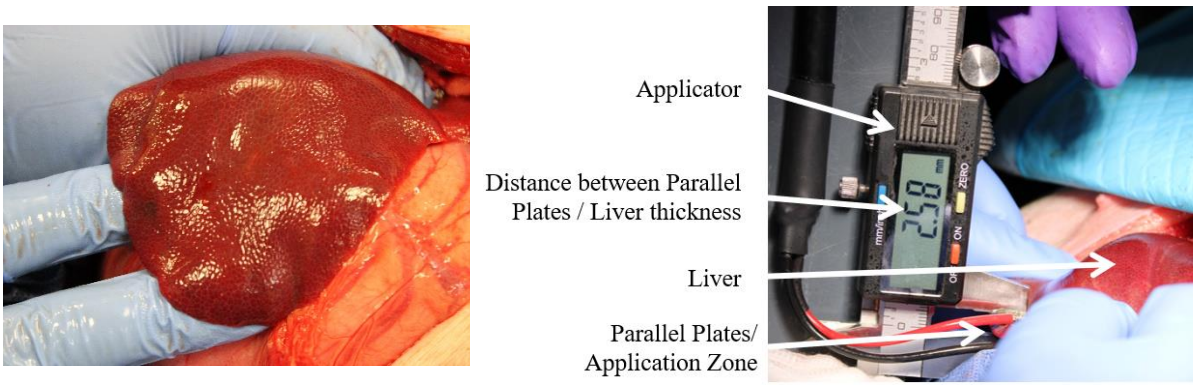
6.1. Introduction

In-vivo pre-clinical testing on the fast nanosecond pulsed electric field (nsPEF) electroporation system was carried out at the Barcroft Animal Testing Facility, Cambridge. The goal of the preclinical was to evaluate the performance of the fast nsPEF electroporation system in terms of delivering nsPEFs into bulk liver tissue and to understand any adverse effects of the nsPEFs on the bulk tissue through histology. This study moves the work from the 50 Ω impedance load described in the previous chapters to focus on the application of fast pulsed electric fields in a real application within a pre-clinical *in-vivo* setting.

6.2. Pre-Clinical Set-up

The pre-clinical investigation was conducted on a porcine subject weighing approximately 65 kg. The subject was suitably medicated and anaesthetised by staff at the Barcroft facility. The heart rate, rhythm, and electrical activity in addition to oxygen saturation, Carbon Dioxide (CO_2) and respiratory rate were measured, via an electrocardiogram (ECG) and recorded.

The liver was accessed by a surgical incision into the abdomen. Ten separate sites on the liver were agreed upon for the application of a specific number of nsPEFs delivered to the site. Following the pre-clinical testing, the subject was terminated, and the treated sites were sectioned for histological analysis. Fig. 6.1 shows how the nsPEF was applied to the liver via the applicator.



(a) (b)

Fig. 6.1. (a) Pre-clinical procedure to access the subject's liver (b) Applicator set-up to deliver pulsed electric field onto the liver

The nsPEFs energy was generated by the fast nsPEF electroporation system, described in Chapter 5. The nsPEFs were delivered into the liver sites using a 10 mm2 parallel plate applicator structure as shown in Fig. 6.3.

The set-up for the pre-clinical study is shown in Fig. 6.2. A positive nsPEF of 248 ns was produced by the fast nsPEF electroporation system and the pulses delivered into each site were captured in real-time by a Tektronix TDS5054B-NV Oscilloscope [1] with a LeCroy PPE 5 kV high-voltage probe [2]. The waveform was measured across the generator's positive nsPEF output port and the ground of the system and not across the liver load/instrument.

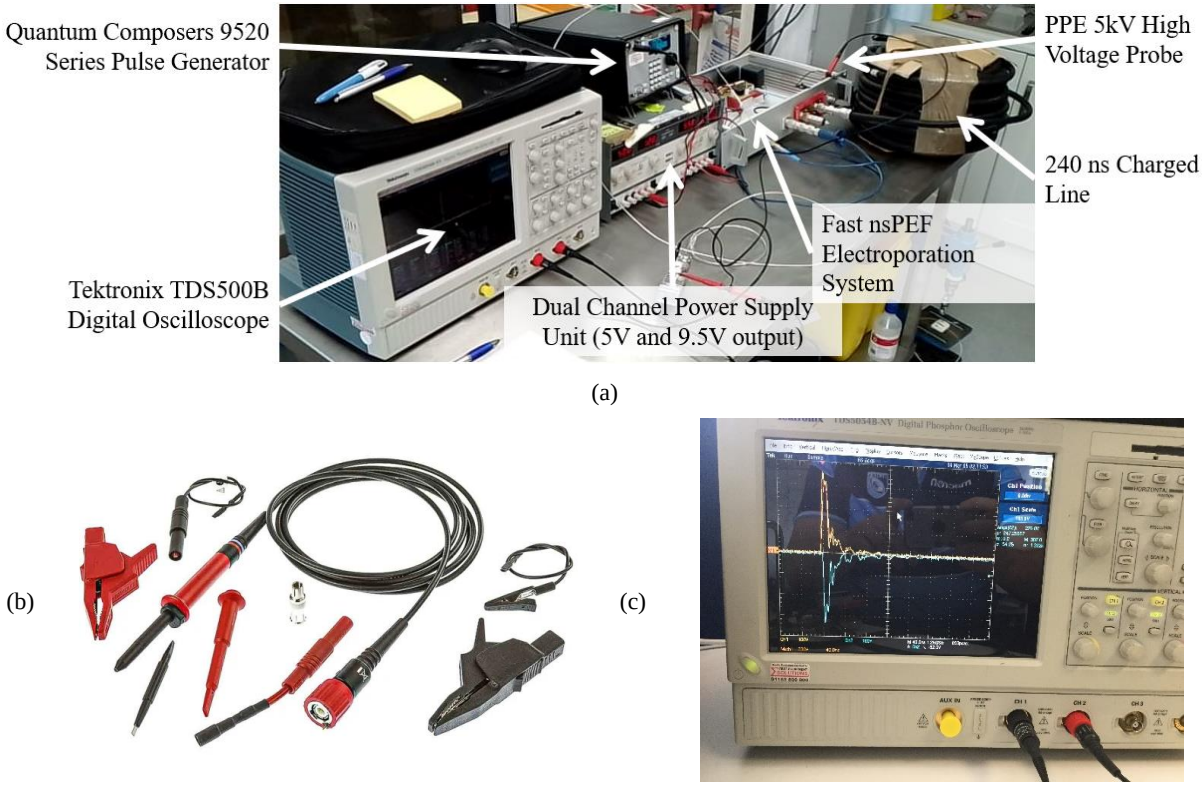


Fig. 6.2. (a) Fast nanosecond pulsed electric field electroporation system set-up for the pre-clinical study (b) PPE 5kV High Voltage Probe (c) Tektronix TDS500B Digital Oscilloscope

This setup provided the capability to verify and validate the performance of the fast nsPEF electroporation system to deliver nsPEFs onto bulk liver tissue loads. By capturing the nsPEF waveform applied to the body it is possible to calculate the electric field, the power and energy delivered into the liver and determine the temperature to ensure that the energy delivery is non-thermal. The method used to calculate these parameters is discussed later in this chapter.

6.2.1. Liver as a model to demonstrate the extracellular effect on cells and matrix (collagen)

The liver was selected for the pre-clinical study because it is easily accessed and most of the work carried out to date to establish electroporation parameters has been performed using the porcine liver model [3]-[8]. This provides referenceable data for the comparison of nsPEFs energy to microsecond pulsed electric fields (µsPEFs) energy delivery. Liver tumours are a prime target for this type of treatment along with skin, kidney, breast, and other solid organ tumours [3]-[8].

The liver is accepted as the place to start to gather appropriate physiological information, including histopathology, which can be consistently repeated [3]-[8].

6.2.2. Applicator

The applicator used a vernier calliper to accurately measure the distance between the two electrodes to determine the applied electric field. The electrodes comprised of a pair of square 10 mm2 (10 mm x 10 mm) plates. This applicator is shown in Fig. 6.3. The pair of 10 mm^2 electrodes produced a uniform electric field across the bulk tissue [9].

The vernier calliper provided a means to measure the thickness of bulk tissue (d) to enable the electric field to be determined. The coaxial cable delivering the pulsed fields to the electrodes is an RG214 50 Ω cable.

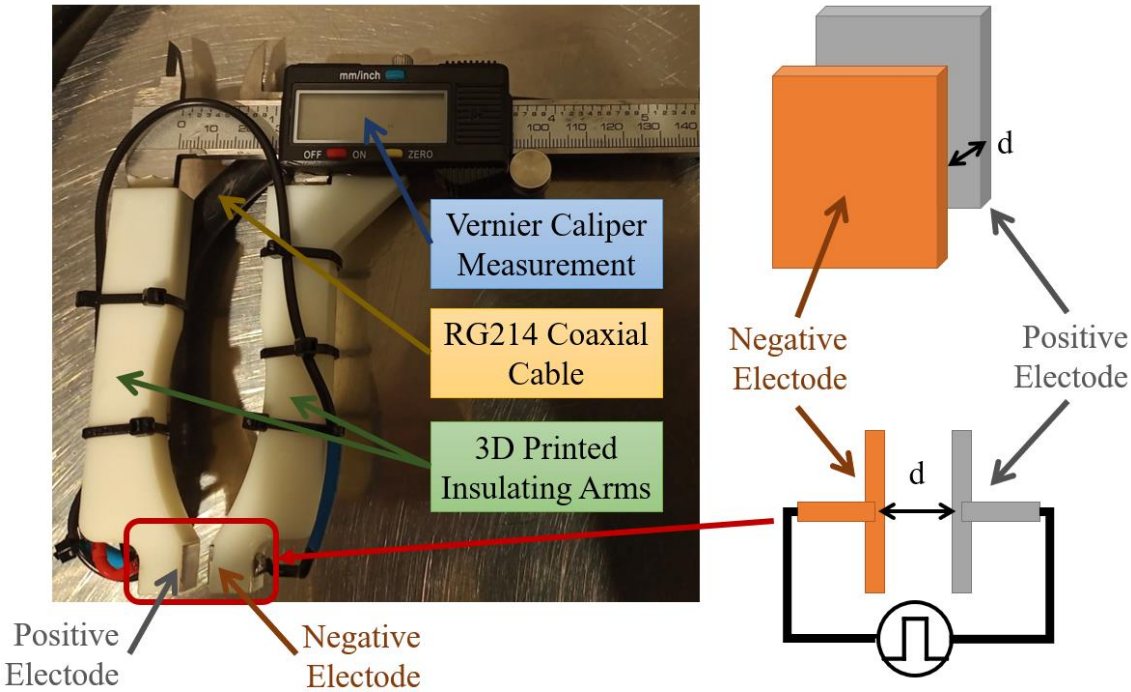


Fig. 6.3. Parallel plate vernier calliper applicator/device

6.2.3. Histology

Histology was carried out to determine if the composition and structure of collagen and cellular effects within the liver differ after exposure to the nsPEFs. The aim of this was to support the hypothesis that nanosecond pulsed electric fields produce a superior clinical outcome.

One tissue sample from each of the ten liver sites was used to produce a stained histology section slide. One section of each tissue was stained with Haematoxylin and Eosin and an additional section was stained with Picro-Sirius Red combined with Millers Elastin stain [8],[10].

All sections were scanned in their entirety and comments on any features of interest were noted and documented with representative photomicrography. This was then used to determine if the effect

of the applied pulses is irreversible, if any permanent cellular changes within liver tissue are observed, and the tolerance borders of the nsPEF delivered by the parallel plate applicator. Morphological and collagen/thermal effects of the nsPEF on liver tissue could also be determined [8],[10].

To appreciate the microscopic effects of the energy delivery it is important to consider a normal section of tissue as a control sample, which was the tenth site used in this pre-clinical, i.e., the tenth site was a control site where no nsPEF energy was applied [10].

For this section, Haematoxylin & Eosin stain will be referred to as H&E and Picro Sirius Red and Miller's Elastin as PicMill. Haematoxylin stains the nuclei blue whilst Eosin stains the cytoplasm and surrounding cellular matrix pink. This allows for an in-depth analysis of the cellular morphology of the tissue and its reaction to the wound creation, coagulation and subsequent healing. Viewing the PicMill slides under polarised light causes birefringence of the collagen within the structure allowing for the analysis of the cellular structure. This also allows commentary on whether the energy delivery has altered this structure.

6.3. Effect of nsPEF on *In-vivo* Bulk Tissue

Classical electroporation is the application of controlled pulsed electric fields of around 100 µs pulse widths. This is now in use to perform a number of clinical procedures that have been approved and guidelines have been written by the National Institute for Health & Care Excellence (NICE) to endorse pulsed electric fields as a treatment of choice. The current clinical use of classical electroporation consists of two forms of treatment; irreversible electroporation (IRE) [12]-[25] and Electrochemotherapy (ECT) [26]-[31]. Where ECT is the combination of reversible electroporation with ionising or chemotherapy. The pulsed electric field treatment predominately consists of the following 100 µs pulsed electric field parameters.

The intent of the preclinical is to deliver enough energy to produce IRE and ECT and steadily reduced this energy until no histological/cellular changes are observed. For simplification, it assumed that for a 240 ns pulsed electric field (PEF), with identical repetition frequency and electric field strength, it would require a total of 3,333 and 333,333, 240 ns pulses to achieve ECT and IRE respectively. The associated application time for delivering 3,333 and 33,3333 PEF of 240ns, with a repetition frequency (rate) of 50 Hz (20 ms), would be 67 seconds and 11 minutes and 11 seconds respectively.

Table 6.2. shows the nsPEF parameters that were applied to each liver site. Pulsed electric fields of 248 ns in duration were applied to nine liver sites. The tenth site was a control site, where no energy was applied.

In sites one to six, the fast nsPEF electroporation system delivered a set number of 248 ns width pulsed electric fields at a repetition rate of 20 ms (50 Hz) with an amplitude in excess of 1 kV. At these sites, the electroporation system delivered the nsPEFs when triggered using the 'Quantum Composers 9520 Series Pulse Generator [34]'. For liver sites seven to nine, the fast nsPEF electroporation system was operating in its 'continuous operation' state, indicated by '*' in Table 6.1, where no trigger pulses were required.

Table 6.1. Pulsed electric field parameters for irreversible electroporation and electrochemotherapy clinical application [12]-[31]

Clinical Application	Pulse Duration, t (µs)	Number of Pulses, N	Repetition Rate, *f* (Hz)	Electric field Strength, E (V/mm)	Total on-time of energy delivered, t_{on}
ECT	100	8	1 to 10,000	40 to 100	800 µs
IRE	100	80	1 to 10,000	150 +	8 ms

The 'continuous operation' state occurs when the output from the FS40 high voltage power supply unit (and therefore the voltage within the charged line) is equivalent to the total collector-emitter breakdown voltage (nBV_{CES}) of the ten stacked avalanche transistors operating as the fast-switching element. In this configuration 10 x 320 V = 3200V. This continuous generation of nsPEF continues until the voltage level across the charged line is below the total collector-emitter breakdown voltage (nBV_{CES}) of the stacked avalanche transistors. The repetition frequency of the continuous nsPEF is equivalent to the charging time of the coaxial line through the 1 MΩ resistor. Therefore, the nsPEFs are generated in a repeatable manner at a repetition rate of 5 ms (200 Hz). It is estimated that 200 pulses were generated by the fast nsPEF electroporation system per second under 'continuous operation' mode.

The application time is when the pulses are applied to the tissue and when the voltage level across the charged line is equivalent to the total collector-emitter breakdown voltage of the stacked transistor switch. The estimated number of pulses applied to each site under this 'continuous operation' can be calculated as:

$$N = f\ t_{on} = 200\ t_{on} \tag{6.1}$$

where N is the estimated number of pulses delivered to sites seven to nine, f is the associated charging frequency of the charged line (in this case 200 Hz), and t_{on} is the application time of the pulsed fields. The number of nanosecond pulsed electric fields that were estimated are given in Table 6.2 and indicated by '*'.

The values indicated by '+' in Table 6.2 does not consider the potential energy and heat loss within the bulk liver tissue load due to natural heat dissipation within the tissue structure and the 'cooldown', or time interval between each applied pulse. The parameters presented here were calculated by evaluating the reflected voltage associated with the incident pulse, as shown in Fig. 6.6. The estimated energy delivered, and increased temperature experienced at each site is the estimated maximum values.

Table 6.2. Nanosecond pulsed electric field parameters applied to each liver site and calculated mean power and maximum energy delivered and calculated max mean rate temperature rise [32]-[33]

Site number	Number of nsPEF, N	nsPEF duration, t (ns)	Repetition Rate (ms)	Pulse Amplitude, V (V)	distance between parallel plates, d (mm)	Electric Field, E (V/mm)	Estimated Load Impedance, Z_L (Ω)	Mean Power Delivered, P (mW)	Maximum Energy Delivered, E_n (J)	Max mean rate of temperature rise (K/second)
1	500	248	20 (50 Hz)	1100	5.00	220.00	122	248	2.5^+	0.135^+
2	1,000	248	20 (50 Hz)	1100	5.01	219.56	122	248	5.0^+	0.135^+
3	2,500	248	20 (50 Hz)	1160	5.01	231.54	126	272	13.6^+	0.148^+
4	5,000	248	20 (50 Hz)	1200	4.98	240.96	150	268	26.8^+	0.146^+
5	10,000	248	20 (50 Hz)	1140	4.97	229.38	154	239	47.8^+	0.131^+
6	500	248	20 (50 Hz)	1220	4.95	246.46	115	312	3.2^+	0.172^+
7*	4,000*	248	5 (200 Hz) *	1460	4.93	296.15	128	1708	34.2^+	0.944^+
8*	8,000*	248	5 (200 Hz) *	1560	4.93	316.43	140	1871	74.9^+	1.033^+
9*	5,000*	248	5 (200 Hz) *	1620	4.93	328.60	148	1969	49.3^+	1.087^+
10	0	0	0	0	4.92	0.00	N/A	0.00	0.00^+	0.00^+

For site number seven the fast nsPEF electroporation system was activated for 20 seconds. As the delay line has a charging frequency of 200 Hz (200 pulses per second) an estimated 4,000 pulses were delivered by the system into this site ($N=f\ t_{on}=200 \times 20=4{,}000$ pulses). For site number eight the system was activated for 40 seconds thus an estimated 8,000 pulses were delivered by the system into this site. For site number nine the system was activated for 25 seconds, thus an estimated 5,000 pulses were delivered by the system into this site.

The amplitude of the nsPEFs delivered into liver sites seven to nine, is higher than that for sites one to six, as the fast nsPEF electroporation system is operating in its 'continuous operation' mode. In the 'continuous operation' mode ($V_{CCmax} = nBV_{CES}$) the voltage across the charged line is higher than in normal operation ($nBV_{CEO} < V_{CC} > nBV_{CES}$). Therefore, the amplitude of the nsPEF, is s higher when the system operates in its 'continuous operation' mode than in normal operation mode.

The estimated electric field (6.2), load impedance (6.3), mean power (6.5) and energy delivered (6.6), and the mean rate of temperature rise (6.7) were calculated from knowing the distance between the electrode plate structure and the nsPEF parameters form the measured waveform captured by the oscilloscope and high voltage probe.

The electric field, E, applied is calculated by (6.2).

$$E = \frac{V}{d} \tag{6.2}$$

where V is the amplitude of the incident pulse and d is the distance between the two plate or thickness of the bulk tissue.

The estimated impedance of the bulk tissue, or load Z_L, was calculated by equation (6.3).

$$Z_L = \frac{\Gamma Z_0 + Z_0}{1 - \Gamma} \tag{6.3}$$

where Z_0 is the impedance of the charged line, which is 50 Ω for the RG214 coaxial cable, and Γ is the reflection coefficient. The reflection coefficient is calculated in (6.4). The reflection coefficient is calculated from the amplitude of the incident nsPEF (forward signal), V^+, and the amplitude of the secondary pulse (reflected signal), V^-, as shown in equation (6.4). These figure where given by the captured nsPEF waveform across the load from the generator standpoint by utilising the oscilloscope and high voltage probe. The example of how the values V^+ and V^- are found from the captured waveform is shown in Fig. 6.5.

$$\Gamma = \frac{V^-}{V^+} \tag{6.4}$$

where V^- is the amplitude of the secondary nsPEF (reflected signal) and V^+ is the amplitude of the incident nsPEF (forward signal) from the applied pulse from the fast nsPEF electroporation system.

The mean power can be calculated by (6.5)

$$\bar{P} = PD \tag{6.5}$$

where the mean power, $\bar{P}$, is the power supplied to the bulk tissue load by the nsPEF produced by the fast nsPEF electroporation system. P is the DC Power $\left(P = \frac{V^{+2}}{Z_0}(1 - \Gamma^2)\right)$ by knowing the amplitude of the incident pulse and the characterise impact of the charged line. And D is the duty cycle $\left(D = \frac{t}{T} = tf\right)$ that determined by the timing characterises of the nsPEF delivered.

where V^+ is the amplitude of the incident nsPEF (forward signal), Z_0 is the impedance of the charged line, Γ is the reflection coefficient of the system, t is the nsPEF duration, and T is the repetition rate or *f* the repetition frequency of the nsPEFs.

The total energy delivered into the bulk tissue from the 248 ns PEF delivered from the fast nsPEF electroporation system can be derived by the below equation

$$E_n = NPt \tag{6.6}$$

Where E_n is the energy delivered, N is the number of PEF applied, P is the DC Power and t is the pulse duration of the nsPEF (248 ns).

Finally, the mean rate of the temperature elevation the bulk tissue experiences, ΔT_{Max}, can be calculated using (6.7). This equation provides an estimate of the temperature increase experienced by the bulk tissue per second (K/second or °C/second).

$$\Delta T_{Max} = \frac{\Delta T}{T} = \frac{E_n}{cm\,T} = \frac{E_n}{c\,\rho vol\,T} = \frac{E_n}{c\,\rho\,A\,d\,T} \tag{6.7}$$

where ΔT is the temperature rise per pulse $\left(\Delta T = \frac{E_n}{cmT}\right)$ without considering temperature loss due to natural dissipation. E_n is the energy delivered into the tissue, and T is the repetition rate of the nsPEFs. The heat capacity (cm) is the mass (m) multiplied by the specific heat capacity (c) of the liver or other bulk tissue load.

The specific heat capacity, c, of the liver is 3.6 J/g/K [35]-[36]. The mass of the liver where the nsPEFs are applied can be calculated by knowing the volume (*vol*) of the bulk tissue and the density (ρ) of liver. The mass, m, of each site can be calculated by knowing the volume, *vol*, and density, ρ, of the liver. $m = \rho\, vol$. The density (ρ) of the liver is approximately 1.02 g/cc [37]-[38]. The average heat capacity (cm) was found to be approximately 1.82 J/K.

The volume, *vol*, of the liver load can be estimated by multiplying the application area (A) and the thickness of the bulk tissue (d) ($vol = A\,d$). The application area, A is 100 mm^2, the area of the parallel plate applicator (10 mm x 10 mm) and d is the liver thickness. The thickness (d) for each site is shown in Table 6.2.

6.4. Histology Result

The fast nsPEF electroporation system and associated device were able to induce irreversible (and possibly reversible) electroporation. This is based on the observed cellular changes within liver tissue. The electroporated cellular features were well demarcated from normal tissue, within close tolerance margins that relate directly to the sites where the instrument was positioned. Morphologically, the effect of treatment is limited to cells, and the collagen within the treated areas is unchanged from normal.

The result from the pre-clinical can be summarised as follows [8], [10], [32]:

1) All histopathological features of irreversible electroporation were seen in six out of the ten samples;

2) The effects were consistent throughout the samples in terms of cellular compromise;
3) The breaching of the cytoplasmic membranes of cells within the planned treatment areas was obvious with the loss of integrity of those cells from the time of energy application;
4) The treatment effects were restricted to the treatment application areas;
5) There was no other collagen effect detected in any of the treated areas;
6) There was no detectable heat-associated effect on collagen in any of the areas of tissue showing cellular compromise. This indicates a non-thermal treatment method;
7) No apparent changes were observed on the subject's ECG recording;
8) No substantial and noticeable contractions and tightening/spasming of the subject muscles were observed;

The detailed report on the histological effects and the overall performance of the fast nsPEF electroporation system are detailed in the histopathology study report [32]-[33].

6.4.1. Control Site, Site Number 10

The micrographs shown in Fig. 6.4. were taken from the control site where the electroporation device clamp was placed in a position associated with the edge of the liver lobe. The tissue section examined here includes the full thickness of this control area where the clamp was applied. In the control case, the device clamps were placed into the liver at the same tension as in the treatment sites, but no energy was activated, as shown in Fig. 6.6.

These micrographs show histologically normal tissue with no recognizable cellular changes or tissue alterations. The number and the distance of cells and the collagen present within the interlobular septae showed normal morphology and normal bi-refringence. The H&E stained and associated PicMill slides for the control site, site ten are shown in Fig. 6.4.

6.4.2. Site Number 8

Fig. 6.6 indicates the nsPEFs that were delivered into site eight resulted in the most positive histological outcome. The highest energy delivery was associated with this site. Additionally, the nsPEFs that were measured across a 50 Ω load and control (site 10) are shown in Fig. 6.5 for comparison.

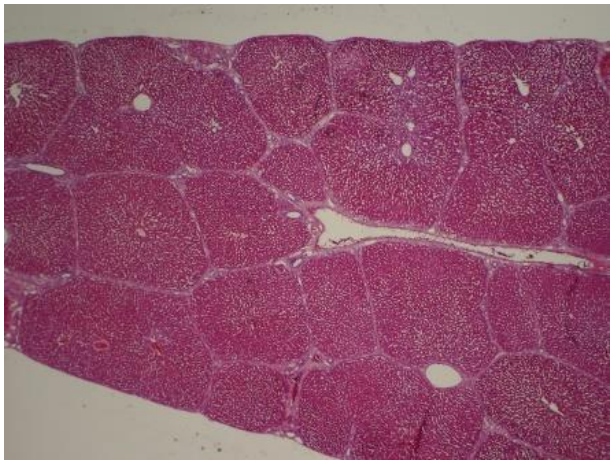


Fig 6.4(a). Liver Control, Site 10, H&E x20

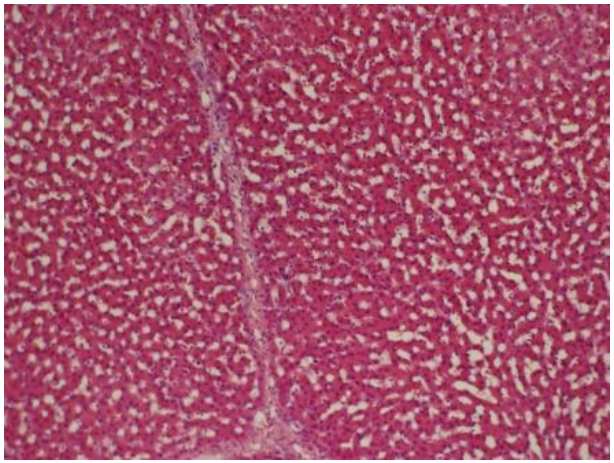


Fig 6.4(c). Liver Control, Site 10, H&E x100

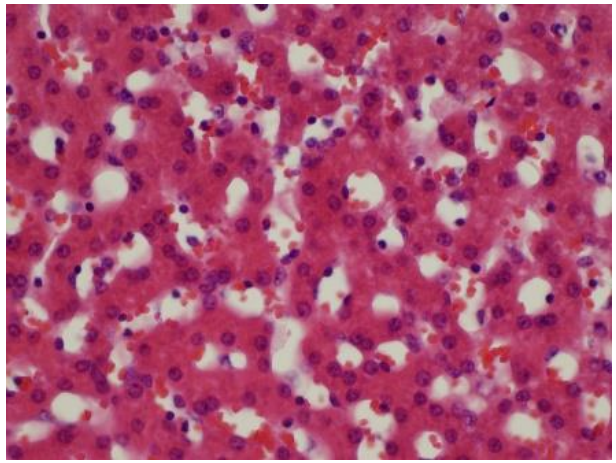


Fig 6.4(e). Liver Control, Site 10, H&E x400

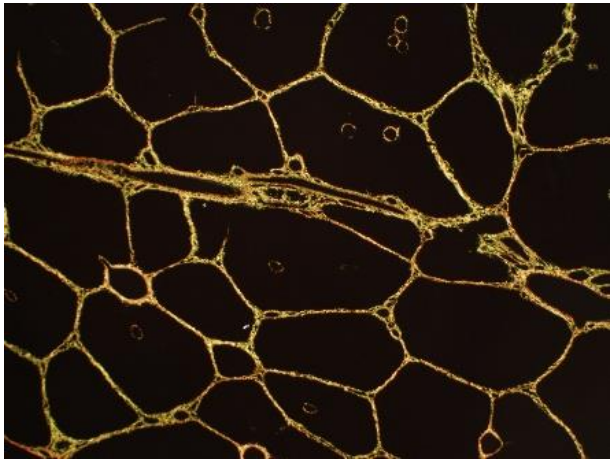


Fig 6.4(b). Liver Control, Site 10, PicMill x20 pol

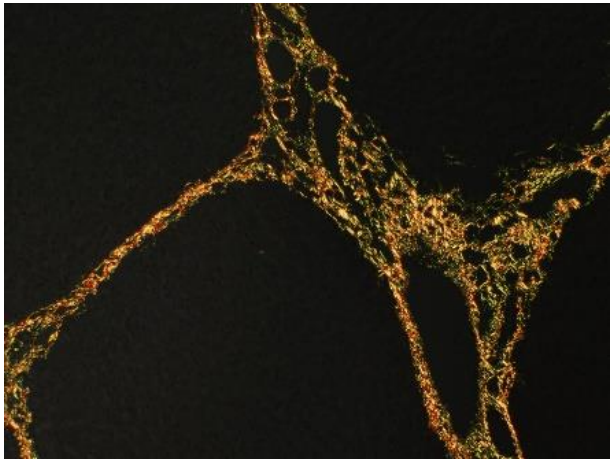


Fig 6.4(d). Liver Control, Site 10, PicMill x100 pol

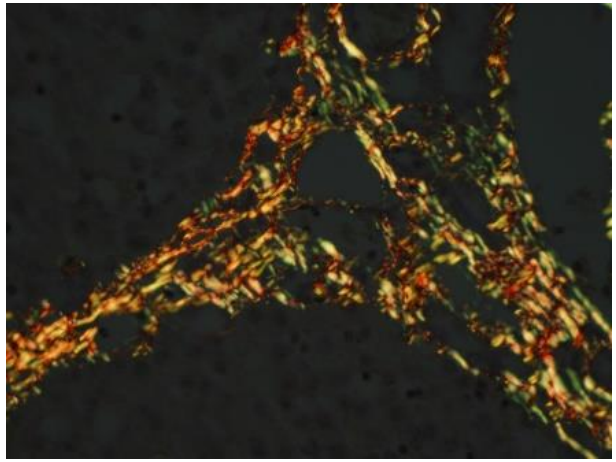


Fig 6.4(f). Liver Control, Site 10, PicMill x400 pol

The voltage across the 50 Ω load, shown in Fig. 6.6, has minimum reflection since the 50 Ω load impedance (Z_L) matches the 50 Ω impedance of the charged line (Z_0), which results in a system reflection coefficient of approximately 0. In comparison, the voltage across the liver had a reflection since $Z_0 \neq Z_L$.

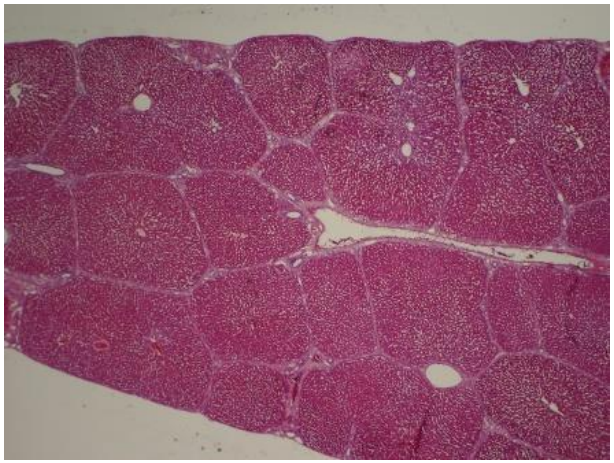


Fig 6.5(a). Liver Control, Site ten, H&E x20

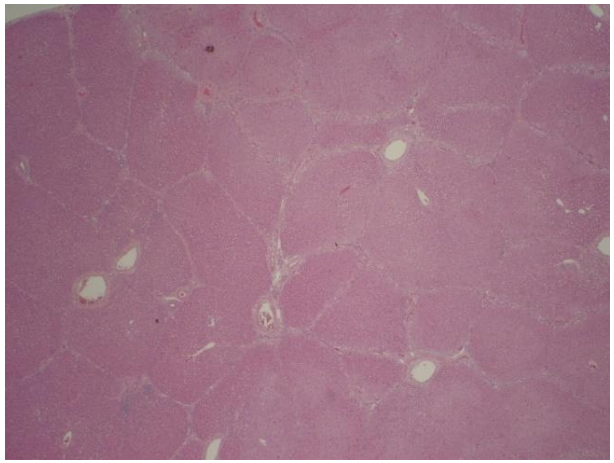


Fig.6.5(c). Liver nsPEF Treated, Site eight, H&E x20

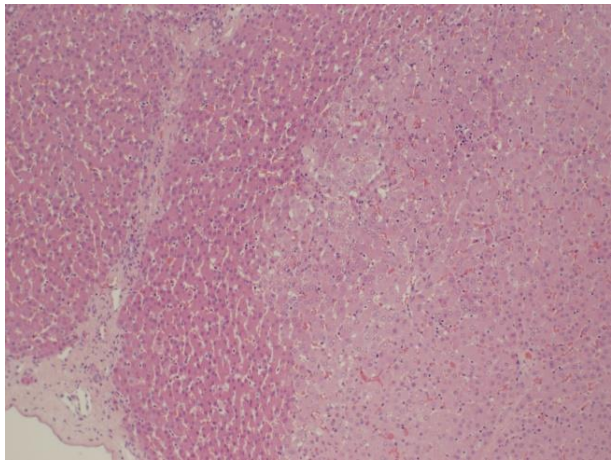


Fig.6.5(e). Liver nsPEF Treated, Site eight, H&E x400

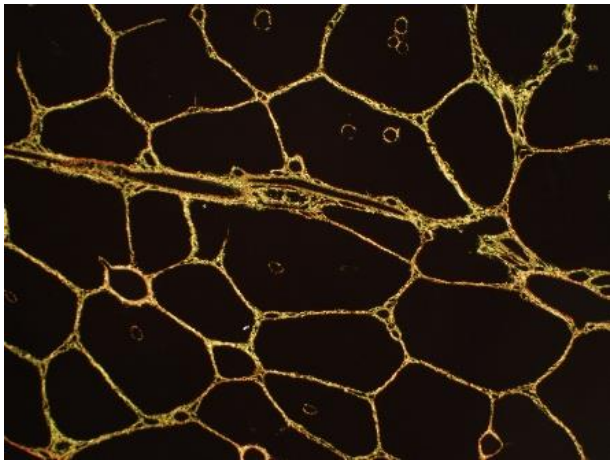


Fig 6.5(b). Liver Control, Site ten, PicMill x20 pol

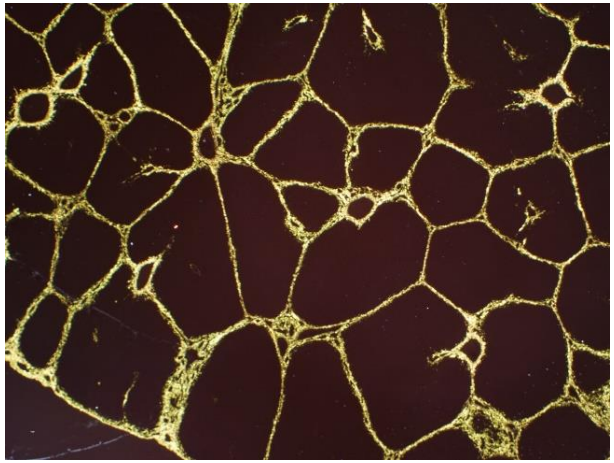


Fig.6.5(d). Liver nsPEF Treated, Site eight, PicMill x20 pol

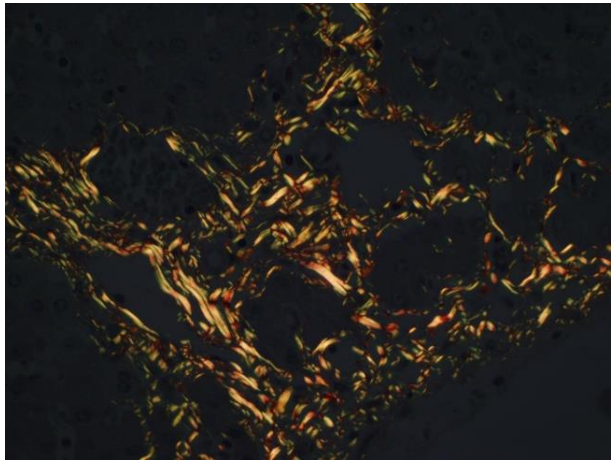


Fig.6.5(f). Liver nsPEF Treated, Site eight, PicMill x400 pol

Considering site number eight, 8,000 pulses of 248 ns in duration, with an incident pulse amplitude (V^+) of 1,560 V, at a repetition rate of 5 ms (200 Hz) were applied over a period of 40 seconds. This implies that an electric field of 316 V/mm was applied across the 4.93 mm thick liver site.

Since the incident voltage is 1,560 V, and the reflected secondary voltage is 740 V, the reflection coefficient is 0.47. The forward (V^+) and reflected (V^-) voltages of the nsPEF applied at site eight are shown in Fig. 6.6. This reflection coefficient suggests that the impedance of the tissue at this site is 138.6 Ω and an estimated 74.8 J of energy was delivered into the tissue. From this, we can say that the bulk tissue experiences a temperature increase of 1 °C/s. This figure does not consider the expected heat dissipation during the time interval between each applied pulse. This calculation, in addition to the histological, results indicates that the application of the nsPEFs produces a non-thermal effect.

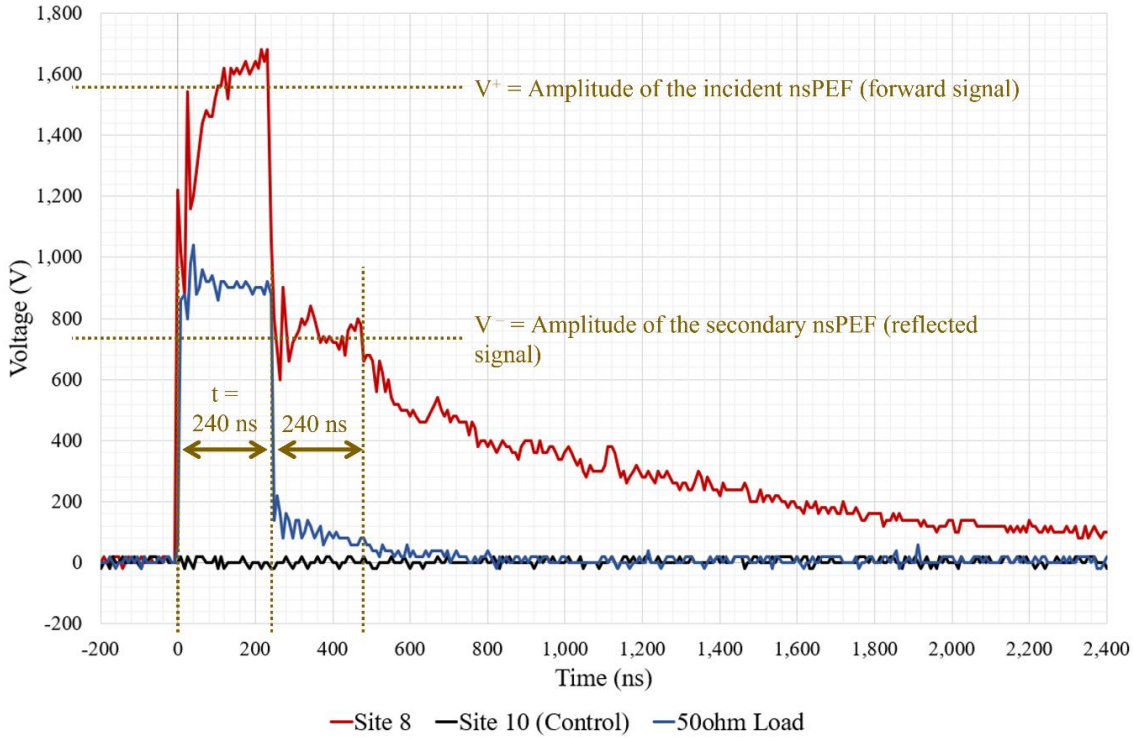


Fig. 6.6. Pulsed electric field applied to sites eight (in 'continuous operation' mode), control site ten and across a 50 Ω load impedance.

It should be noted that the energy applied at this site is larger than any energy applied at other tissue sites. Although the number of pulses delivered at this site, (8,000) is not as high as the 10,000, 248 ns pulses delivered at site five, the amplitude is higher and the time interval between each applied pulse is shorter for site eight than for site five.

The histological sections or micrographs shown in Fig. 6.5 compare the cellular content and the collagen matrix on the liver with and without exposure to the nsPEFs. Fig. 6.5 and Fig. 6.7 show that the affected areas are well-defined. The cells in the treated areas show well-known features of irreversible electroporation, including cytoplasmic membrane disruption resulting in loss of cytoplasmic organelles, loss of integrity of the cytoplasmic structure, some changes to the nuclear definition, alteration of the density of nuclear chromatin, and loss of all cellular separation. The effects were seen through the entire depth of the liver processed between the two plates of the applicator. This suggests that the instrument as configured for the applications in this study would be capable of

irreversibly electroporating a tumour of around 1.0 ml to 1.5 ml in volume. There was no effect detectable on the collagen structures in the treated area [8],[10],[32]. This is shown by comparing the PicMill slides at the control site in Fig. 6.5(b) and the PicMill slide at site eight in Fig. 6.5(d) and Fig. 6.5(f).

6.4.3. Cellular And Collagen Effects

The electroporated cellular features were well demarcated from normal tissue, within close tolerance borders and related directly to the instrument application sites, as shown in Fig. 6.7. The electroporated site is lighter in colour with 'empty' nuclei features. The cellular effect is seen as a loss of cytoplasmic staining and "amalgamation" of cytoplasmic contents. Cytoplasmic membranes are not easily seen and outlining between cells is difficult to identify. Additionally, many nuclei show decreased nuclear content, but without detectable nuclear membrane alteration. The remaining content within these nuclei is appropriately stained and is appropriately in situ. This is illustrated in Fig. 6.7 [8], [10], [32]. The associated cellular changes in the nuclei cells strongly suggest that an irreversible electroporation effect has occurred and that morphologically, the effect of treatment is limited to cells. The nuclei of some cells were unchanged, yet they could have experienced reversible electroporation, as shown in Fig. 6.7(c).

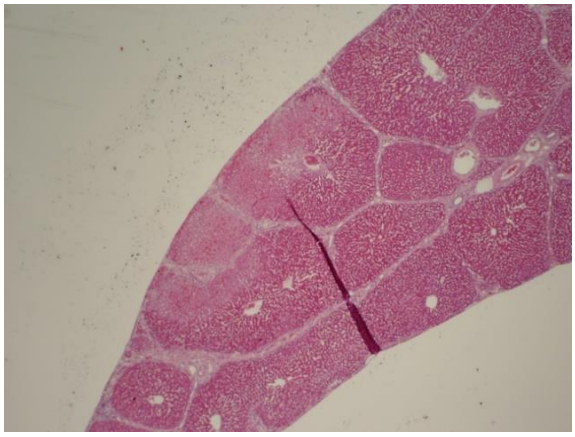


Fig. 6.7(a) Liver Treated H&E x20 [11] slide: P00177-01

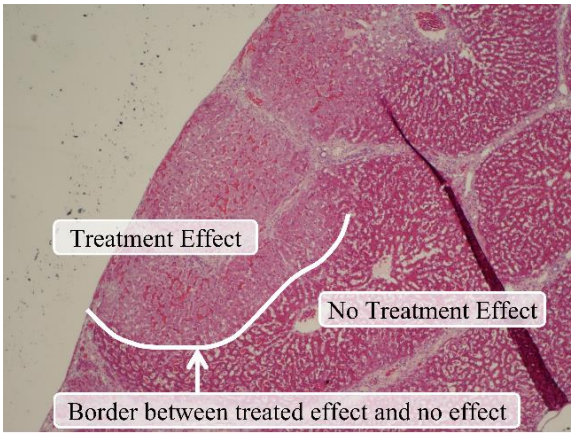
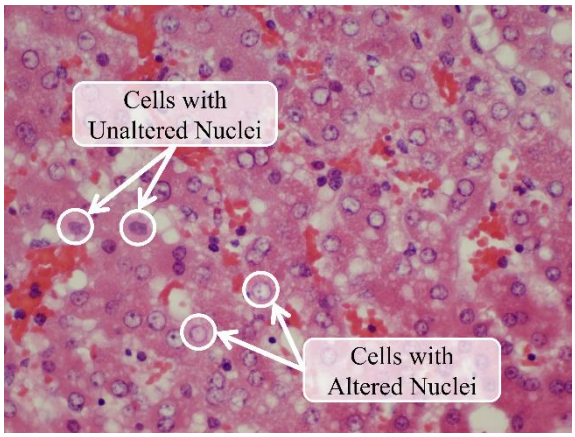


Fig. 6.7(b) Liver Treated H&E x40 [11] slide: P00177-01



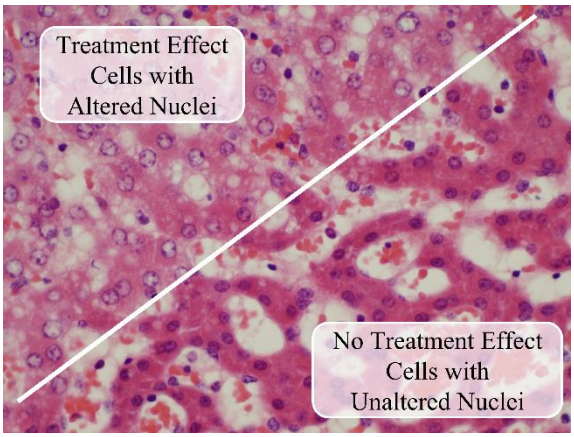


Fig. 6.7(c). Liver Treated H&E x400 [11] slide: P00177-01

The cellular effect is seen as a loss of cytoplasmic staining and "amalgamation" of cytoplasmic contents. Cytoplasmic membranes are not easily seen, and delineation between cells is difficult to identify. Additionally, many nuclei show decreased nuclear content but without detectable nuclear membrane alteration. The remaining content within these nuclei is appropriately stained and is appropriately in situ. There was no effect detectable on the collagen structures anywhere in the treated area. These features are shown in Fig. 6.6 and Table 6.4 [8], [10], [32].

6.4.4. Nanosecond vs Microsecond Pulsed Electric Fields

During the pre-clinical, there were no clinically relevant changes observed on the subject's ECG recording. A change of three beats was observed in the subject's heart rate during the whole nanosecond electroporation investigation. The changes observed in the subject's ECG status were less during this investigation than was observed in an endoscopic procedure investigation that was conducted on the same subject before this nanosecond electroporation investigation [8].

A literature review performed to look at current products on the market in the field of classical electroporation, using µsPEFs highlighted the need to synchronise the pulses with the patient's heart rate. Classical electroporation requires synchronisation with the patient/subject as the pulses can affect the patient's cardiac rhythm (arrhythmia) [39]-[41]. This is because the electroporation threshold associated with 100 µs PEF is larger than the electrostatic threshold of a human body. The electroporation threshold is when the induced membrane voltage is exceeded due to electric stimulation (electric field magnitude exceeds a threshold, $|\vec{E}| > E_{Th_{EP}} \rightarrow EP$). While electrical stimulation is the artificial triggering of action potentials by the delivery of the electrical stimulation (when the gradient of electric field magnitude exceeds a threshold, $\frac{\partial|\vec{E}|}{\partial\tau} > E_{Th_{ES}} \rightarrow E$) [39]-[43]. The need for synchronisation is eliminated with the application of nsPEFs due to the threshold associated with nanosecond electroporation is shorter than the electrostatic threshold of a human body due to the shorter pulse widths and higher frequency associated with nsPEFs in comparison to µsPEFs [39]-[43].

No noticeable contractions and tightening, or spasming, of the subject muscles were observed using nanosecond pulses. Muscle spasm has been observed through the application of conventional electroporation, and the patient normally requires muscle relaxant even, when under general anaesthesia [39]-[43]. This indicates another advantage of nsPEFs in comparison to µsPEFs as a clinical procedure.

6.4.5. Nanosecond Pulsed Electric Fields vs Microwave Energy

A comparison study was performed to compare non-thermal nanosecond pulsed field ablation to the application of 5.8 GHz microwave energy, using a Creo Medical thermal ablation device, compromising of a monopole antenna tunned to deliver microwave energy into biological tissue at 5.8 GHz over a

broad range of tissue impedances. The effects from this device include cellular coagulation, and collagen degradation beyond the ablation area, in addition to some extravasation effect that defines the edge of the energy dissipation effects [44]-[45].

Table 6.3. Collagen effect comparison between nanosecond pulsed electric field and microwave energy

Liver Control Study Report: 210323 EP1 (Site 2) [11]	248 ns pulsed electric field Study Report: EP4 (Site 8) [11]	5.8 GHz Microwave Energy, Study Report: 200716 monopolar antenna [44]	5.8 GHz Microwave Energy. Study Report: 22.02 Creo Strasbourg (Site 39 and 42) [45]

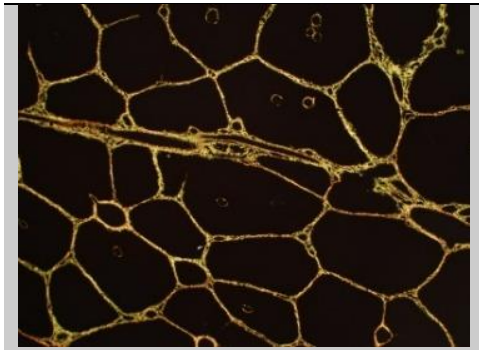
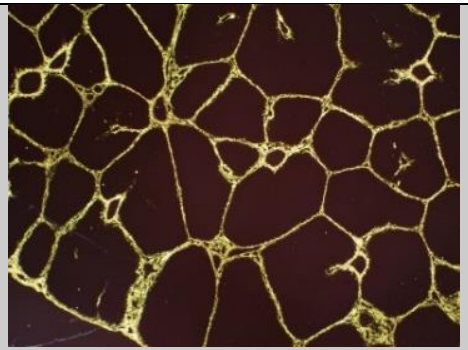
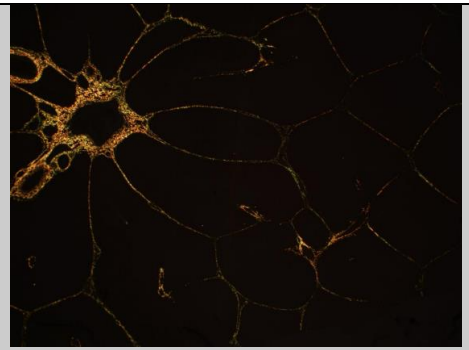
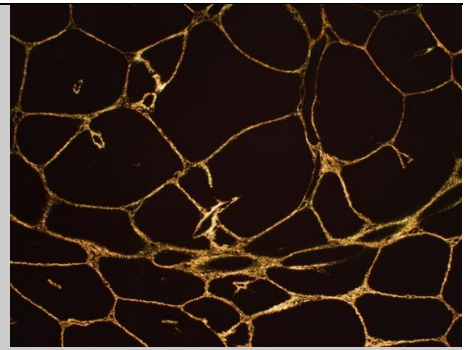

			

Fig. 6.8(a). PicMill x20 pol	Fig. 6.9(a). PicMill x20 pol	Fig. 6.10(a). PicMill x20 pol	Fig. 6.11(a). Site: 39, PicMill x20 pol

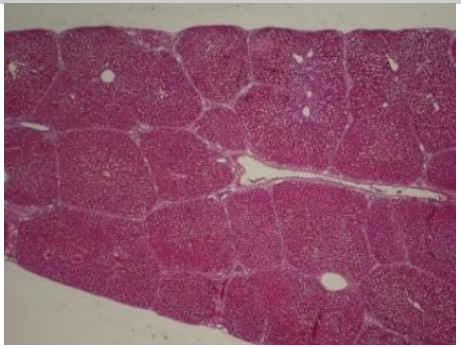
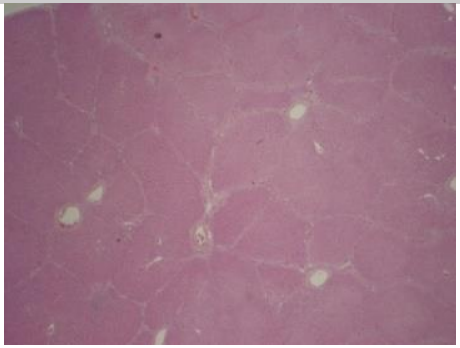
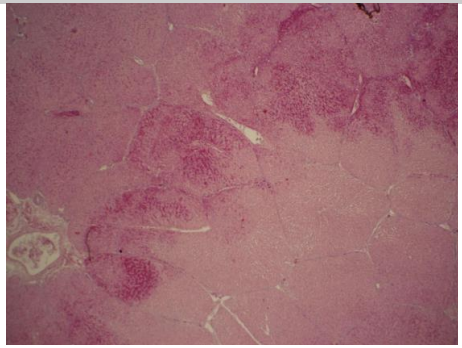
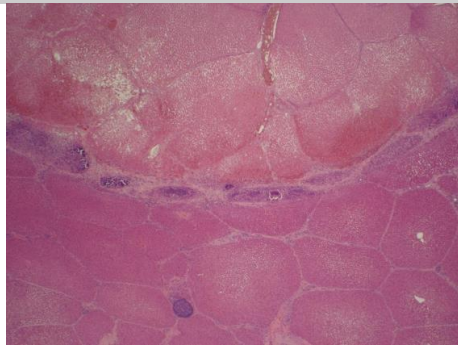

			

Fig. 6.8(b). H&E x20	Fig. 6.9(b). H&E x20	Fig. 6.10(b). H&E x20	Fig. 6.11(b). Site: 39, H&E x20

With the application of sufficient nsPEF energy, morphologically speaking, the effect of nsPEFs is limited to cells and the effect was demarcated from normal tissue within close tolerance borders and related directly to the position of the parallel plate applicator. Concerning the effect of the energy on Collagen, microwave energy degrades collagen, whilst the collagen within the area treated using nsPEFs was unchanged from the normal [44]-[45].

Table 6.3. Collagen effect comparison between nsPEF and microwave energy

Liver Control Study Report: 210323 EP1 (Site 2) [11]	248 ns pulsed electric field Study Report: EP4 (Site 8) [11]	5.8 GHz Microwave Energy, Study Report: 200716 monopolar antenna [44]	5.8 GHz Microwave Energy. Study Report: 22.02 Creo Strasbourg (Site 39 and 42) [45]

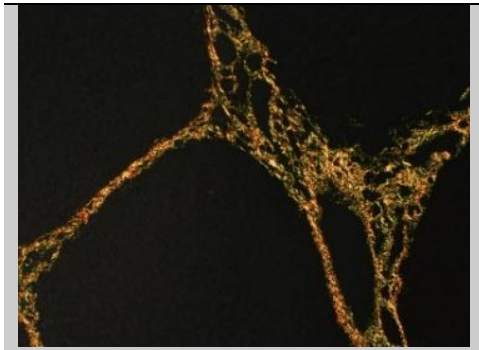
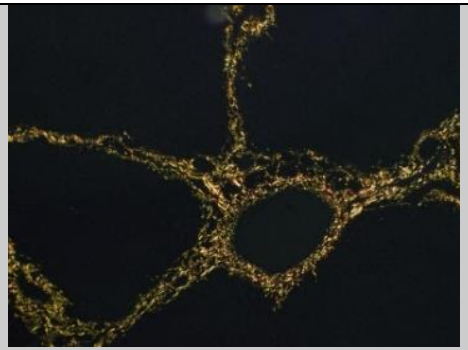
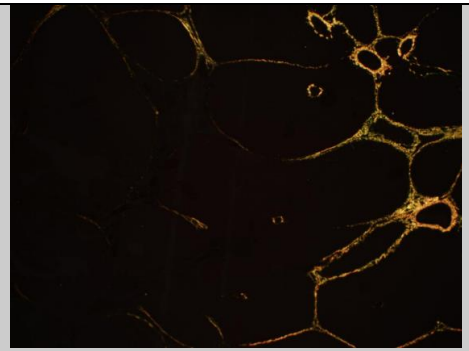
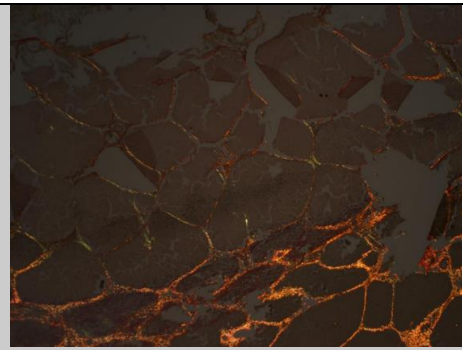

			

Fig. 6.8(c). PicMill x100 pol	Fig. 6.9(c). PicMill x100 pol	Fig. 6.10(c). PicMill x20 pol	Fig. 6.11(c). Site: 42, PicMill x20 pol

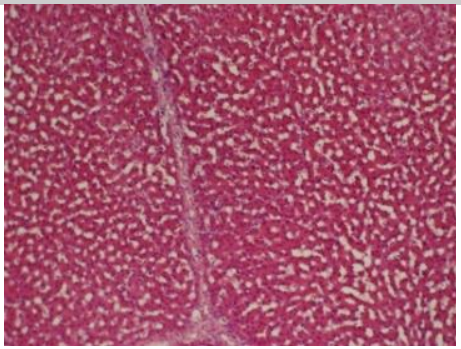
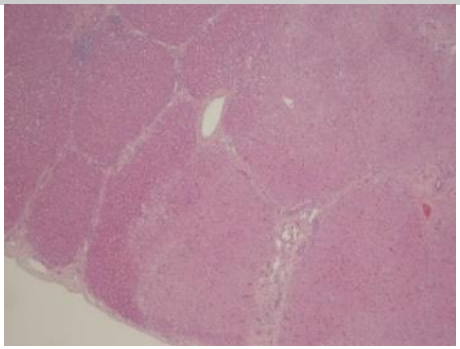
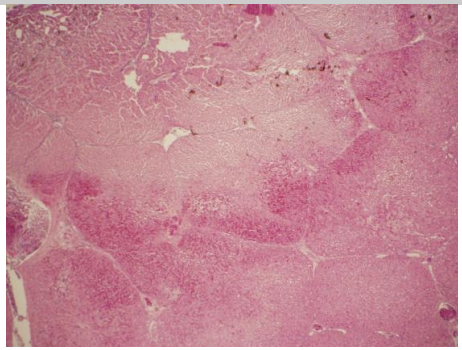
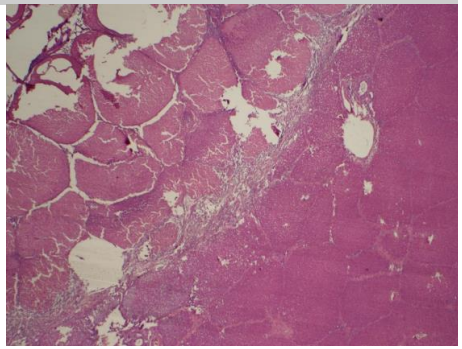

			

Fig. 6.8(d). H&E x100	Fig. 6.9(d). H&E x40	Fig. 6.10(d). H&E x20	Fig. 6.11(d). Site: 42, H&E x20

These findings indicate that affected cells are limited to the area of the applicator and so it can be said that nsPEFs produce precise non-thermal tissue effects. This conclusion is illustrated by comparing the collagen (PicMil slides) and cellular (H&E slides) micrographs given in Table 6.3 and Table 6.4. The

PicMil or collagen images for control shown in Fig. 6.8 are indistinguishable from the PicMil, or collagen micrographs shown in Fig. 6.9 following exposure of the nsPEFs to the *in-vivo* live model. Fig. 6.10 and Fig. 6.11 in Table 6.3 show the degradation of collagen following exposure to thermal microwave energy.

Table 6.4. Comparison effect of nsPEF Energy vs Microwave Energy on Liver

Observations and effects	270 ns pulsed electric field with parallel plates applicator	5.8 GHz Microwave with Creo Medicals monopolar antenna
Collagen	Collagen within the treated areas is unchanged from normal	Degradation and ablation (Minor loss of brightness in the sections viewed using polarised light)
Cellular Changes	Morphologically, the effect of treatment is limited to cells.	Cellular coagulation and collagen alteration
Treatment Effect	Cellular features were well demarcated from normal tissue, within close tolerance borders and related directly to the instrument application sites.	Deep margins of the ablation effect that expands further than the application site. Some extravasation defining the edge of the energy dissipation effects
Thermal Effect	Non-thermal. Treated area temperature does not rise above body temperature (37 °C)	Thermal Treated area temperature rises above body temperature (37 °C) to at least 46 °C

6.5. Pulsed Electric Field Delivery into Bulk Tissue

The fast nsPEF electroporation system developed in this work delivered pulses of 248 ns duration, with amplitudes in excess of 1 kV to each liver site.

Fig. 6.12 and Fig. 6.13 show the nsPEFs delivered into each site using the fast nsPEF electroporation system in its normal and ‘continuous operation’ mode respectively. The profile of the nsPEFs delivered into each liver site was identical. This suggests the fast nsPEF electroporation system can deliver consistent nsPEFs into bulk tissue.

The amplitude of the nsPEFs delivered into the bulk tissue was larger when the system was operating in its ‘continuous operation’ mode, i.e., 1.5 kV (as shown in Fig. 6.13), compared to 1.1 kV nsPEF amplitude (as seen in Fig. 6.12) when the system was operating in its normal mode of operation where the unit is externally triggered. This is because of the higher voltage across the charged line (V_{CC}) required to operate the system in its ‘continuous operation’ mode. In the ‘continuous operation’ mode $V_{CC} = nBV_{CES}$ while the voltage across the charged line in normal operation is between the two total collector-emitter voltage values i.e., $nBV_{CEO} < V_{CC} > nBV_{CES}$.

Taking into account the reflection of the incident 248 ns pulses, it is possible to estimate the mean power and energy delivered, the increase in temperature of the bulk tissue and the impedance of the bulk liver tissue. The results from this analysis are given in Table 6.2.

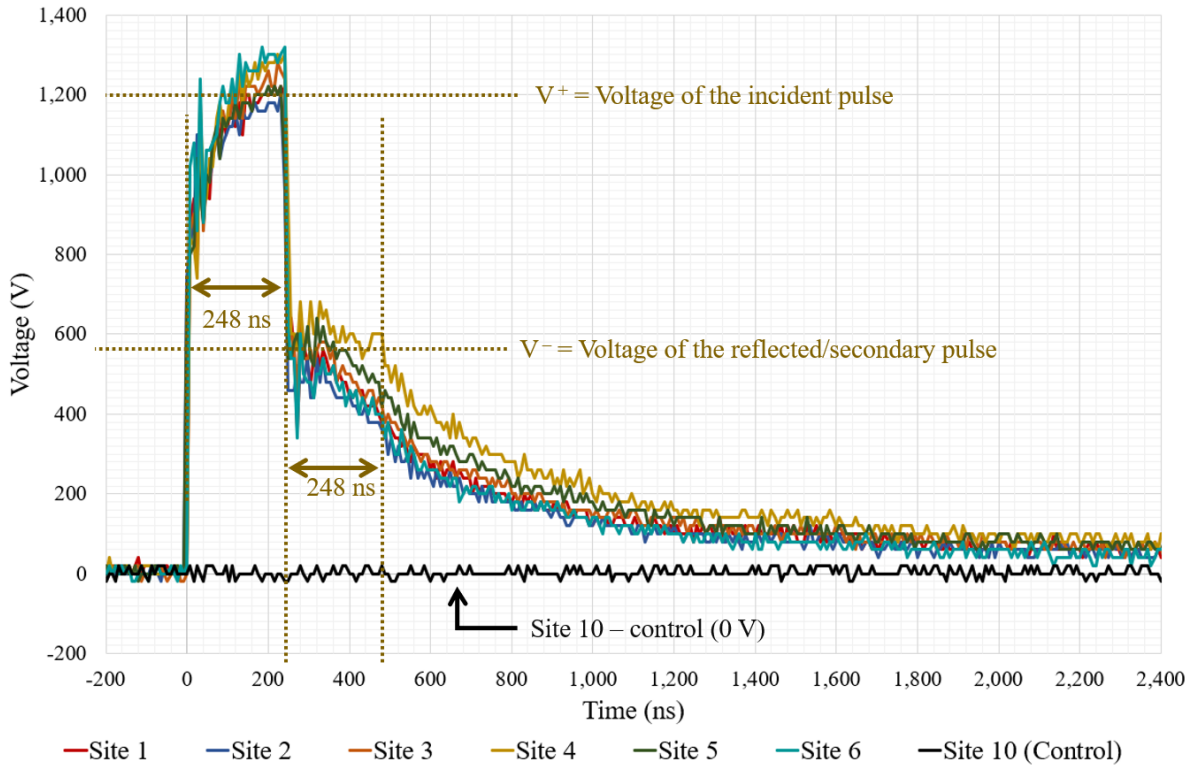


Fig. 6.12. nsPEF applied to sites 1 to 6 and control (site 10) with the fast nsPEF electroporation system operating in normal mode.

The ability to estimate the tissue impedance based on the associated reflections from the applied nsPEFs could provide an extra modality for the fast nsPEF electroporation system in its next iteration. The next iteration of the fast nsPEF electroporation system could provide the ability to measure the impedance of bulk tissue as a function of non-thermal ablation to determine when cells have been destroyed. From observing the nsPEF waveform and associated reflection from each site, the average impedance of the liver tissue is calculated as approximately 134 Ω.

From these results, it can be said that the *in-vivo* testing of the fast nsPEF electroporation system produced some very positive outcomes in terms of observed macroscopic and microscopic tissue effects. This system serves as an effective prototype for the continuous proof-of-concept work to determine clinical applications of nsPEFs as an alternative energy source; in particular as a possible alternative cancer treatment method.

A suggested change for the next iteration of the fast nsPEF electroporation system is to replace the 50 Ω co-axial delay line with a tapered microstrip line that has an associated delay time of 124 ns (2T = 248 ns) and impedance of approximately 134 Ω. This would result in a more compact system that would be desirable for clinicians as it would eliminate the need for the external 24.8 m long coaxial line for the generation of 248 ns. The use of a 134 Ω tapered microstrip charged line would reduce the reflection coefficient to produce a better match with the liver tissue load. This change would result in

fewer pulses required to produce the same histological effects observed in this work and a reduction in treatment time.

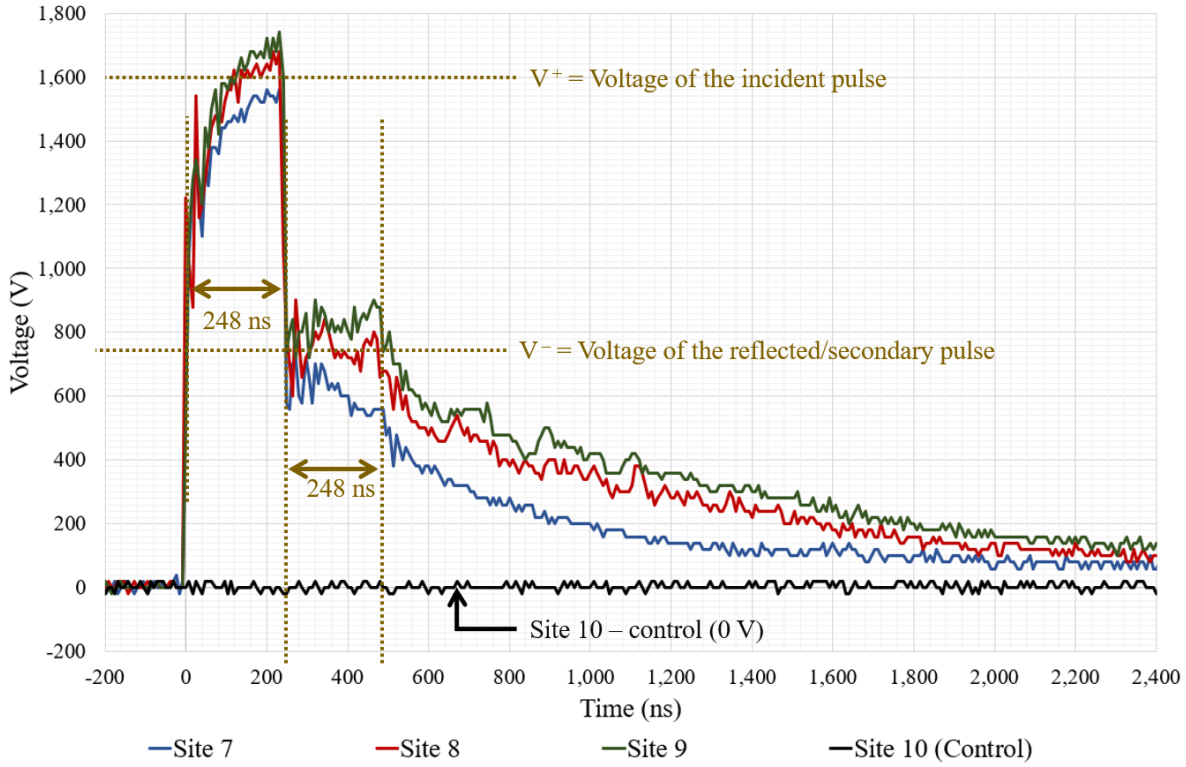


Fig. 6.13. nsPEF applied to sites 7 to 9 and control (site 10) with the fast nsPEF electroporation system operating in 'continuous operation' mode.

6.6. Conclusion

After reviewing the histopathology from the latest pre-clinical, it can be concluded that the application of 248 ns PEFs produced by the fast nsPEF electroporation system and associated applicator developed in this work was able to irreversibly (and possibly reversibly) electroporate bulk liver tissue.

Histopathological features of irreversible electroporation were seen in six out of ten samples, and the histological effects were consistent throughout the samples in terms of cellular compromise. The study suggests that maximum energy of 10 Joules is required to cause irreversible electroporation of liver tissue. This indicates that the effect of irreversible electroporation is dependent on the energy delivered into the tissue load [42]-[43]. It may also be stated that reversible electroporation could have occurred in all sites where nsPEFs were applied. A method of investigating reversible electroporation in a pre-clinical setting is required for future evaluation of nsPEFs to identify the threshold where the reversible effect of the pulses becomes irreversible using nanosecond electroporation.

Morphologically, it has been shown that the effect of treatment is limited to cells. The breaching of the cytoplasmic membranes of cells was restricted to the treatment application areas with obvious loss of integrity of those cells from the time of energy application. Collagen within the treated areas was unchanged from normal (control site), as shown in Table 6.3. This result indicated that there were

no detectable heat associated effects on the collagen in any of the areas of tissue that indicated cellular compromise. Therefore, it can be concluded that the irreversible electroporation demonstrated in this work provides a method of non-thermal tissue ablation.

This pre-clinical work has shown that slow charging and rapid discharging of a charged line with a stack of avalanche transistors is a design that is capable of delivering consistent and sufficient nsPEF energy into a bulk tissue load. Fig. 6.12 and Fig. 6.13 illustrate this. However, these figures also show, as theory suggests, that the system is sensitive to load impedance, and this is highlighted by the associated pulse reflections that follow the incident 248 ns applied pulsed electric field. It is also suggested that these reflections have minimal effect on the histological outcomes from the application of the 248 ns pulses applied to the liver using the fast nsPEF electroporation system and associated device. As suggested above, the measurement of the reflected pulses may be used to provide information on the state of the non-thermal ablated tissue.

This pre-clinical investigation has indicated that the load impedance of a liver bulk tissue is approximately 134 Ω. Therefore, for better matching to provide a reduction of the reflected voltage, thus effective energy delivery, a suggested adjustment is to increase the delay line impedance from 50 Ω to 134 Ω. This may be achieved by fabricating a tapered microstrip printed circuit board (PCB) delay line with an associated delay time of approximately 124 ns (2T = 248 ns).

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CHAPTER VII. SUMMARY, CONCLUSION & FUTURE WORK

7.1. Summary

This work contributes to the field of electroporation; in particular the generation of high voltage nanosecond pulsed electric fields (nsPEFs) to treat cancer. The focus of this work was on the design, development and validation of a slow and fast nsPEF electroporation system for potential clinical applications. The introduction chapter justified nsPEFs as a research topic and the motivation to progress the field and increase available nsPEF electroporation systems available for clinical research.

An overview of the relevance of electroporation, both in the microsecond (µs) and nanosecond regime (ns), and clinical applications were presented in the second chapter. Specifically, details regarding electrochemotherapy (ECT), reversible, irreversible (IRE), and nanosecond electroporation (nsEP) were included. Additionally, a literature review of the various technologies and methods of generating high voltage nsPEFs was presented. The advances in high power fast switching semiconductor devices have been a key enabler in the development of the slow and fast nsPEF electroporation systems. The key considerations in selecting the appropriate technology for the development of the nsPEF electroporation systems were highlighted in this chapter.

The literature search concludes that clinical applications of pulsed electric fields in a growing research field, especially for nanosecond pulsed electric fields. At the time of writing this thesis, no commercial nanosecond electroporation systems were available. Advancements in semiconductor power transistors have resulted in the commercial availability of electronic components that are capable of switching high voltages, in excess of a kilovolt (kV), with transition times in the nanosecond (ns) and even picosecond (ps) regime. Furthermore, advancements in microwave transmission lines and connectors have resulted in their capability to operate at high frequency with high voltage handling capability.

The first work chapter describes the design, development and evaluation of the slow nsPEF electroporation system in electrical and biological terms. Chapter 3 describes the design and development of a push-pull configuration of a power metal-oxide-semiconductor field-effect transistor (MOSFET)-based electroporation system that was optimized to generate 100 ns to 300 ns pulsed electric fields (PEFs) with amplitudes in excess of 1 kV, across a 50 Ω load impedance. This chapter also contains the electrical verification and validation (V&V) of the slow electroporation system. This work includes the evaluation of the nsPEF electroporation system delivering energy across a 50 Ω load, as well as any other representative load impedances.

Chapter 4 describes the *in-vitro* investigation conducted using the slow nsPEF electroporation system. Investigations performed included the permeability, viability, and thermal cellular effects caused by the applied nsPEFs on the D283 medulloblastoma cell line population.

The second work chapter describes the design, development and evaluation of the fast nsPEF electroporation system. Chapter 5 describes the design and development of a nsPEF electroporation system designed to generate nsPEF of 10 ns to 300 ns in duration, with pulse amplitude in excess of 1 kV with sub-nanosecond rise and fall times. The system design is based on the relatively slow charging and rapid discharging of an open circuit coaxial transmission line, through a stack of avalanche transistors that operates as a fast-switching element. This chapter also includes the evaluation of the nsPEF electroporation system performance in terms of the generation of pulsed electric fields of duration from 10 ns to 300 ns across a 50 Ω load impedance.

Chapter 6 discusses the pre-clinical investigation (*in-vivo* study) carried out by applying nanosecond pulsed electric fields to bulk porcine liver. This includes histology to look at the effect on cells and the collagen matrix. The results indicated irreversible (and possibly reversible) cellular changes. This work used Haematoxylin & Eosin and Picro Sirius Red and Miller's Elastin staining to investigate any morphological, collagen and cellular changes that occurred due to the nsPEFs.

7.2. Conclusion

The work presented in this thesis is a direct contribution to the European Union's Horizon 2020 Framework Program FET OPEN funded project called 'Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells' (SUMCASTEC). SUMCASTEC was set up to explore explores a radically new approach for real-time isolation (i.e., within minutes vs current 40 days) and neutralization of cancer stem cells. The work presented in this thesis concentrates on the neutralization aspects of this project. This work successfully met the specified research objectives set out at the beginning of the research program which was focused on the design and development of nsPEF electroporation systems. The primary focus of this work was to support both *in-vitro* and *in-vivo* investigations on the clinical effects of nsPEF on suspended cells and bulk tissue as part of SUMCASTEC. The nsPEF electroporation systems aimed to neutralize or treat, aggressive brain tumours, in particular Glioblastoma and Medulloblastoma, through the delivery of nsPEF energy in a non-thermal manner. This was achieved.

Slow nsPEF Electroporation System

The slow nsPEF electroporation system design was operated through the fast-switching of Silicon Carbide (SiC) power MOSFETs in a push-pull configuration. Chapter 3 demonstrated that the system could produce a specific number of nsPEFs from 100 ns to 300 ns in duration, with amplitudes in excess

of 1 kV, at various repetition frequencies across 50 Ω and above load impedances. The key parameters associated with the slow nsPEF electroporation system are highlighted in Table 7.1.

The slow nsPEF electroporation system enabled data on D283 Medulloblastoma cell populations suspended in a 50 Ω cell line environment to be obtained. The initial results indicated that the SiC MOSFETs connected in a push-pull configuration for the generation of nsPEF are able of controlled non-thermal irreversible nanosecond electroporation, or neutralization, of cancerous cell-line populations that are enriched in cancer stem cells when 20x 300 ns PEFs of 1.4 kV/mm were delivered.

Table 7.1. The slow nanosecond pulsed electric field electroporation system pulse parameters

Parameters	Minimum	Maximum	Determined by
Pulse Duration (ns)	80	1,000	the gate driving signal from the microcontroller and driver circuit
Amplitude (V)	250	1,400	the FS40 high voltage power supply unit
Repetition Rate (Hz)	1	50	the gate driving signal from the microcontroller and driver circuit
The Number of Pulses Generated	1	1,000 or continuous	the gate driving signal from the microcontroller and driver circuit
Rise / Fall Time (ns)	35		the MOSFETs rise time and gate-source current available to charge the gate-source and gate-drain capacitors

Fast nsPEF Electroporation System

The fast nsPEF electroporation system design is based on the relatively slow charging and rapid discharging of an open circuit coaxial transmission line through a stack of avalanche transistors operating as a fast-switching element. Work chapter II showed that the system can produce a user-specified number of nsPEFs from 10 ns to 300 ns in duration, with amplitudes in excess of 1 kV, at various repetition frequencies up to 1 kHz (limited by the transmission line length used) across a 50 Ω load impedance. The key parameters associated with the fast nsPEF electroporation system are highlighted in Table 7.2. This work showed that a 10 ns PEF with an amplitude of 2.5 kV was generated by stacking 20 transistors configured as a fast-switching element.

The fast nsPEF electroporation system was shown to be suitable for delivering high voltage nanosecond pulsed electric fields into porcine liver tissue in an *in-vivo* preclinical setting. The pre-clinical performed as a part of this work confirmed that the system has potential beneficial clinical usage due to the demonstrated ability to selectively destroy cells without causing damage to the collagen matrix within bulk tissue. This system was able to non-thermally irreversibly (and possibly reversibly) electroporate *in-vivo* cells, causing associated cellular changes within liver tissue. The electroporated cellular features were well demarcated from normal tissue and regions of cellular apoptosis-related directly to the instrument application sites. Morphologically, the effect of treatment was limited to cells

and the collagen within the treated areas was unchanged from normal, therefore indicating non-thermal ablative effects.

Table 7.2. The fast nanosecond pulsed electric field electroporation system pulse parameters

Parameters	**Minimum**	**Maximum**	**Incremental increase**	**Determined by**
Pulse Duration (ns)	10	300	10	the transmission line length
Amplitude (V)	100	2,500	100	the number of avalanche transistors in the stack
Repetition Rate (Hz)	1	1,000	1	the charging and discharging times associated with the coaxial line
The Number of Pulses generated	1	1,000 or continuous	1	the input trigger signal
Polarity	Positive, negative or simultaneous generation of positive and negative pulses			the location of the load between the charged line and the ground plane of the system
Rise / fall time (ns)	< 1			The avalanching time associated with the FMMT417

The conclusion from developing the slow and fast nanosecond pulsed electric field electroporation systems and the associated biological investigations carried out to date using these systems is that circa 1kV nanosecond duration pulsed electric fields have the potential to non-thermally ablate cancerous tumours. Histological evidence from the pre-clinical studies indicates advantages over microsecond pulsed electric fields (µsPEF) and other traditional treatment options.

This work has provided the necessary evidence for Creo Medical Ltd to conduct a future study to demonstrate the feasibility of nsPEF energy modules as a means of non-thermal clinical treatment for cancers. Future work aims to build upon the tangible proof of concept work carried out through this research. The non-thermal aspect of the nsPEF systems has the potential to lead to the development of an electrosurgical system and devices for use in routine clinical practice to treat deep-seated tumours in difficult-to-access anatomical locations or sensitive structures that are sensitive to elevated temperatures. Organs such as the brain, head and neck, lung, pancreas, bladder and so forth are possible organs that could benefit.

In conclusion, the slow and fast nsPEF electroporation systems developed in this work were proven to be useful instruments in the field of nsPEF research. By supporting a wide range of energy delivery protocols (pulse width, repetition frequency, number of pulses, and amplitude) it was possible to define the optimal pulsed electric field parameters for successful non-thermal neutralization of cancer cells and cancer stem cells.

7.3. Future Work

To become a commercial system, or a system that could be used to carry out a clinical study on human tissue, these prototype systems, the slow and fast nsPEF electroporation system requires further development.

At the time of designing and developing the slow nsPEF electroporation system, Wolfspeeds's C2M1000170D SiC power MOSFETs driven by Toshiba's TLP352 photocouplers were the best-suited components for the generation of the nanosecond pulsed electric fields. Advancements in semiconductor technology since this work have resulted in the availability of alternative power MOSFETs with faster rise times and lower drain-source ON-resistance, and higher current gate drivers to efficiently drive said MOSFETs. An example of these devices is Infineon's IMBF170R650M1 SiC MOSFET and the 1ED3124MU12H isolated gate driver integrated circuit. Replacing the C2M1000170D SiC MOSFETs and the TLP352 Photocouplers with these components with minimal circuitry adaptation would result in the possibility of optimizing the slow nsPEF electroporation system to generate higher voltage pulses with faster rise and fall times.

Suggested future work for the fast nsPEF electroporation system includes implementing a microcontroller, graphical user interface (GUI), internal power supply units (PSUs) and integration of a variable, or fixed, transmission line or delay line design within the unit. Following analysis of the histological effect of the application of a 248 ns pulsed electric fields of 1.2 kV in amplitude into liver tissue, a fixed microstrip charged line with an associated delay time of 125 ns (generation of pulses of 250 ns in duration) and characteristic impedance of 130 Ω would be best suited for next iteration of the fast nsPEF electroporation system for pre-clinical and clinical evaluation.

APPENDICES

Appendix I - Review of Fast High Voltage Pulse Circuits

a) Marx Generators

The Marx generator topology is an example of a high voltage pulser. Originally, it was designed to test high voltage components used in power grids. The circuit produces high voltage pulses from a low-voltage direct current (dc) supply. This topology has been adopted for pulsed electric field (PEF) generation [1]-[7].

Technology Structure and Operation

Marx topology shown in Fig. I.1, is based on stacking stages of circuits comprising an energy storing capacitor (C) a resistor (R) and a switch (S) in series. The stages are charged in parallel from a dc power supply (V_{CC}) and discharged in series across a load (Z_L) when the switches are triggered [1]-[7].

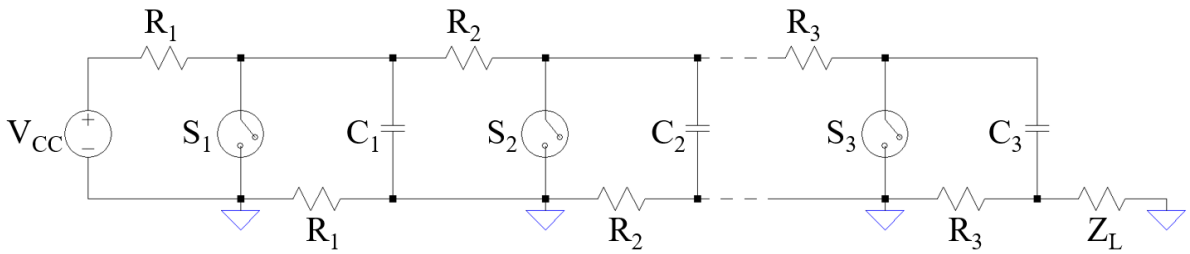

Fig. I.1 Marx generator topology for pulsed electric field generation [1]

The novelty of the Marx generator is to generate a high voltage source and the nanosecond pulsed electric field (nsPEF) timing parameters of the design would be selected by the switching element implemented. The switches used in the Marx topology can consist of a range of switch types, varying from relays to semiconductor-based switches. One popular switch choice used in Marx generator is the spark gap switch, yet semiconductor switches are becoming more popular. The capacitors are fully discharged, creating a decaying capacitive discharge PEF, where the PEF current and voltage are high. For this design, the pulse repetition frequency is in the order of several hertz (Hz) as the circuit relies on the charging time of the capacitors at each stage [1]-[7].

The output voltages are determined by the breakdown voltage of the switching element implemented and the number of stages. The charging voltage can reach tens or possibly hundreds of kilovolts (kV), allowing a PEF of high amplitude in the kV range, as high as 50 to 100 kV to be produced. However, devices in the range of 1 to 6 kV are common in the application of electroporation (EP) [1]-[7].

The Marx topology shown in Fig. I.1, can be adapted to produce bipolar pulses. Bipolar nsPEF generation provides another nanosecond electroporation (nsEP) research and clinical application opportunity. The Marx can be enhanced by a half-bridge and/or full-bridge topology for the generation of bipolar nsPEF, as shown in Fig. I.2 [1]-[7].

In both cases, the half and full-bridge topology can produce positive and/or negative PEFs. However, the half-bridge topology has limitations in operation with capacitive-type loads. The increase in the number of switches in a full-bridge design provides additional operational flexibility similar to the direct capacitor discharge topology in Fig. I.1. To improve the pulse control, and amplitude, several half-bridge or full-bridge pulse forming circuits can be stacked in a modular approach using the Marx generator topology to enable the generation of bipolar pulses with higher voltage amplitude [28], [1]-[7]. Nonetheless, the capacitor discharge of a Marx circuit, in a traditional half or full-bridge design limits the switching dynamics and pulse repetition frequency of the PEFs generated to the microseconds.

The operation of a Marx-generator in conjunction with a half-bridge circuit is seen in Fig. I.2(a). A positive pulsed electric field will appear across the load by operating switch S_1, and an inverse pulse would be produced through the operation of switch S_2. The timing specification of the nsPEF generated would be determined by the switching element implemented.

The general concept of a Marx-generator in a full bridge circuit, as seen in Fig. I.2(b), alternates the polarity of the pulse across the load (Z_L) by operating two switches at a time. A positive pulsed electric field will appear across the load by the operation of switches S_1 and S_4. The polarity of the voltage across the load will be changed to a negative polarity y operating S_2 and S_3 simultaneously. The timing specification of the nsPEF generated would be determined by the switching element implemented with identical transition (rise and fall times) times. An example of a potential switching element for Marx generator designs is the use of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs).

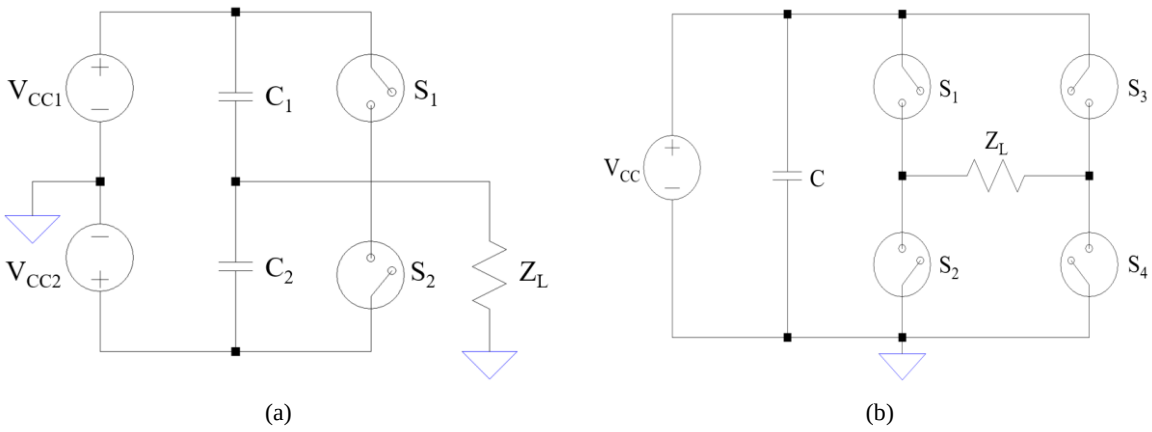

Fig. I.2. Marx generator topology for bipolar pulsed electric field generation (a) half-bridge (b) full bridge [1].

The power is dissipated, and the voltage is dropped across each switching stage in a Marx bank configuration is dependent on the breakdown voltage of the switching element used. With a MOSFET switching element, the maximum voltage and power at each stage of the Max generator, Fig. I.3(a), would be limited to a MOSFETs drain-source breakdown voltage (BV_{DS}). An example of the voltage drops and power dissipation of a Marx generator with a switching element of various specifications can be shown below in Fig. I.3(b) to Fig. I.3(d).

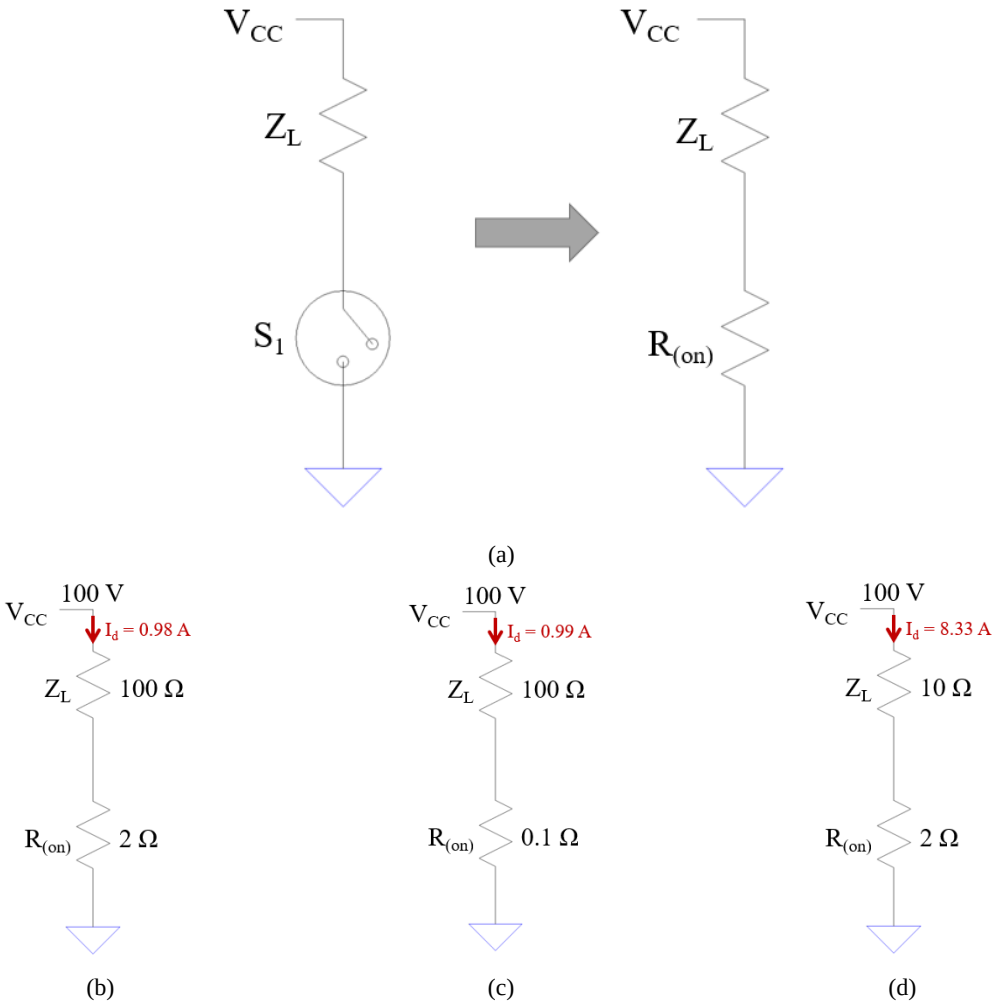

Fig. I.3. A switching element in a Marx bank generator (a) basic circuit and equivalent circuit with various circuit specification parameters (b) $R_{(on)} = 2\ \Omega$, $Z_L = 100\ \Omega$ (c) $R_{(on)} = 0.1\ \Omega$, $Z_L = 100\ \Omega$ (d) $R_{(on)} = 2\ \Omega$, $Z_L = 10\ \Omega$

Table I.1. illustrates the power dissipation and the voltage drop across each component, the load, (Z_L) and the switching elements ($R_{(on)}$). The lower the load impedance the lower the amplitude across the load and the higher the voltage drop across the switching element (V_{drop}) and therefore the power that needs to dissipate by the switching element. In retrospect with a switching element, the change in the ON-resistance of a switching element ($R_{(on)}$) or drain-source ON-resistance of a switching element such as a MOSFET ($R_{DS(on)}$) or has minimum changes in the voltage across the load (compare Fig. I.3(b) to Fig. I.3(c)), yet it significantly increases the voltage drop and power dissipated across the switching element.

Table I.1. Power dissipation and voltage drop across a switching element in a max generator topology and with various circuit load (Z_L) and ON-resistance ($R_{(on)}$)

Circuit	V_{CC} *(V)*	Z_L *(Ω)*	$R_{(on)}$ *(Ω)*	V_L *(V)*	I_D *(A)*	P_L *(W)*	V_{drop} *(V)*	P_{dis} *(W)*
Fig 2.14 (b)	100	100	2.0	98.04	0.98	96.12	1.96	1.92
Fig 2.14 (c)	100	100	0.1	99.90	1.00	99.80	0.10	0.10
Fig 2.14 (d)	100	10	2.0	83.33	8.30	694.44	16.67	138.89

where the voltage drop across a switching element is $V_{drop} = \left(\frac{R_{(on)}}{Z_L+R_{(on)}}\right)V_{cc}$. The power dissipated across a switching element is $P_{dis} = \frac{V_{drop}^2}{R_{(on)}}$. The voltage dropped across a load (Z_L) is $V_L = \left(\frac{Z_L}{Z_L+R_{(on)}}\right)V_{cc}$. The current through a load is $i_d = \frac{V_L}{Z_L}$. And the Power dissipated across a load is $P_L = \frac{V_L^2}{Z_L} = i_d V_L$. Were V_{CC} is the power supply voltage at that Marx single stage, V_{drop} is the voltage drop across a switching element, $R_{(on)}$ is the ON-resistance of the switching element, Z_L is the load impedance, P_{dis} is the power dissipated across the switching element, $V_{L\ is}$ the voltage across the load, i_d is the current through the circuit and P_L is the power dissipated by the load.

b) Charged Transmission Line

Charging and discharging of a transmission line can form the basis of a pulse-forming circuit. This is a common type of circuit topology for the generation of high voltage nsPEF with durations less than 100 ns duration.

Technology structure and operation

The nsPEF is generated through the discharging of a transmission line that functions as a storage element. A rectangular pulse is formed by the discharging of an open-ended delay line, such as a coaxial transmission line cable, of a specific length (*l*) and associated delay time (T), and characteristic impedance (Z_0) through a switch (S) that determines the rise-time of the PEF generated [1]-[2], [8]-[13].

The principle of discharging a charged transmission line to generate nsPEF is illustrated in Fig. I.4. In operation, a transmission line, that is open-circuited at its distal end, is charged to the level of the power supply (V_{CC}) through a high impedance resistor (R_C). A rectangular nsPEF is generated by discharging the charged open-circuit transmission line through a load (Z_L) by closing a switching element (S) that has no switch bouncing or is a mercury-wetted relay. Closing the switching element produces a symmetrical pulse across the load with an amplitude of V_L, which is half the value of the voltage the charged line was charged to $\left(\frac{V_{CC}}{2}\right)$ of a duration that is twice as large as the associated delay time of the transmission line (2T). This is true providing that the characteristic impedance of the transmission line (Z_0) matches the load impedance (Z_L) i.e., $Z_0 = Z_L$, and that the charging resistor (R_C)

is much greater than the characteristic impedance of the transmission line (Z_0) i.e. ($R_C >> Z_0$). To ensure that Z_0 dominates the value of Z_0 is 50 Ω and R_c is 1 M Ω. Therefore, the total impedance is $Z_\Sigma = \frac{R_0 Z_0}{R_0+Z_0} = \frac{50 \text{ x } 1\text{x}10^6}{50+1\text{x}10^6} = \frac{50x10^6}{\sim 10^6} \approx 50\Omega$.

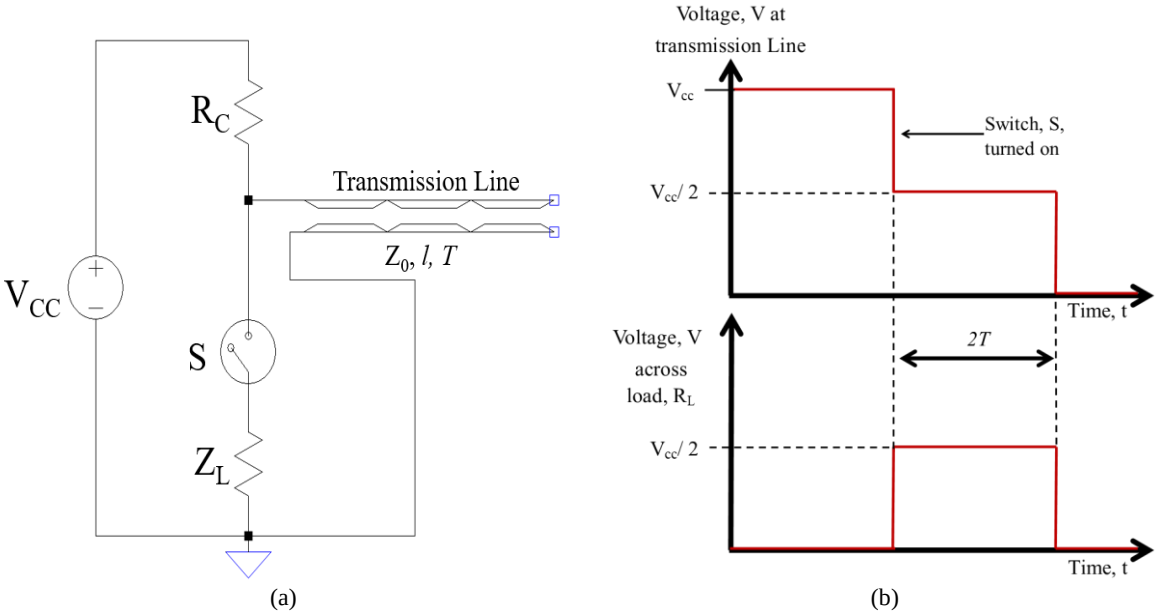

Fig. I.4. Principal operation of generating pulsed electric fields through the discharging of a charged transmission line (a) pulse forming circuit (b) pulsed electric fields waveform principle [1]

The transition time of the nsPEF depends primarily on the properties of the switching element [1].

$$T = \frac{l\sqrt{\varepsilon_r}}{c} \tag{I.1}$$

A transmission line associated delay time, T, is dependent on the transmission lines length (l) and the dielectric constant (ε_r) of the dielectric used to separate the two conductors that form the transmission line. Where c is the speed of light ($3\text{x}10^8$ m/s).

The nsPEF amplitude and shape rely on the matching between the characteristic impedance of the transmission line (Z_0) and the load impedance (Z_L). The pulse shape is dependent on the voltage reflection coefficient (Γ) between Z_0 and Z_L (I.2). While the amplitude is dependent on the potential divider relationship between Z_0 and Z_L (I.3) [130]. Fig. I.5 demonstrates the equivalent circuit relationship between Z_0 and Z_L resulting in equations (I.2) and (I.3).

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{I.2}$$

$$V_L = \left(\frac{Z_L}{Z_L + Z_0}\right) V_{CC} \tag{I.3}$$

where Γ is the voltage reflection coefficient, Z_0 the characteristic impedance of the transmission line, Z_L is the load impedance, V_{CC} is the voltage the transmission line is charged to from a power supply unit, and V_L is the voltage across the load.

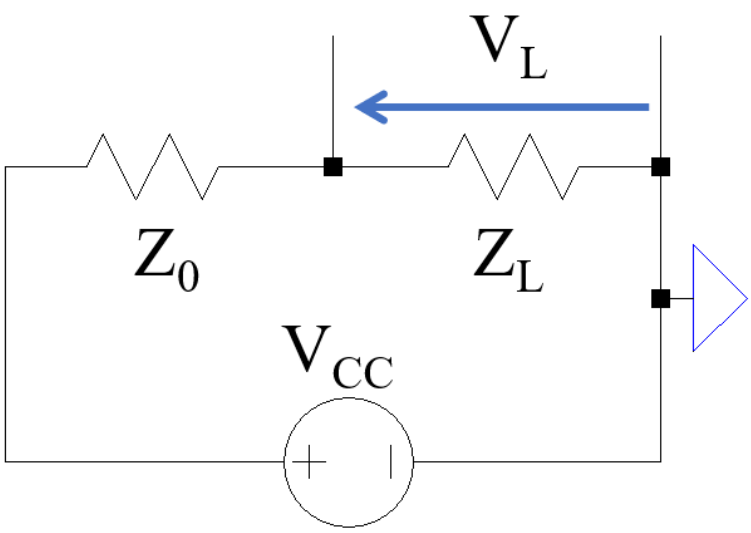

Fig. I.5. Equivalent circuit representing the relationship between the characteristic impedance of the transmission line (Z_0) and load impedance (Z_L) in a charged transmission line topology

Technology limitations

The main limitation of this configuration is the requirement for the impedance match between the load impedance and impedance of the charged lines ($Z_L = Z_0$) to generate symmetrical square nsPEFs with no reflections and the maximum amplitude of the PEF is limited to $\frac{V_{CC}}{2}$ [1]-[2], [8].

Firstly, a biological cell line load is of a low impedance, approximately 10 Ω, while the impedance of a coaxial transmission line is typically 50 Ω or 75 Ω [132]. With a 50 Ω transmission line and cell line load of 10 Ω, the associated reflection coefficient would be $-\frac{2}{3}\left(=\frac{10-50}{10+50}=-\frac{40}{60}\right)$. Therefore, an impedance matching solution is needed to overcome this reflection to prevent $\frac{2}{3}$ of the PEF to be reflected, and only $\frac{1}{3}$ of the voltage to be exerted across the cell line load. A solution to overcome this is to change the transmission line impedance. This can be done through the implantation of a microstrip line design as a charged line or the use of multiple coaxial lines connected in parallel, i.e., five 50 Ω transmission lines would provide a total charged line characteristic impedance value of 10 Ω. Additionally, changing the geometry of the coaxial line i.e. increasing the diameter of the cable conductor could produce a coaxial charged line characteristic impedance value of 10 Ω as indicated by equation (I.4) [1]-[2], [8].

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{138}{\sqrt{\mu_r \varepsilon_r}} \log\left(\frac{b}{a}\right) \tag{I.4}$$

where ε_r is the relative dielectric constant, μ_r is the relative permeability, a is the outside radius of inner conductor of the coaxial cable and b is the inside radius of outer conductor of the coaxial cable. C and L are the capacitance and inductance of the coaxial cable respectable.

Secondly, literature suggest that the impedance of the biological load reduces during pulse delivery. This indicates that with each nsPEFs applied onto the biological load could possibly change the associated refection, and therefore the nsPEF waveforms delivered over time. At best, only half of the power supply input into the circuit will be transferred across the load, thus a large efficiency and power loss is seen.

c) Blumlein

Technology structure and operation

Blumlein is a further development on the basic single charged line topology [1]-[2], [8]-[13]. The topology consists of a variable high voltage power supply (V_{CC}) a high impedance charging resistor (R_C) two identical transmission lines, T_1 and T_2, and a fast-switching element, (S). This is shown in Fig. I.6. This topology operates in two parts. First, a charging phase and secondly a discharging phase. During the charging phase, the switch (S) is turned 'OFF' and the transmission lines, T_1 and T_2, are charged to the voltage level of the voltage power supply (V_{CC}). The nsPEF is generated during the discharging phase when the switch is turned 'ON', and the transmission lines are discharged to the load (Z_L) at the output [1]-[2], [8]-[13].

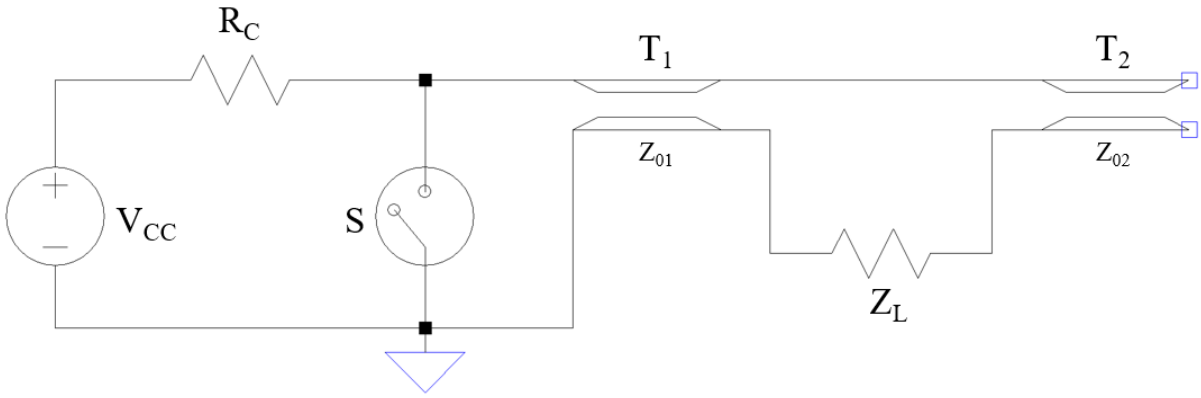

Fig. I.6. Blumlein generator topology for the generation of symmetrical pulsed electric field [1]

The pulse duration of the nsPEF generated is twice the associated delay time, or electrical length, of the transmission lines (T) and its amplitude, equals the value of V_{CC}. The nsPEF shape is reliant on the impedance ratio between the load impedance (Z_L) and the impedance of the transmission lines (Z_0). For zero reflection, the load impedance (Z_L) requires to be twice the impedance of the transmission lines (Z_0) which is the total characteristic impedance of both transmission lines T_1 (Z_{01}) and T_2 (Z_{02}). The reflection coefficient (Γ) for a Blumlein topology is given by equation (I.5) [1]-[2], [8]-[13]. An adaptation of equation (I.2).

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{Z_L - (Z_{01} + Z_{02})}{Z_L + (Z_{01} + Z_{02})} \tag{I.5}$$

where Z_L is the load impedance, Z_{01} is the characteristic impedance of the transmission line T_1, and Z_{02} is the characteristic impedance of the transmission line T_2.

Topology limitations

The limitation of this circuit is the requirement for impedance matching between the load impedance and total characteristic impedance of the transmission lines T_1 and T_2 ($Z_L = Z_0 = Z_{01} + Z_{02}$). This situation is identical to the charged line topology, as biological cell line load is of low impedance of approximately 10 Ω, while coaxial transmission line impedance is typically 50 Ω or 75 Ω value [14]. Therefore, impedance matching between the transmission line and load is essential to reduce reflection. Methods to overcome this have been discussed previously in the technology limitation section of the charged transmission line technique.

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Appendix II - Review of Fast Switches to Create Pulsed Electric Fields

a) Mercury Wetted Relay Switches

Traditional mechanical switches are undesirable for the generation of fast pulses in the nanosecond regime as their contact tends to bounce and cause undesirable multiple pulses and pulse ringing. If the contacts are wetted with mercury, the electric contact is retained on the bounce and multiple undesired pulses are prevented. The contacts are wetted with mercury by feeding mercury from a reservoir to the contacts through capillary action for mercury wetted relay switches [1]-[6].

Technology structure and operation

Fig. II.1 is an example of Schintlmeisters mercery wetted relay [1]. The mercury reservoir is heated to 110 °C, causing mercury vapour to be deposited on the relay switch contacts. To suppress reflections and minimise the rise time during switching, the switching element must be coaxially incorporated into the conduction path.

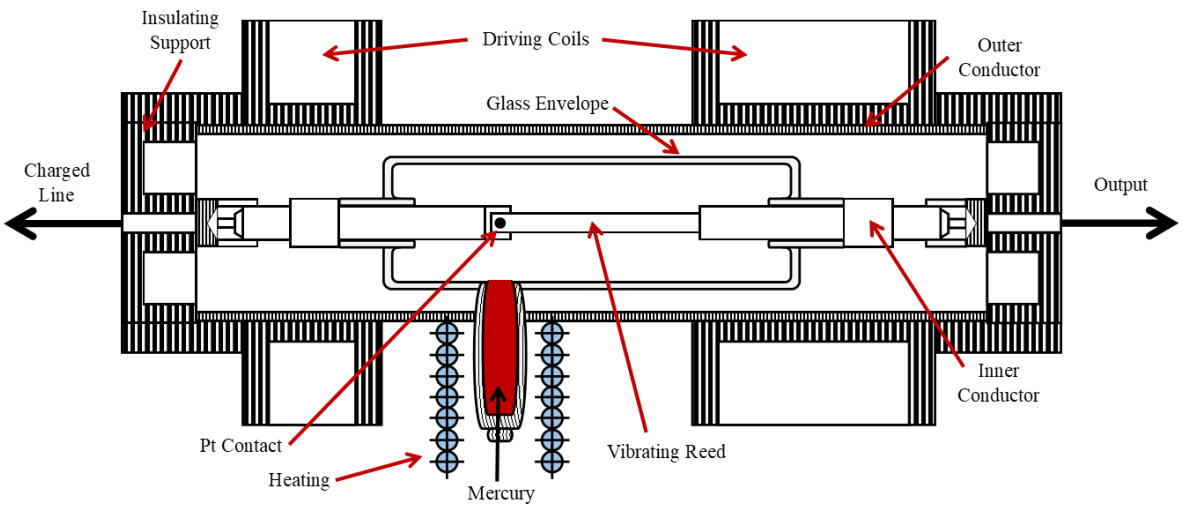


Fig. II.1. Schintlmeisters mercury wetted relay topology. Cross section through a coaxial vibrating switch with mercury wetted contacts [1].

The inner conductor and the vibrating read are constructed from steel. Opposite magnetic poles are induced across the contact gap by a magnetic alternating field that is produced by the driving coils. This results in the contact closing with the cycle of the field due to the magnetic attraction. The strength and frequency of the magnetic field are selected for a smooth reliable vibration of the relay. Other examples of mercury wetted relays can be found in [3], [5] and [6].

A mercury-wetted relay can be utilized in a double-pulse discharge line generator topology as seen in Fig. II.2. This has been demonstrated by Gnoth [130]. The principle of operation is where a pulsed electric field (PEF) is produced by a charged line T_1, where the PEF duration is twice the charged line associated delay time, $2T_1$. The generated pulse utilises the theoretical operation of a charged

transmission line topology. The double-pulse discharge design differs from the conventional single charge transmission line because the generated PEF is transmitted through a diode (D) to the load (Z_L) and an open-circuit delay line, L_2. The second transmission line, T_2, reflects the incident pulse, causing a second pulse to arrive at the load, at a time $2T_2$, if $T_2 > T_1$. When a diode is replaced with a valve to separate the two open circuit transmission lines, T_2 and T_1, a negative PEF is generated [1].

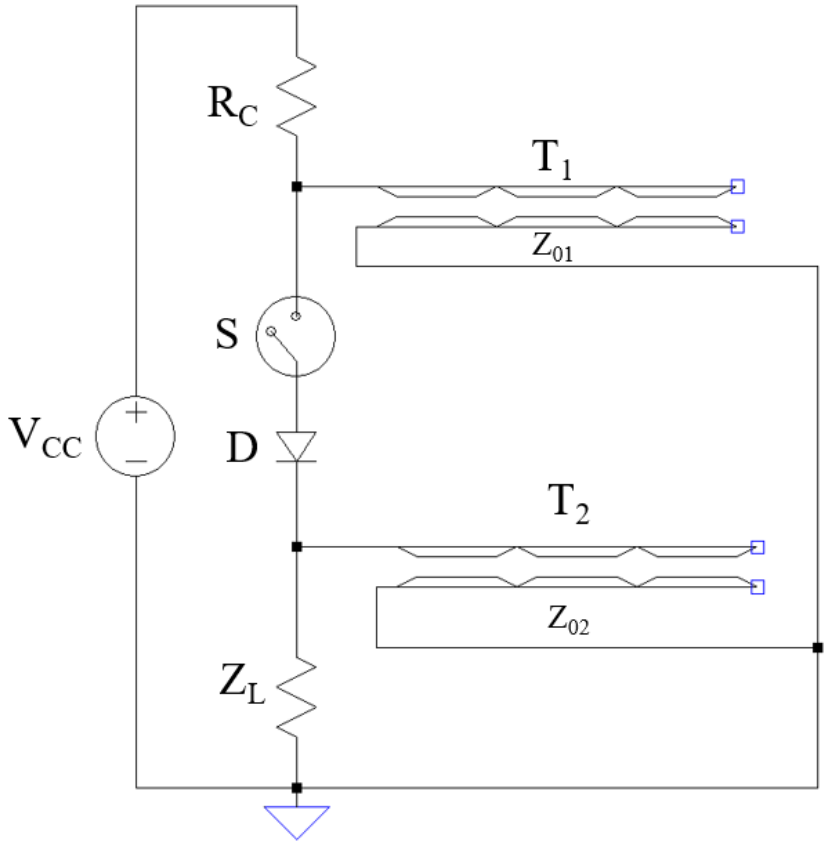


Fig. II.2. Double pulse charged line generator topology with a mercery wetted relay [1]

Technology limitations

The PEF amplitude and polarity of this switch are determined by the direct current (dc) supply voltage (V_{CC}) and the pulse width is determined by the length of the charged line (T_1). The limitation is that this form of switching cannot be triggered with a time delay by an external trigger pulse. Therefore, a low pulse repetition rate is achieved, i.e., between 50 to 500 Hz, and this is dependent on the mechanical construction of the mercury-wetted relay.

One issue of using this switching technology is the toxic effects surrounding the application of mercury. Minimal exposure to mercury can cause serious health problems and toxic effects on a person, such as on the: nervous, digestive, and immune systems, and on organs such as the lungs, kidneys, skin and eyes. Mercury is considered by the World Health Organization (WHO) as one of the top ten chemicals or groups of chemicals of major public health concern [8]. Because of the health risk surrounding this technology wetted relays have been obsolete and through technological and material

advancement has been replaced by solid state relays. This would only be a concern if the sealed glass tube fractures.

b) Spark Gap Switch

Spark gaps can be used to produce nanosecond pulses of a high current or voltage through the discharging of a charged transmission line or a bank of capacitors. Generally, the delay and rise time of the output pulses from spark gaps are less than 1 ns (~350 ps) and ~ 5 ns respectively [1], [9]-[11].

Technology structure and operation

Spark gap switches consist of a pair of electrodes with gas in the centre between the electrodes. Normally, the switch is an ideal open circuit status, as shown in Fig. II.3(a)). When a significant voltage or electric field is set up across the electrodes, a spark occurs in the gas between the electrodes, as shown in Fig. II.3(b). If a sufficient current is available, arcing occurs across the spark channel occurs. This arc turns the switch status from an open circuit (‘OFF’) to a short-circuit (‘ON’), as the voltage travels between the electrodes via arcing [1], [9]-[11].

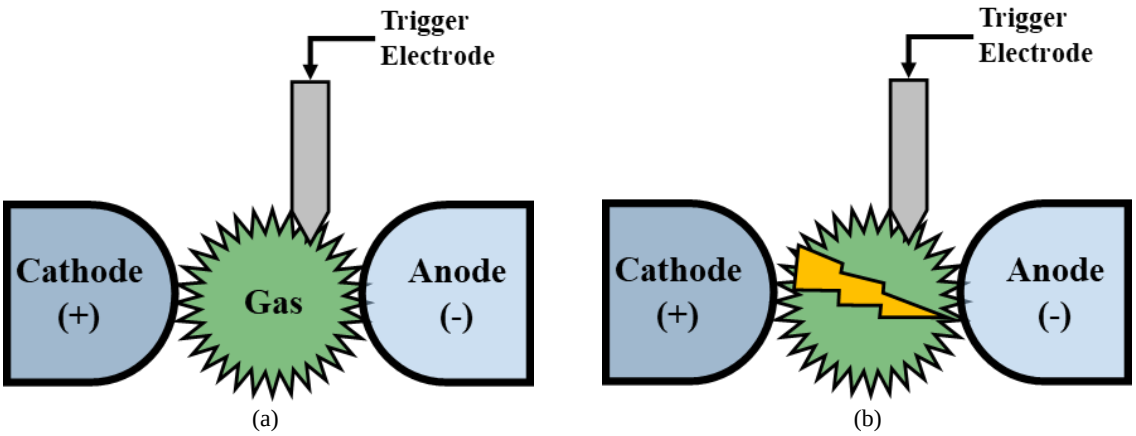
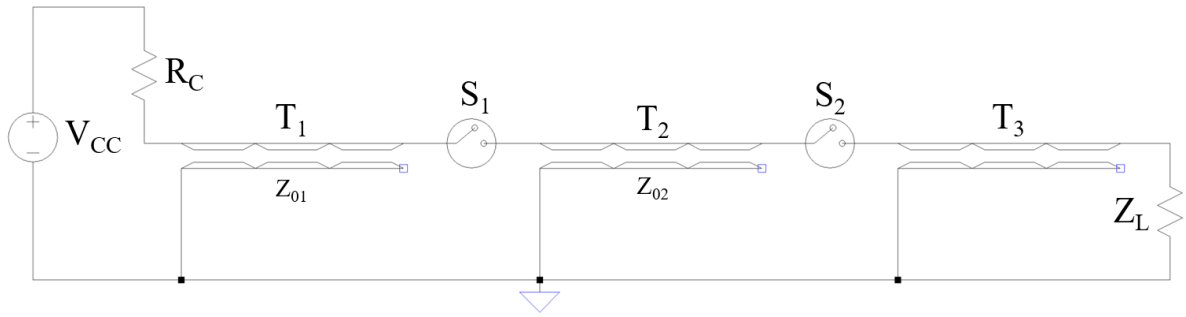


Fig. II.3. Layout of a spark gap switch (a) ‘OFF’ - open circuit state (b) ‘ON’ - short circuit state [9]

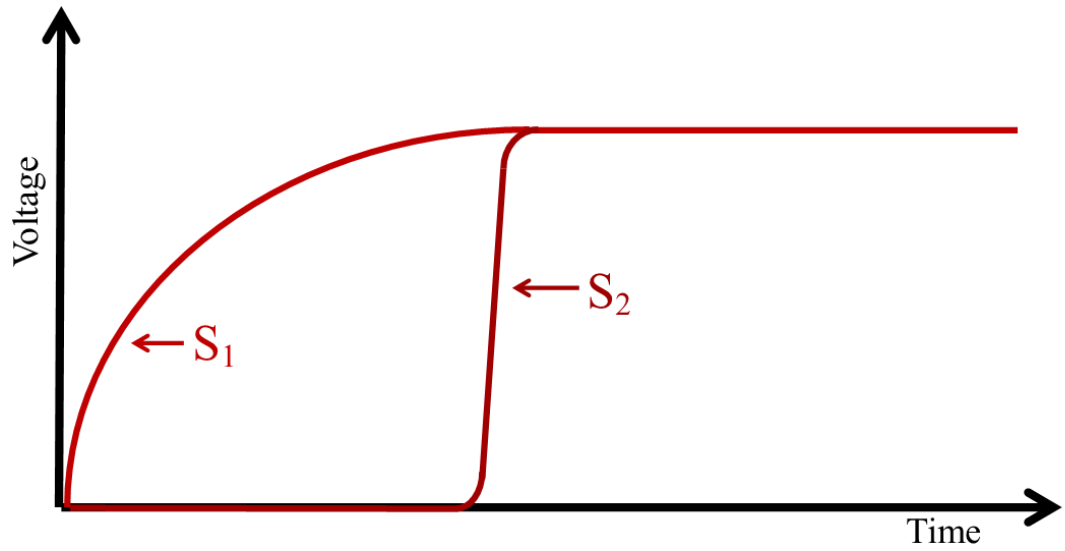
High voltage nanosecond pulsed electric fields (nsPEFs) can be generated by spark gap(s) when implemented in a circuit topology such as Marx-banks or Blumlein. The amplitude of the nsPEFs is controlled by adjusting the spark gap electrode spacing or the gas/dielectric between the electrodes. The larger the gap the larger higher the voltage required for arcing to occur, and the larger the pulse amplitude. In addition, the larger the breakdown voltage of the gas between the electrodes the higher the voltage required for arching to occur, and the larger the nsPEF amplitude [1], [9]-[11].

The principle of a spark gap generator is illustrated in Fig. II.4. A transmission line, T_1, is charged through a high impedance resistor (R_C) and discharged by a spark gap switch, S_1, which is triggered by a negative pulse through an auxiliary electrode. The pulse produced by the transmission line and spark gap, passes through a second transmission line, T_2, to the pulse sharpening spark gap switch, S_2, which receives an overvoltage on the arrival of a pulse from the first spark gap switch, S_1. This results in a

very short rise time of the output pulse, amounting to less than 1 ns across the load Z_L. The pulse sharpening effect of the rise time is illustrated in Fig. II.4(b). The steep slopes produced by the pulse sharpening gap switch, S2, operate on the gas over-pressure and have a capacitance sharping effect, apart from the pulse forming line, T1, that corresponds to a correction capacitance [1].



(a)



(b)

Fig. II.4. Nanosecond pulsed electric field generator with an isolated over-voltage spark gap with pulse sharping technique a) schematic b) waveform [1]

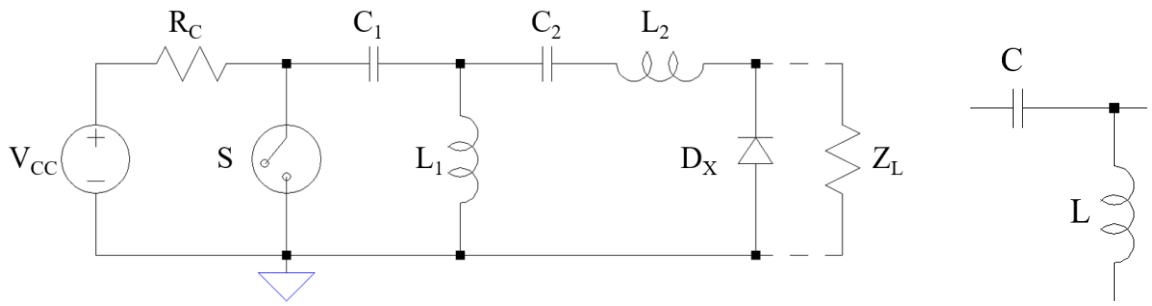
If there was no sharpening gap switch, where S1 was in series between the load (no S_2), the current rise-time would depend on the RC-time constant of the load and transmission line capacitance. With the sharpening gap in the circuit, the full voltage appears across the spark gap switch, S2, before it breaks down. When the gap does break down the full voltage appears across the load almost instantaneously, decreasing the current rise time, thus sharpening the rise time across S2 and the load as seen in Fig. II.4(b) [1], [9]-[11].

This method of producing high voltage nsPEFs has been described in the literature [12]. In several instances, laser pulses were used to trigger the spark gap switches used in the Marx-style generator topologies to obtain high voltage pulse amplitudes [12].

c) Diode Base Switching

Technology structure and operation

Diode-based switches operate similar to the Blumlein topology as both concepts include a high voltage dc power supply (V_{CC}) a high impedance resistor (R_C) a switch (S) and a charging and discharging phases. In comparison to the Blumlein, the diode opening circuit consists of a CL-resonant circuit comprising of inductors, L_1 and L_2, and capacitors, C_1 and C_2, and a stack of diodes, D_X, as shown in Fig. II.5 [1], [13]-[16].



(a) (b)

Fig. II.5. (a) Diode based switch generator topology for generation of high voltage pulsed electric fields (b) Basic CL circuit [1]

During the charging phase, the switch (S) is turned 'OFF' and the high voltage power supply (V_{CC}) charges capacitor C_1 through a charging resistor (R_C) to the voltage level of V_{CC}. In the discharge phase, the switch is turned 'ON', and the CL oscillators ($C_1L_1$and C_2L_2) oscillate. The circuit can act as an electrical resonator, storing energy oscillating at the circuit's resonant frequency due to the CL circuit within a diode-based switch generator topology Fig. II.5(a). Energy is stored in the capacitor, in an electric field, and is depending on the voltage across it. The energy stored in a capacitor is $E = \frac{1}{2}CV^2$. In contrast, an inductor stores energy in its magnetic field and is depending on the current. The energy stored in the inductor is $E = \frac{1}{2}LI^2$. Where E is the energy stored, C is the capacitance, L is the inductance, V is the voltage, and I is the current across the respective component. The resonant frequency, *f*, or oscillation of the circuit is $f = \frac{1}{2\pi\sqrt{LC}}$.

The nsPEF across the load (Z_L) is formed by a diode stack (D_X) that rapidly interrupts the current of the oscillator in the third quarter of the period and transfers it into the load (Z_L). The diode-based switch pulse generator circuit is designed so that the reverse current in the diode is much higher than the forward current and that the depleting of the stored charge ends at the highest reverse current. Therefore, the induced current and voltage is very high across the load [1], [13]-[16].

Technology limitations

The main limitation of this topology is that the inductor cores are used in the LC oscillators, and these cores get easily saturated and limit the switching capability. A higher current is achieved with a saturable-core inductor for the LC oscillator as an alternative substrate to an air-core inductor, but this limits the switching speeds [1].

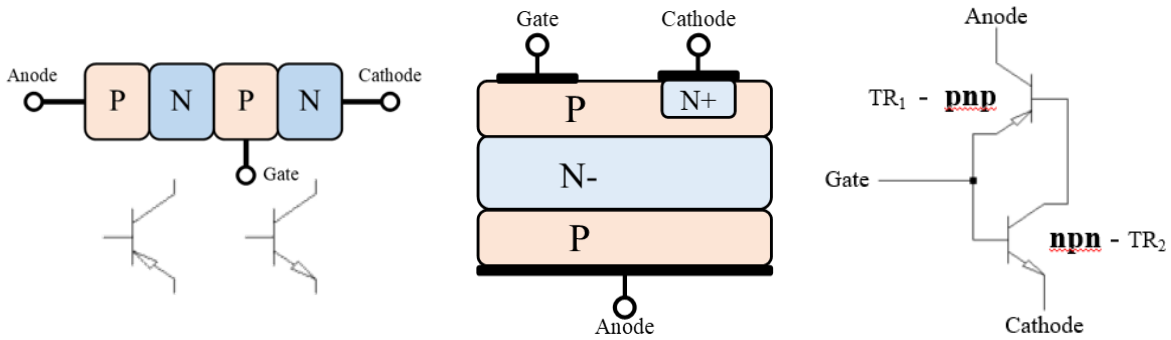
The advantage of a diode-based switch is that the electrical components are more accessible as the power supply does not generate the maximum output amplitude. Additionally, the switch does not need to withstand the whole nsPEF amplitude and does not affect the pulse transition and pulse width of the nsPEF generated. However, this advantage provides a complex generator design [1].

d) Thyristor Switch

Technology structure and operation

The structure of a thyristor is based on four layers of alternating p-type and n-type materials, i.e., forming a PNPN arrangement, with three terminals known as an anode, a cathode, and a gate as shown in Fig. II.5(a). The outer p-type material is the anode terminal whilst the outer n-type is the cathode terminal [1],[17]-[18]. A control terminal, named the gate, is in the p-type material next to the cathode as illustrated in Fig. II.5(a). Similar to other semiconductor-based technology, silicon is a popular material used for thyristors, yet other variants have been developed with silicon carbide (SiC), gallium nitride (GaN), diamond, etc. Each variant provides specific advantages in terms of thermal conductivity as well as a high voltage and current capability, and high operation frequency [1],[17]-[18].

The level of doping between the N and P layers of a thyristor varies. This is highlighted in Fig. II.5(b). The cathode N+ layer is the heaviest doped, whilst the P layers of the anode and gate are the next heavily doped. The lowest doped layer is the central N- layer, which is also the thickness layer. The level of doping and the thickness of the doping layer determines the breakdown voltage of a device with a thinner central N- layer providing a lower breakdown voltage [1],[17]-[18].



(a) (b) (c)

Fig. II.5. Thyristors structures (a) basic (b) fabrication (c) equivalent circuit [153]

The operation of thyristors can be explained in terms of a latching switch as its equivalent circuit. This model consists of two back-to-back transistors, one a PNP and the other an NPN, which forms a positive feedback loop, as shown in Fig. II.5(c). The output of the first transistor, TR_1, (base of the p-type transistor) feeds into the input of the second transistor TR_2, (collector of the n-type). In turn, the output of the second transistor (base of the n-type) feeds into the input of the first (collector of the p-type) transistor. This results in the total current gain of the device exceeding one, and therefore when a current starts to flow it accumulates until both transistors are in saturation [1],[17]-[19].

When a voltage is applied across a thyristor, no current flows as neither transistor, TR_1 and TR_2, is conducting and there is no complete path across the device. When a small current is applied to the thyristor gate electrode this will turn 'ON' TR_2, causing the collector of TR_2 to fall towards the voltage on the emitter or the cathode of the thyristor. When this occurs, current will flow through the base of TR_1 and turn this transistor 'ON'. Again, this will try to pull the voltage on the collector of TR_1 towards its emitter voltage. This will cause current to flow in the emitter of TR_2, causing its 'ON' state to be maintained. Therefore, a small trigger pulse on the gate is required to turn the thyristor 'ON'. Once switched 'ON', the thyristor can only be turned 'OFF' by removing the supply voltage [1],[17]-[19].

A thyristor is a bistable switch with a low-impedance 'ON' state and a high impedance 'OFF' state. Its static characteristics are shown in Fig. II.6. Region O-A of the thyristor is the forward blocking state, A-B is the negative resistance region, and region B-C is the forward conducting state. Region O-D is the reverse blocking state, and D-E is the reverse breakdown state [19]. There is only a single 'ON' state, the conducting state (region B-C), but there are two 'OFF' states. The forward blocking 'OFF' state (region O-A) and reverse blocking 'OFF' state (region O-D). The gate terminal can switch the thyristor from the forward blocking 'OFF' state to the forward conducting 'ON' state, but cannot operate in the reverse order, from the forward conducting 'ON' state to the forward blocking 'OFF' state [19].

Thyristors can be employed as the switching element within the nsPEF generation topologies such as the transmission line and Blumlein. Thyristors can be triggered by a positive pulse to the control grid at a repetition frequency of up to 10 kHz. With small hydrogen-filled thyratrons, pulsed electric fields with a pulse width of a couple of nanoseconds, and amplitudes up to 1 kA and 20 kV respectably have been reported in the literatures [1],[17]-[19].

Fig. II.7 shows a typical thyristor that can be incorporated into a transmission line pulse topology. An open transmission line, T_1, with an impedance characteristic of Z_0 and associated time delay of T is connected to the thyristor anode circuit. The line is charged to the voltage supply level of V_{CC}. The transmission line, T_1, is discharged through load, Z_L, after the thyristor is turned on using a trigger signal. This arrangement produces a symmetrical PEF of duration that is twice as long as the T_1-associated delay time, i.e., 2T. The relationship between load (Z_L) and the transmission line

characteristic impedance (Z_0), and the associated delay time of the transmission line (T_1) effect on the generated PEF amplitude and shape is the same as the description of the charged transmission line technology, a previous subsection of this chapter. If T_1 is replaced by a capacitor, an exponentially decaying pulse is produced across the load (Z_L) [20]-[21].

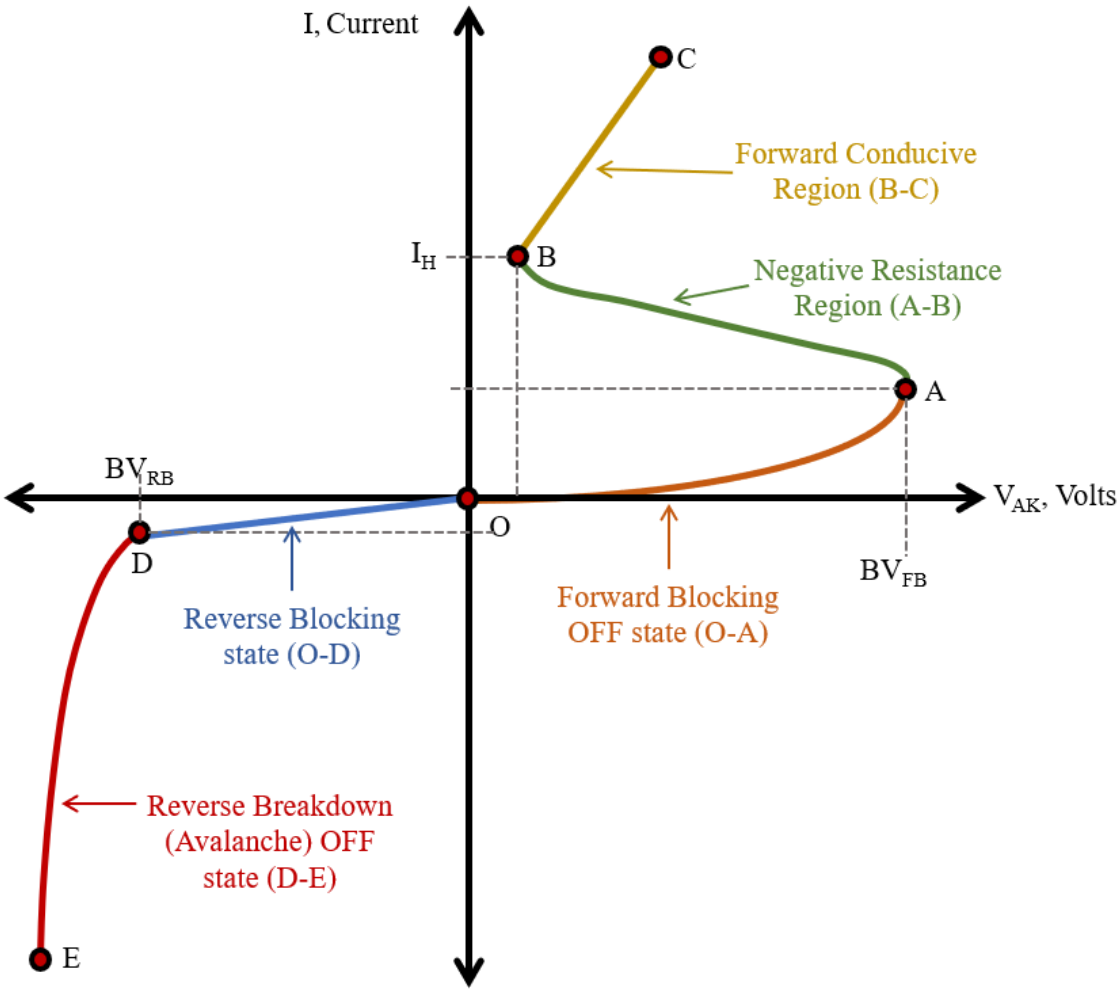


Fig. II.6. Static characteristics of a thyristor [19].

Fig. II.7 shows a typical thyristor that can be incorporated into a transmission line pulse topology. An open transmission line, T_1, with an impedance characteristic of Z_0 and associated time delay of T is connected to the thyristor anode circuit. The line is charged to the voltage supply level of V_{CC}. The transmission line, T_1, is discharged through load, Z_L, after the thyristor is turned on using a trigger signal. This arrangement produces a symmetrical PEF of duration that is twice as long as the T_1-associated delay time, i.e., 2T. The relationship between load (Z_L) and the transmission line characteristic impedance (Z_0), and the associated delay time of the transmission line (T_1) effect on the generated PEF amplitude and shape is the same as the description of the charged transmission line technology, a previous subsection of this chapter. If T_1 is replaced by a capacitor, an exponentially decaying pulse is produced across the load (Z_L) [20]-[21].

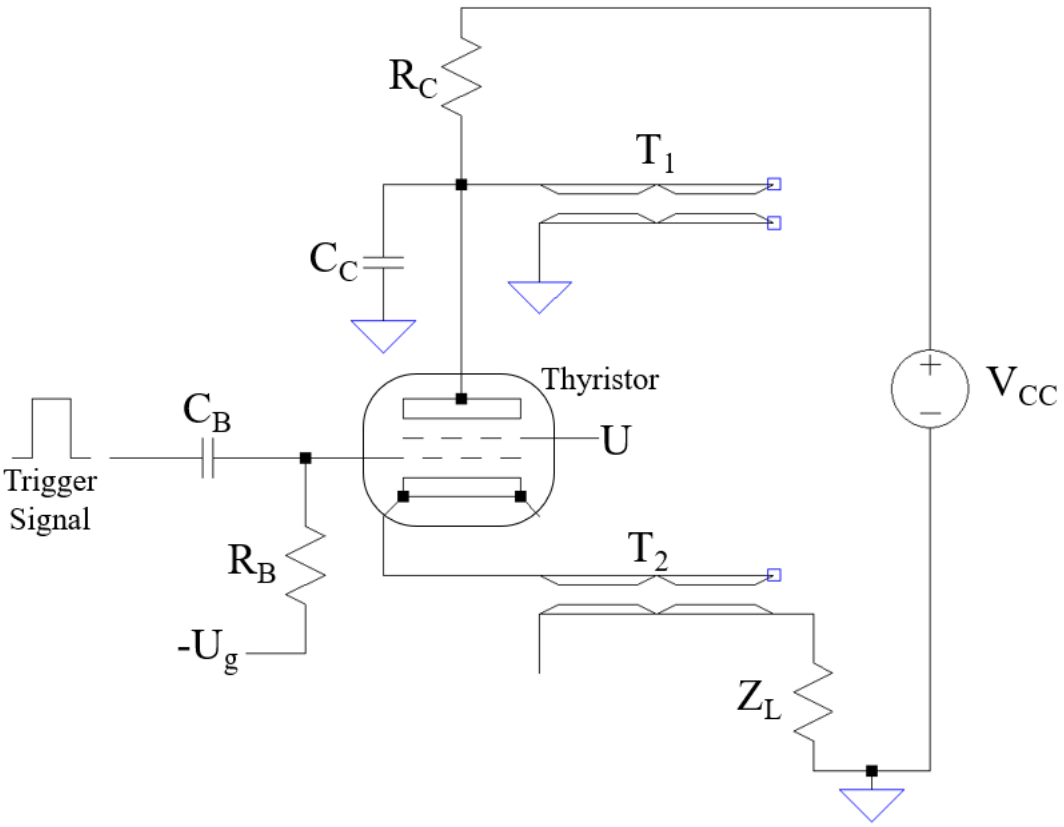


Fig. II.7. Thyristor incorporated in a transmission line pulser circuit for pulsed electric field generation [1]

Placing a capacitor C_c, of approximately 10 pF between the anode of the thyristor and the ground, as illustrated in Fig. II.7, reduces the rise and fall time of the output pulse. Capacitor C_c causes a higher current to flow through Z_L as it acts as a short circuit at switching and reduces the influence of the parasitic capacitance when the thyristor is switched. Additionally, the rise time can be reduced by using a pulse-shaping gap topology [1].

Technology limitations during operation

The delay time between the trigger signal and the output nsPEF could be a drawback of using a thyristor as a switch. This is because of the ionising time required to produce a delay between triggering and generating a nsPEF across a load. This time delay is dependent on the ionisation time, the thyratron geometry, and the operating voltages [151]-[154]. These delays can affect the repetition frequency of the nsPEF. Therefore, a precise triggering circuit for efficient timed pulse generation is required. This precise triggering circuit would need to consider the internal delay of the thyristor operation between the trigger input and nsPEF generation.

e) Bipolar Junction Transistor (BJT) Switch

Bipolar Junction Transistors (BJTs) are current-controlled devices or current-controlled switches, consisting of three regions, the collector, base, and emitter, where a small base current produces a large collector-emitter current.

Technology structure and operation

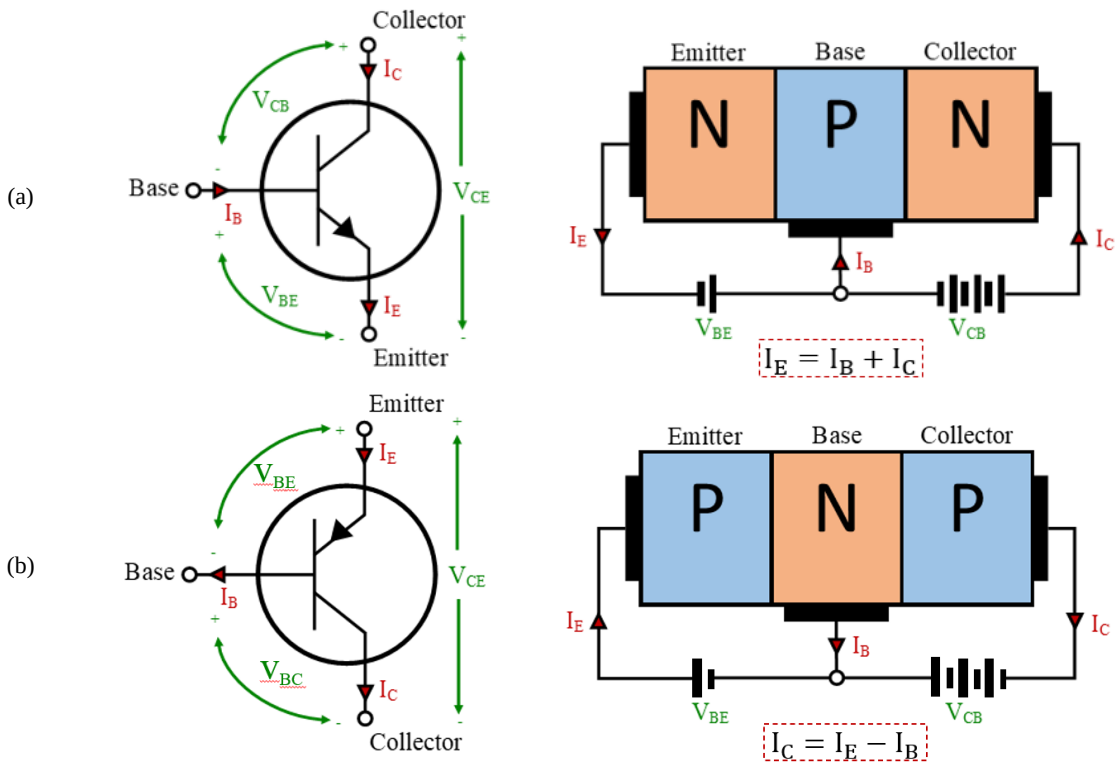


Fig. II.8. (a) NPN and (b) PNP bipolar junction transistor configuration [25]

A bipolar junction transistor is made from two p-n junctions with either two n-regions (NPN transistor) or two p-regions (PNP transistor) forming a common region, the base. The majority carriers of the emitter diode consist of holes in PNP transistors and electrons in NPN transistors as shown in Fig. II.8 [19], [22]-[25].

Technology characteristics

Transistor switching circuits generally fall into three basic device characteristics, depending on their operating mode. These modes are saturation, current active region, and avalanche mode, and are determined by the portion of the transistor output characteristics curve utilised. The operating regions for transistor switching modes are shown in Fig. II.9. For all modes, the switch-off conditions are characterized by an excursion of the load line into the cut-off region of the transistor. The operating mode is determined by the dc biasing arrangement which normally determines the operating points [19], [22]-[25].

Saturation Mode operates similar to a mechanical switch. In its 'OFF' condition, the current through the switch is extremely small. In its 'ON' condition, the transistor is driven into the saturation region that is distinguished as both the collector and emitter are injected into the base, and the transistor displays a virtual short circuit between its emitter and collector terminals [19], [22]-[25].

The bipolar junction transistor can produce high voltage outputs since the power dissipation is small in both the 'OFF' and the 'ON' conditions when the BJT is driven and its saturation or the base current is zero. When a transistor is driven into saturation mode its switching speeds are limited by the BJT's storage delay time [19], [22]-[25].

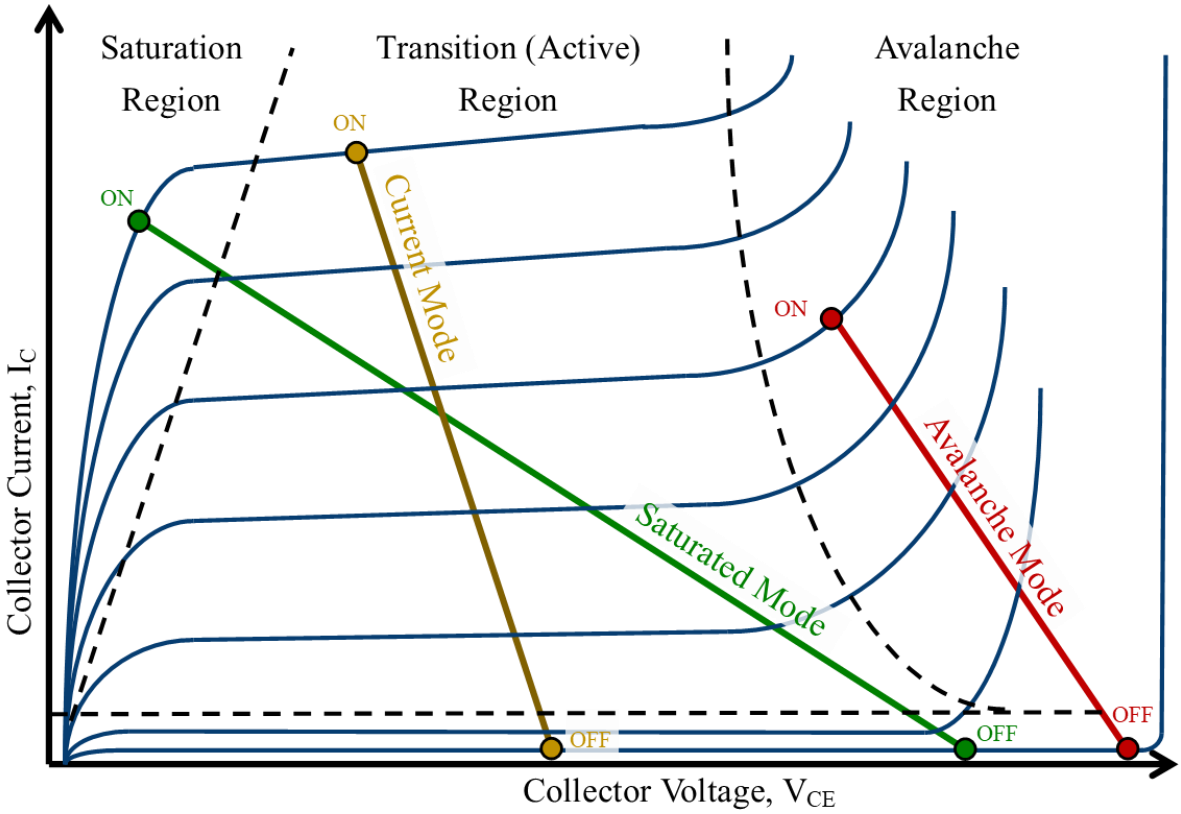


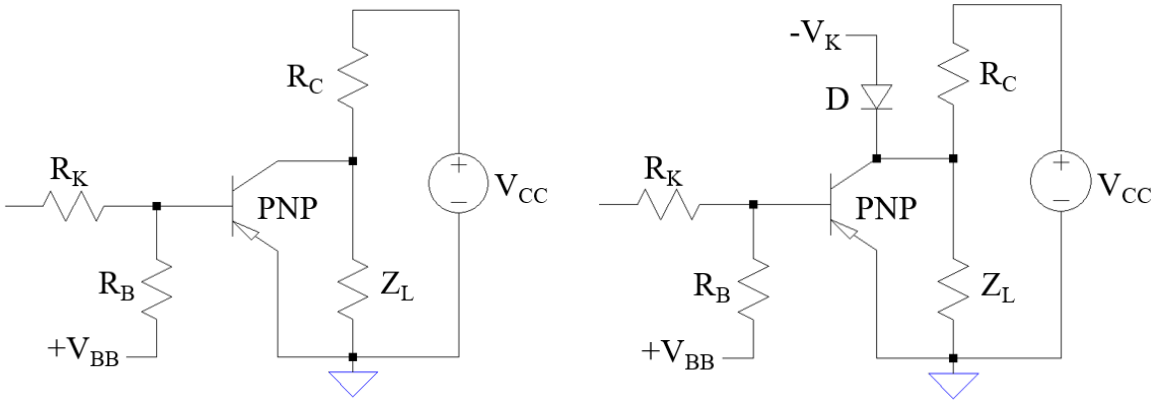
Fig. II.9. Operation region for switching modes of a transistor [19]

The circuits shown in Fig. II.10(a) and (b) are normally used for pulse/switching in saturation mode configuration. In this arrangement, the load (Z_L) is placed across the collector-emitter terminals of the BJT, and the load is virtually short-circuited when the resistor is 'ON'. When the transistor is 'ON', its output represents a virtual open circuit across the load. The load current approaches the limit value of $i_d = \frac{V_C}{(R_C+Z_L)}$ [19], [22]-[25].

The voltage across the load (Z_L) is dependent on the ratio of Z_L and R_C. When the transistor is in an 'OFF' position (high-level signal into the transistor base for a PNP transistor) a voltage of V_L $\left(= \left(\frac{Z_L}{Z_L+R_C}\right) V_{CC}\right)$ is seen across the Load. When the transistor is switched 'ON' (low-level signal into the transistor base for a PNP transistor) the transistor represents a short circuit across the load and no voltage is across the load. nsPEFs can be generated across the load by interpreting the switching mechanism of the transistor in its saturation mode [19], [22]-[25].

If a clamping diode D is included, as seen in Fig. II.10(b), a constant output level can be achieved. When the transistor is in its 'ON' state and represents a short circuit across the load, the diode does not

affect the performance of the circuit. If the load voltage attempts to exceed the value of V_K, the diode becomes conductive and clamps the output voltage to a value of $V_k + V_D$, where V_D represents the forward diode drop which is normally around 0.7 V [19], [22]-[25].



(a) (b)

Fig. II.10. (a) Saturated model of a transistor as a switching circuit (b) with clamp diode included [1]

Theoretically, it is possible to design the circuit so that the condition exists for all anticipated values of Z_L, as the output voltage will vary from virtually zero (transistor in saturation) to a fixed value (transistor in cut-off). This principle is dependent on the values of R_K and R_B for the correct 'ON' and 'OFF' conditions of the transistor to be met. The saturated voltage and input voltage of the transistor and its base leakage current in the 'OFF' condition must be known [19], [22]-[25].

A key drawback of the saturation mode operation is the storage delay time. There is an undesirable delay time between the change of the input voltage and the response of the transistor collector current. This delay is due to the overdrive, or excess base current that is used to drive the transistor into saturation. The excess base current results in an accumulation of stored charge in the base and/or collector, which must be removed before the collector current can change [19], [22]-[25].

Current Mode (Transition) operates a transistor in a current mode eliminates the storage delay time and allows the transistor to act as a high-speed switch. In a current mode circuit, shown Fig. II.11(a), a voltage source (V_{EE}) produces a current flow through a diode (D_E) and resistor (R_E). A voltage drop across the forward-biased diode appears between the emitter of the PNP transistor and the ground. A slightly positive signal on the base of the transistor places the transistor in its cut-off state. A negative signal on the base turns the transistor 'ON' and therefore the diode if 'OFF', and therefore not conducting [19], [22]-[25].

With the transistor in the cut-off, the current, I_E $\left(\frac{V_{EE}}{R_E}\right)$ flows through the diode (D_E); with the transistor turned on, current I_E flows into the emitter of the transistor. If the value of V_{CC} and Z_L are selected to limit the collector current, I_C $\left(\frac{V_{CC}}{Z_L}\right)$, and this current is greater than the emitter current, I_E $\left(\frac{V_{EE}}{R_E}\right)$, then the collector current cannot enter the saturation region. This current mode of operation

eliminates transistor saturation, which removes the storage time as a speed limiting factor [19], [22]-[25].

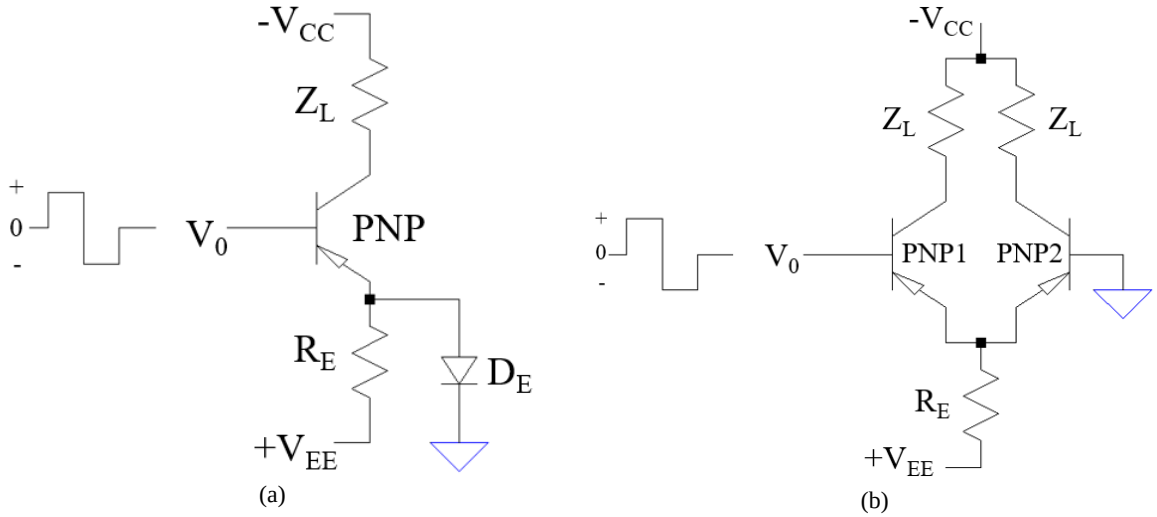


Fig. II.11. Current mode (a) basic circuit (b) circuit to generate complementary pulse outputs [1]

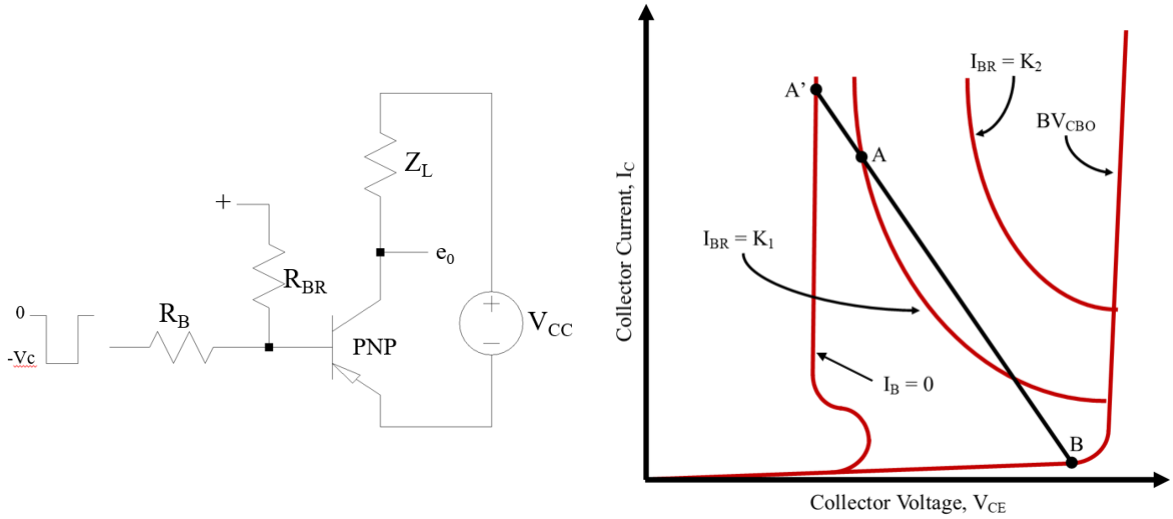
An enhanced more versatile current mode circuit that provides complimentary (out of phase) output signals simultaneously as shown in Fig. II.11(b). This arrangement provides additional advantages to a high speed by reducing the storage time. These include excellent dc stability, high noise immunity due to common mode noise rejection and non-critical transistor parameters. The disadvantage of this circuit is it requires a larger number of transistors in comparison with the single transistor circuit [19], [22]-[25].

The complementary output topology of a current mode circuit consists of replacing the diode, in Fig. II.11(a), but the circuit operates similarly to when the diode is used. When the second transistor, PNP2 (in Fig. II.11(b)), is conducting the emitter will have potential across the base-emitter voltage (V_B–V_E), V_{BE}. When the emitter is positive, the input signal at the base of PNP1, V_0, must be V_{BE}–V_T to keep PNP1 in a cut-off condition. V_T is the threshold voltage [19], [22]-[25].

As input signal V_0 becomes negative, the emitter current divides between the two transistors (PNP1 and 2) until V_0 has a value of $V_{BE} - V_T$. At this point, the emitter will be at a potential of V_T, causing the ground-base transistor (PNP2) to cut off and permitting all current from V_{EE} to flow through the base-emitter junction of PNP1 [19], [22]-[25].

The output voltage, $+e_0$, from PNP2 is in phase with the input signal, V_0, while $-e_0$, the output of PNP1 is 180° out of phase of e_0 and V_0. Thus, producing a simultaneous complementary output signal from a current mode circuit topology of transistors PNP1 and PNP2 connected in differential mode [19], [22]-[25].

Avalanche Mode operates a transistor in the common-emitter breakdown region utilizes the negative-resistance characteristics of the bipolar junction transistor. A basic avalanche mode circuit for a PNP transistor and its associated operating curves is illustrated in Fig. II.12 [19].



(a) (b)

Fig. II.12. Avalanche mode (a) basic circuit (b) load line operation [19]

Initially, a small reverse current holds the transistor operating point at Point B, where $I_{BR} = K_1$. If a negative trigger voltage is applied, the base current is reduced to zero, and the operating point of the transistor shifts to Point A' on the $I_B = 0$ curve, in Fig. II.12(b). The extreme transition speed with which the transistor does this is the main attraction of the avalanche mode operation as a fast switch. When the trigger pulse resides, the operating point shift to point A in Fig. II.12(b) and remains at this operating level. The switch has two stable states. To return to the 'OFF' state, Point B, it is necessary to apply sufficient reverse current to allow only a single stable condition. A small positive trigger signal accomplishes this, as indicated by $I_{BR} = K_2$ [19], overcome by alternating current (ac) coupling the input signal and so this arrangement has no use in logic systems [19], [22].

Technology limitations

Saturated and current mode transistors have further limitations in comparison to transistors operating in avalanche mode for the generation of high voltage nsPEFs. With a saturated transistor, the maximum switching speed from 'ON' to 'OFF' is limited by the charge storage time. The drawback of this arrangement is the safe operation area (SOA) of the transistor. The duration, voltage and current of the pulse are limited due to the high-power dissipation when transistor is working in its linear operating region [19], [22].

Avalanche mode differs from the normal transistor as they operate at a much higher breakdown collector voltage. Breakthrough between collector and emitter causes an avalanche-type current rise, which is equivalent to a transient switching time of ~300 ps. Avalanche mode operation of bipolar junction transistors is the preferred operating mode for high voltage nsPEF generation [19], [22].

f) Metal-Oxide-Semiconductor Field-Effect Transistor Switch

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are voltage-controlled devices, consisting of three terminals: gate, source, and drain. There are three types of MOSFET: the depletion-enhancement, enhancement and junction mode. Each of which is either p-channel or n-channel. The power version of the n-channel enhancement MOSFET is commonly used to implement switching circuits and is therefore explored in detail and used in this work.

Structure and operation

MOSFETs generally have a vertically oriented structure with a source, gate, and drain of alternating p-type and n-type doping. Enhancement mode MOSFETs do not conduct when there is no voltage across the gate-source voltage terminals ($V_{GS} = 0$). Each device is made up of several thousand cells, similar to that shown in Fig. II.13, where the $n^+ pn^- n^+ n^+ pn^- n^+$ structure forms the bias of an n-channel enhancement mode device [25]-[27]. In operation, the charge carriers enter the channel from the source and exit through the drain. The channel width is controlled by the voltage on the gate electrode which is located between the source and drain. It is insulated from the channel using an extremely thin layer (e.g., <1 nm) of metal oxide [25].

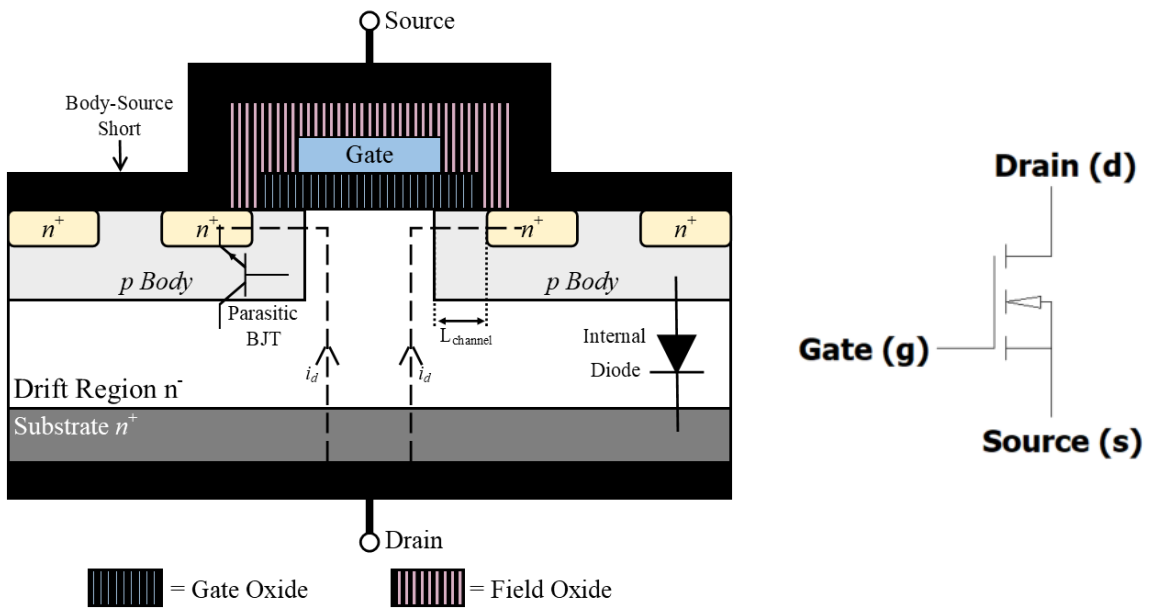


Fig. II.13. A single cell of an n-channel enhancement power metal-oxide-semiconductor field-effect transistors [25].

The doping of the n^+ end layers is large. The p-type middle layer channel is established between the source and drain. The n^- layer is the drift region and determines the drain-source breakdown voltage, BV_{DS}, of the device [25]-[27]. A vertical structure enables a short channel to be implemented, resulting in a small gate-source threshold voltage ($V_{GS(th)}$). There is no injection of minority carriers into the body region (p-type middle layer) via the gate terminal as the gate is isolated from the body by an insulator layer. Traditionally, the insulating layer consisted of silicon dioxide but recent advancements in material

science have resulted in the layer being constructed of SiC and GaN. Applying a voltage that biases the gate positive, with respect to the MOSFET's source, will convert the silicon surface beneath the gate oxide into an n-type layer/channel, thus connecting the source to the drain and allowing a drain current, i_d, to flow [25]-[27].

The number of gate-source regions connected electrically in parallel determines how current will flow for a given gate-source voltage, while the geometric shape of the source regions influences the drain-source on-state resistance ($R_{DS(on)}$). $R_{DS(on)}$ should be kept as small as possible for other devices to dissipate minimum power [25]-[27].

The on-state resistance affects the power the MOSFET must dissipate. The importance for the $R_{DS(on)}$ to be as small as possible is highlighted in Fig. II.14, and Table II.1.

Table II.1. illustrates the power dissipation and the voltage drop across a MOSFET with a different on-state resistance value of 0.1 Ω and 2 Ω, with a load, Z_L, values of 10 Ω and 100 Ω. The lower the on-state resistance of a MOSFET is the lower the power the MOSFET must dissipate and the voltage that is dropped across it. This implies that a larger PEF amplitude would be excreted on a load. Therefore, a MOSFET operating as a high voltage switch, with a low drain-source on-state resistance ($R_{DS(on)}$) the more desirable the MOSFET and the less power it requires to dissipate when switching.

Table II.1. Power dissipation and voltage drop across a metal-oxide-semiconductor field-effect transistors when switching a 100 V supply with various load (V_L) and ON-resistance ($R_{DS(on)}$) values

Example	V_{CC} *(V)*	Z_L *(Ω)*	$R_{DS(on)}$ *(Ω)*	V_L *(V)*	i_d *(A)*	P_L *(W)*	V_{drop} *(V)*	P_{dis} *(W)*
1	100	100	2.0	98.04	0.98	96.12	1.96	1.92
2	100	100	0.1	99.90	1.00	99.80	0.10	0.10
3	100	10	2.0	83.33	8.30	694.44	16.67	138.89
4	100	10	0.1	99.01	9.90	980.30	0.99	9.80

The figures in Table II.1 for the power dissipation and voltage drop across the MOSFET were calculated. The voltage drop across the MOSFET can be calculated by $V_{drop} = \left(\frac{R_{DS(on)}}{Z_L + R_{DS(on)}}\right) V_{cc}$. The power dissipated across the MOSFET can be calculated by $P_{dis} = \frac{V_{drop}^2}{R_{DS(on)}}$. The voltage drop across a load is $V_L = \left(\frac{Z_L}{Z_L + R_{DS(on)}}\right) V_{cc}$ and the current through a load is $i_d = \frac{V_L}{Z_L}$. Finally, the power dissipated across a load is $P_L = \frac{V_L^2}{Z_L} = i_d V_L$.

Where V_{CC} is the power supply voltage at that Marx single stage, V_{drop} is the voltage drop across a switching element, $R_{DS(on)}$ is the ON-resistance of the switching element, Z_L the load resistance, P_{dis} is the power dissipated across the switching element, V_L the voltage across the load Z_L, i_d is the current through the circuit and P_L is the power dissipated by the load Z_L.

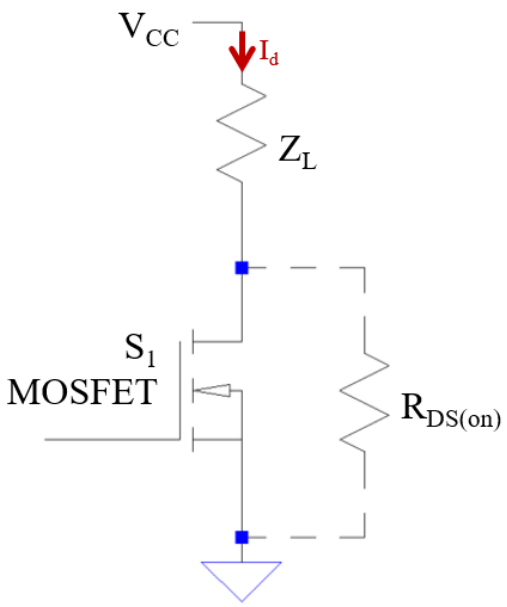


Fig. II.14. Basic metal-oxide-semiconductor field-effect transistors switching circuit to produce pulses.

The input gate voltage controls the flow of the current between the drain and source output terminals. The output characteristics: drain current, i_d, as a function of drain-source voltage (V_{DS}) with the gate-source voltage (V_{GS}) as a parameter, are illustrated in Fig. II.15 for an n-channel enhancement device. When used as a switch in a power application, the MOSFET traverses the $i_d - V_{DS}$ characteristics from cut-off through the active (saturation) region, to the ohmic region as the device is turned 'ON', and back again when turned 'OFF'. The device is in its cut-off region when the gate-source voltage is less than the threshold voltage ($V_{GS(th)}$). When in cut-off the device is an open circuit and must hold off the power supply applied to the circuit. The drain-source breakdown voltage (BV_{DS}) must be larger than the applied drain-source voltage to avoid breakdown [25]-[27].

When the device is driven by a high V_{GS}, it will be operating in the ohmic region, where V_{DS} is small. The condition for operating in this region is given by equation (II.1). In the active (saturation) region the drain current (i_d) is independent of the drain-source voltage (V_{DS}) and depends solely on the value of the gate-source voltage (V_{GS}). In this region, the channel is said to be in pinch-off and the device can be used to provide a reliable constant current source [25]-[27].

$$V_{GS} - V_{GS(th)} > V_{GS} > 0 \tag{II.1}$$

When operating in this region the drain current is given by equation (II.2).

$$i_d = \mu_n C_{ox} \frac{W_{gate}}{2L_{channel}} \left(V_{GS} - V_{GS(th)}\right)^2 (1 - \lambda V_{DS}) \tag{II.2}$$

where V_{GS} is the gate-source voltage, $V_{GS(th)}$ is the gate-source threshold voltage. μ_n is the inversion layer majority carrier mobility (in $cm^2V^{-1}s^{-1}$), C_{ox} is the capacitance due to the gate oxide layer, W_{gate} is the gate width and $L_{channel}$ is the channel length. The λ term is the channel length modulation

parameter which describes the spread of the pinch-off region into the channel (reduces in length when V_{DS} is increased). When λ is multiplied by V_{DS} this gives the drain-source resistance, $R_{DS(on)}$ [25]-[27].

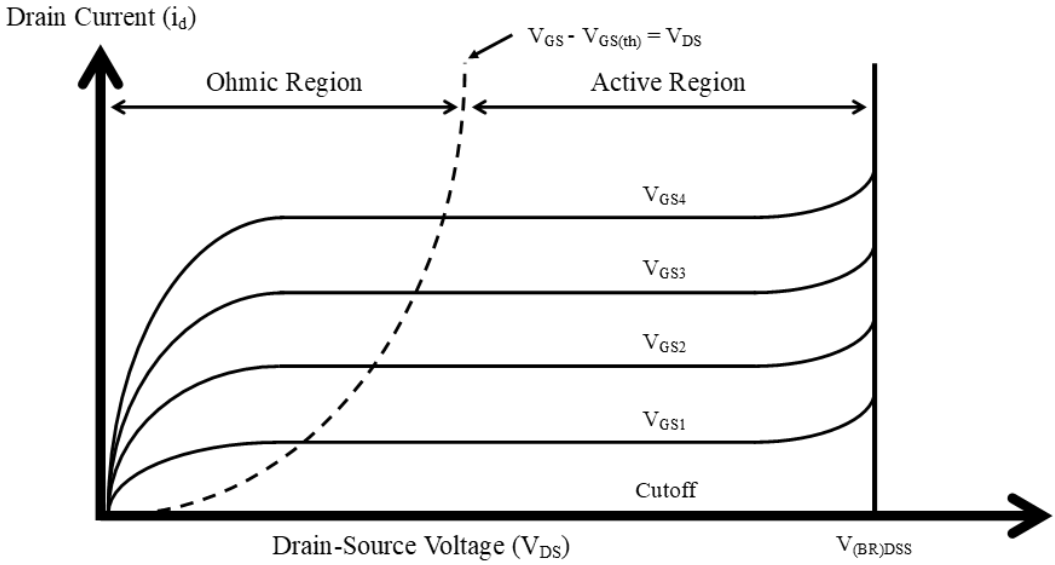


Fig. II.15. Output characterises of a power metal-oxide-semiconductor field-effect transistors [26].

At the boundary between the ohmic and active regions, $V_{GS} - V_{GS(th)} = V_{DS}$. The slope of the transconductance curve $\frac{i_d}{V_{GS}}$ is approximately constant for high drain currents, thus giving a constant transconductance, g_m, value for the device. As shown in Fig. II.16 [25]-[27].

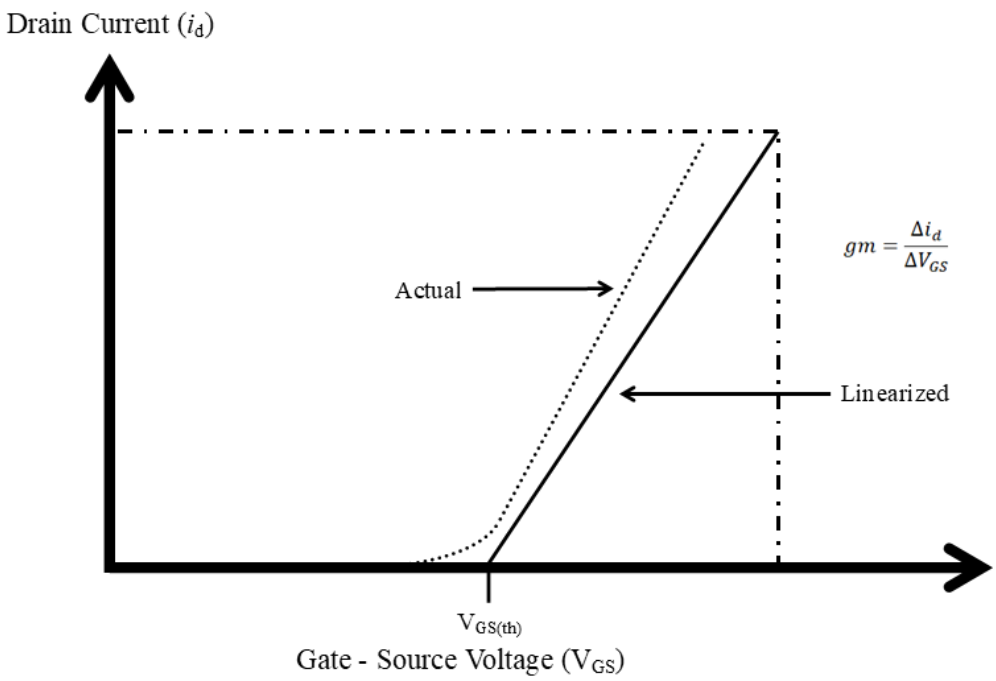


Fig. II.16. Metal-oxide-semiconductor field-effect transistors transconductance curve [26]

Limitations on the use of MOSFET as a high voltage fast switch

Latch-up causes high-power dissipation within the device, which can lead to thermal damage. This occurs when the MOSFET goes into saturation. As the length of the MOSFET body is short to minimise the ON-resistance ($R_{DS(on)}$) the gain of the device can be high. If the base was left to float, the breakdown voltage (BV_{DS}) would be reduced and the base-emitter voltage (V_{BE}) of the bipolar junction transistor within the MOSFET, (as seen in Fig. II.13) and becomes significantly faster in terms of turning the device 'ON', as the MOSFET goes into saturation. When the BJT, within the MOSFET, is 'ON' it cannot be turned 'OFF', as the base is not accessible. Interrupting the drain current flow is the only method of switching the BJT 'OFF'. To prevent the BJT from being turned 'ON', the p-body is shorted to the source. This results in a parasitic diode between the drain and the source of the MOSFET. With the body short circuit, the BJT can be turned 'ON' if the device is turned 'OFF' very quickly, thus slowing the fall time, or turn 'OFF' edge of the peak is required to ensure this does not happen when switching 'OFF' the MOSFET [25]-[27].

MOSFET devices have a maximum gate-source voltage (V_{GSmax}) that must not be exceeded. This factor is determined by the gate thickness of the oxide layer and the magnitude of the applied electric field. Once the drain-source breakdown voltage (BV_{DS}) is exceeded, the breakdown of the gate oxide will occur, and the MOSFET is permanently damaged [25]-[27]. The maximum drain-source voltage, or breakdown voltage, must not be exceeded as this is the largest voltage that the device can hold off without avalanche breakdown of the drain-body PN junction occurring.

When designing a switching circuit that uses MOSFETs it must be ensured that the parameters above are not exceeded, and that the device is operated within the SOA. To summarise, three features that determine the SOA are the maximum drain current, i_d, the internal operating junction temperature (T_J) (governed by the power dissipation in the device), and the drain-source breakdown voltage (BV_{DS}) [25]-[27].

MOSFETs can be designed in a push-pull or full bridge amplifier configuration for the generation of bipolar pulses and as a means of doubling the amplitude of the pulse and quadrupling the power.

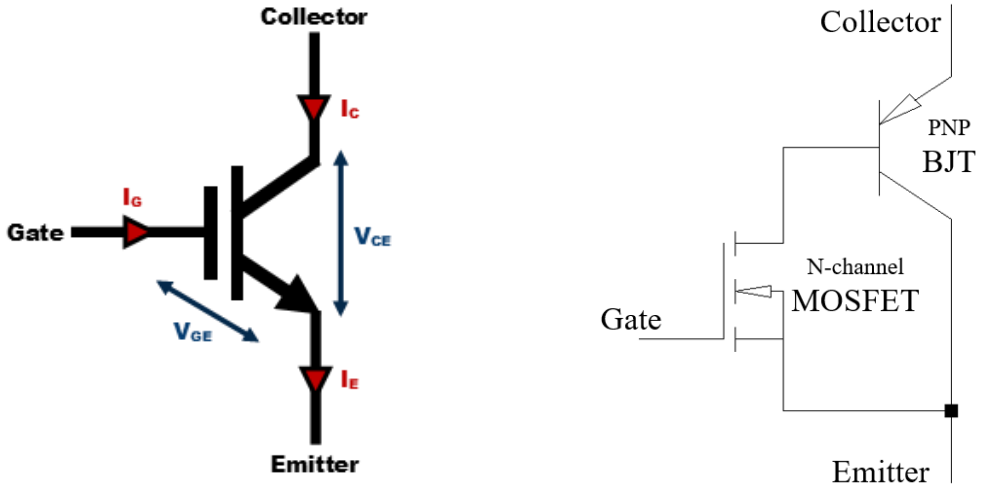
g) Insulated-Gate Bipolar Junction Transistor Switch

Structure and operation

An Insulated-Gate Bipolar Junction Transistors (IGBJTs) is a functional integration of a MOSFET and bipolar junction transistor in a monolithic form. The IGBJT combines the attributes of the insulated gate technology of a MOSFET and the output performance characteristics of a conventional BJT with no integral diode. An IGBJT is capable of handling large collector-emitter currents with virtually zero gate current drive. The key attributes associated with the IGBJT include the high input impedance input

and high switching speeds of a MOSFET, and the low saturation voltage of a bipolar transistor [18], [25], [28].

IGBJTs have three terminals, a collector, gate, and emitter as shown in Fig. II.17. It can be repented as an n-channel MOSFET integrated with a p-type transistor in a Darlington-type configuration as shown in Fig. II.17(b). Its collector to emitter terminals is associated with a conductive path which passes a current that is controlled by the gate terminal [18], [25], [28].



(a) (b)

Fig. II.17. Insulated-gate bipolar junction transistor (a) circuit symbol (b) equivalent circuit [25]

IGBJTs are mainly used in power electronics applications, such as inverters, converters, and switch mode power supplies, where the demands of the solid-state switching device are not fully met by power BJTs and MOSFETs. The IGBJT combines the low conduction loss of a BJT with the high switching speed of a power MOSFET, thus these devices are ideal for use in power electronics applications [18], [25], [28].

The forward blocking operation of the IGBJT is identical to a power MOSFET, but they have a much lower "on-state" resistance, or ON-resistance ($R_{DS(on)}$). Therefore, the I^2R power dissipation associated with the bipolar output structure for a given switching current is much lower than that of a MOSFET. As a voltage-controlled switch, the IGBJT has similar current and voltage ratings to that of a BJT, but the inclusion of an isolated gate in the IGBJT indicates a smaller continuous current is required. But the capacitance associated with the isolated gate has to be changed which can lead to the requirement of a large transient current for switching [18], [25], [28].

The IGBJT is a unidirectional voltage-controlled device and a small voltage on the gate is required to maintain current conduction through the device, from its collector to its emitter. The operation of the gate drive circuit is like that of a MOSFET. IGBJTs are turned 'ON' and 'OFF' by a control/trigger signal to their gate terminal. Applying a positive input voltage signal across the gate and emitter will

turn the device 'ON' and keep the device in the 'ON' state. While a zero or negative voltage signal would turn the IGBJT switch 'OFF' [18], [25], [28].

The advantages of IGBJTs are their capability of handling large currents and voltages, with a low drain-source ON-resistance ($R_{DS(on)}$) and a simple drive circuit. This makes IGBJTs a good candidate for moderate speed, high voltage applications such as pulse width modulated (PWM), variable speed control and switch-mode power supplies.

Technology limitations

High-current and high voltage IGBJTs offer greater power gain, higher voltage operation and lower input losses, but they have lower switching speeds in comparison to other semiconductor power devices. This is the key limitation of IGBJTs for the generation of nsPEF. The output pulse rise time for high voltage IGBJTs has been said to be in the hundreds of nanoseconds regime, with the minimum rise time reported as 52.4 ns [28].

Appendix I References

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Appendix III - C2M1000170D Silicon Carbide Power metal-oxide-semiconductor field-effect transistor (MOSFET) Datasheet

CREE

C2M1000170D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
N-Channel Enhancement Mode

V_{DS}	1700 V
$I_{D\ @\ 25°C}$	5.0 A
$R_{DS(on)}$	1.0 Ω

Features

- High Speed Switching with Low Capacitances
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to Parallel and Simple to Drive
- Ultra-low Drain-gate capacitance
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Increased System Switching Frequency
- Reduced Cooling Requirements
- Increased System Reliability

Applications

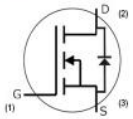
- Auxiliary Power Supplies
- Switch Mode Power Supplies
- High-voltage Capacitive Loads

Package

TO-247-3

Halogen-Free

RoHS



Part Number	Package
C2M1000170D	TO-247-3

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1700	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	5.0	A	V_{GS} = 20 V, T_C = 25°C	Fig. 19
		3.5		V_{GS} = 20 V, T_C = 100°C	
$I_{D(pulse)}$	Pulsed Drain Current	6.0	A	Pulse width t_P, limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	69	W	T_C=25°C, T_J = 150 °C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	°C		
T_L	Solder Temperature	260	°C	1.6mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

CREE

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.4	3.1		V	V_{DS} = 10 V, I_D = 0.5 mA	Fig. 11
		1.8	2.3		V	V_{DS} = 10 V, I_D = 0.5 mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS} = 1.7 kV, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		1.0	1.4	Ω	V_{GS} = 20 V, I_D = 2 A	Fig. 4,5,6
			2.0			V_{GS} = 20 V, I_D = 2 A, T_J = 150 °C	
g_{fs}	Transconductance		0.82		S	V_{DS}= 20 V, I_{DS}= 2 A	Fig. 7
			0.81			V_{DS}= 20 V, I_{DS}= 2 A, T_J = 150 °C	
C_{iss}	Input Capacitance		200		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		12				
C_{rss}	Reverse Transfer Capacitance		1.3				
E_{oss}	C_{oss} Stored Energy		7		μJ		Fig 16
E_{ON}	Turn-On Switching Energy		40		μJ	V_{DS} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A, $R_{G(ext)}$ = 2.5 Ω, L= 1478 μH, T_J = 150 °C	Fig. 26
E_{OFF}	Turn Off Switching Energy		15				
$t_{d(on)}$	Turn-On Delay Time		6		ns	V_{DS} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 600 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		10.5				
$t_{d(off)}$	Turn-Off Delay Time		11				
t_f	Fall Time		60				
$R_{G(int)}$	Internal Gate Resistance		24.8		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		4.7		nC	V_{DS} = 1.2 kV, V_{GS} = -5/20 V I_D = 2 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		5.4				
Q_g	Total Gate Charge		13				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.8		V	V_{GS} = - 5 V, I_{SD} = 1 A, T_J = 25 °C	Fig. 8, 9, 10
		3.3		V	V_{GS} = - 5 V, I_{SD} = 1 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		4	A	T_C= 25 °C	Note 1
t_{rr}	Reverse Recovery Time	20		ns	V_{GS} = - 5 V, I_{SD} = 2 A T_J = 25 °C V_R = 1.2 kV dif/dt = 1200 A/μs	Note 1
Q_{rr}	Reverse Recovery Charge	24		nC		
I_{rrm}	Peak Reverse Recovery Current	6.5		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.7	1.8	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

Appendix IV - FS Series (FS40) Isolated proportional dc to HV dc Converters Datasheet

Proven Reliability

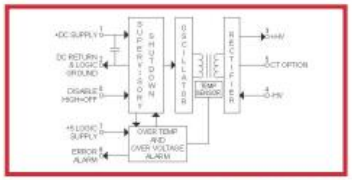
FS SERIES

ISOLATED, PROPORTIONAL DC TO HV DC CONVERTERS

200V to 6kV at 10W

PRODUCT DESCRIPTION

The new FS Series of isolated, proportional DC to high voltage DC converters offers stout design and enhanced features for excellent long term reliability. Outputs ranging from 200V through 6kV are offered in miniature, cost-effective, PC-mount packages. Based on XP-EMCO's proven high-reliability, high voltage power conversion topology, the FS Series boasts a full ten watts of output power for each model and features a low 0.7V turn-on voltage. The output voltage is proportional to the input voltage, from turn on to maximum output voltage, enabling easy control of the high voltage. XP-EMCO's proprietary, quasi-sin-ewave, resonant oscillator produces clean, reliable high voltage with inherently low ripple, low EMI/RFI, low input ripple current, and low conducted emissions. Additional features such as arc protection[*], short circuit protection, surge current limiting, and over-temperature protection are available.



APPLICATIONS

- Electrophoresis
- Piezo Devices
- Capacitor Charging
- Mass Spectrometry
- Electrostatic Chucks

OPTIONS

- Available in Four Standard Input Voltage Ranges: 0–12, 15, 24, and 28V. (For Other Input / Output Voltages, Consult Factory)
- Polarity: Choose Negative or Positive Outputs for Models FS50 and FS60
- Output Center Tap: Available for Models FS02CT through FS40CT
- B Version - Without Enhanced Features. See 'B' Drawing.
- Extended Operating Temperature: -55° to +85°C (Case)(-T Option)[*6]
- Extended Environmental Screening and Burn-In Available, Consult Factory

PRODUCT SELECTION TABLE

MODEL	OUTPUT VOLTAGE*2 (POSITIVE OR NEGATIVE)	OUTPUT CURRENT *1	OUTPUT POWER*4
FS02	0 to 200V	50mA	0 to 10W
FS03	0 to 300V	33.3mA	0 to 10W
FS05	0 to 500V	20mA	0 to 10W
FS10	0 to 1kV	10mA	0 to 10W
FS20	0 to 2kV	5mA	0 to 10W
FS30	0 to 3kV	3.33mA	0 to 10W
FS40	0 to 4kV	2.5mA	0 to 10W
FS50	0 to 5kV	2mA	0 to 10W
FS60	0 to 6kV	1.67mA	0 to 10W

Complete List of Models on pages 2 and 3

FEATURES

- Output Proportional and Linear to Input
  <0.7V Turn-On Voltage
- **SMART FEATURES** for Enhanced Reliability:
  Over-Temperature Protection with Automatic Shutdown and Error Code
  Over-Voltage Protection with Automatic Shutdown and Error Code Output
- Disable Pin, TTL Compatible High=Off
- No Minimum Load Current Required
- Low-Noise, Quasi-Sinewave Oscillator
- Inaudible >25kHz Oscillator, Low EMI/RFI
- Low Conducted Emissions and Low Input Ripple Current
- Stable Operating Frequency Over Entire Operating Range
- High Input to Output Galvanic Isolation
- Very Low Input/Output Leakage Current: <100nA
- Very Low Input/Output Coupling Capacitance: <100pF
- Reversible Output Polarity (4kV Modules and Below)
- High Efficiency, No Derating Required
- Robust Design: Conservative Internal High Voltage Clearance and Voltage Gradient Control for Exceptional Long-Term Reliability
- Arc Protection[*] and Short Circuit Protection[*5]
- Output Surge Current Limited
- High Reliability: MTBF > 840,000 Hours per Belcore TR 332
- Excellent Internal Thermal Management
- Anodized Aluminum Heatsink Surface
- Two Threaded, Blind Inserts Allow for Easy Heatsinking and/or Chassis Mounting Options
- UL Certified Encapsulant, Meets 94V-0 Flammability
- RoHS Compliant

ISO 9001:2008 CERTIFIED ISO 14001:2004 CERTIFIED RoHS COMPLIANT IPC

ELECTRICAL SPECIFICATIONS*3

MODEL	OUTPUT CURRENT	RIPPLE*4	REVERSIBLE MODEL	OUTPUT VOLTAGE	CENTER TAP MODEL	OUTPUT VOLTAGE
FS02/FS02CT	50mA	<6%	FS02	0 to 200 VDC	FS02CT	0 to +/- 100V
FS03/FS03CT	33.3mA	<2%	FS03	0 to 300 VDC	FS03CT	0 to +/- 150V
FS05/FS05CT	20mA	<2%	FS05	0 to 500VDC	FS05CT	0 to +/- 250V
FS10/FS10CT	10mA	<1%	FS10	0 to 1 kV	FS10CT	0 to +/- 500V
FS20/FS20CT	5mA	<2.5%	FS20	0 to 2kV	FS20CT	0 to +/- 1kV
FS30/FS30CT	3.33mA	<2%	FS30	0 to 3kV	FS30CT	0 to +/- 1.5kV
FS40/FS40CT	2.5mA	<1.5%	FS40	0 to 4kV	FS40CT	0 to +/- 2kV
MODEL	**OUTPUT CURRENT**	**RIPPLE*4**	**POSITIVE MODEL**	**OUTPUT VOLTAGE**	**NEGATIVE MODEL**	**OUTPUT VOLTAGE**
FS50P/FS50N	2mA	<2.5%	FS50P	0 to +5kV	FS50N	0 to -5kV
FS60P/FS60N	1.67mA	<2.5%	FS60P	0 to +6kV	FS60N	0 to -6kV

	INPUT CURRENT			
	UP to FS40		FS50 & FS60	
VIN	NO-LOAD	FULL-LOAD	NO-LOAD	FULL-LOAD
12V	<0.3A	<1.25A	<0.4A	<1.5A
15V	<0.25A	<1.15A	<0.34A	<1.25A
24V	<0.15A	<0.65A	<0.2A	<0.75A
28V	<0.125A	<0.5A	<0.175A	<0.65A

ELECTRICAL SPECIFICATIONS[1,3]

PARAMETER	VALUE
TURN-ON VOLTAGE	0.7V TYPICAL
ISOLATION	< +/- 2,500V BIAS ON PIN 4
OPERATING TEMPERATURE	-25° to +75°C (CASE)[4,6]
OPTIONAL EXTENDED OPERATING TEMPERATURE	-55° to +85°C (CASE)[4,6]
STORAGE TEMPERATURE	-55° to +85°C
OUTPUT VOLTAGE TOLERANCE	+/-3% FULL LOAD
EFFICIENCY	75% - 85% TYPICAL
INPUT CAPACITANCE	188uF (12V AND 15V in)
	88uF (24V AND 28V)
FREQUENCY	25 TO 125kHz

DETAILED PRODUCT DESCRIPTION

The new FS Series of isolated, proportional DC to high voltage DC converters offers stout design and enhanced features for excellent long-term reliability. Outputs ranging from 200V through 6kV are offered in miniature, cost-effective, PC-mount packages. Based on XP-EMCO's proven high-reliability, high voltage power conversion topology, the FS Series boasts a full ten watts of output power for each model and features a low 0.7V turn-on voltage. The output voltage is proportional to the input voltage, from turn on to maximum output voltage, enabling easy control of the high voltage. XP-EMCO's proprietary, quasi-sinewave, resonant oscillator produces clean, reliable high voltage with inherently low ripple, low EMI/RFI, low input ripple current, and low conducted emissions. The frequency of the oscillator is stable throughout the operating range, allowing for easy additional filtering, and always operates well above the audio frequency range.

This series features sturdy, galvanic input-to-output high voltage isolation, conservatively rated at +/-2,500V + Vout with less than 100pF of coupling capacitance and less than 100nA of leakage current. Robustness and high reliability have been designed into each model by incorporating output arc surge current limiting and short circuit protection. Careful control over internal voltage gradients extends the useful life calculated. Mean time between failure (per Bellcore TR-332) exceeds 840,000 hours.

In addition, the internal transformer temperature and input voltage are actively monitored with supervisory circuits and fed into a shutdown circuit, preventing excessive input voltage or over-temperature failures. Should preset limits be exceeded, the module will automatically shut down and issue an error signal on pin 6 (TTL high).

When the fault condition is removed, the unit restores itself to normal operation, ensuring maximum reliability in the field. However, the pin 6 error signal will remain high until reset by power cycling the +5V logic. The fault monitor circuit is powered by an external 5V to allow for 0.7 to full input voltage proportional operation of the high voltage converter. The FS Series also features an enable/disable function. A TTL high signal on Pin #8 disables the high voltage output.

High power conversion efficiency, coupled with low internal thermal resistance, creates a vigorous package able to withstand wide operating temperatures. A unique integrated anodized aluminum heatsink surface features two threaded blind inserts, which allow for optimal thermal management via external heatsink for high temperature operation and/or convenient chassis mounting configurations. A special proprietary encapsulating formula optimizes internal dielectric strength that is UL-94V0 compliant while low thermal resistance minimizes internal component temperature rise, resulting in a robust module optimized for long-term reliability.

Appendix V - FMMT415 | FMMT417 npn avalanche transistor in SOT23 Datasheet

DIODES INCORPORATED

Lead-free Green

FMMT415
FMMT417

NPN AVALANCHE TRANSISTOR IN SOT23

Features

- Avalanche Transistor
- 60A Peak Avalanche Current (Pulse width = 20ns)
- BV_{CES} > 260V (415) & 320V (417)
- BV_{CEO} > 100V
- Specifically designed for Avalanche mode operation
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.008 grams (Approximate)

Description

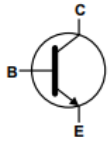
The FMMT415/417 are NPN silicon planar bipolar transistors designed for operating in avalanche mode. Tight process control and low inductance packaging combine to produce high-current pulses with fast edges.

Applications

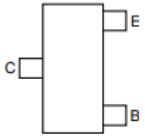
- Laser Diode Drivers for Ranging and Measurement (LIDAR)
- Radar Systems
- Fast Edge Switch Generator
- High Speed Pulse Generators

SOT23

Top View



Device Symbol



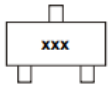
Top View
Pin-Out

Ordering Information (Note 4)

Product	Compliance	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
FMMT415TD	AEC-Q101	415	7	8	500
FMMT417TD	AEC-Q101	417	7	8	500

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



xxx = Product Type Marking Code
(See Ordering Information)

DIODES INCORPORATED

FMMT415
FMMT417

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	FMMT415	FMMT417	Unit
Collector-Base Voltage	V_{CBO}	260	320	V
Collector-Emitter Voltage	V_{CES}	260	320	V
Collector-Emitter Voltage	V_{CEO}	100	100	V
Emitter-Base Voltage	V_{EBO}	6		V
Continuous Collector Current	I_C	500		mA
Peak Collector Current (Pulse Width = 20ns)	I_{CM}	60		A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Power Dissipation	(Note 5)	P_D	500	mW
Thermal Resistance, Junction to Ambient	(Note 5)	$R_{\theta JA}$	250	°C/W
Thermal Resistance, Junction to Lead	(Note 6)	$R_{\theta JL}$	197	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

ESD Ratings (Note 7)

Characteristic	Symbol	Value	Unit	JEDEC Class
Electrostatic Discharge - Human Body Model	ESD HBM	4,000	V	3A
Electrostatic Discharge - Machine Model	ESD MM	400	V	C

Notes:
5. For a device mounted with the collector lead on 15mm x 15mm 1oz copper that is on a single-sided 1.6mm FR4 PCB; device is measured under still air conditions whilst operating in a steady-state.
6. Thermal resistance from junction to solder-point (at the end of the collector lead).
7. Refer to JEDEC specification JESD22-A114 and JESD22-A115.

Appendix VI - User manual of the slow nanosecond pulsed electric field (nsPEF) electroporation system

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User's guide

Concept project number:	Q7
Project title:	Electroporation: SUMCASTEC Pulse Generator 1 – "SPG-1"
Reference:	ENEA Dec. 17

Table of Contents

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Concept Lab

1. Document history

Date and name	Change	SW revision
15 Dec. 2017 Ilan Davies	First draft.	
20 Dec. 2017 Ilan Davies	Second draft.	
08 Aug. 2017 Ilan Davies	Third draft.	
17 Sept. 2018 Ilan Davies	Fourth draft.	

1.1. Omissions

- No predefined treatments available in software
- Update software to show percentage voltage at load

2. Description

The Concept project, Q7 Electroporation, is a prototype nanosecond pulsed electric field (nPEF) generator that contains a high-voltage unit (FS40) from XP-Power that can deliver 1.4kV pulsed with pulse width of 80 ns up to 1µs. This is the first electroporation generator funded by the European Union's Horizon 2020 Framework Programme FET OPEN, research and innovation under grant agreement N° 737164. This is the first concept of two to three generator for the Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells (SUMCASTEC) project generating with the slowest and smallest nPEF. Please read the safety considerations on page 10.

3. Familiarisation

The front panel is shown in Figure 1.

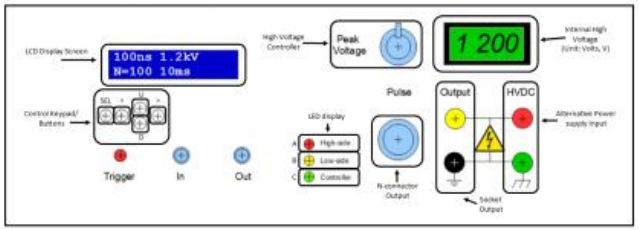

Figure 1 Q7 SPG-1 front panel

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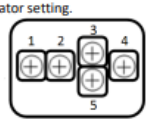
LCD Display Screen: Interaction display. Displays current generator settings.

Control Keypad/Buttons: Keypad/Buttons that interact and control the generator setting.

Button Number	*Control Operation*	*On Screen Representation*
1	Select	SEL
2	Left	>
3	Up	U
4	Right	<
5	Down	D



High Voltage Controller: Controls the high voltage output (the pulse voltage amplitude).

Rotate Clockwise – Increases Output Voltage

Rotate Anticlockwise – Decrease Output Voltage

Internal High Voltage: Displays the voltage (in volts) the voltage supplied by the generator internal High voltage supply (FS40)

LED Display: LED display indicates power source status to various PCB within the generator.

LED On: Power is delivered to PCB.

LED Off: PCB are not powered. Indicate possible problem (short circuit, faulty component etc) on the indicated PCB.

A – Red LED: High-side 20V power source and high-side driver circuit.

B – Yellow LED: Low-side 20V power source and low-side driver circuit.

C – Green LED: 5V power source for controller.

N-connector Output: Output source of generated nanosecond pulse via.

Socket Output: Output source of generated nanosecond pulse via twisted wires.

Black connector - Ground Yellow connector - Positive (+ve) Output

Alternative Power Supply Input: An alternative power (voltage) supply can be inputted into generator. The voltage supplied here will determine the amplitude of the nanosecond pulse generated.

Positive supply to the **Red** connector

Ground (negative) supply to Green connector.

Note: *Internal High Voltage supply must be disconnected manually from within the generator (disconnecting the connector between the variable voltage supply PCB and the high voltage power source FS40) Alternative power supply must be a DC supply and* ***NOT*** *exceed 1700V.*

Trigger BNC Connectors:

Out BNC: The control clock signal from the generator. The generator internal clock pulse or external clk pulse, depending on setting, is outputted form this BNC connector.

In BNC: Send external control clock signal to trigger pulse generation. The repletion frequency of nanosecond pulses will be dependent on the clock signal sent into the In BNC connector.

4. Switch on and off

The generator will operate from AC supplies of 110V to 240V and dissipates approximately 1400V, 10W power when delivering pulses.

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4.1. Switching on

Plug in an IEC mains connector and turn the mains power switch on. The three LED display will light-up and the internal high voltage monitor will display ~0 'V'. The unit will boot up and show two welcoming messages. Following the welcoming message the first of four pulse characterisation selection will be display, "Pulse Width".

4.2. Switching off

It is safe to turn the generator off make sure the generator is not generating high voltage pulses. If so press the select button and wait for the first of four-pulse characterisation selection, "Pulse Width" to be displayed. Then you may switch the main power switch off at the back of the generator and unplug the IEC main connector.

5. Mode selection

The nPEF that will be generated from the generator has four characterisation mode to select. Pulse width, repetition frequency, number of pulses or burst and internal or external pulse clock trigger.

Setting Menu: Characterisation of nanosecond pulses

Characteristics	*Abbreviation*	*Description*	*Range*
Pulse Width	PW	Sets the pulse width	80ns - 1us
Burst of Pulses	B	Sets the number of pulses in the burst mode to generate before inhibiting output.	Continuous generation of pulses, or 1-1000 bursts
-	Cont.	Generate continuous pulses until the Select button (SEL) is pressed	-
Trigger	Tr	Select if the repetition frequency of generated pulses is dependant on an external clock trigger or generator internal clock trigger (In). The clock signal used can be sent from the generator for monitoring also (out).	N/N, Y/N, N/Y, Y/Y
Frequency	F	Sets output frequency of the unit (which determines the fundamental T_0 period).	1Hz - 50Hz

Pressing the left "<" or right ">" button allows the user to change between the various pulse characterisation menu.

Pressing the up "U" or down "D" button allows the use to change the selected characterisation requirement. i.e. in pulse width characterisation menu up to increase the pulse width required or down to decrease.

The select button is the button to start or stop the generator of expulsing high voltage pulses of nanosecond width.

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6. Configuration

Step 1: Switching Generator On:

Switch the switch at the back of the unit.
User greeted with two automated welcome messages.

Step 2: Select Output Pulse Settings:

Characteristics as: Pulse Width (W), Frequency (F) and Burst (B) (number of pulses to be generated) and Trigger.

Change the characteristic value: Press Up (U) and Down (D) on keypad

Move between selected pulse characteristic: Press Left (<) and Right (>) keypad buttons.

Selecting Pulse Width (PW):
Press Up, (U) and Down, (D) buttons to select Pulse Width.
From 80ns to 1000ns. (increment of 10ns between 80ns to 400ns and increment of 20ns between 400ns and 1000ns)
Press Left, < button to selecting the Burst / number of pulses to generate option.
Press Right, > button to select Frequency / repetition frequency of pulses to generate option.
Press Select (SEL) button for the SPGI to start generating pulses (*Step 3).*

Selecting Frequency (F):
Press Up, (U) and Down, (D) buttons to select the repetition frequency.
From 1Hz to 50Hz (increment of 1Hz)
Press Left, < button to select Pulse Width of pulses to generate option.
Press Right, > button to selecting the Trigger function option.
Press Select (SEL) button for the SPGI to start generating pulses (*Step 3).*

Selecting Trigger Mode (Tr):
Press Up, (U) and Down, (D) buttons to select the trigger function.

N/N – Generator operates with internal Clock function and no output clock signal generated.
N/Y - Generator operates with internal Clock function and clock signal used is generated on the 'Out' BNC connector
Y/N - Generator operates with external Clock function and no output clock signal generated.
Y/Y - Generator operates with external Clock function and clock signal used is generated on the 'Out' BNC connector.

Press Left, < button to select Trigger function option.
Press Right, > button to select Pulse Width of pulses to generate option.
Press Select (SEL) button for the SPGI to start generating pulses (*Step 3).*

Selecting Burst Mode (B):
Press Up, (U) and Down, (D) buttons to select the number of Bursts / number of pulses to be generate. *Note: 'Cont'. mean continuous generation of Pulses*

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From single pulse to continuous generation of pulses.
Press Left, < button to select Trigger function option.
Press Right, > button to select Pulse Width of pulses to generate option.
Press Select (SEL) button for the SPGI to start generating pulses (*Step 3).*

Step 3: Generating Nanosecond Pulses:

Press Select (SEL) button when in any of the generator setting option.
Pulses will be generated from the generator n-connector or Output banana connectors.
Three sequences of event will occur:

Message 1: "Generator Ready". Clock pulse width setting are entered
Message 2: "Charging!". Enable High Voltage supply and charging High Voltage capacitor. *(**Note:** Internal High Voltage display on the top right hand of the front panel should be increasing to ~1300-1400)*
Message 3: "Generator On". Generating nanosecond pulses

Note:
- Warning High Voltage)
- Pulse Voltage Amplitude can be adjusted by turning the *high voltage controller* knob at any time during operation.

Step 5: Stop Generation of Pulses:

Pulses will automatically stop being generated after specific amount of pulses have been generated. (Depending on value selected in Burst mode setting).
If in continuous mode: Press Select (SEL) keypad button to stop the generation of pulses.
After termination of pulses the screen will revert back to setting menu. Specifically Pulse Width mode.

Note:
- Press Select (SEL) button for Emergency Stop to halt generation of nanosecond pulses.
- This can be done anytime during generation of continuous or during bursting a specific number of bursts.
- The Internal High Voltage display on the top right hand of the front panel should be decreasing to indicate ~0-40.

Turn SPGI generator off:

Switch the switch at the back of the unit.
Do not turn the generator off while the generator is in *Step 4 or 5*

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7. Fault Detection

7.1. Common Fault 1:

Indicator: LED displays

If any of the LED display on the front panel are off then there is a fault on a specific PCB(s).

Red LED indicates a fault has occurred on the high-side power source and driver circuit
Yellow LED indicates a fault has occurred on the low-side power source and driver circuit.
Green LED indicates a fault has occurred on the 5V power source for controller.

The main cause of this is a short circuit in the indicated PCB.
If either or both Red and Yellow LEDs are off, then the source of this fault is most likely because of a short circuit. The common solution is replacing the opto-coupler.

If the fault is still present further fault finding and troubleshooting is required.

7.2. Common Fault 2:

Indicator: Internal High Voltage Display.

If the internal high voltage display (top right-hand side of the front panel) does not increase in Step 3, Message 2 (described in the Operation section of the manual). Then this indicates a fault with the high voltage source.

The fault is most likely caused by a defected (shorted out) MOSFET. The common solution is to replace the MOSFET(s).

If the fault is still present further fault finding and troubleshooting is required.

8. High level specifications

- 1.4kV, 10W peak pulse amplitude.2kW peak power 120W average power (10W minimum peak power)
- Minimum/maximum pulse width: 80ns/1us
- Configurable voltage level and durations number of pulse and repletion rate of pulse with display for power and energy delivered
- N output connector and/or banana connector
- 100:1 build in attenuator.

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9. Safety considerations

High voltage is dangerous.

This User's guide is not a safety guide for appropriate precautions to observe when handling microwave radiation. The user should be fully experienced and trained in safe handling procedures for microwave generators and delivery of high-level microwave power before attempting to use this generator.

Additional precautions to observe when using this generator:

i. Only authorised users may operate this generator.
ii. Read this guide and be familiar with the operating instructions before use.
iii. The generator contains a hardware-wired footswitch AND logical input for master enable/disable. Software provides secondary control, so removing pressure from the blue foot-pedal will always turn off microwave power from the output.
iv. Never look into the output connector of the generator.
v. Never modify the footswitch (e.g. by use of weights, clamps or otherwise) to allow unsupervised power delivery. The user must always be present and in active control of the generator during power delivery.
vi. If in doubt about any aspect of operation of the generator then seek guidance from Creo Medical Concept Lab.

10. Contact

Ilan Wyn Davies

Address:
Creo Medical
Unit 2
Riverside Court
Bath
BA2 3DZ
UK
E-mail: ilan.davies@creomedical.com
Phone: +44 1225 303457

Appendix VII - User manual of the fast nanosecond pulsed electric field (nsPEF) electroporation system

Concept Project Name	**Sumcastec EP**
Concept Projects Sequential Code	**Q7**
Filename	**CS-000079-DC-A-SumcasteePG-3InstructionManual.docx**
Saved date	**08 November 2022 13:41**
Author	**Ilan Wyn Davies**

SUMCASTEC Pulse Generator 3 – SPG-3

1kV, 10 ns Pulse generation

Generation Fast Pulsed Electric Field Generator

User Manual

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Q7-Electroporation

User Guide

Concept Project Number	Q7
Project Tittle	SUMCASTEC Pulse Generator 3 – SPG-3
Purpose	User Manuel
Reference	ENEA Sept. 17

Document History

Version	Date	Changes	By
1	29th Sept. 2020	First Draft	Ilan Davies

Acronyms

nsPEF	-	Nanosecond Pulsed Electric Field
PPE	-	Personal Protective Equipment
SSW	-	Safe System of Work
SUMCASTEC	-	Semiconductor-based Ultrawideband Micromanipulation of CAncer STEm Cells
VNA	-	Vector Network Analyzer

Contents

1. Introduction

1.1. General Description

SUMCASTEC Pulse Generator 3 (SPG-3) is a porotype nanosecond pulsed electric field generator that can provide a wide arrange of pulsed electric field of 1 kV amplitude, with a rise and fall time less than 2 ns. The pulse parameters such as pulse width, amplitude and repletion rate is selected by external signal that are required as input to the generator. The instrument may be operated with either a positive or negative pulse polarity terminal ground, as selected by grounding the opposite connector output.

The SPG-3 is a design that based on relatively slow charging and ultrafast discharging of a co-axial transmission line in conjunction with a stack of low-cost avalanche breakdown transistors which operate as a fast switching element to generate sub 2 ns rise time. A FS40-12 DC to high voltage DC converter is incorporated to generate the DC high voltage supply.

1.2. Receiving Inspection

This instrument has been thoroughly checked and tested before being shipped from the factory. Immediately after receiving the instrument, carefully inspect for damage which may have occurred in transit. If any damaged is noted, contact relevant department as outlined on the Contact page in the back of this manual.

2. Specifications

2.1. Electrical

Output Voltage:	0 to 1000 V
Output Polarity:	Positive or Negative, *Select by grounding the inverse connector output*
Pulse Width:	10 ns – 300 ns. *The pulse duration is depending on the transmission line length that is connected*
Rise and Fall Time:	< 2 ns
Repetition Frequency:	1 Hz – 1 kHz with a 10 ns transmission line. *The rate is limited to the charging time of the cable used.*
Pulse Amplitude:	1 kV *The amplitude can be reduced or increase but may affect pulse generation efficiency. Increase may cause permanent damage to avalanche transistors used.*
Load Regulation:	50 Ω *Design to match 50 Ω load at either the positive or negative output OR 25Ω on both load. This will produce best pulse outcome with reflection minimized.*
Output Connectors:	50Ω Straight Panel Mount N Connector

2.2. Mechanical

Humidity:	0 to 80 %
Operating Temperature Range:	0 °C to 50 °C
Storage Temperature Range:	-20 °C to +70 °C
Size:	88.1 mm x 482.6 mm x 285 mm

3. Familiarization

3.1. Front Panel

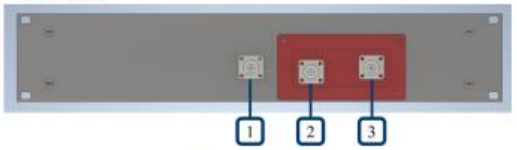


Figure-1, Front Panel

3.2. Back Panel

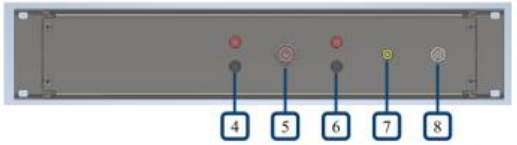


Figure-2, Back Panel

3.3. Top View

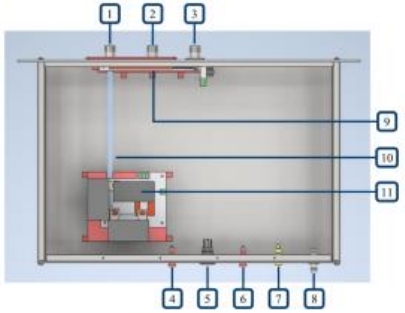


Figure-3, Top View

3.4. Components

Ref Design	Location	Components	Function
1	Front Panel	n-connector	Positive nsPEF Output
2	Front Panel	n-connector	Negative nsPEF Output
3	Front Panel	n-connector	Transmission Line Input: *Determine nsPEF duration / width*
4	Back Panel	Banana Connector	**0 V - 7.8 Vmax** V High Voltage Control; DC to High Voltage DC (FS40) Controller: *Determine nsPEF amplitude*
5	Back Panel	Push Button Switch	On/Off Switch: Switches the high voltage supply on and off and the nsPEF output.
6	Back Panel	Banana Connector	**5 V input:** *Essential for the nsPEF generator to work. Make sure 5V input before you switch on.*
7	Back Panel	Banana Connector	Error output: from internal DC to High Voltage DC (FS40) power supply issue an error signal when signal is high
8	Back Panel	BNC	Trigger signal input: *Determine nsPEF repletion rate and number of pulses.* ***5V (TTL), 600 ns pulses.***
9	Bottom Plate	Avalanche Circuit	Stacked avalanche breakdown transistors (FMMT417 x10) circuit. *Act as a fast switching element*
10	Bottom Plate	High Power Resistors	1 MΩ Resistor HVR*3700001004FR500 - Through Hole Resistor, 1 Mohm, HVR37 Series, 500 mW, ± 1%, 3.5 kV*
11	Bottom Plate	High Voltage Circuit	Generate High Voltage DC from a DC to High Voltage DC (FS40) supply.

4. Operation Instructions

4.1. Initialisation

Step 1: Check the stacked Avalanche transistor impedance

- Measure the impedance across each transistor. The impedance across each transistor should be about the same value. (Figure -4)
- ~ 430 kΩ to ~480 kΩ

If the impedance value across a transistor is vastly different from others in the stack it indicates that this transistor is broken and needs to be replaced.

Note the red output from the multi-meter should be place on the lower end of the transistor (facing the n-connector connection for the positive nsPEF output / transformer).

Figure-4, Measuring transistor impedance

Step 2: Provide necessary Input/Output connection to the instrument

Ref Design	See Figure	Input/Output	Source	Description / Supply
1	1 and 3	Output	Load	*n/a*
2	1 and 3	Output	Load	*n/a*
3	1 and 3	Input	Transmission Line	*n/a*
4	2 and 3	Input - Red	0 – 7.8 V DC	DC Power Supply
		Input - Black	Ground	
5	2 and 3	Input	On/Off Button	Push Button
6	2 and 3	Input - Red	5 V DC	DC Power Supply
		Input - Black	Ground	
7	2 and 3	Output	Monitor TTL output	Oscilloscope
8	2 and 3	Input	5 V (TTL), 600 ns pulse width.	Signal Generator

Note: is it imperative that the 5V DC input (Ref Design 5) is delivered into the instrument before any other inputs is switched on.

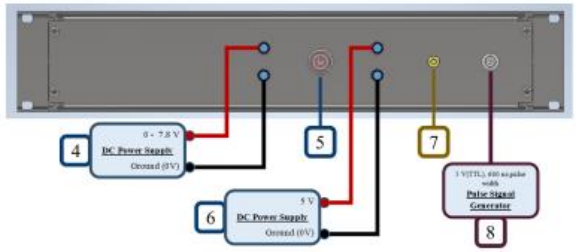


Figure-5, Initialisation Set-up

4.2. Switching On and Off

To switch the instrument on press the push button, Ref Design Input 5 in Figure 2. If the button is pressed in this means the instrument is on. ***Note: the red LED light will always be on.***

Switching this switch on will switch the high voltage supply of the instrument on.

nsPEF generation will not occur until you provide the relevant trigger / initialisation signal to the instrument by a pulse signal generator connected to the back-panel Ref Design Input 8

4.3. Pulse Generation

Parameters of the generated nsPEF can be adjusted. nsPEF parameters include polarity (negative or positive), width (duration), repetition rate and number of pulses.

Pulse Polarity

The polarity of the output can be selected by shorting the undesirable output you required.

Example of shorting an output by connecting the inner and outer of a male n-connector (Figure-6). Connecting the connector (Figure-6) to positive output connector (Ref Design Output 1 in Figure 1) and a load on the negative output connector (Ref Design Output 1 in Figure 1) would produce a negative nsPEF polarity on the load. And vice versa.

Pulse Polarity Required	Positive Output Connector Ref Design Output 1 in Figure 1	Negative Output Connector Ref Design Output 2 in Figure 1
Positive	Load	Short
Negative	Short	Load

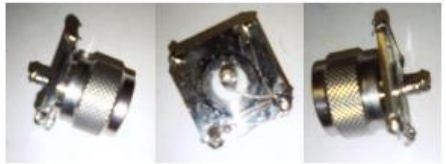
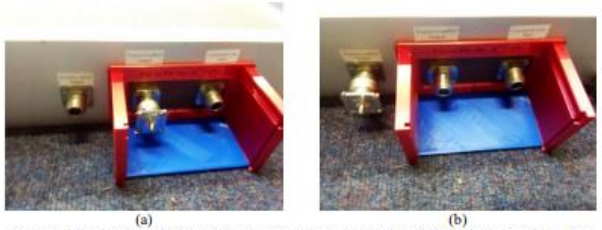


Figure-6: Short connector for nsPEF polarity selection



(a) (b)

Figure-7, The shorting of a connection outputs to generate a (a) positive and (b) negative nsPEF

Pulse Width

Pulse width of the nsPEF is depending on the length of the open-ended transmission line that will be connected to the transmission line n-connector input Ref Design Output 3 in Figure 1.

Transmission line length required:

Calculate length:

1) The calculated delay time of the microstrip cable within the instrument is 1.3 ns
2) Subtraction 1.3ns from the pulse width you desire which is t
3) Calculate the length of the open-circuit transmission line you required

$$length, l = \frac{\left(\frac{c}{\sqrt{\varepsilon_r}}\right)}{\left(\frac{t}{2}\right)}$$

c is the speed of light ($3x10^8$m/s),
ε_r is the dielectric constant of the dialectic material used for the transmission line
t is subtracting 1.3ns form the pulse width you required

Then cut the transmission line to the length calculated and create a cable assembly with the coaxial transmission line and a suitable connector at one end of the cut transmission line. Do not connect a connector on the other end, keeping an open-circuit termination.

To confirm the delay in the cable you have assembled can be verified via a VNA.

Example: for a 10ns pulse.

1) 10 ns – 1.3 ns = 8.7ns
2) 8.7 ns/2 = 4.35 ns
3) $l = \frac{\left(\frac{3x10^8}{\sqrt{\varepsilon_r}}\right)}{4.35x10^{-9}}$

Connector and Cable suggestion:

Cable: RG214/U Coaxial Cable, *RS: 521-8391*

Connector: Telegartner 50Ω Straight Cable Mount N Connector, Plug, *RS: 112-2094*

Pulse Amplitude

The amplitude of the nsPEF is dependent on the DC input into Ref Design 4, in Figure 2.

The instrument is designed to produce a 1 kV nsPEF.

A 7 V input into Ref Design 4, in Figure 2.

Further details are in section 4.4. Operational Notes

Repetition Rate

The repetition rate is determined by the trigger signal input into Ref Design 8, in Figure 2.

The recommended trigger signal is a 5V (TTL) pulse of 600 ns. The repletion rate of the trigger signal determines the repletion rate of the high voltage nsPEF generated by the instrument.

Note: The maximum repetition rate that can be generated is limited by the open-circuit transmission line length (pulse width)

Suggested maximum repletion rates:*

*10 ns pulses – 1 m open-circuit transmission line length – 1 kHz max, suggested 500 Hz max**

*50 ns pulse– 5 m open-circuit transmission line length – 250 Hz max, **

*200 ns pulse– 20 m open-circuit transmission line length – 100 Hz max**

**using RG214/U Coaxial Cable, RS: 521-8391*

Number of Pulses

The instrument produces a nsPEF when triggered by the trigger signal input into Ref Design 8, in Figure 2.

The trigger signal dictates the number and when a nsPEF is generated.

4.4. Operational Notes

First Time Use

Important notice for first use of interment after following above instructions:

When the instrument is first used it important to probe with a high voltage probe the high voltage side, preferable following the high-power resistor on the avalanche circuit side (Figure-8).

Then turn the external DC power supply into Ref Design 4, in Figure 2, and increase from 0 V input and increase gradually until the voltage at the probing point is 2.5 kV. – 2.7 kV.

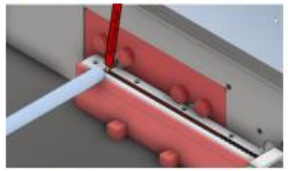


Figure-8: High Voltage probing for initial use

Load / Loading

The instrument is load sensitive, due to the use of transmission line design.

Optimal Load: 50 Ω Load

5. Maintenance

5.1. List of Replaceable Parts

This section contains information to describe all normally replaceable parts. Each list has a corresponding illustration on which the parts for that list are identified. Part are called out on both list and illustration by reference designation from the schematic diagram.

Each list provides the following information:

Ref Design: indicates the reference designation used on the schematic diagram

Description: describes the part in words, along with any applicable values, tolerance etc.

MFR: Indicate a typical manufacturer /distributor of the part.

MFR Part #: part number assigned by the manufacturer indicated.

Total Qty: total quantity of the part used in the instrument.

Chassis				
Ref Design	**Description**	**MFR**	**MFR Part #**	**Total Qty**
The Chassis	*2U Rack Chassis*	Farnell	1816035	1
The Chassis	*2U Rack Handle*	Farnell	1370448	1
1, 2, 3	*Straight Panel Mount N Connector*	RS	819-4443	3
4, 6	*RS PRO Black, Red Female Test Socket*	RS	191-7883	1
5	*Latching Blue LED Push Button Switch*	RS	194-2055	1
7	*Staubli Yellow Female Banana Plug*	RS	122-9721	1
8	*Straight 50Ω RF Adapter BNC Socket to BNC Socket*	RS	546-4572	1
9	*Front Panel Insulator Jig*	Creo	CS-000087-DG	1

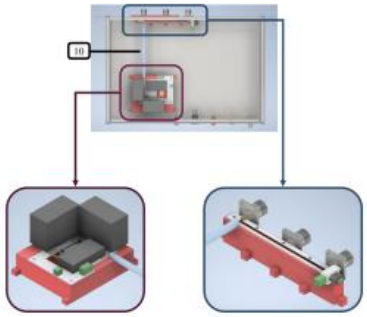


Figure-11, Internal components reference designation

Avalanche Circuit				
Ref Design	***Description***	**MFR**	**MFR Part #**	**Total Qty**
10	*Through Hole High Voltage Resistor, 1 Mohm,*	Farnell	1551410	1
11	*PCB Avalanche Circuit*	CREO	CS-000083-DG	1
12	*Avalanche Circuit Jig*	CREO	CS-000084-DG	1
13	*Gate Drive Transformer*	CREO	1-EMR-046	1
14	*FMMT417TD Avalanche Mode Transistors*	MOUSER	522-FMMT417TD	10

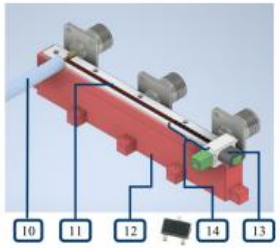


Figure-12, Avalanche Circuit component reference designation

High Voltage Supply Circuit				
Ref Design	***Description***	**MFR**	**MFR Part #**	**Total Qty**
15	*1 uF High Voltage Capacitor*	RS	7757545	2
16	*3.3Meg Ohm Resistor*	RS	849-2788	2
17	*DC-High Voltage DC Isolated 10 W 4kV*	RS	1238405	1
18	*3 Way, 1 Row, Straight PCB Header*	RS	4838477	1
19	*2 Way, 1 Row, Straight PCB Header*	RS	483-8461	1
20	*PCB Power Supply*	CREO	CS-000085-DG	1
21	*Power Supply Jig*	CREO	CS-000086-DG	1

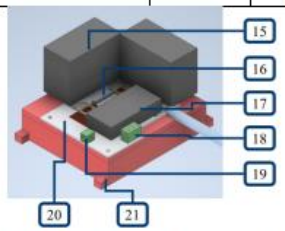


Figure-13, High voltage supply component reference designation

5.2. Wire Diagram

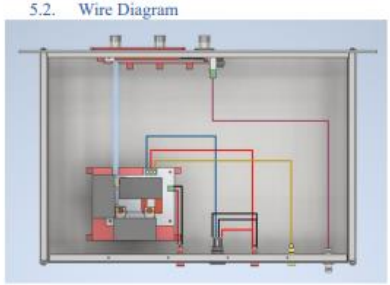


Figure-14 Internal wiring diagram

6. Safety Considerations

6.1. High Voltage

HIGH VOLTAGE: HAZARD OF ELECTRICAL SHOCK. DISCONNECT INCOMING POWER BEFORE WORKING ON THIS CONTROL

HIGH VOLTAGE: Dangerous voltage exists until power light is off. Wait at least 5 minutes after input power is disconnected before performing maintenance

Please employ relevant Personal Protective Equipment (PPE) equipment:

- Insulation Gloves

6.2. Ground planes

Ground planes are located on the instrument chassis and the outer connector of the positive output n-connector, Ref Design Output 1 in Figure 1

6.3. Floating Voltages

The outer contacts of the n-connector for output nPEF (Ref Design 2) and input output transmission line (Ref Design 3) are floating when instrument is on. DO NOT TOUCH

DO NOT TOUCH this section

Figure-15, Danger floating voltage area indication

For safety please employ Safe System of Work (SSW). Implement the insulating protective surrounding for the high voltage floating area which is include with instrument.

The Safe System of Work:

Figure-16, Safe System of Work set-up