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A multi-variant investigation of CdTe/CdS photovoltaic material

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A multi-variant investigation of CdTe/CdS photovoltaic material

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R. L. Rowlands-Jones

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Acknowledgements

Abbreviations

AQE	-	Apparent Quantum Efficiency
CBD	-	Chemical Bath Deposition
CIGS	-	$CuInGaSe_2$
CIS	-	$CuInSe_2$
CL	-	Cathodoluminescence
CSS	-	Close-Spaced Sublimation
EBIC	-	Electron Beam Induced Current
FF	-	Fill Factor
ITO	-	Indium Tin Oxide
I-V	-	Current-Voltage
J_{sc}	-	Short-Circuit Current
LBIC	-	Laser Beam Induced Current
MOCVD	-	Metal Organic Chemical Vapour Deposition
η	-	Efficiency
OBIC	-	Optical Beam Induced Current
PV	-	Photovoltaic
QE	-	Quantum Efficiency
R_s	-	Series Resistance
R_{sh}	-	Shunt Resistance
SIMS	-	Secondary Ion Mass Spectrometry
TCO	-	Transparent Conducting Oxide
V_{oc}	-	Open-Circuit Voltage

Abstract

Six matrices of experiments were designed and carried out to investigate various deposition parameters of CdS/CdTe solar cells deposited by MOCVD. The results of the matrices were analysed using a criterion to establish which growth parameters are significant and warrant further investigation. The most significant parameters were CdTe growth temperature and *in situ* arsenic doping of the CdTe absorber layer. Characterisation of the device structures showed CdTe grain enlargement from 1μm to ~3μm at the higher deposition temperature of 390°C.

A series of CdS/CdTe devices with different TDMAAs partial pressures were grown by MOCVD to investigate the incorporation of arsenic in the bulk. Characterisation of the device structures using SIMS analysis showed arsenic concentrations ranging from 1×10^{16} to 1×10^{19} atoms cm^{-3}. A square law dependence of arsenic concentration on the TDMAAs vapour concentration was observed. A reaction mechanism for the decomposition of TDMAAs precursor via dimerisation is presented and discussed in terms of reaction kinetics. A model for the behaviour of arsenic in polycrystalline CdTe material, based on only partial passivation of grain boundaries and saturation of the grain boundaries at arsenic concentrations greater than 2.5×10^{18} atoms cm^{-3} is outlined and discussed.

A LBIC apparatus was designed and constructed in house and used to characterise CdS/CdTe device structures. The LBIC response from the devices was found to generate a small AC signal superimposed on a large DC current. Results are presented on the effect of arsenic concentration in the CdTe bulk on the induced current and uniformity. A plot of the arsenic concentration versus LBIC response and device efficiency clearly goes through a maximum in terms of induced current and device efficiency at 2×10^{18} atoms cm^{-3}. Each device scan shows microscopic variations in the induced current with new linear "furrow defects" features that are too large to correlate directly to the grain boundaries.

Attempts to engineer large grains in the CdS and CdTe layers by depositing the device structures onto Cd nuclei, Au nano-structured templates and patterned photo-resist were investigated. The Cd nuclei templates exhibit templating effects in CdTe but not uniformly across the substrate. Texturing the glass substrates increases the density of nuclei across the substrate area. The Au nano-structured templates also produce a templating effect and show evidence of a change in preferred orientation in CdTe from the (111) plane to the (311) plane.

1.0 Introduction

1.1   Background

This chapter provides an overview of the variety of solar cells being actively researched, the physics behind the devices and introduces some of the key areas addressed in this thesis. A summary of the various photovoltaic synthesis techniques are presented. Finally the main challenges tackled in this work are outlined.

1.2   Energy needs

The continuing economic growth of our societies and the growing need to reduce carbon dioxide emissions are major driving forces in the research for alternative energy sources. The world's current consumption of fossil fuels is depleting the available reserves at an alarming rate. The projections for future greenhouse gas emissions highlight an increasing problem if society continues to use fossil fuel at this rate. A large proportion of investment has been concentrated on the most promising renewable energy sources including: hydropower, wind, marine energy, bio-fuels, fuel cells and solar cells. The potential positive impact of alternative energy source research on total greenhouse gas emissions, as shown in figure 1.0 is a hot topic at present.

To date, renewable energy sources including biomass, wind and hydropower have had only limited success in the energy market. Photovoltaics are a promising replacement for fossil fuels as they are a renewable energy source that has the potential to cover the world's total energy demand. Every year the amount of solar radiation reaching the earth's surface is more than 10,000 times the world's annual energy consumption. Solar cells are capable of providing clean electricity to meet the demands of large industrial societies and the increasing needs of developing countries.

POPULATION TRENDS AND CO$_2$ EMISSIONS*
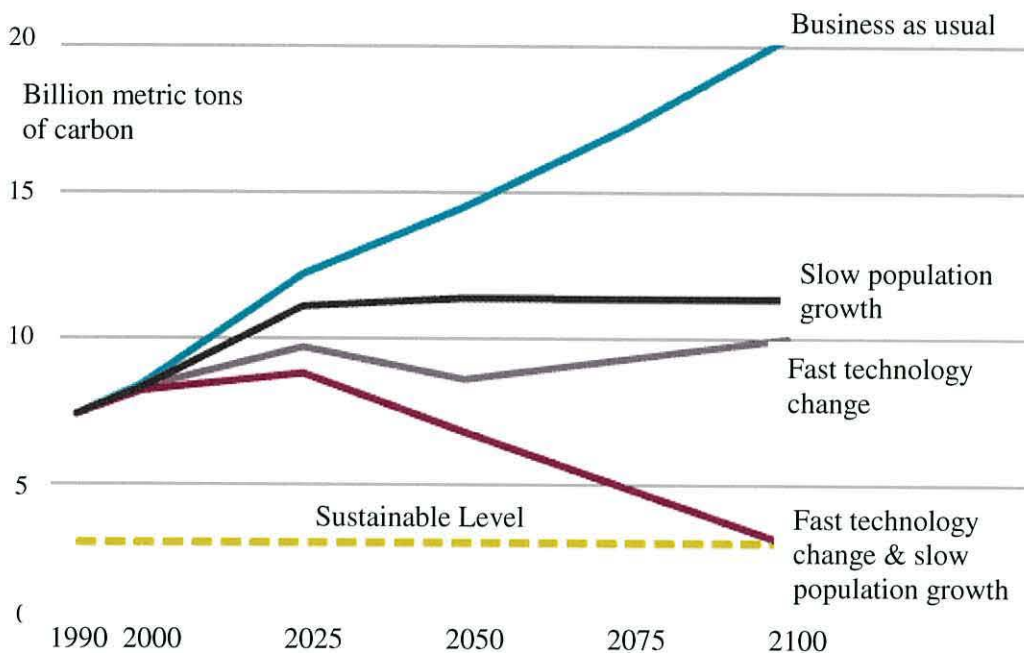
Fig.1.0 A plot illustrating the global CO_2 emission projections for a variety of scenarios,
(Image source at www.atlas.aaas.org).

* This figure expresses CO_2 emissions as elemental carbon. 1 ton elemental carbon = 3.664 tons CO_2.

A major advantage of solar energy is "point of use" power, the ability to use the electricity where it is produced. This has added benefits in terms of security of supply and less pressure to import electricity or fossil fuels from elsewhere. Interest in photovoltaics has rapidly increased over the last fifty years, with a substantial growth in world module production in the last decade.

1.3   Historical background

A material is termed photovoltaic if a voltage and/or current is generated by the absorption of light in a material or combination of materials. This phenomenon is known as the "photoelectric effect" and was observed by Becquerel in 1839, who identified a photovoltage when an electrode in an electrolyte solution was exposed to light [1]. Nearly 40 years later Adams and Day observed the same effect in Selenium [2]. Semiconductor photovoltaics gained popularity in 1954 when Chapin *et al.* developed a Silicon cell with a solar conversion efficiency of 6 % [3]. 1954 also saw the first thin-film

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solar cell comprised of a Cu_xS/CdS junction and achieved an efficiency of 6 % [4]. This efficiency was further increased to 9 % by 1980 [5].

1.4   Physics of photovoltaic devices

The basic concept of the photovoltaic process is that if a semiconductor material absorbs quanta of light of energy equal to or greater than the bandgap of the material, absorption occurs and electron-hole pairs are generated. A fundamental characteristic required for solar cells is the presence of an internal electric field capable of separating the carriers, allowing them to pass out of the material into an external circuit before they can recombine with one another. The most common structure is a pn junction, which combines two different semiconductor materials, one p-type and one n-type, to form an electric field (e.g. p-CdTe/n-CdS) [6, 7]. Figure 1.1 shows a schematic of a pn junction formed by p-CdTe/n-CdS.
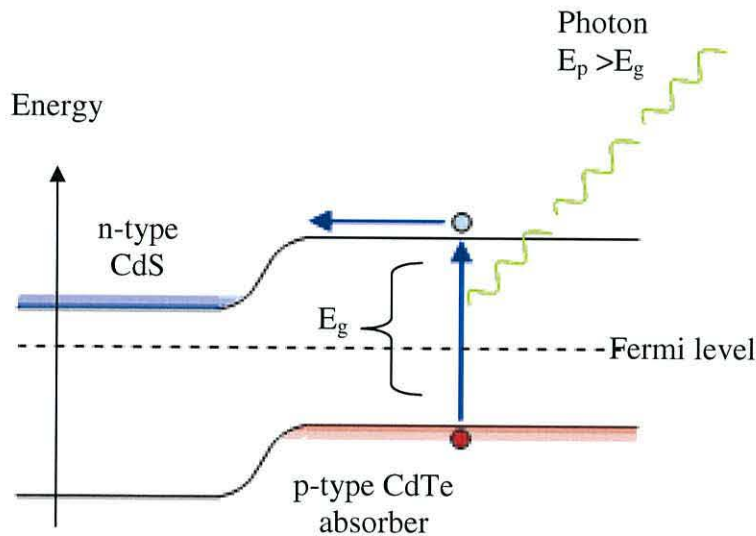
Fig.1.1 A schematic of a pn-junction, on absorption of a photon an electron is promoted to the conduction band.

Upon absorption of a photon, an electron is promoted to the conduction band. The electron is a minority carrier and therefore unstable. For the electrical power to be extracted the generated minority carriers have to diffuse to the junction where they are swept across by the internal field. The minority carriers become majority charge and can be conducted to an external circuit.

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1.5 Electrical characterisation of solar cells

Solar cells are routinely characterised electrically under illumination and under dark conditions. It is important to measure devices under comparable illumination and spectral conditions. It is therefore necessary to define the atmospheric absorption when quoting efficiency as the spectral distribution and total energy will be affected by the depth of atmosphere the solar radiation passes through. The air mass (AM) is the measurement used, and is defined as zero for solar radiation outside the atmosphere and 1 for radiation reaching the ground when the sun is at its zenith. AM1.5 is the conventional value used when quoting device efficiency and corresponds to a solar angle of 45°. The portion of the AM1.5 spectrum that can be captured by a CdTe solar cell is shown in figure 1.2.
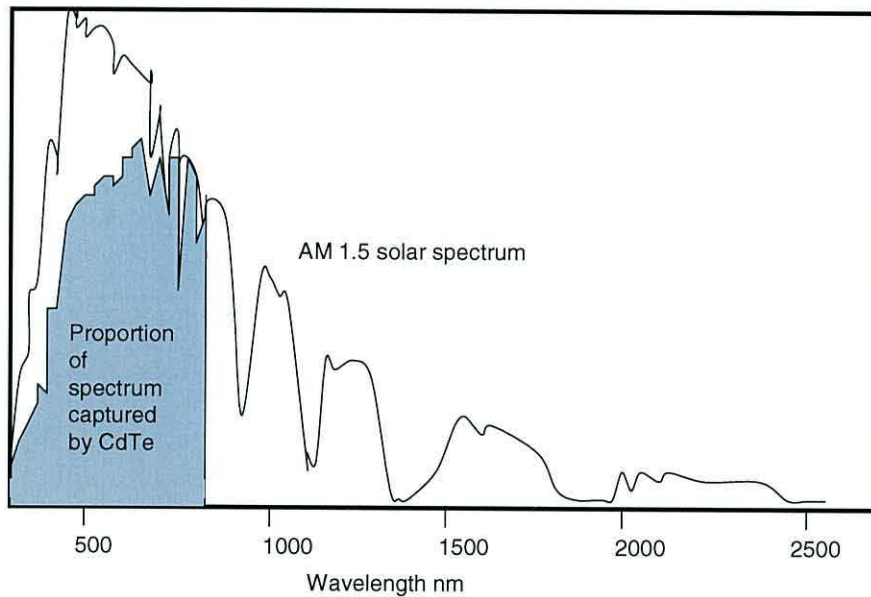
Fig.1.2 A graphical representation of a CdTe solar cell's maximum extractable energy with a bandgap energy of 1.45eV, under an AM1.5 spectrum.

The efficiency of a solar cell is strongly related to the generation of electron-hole pairs and the probability of their recombination before being delivered to the external circuit. In 1960 Schottky and Queisser were able to determine the theoretical maximum efficiency for a solar cell [8]. This limit is 40.7 % for a black body approximated solar spectrum at 6000 K, which arises from inherent losses including: loss of photons due to reflection, non-absorption of photons with insufficient energy ($E_p < E_g$) and carrier recombination before reaching the junction.

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Solar cells are routinely characterised using current-voltage (J-V) measurements to determine key device parameters such as: overall solar conversion efficiency (η), fill factor (FF), short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}). The electrical behaviour of solar cells has been the subject of many studies [9, 10]. To fully characterise the current-voltage behaviour of solar cells, the following device parameters must be correctly modelled: main junction, front and back contacts and series and shunt resistance. Figure 1.3 shows an example of a current-voltage curve of a photovoltaic cell under both light and dark conditions.
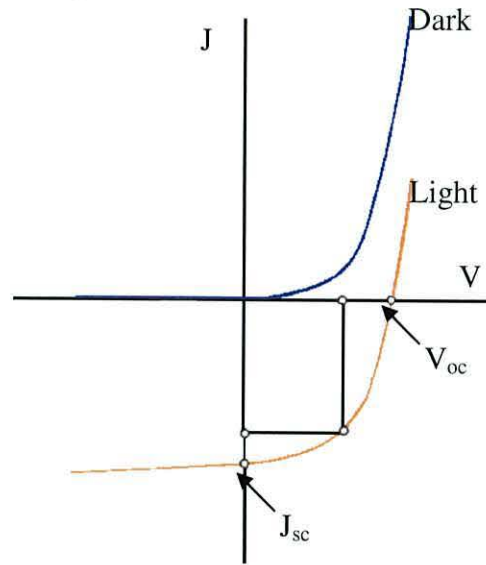
Fig.1.3 A schematic showing an example of the J-V characteristics for a PV cell under light and dark conditions.

(Image from Photovoltaic Materials by Richard H. Bube).

The shunt resistance (R_{sh}) is calculated by taking the reciprocal of the slope of the current-voltage in reverse bias (V < 0). The series resistance (R_s) is calculated from the reciprocal of the gradient of the J-V curve (slope) in forward bias (V > 0).

The flow of carriers into the external circuit constitutes the reverse electrical current density, J, and under short circuit conditions is known as the short-circuit current density, J_{sc}. The standard expression for current density in a solar cell is derived from the J-V curves. Equation (1.0) represents the electrical behaviour of all the device parameters except non-linear series resistance effects at the front and back contacts.

$$J = J_0 \left[\exp\left(\frac{q\phi}{AkT} \right) - 1 \right] - J_L \tag{1.0}$$

Some of the key terms are; the reverse saturation current density (J_o), diode quality factor (A), light generated current density (J_L) and voltage (ϕ). The main junction performance is characterised by two parameters: diode quality factor, A and reverse saturation current density, J_o.

Equation (1.1) shows the expression for J_{sc} and is identical to the standard solar cell expression in the dark.

$$J_{sc} = J_0 \left[\exp\left(\frac{q\phi}{AkT} \right) - 1 \right] \quad (1.1)$$

The expression for the open circuit voltage (ϕ_{oc}) given by equation (1.2) and shows that ϕ_{oc} is controlled by the current generation and recombination processes.

$$\phi_{oc} = \left(\frac{AkT}{q} \right) \ln\left[\left(\frac{J_L}{J_0} \right) + 1 \right] \quad (1.2)$$

The Fill Factor (FF) is the area of the rectangle in figure 1.3 between the dark and light J-V curves and is given by equation (1.3).

$$FF = \frac{J_m \phi_m}{J_{sc} \phi_{oc}} \quad (1.3)$$

J_m and ϕ_m represent the maximum current and voltage values respectively. Finally equation (1.4) shows several expressions for the overall device efficiency (η), the most commonly quoted parameter of PV devices.

$$\eta = \frac{P_m}{P_{rad}} = \frac{J_m \phi_m}{P_{rad}} = \frac{J_{sc} \phi_{oc} FF}{P_{rad}} \quad (1.4)$$

P_m and P_{rad} represent the maximum power and the total power incident on the cell respectively.

J-V measurements can also reveal information on the Schottky barrier. A Schottky barrier is formed when a metal and semiconductor are brought into contact. The difference in work function of the metal and semiconductor gives the contact potential, Φ_{sc}, as shown in equation (1.5). As the work function of the semiconductor depends on the position of the Fermi energy level, the contact potential varies with dopant concentration.

$$\Phi_{sc} = \Phi_M - \Phi_S \quad (1.5)$$

Copper is commonly used as the back contact as a high work function is needed for n-type II-VI semiconductors. Many research groups have investigated the effect of back contacts and Cu has been found to diffuse into the device and cause degradation [11-13]. Some novel alternatives to Cu have been discovered [14-16]. The fundamental physical origin of recombination currents or leakage currents at pn-junctions is an important property as many authors suggest the key to high performance devices is to reduce the leakage current at the metallurgical interface [9, 17, 18].

1.6 Variety of photovoltaic materials

A limited number of materials exhibit the photoelectric effect. Crystalline silicon (c-Si) in either single or multicrystalline wafers, accounts for > 85 % of the current PV market because the PV industry could easily utilise previous advances in silicon device knowledge from the microelectronics industry without the need to recreate scientific and technological infrastructures. Silicon has a bandgap of 1.1 eV that is a good fit for the photovoltaic absorber layer. The basic structure of a silicon cell is presented in figure 1.4.
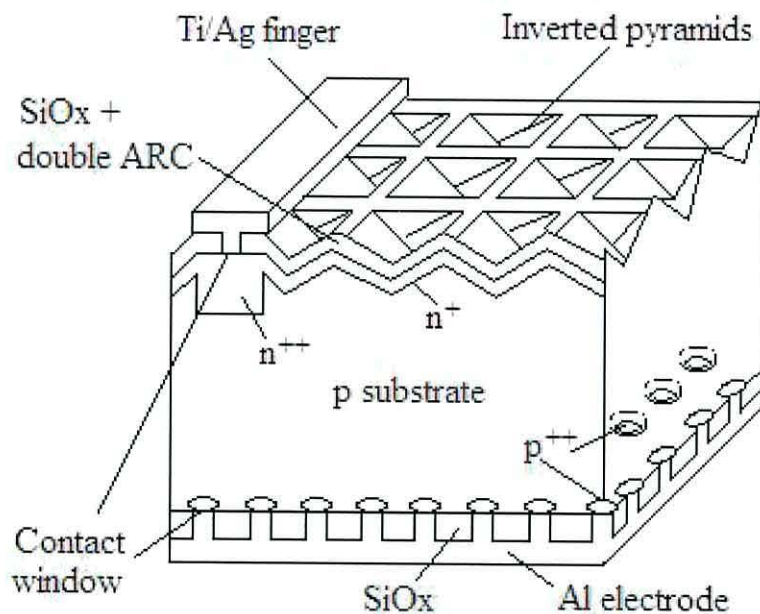
Fig.1.4 Schematic representation of a silicon solar cell.

There are several types of silicon used to produce solar cells: crystalline, amorphous and microcrystalline. Crystalline silicon cells have reached 24 % efficiency [19, 20]. The record efficiency for amorphous silicon (a-Si) has reached 13 % [21].

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Gallium Arsenide (GaAs) is a compound semiconductor solar cell material often used in space applications where high efficiencies and minimal weight are required but cost is not an issue. GaAs is favoured over silicon for these applications due to a significantly better resistance to radiation. GaAs also has a direct bandgap of 1.43 eV which is nearly ideal for solar conversion. In 1980 several III-V cells had been tested in space and a 16 % GaAs PV cell developed by 1989. Generally multi-junction devices as shown in figure 1.5 are used to obtain the high efficiencies needed for many space applications.
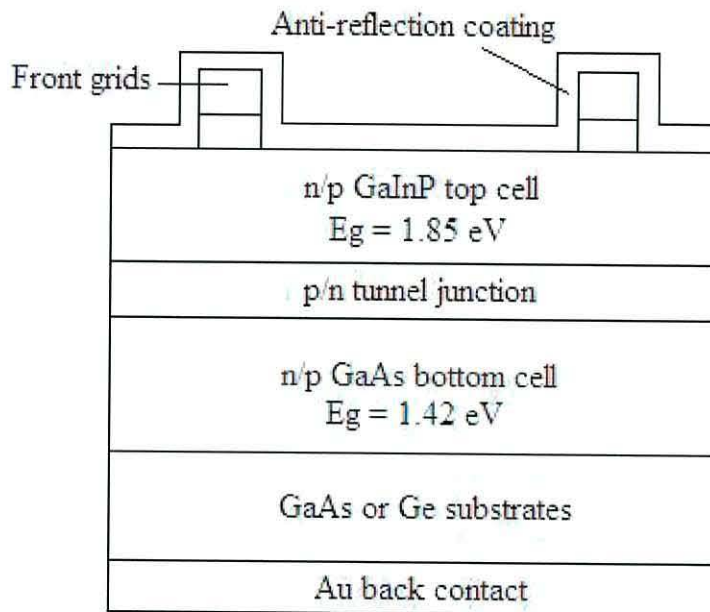
Fig. 1.5 Schematic of a GaInP multi-junction solar cell.

In 1999 Spectrolab and National Renewable Energy Laboratory (NREL) in the USA achieved a world record efficiency greater than 32 % from a triple junction GaInP$_2$/GaAs/Ge concentrator solar cell [22]. They took the basic cell design concept and made it cost effective for terrestrial applications by combining the solar cell with a concentrator system.

Other compound semiconductors including Cadmium Telluride (CdTe), CuInSe$_2$ (CIS) and CuInGaSe$_2$ (CIGS) are becoming increasingly common in the PV market. These materials are known as thin film PV devices as they require only a few microns of absorber material compared to the conventional silicon cells. A review of the status of thin film solar cells in terms of research and production was carried out in 2004 [23]. The

maximum theoretical efficiencies of these devices are CdTe 28.5 % and CIGS 27.5 %. The main manufacturers of these thin film modules are BP Solar, Antec and First Solar.

CIGS is a promising material for solar cells due to a high absorption coefficient, increased stability and direct bandgap. The basic structure of a CIGS cell is shown in figure 1.6.
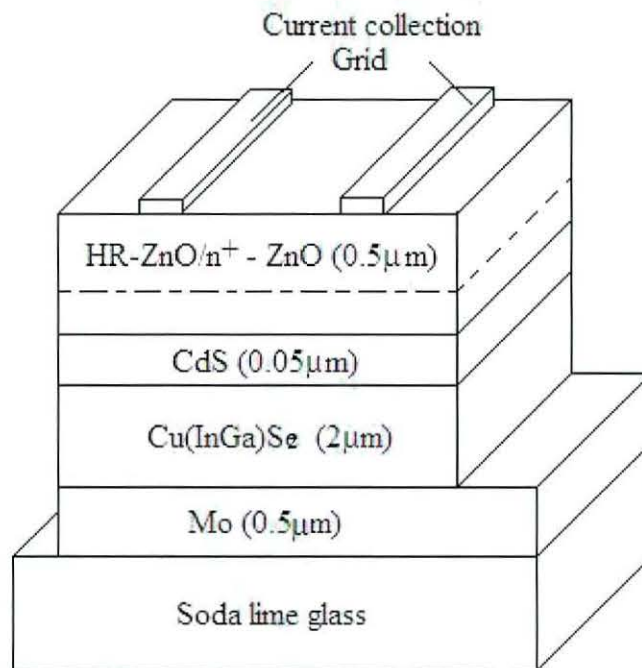
Fig.1.6 Schematic of a CuInGaSe$_2$ solar cell in the substrate configuration.

The bandgap in Cu(In,Ga)Se$_2$ devices is an important parameter for high efficiency devices as the bandgap can be graded by increasing the gallium content. At least ten groups world wide have fabricated high efficiency devices [24]. CIGS laboratory scale devices (1 cm^2) have achieved conversion efficiencies of 16.9 % in 2002 [25]. This efficiency was recently increased to 19.2 % [26].

CdTe is an excellent bandgap match for solar conversion efficiency with a bandgap of 1.5 eV and a high absorption coefficient > 5 × 10^5 cm^{-1}. The basic structure of a CdS/CdTe solar cell is shown in figure 1.7. The CdTe absorber based solar cell generally follows the superstrate configuration where the device is deposited on a glass substrate using a transparent conducting oxide (TCO) as the front contact, and most often, CdS as the n-type window layer. There is a lattice mis-match of ~ 10 % between the CdS and CdTe layers.
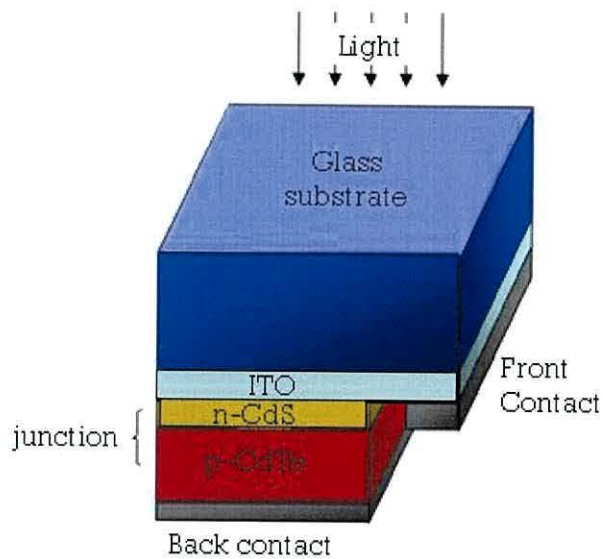
Fig.1.7 Schematic of a CdS/CdTe solar cell.

The recent CdTe work sponsored by the National Renewable Energy Laboratory (NREL) in the USA was reviewed by Ferekides *et al.* including discussions on back contact formation, buffer layers and thin CdS window layer [27].

Photoelectrochemical solar cells (PSC) consist of a photoelectrode, redox electrolyte and a counter electrode. Under irradiation, photo-corrosion of the electrode in the electrolyte solution readily occurs, leading to poor stability. Oxide semiconductor materials such as titanium oxide (TiO_2), zinc oxide (ZnO) and tin oxide (SnO_2) have good stability, but cannot absorb light in the visible region of the spectrum because of their relatively wide bandgap. Sensitisation of semiconductor oxides with photosensitisers like organic dyes can overcome this obstacle producing dye-sensitised solar cells. A simplified schematic of a dye-sensitised (PSC) solar cell is shown in figure 1.8.
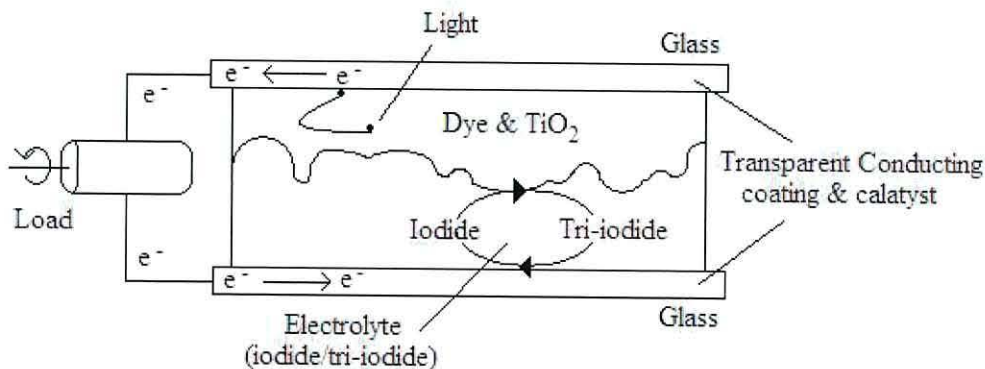
Fig.1.8 Schematic representation of a dye-sensitised solar cell (DSSC)

In the sensitisation process, organic dyes adsorbed onto the semiconductor surface absorb visible light and the excited electrons are injected into the conduction band of the semiconductor electrode. Tang and Yu carried out early work on organic solar cells. Efficiencies up to 4% have been achieved using PCBM polymer blends [28, 29].

1.7   Advantages of CdTe solar cells

Although silicon modules dominate the PV market, it is not the optimal material for photovoltaic conversion. The solar spectrum can be approximated by a black body that ranges from the ultraviolet to the near infrared. As stated earlier a semiconductor material can only convert photons with energy equivalent or greater than the bandgap energy with good efficiency. As a result the curve of efficiency versus bandgap goes through a maximum as shown in figure 1.9.
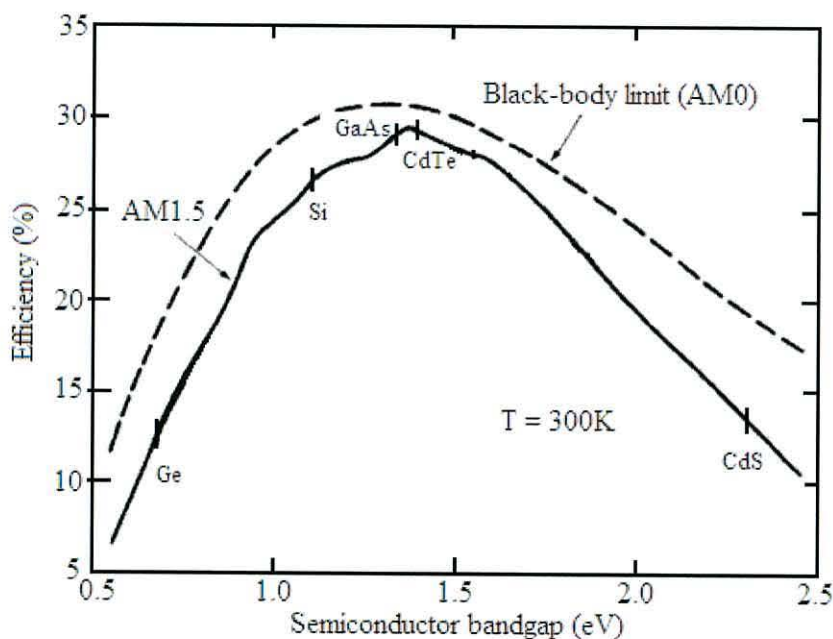
Fig.1.9 Schematic of conversion efficiency versus semiconductor bandgap energy.

Although the bandgap of Si produces a high maximum theoretical conversion efficiency of ~ 26 %, the bandgap of CdTe results in a higher maximum theoretical conversion efficiency of ~ 28 % under AM1.5 spectrum. Si is also an indirect bandgap semiconductor and light absorption is much weaker in an indirect bandgap semiconductor than in a direct bandgap semiconductor like CdTe. Figure 1.10 shows the difference in the materials band structure.
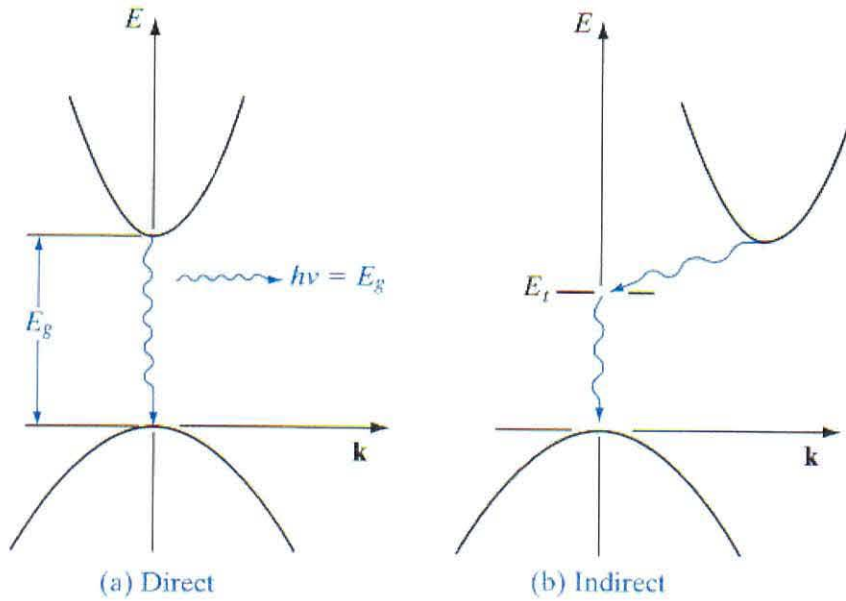
(a) Direct (b) Indirect

Fig.1.10 Schematic showing the difference between a direct and indirect bandgap semiconductor

For 90 % light absorption only 1 μm of CdTe (direct) is needed compared to 100 μm of silicon (indirect). Consequently the diffusion length of the minority carriers in silicon needs to be about 200 μm in order for the carriers to reach the junction. This requires material of high crystalline purity, which dramatically increases the cost of silicon solar cells. Cadmium telluride solar cells are the material of focus for the remainder of this thesis.

1.8   Polycrystalline Cadmium Telluride

In a perfect, pure semiconductor the recombination route for electron hole pairs depends only on the band structure, temperature and to a lesser extent the local injection density. Figure 1.11 shows the ideal one-dimensional device structure which accurately describes crystalline or epitaxial thin film devices.
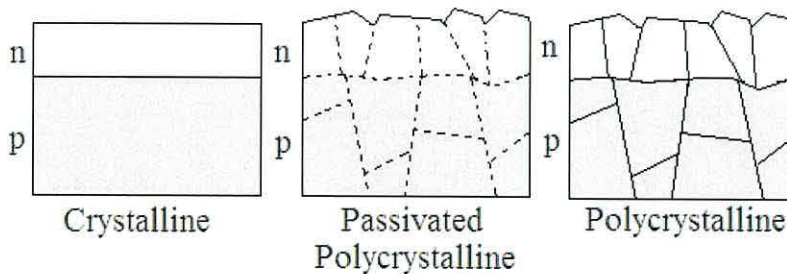
Fig.1.11 Schematic showing the difference between crystalline, polycrystalline and passivated polycrystalline material.

Polycrystalline material like CdTe contains grain boundaries and other defects that result in a more complex situation as impurities and defects strongly influence the local recombination behaviour of the charge carriers. At surfaces and defect centres, carrier lifetimes are greatly reduced as the defects provide a more probable, non-radiative recombination route than the pn junction.

Effectively passivating the CdTe grain boundaries will alter the properties of the grain boundaries which are known to determine the electrical and optical properties of the material and create a situation more comparable to crystalline material. This is an area of immense importance, but has been investigated by a limited number of research groups [30-32]. The polycrystalline nature of CdTe can also affect doping as there is considerable compensation of incorporated dopants from grain boundary states that results in the effective carrier concentration being orders of magnitude lower than the dopant concentration.

1.9   Growth methods

A wide variety of growth techniques are used to deposit CdTe solar cells including: close-spaced sublimation (CSS), chemical bath deposition (CBD), rf-sputtering and chemical vapour deposition (CVD). The efficiency of the solar cells alters depending on the deposition method used. CSS is the most common deposition method used as it produces the highest efficiency devices by exploiting the chemistry of CdTe. At temperatures above 600 $^{\circ}$C under vacuum CdTe sublimes, at temperatures above 400 $^{\circ}$C CdTe condenses stoichiometrically. Therefore CSS provides an easy route to stoichiometric films. The rate of deposition can be extremely fast but often leads to stacking faults.

Metal organic chemical vapour deposition (MOCVD) is a form of CVD that is versatile and adaptable and can operate at relatively low temperatures used to grow high quality thin films for use as solar cells. The basis of MOCVD is the reaction of volatile precursors in the presence of a substrate in a reactor. The metal organic precursors most commonly used for the CdTe absorber layer are Dimethylcadmium (DMCd) and Diisopropyltelluride (DIPTe). The choice of precursor is an important consideration in order to obtain the desired product and avoid undesirable side reactions.

The process of chemical vapour deposition involves several steps shown schematically in figure 1.12. The formation of CdTe from the metallic precursors is shown below.

$$Cd_{(g)} + \tfrac{1}{2} Te_{2(g)} \rightleftharpoons CdTe_{(s)}$$
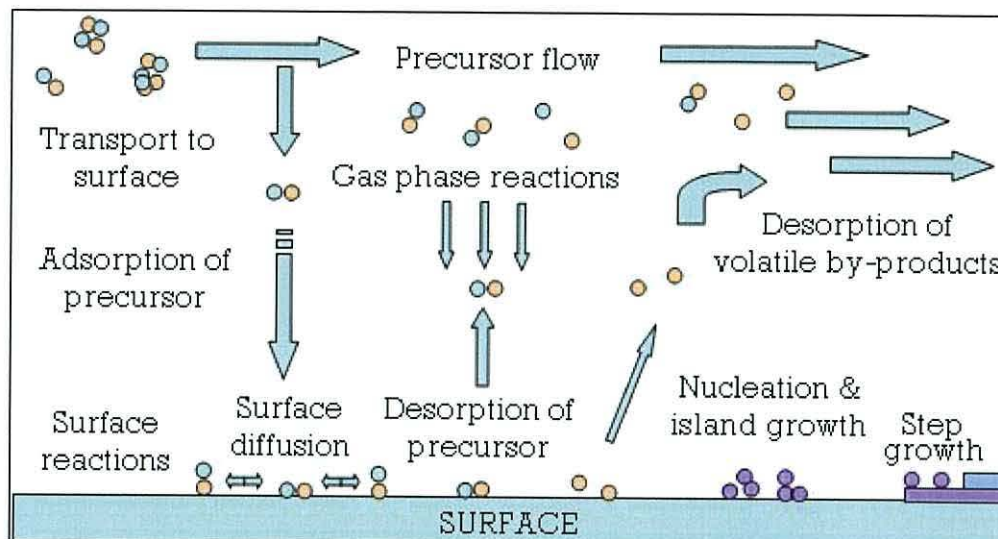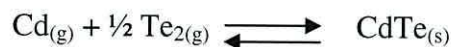
Fig.1.12 Schematic showing the many processes involved in MOCVD.

(Image from Chemical Physics of Thin Film Deposition Processes for Micro-and Nano-Technologies, Edited by Yves Pauleau).

Solid CdTe at atmospheric pressure exists as face-centred cubic zinc blende structure with unit cell dimension of 6.481 Å and CdTe bond length of 2.806 Å.

Despite the many steps involved in MOCVD this technique offers control over a variety of crucial growth parameters including: temperature, time, metal organic precursor and concentration. MOCVD also has the potential to deposit material over a large area onto a variety of substrates including steel, glass and polymers [33].

1.10   Challenges and Limitations

MOCVD offers independent control of a large number of materials parameters. The initial aim of this research is to systematically investigate materials parameters including; diffusion of impurities, layer thickness, growth rate, growth temperature, II/VI ratio for improved device parameters, with the main focus being investigation of significant deposition parameters and material characterisation. Secondly, explore pathways to engineer grain sizes greater than 2 μm at the junction to improve the material quality. Thirdly, construct in-house and modify a laser beam induced current

(LBIC) apparatus to characterise the growth material in terms of: defects, grain boundaries, and lateral collection. These challenges have been met and are discussed within this thesis.

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2.0 Literature Chapter

2.1 Introduction

The CdS/CdTe solar cell structure is the main focus for the remainder of the thesis. To improve the photovoltaic conversion efficiency of CdTe solar cells research is needed to investigate the complex nature of the polycrystalline material. This chapter reviews the key literature highlighting the large number of material parameters, common losses and recombination pathways, which contribute to the challenges of producing low cost high efficiency CdS/CdTe devices. The progress of thin film CdTe devices is discussed in terms of preferred growth technique, common treatments and device performance. Finally, the emerging field of grain engineering and the characterisation of the grain boundaries and grain structure are discussed.

2.2 High efficiency CdTe devices

CdTe is a promising material for photovoltaics as it has a bandgap that lies in the optimum range for solar energy conversion (1.45 eV). Loferski first proposed using CdTe for photovoltaic applications in 1956 [1]. Extensive work was carried out on heterojunctions with n-type CdTe and p-type Cu_2Te in the early 1960s [2-5]. The best CdTe/Cu_2Te cell reached efficiencies >7 % (60 mW/am^2 irradiance) [6]. Difficulty in controlling the formation process of Cu_2Te, poor device stability and the lack of a transparent p-type conductor all contributed to a shift to heterojunctions using p-type CdTe, which is now the norm. Bonnet and Rabinhorst produced a CdTe device with 5-6 % efficiency using CVD in 1972 [7]. Conversion efficiencies greater than 10 % were reported by several groups [8-10] and this was quickly followed by significant advances in the field.

Britt *et al.* reported a solar conversion efficiency of 14.6 % on a laboratory scale device in 1992 [11]. The CdS layer was chemically deposited at 70-90 °C from a solution of cadmium acetate, thiourea and ammonia acetate. The CdTe was grown via CSS at 600-700 °C reporting an average grain size of 3-5 μm. This efficiency was improved to 15.1 % in 1997 with CVD CdS and CSS CdTe and a CdCl$_2$ anneal [12]. The efficiency was further improved to 16.5 % in 2001 by Wu *et al* [13]. Interdiffusion between the CdTe and

CdS layers is known to have a significant affect on the device performance commonly attributed to intermixing causing a reduction of the bandgap in the junction region.

Figure 2.0 shows the progress in CdTe efficiency compared to the other solar cell materials over the last thirty years. Progress in thin film CdTe devices has slowed in the last decade with the overall device efficiency improving by just 1.3 %.
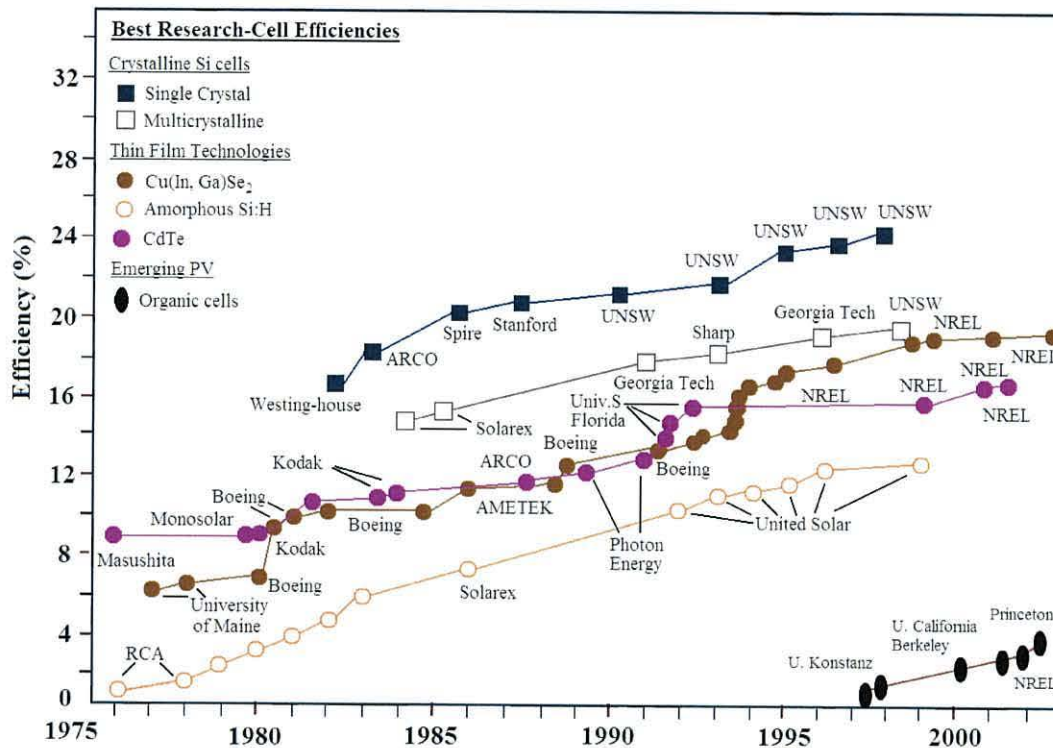
Fig. 2.0 A plot of the progress of the available photovoltaic material conversion efficiency with time, image from national renewable energy laboratory (NREL).

There remains plenty of potential for significant increase in the conversion efficiency and new approaches to experimental design, characterisation and novel materials could hold the key to the next surge in increased conversion efficiency. The high efficiency devices remain far from their theoretical optimum of near 30 % solar conversion efficiency, mainly because the materials chemistry of polycrystalline devices is not well understood. Many groups have made only incremental improvements to the device efficiency with little extension of the understanding of the material and improvements occurring from minimal adaptations of the now common $CdCl_2$ heat treatments.

All the devices mentioned previously are laboratory scale (1cm^2) and require scale up before implementation in the energy market. The manufacturing of 10MW$_p$ of CdTe modules per annum by ANTEC solar GmbH was reported by Bonnet in 2000 [14]. Both the CdS and CdTe layers are deposited by CSS in an in-line process. Advances in large scale modules of 1376 cm^2 have reached an efficiency of 10.5 % [15]. Wu also reported two manufacturing processes for producing high efficiency CdTe modules [16]. This progress indicates that CdTe solar cells have attained a comparable level to more sophisticated devices such as crystalline silicon and this is a key driving point for continued research in this area.

2.3 Cadmium chloride treatments and anneals

A cadmium chloride (CdCl$_2$) heat treatment is a common component in the fabrication of the recent high efficiency CdTe devices [17-21]. This step is employed as it is reported to enhance grain growth and improved cell performance although there is no commonly accepted mechanism for how these improvements are achieved [22]. The CdCl$_2$ treatment involves exposing the device to a chlorine source such as CdCl$_2$:CH$_3$OH, CdCl$_2$:H$_2$O, MnCl$_2$:C$_5$H$_5$N or CsCl:H$_2$O solutions and heating the sample to at least 400 ^{o}C under an inert atmosphere or in air for 10 to 30 minutes. Although there are benefits to the material and device performance, it also adds a high temperature step to the eventual industrial production of thin film PV, which will increase costs and production times. The benefits of grain growth and improved device performance are obtained in both inert and oxygen-containing atmospheres, which indicates that several characteristics may be changing during the Cl anneal. An approach that can identify and separate out the changes in the material could enable researchers to understand the mechanism of the CdCl$_2$ treatment.

It is suggested by Dobson *et al.* that during the treatment small CdTe grains may recrystallise and produce a more ordered structure with less lattice defects and larger grains [23]. The reduction in lattice defects would be beneficial to the conversion efficiency as there are fewer sites for recombination at native defects. Chu *et al.* stated that when CdS/n-CdTe structure is subjected to a CdCl$_2$ treatment, the n-CdTe is converted to p-type due to the incorporation of oxygen, when heated in air, which enhances the p-type conductivity of CdTe, but the exact mechanism for this is not known. In this work the CdTe absorber layer is doped *in situ* using arsenic and

consequently the CdCl$_2$ treatment may not be as beneficial in this material as the CdTe is already p-type.

Research into the properties and effects of the CdCl$_2$ treatment and possible alternatives has been a major focus of recent research [24-28]. There are many variations of the CdCl$_2$ anneal in terms of temperature, time, atmosphere and Cl precursor. Some of the proposed components of improved devices from CdCl$_2$ anneals are: Cl diffusion into the CdTe, conversion of n-type CdTe to p-type CdTe by oxygen incorporation, grain boundary passivation and an increase in grain size. This array of components indicates that a variety of changes are occurring in the material simultaneously. Despite advances the cell parameters quoted in the literature exhibit significant variation from group to group and there is poor understanding of the mechanisms which limit the conversion efficiency of CdS/CdTe solar cells. Although this treatment is now commonly used to produce high efficiency devices it might not be a necessity. CdTe material can be converted to p-type by doping the material and grain growth may be possible by other routes such as patterned substrates, templating or grain engineering.

Other groups have investigated the effects of CdCl$_2$ treatments via Electron Beam Induced Current (EBIC) measurements and have shown that grain boundary passivation occurs [29, 30]. This hypothesis is more feasible for CdTe material that is doped prior to the CdCl$_2$ treatment as the material is already converted to p-type by the dopant. Therefore the role of oxygen incorporation may not be as critical in previously doped material. Impurities in the material whether intentional dopants or components of the CdCl$_2$ treatment will segregate to the grain boundaries facilitating grain boundary passivation. Passivation of the grain boundaries can lead to increased carrier lifetime and reduce recombination of the electron-hole pairs at grain boundaries, making it more probable for the carriers to reach the junction, improving the electrical characteristics of the device.

Further work is needed to understand the effect the CdCl$_2$ heat treatment has on the grain structure and the electrical and optical properties. To fully understand the mechanisms involved the various components of the CdCl$_2$ treatment need to be investigated in isolation. MOCVD offers independent control of the various growth parameters and could be used in a systematic investigation. This could lead to the CdCl$_2$

treatment becoming redundant and open cost reducing pathways by removal of a high temperature step and the need of fewer chemicals.

2.4   MOCVD

The MOCVD growth technique is very versatile and is commonly used for semiconductor fabrication [31] and a wide range of materials within optoelectronics including: GaAs [32-34], ZnSe [35], InGaP [36], CI(G)S [37], metal oxides [38, 39] and CdTe [40-43]. The first GaN-based high brightness LEDs consisted of a thin film of GaN deposited via MOCVD on sapphire. One key advantage of this technique is the possibility of growing thin films on a variety of substrates; glass, polymers and steel creating flexibility for future PV products [44, 45]. As mentioned previously the process of MOCVD involves many complex steps and a numerical study of the growth conditions was reported by Tena-Zaera et al [42]. MOCVD can be used to grow large areas of material at one time if a high level of uniformity can be achieved and the relatively low deposition temperature also offers a possible cost reducing pathway.

Kruger and de Nobel have shown that the type of conductivity in CdTe can be altered by varying the Cd:Te stoichiometry [46]. Cadmium-rich films produce n-type material and Te-rich films result in p-type material. Bonnet and Rabinhorst produced the first CdS/CdTe heterojunction solar cell using CVD in 1972, with an efficiency of 5-6 % [7]. Chou et $al.$ produced an 11.9 % efficiency device with the absorber layer deposited via MOCVD [47]. The device fabrication involved a $CdCl_2$ treatment in $CdCl_2$:CH_3OH solution followed by an anneal in air at 400 $^{\circ}$C for 30 minutes [47]. In $situ$ monitoring of growth characteristics has been implemented using laser interferometry allowing researchers to monitor the growth rate, layer thickness and surface roughening in real time [48]. Increased understanding of these characteristics could lead to improved stability. MOCVD also has the ability to accurately dope material in $situ$. This is important, as the dopant concentration can affect the band structure and surface contact potential. The first CdS/CdTe photovoltaic device to incorporate doping of material on both sides of the pn junction was achieved in 1998 [49].

There are few groups using MOCVD to deposit CdS/CdTe solar cells and numbers have dwindled across Europe and the USA in favour of the CSS technique. As mentioned

previously, CSS produces the highest efficiency devices to date and has a much faster deposition rate of 1-5 μm/min compared to 0.01-0.1 μm/min for MOCVD. Despite these advantages the increase in conversion efficiency of CSS devices has now slowed with only 1.3 % improvement in nearly ten years. The rapid deposition rate often leads to stacking faults in the CdTe layer providing an alternative recombination centre. If conversion efficiencies remain stagnant then progress in reducing the cost per watt will be needed to allow solar cells to integrate the energy market.

MOCVD offers more potential for lower cost CdTe solar cells than CSS as it is a lower temperature and pressure deposition technique. Despite the slow growth rate MOCVD can be utilised for sequential deposition of both the CdS window layer and CdTe absorber layer over large areas. Laser interferometry can be utilised to monitor the growth rate of CdS and CdTe in situ, assisting in obtaining high repeatability and reproducibility required for industrial scale production. CVD is used in the glass coating industry and presents an opportunity for lower cost large scale deposition of CdTe solar cells via an all MOCVD route if the challenges of doping polycrystalline material and uniformity can be overcome.

2.5   Doping

Doping is an important tool in the development of CdS/CdTe solar cells. As a semiconductor absorbs quanta of light equal to or greater than the bandgap of the material to exhibit the photoelectric effect, the band structure is an important parameter. It was found that high dopant concentrations can affect the shape of the band edges. Consequently doping of cadmium telluride material is a subject of interest with research groups investigating various dopant species including Titanium, Vanadium, Bismuth and Indium [50-53].

Figure 2.1 (a) illustrates that the distribution of the valence and conduction band states can become "smeared" producing band tails, which effectively reduce the bandgap width.
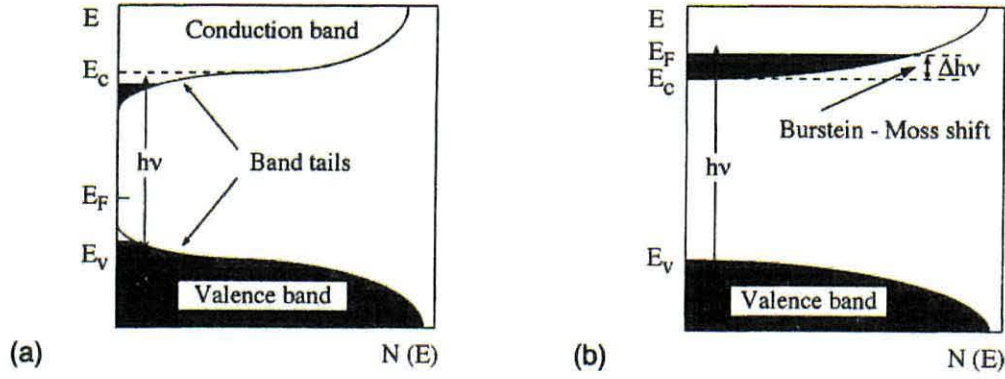
Fig. 2.1 Schematics illustrating changes to the band structure (a) band tails and (b) Burstein-Moss shift.

Lanyon and Tuff calculated the bandgap narrowing ΔE_g as a function of the dopant concentration, N, shown in equation 2.0 [54];

$$\Delta E_g = \frac{3e^2}{16\pi\varepsilon}\left(\frac{e^2 N}{\varepsilon KT}\right)^{1/2} = \frac{3e^2}{16\pi\varepsilon L_D} \tag{2.0}$$

Where ε is the permittivity of the semiconductor and L_D is the Debye length. This bandgap narrowing is an important factor as it needs to be taken into account when determining the performance of the pn junction.

For very high donor concentrations optical transitions in states above the Fermi level are almost impossible as they are occupied. The Fermi level is now in the conduction band resulting in the optical absorption edge shifting as shown in figure 2.1(b). This shift is known as the Burstein-Moss shift and results in the optical band gap appearing larger in degenerate semiconductors.

Arsenic is often selected as the dopant of choice to form p-type CdTe because atomic arsenic has one less electron in the outer shell and a smaller atomic radius than tellurium making incorporation of arsenic into the crystal lattice probable. Ghandhi *et al.* doped epitaxial films grown onto single-crystal CdTe substrates using arsine (AsH$_3$) [55]. There is a large knowledge-base on the pyrolysis of alternative arsenic compounds from research on III-Vs including tertiarybutylarsine (TBAs) [56] and trimethylarsine (TMAs) [57]. Trisdimethylaminoarsine (TDMAAs) was reported to produce improved arsenic doping in MOCVD grown HgCdTe photodiodes with arsenic concentrations of 1×10^{17} cm^{-3} with little change to the alloy composition [58]. Arias *et al.* reported p-type arsenic

doping concentrations in the $10^{14} - 10^{16}$ cm^{-3} range in both CdTe and HgTe/CdTe superlattices using molecular beam epitaxy (MBE) [59].

Doping p-CdTe is a dominant problem in the production of CdS/CdTe solar cells. In polycrystalline material there is considerable compensation of dopants by the grain boundaries resulting in the effective carrier concentrations being orders of magnitude lower than the dopant concentration. The main problem in doping polycrystalline material is that all metallic dopants can easily segregate to the grain boundaries giving rise to metallic, highly electrical conducting phases that can cause shunts in the CdTe layer.

2.6   Common losses and defects

Surprisingly, CdS/CdTe solar cells with conversion efficiencies between 10-16 % have similar photovoltaic behaviour. For CdTe devices to continue to increase in efficiency the loss mechanisms of the material need to be identified and understood. The fundamental issues that influence the development of CdS/CdTe devices include:

1. The role of Cu in p-type doping of CdTe,
2. The controlling role of doping efficiency in CdTe,
3. The effects of abrupt and graded CdS/CdTe junctions,
4. The effects of active and passive grain boundaries,
5. The formation of low-resistance contacts to p-type CdTe.

Some of the more common losses and defects that affect CdTe devices have been reported including the lattice mismatch between the CdS and CdTe layers [23, 60-62]. Losses in photocurrent are attributed to: reflection, window absorption and diffusion length. The open circuit voltage losses are caused by: built-in potential and forward recombination current and fill factor losses are attributed to series resistance and leakage.

To obtain a high current density the CdS window layer needs to be very thin to allow a large portion of photons with energy greater than the bandgap to reach the CdTe absorber layer and hence produce photocurrent. The thickness of the CdS has both beneficial and detrimental affects on the device performance. If the window layer is too thin it can lead to local shunting and pin-holing to the TCO or excessive forward

current. Some of the now common processing treatments such as annealing and chemical treatment can promote interdiffusion between CdS and CdTe resulting in a bandgap shift of CdS, which reduces the transmission and increases the absorption of short wavelengths known as the blue defect. Although some intermixing of CdS and CdTe is beneficial, leading to a reduction in interfacial strain, it can also result in a thinning of the CdS layer.

To reduce the affects of CdS thinning and local shunting a second highly resistive layer such as ZnO is deposited between the TCO and CdS, but this adds an additional layer to the already complex polycrystalline device structure. The addition of a buffer layer can also reduce the diffusion of contaminants from the substrate into the device. The SIMS technique is utilised to investigate trace contaminants, diffusion of impurities and measure dopant concentrations in the device structure and remains an area of interest for many research groups [63-65]. Anneal processes have proven beneficial to the CdTe layer by producing larger grains and producing a more ordered structure. This highlights the importance of understanding that a process treatment can have conflicting effects on the different layers of a CdS/CdTe solar cell.

In all the fabrication methods used for CdTe solar cells there are two dominant problems:

1. Recombination losses associated with the junction interface and grain boundaries.
2. Difficulty in forming low resistance ohmic contacts to p-type CdTe.

When the thermal equilibrium of a semiconductor is disturbed by the generation of electron-hole pairs, recombination mechanisms exist to restore the system to equilibrium. Enhanced recombination at extended defects is caused by additional electronic states in the bandgap. These additional states are produced by the disorder of the crystal lattice and the occurrence of 'dangling' or broken bonds. The corresponding electric field and potential leads to band bending, which shifts the defect states until the occupation limit the Fermi energy of the crystal.

The formation of a stable low resistance ohmic contact to CdTe remains an obstacle in the progress of CdS/CdTe solar cell due to the high work function of CdTe [66, 67]. Early contacting methods then applied copper to form a p^+ contacting layer which is then

contacted with a metal or graphite. The high bulk-diffusion coefficient of Cu in CdTe caused Cu to readily diffuse through the CdTe resulting in degradation of device and poor stability. A Te-rich layer is now commonly formed to aid metal contacting by chemically etching the CdTe surface using a solution of bromine in methanol (Br etch) or a mixture of nitric and phosphoric acid (NP etch). Au is often selected as the contact metal as it is easy to work with and has a high work function however this is not a suitable candidate for solar cells in the long term as Au also diffuses into the material and has added cost issues. A variety of novel back contacts have been investigated including ZnTe and Ni [47, 68, 69].

2.7   Grain boundaries & grain engineering

Grain boundaries are the main crystal defects in polycrystalline thin films and an example of extended lattice defects that change the lifetime and mobility of the charge carriers in the local area. The basis for an understanding of grain boundary behaviour is the description of the atomic structure and chemistry. The structural and chemical disorder determines the electrical states in the forbidden gap, between the valence and conduction bands, primarily responsible for the electrical activity of the grain boundaries. Figure 2.2 shows a schematic of a more realistic representation of a CdS/CdTe polycrystalline solar cell.

GRAIN BOUNDARY
- Potential barrier
- Recombination
- Enhanced atomic diffusion

GRAIN INTERIOR
- Bulk recombination

CdTe

CdS

ITO

Glass

VOID
- Gas transport

GRAIN SURFACE
- Surface recombination
- Depletion layer
- Enhanced surface diffusion

JUNCTION INTERFACE
- Interface recombination
- S and Te interdiffusion
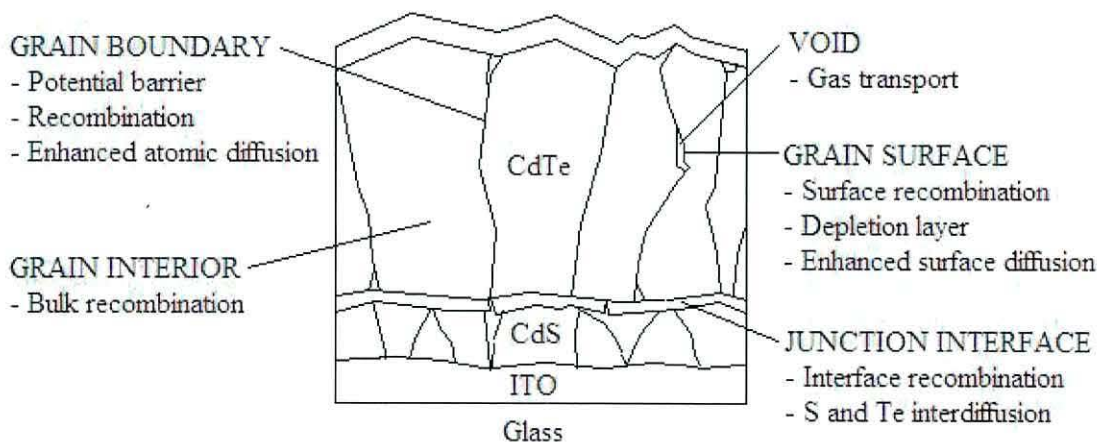
Fig 2.2 Schematic of a more realistic CdS/CdTe structure. A representation from "critical issues and research needs for CdTe-based solar cells" by Compaan *et al.*

Successful device fabrication requires thorough understanding and control of;
- the effects of grain boundaries,
- internal voids,

- pinholes through thin CdS,
- interdiffusion across the CdS/CdTe interface,
- low resistance ohmic contacts,

without significant degradation to the junction properties. Prof. Tadao Watanabe pioneered the objective of grain boundary engineering, to control the population of grain boundary types, in the mid-1980's [70]. Research in the area of grain boundary engineering has reached a period of expansion [71-75]. Grain boundary engineering is focussed on manipulating microstructures to obtain improved material properties. It has been suggested by Frary *et al.* that although the grain boundaries affect the materials properties, the connectivity of these boundaries or grain boundary networks, may also be crucial component in the field of grain boundary engineering [71]. Within this field grain boundaries are classified as special vs. general. Early work in this field used a variety of processing approaches largely based on trial and error. The approaches to grain boundary engineering have increased in sophistication in terms of how grain growth, creep and impurity diffusion are controlled by grain engineered microstructures [74-76].

The grain boundary potential is a complex function of the doping concentration, temperature and grain size. As a function of doping concentration N_d the grain boundary potential has a maximum at

$$N_d \approx \frac{N_B}{L} \tag{2.1}$$

where N_B is the number of grain boundary states per unit area and L is the grain size. This reiterates the fact that doping CdTe material is a key element in the development of polycrystalline material which is affected by the grain structure. Doping therefore requires independent investigation from the $CdCl_2$ heat treatment as this process is known to alter the grain size and could mask some of the affects of doping polycrystalline material, whether beneficial or detrimental to device efficiency.

The ability to manipulate grain boundaries and grain boundary networks has a huge potential importance in solar cells as the electrical properties of the material are largely dictated by the grain structure. Alterations to the material's grain structure via grain growth mechanisms yield beneficial affects on device parameters. The field of grain

engineering has the capacity to manipulate the grain structure by reducing diffusion of impurities through the material and recombination at defect centres.

2.8   Characterisation of grain structure

The characterisation of grain boundaries and grain structure is an essential part of research into CdTe solar cells as the behaviour of the grain boundaries is not well understood. The grain size of CdTe layers can be calculated from x-ray diffraction patterns. The size is determined from the half-width of the $2\theta = 23.7$ ° diffraction maxima using Scherrer's formula [77],

$$d = \frac{k\lambda}{D\cos\theta}$$
(2.2)

where; d is the grain size, λ is the x-ray radiation wavelength, k is the shape factor and D is the diffraction maximum half-width.

Mobility measurements on polycrystalline material yield information on the influence of grain boundaries and are frequently determined by Hall and conductance measurements [69, 78, 79]. The main result for small grain sizes is that the crystal is almost completely depleted from carriers that are trapped in the grain boundary states. For high dopant levels and larger grain sizes, the mobility increases with dopant concentrations and approaches single-crystal values.

The EBIC technique is a method for studying charge carrier recombination at extended defects in semiconductors and offers direct determination of the recombination velocity of a grain boundary. Electron-hole pairs are generated by an electron beam in an SEM and separated by the pn junction. The resulting EBIC current is amplified and used to modulate the signal of the SEM monitor. The collected current is reduced at defects because of locally enhanced carrier recombination. Therefore defects appear as a dark feature on the SEM image. This is a powerful technique as it facilitates direct and immediate observation of the recombination behaviour of the grain boundaries [80-83]. EBIC measurements and other beam injection techniques (OBIC and LBIC) have been used to analyse CdTe device structures [83-85].

The characterisation of grain boundary engineered materials has evolved rapidly since the emergence of the field. Initial characterisation involved transmission electron

microscopy (TEM) analysis. The characterisation of grain boundary character has benefited from SEM-based electron backscatter diffraction (EBSD) techniques allowing grain boundary distribution to be routinely reported [70].

These characterisation methods are powerful tools in understanding CdTe solar cells, but are most beneficial for material with grain sizes greater than 1-2 microns. EBIC and OBIC techniques provide information on the recombination behaviour of the material, but the devices are not characterised under real conditions. The intensities used during characterisation are far lower than solar intensities and therefore these methods do not give a clear indication of how devices will perform when integrated into the energy market.

2.9   Micro LBIC

Although the LBIC technique has been employed for many years, the micro LBIC technique which boasts micron resolution spot size was pioneered at Colorado state university by Hiltner *et al.* [86]. The characterisation technique is based on the EBIC and OBIC techniques but uses a laser source that can match solar intensities. A schematic of the optical setup of the apparatus is presented in figure 2.3. A laser beam is focussed through a microscope objective onto a device generating an induced current which is mapped across the device.
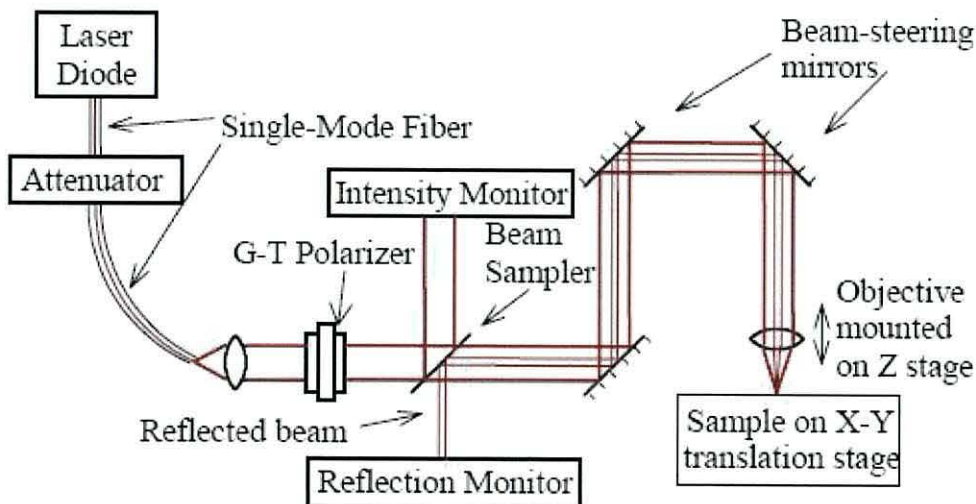
Fig 2.3 A schematic of the optical setup used by Hiltner *et al* [87].

The LBIC technique can provide information on local recombination, shunts, pinholes, uniformity and apparent quantum efficiency (AQE). At its lowest resolution (100 μm spot size) the area of a research-sized device can be mapped. At the highest resolution (1 μm spot size) the response of a single grain can be examined. The laser spot size is an important parameter as the resistance increases as the spot size decreases, which can introduce complications in separating high injection effects and resistive effect as both are dependent on carrier generation area.

This technique is now widely used in the characterisation of materials [88-92]. The ability to place a sample in the setup with micron precision allows monitoring of the affect of annealing and degradation over time. Much of the early work concentrated on the effects of stress and uniformity on devices after various periods of light soaking [93, 94]. A disadvantage of this characterisation method lies in the interpretation of the raw data as variations in the induced current can occur for many reasons in polycrystalline material including:

- local quality of the junction,
- local shunting effects,
- spatial variation in resistivity,
- density of local defects,
- uniformity.

One of the major limitations in the understanding of grain boundaries in polycrystalline material is the material itself. The laser beam induced current technique is commonly used to great effect on silicon solar cells due to their significantly larger grain size (10 μm) compared to CdTe (1-2 μm) [95]. Manipulating the microstructure of CdTe to obtain larger grain sizes greater than 5 μm would be hugely beneficial in increasing the resolution of the LBIC technique and the knowledge and understanding of the grain structure behaviour during anneal steps, chemical etching and $CdCl_2$ treatments.

2.10 Statistical methods

Many industrial processes are not fully optimised or suffer from seemingly random variation. Statistical methods have been crucial to the success of the semiconductor industry and are now widely used to reduce losses and waste [96, 97]. Meng *et al.* studied a reactive ion etching process using fractional factorial experiments and a statistical

response surface method [98]. He and Wang used a variety of statistical methods to investigated fault detection of batch processes including [99]: statistical process monitoring (SPM), principal component analysis (PCA) and k-nearest-neighbour (kNN) rule. These methods are effective, but require an immense amount of data beforehand, to accurately model the system under investigation. This approach is only suitable for established technologies and materials where there is a large knowledge and database and would not be beneficial for technologies still in their infancy such as dye-sensitised solar cells.

The 'Taguchi Matrix Method' is a statistical approach adopted by the US semiconductor industry in the 1980's and was pioneered by Dr. Genichi Taguchi [100-102]. The Taguchi method has been described as a scientifically disciplined mechanism for evaluating and implementing improvements. The methodology is based on 'orthogonal arrays' of investigation that can rapidly 'tune' a given process using an eight step procedure for optimal results. In recent years the Taguchi method has been employed in many areas of science and engineering. Plasma surface hardening was explored by Yang in 2001 [103]. Chen *et al.* applied the Taguchi method to optimise the etching recipe for deep silicon trenches in 2005 [104]. The Taguchi method was employed by Del Cano *et al.* to evaluate the emission of an electroluminescent device [105]. Pin holes have been investigated in Aluminium films by Takatsuji and Arai [106], and more recently in indium tin oxide by Lee and Park [107].

The analysis of the Taguchi results in these papers is thorough, but there is no explanation of what level of noise exists in the systems and how this is taken into account within the data analysis. There appears to be no common convention between the papers for how to approach this issue even though the methodology clearly highlights the importance for a low noise system. The nature of polycrystalline CdS/CdTe material and the MOCVD growth technique utilised in this work produce an immense number of growth parameters. The Taguchi method was adopted over the other available statistical methods as the system does not need to be modelled beforehand and a relatively small number of growth experiments are required. Further details of the methodology and its implementation are discussed in Chapter 4.

2.11 Summary

Research into CdTe solar cells has progressed with significant advances during the early 90's. High efficiency devices of 16.5 % have been achieved with the addition of a $CdCl_2$ heat treatment, which has since become a common part of CdTe solar cell fabrication. The important controlling factors for improved devices are recognised as: stoichiometry, growth morphology, quality of the grain boundaries, doping and contacting. Despite relatively high efficiency devices of 16.5 % there is still considerable improvement needed to obtain device efficiencies comparable to the theoretical conversion efficiency of 28 % for CdTe solar cells. The $CdCl_2$ treatment commonly employed to achieve efficiencies greater than 10 % is not fully understood in terms of the morphology and electrical and optical properties of the material. This treatment adds a process step to the CdTe structures that may become redundant if the grain enlargement and grain boundary passivation can be achieved by other processing routes such as grain engineering and arsenic doping.

For CdTe devices to increase in efficiency and reduce costs to impact on the energy market, an increased understanding of the theoretical limits, process steps and common losses is needed. Statistical methods could be utilised to rapidly survey the large number of growth parameters associated with polycrystalline CdTe solar cells in a minimal number of experiments. The characterisation of these materials is a crucial step in understanding how materials processes affect the growth material and aid conversion efficiency. Translating high efficiency cells to high efficiency modules will require additional understanding of processing tolerances and the effects of thermal and chemical non-uniformities in processing large-area devices.

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3.0 Processing and characterisation techniques

3.1 Introduction

This chapter gives details of the growth conditions of the experimental matrix growth layers and details how the growth material is processed into devices. The setup and procedure for J-V characterisation of the devices is discussed. Finally the characterisation techniques employed in this work are detailed.

3.2 Substrate preparation

The preparation of the substrate is a crucial step as the surface morphology and particulates on the substrate can greatly affect the growth coverage. The preparation of the glass substrates involves a series of washes and rinses as shown below:

- Swab with methanol and dry with nitrogen gun.
- 10 minute ultrasonic bath with deionised water.
- Rinse with methanol and dry with nitrogen gun.
- 10 minute heated ultrasonic bath with 2 % Decon90 in deionised water.

Between the above steps the substrates are placed in a heater cabinet at 50 °C to dry. Once the cleaning process is complete the substrates are stored in the heater cabinet. When carrying out a growth run the substrates are swabbed with methanol and dried with a nitrogen gun immediately before the growth run.

3.3 MOCVD growth conditions

MOCVD is a variation of Chemical Vapour Deposition (CVD). Growth is carried out in a cold-walled reactor and material is only deposited at the heated areas. The process uses mass flow controllers (MFC's) to regulate and control the flow of the organic precursors into the reactor. Photovoltaic thin films of the general formula glass/ITO/n-CdS/p-CdTe/Au were grown. The MOCVD reactor setup is shown schematically in figure 3.0.
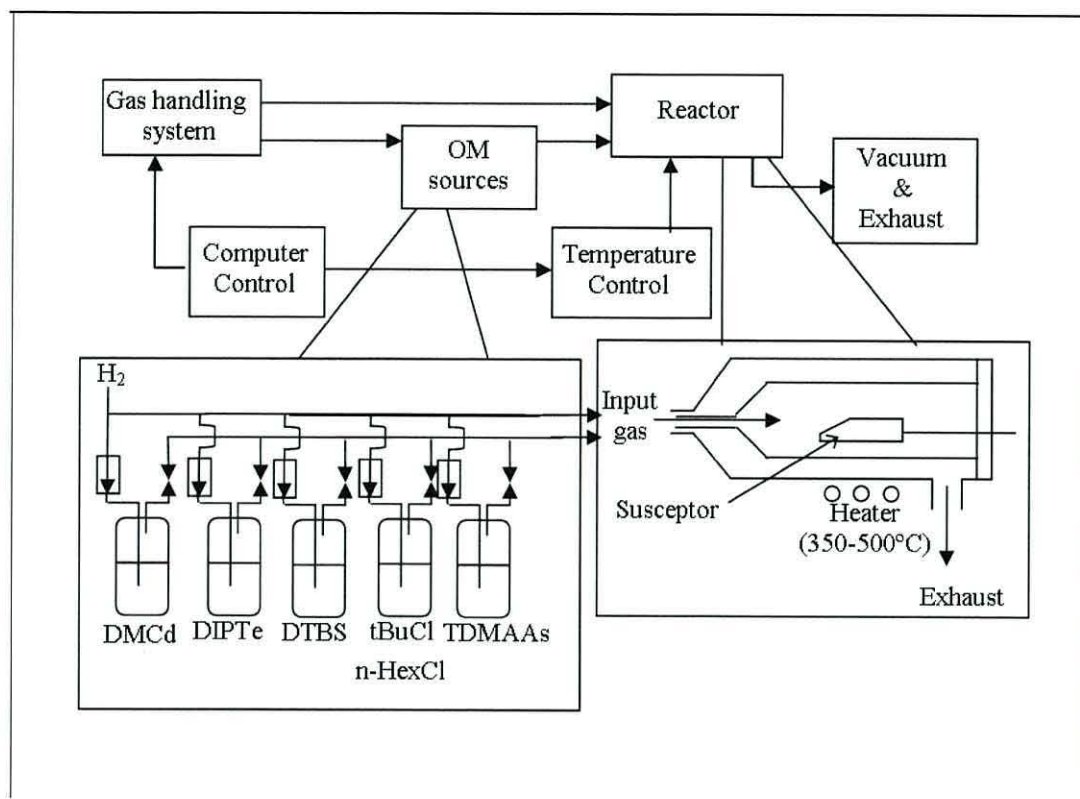
Fig 3.0 A Schematic of an MOCVD reactor.

Hydrogen was the carrier gas used for the organometallic precursors. The susceptor is heated using a retention heater. A horizontal MOCVD reactor was used to grow CdS/CdTe device structures at atmospheric pressure onto commercially available ITO/glass substrates from Merck (soda lime) and Delta Technologies Limited (alumino-silicate).The Cd, S and Te metal organic precursors used were; Dimethylcadmium (DMCd), Ditertiarybutylsulphide (DTBS) and Diisopropyltelluride (DIPTe), respectively. The dopant precursors were Trisdimethylaminoarsine (TDMAAs), n-Hexylchloride (n-HexCl) and Tertiarybutylchloride (tBuCl). The organometallic precursor temperature is regulated by temperature baths to control the precursor's vapour pressure. The layer thickness is monitored in real-time using *in situ* laser interferometry and can provide information on the growth rate. The average growth rate of the CdS and CdTe layers are 0.16 nm/s and 0.45 nm/s, respectively. A complete device structure growth takes approximately one working day after heating and cooling times and cleaning the reactor.

The choice of precursor is crucial in obtaining the desired properties from the products. The control of the film quality is pivotal and is related to the conditions in the reactor. Some of the key growth conditions are; temperature, gas feed composition, gas flow

rates and chamber pressure. MOCVD is in essence a multidisciplinary technique involving: The synthesis of precursors, the growth of high quality materials (on a large scale), thermodynamics, kinetics, chemical engineering and modelling. MOCVD offers a high degree of control over a large number of growth parameters.

3.4   Device Processing

Processing the growth material into devices involves chemical etching, evaporating the metal back contacts and making an electrical contact to the TCO using GaIn. The different processing steps are summarised in figure 3.1. The thin films are cleaved to the desired size (25×17 mm) using a diamond tip to score a guideline on the reverse of the grown layers, and tile cutters are used to cut the samples. The films are processed using two different bromine methanol etches. The first is used to etch strips off either side to allow the GaIn front contact to be added at a later stage (0.2 mL Br and 9.8 mL methanol). The second etch is more dilute (0.25 %) and is applied across the remaining CdTe surface to aid contacting to the back surface.

| The growth material is cleaved into three using diamond tip | Br/MeOH strip etch back to ITO for front contact | Br/MeOH or NP surface etch |

New process route omits wet chemical etch steps

Addition of GaIn front contact

Evaporation of Au back contacts

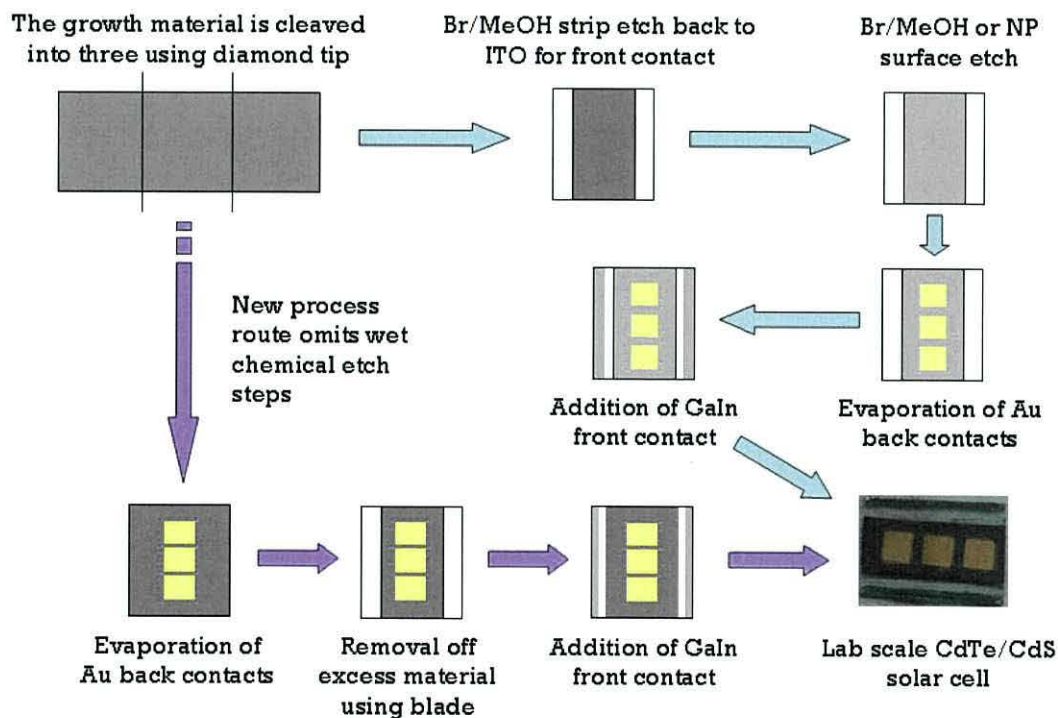| Evaporation of Au back contacts | Removal off excess material using blade | Addition of GaIn front contact | Lab scale CdTe/CdS solar cell |

Fig 3.1 Schematic showing a summary of the process steps involved in producing a solar cell.

The chemicals for the various etches are; bromine (Aldrich), HPLC grade methanol (WWR International Ltd), 70 % analytical grade Nitric acid (Fisher Scientific), 99+ %

Acetone (Aldrich) and 85 % WT solution phosphoric acid (Aldrich). The gold wire used for the back contacts was supplied by Agar Scientific.

The back contact of a PV device is a crucial element as it is one of the main areas for losses and therefore lowered efficiency. Copper is often used as a back contact metal with a work function of 4.65 eV, but Cu readily diffuses through the structure causing degradation. Gold is another common back contact metal with a work function of 5.12 eV. Au also diffuses through the structure causing degradation and has an added cost disadvantage. The contacts utilised are Au for the back contact and GaIn for the front contact. Gold is used as the back contact metal despite the cost as it is easy to deposit and has a high work function that is needed to contact wide bandgap semiconductors. As GaIn is liquid at room temperature the application is straightforward and simply involves spreading the liquid over the TCO previously revealed by etching.

The Au contacts are evaporated inside a tungsten filament evaporator at 4×10^{-5} Torr. The sample is placed in the evaporator with the desired mask on top. Au wire is placed in the filament directly above the mask and sample. The current is increased and the gold wire evaporates leaving the desired masking on the sample. The area and array of Au back contacts used throughout this work alters with the natural progression. The back contact area for all results will be quoted as this is an important property.

3.5 J-V characterisation

The electrical properties of PV devices are analogous to a diode and therefore the electrical behaviour can be explained in terms of standard diode equations with some modifications. Current-voltage characterisation is a non-destructive ex situ technique. I-V measurements are taken of the completed device. This technique provides averaged results and therefore does not yield information regarding local defects and non-uniformity. The device is subjected to a dark-sweep and then a light-sweep during which J-V measurements are taken as the voltage is swept between 1 and -1 volts. A range of information can be obtained from these curves including the standard device parameters;

- Short Circuit Current (J_{sc}),
- Open Circuit Voltage (V_{oc}),
- Fill Factor (FF)

- Overall conversion efficiency (η)

These values are commonly quoted in the literature to indicate the relative performance of the PV devices and are measured under standard conditions of 25 °C and AM1.5 spectrum. The device parameter values quoted were measured on the halogen lamp setup, however a comparative result for one device measured under AM1.5 (J_{sc} = 12.83 mAcm^{-2}) compared to the halogen light source (J_{sc} = 24.52 mAcm^{-2}) highlights that this setup over estimates the J_{sc} values.

J-V characterisation of the devices is undertaken at a constant power over the area of the photovoltaic test array (100 mW cm^{-2}) and was achieved using a light source consisting of 4×60 W halogen lamps. The light bank was calibrated before each batch of samples was analysed. The sensor objective has a diameter of 1 cm resulting in an active area of 0.78 cm^2. To ensure a power output of 100 mW cm^{-2} the light bank needs adjusting to read in the range of 76 < 78 > 80 mW. The lights are secured to an adjustable platform to aid calibration. Calibrating the entire exposed area is difficult to achieve as the light levels drop off at the edges. To aid calibration the position of the devices is marked on the set up and only this area is calibrated. The current-voltage measurements were carried out under illumination and dark conditions. The series and shunt resistances can be calculated from the I-V curves using the following equations:

$$V = IR \qquad R = \frac{V}{I} \qquad (3.0)$$

Calculating the gradient of the light sweep curve results in the conductivity (κ) of the device. The reciprocal of conductivity (κ) is the resistance.

$$R = \frac{1}{\kappa} \qquad (3.1)$$

The dynamic series resistance is the reciprocal of the gradient in forward bias (V > 0). The shunt resistance is calculated as the reciprocal of the gradient in reverse bias (V < 0). In each case a line of best fit to the relevant slope is drawn. A series resistance of <10 Ω and a shunt resistance of >130 Ω are common values for high efficiency devices. For each sample the resistance was calculated from the best contact on that device.

3.6   Optical microscopy

Optical microscopy is a non-destructive *ex-situ* characterisation technique, which enables the surface of the thin film to be viewed. This technique gives information on the uniformity of the growth, surface defects and surface roughness. The sample is placed on a microscope slide (glass side down) and positioned beneath the microscope objective. Surface defects including; scratches, pinholes and particulates can be identified. The thin film can be analysed at different magnifications. These defects have the potential to reduce the photo-response and therefore the device efficiency. Information obtained by optical microscopy is limited by the resolution and depth of focus; therefore other characterisation techniques are also employed. The magnification ranges are: M5, M10, M40 and M100. The optical microscope is connected to a camera to allow ease of assessment of the entire substrate.

3.7   X-ray diffraction (XRD)

X-ray diffraction (XRD) is the main analytical technique for structure analysis. This method provides precise determination of the atom positions in crystalline materials and solids with little error. X-rays interact with the planes of atoms in the 3D lattice, the separation of which is known as the d-spacing (d_{hkl}). Crystalline solids produce unique X-ray diffraction patterns based on the positions and intensities of each observed reflection. In mixtures of compounds each phase forms an individual set of reflections. The relative intensities of the different phase reflections give an indication of the amount of each phase present. Several factors can affect the intensity and number of reflections. These include; lattice type, crystal class, unit cell parameters and the distribution and atom type in the unit cell.

CdS has a hexagonal greenokite type structure and the reference X-ray diffraction pattern is shown in figure 3.2.
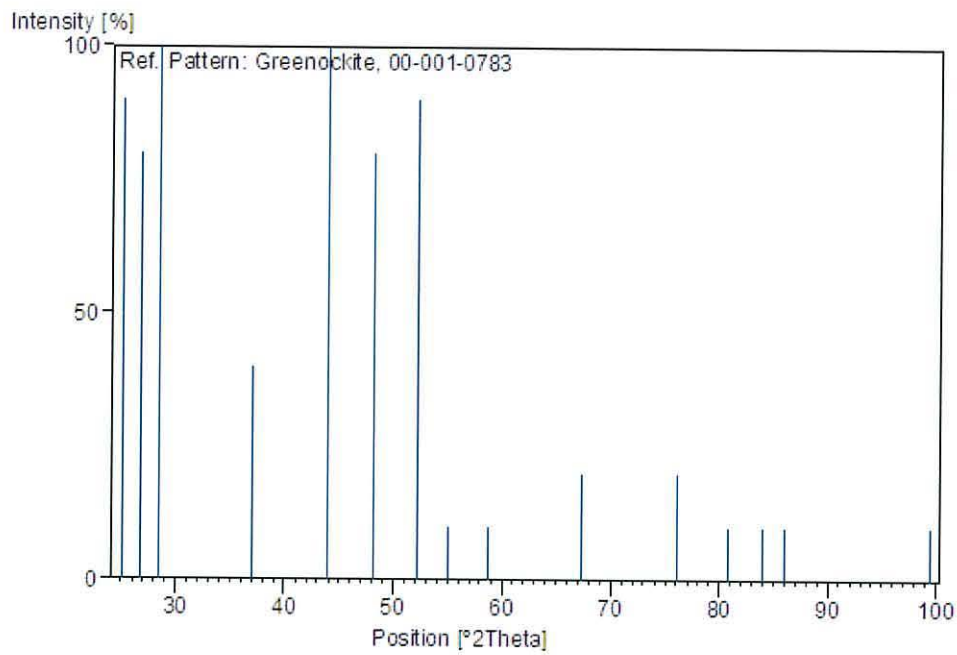
Fig 3.2 The reference X-ray diffraction pattern of hexagonal CdS [1].

The X-ray diffraction pattern of polycrystalline CdTe displays sharp (111), (220) and (311) peaks and has been indexed according to the CdTe cubic zinc blende structure. The reference pattern for cubic CdTe is shown in figure 3.3.
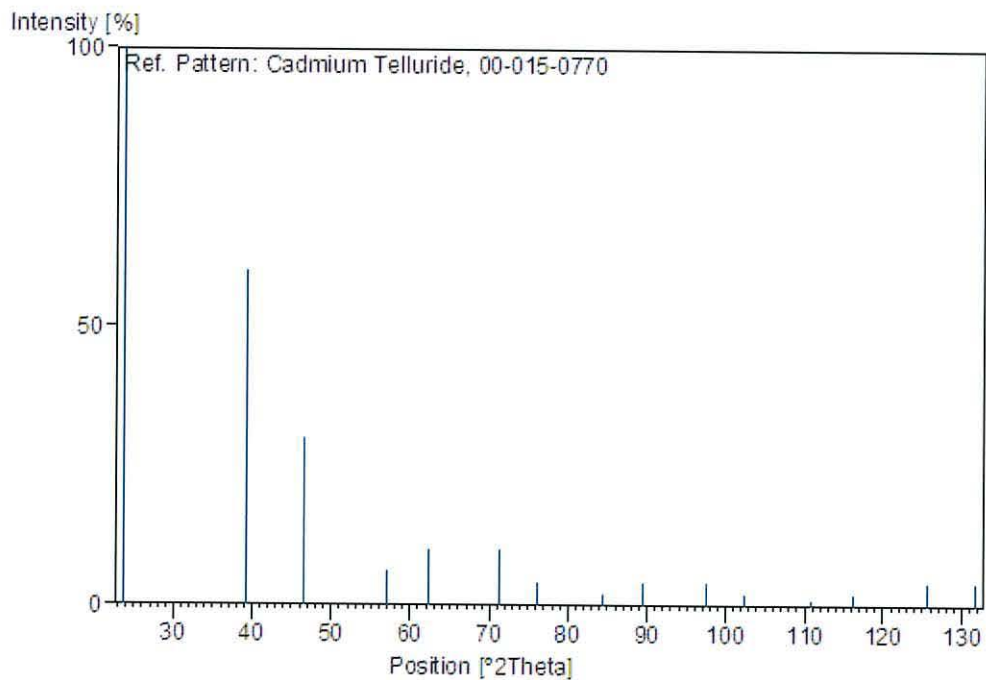

Fig 3.3 The reference X-ray diffraction pattern of cubic CdTe [2].

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XRD has been used to prove the existence of a Te layer after chemical etching with the observation of a Te (1121) peak at $°2\theta = 27.6$.

3.8 Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) was carried out on a Hitachi S-520 instrument. Samples were mounted on double-sided carbon tape on a sample stub. SEM operates in a reflection mode, secondary electrons reflected from the surface of the sample form the image. A voltage of 14 kV and emission current of 60 mA were utilised. Images were taken at varying magnifications (5-30 K), allowing the study of the general morphology and grain size. SEM also has a good depth of field and allows the study of samples at various angles. An electron gun acts as the source and produces a beam of high-energy electrons. The electron beam travels through a series of apertures and lenses, which focus the beam to a fine point. A set of scanning coils near the bottom of the apparatus, move the beam across the sample row by row. As the electron beam strikes the sample secondary electrons are produced. The final image is produced from the number of secondary electrons detected from each spot on the sample.

3.9 Energy Dispersive Analysis of X-rays (EDAX)

SEM is often accompanied by microanalysis allowing verification of the homogeneity of the chemical composition and confirming the presence or absence of different mineral phases. The secondary x-rays emitted from the sample can be used diagnostically to provide information on the composition of the sample. Detailed information on the identity of trace amounts of elements present can be determined, allowing the formation of maps of elemental distribution for the scanned area. This process is called Energy Dispersive Analysis of X-rays (EDAX).

3.10 Secondary Ion Mass Spectrometry (SIMS)

SIMS is a crucial technique for determining the extent of inter-diffusion within the thin films as this can lead to increased efficiency by aiding flow of electron-hole pairs, or degradation if contact metals (Cu) diffuse. SIMS depth profiles were carried out, using a Cs^+ primary ion beam, in a Cameca IMS 4f at CSMA-MATS UK and Loughborough surface analysis (LSA). The main experimental conditions of the SIMS profiles are summarised in table 3.0. The species investigated were; the matrix elements Cd, Te and

S and the intentional dopants arsenic and chlorine. The detection limits of As and Cl were in the region of low $\times$ 10^{16} atoms cm^{-3} and low to mid $\times$ 10^{16} atoms cm^{-3} respectively.

Instrument	Cameca ims 4f
Primary ion species	Cs$^-$
Primary ion energy	10keV
Primary ion current	70nA
Raster size	200μm
Secondary ions	Negative
Transfer lens	150μm
Analysed area	30μm
Contrast aperture	No. 3
Mass resolution	250

Table 3.0 Summary of the experimental conditions used during SIMS depth profiling.

The samples were chemically polished with a 0.25 % Br in methanol prior to characterisation to reduce surface contaminants and to smooth the CdTe surface. The sample preparation was adapted when characterising a dip in the arsenic as the chemical polish would remove the material of interest. These device structures were swabbed with methanol and dried with a nitrogen gun. SIMS depth profiles of the two preparation methods are shown in figure 3.4.
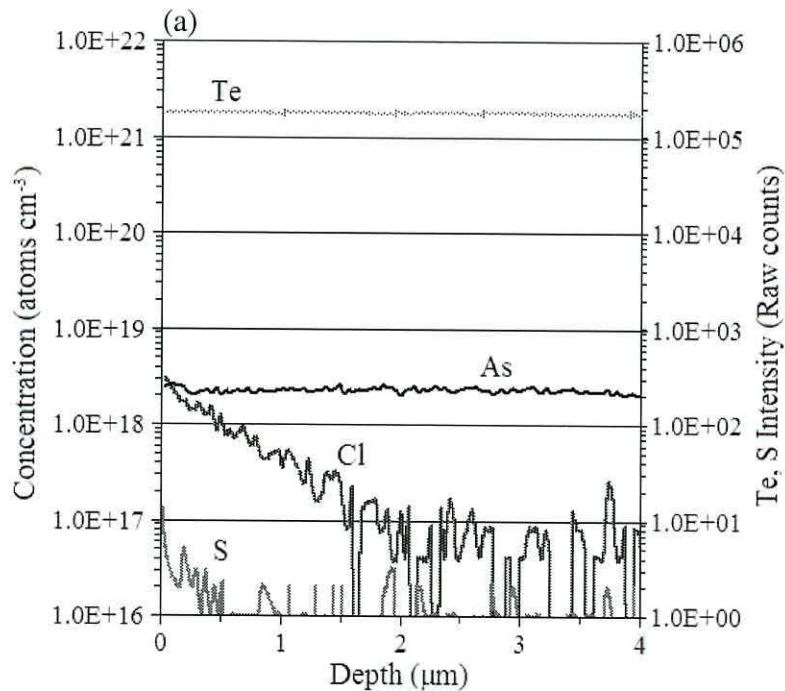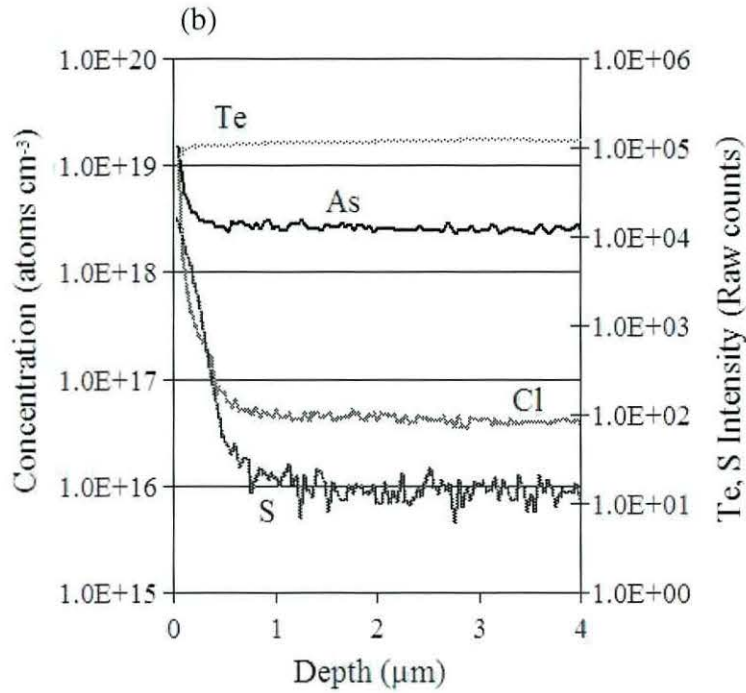
Fig 3.4 SIMS depth profiles of the two preparation methods (a) Br MeOH polish (b) Methanol swab

The Cl and S profiles have large initial concentrations which rapidly decrease away from the surface indicating the presence of surface contaminants. Although this effect is observed for both preparation methods it is less pronounced for the chemically polished sample.

Conditions were selected to simultaneously monitor the depth profiles for; the dopants Cl and As, diffusion impurity Na, process impurity H and atmospheric contamination O. The ion counts were calibrated into concentrations (atoms cm^{-3}) using supplied reference material of As and Cl implants in CdTe layers on glass substrates. The depth scales were determined by measuring the sputtered crater depths of the reference material using interference microscopy and assuming a constant rate of erosion. The samples supplied were 1 cm^2 sections cleaved from the device structures.

SIMS is a destructive analytical depth profile technique, which provides information on the thickness of the different layers, the amount of doping, inter-diffusion and the effect of etching. A schematic of a SIMS experiment is shown in figure 3.5. A high-energy, primary ion beam (incident beam) usually Cs$^+$ or O$^-$ bombards the surface. As the incident beam strikes the surface both neutral and charged species are ejected (sputtered).

47
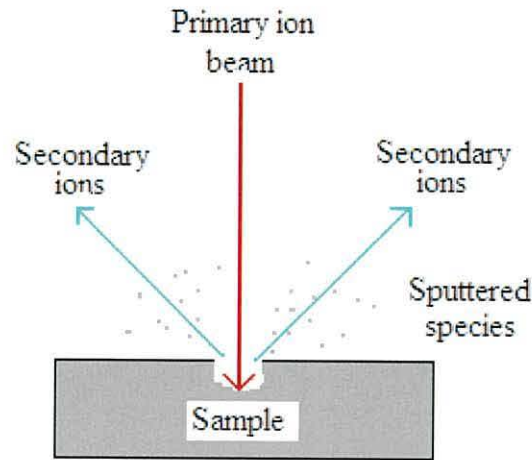
Fig 3.5 A schematic showing the primary ion beam milling the surface and the secondary ions ejected from the surface which are mass analysed.

The SIMS spectrum therefore consists of both the secondary ions that are stable to dissociation and the ionic fragments, which are not. These charged species are known as secondary ions and are energy filtered before being mass analysed. Only ions within a limited range of kinetic energies are mass analysed. The number of mass fragments contained in a SIMS spectrum is immense and therefore contains a wealth of useful information. This is one of the key advantages to SIMS and justifies the use of this highly destructive technique.

There are two types of secondary-ion mass spectrometry available: static and dynamic. The static SIMS experiment only removes and analyses the top layer of the sample. Dynamic SIMS removes and analyses several layers and yields information on depth profiling. Depth profiling is carried out to determine the thickness of the individual layers and the extent of interdiffusion. The sputtered species can settle back onto the surface, therefore to produce a realistic representation of the sputtered ions from the surface at a certain depth, the rate at which the beam erodes away the surface needs to be faster than the re-formation of the layer. The initial roughness of the surface can dictate the resolution of depth profiling. SIMS has detection sensitivity in the parts-per-million level. The detector response to different elements can vary by several orders of magnitude.

3.11　Summary

This chapter has described some of the characterisation tools which have been used in this work. The characterisation of polycrystalline material is a critical part of research into CdS/CdTe solar cells. Any additional characterisation techniques employed in this work are described in the appropriate sections of this thesis.

3.12 References

[1] Ylrich, Zachariaben., *Z. Kristallogr*, 1925, **62**, 262.
[2] Natl. Bur. Stand. (U. S.) Monogr, 1964, 25, **3**, 21.

4.0 Design and construction of a micro-LBIC and the discussion of preliminary results

4.1 Introduction

Chemical etches, anneal treatments and metallurgical processes used in the fabrication of PV devices can aggressively alter the surface morphology and cause microscopic variations in the electrical characteristics of CdTe PV devices. The micro-LBIC technique is a powerful tool in characterising photovoltaic materials, but is not routinely used in characterisation due to difficulties in achieving high resolution and the interpretation of the data. Hiltner *et al* [1]. identified that intensity and bias dependent effects could lead to misleading interpretations of the LBIC results. An advantage of the LBIC technique is the capacity to study devices under solar intensities thereby providing information on device behaviour under real conditions. This chapter discusses the design and construction of a micro-LBIC setup and presents and discusses the preliminary results.

4.2 Construction of LBIC apparatus

Although the LBIC technique has been employed for many years using a light source, the micro LBIC technique which can achieve micron resolution spot size utilising a laser source was pioneered at Colorado state university by Hiltner *et al* [1]. The characterisation technique is based on the electron beam induced current (EBIC) and optical beam induced current (OBIC) techniques but uses a laser source that can match solar intensities. The LBIC setup described here is largely based upon the system developed at Colorado.

This setup aimed to reduce the effects of background light and reflections by containing the apparatus in a blacked-out cabinet and placing the optical components in a vertical arrangement. The vertical arrangement also provides a pathway to reduce the error due to angular alignment as the housing components have individual alignment controls in all directions and tilt control. The occurrences of bias dependent effects, which can result in mis-leading interpretations of the data, were reduced here as all scans were carried out at zero bias. The laser beam is connected to a pulse generator which

provides an AC laser beam instead of a mechanical chopper as a chopper has poorer noise performance.

The LBIC apparatus consists of three subsystems; optics, device mounting and electronics, which are discussed below. The differences between the setup at Colorado State University and that at the University of Wales, Bangor are highlighted throughout the discussion.

Optics

The basic components for the optics system are: a fibre coupled laser diode, collimating lens and a microscope objective. Class 3B single mode fibre coupled laser diodes from Laser 2000 with wavelengths of 658 nm and 808 nm were selected and are a good match to the spectral response of the CdS/CdTe solar cells. The 658 nm laser was selected as it corresponds to the centre of the spectral range and the 808 nm laser was selected as it lies near the absorption edge of CdTe as shown in figure 4.0.
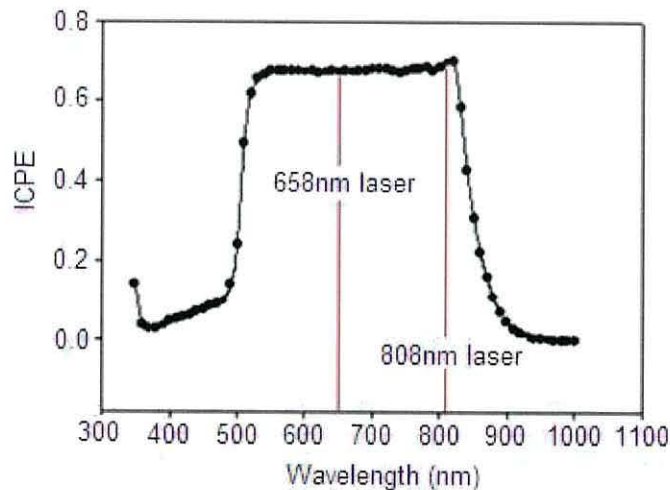
Fig 4.0 A plot of incident photon to current conversion efficiency (ICPE) of a CdS/CdTe solar cell.

The setup at Colorado included wavelengths of 830 and 850 nm, these wavelengths were not included in this setup as they lie beyond the absorption edge of CdTe and therefore are not necessary for characterisation of these devices. Additional wavelength lasers can easily be incorporated into the setup if alternate absorber layer devices are to be investigated.

The maximum output of these laser diodes at the end of the fibre is 14 mW (808 nm) and 31 mW (658 nm). The power of the lasers is controlled via a potentiometer on the

laser diode. The lasers are fibre coupled with single mode fibres which ensure a Gaussian profile. The setup is enclosed in an aluminium cabinet with blacked-out walls to reduce the effects of background light and reflections. The orientation of the optical setup also reduces the probability of accidental exposure to the direct beam.

The planar convex (PCX) lens was selected to produce a collimated beam radius that would fill the clear aperture of the microscope objective. The collimated beam radius, ω of the beam leaving the PCX lens can be calculated using equation 4.0

$$\omega = N.A \times f \tag{4.0}$$

Where $N.A$ is the numerical aperture and f is the focal length. The collimated beam radius of the light exiting the PCX lens in the experimental setup is calculated as 5.5 mm:

$$\omega = 0.23 \times 24 = 5.5mm$$

Alignment of the incoming beam is important as the collimating lens is sensitive to angular alignment. The mounting sections allow movement and angular adjustment in both the x and y directions to aid laser alignment.

The single mode fibre produces a Gaussian profile, which is transferred into another Gaussian beam when reflected by a lens. A Gaussian laser beam which is focused to a small spot spreads out rapidly as it propagates away from the spot. Therefore to ensure that the laser beam is well collimated through the apparatus a large beam diameter is required. The relationship between aperture and minimum spot size shown in equation 4.1 can be used to calculate the minimum spot size as discussed below.

An Olympus LUCLANFL ($\times$40/0.60) microscope objective with a working distance of 2.7 - 4 mm was selected. The microscope objective has a clear aperture of 9.5 mm in diameter which is sufficiently filled by the incoming beam radius from the collimating lens. The minimum theoretical spot size (ω_o) through the microscope objective is calculated from equation 4.1.

$$\omega_{min} = \frac{\lambda}{2\pi \, N.A} \times \frac{\phi}{\omega_o} \tag{4.1}$$

Where, ω_o is the radius of the incoming beam and ϕ is the clear aperture. The minimum theoretical spot size calculations based on the physical properties of the microscope objective for the two wavelength lasers are shown in the calculations below.

(1)
$$\omega_{min} = \frac{658 \times 10^{-9}}{2\pi \times 0.60} \times \frac{9.5 \times 10^{-3}}{5.5 \times 10^{-3}} = 0.30 \mu m$$

(2)
$$\omega_{min} = \frac{808 \times 10^{-9}}{2\pi \times 0.60} \times \frac{9.5 \times 10^{-3}}{5.5 \times 10^{-3}} = 0.40 \mu m$$

The optics system is shown in figure 4.1. This setup does not include the steering mirrors, polarizer and mechanical chopper from the Colorado setup as the laser diode output feeds directly into the collimation and objective lens system. The removal of a polarizer reduces errors caused by mode-hopping.
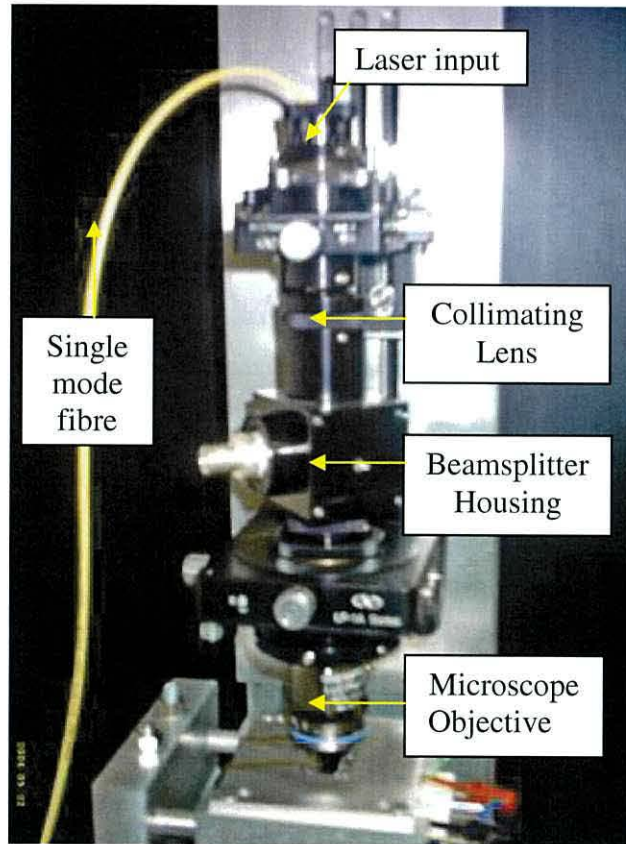
Fig. 4.1 A photograph of the optics system of the LBIC apparatus showing the direct input of the single mode fibre into the optical setup.

This arrangement reduces reflections and scattering and also allows quick exchange of the laser diodes if required.

Device mounting

Mounting the sample onto the xy stages was a challenge due to space constraints due to the small working distance of the microscope objective and the need to avoid damage to the microscope objective. The design for the sample holder on the Colorado setup is not suitable for the devices produced at University of Wales, Bangor and requires modification in order to accommodate the CdS/CdTe devices as presented in figure 4.2.

Sample Holder Design
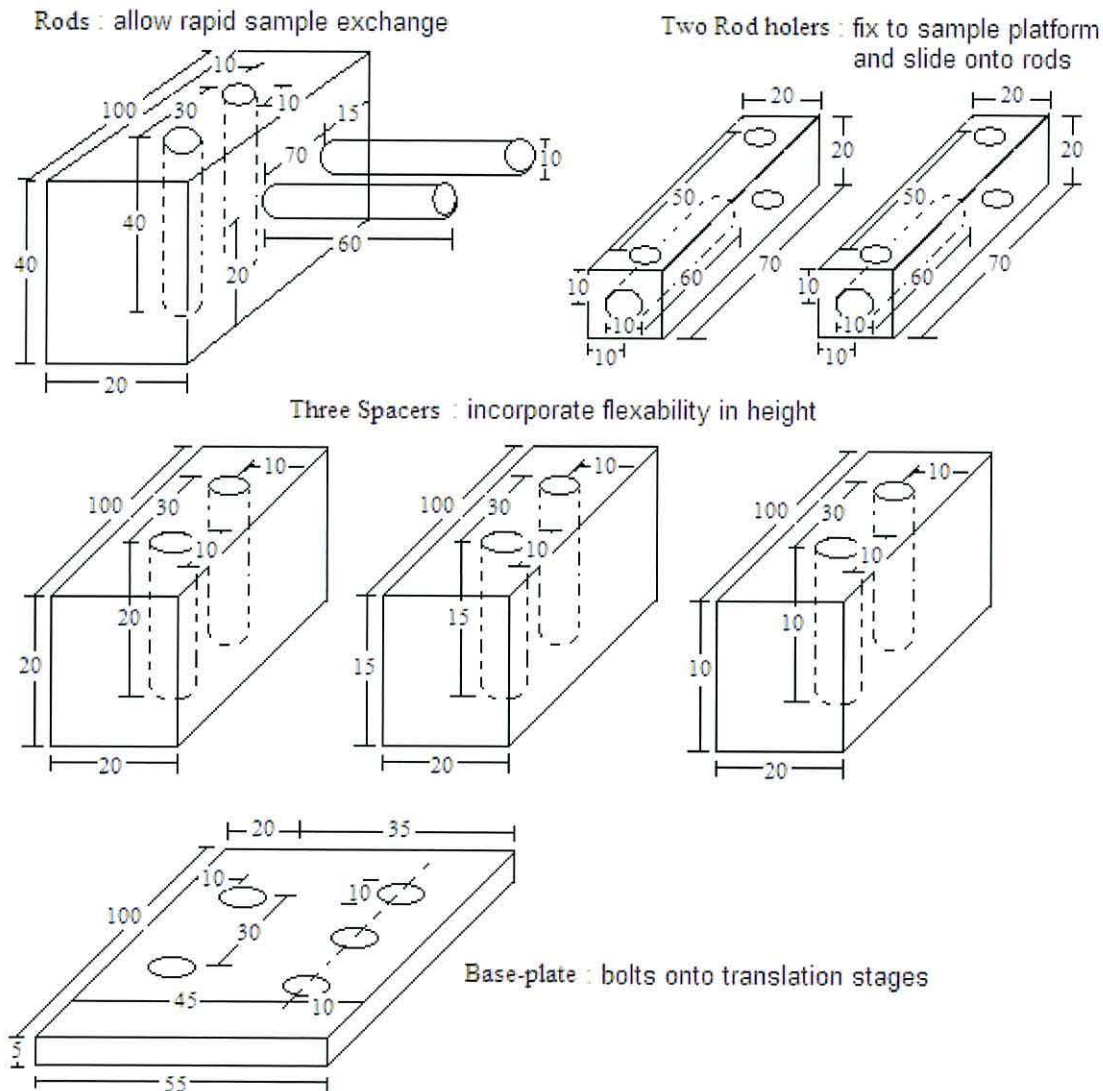
Fig. 4.2 A detailed design of the components of the sample holder: base-plate, spacers, Rods and rod holders.

The general concept of a platform on rods for ease of sample exchange utilised in the Colorado setup was adopted here. The sample holder with the rod supports is split into sections unlike the Colorado setup. Splitting the main rod section into several pieces and inserting various sized spacers between the base plate and the rods allows for future

variation and flexibility of the sample height beneath the microscope objective. The base plate is secured to the top translation stage through the three screw holes on the front. The two remaining holes house bolts to secure the spacer and rods sections to the base plate. Three different sized spacers 10, 15 and 20 mm were constructed to allow flexibility in the z direction.

The sample platform was constructed from a steel plate and has an aperture slightly larger than the size of a completed device as shown in figure 4.3. The device to be studied is positioned glass side up on the sample platform.
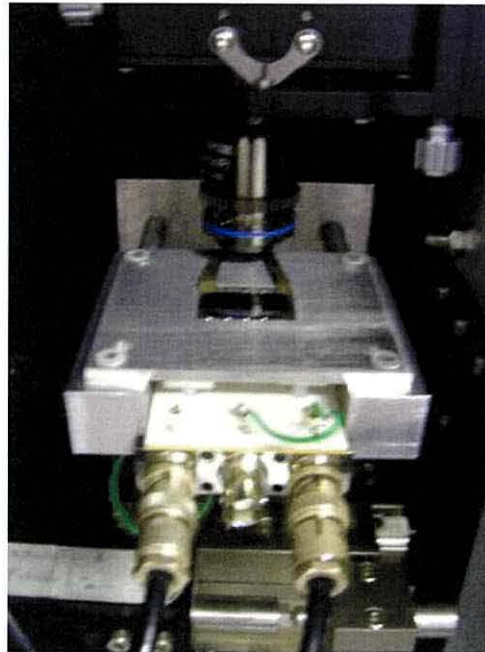
Fig. 4.3 Photograph of the sample platform designed to house the CdTe PV devices.

The GaIn front contact of the device rests on a series of spring pins which form one electrical contact. A section of gold wire on a magnetic arm is used to contact the Au back contacts from below. It was crucial to ensure the device lies flat in order to minimise the risk of damage to the microscope objective during a scan. Metal clips hold the device onto the spring pins ensuring a stable contact and also helps to keep the device level.

Electronics

A schematic of the electrical setup with all the key components is shown in figure 4.4. The laser diode is connected to a 12V DC power source and a pulse generator to power the laser and allow easy control of the laser frequency and symmetry of the laser beam

(i.e. how the laser is pulsed). The laser beam is modulated with the pulse generator to produce an AC laser beam. The pulse generator is used in place of a mechanical chopper and the modulation can also acts as the reference for the Lock-In amplifier ensuring that the measurement is synchronised with the pulsing of the laser. A laser frequency of ~15 Hz was selected based on the work by Sites et al [2].
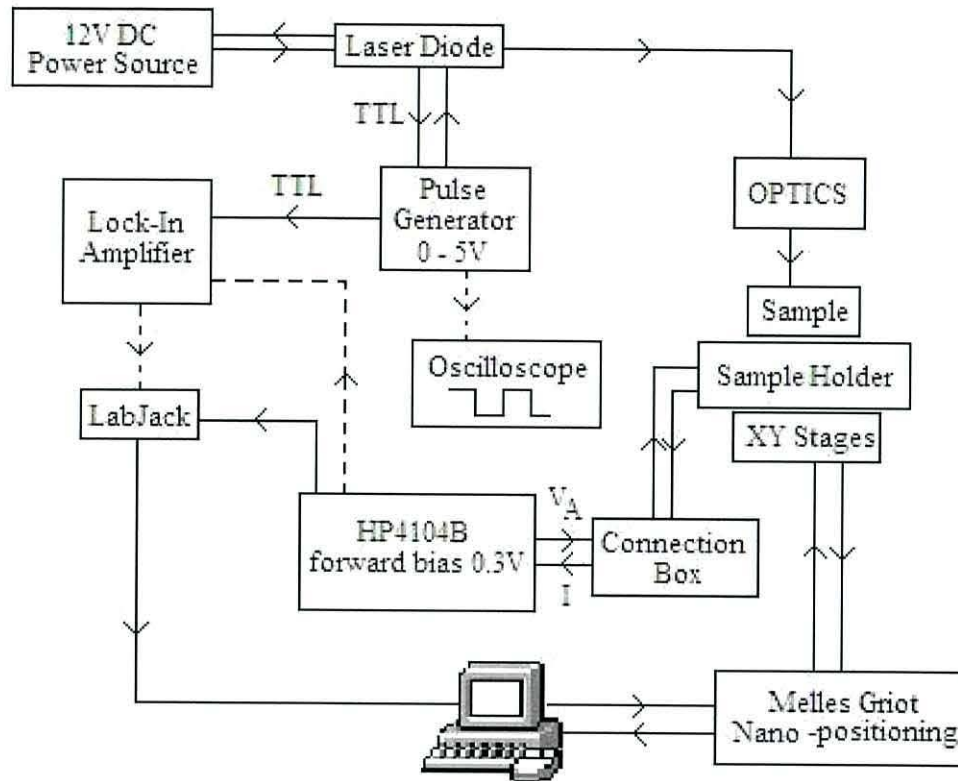
Fig. 4.4 A schematic showing the components of the electrical setup and how they are connected.

The device is incorporated into the electrical setup from the BNC connections on the sample holder via a connection box to the pico-Ampere (pA) meter. The current induced from the device by the laser is recorded by the pA meter, which converts the current signal into a voltage and then outputs this voltage to the Lock-In amplifier. The connection box can also apply a forward bias (0.3 V) across the device via the pA meter if desired.

A visual basic program was written to allow control of the LBIC apparatus from one screen and is presented in figure 4.5. The section headed "Channel Settings" provides control of the two nanostep stages. The run identification, scan area and step size are controlled in the "Scan Parameters" section.
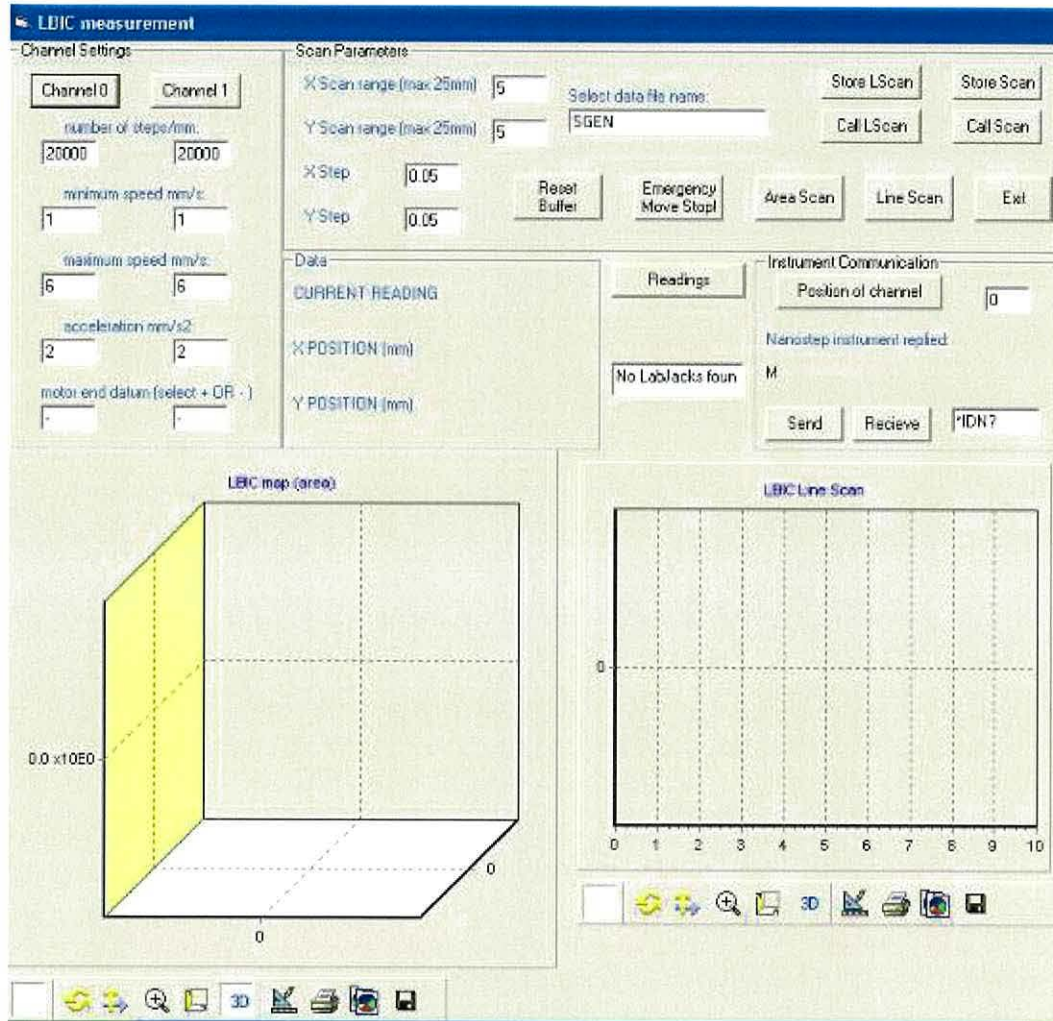
Fig 4.5 The operation screen of the visual basic program for controlling the LBIC apparatus.

The x and y position and reading are displayed in the "Data" section in real time and the data is plotted below in the appropriate axis for the type of scan. The operation screen also allows the user to save the images and manipulate the plot in 3 dimensions.

4.3   Initial LBIC images

At the lowest resolution (100 μm spot size) the area of a research-sized device can be mapped. At the highest resolution (1 μm spot size) the response of a single grain can be examined. The laser spot size incident on the device is an important parameter as the series resistance (R) of the device varies with the area of illumination as shown in equation 4.2.

$$R = \frac{\rho L}{A} \qquad\qquad (4.2)$$

Where, ρ is the resistivity of the material, L is the length the current flows and A is the area of illumination (laser spot size). This can introduce complications in separating high injection effects and resistive effects as both are dependent on carrier generation area[3, 4].

To determine whether the experimental setup and the visual basic program operate correctly an X is scribed into one of the square gold contacts. It is expected that where the X is scribed the induced current will be significantly reduced and therefore would be visible within the mapped area. A scan range of 10×10 mm was selected to ensure the 658 nm laser beam passes over the contact. The other key parameters were a spot size of ~300 µm and a step size of 100 µm. The resulting LBIC map is presented in figure 4.6 below.
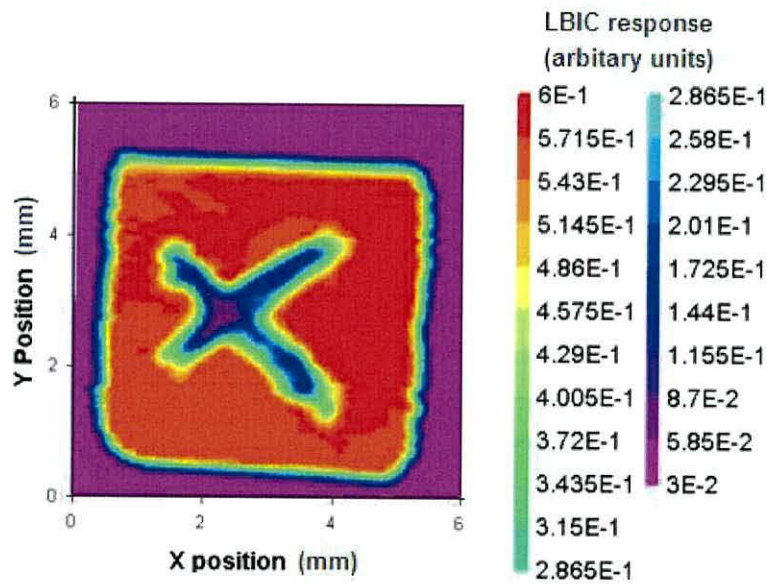
Fig 4.6 LBIC map of one gold contact with an X scribed into the gold contact with zero bias using the 658nm laser.

A square area of response, which is comparable to the size of one square contact 5×5 mm, is clearly visible with an X in the centre indicating that the experimental setup is operational. Lateral collection within a device can result in larger J_{sc} values as the collection area is larger than the contact area. This effect can be observed on an LBIC map as blurring of the edge of the contacts. The edges of the square in figure 4.6 are well defined and indicate that lateral collection of carriers from outside the contact area is not a dominating factor under these scan conditions. The NP etch commonly used in

the production of CdTe devices is more aggressive than the bromine methanol etch used to process the scanned device and it is assumed that lateral collection would be a more dominant factor for NP etched devices.

A LBIC scan of the same contact is presented in figure 4.7 with a scan range of 5×5 mm. The edge of the contact appears more graded than in the previous scan and highlights that although the edge of the gold contact is clearly defined in the LBIC maps the physical sharpness of the contact edge and any effects of lateral collection will limit the accuracy of the calculated spot size.
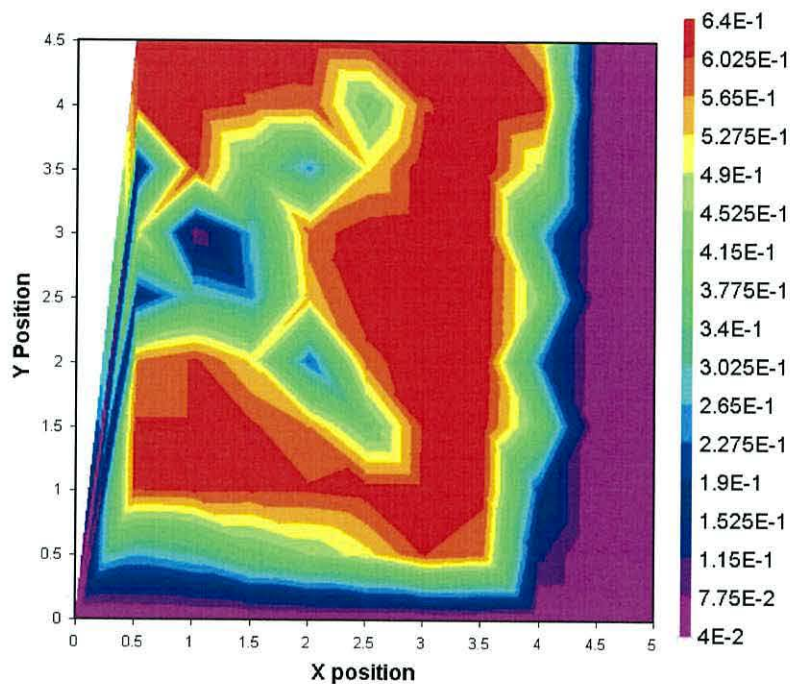
Fig 4.7 LBIC map of a contact with a X in the centre and a scan range of 5mm, using the 658nm laser.

There are three standard resolutions now commonly used in the LBIC characterisation of a PV device with a stepping distance commonly set to half the beam size [2]:

1. 5×5 mm area with 100 μm spot size.
2. 500×500 μm area with 10 μm spot size.
3. 50×50 μm area with 1 μm spot size.

The initial LBIC images presented above are at the lowest resolution and therefore the experimental setup requires optimisation to obtain a spot size in the order of 1 μm.

4.4 Optimising LBIC setup

As mentioned previously one of the main barriers to the routine use of the LBIC technique lies in the interpretation of the data. To reduce misleading interpretations, specific and reproducible methods of operation are needed.

Raw data

To investigate the reliability of the data the output of the pA meter was connected to an oscilloscope to visualise the signal. The LBIC response from the device generates a small AC signal which is superimposed on a large DC current. Hiltner et al [5]. found that devices in forward bias produced a large DC signal, but the scans in this work were carried out at zero bias. The performance of semiconductor devices is greatly influenced by the deep levels [6-8]. Deep level transient spectroscopy (DLTS) is a technique used to monitor the transients of junction capacitance and it has been found that small junction capacitance can occur in highly resistive materials [9, 10]. Deep trap levels in the CdTe material can therefore increase the capacitance and produce a large DC signal.

The large DC signal saturates the Lock-In amplifier and as a result the Lock-In amplifier was by-passed and the output of the pA meter was connected directly to the LabJack in order to obtain DC LBIC maps. This approach was adopted as the majority of the signal is DC and working with the smaller AC signal may result in more signal to noise problems. The Colorado setup electronically subtracts the DC portion of the signal, in order to obtain the small AC signal. Subtracting the DC may not be the best approach as the DC signal varies across the device. An alternate method to isolate the AC signal would be to incorporate a capacitor of an appropriate value to facilitate good conductance of the AC signal.

Laser spot size

The spot size is an important parameter as the resistance of the device is inversely proportional to the area as discussed in section 4.3 above. Calculating the experimental laser spot size obtained in the setup can be achieved by two methods:

1. measure the LBIC response through a slit
2. measure the LBIC response of a device with a sharp edge translated through the laser beam

Both methods will produce a step profile of LBIC response against position, which allows the laser spot size to be calculated. A series of line scans produced from the LBIC response achieved by translating the edge of a gold contact through the 658 nm laser beam at different microscope objective focuses are presented in figure 4.8. The translation stages had a step size of 1 μm.

Step profiles at different microscope objective focus

Fig 4.8 A plot of line scans off the edge of a contact with the 658nm laser to produce step profiles assuming negligible lateral collection. It should be noted that the focus numbers correlate to the different focus increments on the microscope objective.

The spot size of the 658 nm laser was calculated for each line scan using the $1/e^2$ approximation employed by Hiltner[1] and ranged from 6-36 μm. A plot of the calculated experimental laser spot size against microscope objective focal increment is presented in figure 4.9. As discussed above the observed sharpness (lateral collection) of the gold contact will affect the calculated spot size. In order to obtain a more accurate spot size a razor blade can be placed over the contact and used as the sharp edge translated through the laser beam.
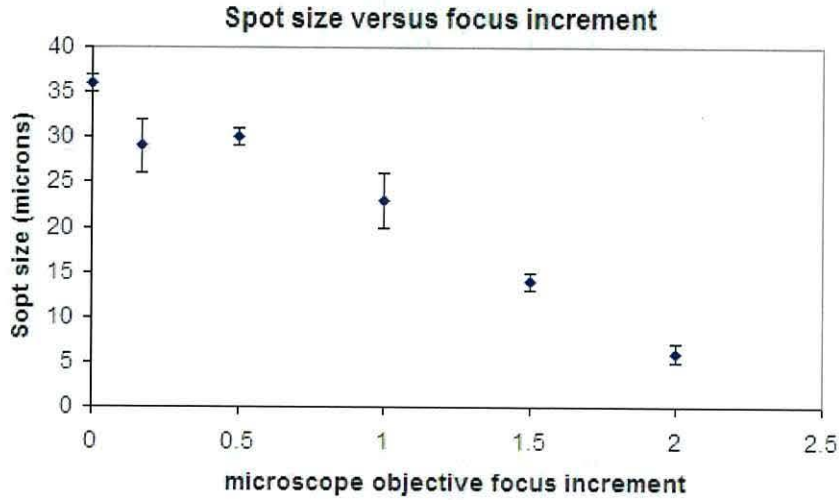
Fig 4.9 A plot of the calculated laser spot size against the focus increments on the microscope objective.

A $1/e^2$ definition of the LBIC response was utilised to calculate the laser spot size and results in a minimum spot size achieved to date of 6 μm ± 2 μm assuming negligible lateral collection. The largest calculated spot size from the data presented in figure 4.9 is 36 μm ± 2 μm. This indicates a range of 30 μm in laser spot size across the microscope objective focus increments for the 658 nm laser.

The same approach was carried out in order to obtain a minimum spot size for the 808 nm laser. The step profiles for the 808 nm laser are presented in figure 4.10.
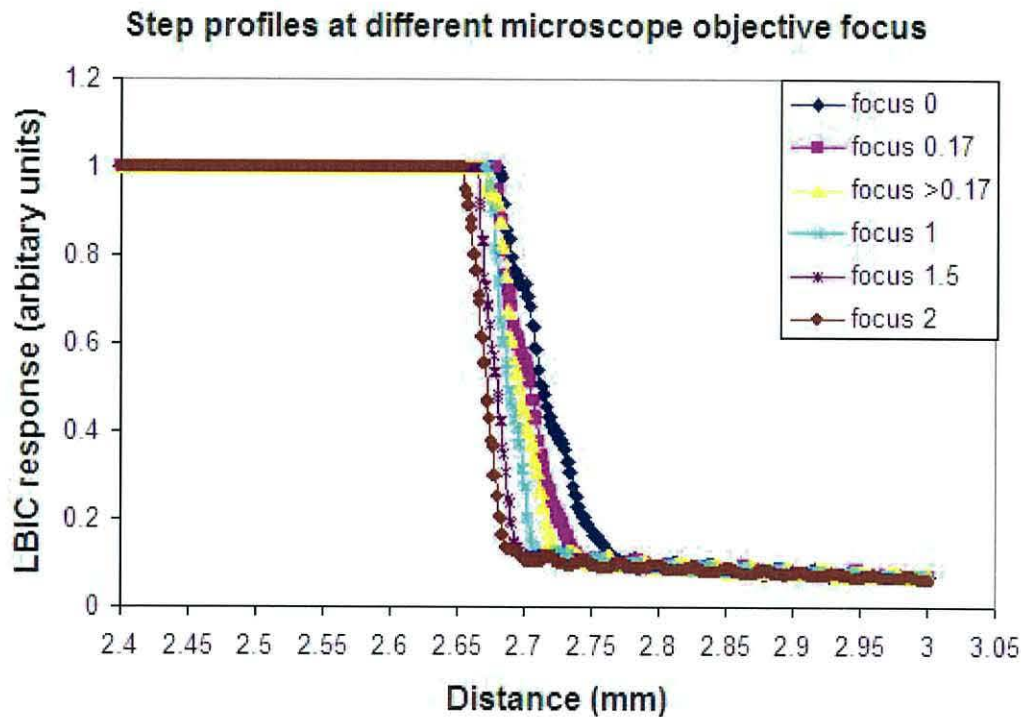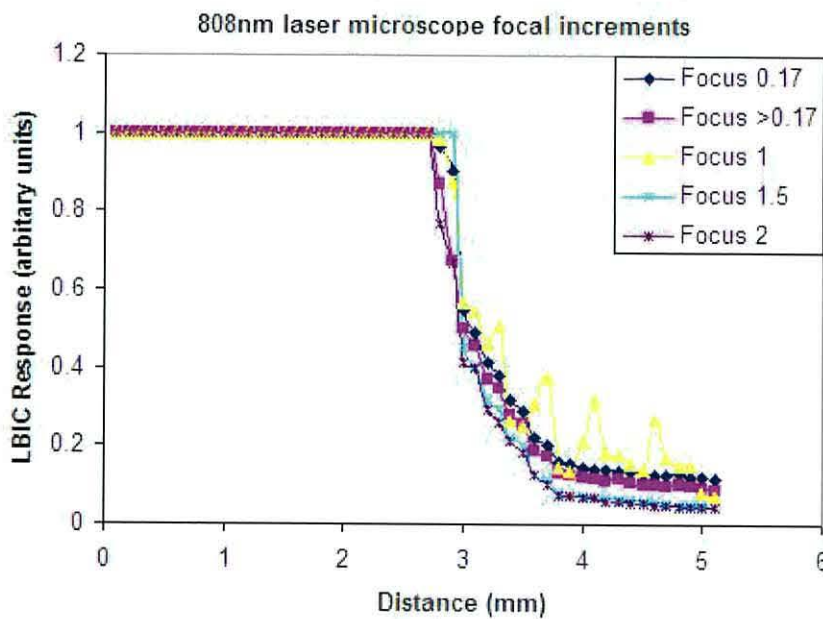

Fig 4.10 A plot of line scans off the edge of a contact with the 808 nm laser to produce step profiles assuming negligible lateral collection.

The minimum calculated spot size achieved to date for the 808 nm laser is 10 μm ± 2 μm, assuming negligible lateral collection. The maximum spot size obtained is 100 μm ± 10 μm, again assuming negligible lateral collection effects. The focal length of the 808 nm laser is different to the 658 nm laser and therefore the distance between the sample and the incident laser beam needed to be adjusted in order to obtain this resolution. The limitations to the obtainable spot sizes are discussed in more detail below.

Limitations to resolution

Spot size

A major factor in accurately determining the spot size is dependent on the device being perpendicular to the incident laser beam. If the device is not level beneath the laser, as the device is scanned there will be errors in the spot size across the scan area. Establishing where the drop-off in the step profiles occurs also presents an error in calculating the spot size. As mentioned above the $1/e^2$ approximation was used to establish the area of significance. Despite improvement to the spot size measurement with the use of a razor blade, the edge will not be infinitely sharp (due to diffraction) and therefore there is always an inherent limitation to the calculated experimental spot size.

Circular aperture diffraction

When light from a point source, such as a laser, passes through the small circular aperture of a microscope objective, it does not produce a single bright dot. Instead a diffuse circular disc or Airy's disc surrounded by much fainter concentric circular rings is produced. The imaging process is deemed to be diffraction-limited when the first diffraction minimum of the image of one source point coincides with the maximum of another. This is then the best resolution attainable with that size aperture. This limitation on the resolution of images can be quantified using the Rayleigh criterion so that the limiting resolution of a system can be calculated using equation 4.3,

$$\sin\theta_R = \frac{1.22\lambda}{d} \qquad (4.3)$$

Where, $\sin\theta_R$ is the resolution in radians, d is the aperture diameter and λ is the wavelength. The resolution of a microscope can be calculated from equation 4.4,

$$R = \frac{1.22\,\lambda}{n\sin\theta} \qquad\qquad (4.4)$$

Where, n sin θ is known as the numerical aperture of the microscope objective (0.60). This results in a theoretical resolution of 1.34 μm with the 658 nm laser and therefore the best spot size attainable with this optical setup is 1.34 μm compared to the calculated theoretical minimum spot size of the optical setup of 0.30 μm for the 658 nm laser using equation 4.1 as discussed in section 4.2 (optics).

Optical aberration

An optical aberration is an imperfection in image formation as a result of the optical system and is therefore another factor in limiting the attainable resolution of the LBIC apparatus. There are two forms of optical aberration that are relevant to this discussion:

1. Spherical aberration, which occurs when light rays strike a lens or mirror near its' edge.

2. Defocus aberration, which occurs when a system is out of focus.

A smaller aperture correlates to lower resolution and therefore the above features are important, but are unlikely to be the dominant factor in limiting the resolution of the optics setup as a smaller aperture reduces the effects of these aberrations.

4.5 micro-LBIC characterisation of CdTe PV device

LBIC measurements can provide information on the microscopic variations in minority carrier current caused by the contacting procedure, dopant incorporation and uniformity, but is not routinely used in cell characterisation. The LBIC setup was used to characterise CdS/CdTe solar cells deposited by MOCVD with different *in situ* arsenic doping concentrations to monitor the effect on device efficiency and lateral collection. LBIC maps of the five devices (SGEN 198, 199, 200, 203 and 204) with arsenic concentrations ranging from 1×10^{17} - 2×10^{19} atoms cm^{-3}, using the 808 nm laser, with a scan area of 5 mm^2 and a 0.1 mm step size are presented in figure 4.11.
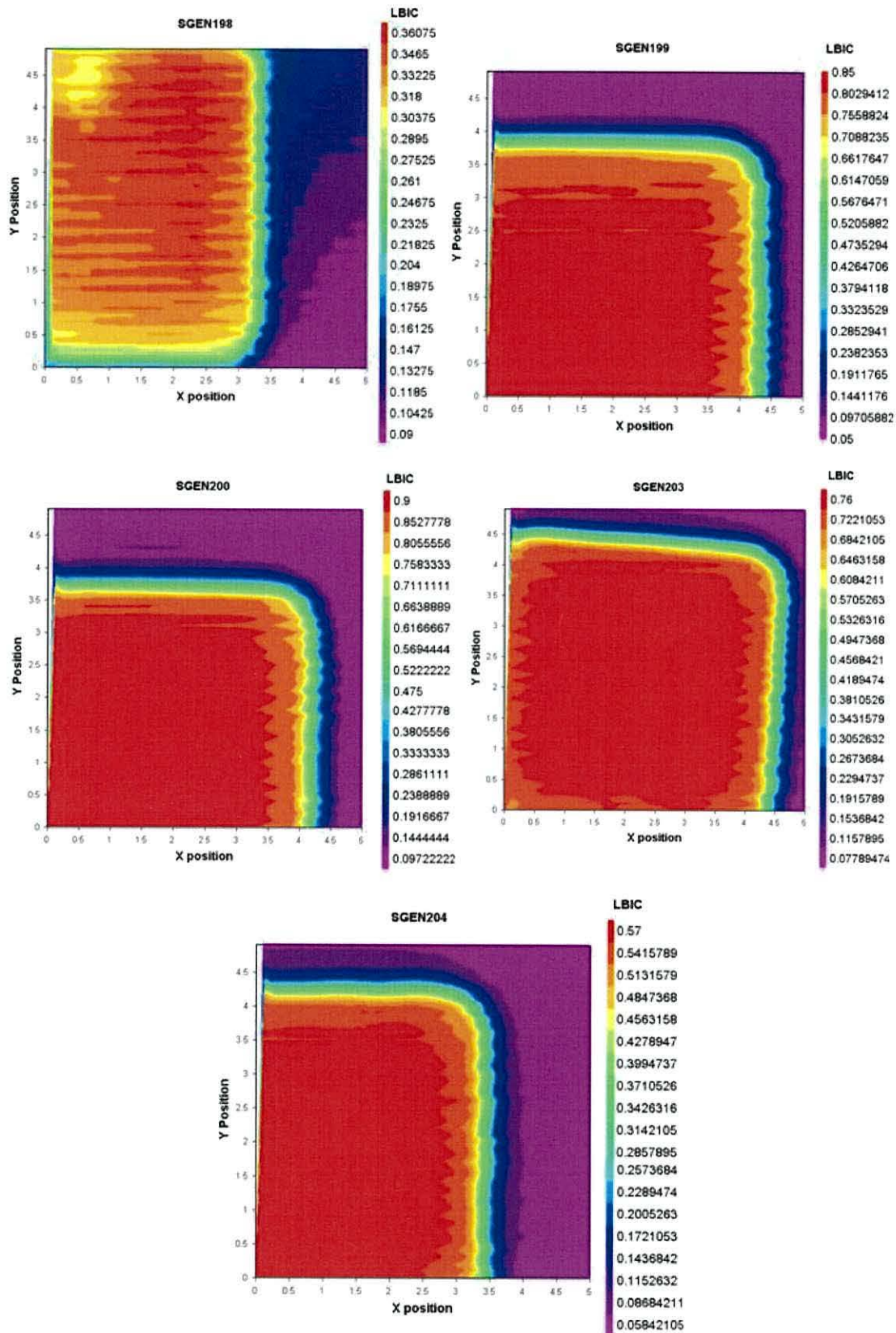
Fig 4.11 LBIC maps of five CdS/CdTe devices with different arsenic concentrations: SGEN198, SGEN199, SGEN 200, SGEN 203 and SGEN204. The x and y axis are the distance in mm and range from 0 to 5 with 0.5 mm increments.

In each image a large area of increased induced current (red) is visible which is attributed to the gold contact. These areas appear uniform with not obvious defects on the contact surface. The induced current from the devices is measured by the pA meter which converts the signal into a voltage and this voltage is read by the LabJack. Each LBIC map has a LBIC range of ~ 50 mV ±15 mV. The upper values of the LBIC scales for the five devices range from 237 mV to 916 mV indicating that the arsenic concentration affects the induced current. A plot of arsenic concentration versus LBIC response and device efficiency is presented in figure 4.12.
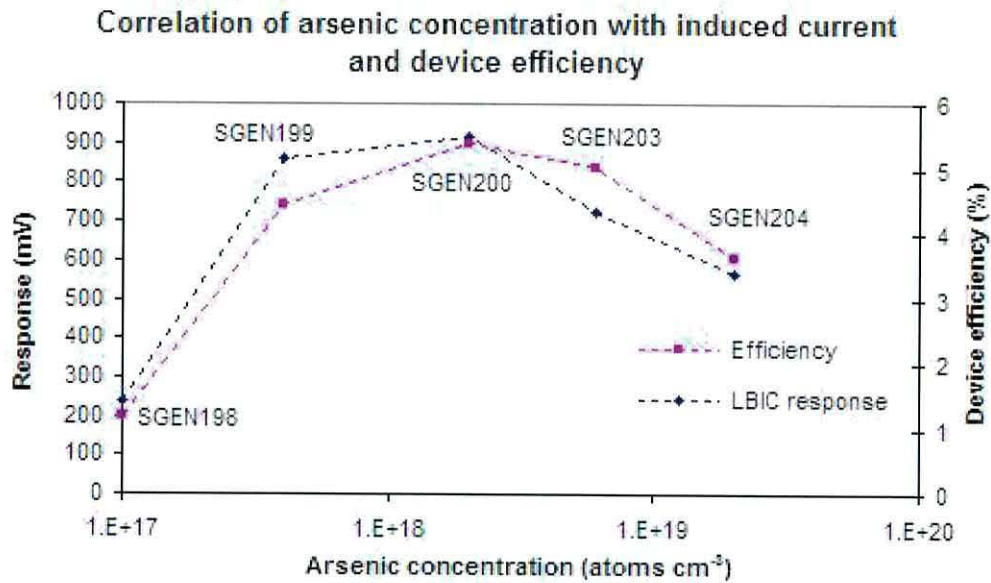
Fig 4.12 A plot sowing the relationship between the arsenic concentration, device efficiency and LBIC response of the five devices SGEN198, SGEN199, SGEN200, SGEN203 and SGEN204.

The plot in figure 4.12 clearly shows that the arsenic concentration in the CdTe layer goes through a maximum in terms of induced current and device efficiency at 2×10^{18} atoms cm^{-3}. The incorporation and activation of arsenic in CdTe is discussed in more detail in chapter 6.

LBIC mapping of each device was carried out over a 50 μm^2 area with a 5 μm step size (approximately half the beam width) to establish whether the micro-structure of the devices could be resolved. LBIC maps of the five devices are shown below in figure 4.13.

SGEN198

SGEN198

SGEN199

SGEN199

SGEN200

LBIC

- 0.916
- 0.9122353
- 0.9084706
- 0.9047059
- 0.9009412
- 0.8971765
- 0.8934118
- 0.8896471
- 0.8858824
- 0.8821176
- 0.8783529
- 0.8745882
- 0.8708235
- 0.8670588
- 0.8632941
- 0.8595294
- 0.8557647
- 0.852

SGEN 200

SGEN203

LBIC

- 0.724
- 0.72025
- 0.7165
- 0.71275
- 0.709
- 0.70525
- 0.7015
- 0.69775
- 0.694
- 0.69025
- 0.6865
- 0.68275
- 0.679
- 0.67525
- 0.6715
- 0.66775
- 0.664
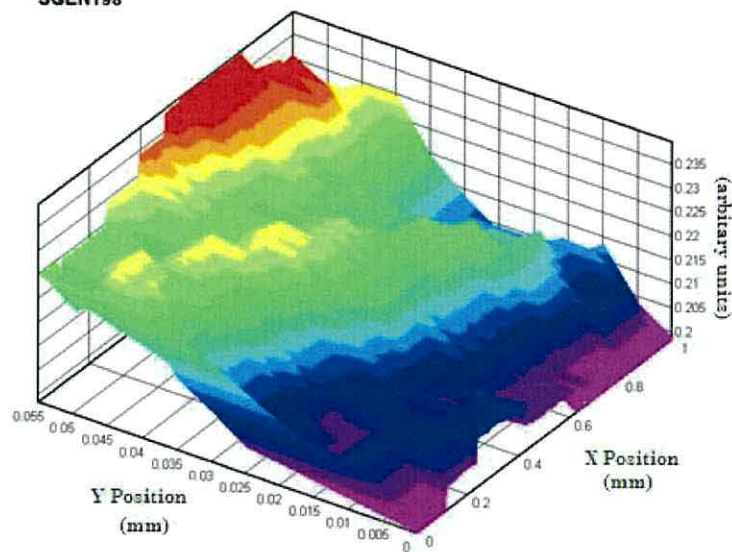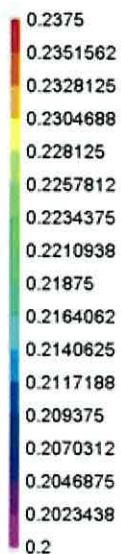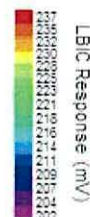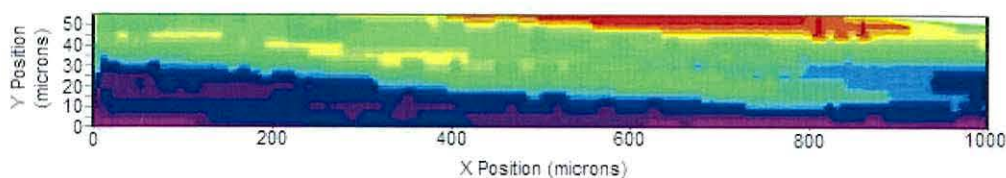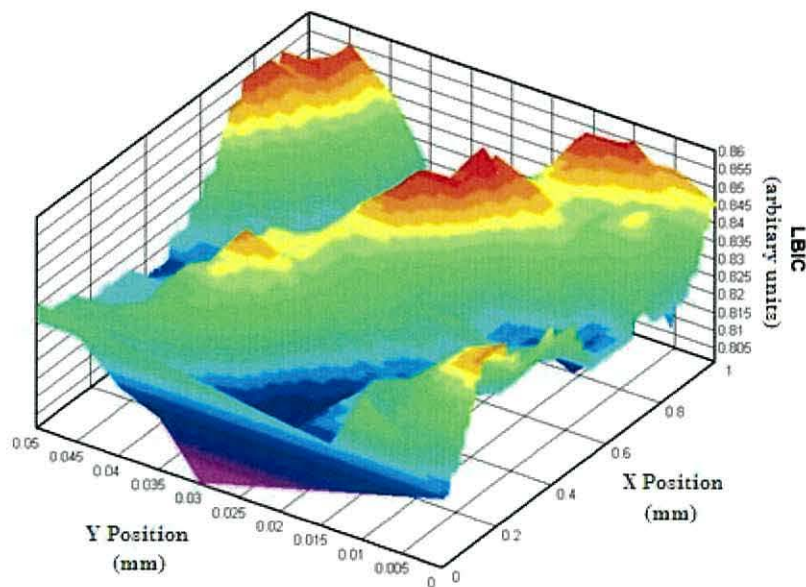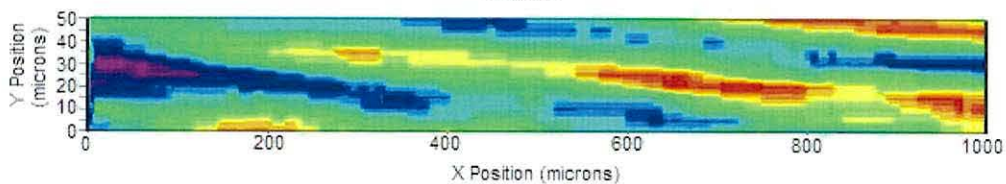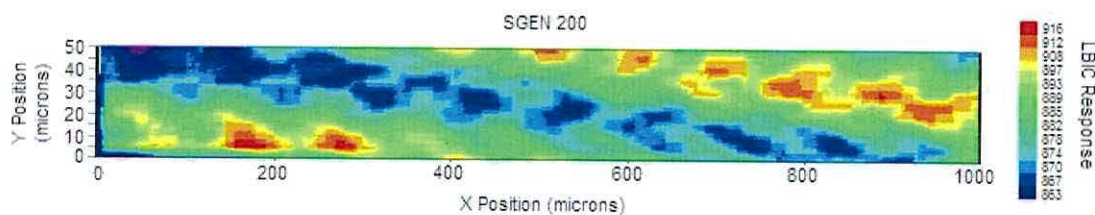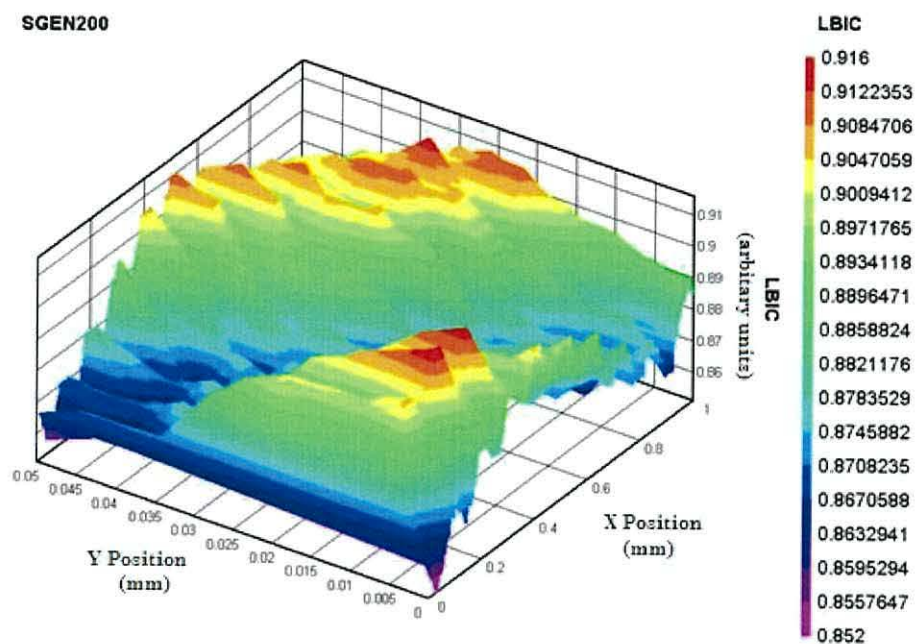
SGEN203
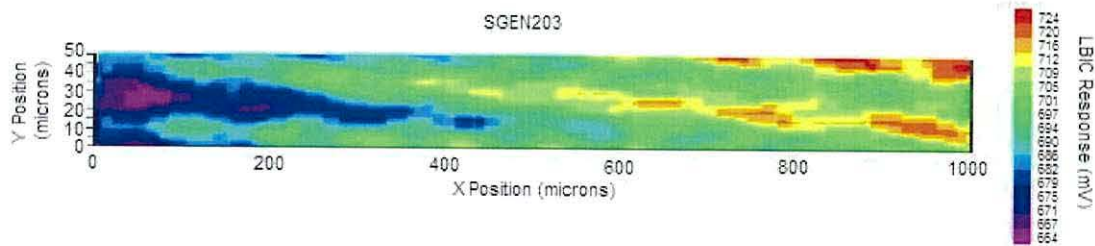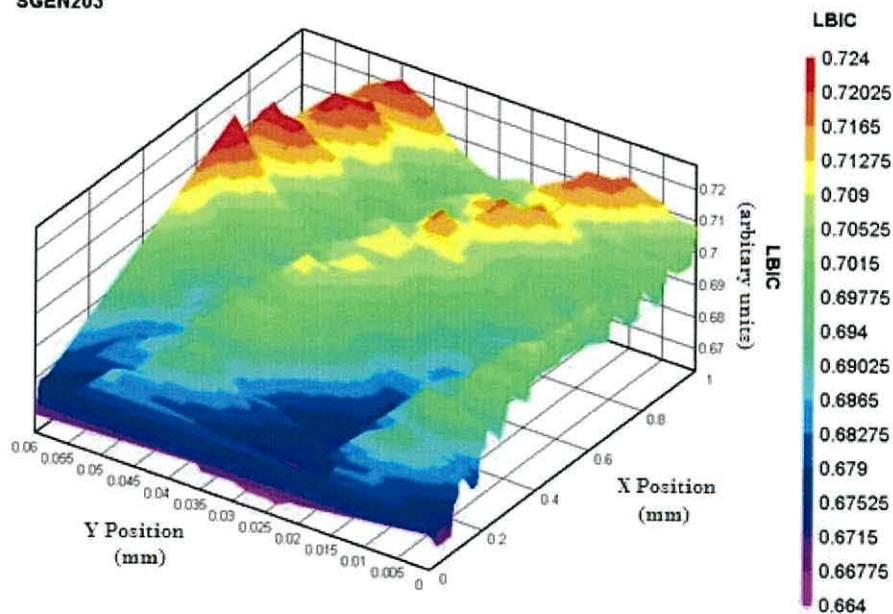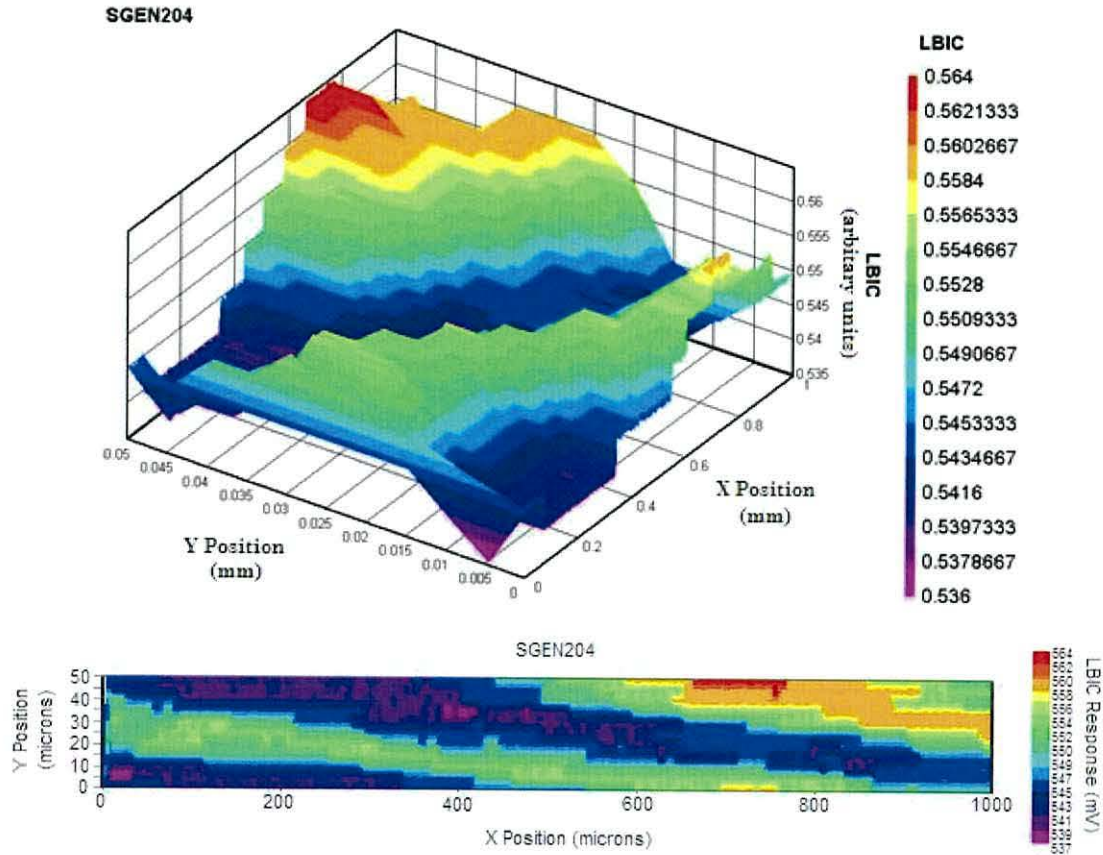
Fig 4.13 LBIC maps of five devices with different arsenic concentrations: 1×10^{17}, 4×10^{17}, 2×10^{18}, 6×10^{18} and 2×10^{19} atoms cm^{-3}, respectively, showing the difference in LBIC response (mV) across the scan area.

It should be noted that the 3D images are automatically plotted on a square axis despite the difference in the values of the x and y axis. Each map shows microscopic variations in the induced current with linear "furrow defect" features. These furrow defects are too large to correlate directly to the grain boundary networks in CdTe as they are ~10 μm across, but this highlights that there are microscopic changes in the electrical characteristics of CdTe, which are affected by the arsenic concentration in the bulk.

4.6 Summary

This chapter discussed the design and construction of a laser beam induced current (LBIC) apparatus at the University of Wales, Bangor. The setup was largely based on the apparatus designed by Hiltner et al [1]. at Colorado State University, but required several modifications. The laser diode input was connected directly to the optics setup in a vertical alignment to remove the need of beam steering mirrors, polarisers and beam choppers. This arrangement also reduced the effects of background light and reflections and the probability of accidental exposure to the direct laser beam to the

naked eye. The vertical setup provides increased control over angular alignment as each mounting component provides individual alignment control in all directions and angular movement. The use of a pulse generator in place of the mechanical chopper could provide a pathway to improved resolution. The limitations on the attainable resolution of the setup were discussed and using Rayleigh criterion calculated the optimum spot size attainable with the microscope objective as 1.34 μm for the 658 nm laser.

Initial low resolution LBIC images clearly show the intentional X scribed into the square gold contact. The edges of the contacts are clearly defined and sharp indicating that lateral collection from outside the contact area is not a dominant factor for these devices. The resolution of the setup has been improved and the spot size was calculated using a series of line scans off a gold contact. The best spot size achieved to date with $1/e^2$ definition is 6 μm ±2 μm (658 nm) and 10 μm ±2 μm (808 nm).

The induced current and device efficiency are both dependent on arsenic concentration within the bulk and pass through a maximum at 2×10^{18} atoms cm^{-3}. This indicates that the role of arsenic within CdTe devices could cause microscopic variations in the electrical characteristics of the material. High resolution LBIC maps of CdS/CdTe devices have revealed complex microscopic variations in the induced current with linear defects. These furrow defects are larger than the grain size of the material indicating that these features do not correlate directly to grain boundary networks as they are too large. These are preliminary results and therefore the nature of these defects is not yet fully understood, but this work has highlighted that the LBIC technique can provide pathways to monitor the effects of growth parameters on the induced current. Understanding these microscopic non-uniformities in electrical characteristics may help to overcome the barrier to improved CdTe device efficiency deposited by MOCVD.

4.7 References

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5.0   Application of the Taguchi Methodology

5.1   Introduction

The nature of polycrystalline CdS/CdTe material and the MOCVD growth method used in this research provide an immense number of growth parameters that may or may not be essential in achieving high efficiency devices. This posed the question, how do you incorporate all of the identified parameters and systematically achieve a high efficiency? This chapter provides a step by step guide to applying the Taguchi matrix method to MOCVD grown CdS/CdTe solar cells. A proposed criterion for establishing a control parameter's significance is outlined.

5.2   Constructing a matrix

The Taguchi method[1, 2] is aimed at improving the desired characteristics whilst simultaneously reducing the number of defects. This is achieved by studying the key variables controlling the process and optimising the procedures or design to yield the best results. The Taguchi methodology includes a set of tables that enable main variables and interactions to be investigated in a minimum number of trials. The Taguchi method design of experiments has been used to investigate the MOCVD growth technique of CdTe solar cells. The methodology is based on 'orthogonal arrays' of experiments to provide a minimal number of investigations that can rapidly 'tune' a given process for optimal results. There are eight key steps in the Taguchi methodology:

1. Identify the main function, side effects and failure mode
2. Identify the noise factors, testing conditions and quality characteristics
3. Identify the objective function to be optimised
4. Identify the control factors and their levels
5. Select the orthogonal array experiment
6. Conduct the matrix experiments
7. Analyse the data, predict the optimum levels and performance
8. Perform the verification experiment and plan future action

The main function was identified as the growth of high efficiency thin film CdS/CdTe photovoltaic material. The overall device conversion efficiency was selected as the objective function to be optimised (T_i). The side effects or failure modes were identified as: extended lattice defects including material uniformity and pin-holes, grain boundaries and recombination at defect centres and grain boundaries. Table 5.0 shows one of the L_8 matrices investigated in this work.

CdS growth temp. (°C)	CdS II:VI	Interaction	CdS thickness (nm)	CdTe thickness (µm)	CdTe growth temp. (°C)	As doping *p. p (atm)
-1: 300 1: 330	-1: 0.76 1: 1		-1: 240 1: 350	-1: 4 1: 6	-1: 350 1: 390	-1: 4×10⁻⁷ 1: 8×10⁻⁷
-1	-1	-1	-1	-1	-1	-1
-1	-1	-1	1	1	1	1
-1	1	1	-1	-1	1	1
-1	1	1	1	1	-1	-1
1	-1	1	-1	1	-1	1
1	-1	1	1	-1	1	-1
1	1	-1	-1	1	1	-1
1	1	-1	1	-1	-1	1

Table.5.0 An L_8 matrix of experiments investigated in this work (*p.p is partial pressure).

The matrix is termed L_8 as it consists of eight growth runs. The column headings indicate the chosen control factors and their designated levels. A matrix with three levels was also investigated in this work and is discussed in more detail in section 5.14.

5.3 Interactions

The orthogonal nature of the Taguchi method makes it crucial when designing a matrix to keep the number of interactions to a minimum due to their complexity. Even with careful design some interactions are unavoidable. A natural interaction exists between As doping and the CdTe precursors II/VI ratio. In such cases an additional column (A+B) is added to the matrix to monitor the sensitivity of any interaction. Due to the complex nature of interactions it is not possible to determine which combination of the two parameters produces the optimum result. The Taguchi method simply highlights where interactions occur and can monitor their sensitivity. The interactions need to be investigated outside of the matrix experiments to establish their effect on device performance.

5.4 Analysis of a matrix

Equation (5.0) is used to calculate the result of each control factor for matrices with only two levels. For each column in the experimental matrix there will be a value (T_i), which represents the effect of that parameter. The results of a Taguchi matrix, T_i are based on the following:

i.   The average device efficiency results (η_j) for each run (j)

ii. The (+) and (-) combinations of levels (L_{ij}) for each parameter (i) and each run (j)

$$T_i = \sum_j \eta_j \times L_{ij} \qquad (5.0)$$

A negative value favours the original level, a positive value favours the new level and zero would indicate that the ith parameter has no effect. It is essential to determine what value for T_i signifies a significant change or can be considered as zero within statistical error. Each matrix establishes a new set of optimum conditions, which then requires a verification experiment. The sixth experimental matrix requires an alternate analysis as there were three levels for each control factor and this is discussed in detail in section 5.14.

5.5 Stability of results

Due to the statistical nature of the Taguchi methodology uniformity across the growth layers and stability of results are important factors. To monitor the variance each device was processed with an array of ten gold spot contacts (0.025 cm^2), as back contacts. An average efficiency and standard deviation were calculated for each device based on the J-V curves of each individual Au spot. This approach was also utilised for the Fill Factor (FF), Short-circuit current (J_{sc}) and Open-circuit voltage (V_{oc}). The stability of the MOCVD growth method was monitored in two ways:

i.   Growth of the verification experiment

ii. Regular repeat growth runs

The verification experiment is a crucial part of the Taguchi method and can also provide a means of monitoring the growth technique. Running regular repeat devices supplies a means of checking the growth setup after routine maintenance and the changing of bubblers.

The general convention of the Taguchi method as mentioned previously is to select one function to be optimised. During this work the device efficiency was selected to be optimised whilst extending the approach to simultaneously monitor the other key device parameters; FF, J_{sc} and V_{oc}. Monitoring all of the device parameters provides a more diagnostic investigation by highlighting which device parameter has caused the overall device efficiency to change. Thereby evaluating reasons why the control parameter has a positive, negative or negligible effect on the device efficiency.

5.6 What is a significant result?

This section looks critically at the Taguchi methodology on a system with inherent noise and applies a novel criterion to establish significant results [3]. In order to interpret the results of the matrix it has become essential to establish a threshold value in order to determine whether a parameter has a positive, negative or negligible effect. To the authors knowledge there is no common convention for identifying a suitable threshold value. To identify the value for significant change the following method was employed:

    i.   Calculate the standard deviation for each result, using an array of back contacts.

    ii.   Calculate the standard deviation (σ) of each Taguchi result (T_i) from the RMS of the combined standard deviations from each run.

    iii.   Any Taguchi result (T_i) value equal to or greater than the threshold of 1 $\times\ \sigma$ is a significant effect, all other values are neglected.

Efficiency (%)	Standard deviation
4.26	0.32
3.49	0.10
4.60	0.19
3.43	0.29
2.83	0.05
5.40	0.08
4.73	0.40
2.81	0.03

Table 5.1 The average device efficiencies and standard deviations from the third matrix of experiments used to calculate the threshold value for significance.

An example of the application of this methodology is shown in the calculation below, with values taken from the standard deviation listed in table 5.1, identified as step i. The standard deviation (ΔT_i) for all the Taguchi results is then calculated from the RMS value of the standard deviations as follows (step ii):

$$\Delta T_i = \sqrt{(0.32)^2 + (0.10)^2 + (0.19)^2 + (0.29)^2 + (0.05)^2 + (0.08)^2 + (0.40)^2 + (0.03)^2}$$

$$\Delta T_i = 0.63$$

Therefore, any Taguchi result (T_i) equal to or greater than 0.63 has a significant effect; all other values can be taken as having a negligible effect within statistical error. The outcome of the Taguchi matrix analysis is represented graphically in figure 5.0.
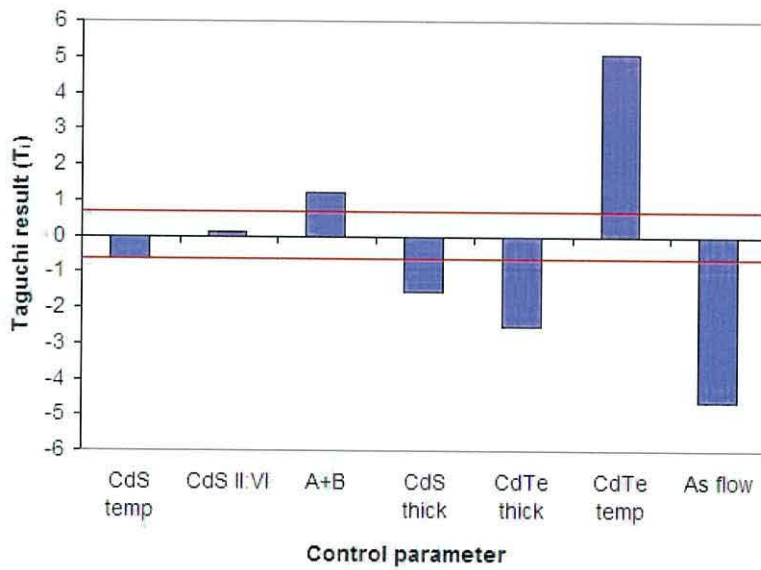
Fig.5.0 The deviation of the control parameters Taguchi results from the established threshold value 0.63.

The red lines mark the band established as insignificant change. The Taguchi results for the following control parameters; CdS growth temperature ($T_{i(\eta)}= -0.62$) and CdS II:VI ($T_{i(\eta)} = 0.1$) fall within this limit and are therefore deemed insignificant results under the chosen conditions. Any value outside this area warrants further investigation. This approach can also be applied to other device parameters being monitored.

5.7   Verification experiments

The final step of the Taguchi methodology is to perform a verification experiment in order to confirm the predicted optimum conditions produce the optimal result within the investigated levels. It is important to note that the confirmatory experiment might not necessarily be one of the combinations investigated. The verification experiment can be one of the following:

- A repeat of the best result
- A combination of the best control factor levels

The first option will confirm whether the best result from the experimental matrix is repeatable, but will always neglect the combinations that were not included in the matrix design. The second approach will encompass the investigated combinations and those excluded from the original matrix design. Consistently using either method makes both approaches valid verification experiments.

In this work the first growth run of each matrix acts as the verification and is a combination of the best control factor parameter levels from the previous matrix. For example the first growth in the second experimental matrix is the verification experiment for the first experimental matrix. The verification experiment also acted as a means to monitor any variation in the growth technique. Neither of the approaches listed above monitor the affect of the control factor levels on the formation of stable front and back contacts, therefore these issues need to be monitored separately.

5.8   MOCVD growths

The growth runs were carried out by Dr Vincent Barrioz, Mr Eurig Jones and I. Details of the MOCVD reactor and the organometallic precursors used can be found in chapter 3. The construction of the matrices was a collaborative effort within our research group. The processing of the growth material, characterisation of the completed devices and analysis of each matrix are the main focus of this part of the thesis. The individual growth run material was sectioned into thirds and one segment (17×25 cm) was processed into a working device by a series of chemical etching and metal contacting as described in chapter 3. The back contact array utilised in fabricating a working device will be highlighted separately for each matrix of experiments. This work focuses on the interpretation of the matrix results in terms of: (i) what is a significant result and (ii) material characterisation. Each of the six experimental matrices is discussed in the following sections in terms of (i) experimental design, (ii) device characterisation and (iii) Taguchi results.

5.9   First matrix

The growth conditions used as the start point for the design of the first matrix are:

1.   ITO soda lime glass substrates,

2. CdS deposition temperature 300 °C with II:VI of 0.76,

3. CdTe deposition temperature 350 °C with II:VI of 1 and a thickness of 2 µm [4].

These growth parameter settings were used as the first growth run within the first Taguchi matrix of experiments. In addition to the above growth steps the following were considered: (i) arsenic and chlorine doping of CdTe, (ii) affects of an anneal step and (iii) CdCl$_2$ top layer, as they are critical steps in the fabrication of high efficiency devices[5].

As described in section 5.2 each column heading is a separate control factor and each control factor is assigned two levels denoted (1) and (-1). The First matrix shown in table 5.2 is known as an L$_{12}$ matrix as there are twelve different growth runs generated by the chosen control factors and parameter levels. The design of this matrix incorporates several interaction columns as annealing can have a complex affect on polycrystalline material causing intermixing of the CdS and CdTe layers, aid interdiffusion of impurities and facilitate grain growth mechanisms. The four end columns in the matrix denoted; AE, CE, DE and EF were included to monitor the sensitivity of the possible interactions between the control factors.

Run ID	CdS thickness	CdTe thickness	As doing (p.p*)	Cl doping	30 min anneal	CdCl$_2$ layer	AE	CE	DE	EF
	1:240nm -1:120nm	1:4µm -1:2µm	1:4×10^{-7}atm -1:None	1:2sccm -1:None	1:500°C -1:350°C	1:10nm -1:None				
sgen6	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
sgen7	-1	-1	-1	-1	-1	1	-1	-1	-1	-1
sgen8	-1	-1	1	1	1	-1	-1	1	1	-1
sgen9	-1	1	-1	1	1	-1	-1	-1	1	-1
sgen10	-1	1	1	-1	1	1	-1	1	-1	1
sgen11	-1	1	-1	-1	1	1	-1	-1	-1	1
sgen12	-1	1	1	1	-1	1	-1	-1	-1	-1
sgen13	1	-1	1	-1	1	1	1	1	-1	1
sgen14	1	-1	-1	1	1	1	1	-1	1	1
sgen15	1	1	1	-1	-1	-1	-1	-1	-1	-1
sgen16	1	1	-1	1	-1	1	-1	-1	-1	-1
sgen17	1	1	-1	-1	1	-1	1	-1	-1	-1

Table 5.2 The first Taguchi matrix of experiments showing the control factor and the levels under investigation.

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* TDMAAs partial pressure

The orthogonal nature of the Taguchi matrix method makes it crucial when designing a matrix to keep the number of interactions to a minimum. Due to the complex nature of interactions it is not possible to determine which combination of the two parameters produces the optimum result. The Taguchi method simply highlights where interaction occur and can monitor their sensitivity.

5.9.1 Characterisation of the first matrix

J-V measurements

The deposited material from each individual growth run was processed into working devices with a back contact array of six Au circular contacts 0.03 cm^2 in area. J-V measurements were carried out under test conditions of 100 mWcm^{-2} from four 60 W halogen lamps. The J-V characteristics of each Au back contact is measured yielding values for conversion efficiency (η), fill factor (FF), short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}) and the best parameters for each device are shown in table 5.3.

Device ID	η (%)	FF (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)
SGEN6	0.04	24	1.50	0.13
SGEN7	0.10	52	0.60	0.32
SGEN8	0.03	40	0.34	0.23
SGEN9	0.03	50	0.20	0.26
SGEN10	0.03	51	0.25	0.26
SGEN11	0.03	51	0.20	0.27
SGEN12	3.70	47	15.00	0.53
SGEN13	0.07	54	0.40	0.31
SGEN14	0.05	53	0.30	0.30
SGEN15	2.70	44	11.30	0.54
SGEN16	0.05	52	0.28	0.35
SGEN17	0.03	52	0.19	0.30

Table 5.3 Summary of the best J-V results of each device structure from the first matrix.

SIMS depth profiles

SIMS depth profiles of three device structures from the first matrix shown in figure 5.1 were carried out to establish the level of impurities (Na, H and O), dopants (As and Cl) and the affects of the anneal treatment. Arsenic and hydrogen levels have been quantified by reference to implanted CdTe material. The chlorine and sodium levels have been estimated by cross correlation with previously analysed films. Oxygen and

the matrix species; cadmium, tellurium and sulphur are represented on a raw arbitrary count scale. SGEN6 confirmed the background level sensitivity for each of the studied species as there was no doping or anneal treatment in this device structure:

- Arsenic 2×10^{16} atoms cm^{-3}
- Sodium 1×10^{16} atoms cm^{-3}
- Chlorine 3×10^{17} atoms cm^{-3}
- Hydrogen 3×10^{18} atoms cm^{-3}
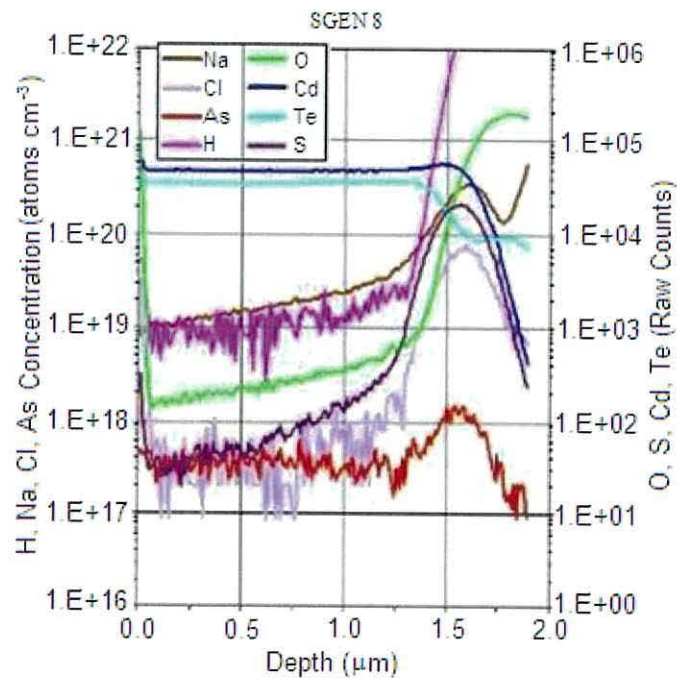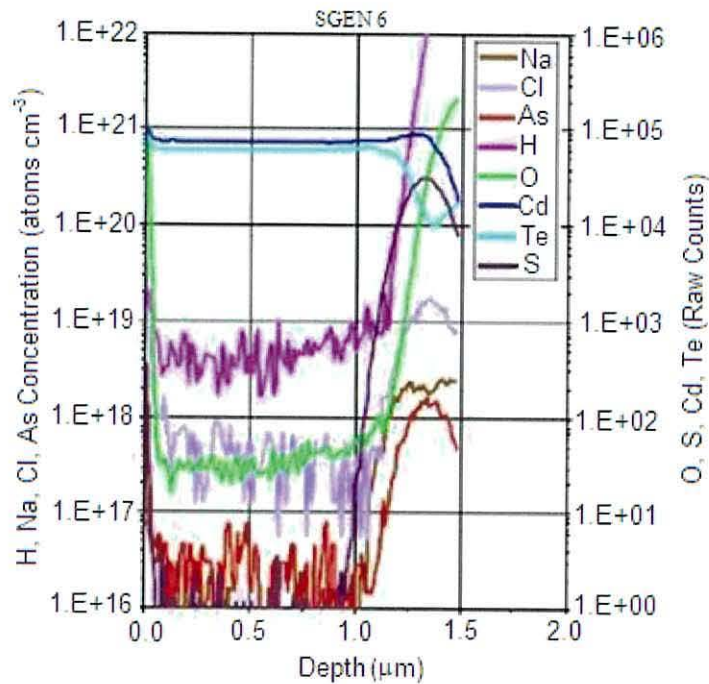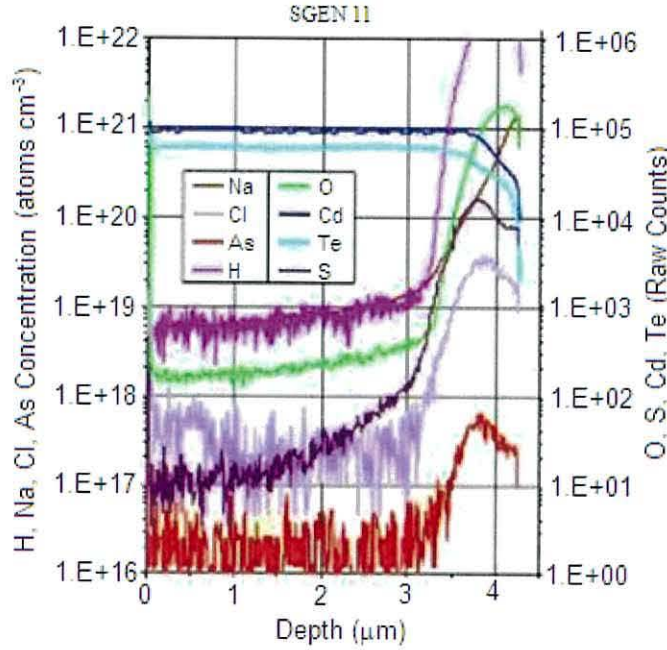
Fig 5.1 SIMS depth profiles of the device structures SGEN6, SGEN8 and SGEN11 from the first Taguchi matrix. The raw counts indicate values not compared to implanted reference material.

The 4×10^{-7} atm partial pressure of TDMAAs correlates to an arsenic concentration in the device structure of 4×10^{17} atoms cm^{-3}. The SIMS analysis of the annealed device structures show steeper rises in the hydrogen (pink), oxygen (green) and sodium (brown) traces from 0.5 μm to 1.5 μm. This is indicative of diffusion of impurities through the absorber layer to the CdTe/CdS interface. This affect is most prominent in SGEN8 with the thinner 2 μm CdTe layer and the higher temperature anneal of 500 °C. The SIMS profile of SGEN11 shows less evidence of impurity diffusion which can be attributed to a thicker absorber layer (4 μm). The overall level of H_2 in SGEN8 has increased due to annealing. Hydrogen segregating at the grain boundaries is also increased with annealing. Therefore it is probable that hydrogen maybe reacting with arsenic.

Scanning electron microscopy

SEM micrographs of two device structures with different TDMAAs partial pressures and anneal treatments are presented in figure 5.2. The unannealed device structure has a rough surface morphology with small grains of up to 1 μm in size.
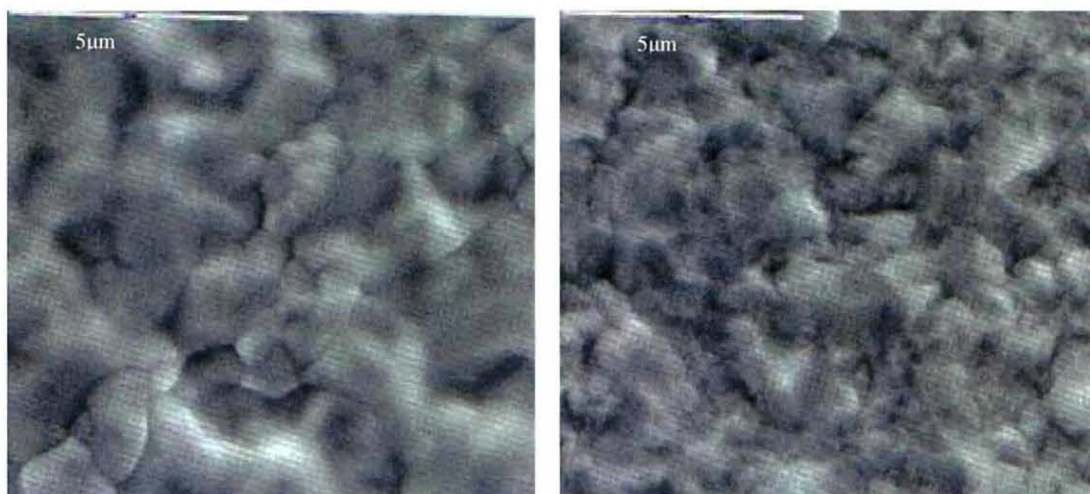
Fig 5.2 SEM micrographs of SGEN 11 annealed undoped device structure and SGEN 12 unannealed arsenic doped device structure.

The surface morphology of the annealed device structure (SGEN11) has more defined grain boundaries and larger grains of ~ 2 µm indicating that the anneal step promotes grain growth. The grain enlargement most likely occurs via Oswald ripening in which the smaller grains are consumed by large neighbouring grains.

A measurable thickness of the $CdCl_2$ layer was not obtained indicating that although the CdTe surface was exposed to n-Hexylchloride and DMCd the desired $CdCl_2$ layer did not form.

5.9.2 Analysis of the first matrix

The Taguchi results for device efficiency ($T_{i(\eta)}$), excluding the interaction columns, are summarised below in table 5.4. The best J-V results of each device structure were used to generate the matrix results as previously outlined in section 5.4. The approach adopted in analysing this matrix of experiments was to focus on the step changes, which have the largest positive or negative affects on the overall device efficiency. The control parameters with step changes in device efficiency are highlighted showing that three of the investigated growth parameters have a significant affect on the device performance under the selected experimental conditions.

	CdS thickness	CdTe thickness	As doping (p.p*)	Cl doping	CdCl$_2$ layer	30 mins anneal
	1:240nm	1:4µm	1:4 × 10^{-7} atm	1:2sccm	1:10nm	1:500°C
	-1:120nm	-1:2µm	-1:None	-1:None	-1:None	-1:350°C
$T_{i(\eta)}$	-1.06	6.28	6.20	0.86	1.2	-6.32

Table 5.4 The results for device efficiency, $T_{i(\eta)}$, of the first Taguchi matrix of experiments.

The signs dictate whether the initial level (1) or the new level (-1) is most beneficial to the main function. The CdTe thickness ($T_{i(\eta)}$ = 6.28) and arsenic doping ($T_{i(\eta)}$ = 6.20) control factors both have large positive results indicating that the original levels of CdTe 4 µm and arsenic partial pressure 4×10^{-7} atm are most beneficial for the device efficiency. The 30 minute anneal control factor has a large negative result ($T_{i(\eta)}$ = -6.32) indicating that the lower anneal temperature is most beneficial for conversion efficiency.

The analysis of the experimental matrices was extended to include the other device parameters; FF, J_{sc} and V_{oc} with characterisation. Utilising the results of the remaining device parameters can provide a more diagnostic investigation of why a control factor has a particular affect on the overall conversion efficiency. The Taguchi results for FF, J_{sc} and V_{oc} are summarised in table 5.5, excluding the interaction columns.

The Taguchi results of the remaining device parameters can give an indication of why the conversion efficiency alters with the chosen control factor levels. For example arsenic doping the CdTe has a positive affect on efficiency ($T_{i(\eta)}$ = 6.20) and can be explained by a large positive affect on J_{sc} ($T_{i(jsc)}$ = 24.02). This highlights that arsenic in CdTe has a beneficial affect on the photocurrent producing two implications:

1. The diffusion length of the charge carriers may be increased
2. More charge carriers are reaching the junction

The majority of impurities in polycrystalline material will segregate to native defects in the material such as grain boundaries. The grain boundaries have an open and less ordered atomic structure thereby allowing easier atomic diffusion along the grain boundaries than in the bulk material. It is possible that the arsenic in the CdTe may be passivating some of the grain boundaries reducing the number of recombination sites at crystal defects within the bulk material. This combination of factors can in turn lead to

an increase in the carrier lifetime making it more likely that the charge carrier reach the junction before recombination can occur.

	CdS thickness	CdTe thickness	As doping (p.p*)	Cl doping	CdCl$_2$ layer	30 mins anneal
	1:240nm -1:120nm	1:4µm -1:2µm	1:4 × 10^{-7} atm -1:None	1:2sccm -1:None	1:10nm -1:None	1:500°C -1:350°C
$T_{i(FF)}$	-60.00	124.00	-98.00	-86.00	132.00	150.00
$T_{i(Jsc)}$	-5.62	24.28	24.02	1.68	-26.80	3.50
$T_{i(Voc)}$	-0.20	1.22	-0.06	-0.46	0.06	0.88

Table 5.5 The Taguchi results for the other device parameters: fill factor, short-circuit current and open-circuit voltage.

The results of the four interaction control factors; produced large negative affects on device performance. The Taguchi results of the interaction columns AE, CE, DE and EF were -6.56, -6.60, -6.64 and -6.50, respectively, highlighting that there are significant interactions between the selected control factors in this matrix. The following matrices were designed to reduce the number of interaction present in order to maintain the orthogonality of the methodology.

5.9.3 Optimum factor levels and verification

The results of this experimental matrix for device efficiency produce the following optimum growth conditions for the investigated control factors and levels:

- Thicker CdTe absorber layer (4 µm),
- Arsenic doping in CdTe (4×10^{-7} atm),
- CdS thickness (120 nm),
- Lower temperature 30 minute anneal (350 °C),
- CdTe surface exposure to n-HexCl (10 min).

The verification experiment is a growth run with the best combination of growth conditions from the experimental matrix, but might not be one of the investigated combinations. The verification experiment for the first matrix is the first growth experiment of the next experimental matrix which also acts as the start point for the second matrix of experiments. The anneal conditions in the verification experiment was

at the correct temperature of 350 °C but the length of anneal step was shorter (10 minutes) to reduce the diffusion of impurities through the layers. The device efficiency from the verification experiment $\eta = 1.84 \pm 0.73$ % is in agreement with the best device from the matrix of $\eta = 2.25 \pm 1.47$ %, within experimental error.

5.10   Second matrix

The second experimental matrix shown in table 5.6 was designed to build upon the beneficial affects of arsenic doping and $CdCl_2$ exposure time. The $CdCl_2$ conditions did not yield a layer growth despite a small positive impact on the device efficiency ($T_{i(\eta)} = 1.2$). Alternative exposure times were therefore included in the design of this matrix to obtain a $CdCl_2$ layer. The rapid diffusion of impurities through the device structures, present in the first matrix was also selected for further investigation. To monitor the affect of impurities diffusing from the soda lime glass substrates from Merck, additional alumino-silicate glass substrates from Delta Technologies were also investigated.

Run ID	As doing (p.p*)	CdTe II:VI	A+B	Substrate	CdCl$_2$ exposure	10 min anneal	F+E
	1: 6×10^{-8}atm -1:4×10^{-7}atm	1:1.75 -1:1		1:Delta -1:Merck	1:45min -1:10min	1: 500°C -1: 350°C	
SGEN25	-1	-1	-1	-1	-1	-1	-1
SGEN28	-1	-1	-1	1	1	1	1
SGEN27	-1	1	1	-1	-1	1	1
SGEN29	-1	1	1	1	1	-1	-1
SGEN30	1	-1	1	-1	1	-1	1
SGEN31	1	-1	1	1	-1	1	-1
SGEN32	1	1	-1	-1	-1	1	-1
SGEN33	1	1	-1	1	1	-1	1

Table 5.6 The second Taguchi matrix of experiments showing five control factors and two interaction columns.

The first growth experiment of this matrix is designed to act as the verification experiment for the first matrix which used the parameters from SGEN15 as the start point for the second matrix. The number of interaction columns was reduced to two in order to reduce the number of growth runs in the matrix, but still facilitate monitoring of inherent interactions. The CdTe II:VI was also investigated to establish if there is a correlation with arsenic incorporation in the absorber layer.

5.10.1 Characterisation of the second matrix

J-V measurements

The deposited material from each individual growth run was processed into working devices with a back contact array of ten gold circular contacts 0.02 cm^2 in area. During the back contacting of the device structures it was noted that the contacts were darker in colouration. In the past this has been attributed to increased surface roughness. J-V measurements were carried out at a constant power of 100 mW cm^{-2} across the area of a device achieved by four 60 W halogen lamps. The J-V characteristics of each gold back contact is measured yielding values for conversion efficiency (η), fill factor (FF), short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}) and the best parameters for each device are shown in table 5.7.

Device ID	η (%)	FF (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)
SGEN25	2.28	47	8.89	0.54
SGEN28	0.15	59	0.70	0.36
SGEN27	0.13	57	0.60	0.38
SGEN29	3.14	38	18.48	0.45
SGEN30	2.75	51	9.69	0.55
SGEN31	0.06	55	0.35	0.30
SGEN32	0.03	53	0.19	0.31
SGEN33	2.57	48	9.79	0.54

Table 5.7 Summary of the best J-V results of each device structure from the second matrix.

There is a large range of Jsc values and this improvement in photocurrent correlates with an increase in conversion efficiency. SGEN 29 has the best efficiency of the studied device structures with an average efficiency of $\eta = 2.79 \pm 0.33$ %.

SIMS depth profiles

SIMS depth profiles of two of the device structures with different TDMAAs partial pressures, CdTe II:VI and substrate are shown in figure 5.3. Both device structures have uniform arsenic concentrations up to the CdTe/CdS interface. The TDMAAs partial pressures of 4×10^{-7} atm (SGEN29) and 6×10^{-7} atm (SGEN30) produce arsenic concentrations in the CdTe of 3.4×10^{18} atoms cm^{-3} and 3×10^{17} atoms cm^{-3} respectively. The increase in arsenic concentration in SGEN 29 is probably a result of the CdTe II:VI ratio, with a cadmium rich layer (II:VI = 1.75) aiding arsenic incorporation. Both

devices had the same CdCl$_2$ layer thickness of 100nm, but the SIMS analysis shows a significant difference in the Cl trace. In SGEN 29 the Cl diffuses during the growth of the CdCl$_2$ layer which is shown by a small well in the Cl signal. This feature is not present in SGEN30 and again is most likely due to the difference in CdTe II:VI.
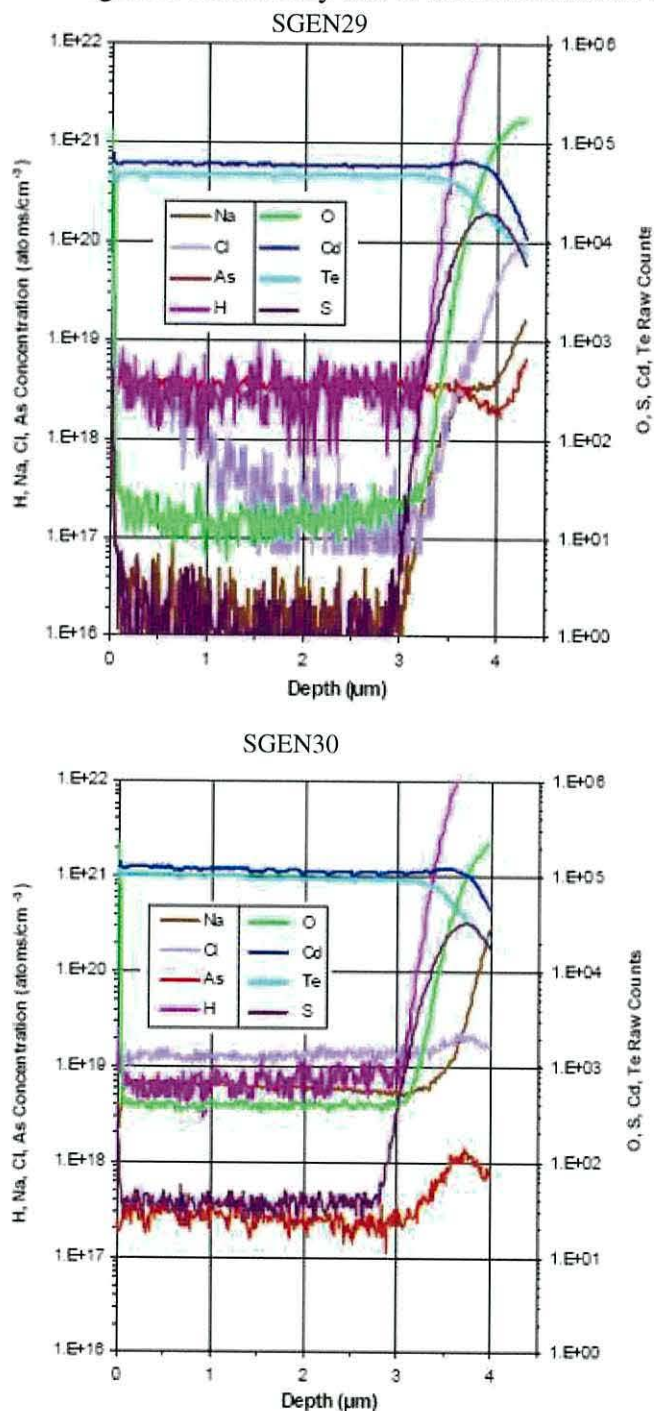

Fig 5.3 SIMS depth profiles of the device structures SGEN29 and SGEN30 from the second Taguchi matrix of experiments. The raw counts indicate values not compared to implanted reference material.

The impurity signals in SGEN30 are much greater than SGEN29 despite both devices having the same anneal conditions (350 °C for 10 minutes). Abnormally high levels of impurity or dopant concentrations can sometimes be due to surface or porosity artefacts such as holes or particulates. As both samples were prepared by the same method it is unlikely that these high levels are the result of such artefacts. The hydrogen signal is the only impurity which is comparable between the devices probably as this is an environmental impurity from the carrier gas. This indicates that the Na and O impurities are diffusing from the soda lime glass substrate. The alternate alumino-silicate substrate (SGEN29) may explain the significantly lower levels of oxygen (1.5×10^{17} atoms cm^{-3}) and the lack of sodium diffusion.

Scanning Electron Microscopy

SEM micrographs of two device structures with different anneal temperatures are presented in figure 5.4. Both device structures have a rough surface morphology consistent with polycrystalline CdTe.
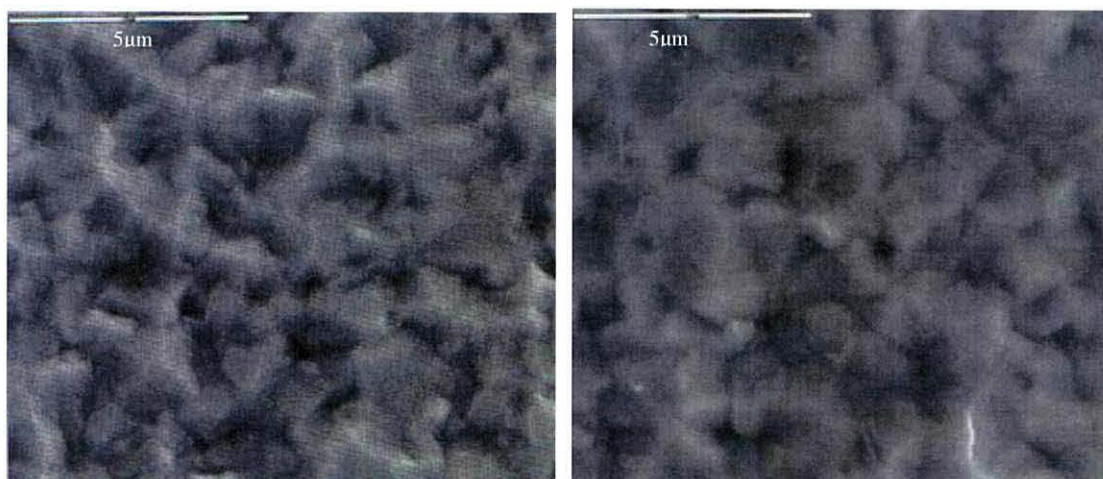
Fig 5.4 SEM micrographs of two device structures with different anneal temperatures; 350°C (SGEN29) and 500°C (SGEN32), respectively.

The lower temperature annealed device (350 °C) has grain size up to 1 μm with few defined grain boundaries. The higher temperature annealed device (500 °C) has a grain size of ~ 2 μm and grain boundaries are more visible across the surface. Despite the advantage of grain growth with the 500 °C anneal this device had a poor average conversion efficiency of η = 0.03 ± 0.01 % due to the rapid diffusion of impurities from the Merck substrate.

5.10.2 Analysis of the second matrix

The Taguchi results for device efficiency ($T_{i(\eta)}$) of the second matrix are presented below in table 5.8. The step change method of analysis used for the first matrix was adopted here. The control parameters with step changes in device efficiency are highlighted in table 5.8. The anneal control factor has the largest impact on device efficiency. The Taguchi result of $T_{i(\eta)}$ = -10.37 indicates a significant benefit to solar conversion efficiency with the more gentle anneal of 350 ^{o}C for 10 minutes. The other control factors with an impact on device efficiency are $CdCl_2$ exposure time, the A+B interaction, substrate and CdTe II:VI.

	As doing (p.p*)	CdTe II:VI	A+B	Substrate	$CdCl_2$ exposure	10 min anneal	F+E
	1: 6×10^{-8}atm -1:4×10^{-7}atm	1:1.75 -1:1		1:Delta -1:Merck	1:45min -1:10min	1: 500°C -1: 350°C	
$T_{i(\eta)}$	-0.29	0.63	1.05	0.73	1.03	-10.37	0.09

Table 5.8 The Taguchi results ($T_{i(\eta)}$) for efficiency in the second Taguchi matrix.

The interaction control factor (A+B) result of $T_{i(\eta)}$ = 1.05 highlights that there is a positive interaction between the control factors with a small benefit to device efficiency. This benefit most likely arises from the increased arsenic incorporation in the bulk in Cd rich layers aiding passivation of the grain boundaries. The $CdCl_2$ exposure time control factor indicates a small benefit to efficiency with the longer exposure time of 45 minutes. The Taguchi results of the remaining device parameters are presented in table 5.9.

	As doing (p.p*)	CdTe II:VI	A+B	Substrate	$CdCl_2$ exposure	10 min anneal	F+E
	1: 6×10^{-8}atm -1:4×10^{-7}atm	1:1.75 -1:1		1:Delta -1:Merck	1:45min -1:10min	1: 500°C -1: 350°C	
$T_{i(FF)}$	5.75	-16.25	-6.25	-8.25	-6.25	39.75	21.75
$T_{i(Jsc)}$	-8.65	9.43	9.55	9.95	9.43	-45.01	-7.13
$T_{i(Voc)}$	-0.03	-0.07	-0.07	-0.13	-0.09	-0.73	0.23

Table 5.9 The Taguchi results for the other device parameters: fill factor, short-circuit current and open-circuit voltage.

The post growth anneal destroys the cells photo response ($T_{i(jsc)}$ = -45.01) even with the shorter anneal time of 10 minutes. This highlights that the destructive process is rapid. The II:VI has a small benefit to device efficiency with Cd rich conditions, with a positive correlation with high arsenic concentration. The alumino-silicate substrate has a beneficial impact on the short-circuit current and dramatically reduces the diffusion of sodium and the oxygen level in the device structures. Due to the complex nature of interactions, incorporation of hydrogen and the rapid diffusion of impurities with a short 10 minute anneal, this step was omitted from the next matrix to allow independent investigation of the affects of post growth anneals on polycrystalline CdTe/CdS devices.

5.10.3 Optimum factor levels and verification

SGEN29 produces the best device efficiency in this matrix of η = 2.79 ± 0.33 %. The new standard growth conditions resulting from this experimental matrix are:

- Alumino-silicate substrate (Delta)
- Cadmium rich CdTe
- As concentration 1×10^{18} atoms cm^{-3}
- 100 nm CdCl$_2$ layer
- 240 nm CdS
- 4 μm CdTe

The average efficiency of the verification experiment (SGEN55) supports the optimum conditions identified producing a device efficiency of η = 4.26 ± 0.32 %.

Despite investigating seven control factors only three had a significant affect on the main function, with two having a marginal improvement. SIMS analysis highlighted that substrate composition and CdTe II:VI are significant growth parameters under the investigated levels, but this is not obvious from the Taguchi results alone. This highlights that the method of analysis used for this matrix, concentrating on large step changes to the device efficiency, can mask the effects of some of the control parameters, confirming that characterisation needs to be utilised in conjunction with the statistical methodology to ensure the affects of the growth conditions are observed. A criterion to establish a threshold value to identify significant Taguchi results, outlined in section 5.6 was applied to all future matrices to determine which parameters warrant further investigation. The general convention of the Taguchi matrix methodology relies on a

low noise system and specifies that Taguchi results of zero have a negligible affect on the main function. In reality this approach is not practical as noise is always present.

5.11   Third matrix

A L_8 matrix of experiments was designed to investigate various deposition parameters of CdTe and CdS and is presented below in table 5.10. The CdCl$_2$ exposure control factor had the largest positive affect on device efficiency in the second matrix, but a measurable CdCl$_2$ layer thickness could not be obtained using the n-HexCl precursor. This process was subsequently removed from the matrix experiments and investigated separately with alternate chlorine precursors. Omitting the CdCl$_2$ control factor enabled the experiments to concentrate on the arsenic doping of CdTe.

Run ID	CdS temperature	CdS II:VI	A+B	CdS thickness	CdTe thickness	CdTe temperature	As doing (p.p*)
	1:330°C -1:300°C	1:1 -1:0.76		1:350nm -1:240nm	1:6μm -1:4μm	1: 390°C -1: 350°C	1: 7×10^{-7}atm -1:4×10^{-7}atm
SGEN55	-1	-1	-1	-1	-1	-1	-1
SGEN56	-1	-1	-1	1	1	1	1
SGEN65	-1	1	1	-1	-1	1	1
SGEN58	-1	1	1	1	1	-1	-1
SGEN59	1	-1	1	-1	1	-1	1
SGEN60	1	-1	1	1	-1	1	-1
SGEN61	1	1	-1	-1	-1	1	-1
SGEN62	1	1	-1	1	1	-1	1

Table 5.10 The third Taguchi matrix of experiments with six control factors and one interaction column.

From this point onwards the soda lime glass substrate form Merck is replaced by the alumino-silicate glass substrates from Delta Technologies Limited. The CdTe II:VI proved a significant parameter in the second matrix and therefore the CdS II:VI was selected as a control factor for this matrix. Post growth annealing to improve efficiency of the devices has not been used in these experiments in order to avoid masking effects of deposition parameters.

5.11.1 Analysis of the third matrix

The results of the third matrix for device efficiency are presented below in table 5.11. The criteria outlined in section 5.6 was employed to analyse this matrix and deemed the

Taguchi results for CdS deposition temperature and CdS II:VI as negligible. The significant Taguchi results on device efficiency are highlighted below in table 5.11.

	CdS temperature	CdS II:VI	A+B	CdS thickness	CdTe thickness	CdTe temperature	As doing (p.p*)
	1:330°C -1:300°C	1:1 -1:0.76		1:350nm -1:240nm	1:6µm -1:4µm	1: 390°C -1: 350°C	1: 7×10⁻⁷atm -1:4×10⁻⁷atm
$T_{i(\eta)}$	-0.62	0.1	1.22	-1.54	-2.54	5.06	-4.62

Table 5.11 The Taguchi results ($T_{i(\eta)}$) for efficiency in the third Taguchi matrix.

The most significant result is a higher deposition temperature of 390 °C for CdTe with a Taguchi result of $T_{i(\eta)} = 5.06$. The two most significant parameters CdTe deposition temperature and arsenic doping are examined in more detail and an empirical model for the incorporation of arsenic into CdTe and its effect on the layer are discussed in chapter 6.

The CdTe and CdS thickness control parameters both produced a negative Taguchi result for device efficiency, indicating a preference for the original (thinner) settings of 4 µm and 240 nm, respectively. Using the other device parameter results shown in table 5.12 a more diagnostic evaluation of why the efficiency has reduced can be undertaken.

	CdS temperature	CdS II:VI	A+B	CdS thickness	CdTe thickness	CdTe temperature	As doing (p.p*)
	1:330°C -1:300°C	1:1 -1:0.76		1:350nm -1:240nm	1:6µm -1:4µm	1: 390°C -1: 350°C	1: 7×10⁻⁷atm -1:4×10⁻⁷atm
$T_{i(FF)}$	17.05	-1.21	0.61	8.71	-14.75	19.75	-17.74
$T_{i(Jsc)}$	-3.8	-1.98	3.02	-6.76	-1.72	6.62	-17.74
$T_{i(Voc)}$	-0.22	0.08	0.04	-0.12	-0.08	0.18	-0.3

Table 5.12 The Taguchi results from the third matrix for the other device parameters: fill factor, short-circuit current and open-circuit voltage.

The J_{sc} was the dominant factor for CdS thickness parameter and decreased with increasing thickness. Spectral response is under 20 % below 500 nm corresponding to the bandgap of CdS indicating that the drop in efficiency is probably caused by a poor response at the blue end of the spectrum, allowing less photons to pass through the

thicker CdS window layer. The FF is the dominant parameter for the CdTe thickness and decreases with increasing thickness. This is an unexpected result as the FF tends to increase with CdTe thickness due to a reduction in pin-holes. These results produce two implications:

1. pin-holes are not a dominant issue in the CdTe layer
2. There is an alternate factor dominating the FF

Fill factor losses are usually attributed to series resistance or leakage currents at the edges of the cell. The series resistance is the most probable dominating factor in reducing the fill factor as it is dependent on the bulk resistance of the semiconductor and therefore a thicker absorber layer is more likely to have a higher series resistance. The average series resistance of the 4 micron CdTe devices is 10 Ω and the average series resistance of the 6 micron CdTe devices is 9 Ω. This indicates that series resistance is not the dominant factor for FF losses. It is possible that with thicker layers, roughness increases and lateral non-uniformity dominates. Igalson *et al* attributed losses in FF to a p^+ layer in the absorber close to the interface for CIGS cells [6], indicating that FF loss is dependent on the amount of charge accumulated in the absorber close to the interface. This explanation may extend to CdTe absorber solar cells with arsenic doping, but further work is needed to explore this hypothesis.

5.11.2   Characterisation of the third matrix

J-V measurements

Current-voltage (J-V) characterisation of the devices was undertaken at a constant power over the area of the PV test array (100 mW cm^{-2}) and was achieved using a light source consisting of 4×60 W halogen lamps. While processing this material the back contacts became considerably darker than previously observed and produced poor devices with high series and shunt resistance. The darkening of the back contacts was attributed to carbon contamination from the grease within the evaporator bell jar.

Run ID	η (%)	FF (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)
SGEN55	4.52	36.00	24.97	0.50
SGEN56	3.61	42.63	20.07	0.42
SGEN65	4.96	43.99	22.45	0.50
SGEN58	3.83	34.34	23.11	0.48
SGEN59	2.88	39.93	19.91	0.36
SGEN60	5.55	47.53	24.74	0.47
SGEN61	5.02	41.21	24.75	0.49
SGEN62	2.85	45.34	17.40	0.36

Table 5.13 The best device parameters from the J-V characterisation of the third matrix.

After a thorough clean with acetone additional contacts were added down the centre of the deposited material to allow re-characterisation without the need to process additional material. The new contact array consists of four circular contacts 0.02 cm^2 in area and produced bright gold contacts. This contact array was re-characterised using J-V measurements and the resulting values presented in table 5.13 were utilised in the analysis of this matrix.

Scanning Electron Microscopy

The most relevant parameter tested was CdTe growth temperature, $T_i = 5.06$. This favours the higher temperature setting of 390 ^{o}C. Figure 5.5 shows SEM micrographs of two layers, one at each CdTe deposition temperature. There is clear evidence of CdTe grain enlargement from 1 μm to 3 μm at the higher temperature. Grain enlargement is most likely occurring via an Oswald ripening type mechanism, where small grains do not grow as fast as their larger neighbours, forming fewer and larger grains near the surface, as viewed in figure 5.5.
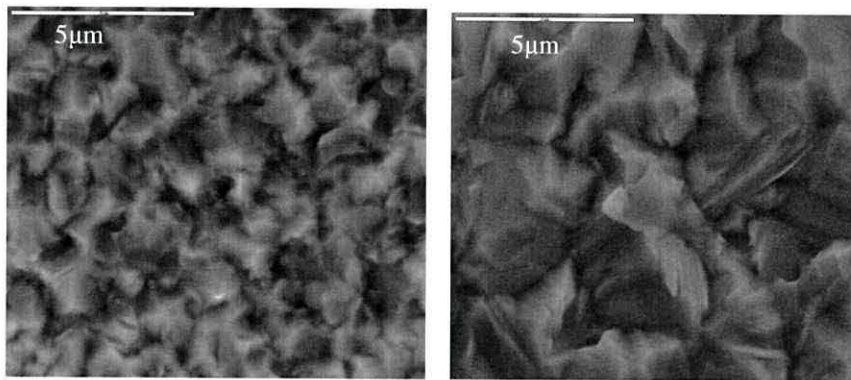

Fig.5.5 SEM micrographs showing the difference in CdTe grain size with CdTe deposition temperatures of 350 ^{o}C or 390 ^{o}C, respectively.

This results in fewer small grains overall. Enlarged grains can be linked to improved device performance as many of the optical and electrical properties of polycrystalline CdTe/CdS material are determined by the properties of the grain boundaries, which can act as rapid carrier recombination sites.

SIMS depth profiles

The next significant parameter resulting from the matrix analysis was arsenic doping of the CdTe layer ($T_i = -4.62$). The negative sign indicates that the original parameter setting of a partial pressure of 4×10^{-7} atm was most beneficial. SIMS depth profiles of two growth layers were made to determine the concentrations of arsenic in the CdTe layers. Two samples were selected, one at each of the arsenic partial pressure settings and are presented in figure 5.6.
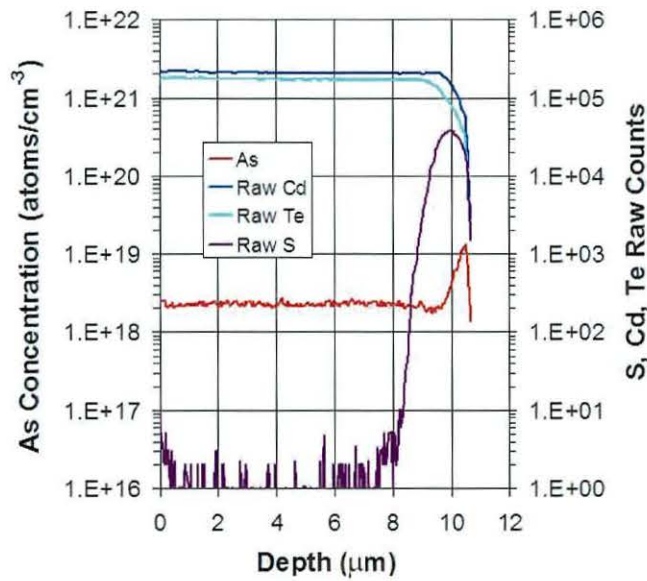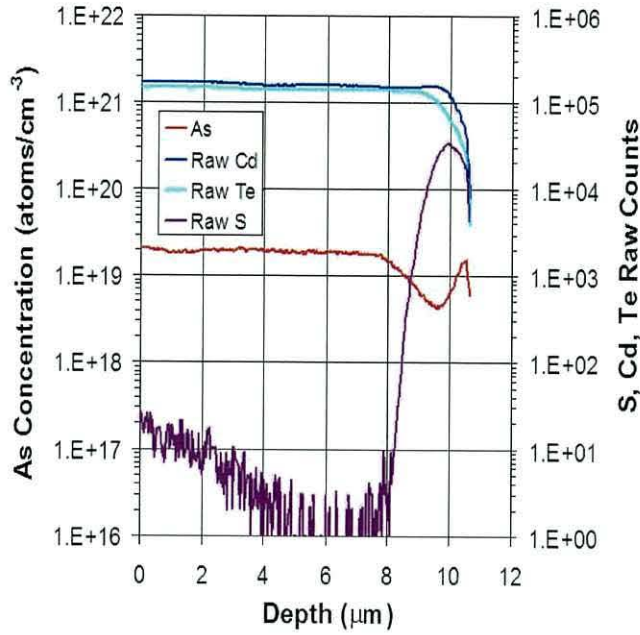
Fig.5.6 SIMS depth profiles showing the arsenic concentration within the device structure for the different arsenic partial pressures of a) 4×10^{-7} atm. and b) 8×10^{-7} atm.

The arsenic dopant level was calibrated using implanted reference samples of arsenic in CdTe layers. The SIMS depth profiles show the presence of a uniform concentration of arsenic in the layers up to the interface with CdS. The partial pressures of 4×10^{-7} atm and 7×10^{-7} atm resulted in arsenic concentrations within the CdTe layers of 2.5×10^{18} atoms cm^{-3} and 2×10^{19} atoms cm^{-3}, respectively. It appears from these results that, although a high arsenic concentration in the CdTe is needed to improve cell efficiency, there is an optimum concentration, above which the efficiency will reduce.

5.11.3 Optimum factor levels and verification

As detailed earlier, each Taguchi matrix provides a new set of optimum conditions based on the investigated parameter settings. These predicted optimum conditions might not necessarily be one of the investigated combinations. The optimum control factor levels of the L_8 matrix are summarised below. The CdTe growth temperature of 390 °C produced the largest beneficial result on device efficiency, attributed to grain growth from 1 μm to 3 μm via an Oswald ripening type mechanism. The next significant parameter was attributed to a lower arsenic partial pressure of 4×10^{-7} atm yielding an arsenic concentration in the layer of 2.5×10^{18} atoms cm^{-3}. An arsenic concentration of 2×10^{19} atoms cm^{-3} in the CdTe was obtained, but did not yield the same beneficial effects on device efficiency as the lower arsenic concentration of 2.5×10^{18} atoms cm^{-3}

indicating that the benefit to device efficiency from arsenic incorporation is a limited process. The thickness of both the CdTe and CdS parameters preferred the thinner settings of 4 μm and 240 nm, respectively. These Taguchi results were deemed significant by the criterion, but were considerably smaller effects than the CdTe growth temperature and the arsenic partial pressure. The most favourable settings from the third matrix are;

- CdS deposition temperature 300 °C.
- CdS II:VI of 1.
- 240 nm CdS.
- 4 μm CdTe.
- CdTe deposition temperature 390 °C.
- Arsenic concentration 2.5×10^{18} atoms cm^{-3}.

The predicted parameter levels do not correspond to any of the selected combinations in the matrix. A verification growth was performed to check the predicted performance. The average device results across a 10 gold dot contact array were: η = 4.63 %, FF = 42.94 %, J_{sc} = 20.91 mA cm^{-2} and V_{oc} = 0.51 V. The efficiency of the verification device was lower than the best device from the matrix, however only by 0.77, showing that the predicted optimum conditions for the parameters investigated were correct within experimental error.

5.11.4   Third matrix summary

A L_8 matrix of experiments was designed to determine which growth variables have a significant effect on CdTe/CdS device parameters and therefore warrant further investigation. This study was performed in isolation from the CdCl$_2$ treatment. A criterion for determining a threshold value for significant changes was successfully applied to the matrix results. The two most relevant parameters were CdTe growth temperature and arsenic doping of the CdTe layer. SEM micrographs verify that grain growth from 1 μm to 3 μm occurred when CdTe was grown at the higher temperature of 390 °C. SIMS depth profiling revealed that the arsenic concentration in the growth layers was an order of magnitude greater with the higher partial pressure of 8×10^{-7} atm compared to the lower setting of 4×10^{-7} atm. The lower arsenic partial pressure was preferred, indicating an optimum arsenic concentration above which device efficiency reduces. A paper on this work entitled "The application of a statistical methodology to investigate deposition parameters in CdTe/CdS solar cells grown by MOCVD" was

accepted for publication in the Journal of materials science: materials in electronics and is presented in appendix B [3].

5.12 Fourth matrix

The fourth Taguchi matrix was designed to investigate the CdS window layer in more detail. The L_8 matrix of experiments is presented below in table 5.14. This matrix investigates a cadmium rich window layer and a variety of heat and chemical treatments.

Run ID	CdS temperature	CdS II:VI	A+B	CdS thickness	CdS anneal 450°C N$_2$	DiPTe flow 390°C	Cl doping CdS
	1: 315°C -1:300°C	1:1.5 -1:1		1:180nm -1:240nm	1:5mins -1:None	1:10mins -1:None	1:10sccm -1:None
SGEN65	-1	-1	-1	-1	-1	-1	-1
SGEN73	-1	-1	-1	1	1	1	1
SGEN67	-1	1	1	-1	-1	1	1
SGEN68	-1	1	1	1	1	-1	-1
SGEN69	1	-1	1	-1	1	-1	1
SGEN70	1	-1	1	1	-1	1	-1
SGEN71	1	1	-1	-1	-1	1	-1
SGEN72	1	1	-1	1	1	-1	1

Table 5.14 The fourth Taguchi matrix of experiments with six control factors and one interaction column.

Previous SIMS analysis of annealed device structures showed the incorporation of hydrogen into the absorber layer most likely from the carrier gas during the growth runs. Therefore annealing the CdS layer was designed to be carried out under a nitrogen atmosphere.

5.12.1 Characterisation of the fourth matrix

J-V measurements

The deposited material from each individual growth run was processed into working devices with a back contact array of ten gold circular contacts 0.025 cm^2 in area. The J-V characteristics of each back contact is measured yielding values for conversion efficiency (η), fill factor (FF), short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}) and the best parameters for each device are shown in table 5.15. Current-voltage (J-V) characterisation of the devices was undertaken at a constant power over the area of the

PV test array (100 mW cm^{-2}) and was achieved using a light source consisting of 4×60 W halogen lamps. There is a small variance in device parameters across this L$_8$ matrix, which may indicate little effect for the investigated control factors at the chosen levels. The best device efficiency resulting from this matrix was = 4.99 % (SGEN70).

Run ID	η (%)	FF (%)	J$_{sc}$ (mAcm^{-2})	V$_{oc}$ (V)
SGEN65	4.96	43.99	22.45	0.50
SGEN73	3.77	43.77	16.47	0.52
SGEN67	4.13	40.36	19.20	0.53
SGEN68	4.38	43.84	19.86	0.50
SGEN69	4.82	46.62	20.98	0.49
SGEN70	4.99	48.20	19.80	0.52
SGEN71	4.98	43.86	20.92	0.54
SGEN72	4.27	45.58	19.83	0.47

Table 5.15 The best device parameters of the device structures from the fourth experimental matrix.

SIMS depth profiles

SIMS depth profiles of SGEN65 and SGEN67 are shown in figure 5.7. These device structures have different CdS II:VI and Cl doping to monitor the effect on Cl incorporation and diffusion in the window layer. SGEN65 is considerably thicker than expected with an absorber thickness of approximately 8 μm. It was found that the thicker samples were processed from a different position on the susceptor highlighting a uniformity issue across the susceptor. Both device structures have a uniform arsenic concentration throughout the absorber layer in the range of 2×10^{18} - 7×10^{18} atoms cm^{-3}.
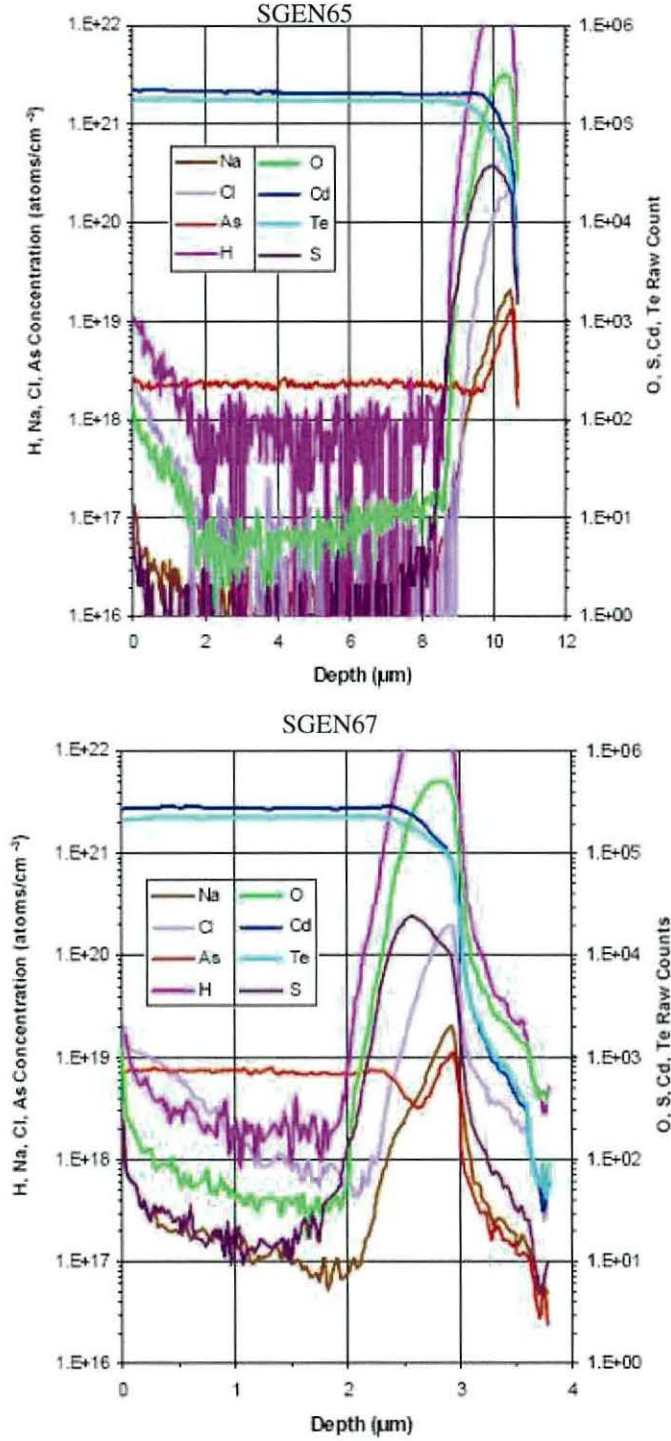
Fig 5.7 SIMS depth profiles of two device structures (SGEN 65) and (SGEN67) with different CdS II:VI and Cl doping levels.

The chlorine concentration in SGEN67 is 6×10^{17} atoms cm^{-3} which is above the background level indicating that Cl doping has been achieved. Despite the evidence for Cl doping in the CdS layer there is little impact on the device efficiencies.

5.12.2 Analysis of the fourth matrix

Using the criteria outlined in section 5.6 the threshold value for a significant result for this matrix is 0.68.

$$\Delta T_i = \sqrt{(0.24)^2 + (0.20)^2 + (0.27)^2 + (0.19)^2 + (0.18)^2 + (0.30)^2 + (0.30)^2 + (0.21)^2}$$
$$\Delta T_i = 0.68$$

The outcome of the Taguchi analysis is represented graphically in figure 5.8. The red band indicates the area of insignificant Taguchi results for device efficiency.
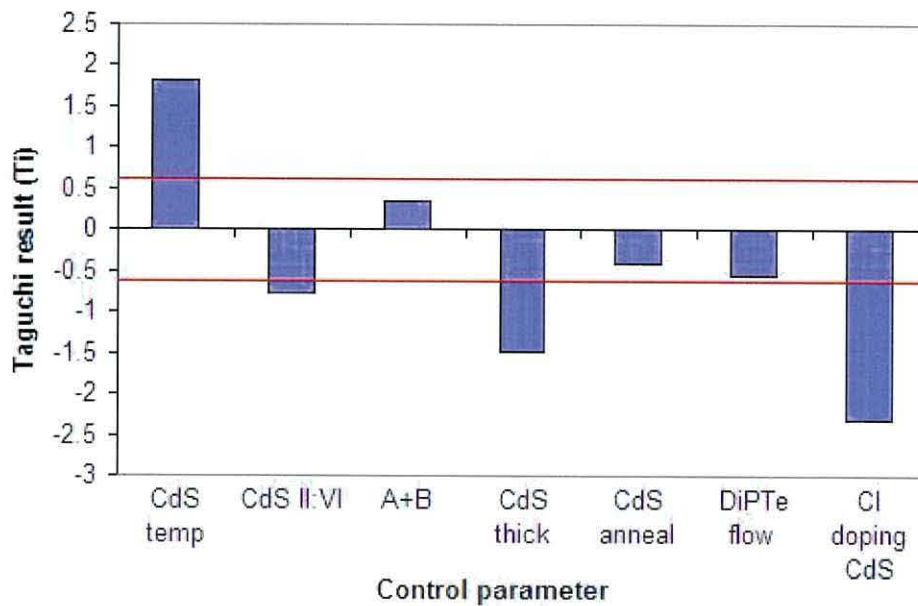

Fig 5.8 A plot of the deviation of the control parameter Taguchi results from the established threshold value 0.68.

Application of the criteria identified three of the control factors as negligible;

- The A+B interaction.
- Annealing the CdS for 5 minutes under a nitrogen atmosphere.
- DiPTe flow (Te layer).

The Taguchi results of each control factor are presented in table 5.16 with the significant values highlighted.

	CdS temperature	CdS II:VI	A+B	CdS thickness	CdS anneal 450°C N$_2$	DiPTe flow 390°C	Cl doping CdS
	1: 315°C	1:1.5		1:180nm	1:5mins	1:10mins	1:10sccm
	-1:300°C	-1:1		-1:240nm	-1:None	-1:None	-1:None
T$_{i(\eta)}$	1.82	-0.78	0.34	-1.48	-0.40	-0.56	-2.32

Table 5.16 The Taguchi results (T$_{i(\eta)}$) for efficiency in the fourth Taguchi matrix.

The Cl doping control factor has the largest impact on device efficiency with a Taguchi result of $T_{i(\eta)} = -2.32$ highlighting that no doping is most beneficial under the investigated levels. Hartley *et al* studied the effects of Cl diffusion from the CdS:Cl layer across the junction into the CdTe:As layer and found this to have a detrimental affect on the cell performance with considerable degradation of the photocurrent [7]. It is feasible that the CdS anneal parameter would aid Cl diffusion to the CdTe and cause rapid destruction of the photocurrent and device efficiency. As a result the CdS anneal step was omitted from the matrix experiments.

The higher CdS deposition temperature of 315 °C has a Taguchi result of $T_{i(\eta)} = 1.82$ indicating an advantage in moving to the higher deposition temperature. The original CdS thickness of 240 nm has a positive affect on the efficiency most likely due to a more ordered structure with fewer pinholes and reduced diffusion of Cl through to the CdTe. A thicker window layer is not ideal as photons need to pass through this layer before being absorbed by the CdTe layer. A resistive buffer layer such as SnO_2, In_2O_3 and Zn_2SnO_4 can be deposited between the conductive layer (ITO) and CdS and has been shown by Ferekides *et al* to improve solar cell performance by reducing the effects of shunting and pin holes for thinner window layers (80-100nm) [8, 9].

The Taguchi results for other device parameters are presented in table 5.17. The Cl doping has a negative affect on all of the device parameters. Increasing the CdS deposition temperature to 315 °C has a small benefit to the short-circuit current and fill factor.

	CdS temperature	CdS II:VI	A+B	CdS thickness	CdS anneal 450°C, N$_2$	DiPTe flow 390°C	Cl doping CdS
	1: 315°C -1:300°C	1:1.5 -1:1		1:180nm -1:240nm	1:5mins -1:None	1:10mins -1:None	1:10sccm -1:None
$T_{i(FF)}$	12.30	-8.94	1.82	6.56	-0.04	-3.84	-3.56
$T_{i(Jsc)}$	3.55	0.11	0.17	-7.59	-3.05	-6.73	-6.55
$T_{i(Voc)}$	-0.03	0.01	0.01	-0.05	0.03	0.15	-0.05

Table 5.17 The Taguchi results for the other device parameters: fill factor, short-circuit current and open-circuit voltage.

The thinner CdS layer (180 nm) has a positive affect on the fill factor but this does not out-weigh the negative impact these conditions have on: device efficiency, short-circuit current and open-circuit voltage.

5.12.3 Optimum factor levels and verification

The best device structure is SGEN 71 with an average efficiency of $\eta = 4.65 \pm 0.30$ %. The optimum growth parameter conditions resulting from the fourth Taguchi matrix are:

- CdS deposition temperature 315 °C.
- CdS II:VI of 1.
- 240 nm CdS.
- No anneal step, Te layer or Cl doping in the CdS.

The verification experiment (SGEN 75) produced a device efficiency of $\eta = 4.91 \pm 0.68$ %. This result highlights that although the growth conditions for SGEN 71 yielded the highest device efficiency, all of the device structures from this matrix produced similar device parameters. Therefore the best combination of growth conditions was ambiguous and indicates the importance of a verification experiment. As a result of these findings the optimum growth conditions from the previous matrix remained the start point for the fifth matrix.

5.13   Fifth matrix

The formation of a stable low resistance ohmic contact is one of the main challenges in producing high efficiency CdTe solar cells. To address this issue the fifth Taguchi matrix was designed to investigate the interface between the CdTe absorber layer and the back contact and the possible benefits of a buffer layer between the CdS and ITO. A high resistive buffer layer was investigated as Ferekides *et al* had shown high resistive layers between the CdS window layer and ITO can facilitate reduced window layer thickness without the losses to V_{oc} and FF [9]. ZnS was selected as the buffer layer as there is a common element between the buffer layer and CdS window layer, which may yield benefits from reduced lattice mismatch and aid sulphur diffusion into the CdTe possibly leading to a graded junction. An arsenic doped ZnTe (ZnTe:As) contact layer was investigated as Mondal *et al* had demonstrated that ZnTe:Cu deposited by electrochemical deposition produced an 8.7 % device efficiency [10]. The intention of this step is to create a p-ZnTe layer as a contact material to polycrystalline CdTe by the formation of a p-i-n junction.

The previous matrices all highlighted a TDMAAs partial pressure of 4×10^{-7} atm as the optimum. During this matrix higher TDMAAs partial pressures were investigated to establish whether there is a limit to the benefit to device efficiency from arsenic incorporation into CdTe. The L_8 matrix of experiments is presented in table 5.18.

Run ID	CdTe temperature	As doping (p.p*)	A+B	CdTe II:VI	Arsenic dip	ZnS buffer layer	ZnTe:As contact layer
	1:410°C -1:390°C	1:1×10⁻⁶ atm -1:7×10⁻⁷ atm		1:0.76 -1:1.8	1:1μm -1:None	1:80-100nm -1:None	1:5μm -1:None
SGEN101	-1	-1	-1	-1	-1	-1	-1
SGEN106	-1	-1	-1	1	1	1	1
SGEN107	-1	1	1	-1	-1	1	1
SGEN108	-1	1	1	1	1	-1	-1
SGEN109	1	-1	1	-1	1	-1	1
SGEN115	1	-1	1	1	-1	1	-1
SGEN116	1	1	-1	-1	-1	1	-1
SGEN117	1	1	-1	1	1	-1	1

Table 5.18 The fifth Taguchi matrix of experiments with six control factors and one interaction column.

An intentional dip in the TDMAAs flow was included to monitor the level of control available over the *in situ* doping of the absorber layer. The results of the third matrix showed a higher CdTe deposition temperature was beneficial to the conversion efficiency and as a result this control factor was increased to 410 °C to establish if there is an upper limit.

5.13.1 Characterisation of the fifth matrix
J-V measurements

The deposited material from each individual growth run was processed into working devices with a back contact array of ten Au circular contacts 0.025 cm² in area. Current-voltage (J-V) characterisation of the devices was undertaken at a constant power over the area of the PV test array (100 mW cm⁻²) and was achieved using a light source consisting of 4×60 W halogen lamps. The J-V characteristics of each Au back contact was measured yielding values for conversion efficiency (η), fill factor (FF), short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}) and the best parameters for each device are shown in table 5.19.

Run ID	η (%)	FF (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)
SGEN118	3.68	54.22	15.01	0.45
SGEN106	0.04	37.72	0.28	0.34
SGEN107	0.05	34.28	0.36	0.38
SGEN108	4.85	48.90	18.27	0.51
SGEN109	0.00	28.05	0.02	0.37
SGEN115	0.06	48.79	0.36	0.33
SGEN116	4.47	50.98	18.17	0.48
SGEN117	0.24	30.01	1.57	0.50

Table 5.19 The best device parameters from the fifth experimental matrix

The J-V measurements show a large range of efficiency values which appear to be linked to a huge loss of photocurrent, which correlate to the ZnS buffer layer and the ZnTe:As contact layer. The best device of the matrix is SGEN108 with an efficiency of $\eta = 4.27 \pm 0.18$ %. The J-V curve of SGEN108 is shown below in figure 5.9.
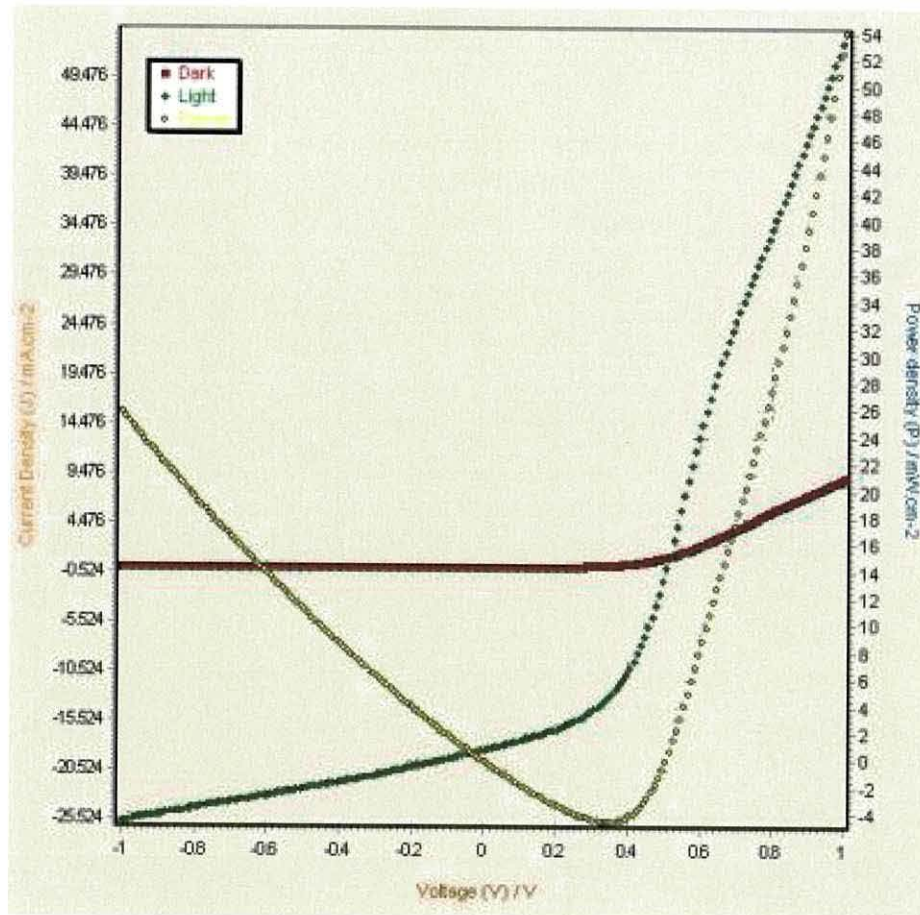

Fig 5.9 Current-voltage curve of SGEN108 showing: illumination in the light (green), illumination in the dark (red) and power (yellow).

The series resistance (R_s) and shunt resistance (R_{sh}) of SGEN108 are 8 Ω and 124 Ω, respectively. This device structure did not contain the ZnS buffer layer or the ZnTe:As contact layer.

Figure 5.10 shows the J-V curve for the device structure SGEN115 which contained the ZnS buffer layer. The light illumination J-V curve (green) for SGEN115 shows a bulge at positive voltage values. This feature may be indicative of an additional Schottky barrier. The series and shunt resistance values calculated for this device are 64 Ω and 4350 Ω, respectively. These results show that the inclusion of the ZnS buffer layer increases the series and shunt resistance values dramatically.
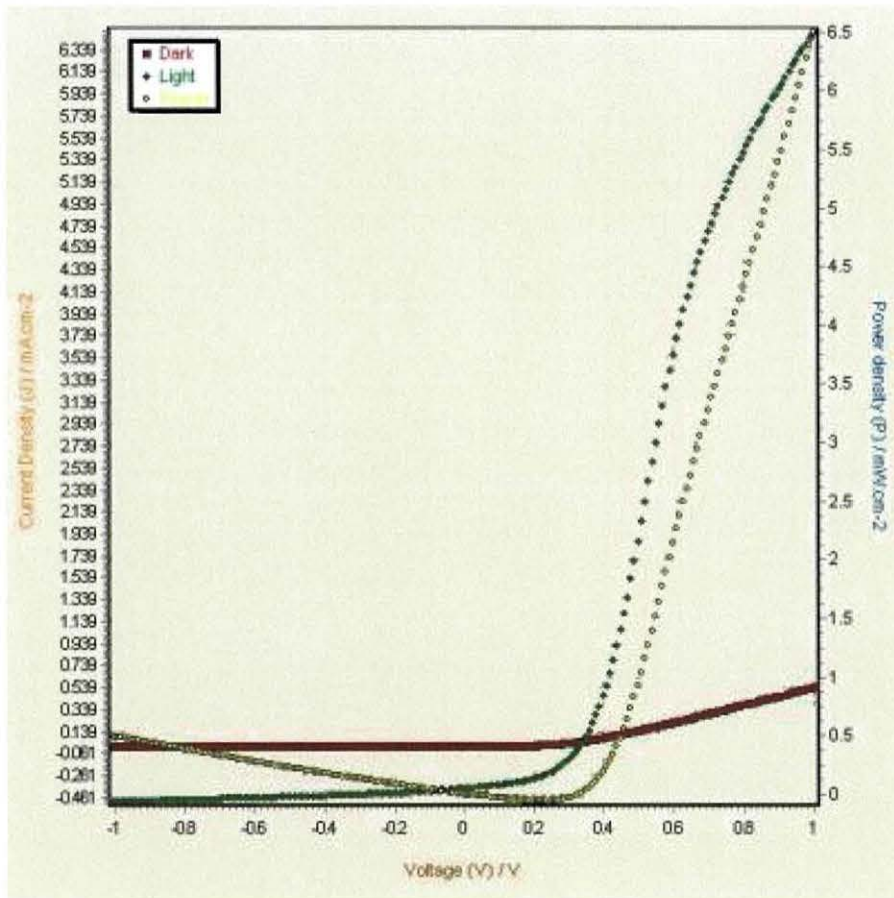

Fig 5.10 Current-voltage curve of SGEN115 showing: illumination in the light (green), illumination in the dark (red) and power (yellow).

The J-V curve of a device structure with the ZnTe:As contact layer (SGEN117) is presented in figure 5.11. The overall shape of the light J-V curve (green) has altered considerably compared to SGEN108 and SGEN115. The series and shunt resistance values calculated for this device are 261 Ω and 933 Ω, respectively.
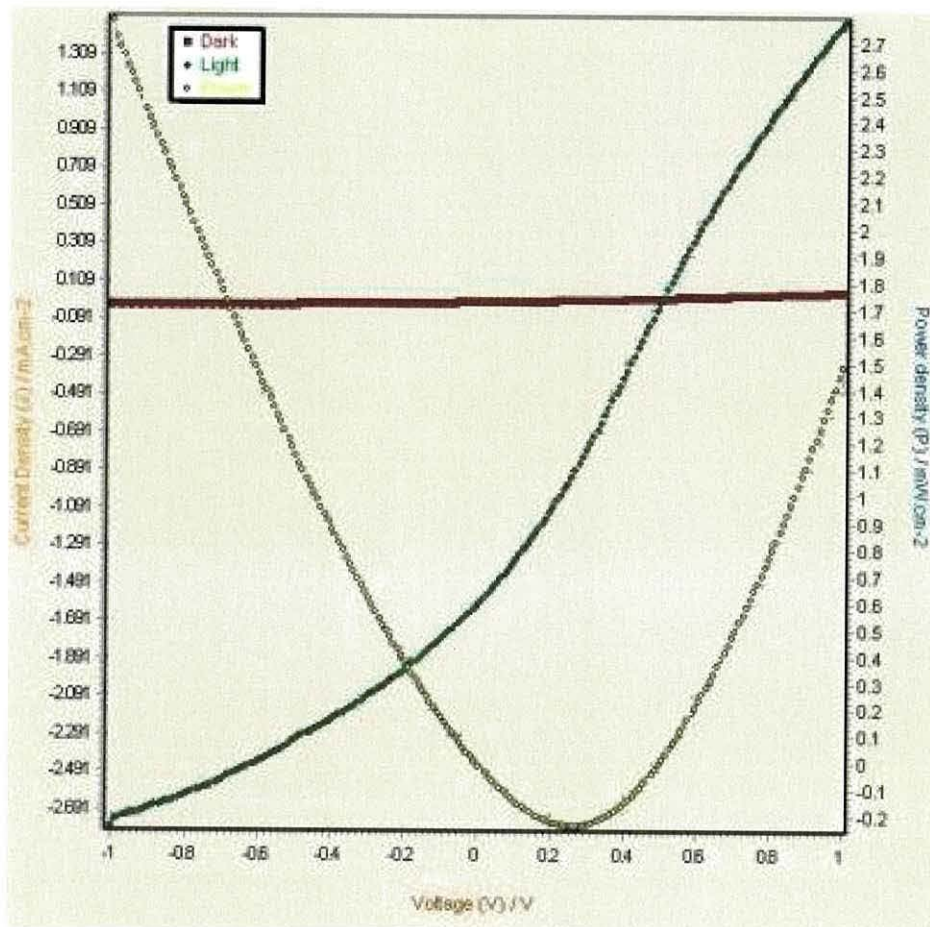
Fig 5.11 Current-voltage curve of SGEN 117 showing: illumination in the light (green), illumination in the dark (red) and power (yellow).

The ZnTe:As layer has a drastic affect on the shunt resistance of the device, visible in figure 5.11 at voltages less than zero. The most probable cause of the large shunt resistance is that the desired p-i-n junction did not form and therefore a tunnelling contact was not obtained under the investigated conditions.

SIMS depth profiles

The intentional dip in the TDMAAs flow during the growth of the absorber layer is visible in both of the SIMS depth profiles presented in figure 5.12. This highlights that there is a high degree of control over the dopant flow during a growth.
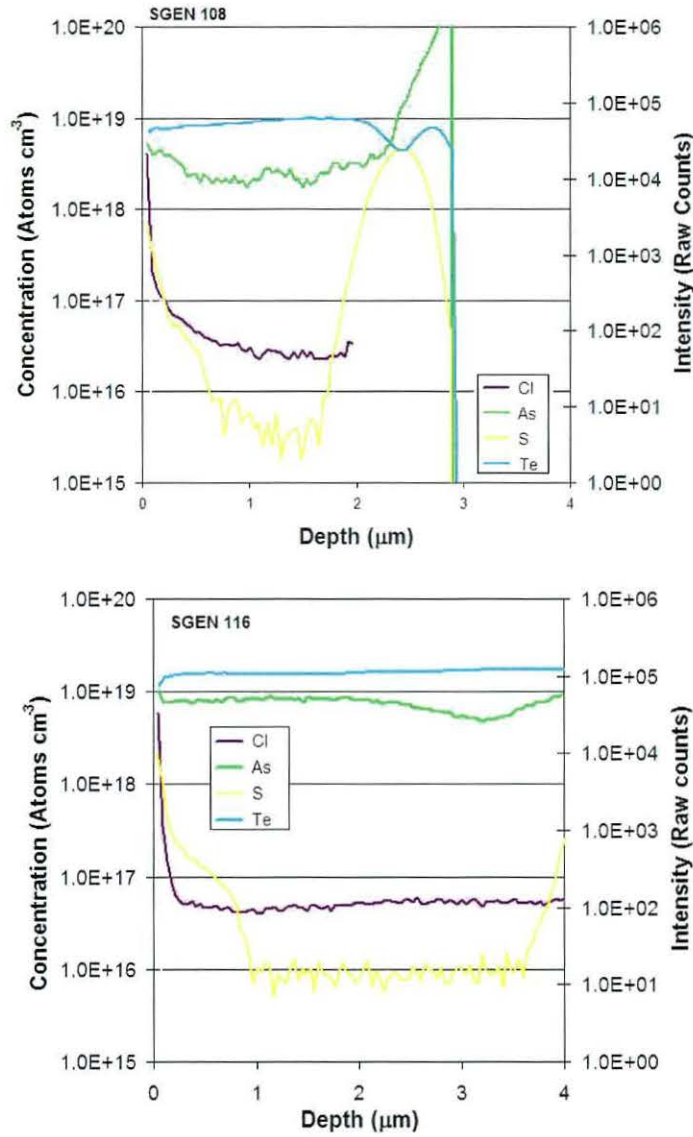
Fig 5.12 SIMS depth profiles of two device structures, (SGEN 108) and (SGEN116), showing the intentional dip in the TDMAAs flow during the deposition of the CdTe layer.

The higher TDMAAs partial pressure of 1×10^{-6} atm results in an arsenic concentration in the absorber layer of 2×10^{19} atoms cm^{-3}. The arsenic profiles are continuous throughout the CdTe layer and appear to quickly recover to the original arsenic concentration after the intentional dip in TDMAAs flow.

5.13.2 Analysis of the fifth matrix

Using the criteria outlined in section 5.6 the threshold value for a significant result for this matrix is 0.44.

$$\Delta T_i = \sqrt{(0.18)^2 + (0.07)^2 + (0.02)^2 + (0.18)^2 + (0.00)^2 + (0.02)^2 + (0.34)^2 + (0.08)^2}$$
$$\Delta T_i = 0.44$$

The Taguchi results of the fifth matrix are presented graphically in figure 5.13. The red band indicates the area of insignificant Taguchi results or efficiency.
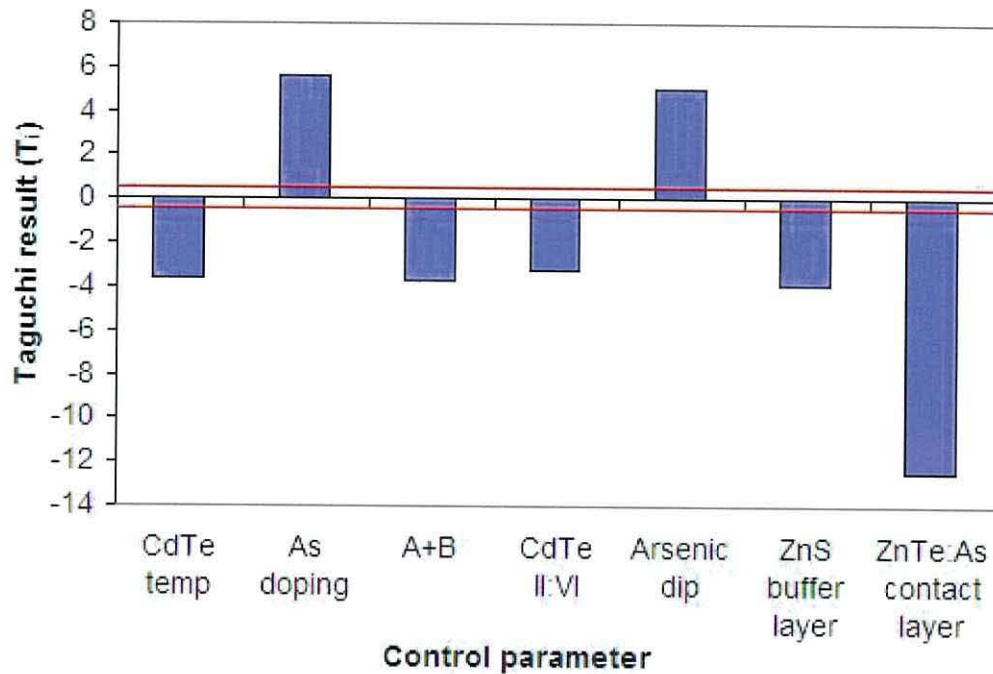

Fig 5.13 A plot of the deviation of the control parameter Taguchi results from the established threshold value of 0.44.

The threshold value of 0.44 deems all the control factor results as significant under the investigated conditions. The results of the fifth Taguchi matrix are presented in table 5.20.

	CdTe temperature	As doping (p.p*)	A+B	CdTe II:VI	Arsenic dip	ZnS buffer layer	ZnTe:As contact layer
	1:410°C -1:390°C	1:1×10^{-6} atm -1:7×10^{-7} atm		1:0.76 -1:1.8	1:1µm -1:None	1:80-100nm -1:None	1:5µm -1:None
$T_{i(\eta)}$	-3.58	5.56	-3.74	-3.28	5.06	-3.88	-12.46

Table 5.20 The Taguchi results ($T_{i(\eta)}$) for efficiency in the fifth Taguchi matrix.

The largest affect on device efficiency was the detrimental impact of the ZnTe:As contact layer. The intention of this step was to create a p-ZnTe layer as a contact material to polycrystalline CdTe in the formation of a p-i-n junction, but as shown in table 5.21 has a negative impact on all of the device parameters. The ZnS buffer layer was also unsuccessful as this had a large negative affect on short-circuit current and open-circuit voltage, which may indicate that the ZnS was high impedance. The

resistivity of the ZnS layers was too high to measure using the four-point probe technique indicating that a high resistive (high-ρ) layer had been deposited. Despite obtaining a high-ρ layer the expected benefits to the V_{oc} and FF were not observed, and the predicted improvement to the rectifying contact between the CdS and ITO layer was not observed. ZnS does not produce the expected benefits of a high-ρ layer under the investigated conditions. Consequently this process step was removed from future matrix experiments due to the detrimental affect on the device performance. Investigations for a suitable buffer layer were carried out independently to the Taguchi experiments.

	CdTe temperature	As doping (p.p*)	A+B	CdTe II:VI	Arsenic dip	ZnS buffer layer	ZnTe:As contact layer
	1:410°C -1:390°C	1:1×10^{-6} atm -1:7×10^{-7} atm		1:0.76 -1:1.8	1:1μm -1:None	1:80-100nm -1:None	1:5μm -1:None
$T_{i(FF)}$	-17.29	-4.61	-12.91	-2.11	-1.65	10.59	-72.83
$T_{i(Jsc)}$	-13.80	22.70	-16.02	-13.08	19.44	-15.70	-49.58
$T_{i(Voc)}$	0.00	0.38	-0.18	0.00	0.04	-0.30	-0.18

Table 5.21 The Taguchi results for the other device parameters: fill factor, short-circuit current and open-circuit voltage.

The dip in TDMAAs flow during the deposition of the CdTe layer has a positive affect on the device efficiency and is due to a large increase in photocurrent. Despite this result the incorporation of a dip in the dopant flow is a process step that may become redundant if the ideal arsenic concentration is attained. The higher TDMAAs partial pressure of 1×10^{-6} atm has a positive impact on the device efficiency with a large benefit for short-circuit current and open-circuit voltage, but produce a lower device efficiency than the TDMAAs partial pressure of 4×10^{-7} atm investigated in the previous matrices.

The CdTe II:VI control factor has a Taguchi result of $T_{i(\eta)}$ = -3.28 confirming the result from the second matrix, that a Cd rich absorber layer is beneficial to the conversion efficiency. With a Cd-rich II:VI a higher arsenic incorporation could be obtained as the arsenic dopant may be encouraged to occupy the Te vacancies as suggested by Stafford et al [11]. The CdTe deposition temperature has a Taguchi result of $T_{i(\eta)}$ = -3.58 which also confirms a deposition temperature of 390 °C remains the most beneficial deposition temperature and highlights an upper limit.

5.13.3 Optimum factor levels and verification

The optimum control factor levels from the fifth matrix are summarised below:

- CdTe deposition temperature 390 °C.
- Arsenic concentration from third matrix 1×10^{18} atoms cm^{-3}.
- Cd rich CdTe (II:VI = 1.8).
- Dip in TDMAAs flow during deposition of CdTe.

The verification experiment produced and average device efficiency of η = 3.16 % ± 0.18. Despite the preference for a higher arsenic concentration of 2×10^{19} atoms cm^{-3}, the highest device efficiency from the fifth matrix (η = 4.27 % ± 0.18) and the verification experiment are both lower than the best device of the third matrix (η = 5.40 % ± 0.08) and fourth matrix (η = 4.65 ± 0.30) indicating that there is an optimum arsenic concentration in the CdTe bulk around 1×10^{18} atoms cm^{-3}. As a result of these findings the TDMAAs partial pressure of 4×10^{-7} atm from the previous matrices was selected as the optimum for the next matrix. The ZnS buffer layer and ZnTe:As contact layer appear to be the main cause of the massive photocurrent losses, highlighting the importance of good electrical contacts. These contact parameters were investigated independently to the matrices due to the detrimental affects on the photocurrent and overall device efficiency.

5.14   Sixth matrix

CdTe/CdS solar cells are normally activated with a cadmium chloride treatment [5, 12, 13]. Although a CdCl$_2$ anneal is conventionally used to activate CdTe solar cells the exact procedure varies in terms of Cl precursor, anneal time and temperature and ambient atmosphere. A process for the deposition of CdCl$_2$ layer via MOCVD using tertiarybutylchloride (tBuCl) as an alternate Cl precursor to the earlier attempt in the first and second matrices was successfully developed independently to the Taguchi experiments [14]. A L$_9$ orthogonal array of experiments with four factors and three levels was constructed to investigate some of the key parameters involved in the CdCl$_2$ deposition process. The four factors were selected as: anneal temperature, anneal time, CdCl$_2$ substrate temperature and arsenic doping. The four factors and their designated levels are shown in table 5.22.

Level	Anneal Temperature (^{o}C)	Anneal Time (mins)	CdCl$_2$ Temperature (^{o}C)	As doping (p.p.[*])
1	400	10	200	0
2	420	20	300	1×10^{-7} atm
3	450	30	400	4×10^{-7} atm

Table.5.22 The four factors under investigation and their corresponding levels

The matrix levels were selected based on previous work. The use of a ZnO buffer layer investigated independently of the matrix experiments was included as a standard in this matrix [15]. The condition of no arsenic doping was included to establish whether arsenic has any effect on the CdCl$_2$ anneal. The L$_9$ matrix of experiments constructed in this work is shown in table 5.23. The column headings indicate the four factors under investigation and the numbers correspond to one of the three levels established earlier in table 5.22. The matrix is termed L$_9$ as there are nine growth experiments in total.

Run ID	Anneal Temp Level	Anneal Time Level	CdCl$_2$ Temp Level	As doping Level
SGEN238	1	1	1	1
SGEN247	1	2	2	2
SGEN240	1	3	3	3
SGEN241	2	1	2	3
SGEN248	2	2	3	1
SGEN243	2	3	1	2
SGEN244	3	1	3	2
SGEN245	3	2	1	3
SGEN246	3	3	2	1

Table.5.23 The L$_9$ matrix of experiments for the 6th Taguchi matrix investigation.

The incorporation of three control factor levels, compared to the usual two, adds robustness to the investigation. This approach requires an alternative analysis method to obtain the Taguchi results, which are discussed below in section 5.14.2.

5.14.1 Characterisation of the sixth matrix

J-V measurements

Current-voltage (J-V) characterisation of the devices was undertaken at a constant power over the area of the PV test array (100 mW cm^{-2}) and was achieved using a light source consisting of 4×60 W halogen lamps. Each device was contacted with three gold square contacts 0.26 cm^2 in area. Adopting a larger contact area reduces the percentage error in contact area resulting in more accurate J-V measurements and also provides a pathway to explore the effects of lateral collection on the J_{sc} values. The average device parameters across the contact array are shown in table 5.24.

Run ID	η (%)	FF (%)	J_{sc} (mAcm^{-2})	V_{oc} (V)
SGEN238	3.04	40.79	11.19	0.67
SGEN247	2.80	60.13	8.88	0.52
SGEN240	6.04	59.12	17.44	0.58
SGEN241	6.30	55.39	18.16	0.63
SGEN248	0.49	59.00	1.73	0.48
SGEN243	2.86	61.00	7.47	0.63
SGEN244	0.75	52.21	2.85	0.50
SGEN245	4.42	47.09	16.60	0.56
SGEN246	0.47	52.35	1.86	0.48

Table.5.24 The best J-V results of the 6th Taguchi matrix of experiments.

The J_{sc} values were lower than exhibited in the previous matrices most likely as a result of the larger contact area utilised in the fabrication of these devices. These results show that increasing the contact area provides a more accurate photocurrent measurement, but further investigation is needed to establish whether this is due to lateral collection or a more accurate contact area value. The average device parameters across the three contacts were used in the analysis of the L_9 matrix. SGEN 241 produced the highest average efficiency device of $\eta = 6.16 \pm 0.13$ %.

5.14.2 Analysis of the sixth matrix

The analysis for this matrix differs from the previous five matrices as this matrix contains three control factor levels to add robustness to the matrix. For each factor, the means of each level are calculated from the average device parameter values across the

contact array: efficiency (η), fill factor (FF), short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}). A delta value corresponding to the maximum difference of each level is calculated (i.e. the maximum mean value minus the minimum mean value). The highest mean value for each factor is then used to rank the significance of the factors on the parameter to be optimised. The results of this analysis for device efficiency are presented in Table 5.25 with the highest mean value of each factor highlighted.

	Anneal Temp	Anneal Time	CdCl$_2$ Temp	As doping
Level1	3.96	3.36	3.44	1.33
Level2	3.22	2.57	3.19	2.14
Level3	1.88	3.12	2.43	5.59
Delta	2.08	0.79	1.01	4.26
Rank	2	4	3	1

Table 5.25 The analysis of the L$_9$ matrix for device efficiency (%).

The order of the factors significance on the overall device efficiency was: arsenic doping > anneal temperature > CdCl$_2$ substrate temperature > anneal time. The arsenic doping was the dominant factor, with the arsenic concentration of 1×10^{18} atoms cm^{-3} remaining the optimum value resulting in an increase in the efficiency, J_{sc} and V_{oc}. These orders of influence suggest that a short anneal time (10 minutes) and low anneal temperature (400 ^{o}C) are the optimum conditions based on the levels investigated. The results of the matrix experiments can also be presented graphically. Figure 5.14 shows the trends of the factor levels influence on device efficiency. Figure 5.14d shows a clear linear trend of higher arsenic partial pressure resulting in improved device efficiency.
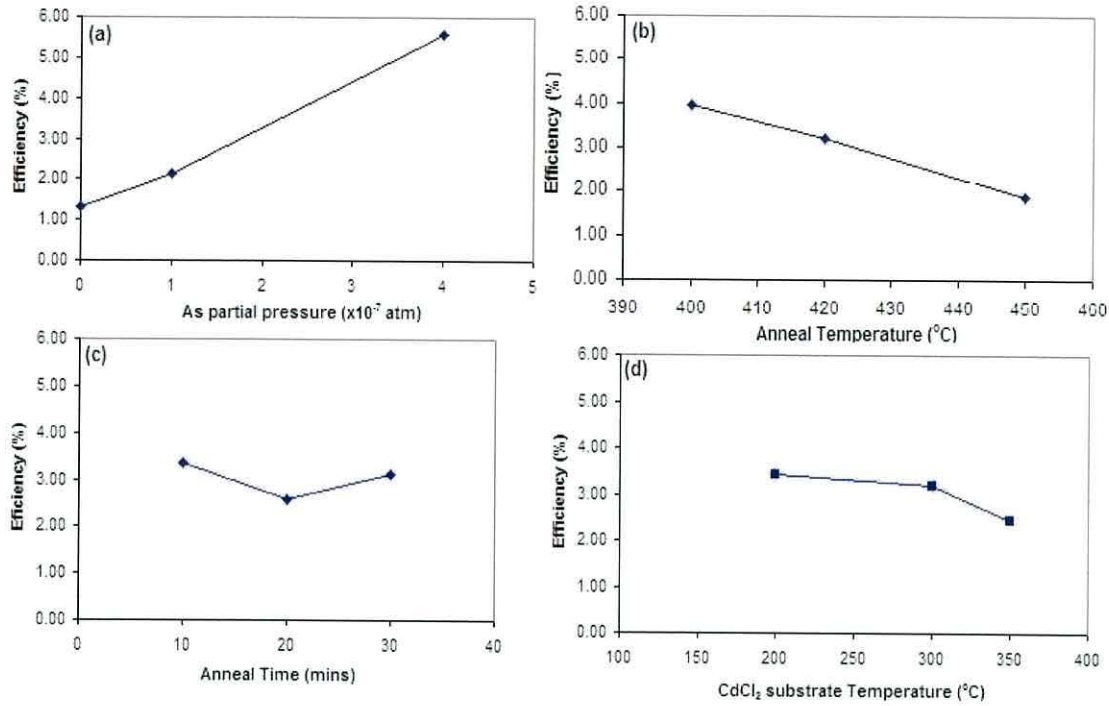
Fig.5.14 Trend charts of the overall device efficiency against the factors: a) arsenic doping b) anneal temperature c) anneal time, d) CdCl$_2$ substrate temperature.

The highest mean value for arsenic doping is 5.36 and corresponds to level 3 (p.p. 4×10^{-7} atm). The mean values of the three levels have a delta of 4.95. This is the largest delta value for device efficiency and therefore ranks arsenic partial pressure first. This indicates that arsenic is still needed in the CdTe even with a measurable CdCl$_2$ thickness. It is possible that the arsenic is required to obtain p-type CdTe and the CdCl$_2$ provides passivation of the grain boundaries and grain growth. These implications are discussed in more detail in chapter 6. A verification experiment will be needed to determine whether this trend goes through a maximum at other levels (i.e. partial pressures above 4×10^{-7} atm).

The order of influence for FF is significantly different to the other device parameters. The results of the Taguchi analysis for FF are presented graphically in figure 5.15. The ranking order is: anneal time > anneal temperature > arsenic doping > CdCl$_2$ substrate temperature.
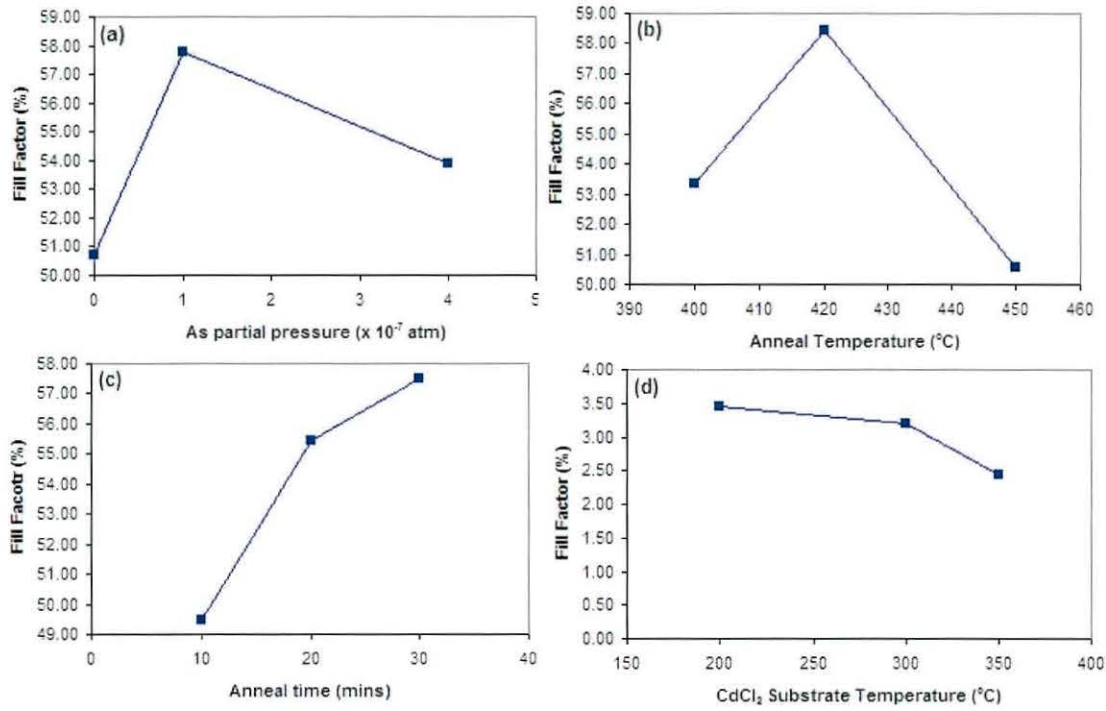
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Fig 5.15 The analysis of the L9 matrix for fill factor (%).

The highest mean values of each investigated parameter are comparable within delta and therefore these effects can be deemed insignificant compared to the other device parameters.

The Taguchi analysis results for short-circuit current are presented below in figure 5.16. The largest influence on J_{sc} is caused by arsenic partial pressure with the higher TDMAAs partial pressure of 4×10^{-7} atm resulting in an average J_{sc} value of 16.19 mAcm^{-2}. This result reiterates the beneficial affects of arsenic incorporation of the order of 1×10^{18} atoms cm^{-3} in the CdTe layer observed in the earlier matrices.
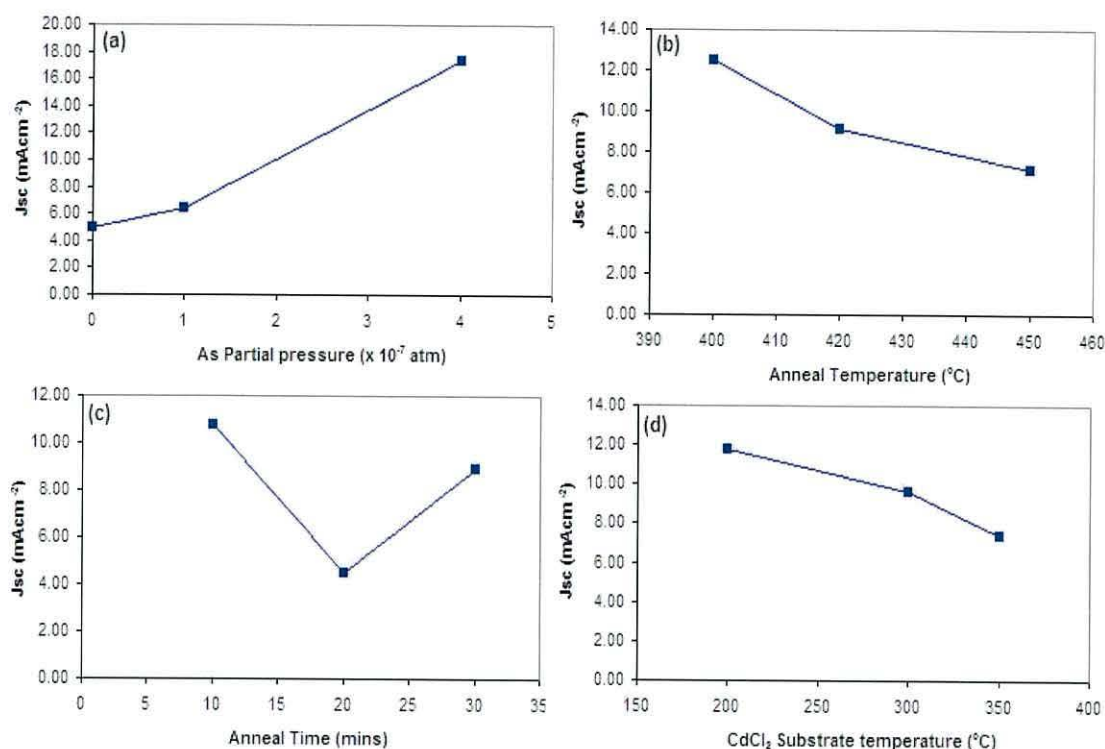
Fig 5.16 The analysis of the L9 matrix for J_{sc} (mAcm^{-2}).

Without *in situ* arsenic doping a J_{sc} of 1.46 is obtained, indicating that the material is not photoactive without doping. The anneal temperature; anneal time and CdCl$_2$ substrate temperature control factors have a similar influence on the J_{sc} with highest mean values of: 8.05, 8.14 and 8.86, respectively.

The results of the Taguchi analysis for open-circuit voltage are presented graphically in figure 5.17. The arsenic doping and CdCl$_2$ substrate temperature control factors both rank first.
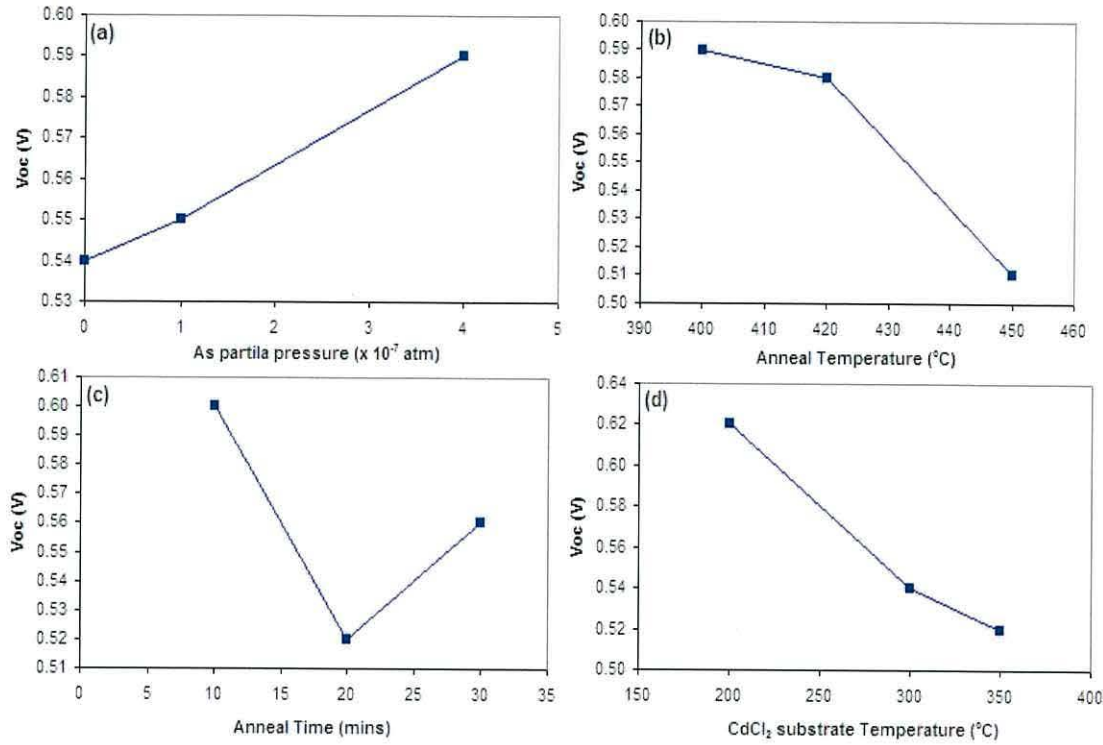
Fig 5.17 The analysis of the L9 matrix for V_{oc} (V).

Plot (a) shows an upward trend for V_{oc} with increased arsenic partial pressure, but this would come at a sacrifice to the device efficiency as the fifth matrix investigated higher arsenic concentrations in the CdTe, but yielded lower efficiency devices.

5.14.3 Optimum factor levels and verification

The Taguchi method was applied to survey process parameters used for *in situ* $CdCl_2$ treatment and arsenic doping. A L_9 orthogonal array of experiments was constructed to investigate four factors: anneal temperature, anneal time, $CdCl_2$ substrate temperature and arsenic partial pressure. The new optimum conditions for improved device efficiency based on the investigated levels are: arsenic partial pressure 4×10^{-7} atm, $CdCl_2$ substrate temperature of 200 °C, anneal temperature 400 °C and anneal time of 10 minutes. The dominant factor for three of the device parameters was arsenic partial pressure, favouring level 3 in each case (p.p. 4×10^{-7} atm). The anneal conditions favoured the low level settings of 10 minutes (level1) at 400 °C (level1), for three of the device parameters (η, J_{sc}, and V_{oc}), indicating that a gentle anneal is required to obtain optimum conditions.

The optimum factor levels for improved device efficiency from this matrix investigation are:

- Arsenic partial pressure 4×10^{-7} atm
- $CdCl_2$ substrate temperature 200 °C
- Anneal temperature 400 °C
- Anneal time 10 minutes

The verification experiment (SGEN272) was carried out with the above factor settings which yielded an average device efficiency of $\eta = 6.55$ % ± 0.73 under 100 mW cm^{-2} power from a four halogen lamp setup.

Throughout the matrix investigations the reliability of the spectral match between the halogen lamps and the AM1.5 spectrum has been questioned due to J_{sc} values above the theoretical limit of CdTe material (J_{sc} theoretical maximum ~ 28 mAcm^{-2}) when the device structures were processed with an alternate etch treatment of nitric and phosphoric acid, conventionally known as the NP etch. To allow comparison between the matrices all device were J-V characterised using a four halogen lamp source. The spectral output of the halogen lamps is shown in figure 5.18 below and clearly shows a poor correlation to the AM1.5 spectra.
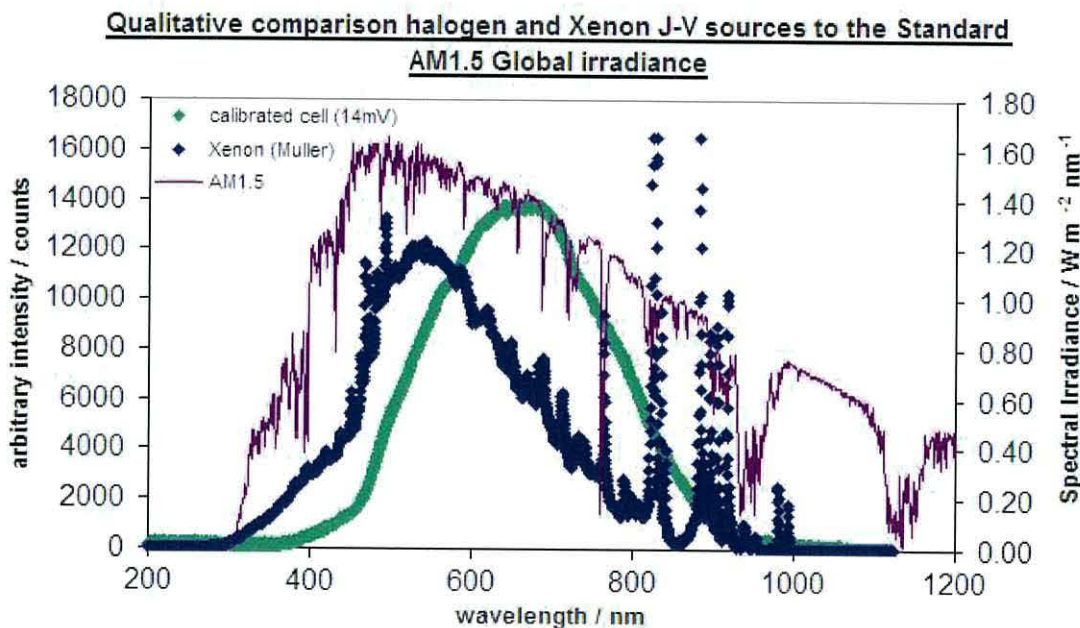

Fig 5.18 Plot showing the spectral match of the halogen and Xenon J-V source compared to the AM1.5 solar spectrum.

The halogen lamp setup was replaced by a xenon lamp source which is a better fit to the AM1.5 irradiance spectra than the halogen source. The power output of the xenon lamp was increased in order to improve the spectral match shown in figure 5.18 and calibrated to a test cell provided by Tim Gessert from National Renewable Energy Laboratory (NREL) in America. The device with the 200 °C CdCl$_2$ substrate temperature was re-tested (SGEN272) with the xenon light source and resulted in an improved average device efficiency of η = 10.64 % ± 0.47. These results highlight the importance of a reliable J-V setup with a good spectral match to the AM1.5 solar spectrum.

5.15   Summary of Taguchi matrix experiments

The Taguchi method has proved to be a useful tool in an empirical investigation of MOCVD grown CdTe/CdS solar cells, but must be used in conjunction with characterisation of the layers to understand the effect on device efficiency and help determine why one parameter becomes more significant than another in an optimisation process. A criterion for determining a threshold value for significant changes was successfully applied to the third, fourth and fifth matrix results.

The first matrix investigated the starting parameters established in earlier work and extended the investigation to include arsenic doping of the CdTe absorber layer, *in situ* CdCl$_2$ treatment and *in situ* post growth annealing. The second matrix was designed to investigate the affects of impurities observed in the first matrix. The largest benefit resulted from swapping to an alumino-silicate substrate due to a considerable reduction in impurity diffusion through the device structure.

The starting conditions for the third matrix were based on SGEN29 but omitted the CdCl$_2$ treatment to allow concentration on arsenic doping of the CdTe absorber layer. The two most relevant parameters were CdTe growth temperature and *in situ* arsenic doping of the CdTe layer. SEM verified that grain enlargement from 1 μm to 3 μm occurred when CdTe was deposited at the higher temperature of 390 °C. SIMS depth profiling revealed that the arsenic concentration in the device structures was an order of magnitude greater with the higher partial pressure of 8×10^{-7} atm compared to the lower setting of 4×10^{-7} atm. The lower arsenic partial pressure was preferred, indicating an optimum arsenic concentration above which device efficiency reduces.

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The fourth matrix was designed to further investigate the CdS window layer and the CdS/CdTe interface. The criteria established three of the investigated control factors as insignificant: interaction A+B, DIPTe flow to produce a Te layer and CdS anneal for 5 minutes in a nitrogen atmosphere. Cl doping of the CdS layer was achieved and confirmed by SIMS analysis. Cl diffusion from the CdS:Cl layer across the junction into the CdTe:As layer aided by the CdS anneal was deemed to have a detrimental affect on the cell performance with considerable degradation of the photocurrent.

The fifth matrix examined the interface between the CdTe absorber layer and the back contact. A ZnS buffer layer was introduced to investigate the possible benefits of a high resistive (high-ρ) layer between the TCO and CdS window layer. A highly resistive ZnS layer was deposited, but it did not yield the expected improvements in device efficiency due to an increase in series resistance. The ZnTe:As back contact proved detrimental to the short-circuit current and device efficiency due to a large increase in both series and shunt resistance and was subsequently removed from future matrix experiments. An upper limit for the deposition temperature of CdTe was identified as 390-410 °C. An upper limit for the incorporation of arsenic was investigated using two high TDMAAs partial pressures. The Taguchi results showed a preference for the higher arsenic incorporation of 1×10^{19} atoms cm^{-3}, but resulted in lower device efficiencies than in the previous matrices indicating an limit to the benefits of arsenic incorporation. As a result the TDMAAs partial pressure from the earlier matrices was carried forward as the optimum (4×10^{-7} atm).

The sixth matrix was an L_9 orthogonal array of experiments constructed to survey cadmium chloride layer deposition and annealing processing parameters and arsenic doping in CdTe/CdS solar cells. This matrix added robustness with the incorporation of three control factor levels in place of the two levels used in the previous five matrices. The dominant factor for three of the device parameters was arsenic partial pressure, favouring level 3 in each case (p.p. 4×10^{-7} atm). The anneal conditions favoured the low level settings of 10 minutes (level1) at 400 °C (level1), for three of the device parameters (η, J_{sc}, and V_{oc}), indicating that a gentle anneal is required to obtain optimum conditions. A verification experiment using the selected optimum conditions produced an improved device with an average efficiency of 5.82 % ± 0.38. Additional

growth experiments with a $CdCl_2$ temperature of 200 ^oC produced an average device efficiency of η = 6.55 % ± 0.73 with the standard halogen lamp setup. The same device was tested with a class A xenon light source with an improved spectral match to AM1.5 than the standard halogen lamp setup resulting in an average device efficiency of η = 10.64 % ± 0.47.

5.16 References

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6.0 Arsenic doping CdTe

6.1 Introduction

Intentional doping of both sides of the pn-junction in MOCVD grown CdS/CdTe devices was first reported by Berrigan et al [1]. The statistical method used in this work highlighted arsenic concentration in the absorber layer as a key parameter in the development of CdS/CdTe PV devices [2]. Doping is a complex process and effective control of this operation requires an understanding of several factors including; precursor decomposition, transport to the surface, surface reactions, gas reactions and surface sites. Arsenic is often selected as the dopant of choice to form p-type CdTe because atomic arsenic has one less electron in the outer shell and a smaller atomic radius than tellurium making incorporation of arsenic into the crystal lattice probable. Ghandhi et al. doped epitaxial films grown onto single-crystal CdTe substrates using arsine (AsH_3) [3]. Other arsenic precursors have been investigated in detail for the growth of III-V's, including tertiarybutylarsine (TBA) [4] and trimethylarsine (TMA) [5].

Doping p-CdTe is a dominant problem in the production of CdS/CdTe solar cells. In polycrystalline material there is considerable compensation of dopants by the grain boundaries resulting in the effective carrier concentrations being orders of magnitude lower than the dopant concentration. The main problem in doping polycrystalline material is that all metallic dopants can easily segregate to the grain boundaries giving rise to metallic, highly electrical conducting phases that can cause shunts in the CdTe layer. The complex material structure of polycrystalline photovoltaic devices makes the separation of the effects of growth parameters increasingly difficult. Characterisation of these materials plays an important role in understanding the effects of dopants within the structure.

6.2 Experimental

The choice of precursor can affect: homogeneity, morphology and contamination of the device structure. Alternative organometallic precursors can provide information on growth stability issues including thermal stability and pre-reaction. Pre-reactions are important as they can produce difficulties in controlling growth defect chemistry and

dopant incorporation. The precursor ratio can also greatly affect the stoichiometry. In this work tris(dimethylamino)arsine (TDMAAs) is selected as the arsenic precursor as it pyrolyses at lower temperatures than arsine and tertiarybutylarsine (TBA) with 50% decomposition achieved at 350 °C leading to elemental arsenic [6]. Although pyrolysis data is crucial, other parameters including surface catalysis and surface kinetics can dominate. Easton *et al.* showed that the decomposition of diethyltellurium (DETe) was significantly effected by surface specificity [7]. Another possible benefit of TDMAAs is that it does not contain As-H bonds, which can passivate the arsenic dopant

CdS/CdTe device structures were grown using atmospheric MOCVD, onto commercially available ITO/glass substrates from Delta Technologies Ltd. The organometallic precursors for Cd, S and Te were: Dimethylcadmium (DMCd), Ditertiarybutylsulphide (DTBS) and Diisopropyltelluride (DiPTe), respectively. The CdTe layers were *in situ.* arsenic doped using TDMAAs in a double dilution line arrangement with different partial pressures ranging from 3×10^{-9} to 1×10^{-6} atm. The arsenic concentrations within the device structures were determined by secondary ion mass spectrometry (SIMS).

SIMS depth profiles were carried out on a Cameca ims 4f instrument with a Cs^+ 10KeV primary ion beam, from the CdTe surface through to the TCO. The ion counts were calibrated into concentrations (atoms cm^{-3}) using supplied reference samples of arsenic implants in CdTe layers on glass substrates. Abnormally high levels of dopant concentrations can sometimes be attributed to surface or porosity artefacts such as holes and particulates.

Depth scales were determined by measuring the sputtered crater depth on the reference samples by interference microscopy assuming a uniform erosion rate. The reliability of identifying the exact depth and interfaces can be difficult depending on the roughness of the layer surfaces. CdTe material has a relatively rough surface which can lead to blurring of the interface between the CdS and CdTe. To reduce these effects the samples were chemically polished with 0.25 % bromine in methanol solution, which is shown to reliably remove 1μm of material, smooth the surface and remove surface contaminants.

6.3   Arsenic control

The Taguchi methodology discussed in chapter 5 highlighted arsenic concentrations in the CdTe layer as an important growth parameter in potentially improving the device characteristics including overall conversion efficiency. Control over the dopant incorporation is therefore a critical step in producing CdS/CdTe solar cells. At the surface of the CdTe layer there are tellurium vacancies, which can be filled by arsenic causing p-type doping. SIMS depth profiles of two completed structures with TDMAAs partial pressures of 3×10^{-7} and 5×10^{-7} atm, deposited at different growth temperatures (390 $^{\circ}$C and 410 $^{\circ}$C) as a means of monitoring the control and sensitivity of *in situ.* arsenic doping using MOCVD are shown in figure 6.0.
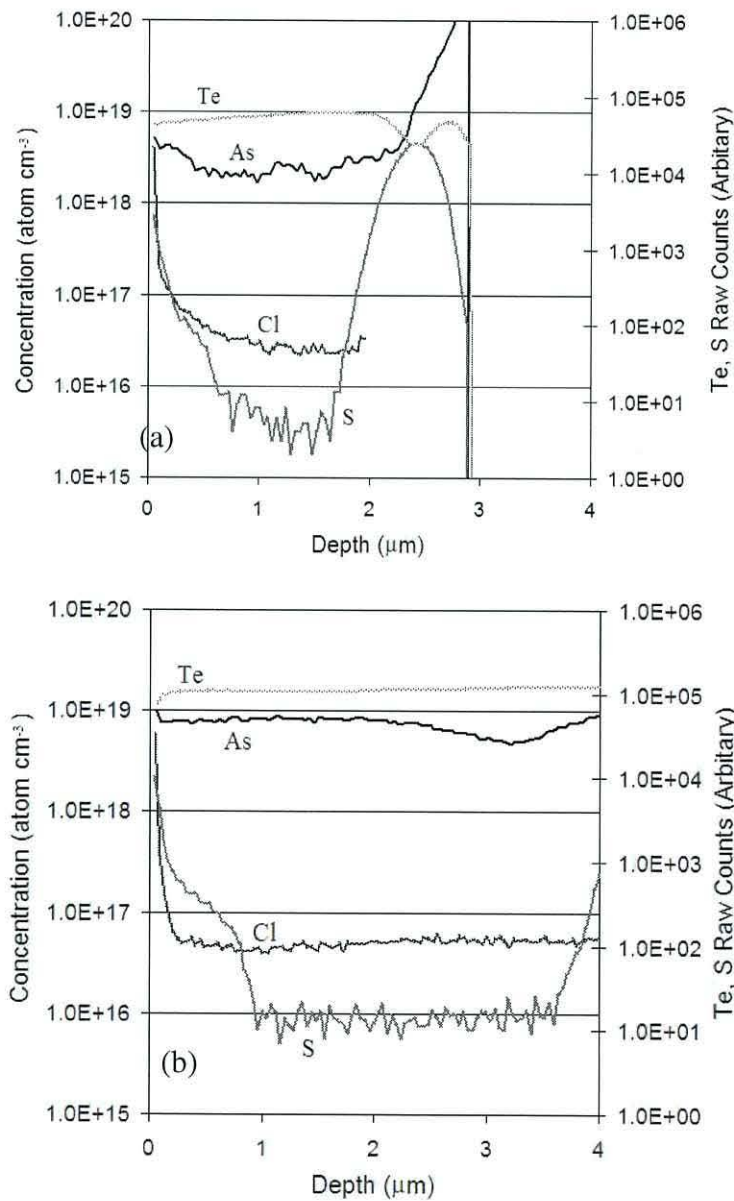
Fig.6.0 SIMS depth profiles of CdS/CdTe structures deposited at a) 390 $^{\circ}$C and b) 410 $^{\circ}$C, with arsenic concentrations of 2×10^{18} and 8×10^{18} atoms cm^{-3}, respectively.

The arsenic concentration of the low temperature (390 °C) and the high temperature (410 °C) are 2×10^{18} atoms cm^{-3} and 8×10^{18} atoms cm^{-3}, respectively. The higher arsenic concentration of 8×10^{18} atoms cm^{-3} in the higher growth temperature structure indicates that incorporation of arsenic into the structure increases with deposition temperature.

The level of control available with *in situ* doping, using MOCVD was investigated by depositing device structures with an intentional "dip" in the TDMAAs flow during the CdTe layer. The incorporation of the dopant dip required an alternative sample preparation method, as the standard Br/MeOH etch used to reduce roughness may remove the material of interest. These samples were swabbed with methanol and dried with a nitrogen gun. The low temperature growth has a non-uniform arsenic profile which masks the arsenic dip. The SIMS depth profile of such a structure is presented in figure 6.1.
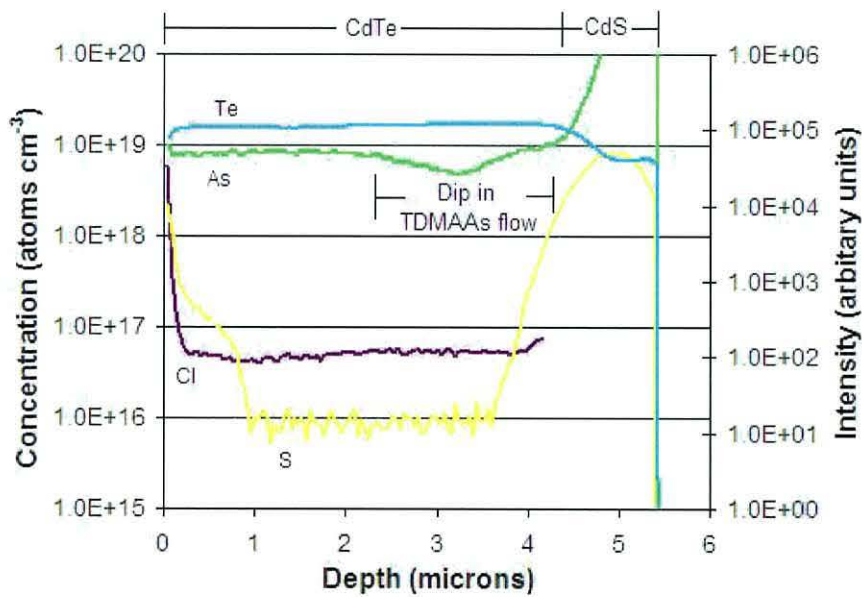

Fig 6.1 SIMS depth of a device structure with a deliberate dip in the TDMAAs flow during the CdTe deposition.

The intentional dopant dip can be clearly seen in the high temperature growth at ~ 3 μm and is an indication of the control available from the MOCVD growth technique, highlighting effective control of dopant profiles in device structures.

The polycrystalline nature of CdTe creates a complex situation as impurities and defects such as grain boundaries strongly influence the local recombination behaviour of the charge carriers. At surfaces and defect centres, carrier lifetimes are greatly reduced as

the defects provide a more probable, non-radiative recombination route than the pn junction. The polycrystalline nature of CdTe can also affect doping as there is considerable compensation of incorporated dopants from grain boundary states that results in the effective carrier concentration being orders of magnitude lower than the dopant concentration.

Arsenic doping mechanisms

Some of the key stages involved in arsenic incorporation are shown in figure 6.2 including:

- Transport of the organometallics
- Decomposition of the organometallics
- Adsorption on the surface
- Desorption of organic products
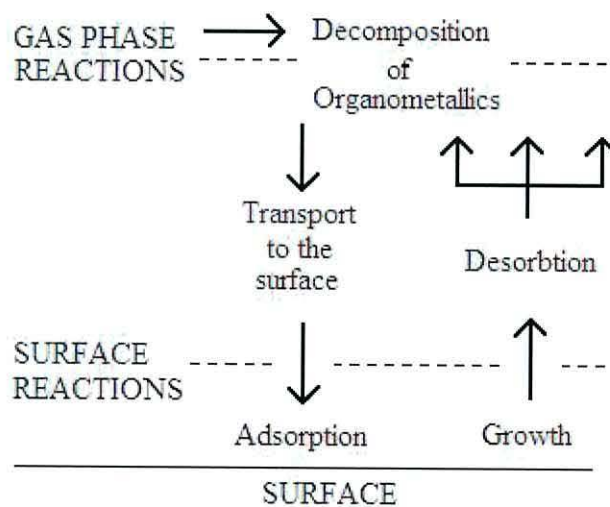
Fig. 6.2 A schematic showing some of the steps involved in order for arsenic incorporation into the layer.

This schematic clearly shows that doping via MOCVD is a complex process. The reactions at the surface and in the gas phase will both occur during growth. Which process dominates is determined by a number of factors including: temperature at the surface, temperature in the gas phase and site specificity. The precursors will absorb onto the surface via chemisorption or physisorption. The Taguchi matrix method utilised in this work identified arsenic doping as a significant control factor for possible improvements to CdTe device parameters. The Taguchi method is a powerful tool, but only identifies the most beneficial parameter levels of the experimental conditions investigated.

Arsenic incorporation into CdTe

A series of CdS/CdTe structures were grown with different TDMAAs partial pressures ranging from 3×10^{-9} to 1×10^{-6} atm were grown to monitor the control and incorporation of arsenic into the bulk and identify the optimum arsenic doping level. The arsenic concentrations within the CdTe layers were determined using SIMS depth profiles, which in each case showed a constant concentration within the bulk of the CdTe layer. The device structures with TDMAAs partial pressures of 3×10^{-8} and 3×10^{-9} atm, shown in figure 6.3, yield arsenic concentrations in the background region indicating a detection limit of 1×10^{16} atoms cm^{-3}. Therefore the arsenic profiles for these device structures cannot be clearly seen.
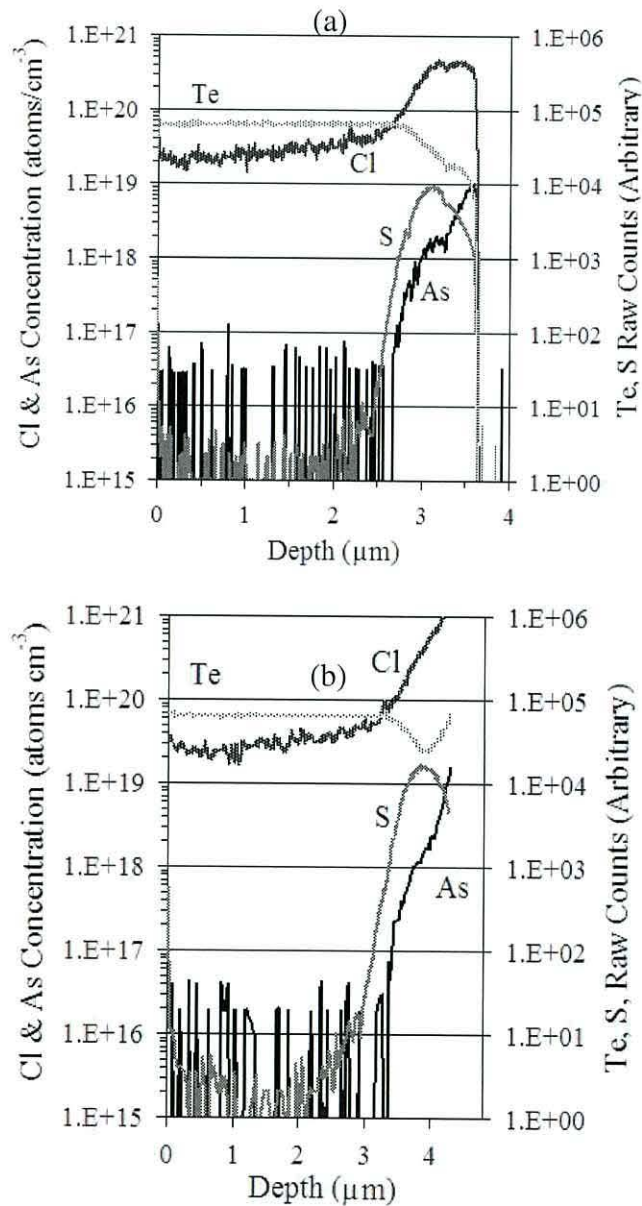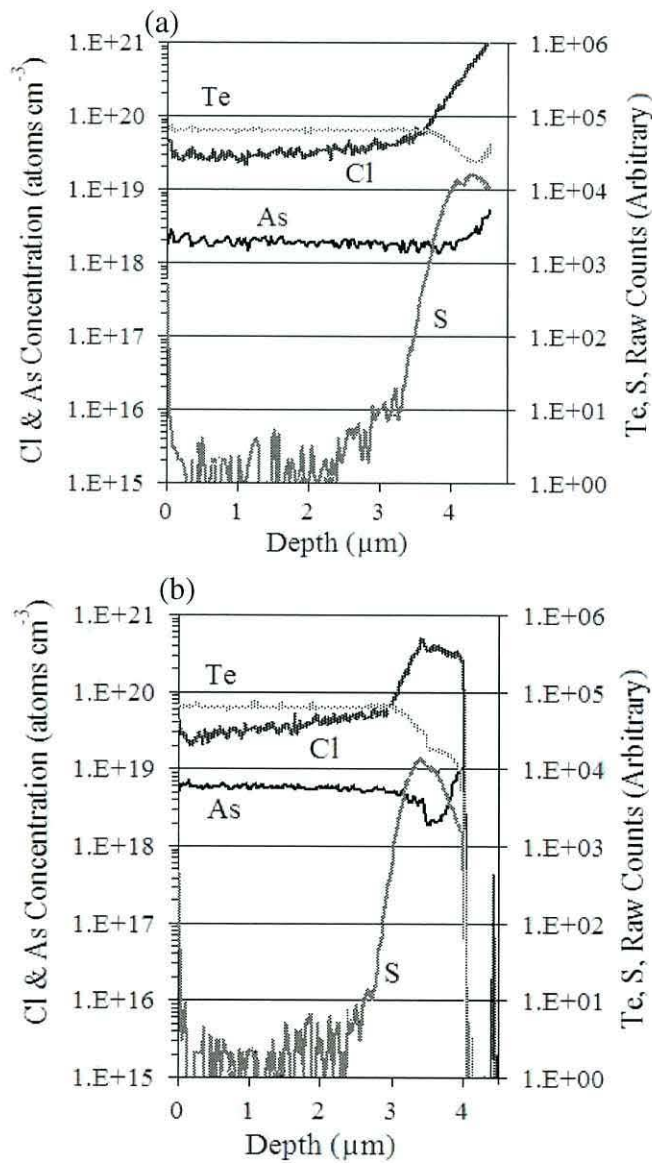

Fig. 6.3 SIMS depth profiles of device structures with TDMAAs partial pressures of (a) 3×10^{-8} and (b) 3×10^{-9} atm indicating a detection limit of 1×10^{16} atoms cm^{-3}.

This indicates that the detection limit for arsenic on the Cameca ims 4f instrument of the order of 1×10^{16} atoms cm^{-3}. SIMS depth profiles of higher TDMAAs partial pressures ranging from 6×10^{-8} up to 1×10^{-6} atm, presented in figure 6.4, clearly show concentrations above the background. Each device structure has a uniform arsenic profile throughout the CdTe layer with minimal noise. A drop in the arsenic signal in the CdS is visible in figure 6.4 b and c but not in a. The drop in arsenic signal correlates with a rise in the chlorine signal in both cases. The CdTe growth rate of the two device structures was slightly higher (0.46 nm/s) compared to the usual growth rate (0.43 nm/s). This is only a marginal increase but may effect the incorporation of dopants into the CdS layer.
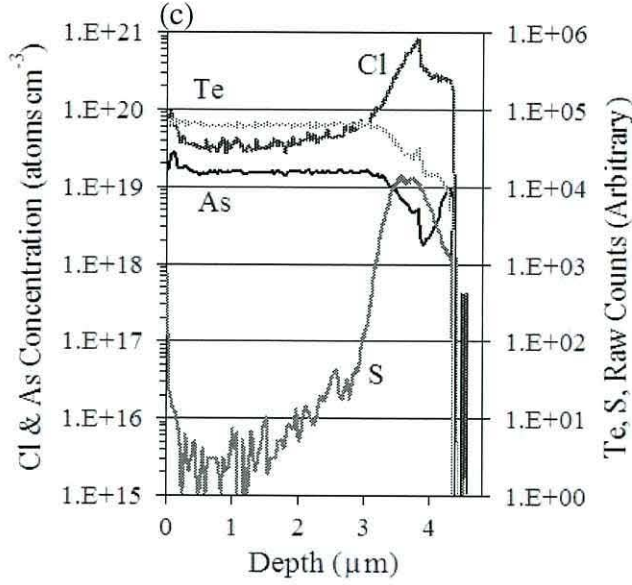
Fig. 6.4 SIMS depth profiles of device structures with TDMAAs partial pressures of (a) 3×10^{-7} (b) 5×10^{-7} (c) 1×10^{-6} atm corresponding to arsenic concentrations up to 1.5×10^{19} atoms cm^{-3}.

The arsenic concentrations in the layers range from 1×10^{18} to 1×10^{19} atoms cm^{-3}. SIMS analysis was also carried out on device structures with TDMAAs partial pressures of 6×10^{-8} atm and 1×10^{-7} atm which resulted in arsenic concentrations in the CdTe of 1×10^{17} atoms cm^{-3} and 4×10^{17} atoms cm^{-3}, respectively.

6.4 Square law dependence

A plot of the logarithms of TDMAAs partial pressure against the logarithms of arsenic concentration in the CdTe layers in figure 6.5 show a linear trend with a slope of 2 above the detection limit of the Cameca ims 4f instrument. This trend can be explained in terms of reaction kinetics. If we assume the rate law for a reaction with reactive species, A, in isolation is;

$$r = k[A]^a \qquad (6.0)$$

Then the initial rate r_0 is given by the initial value of the concentration of A as expressed in equation 6.1. For these experiments this can be assumed to be the inlet concentration of TDMAAs.

$$r_0 = k[A]_0^a \qquad (6.1)$$

Taking logarithms:

$$\log r_0 = \log k + a \log[A]_0 \qquad (6.2)$$

Therefore for a series of initial concentration, a plot of the logarithms of the initial rates against the logarithms of the initial concentration should be linear with slope a.
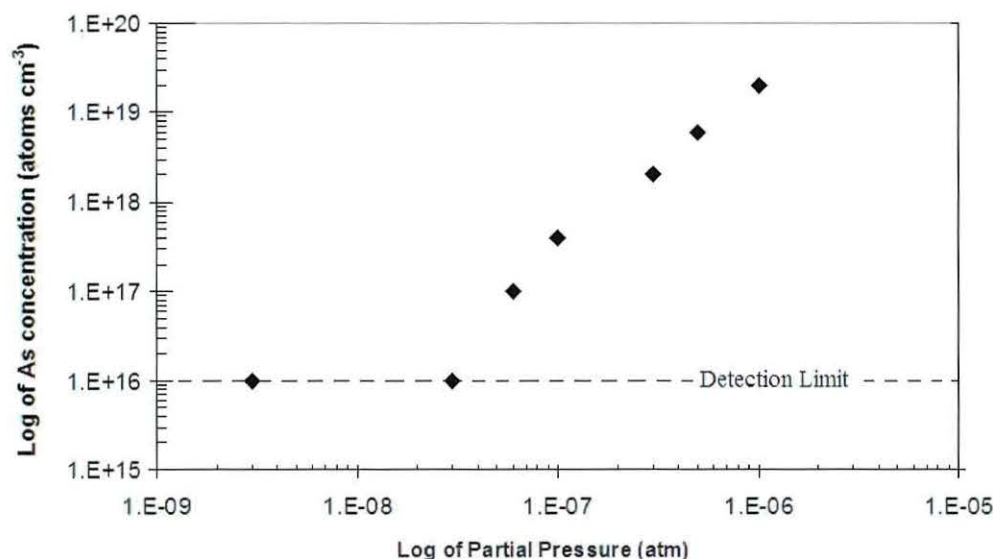
Fig.6.5 A plot of the logarithms of arsenic concentration in the CdTe layer against the logarithms of arsenic partial pressure during the growth.

The rate of arsenic incorporation is taken as the concentration of arsenic in the layer as the growth rate of CdTe was independent of arsenic concentration. The linear trend has a slope of a = 2, which can be described as a square law dependence of arsenic incorporation into the bulk material on partial pressure indicating that the reaction follows second order kinetics.

The growth rate is proportional to the flux of reactants being transported, by diffusion through the gas phase to the interface, and is equivalent to the flux of reactants crossing the interface to the solid under steady state conditions. Some of the key stages involved in arsenic incorporation into the bulk are listed below:

1. Transport of the organometallics
2. Decomposition of the organometallics
3. Adsorption on the surface
4. Desorption of organic products

It can be assumed that there are a fixed number of reactive sites upon the surface, which an atom or molecule can chemisorb to. Once a site is filled, a second molecule cannot absorb there. The number of atoms that desorb from the surface is dependent on the surface concentration at a constant temperature. The maximum amount of arsenic incorporation that can be achieved is the amount that would establish equilibrium assuming the molar concentration is constant in the gas stream.

Previous SIMS characterisation shows a saturation point above a partial pressure of 1×10^{-6} atm. A blockage in the double dilution line was cleared and resulted in a higher TDMAAs flow with the same arsenic setting used to obtain a partial pressure of 1×10^{-6} atm. A partial pressure of 1.5×10^{-6} atm. was achieved with the blockage removed, but yielded the same arsenic concentration in the layer of 2×10^{19} atoms cm^{-3} as shown in figure 6.6.
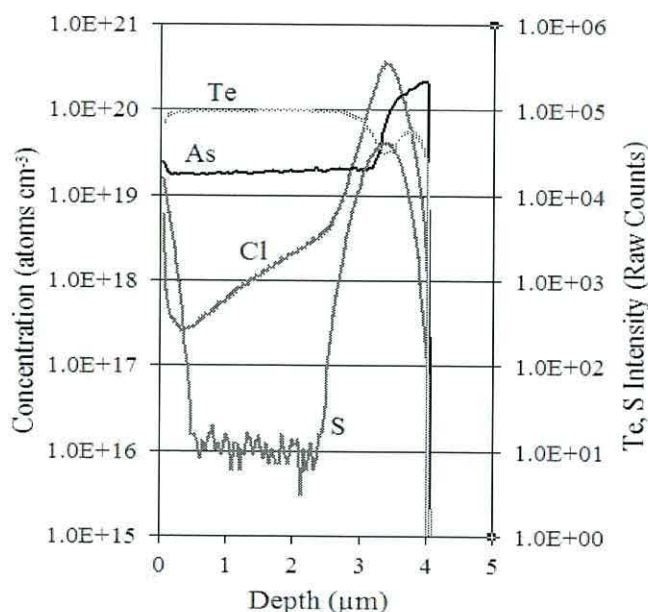

Fig 6.6 SIMS depth profile of a device with a higher TDMAAs partial pressure of 1.5×10^{-6} atm which yields the same As concentration as a device with a lower partial presure 1×10^{-6} atm.

This would be indicative of a limit to the incorporation of arsenic in these layers. This shows that the active carrier concentration for arsenic incorporation into the CdTe bulk is limited to 2×10^{19} atoms cm^{-3}.

6.5   Decomposition of TDMAAs

In addition to the four main growth parameters of MOCVD; temperature, pressure, deposition time and site specificity, the chemical nature and behaviour of the metal-organic precursor is also crucial. The chemical structure of the precursor may make site blocking a dominant factor. Figure 6.7 shows the incorporation of arsenic into a CdTe layer by the filling of tellurium vacancies.
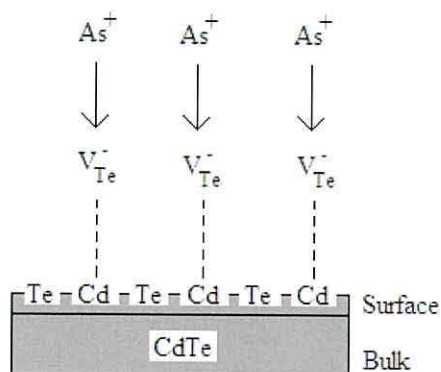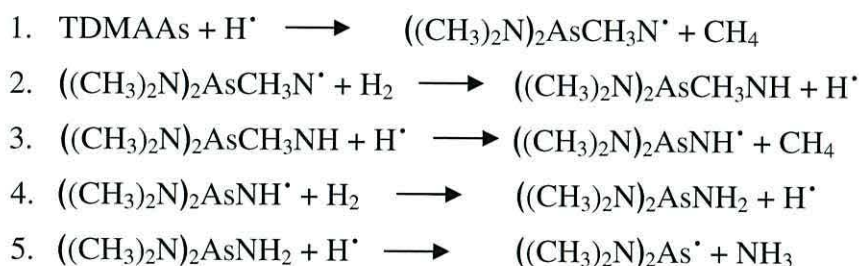
Fig. 6.7 A schematic of the doping sequence of arsenic in CdTe showing the Tellurium vacancies being filled by arsenic.

The experimental data shows second order kinetics. This requires a rate limiting step that is second order. One possible explanation for second order kinetics is the decomposition of TDMAAs via dimerisation. A potential mechanism for the decomposition of TDMAAs in the gas phase is presented below. The proposed mechanism is a chain reaction initiated by homolysis or reaction with hydrogen radicals produced during the decomposition of DMCd. Once initiated the hydrogen radicals are replenished during the decomposition of TDMAAs in steps 2 and 4.

1. $TDMAAs + H^\bullet \longrightarrow ((CH_3)_2N)_2AsCH_3N^\bullet + CH_4$

2. $((CH_3)_2N)_2AsCH_3N^\bullet + H_2 \longrightarrow ((CH_3)_2N)_2AsCH_3NH + H^\bullet$

3. $((CH_3)_2N)_2AsCH_3NH + H^\bullet \longrightarrow ((CH_3)_2N)_2AsNH^\bullet + CH_4$

4. $((CH_3)_2N)_2AsNH^\bullet + H_2 \longrightarrow ((CH_3)_2N)_2AsNH_2 + H^\bullet$

5. $((CH_3)_2N)_2AsNH_2 + H^\bullet \longrightarrow ((CH_3)_2N)_2As^\bullet + NH_3$

Bond strength data indicates that the N-C bonds are the weakest in the precursor (305 kJmol^{-1}). It is conceivable that the methyl group is removed, producing a nitrogen radical species and methane as shown in step 1. Once both methyl groups have been removed from the nitrogen (steps 2-4), the As-N bond (489 kJmol^{-1}) will break, resulting in an arsenic radical species and a stable leaving group, ammonia (step 5). The removal of the remaining dimethylamino groups will become less favourable via the same pathway as the bond strengths will increase as groups are removed despite the possibilty of stable leaving groups. This reaction pathways is

supported by a study showing that methyl radicals are not produced during the decomposition of *tris*(dimethylamino)antimony (TDMASb) [8].

Step 6 shows a reaction step proposed by Salim *et al.* for the initial decomposition of *tris*(dimethylamino) As, P and Sb species via reaction initiated by homolysis or reaction with hydrogen radicals [9].

6. $[(CH_3)_2N]_3As + H^\bullet \longrightarrow [(CH_3)_2N]_2As^\bullet + (CH_3)_2NH$

Both routes result in the same arsenic radical species with two dimethylamino groups which can then undergo dimerisation as shown in step 7.

7. $2 \times ((CH_3)_2N)_2As^\bullet \longrightarrow ((CH_3)_2N)_2AsAs(N(CH_3)_2)_2$

It is proposed that the dimerisation of the *bis*-dimethylaminoarsenic species occurs before subsequent dimethylamino groups can be removed. The proposed dimer structure is shown in figure 6.8.
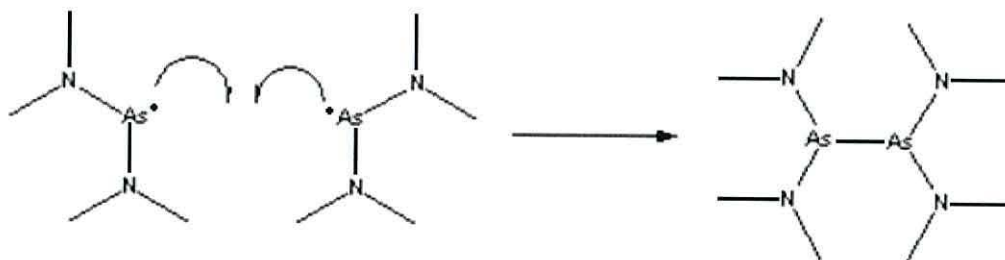

Fig. 6.8 The proposed termination reaction of two *bis*-dimethylaminoarsenic species resulting in an arsenic dimer species.

The As-As bond is stronger than the As-N bond and therefore removal of the remaining dimethylamino groups will occur more readily in an arsenic dimer species. The experimental data shows a square law dependence, indicating that the rate limiting step is second order. This indicates that for decomposition to occur a dimer has to form. The formation of the dimer is assumed to be the rate-limiting step of the decomposition of TDMAAs and the rate law for this step is shown in equation 6.3.

$$r = k\left[\left((CH_3)_2N\right)_2As^\bullet\right]^2 \qquad (6.3)$$

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The rate law in equation 6.3 shows that the rate of reaction is directly proportional to the square of the concentration of one of the reactants, which is the criteria for a second order rate law. The rate equation for the dimer formation follows this relationship and therefore provides an explanation for the experimental evidence of a second order rate law.

It is unlikely that a bulky species, such as the proposed arsenic dimer structure, adsorbs to the surface as the CdTe growth rate would be hindered by site-blocking mechanisms. The observed growth rate of the CdTe remained constant throughout this work and is evidence that a less bulky group is adsorbing to the surface. It is probable that the final species adsorbing to the surface is an arsenic dimer species (As_2) which leads to monoatomic arsenic [6]. A paper on this work entitled "SIMS analysis of intentional *in situ* arsenic doping in CdTe/CdS solar cells" has been published in Semiconductor Science and Technology [10] and is presented in appendix C.

Photocurrent spectroscopy and Electrolyte Electro-reflectance (EER) spectroscopy characterisation was carried out at the University of Bath by Dr Samantilleke, on the *in situ* arsenic doped CdS/CdTe devices with and without the $CdCl_2$ anneal, grown at the University of Wales, Bangor. Incident photons to current conversion efficiency (ICPE) data of p-CdTe devices with and without $CdCl_2$ treatment are presented in figure 6.9. Figure 6.9a produces a sloping profile highlighting that the ICPE is not consistent through the range of photon energies, which can be indicative of poor grain boundary passivation. Doping induced deep levels can be observed in the optical absorption as an increase in sub-bandgap absorption. The device structure shows evidence of a sub-bandgap response around 900nm.
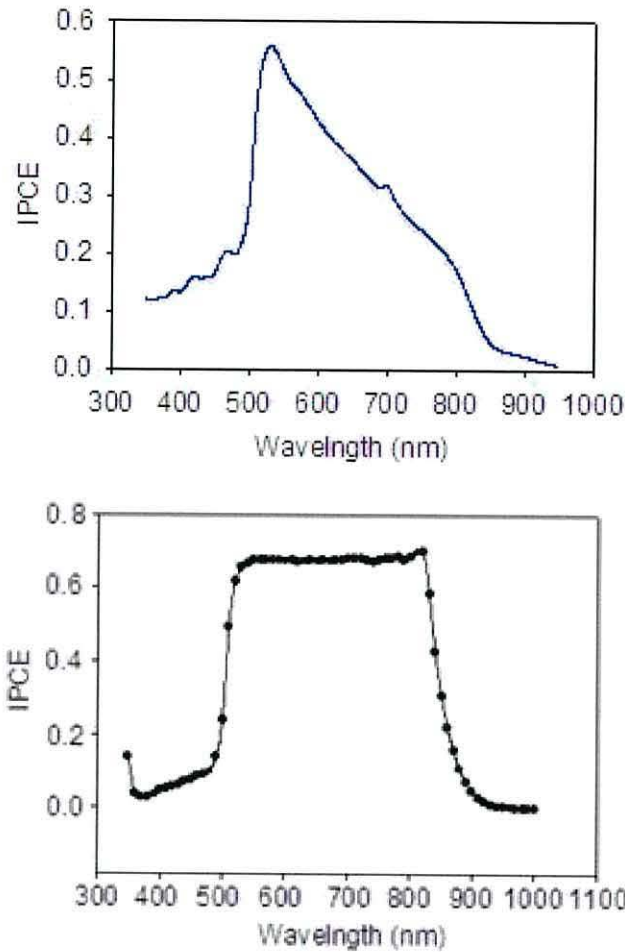
Fig 6.9 ICPE data of an in situ arsenic doped device: a) without a CdCl$_2$ anneal and b) with a CdCl$_2$ anneal.

Figure 6.9b shows a "top-hat" profile, which represents an increase in spectral response, which is attributed to the CdCl$_2$ anneal. This suggests that the CdCl$_2$ provides more effective passivation of the grain boundaries compared to arsenic alone. The sub-bandgap response is less prominent in this device. The Taguchi experiments highlighted that arsenic concentration remains an important parameter and therefore it is probable that the arsenic doping produces p-type CdTe material.

6.6 Model for Arsenic incorporation and activation in polycrystalline CdTe

The grain enlargement with temperature from the Taguchi experiments is a crucial observation as many electrical and optical properties of the material are dictated by the properties of the grain boundaries. The presence of grain growth will reduce the density of grain boundaries, altering the chances of recombination at grain boundary sites. The other important observation is that the J-V measurements show photoactive material

with arsenic doping. These observations from the third Taguchi matrix of experiments are discussed below in support of a model to explain the behaviour of arsenic within the polycrystalline CdTe layer. The model consists of the following features:

1. Arsenic predominantly segregates to the grain boundaries.
2. Only partial passivation of the grain boundaries is achieved.
3. CdTe grains are converted to p-type by the residual arsenic in the grains.
4. Higher arsenic concentration ($>2.5\times10^{18}cm^{-3}$) saturates the grain boundaries causing more arsenic to go into the grains and create compensating defects.

The majority of impurities in polycrystalline material will segregate to native defects within the material such as grain boundaries. The experimental evidence suggests that the active concentration of acceptors is $<1\times10^{15}$ atoms cm^{-3}. SIMS characterisation verified that arsenic concentrations of this order were obtained in the bulk. It is therefore plausible that arsenic will also segregate to the grain boundaries although some arsenic may also be available for substitutional doping in the grains.

Capacitance-Voltage (C-V) characterisation shows a large spectral response and confirms that p-type CdTe grains were achieved. J-V measurements of the matrix experiments also support that photoactive material is produced. Despite the large concentrations of arsenic in the bulk and the formation of photoactive material, the J_{sc} values are considerably lower than $CdCl_2$ treated material, which more effectively passivates the grain boundaries. The polycrystalline nature of the CdTe bulk will provide considerable passivation to dopants in the bulk through grain boundary sites. This often results in the effective carrier concentrations being orders of magnitude lower than the dopant concentrations. Spectral response measurements show a reduction in the quantum efficiency at longer wavelengths without Cl treatment, which is consistent with poor grain boundary passivation.

The third Taguchi matrix results for arsenic partial pressure ($T_i = - 4.62$) favoured the lower partial pressure setting in these experiments indicating that arsenic incorporation into CdTe is an optimum effect above which efficiency decreases. Therefore the higher arsenic partial pressure used in this investigation is suggested to have been saturating the grain boundaries causing more arsenic to move into the grains and create point defects that form deep level traps. The grain size becomes crucial as the ability to bring carriers generated by less absorbing long wavelengths to the junction is dependent on

carriers avoiding the grain boundaries. The higher CdTe growth temperature (390°C) investigated in the Taguchi experiments produced significant improvements to the device efficiency and produces larger CdTe grains, which reduce the probability of recombination at the grain boundaries. The presence of larger grains reduces the density of grain boundaries, but is unlikely to change the relative chemical potentials for arsenic incorporation into either the grain boundaries or grains.

6.7   Summary

A series of CdS/CdTe device structures with different TDMAAs partial pressures were grown by MOCVD to investigate the incorporation of arsenic into the bulk. The arsenic concentrations within the absorber layer were measured using SIMS depth profiling and ranged from 1×10^{16} to 1×10^{19} atoms cm^{-3}. A plot of the logarithms of arsenic partial pressure versus the logarithms of arsenic concentration in the bulk produced a linear trend with a slope of 2, indicating that above the detection limit the incorporation of arsenic rises as the square of the precursor partial pressure and therefore follows second order kinetics. The uniform growth rate is evidence that a less bulky group such as (As$_2$) adsorbs on the CdTe surface. It is proposed that the rate-limiting step is the formation of an arsenic dimer. A model for arsenic doping in polycrystalline CdTe material was proposed which stated that although p-type grains are obtained; arsenic only partially passivates the grain boundaries compared to Cl annealed material.

6.8 References

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7.0 Grain Engineering

7.1   Introduction

The Taguchi matrix experiments discussed in chapter 5 show that an increase in CdTe grain size has a beneficial affect on the device parameters. The phenomenon of grain growth is also a common result of the $CdCl_2$ treatment employed in the fabrication of the most efficient CdTe solar cells. Grain-growth in a crystal is caused by the material's attempt to minimise the excess Gibb's free energy from the presence of grain boundaries by reducing the total grain boundary area.

The relatively new field of grain engineering is focussed on manipulating the microstructures of materials to obtain desired materials properties [1-4]. Grain boundaries are the main crystal defects in polycrystalline CdTe thin films and understanding their behaviour is a major challenge. Grain boundaries are a higher energy, non-equilibrium condition compared to a single-crystal structure. Therefore any technique that applies sufficient energy to mobilise grain boundaries can initiate grain enhancement.

This chapter concentrates on engineering larger grain sizes in both the CdS window layer and the CdTe absorber layer by depositing the device structures onto a cadmium nuclei template. Although Au nanodots are commonly used as a template [5, 6], a cadmium nuclei template was the focus of this chapter as this approach would not introduce an impurity to the device structure if the cadmium diffuses into the CdS window layer.

7.2   Experimental

This section describes the growth conditions used in the deposition of the cadmium nuclei template and the deposition of the CdS/CdTe device structures. Hydrogen was the carrier gas used for both the cadmium nucleation experiments and the device structure growths, and both were deposited at atmospheric pressure onto commercially available alumino-silicate glass substrates and ITO/glass substrates from Delta Technologies Limited. The process used to texture the glass substrates is also outlined in this section.

7.2.1 Cadmium nucleation

Dimethylcadmium (DMCd) was selected as the cadmium precursor for the cadmium nucleation experiments with a partial pressure of 4×10^{-4} atm. A range of deposition temperatures from 240 °C to 280 °C were investigated based on previous work within our research group. The standard gas flows used were 4000 sccm window flow and 2000 sccm dilution flow. The substrates were placed in three different positions on the susceptor as shown in figure 7.0 to provide a direct comparison between the ITO and glass substrates and create a series of data points for each growth run.
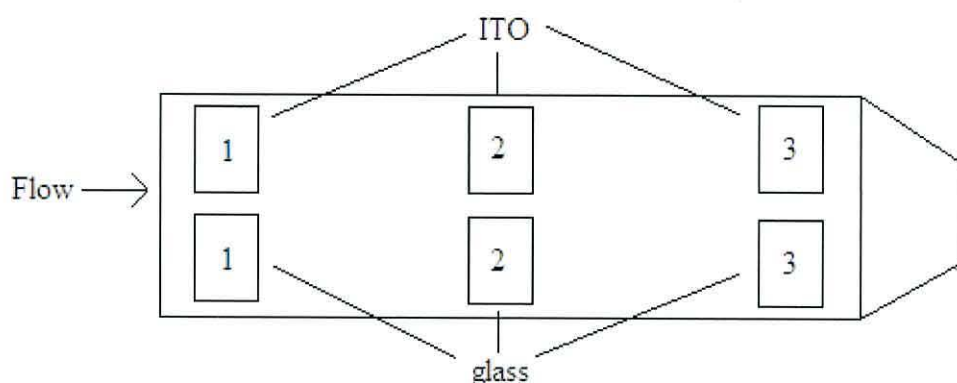
Fig 7.0 A schematic showing the three positions on the susceptor for the glass and ITO substrates.

The premise for this setup was that the two substrates will have different surface morphologies and nucleation sites, therefore one substrate may be more beneficial for cadmium nucleation.

7.2.2 Subsequent CdS/CdTe growths

The device structures deposited on the various templates were half the thickness of the optimum device structure investigated in chapter 5 to allow any templating affect to be observed more easily. The organometallic precursors used for the device structures were: Dimethylcadmium (DMCd), Diisopropyltelluride (DIPTe) and Ditertiarybutylsulphide (DTBS). A 120 nm window layer of CdS was deposited at 315 °C with a growth rate of 0.14 nm/s. The partial pressures of DTBS and DMCd were 2.7×10^{-4} atm obtaining a II:VI of 1. A 1 μm CdTe absorber layer was deposited at 390 °C with a growth rate of 0.4 nm/s. A DIPTe partial pressure of 1.1×10^{-4} atm and DMCd partial pressure of 2.0×10^{-4} atm were used resulting in a II:VI of 1.8.

7.3   Cadmium nucleation study

The deposition of cadmium nuclei was investigated on a range of different substrates as surface specificity can greatly effect nucleation. Cadmium nucleation experiments were carried out at atmospheric pressure with deposition temperatures between 250-280 °C and growth times between 5-50 minutes. The growths deposited at 270 °C all produced yellow films at the central position. Figure 7.1 shows the mixed growth phases of metallic nuclei and thin film growth.
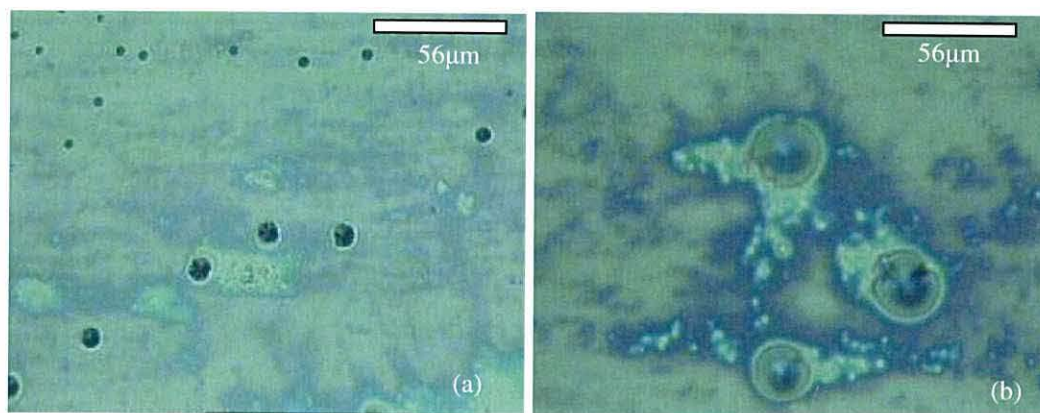

Fig 7.1 Optical micrographs of mixed phases of Cadmium nuclei and CdO on ITO/glass substrate (position 1).

The cadmium nuclei are deposited on the yellow film indicating that the growth mode adopted here could follow a Stranski-Krastonov (SK) growth mechanism, where the initial layers grow layer-by-layer, but at some point during the growth the ordered sequence gives way to the formation of bulk crystallites. The cadmium nuclei range from 5–10 μm in size, but with a poor distribution across the substrate area. The cadmium nuclei are mostly located at the corners of the substrates and at the edges where cleaning is less effective and defects in the surface are present as a result of cleaving the glass substrate.

Characterisation by XRD presented in figure 7.2 identified mixed phases of Cd and CdO. The majority of the peaks in the diffraction pattern can be assigned to the ITO substrate.
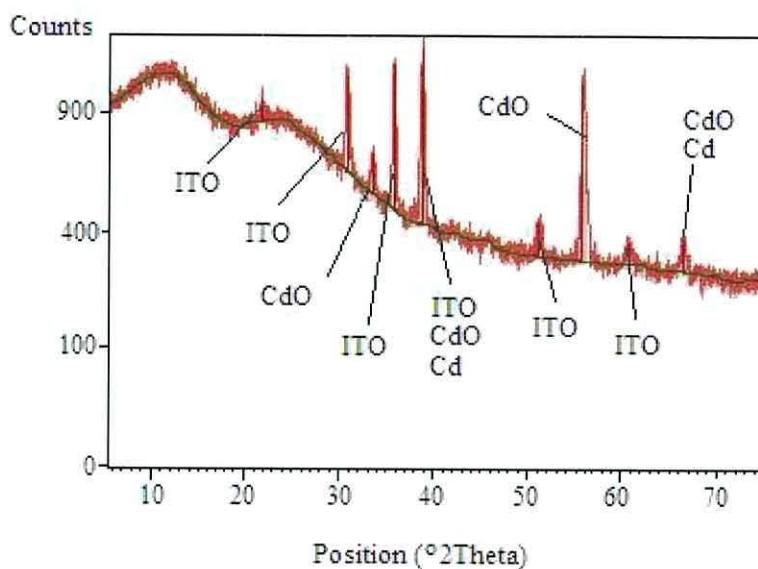
Fig 7.2 The x-ray diffraction pattern of a cadmium nucleation growth with a mixed phase of cadmium (Cd) and cadmium oxide (CdO).

Two of the peaks are assigned to CdO and two peaks could be either Cd or CdO. EDAX analysis shown in figure 7.3 confirms the presence of oxygen and cadmium in the yellow deposits confirming that the yellow growth is CdO.
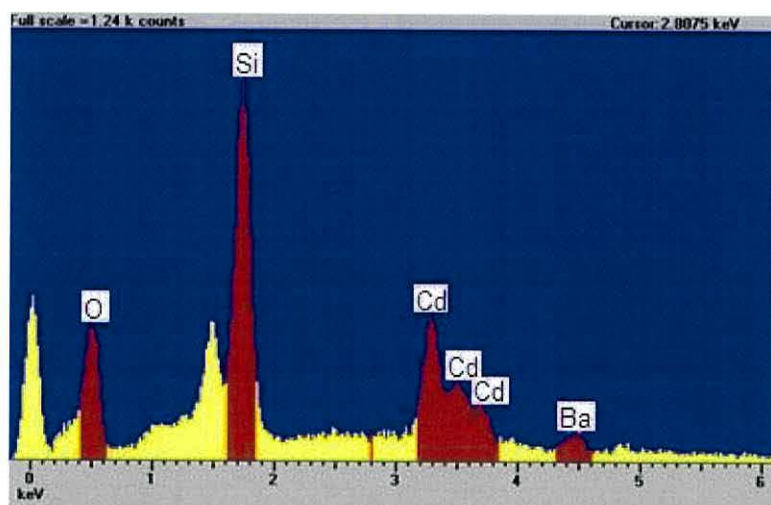

Fig 7.3 The EDAX of a cadmium nucleation growth showing the presence of cadmium and oxygen.

This evidence indicates that an initial monolayer of cadmium is deposited, which rapidly oxidise to form a CdO film and the Cd nuclei then deposit on the CdO film, indicating that a Stranski-Krastonov-type mechanism may occur for the CdO layer. This does not necessarily imply that the subsequent growth of the cadmium nuclei also follows this growth mechanism.

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7.3.1 Glass and ITO substrates

The nucleation experiments were carried out at deposition temperatures between 240-260 °C, which produced scattered areas of metallic deposition as shown in figure 7.4 with no yellow deposits. The optical micrographs show evidence of the Volmer-Weber (VW) growth mode. Bulk crystallites form as the adsorbate (Cd) does not "wet" the surface and there is no evidence of an initial layer of Cd or CdO.
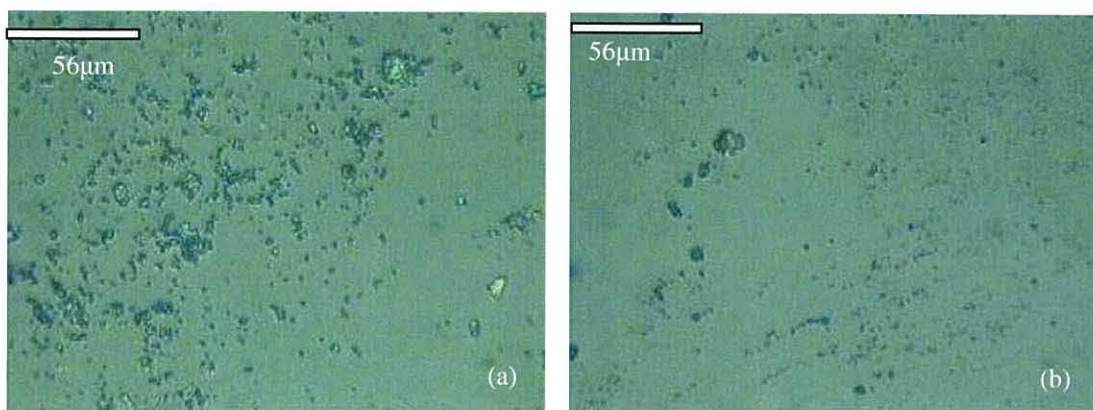
Fig 7.4 Optical micrographs showing variation in nuclei size and density across a cadmium nuclei growth.

These initial experiments to obtain cadmium nuclei resulted in a high degree of non-uniformity in both nuclei size and distribution across the substrates. The average nuclei size is ~ 2-3 μm with a density of 10 nuclei in an area of 10 μm^2. This complicated the characterisation of the material in determining whether a template effect was obtained with the deposition of subsequent layers over the cadmium nuclei. Figure 7.5 shows smeared deposition of cadmium across the edges of the substrates where cleaning was less effective.
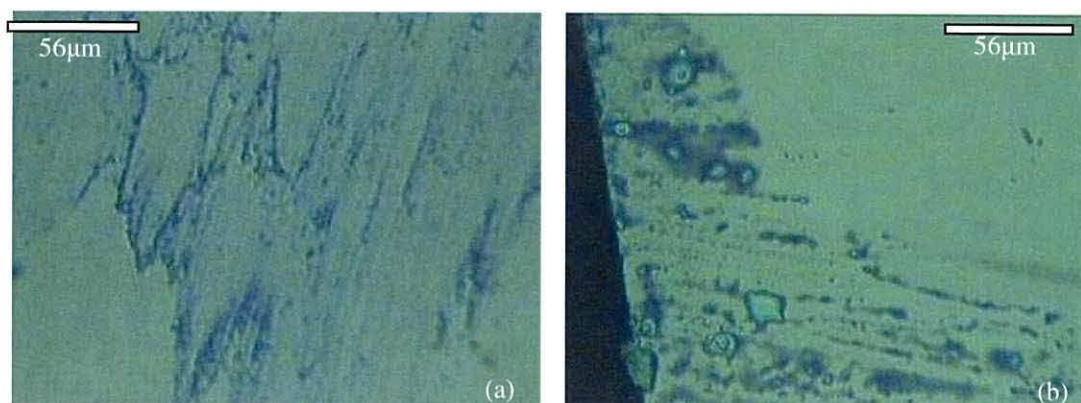
Fig 7.5 Optical micrographs showing smeared cadmium growth consistent with poor cleaning of the substrates.

Nucleation was more pronounced on the ITO substrates than alumino-silicate glass which is attributed to the increased roughness of ITO surface compared to the glass substrates. The morphology of the substrate can affect nucleation and could therefore provide a pathway to more effective control of the Cd nuclei size and distribution.

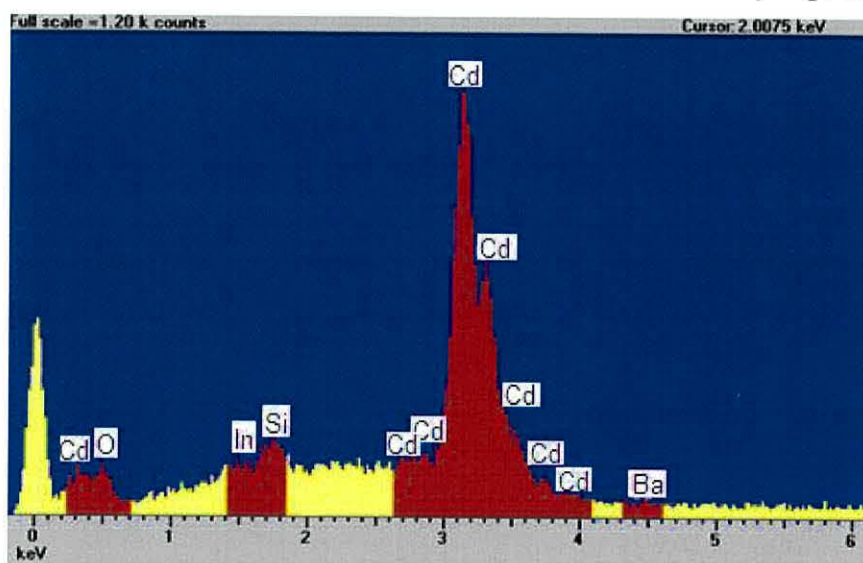EDAX analysis presented in figure 7.6 indicates a high Cd content with all other peaks negligible. This confirms that cadmium nuclei have been successfully deposited.

Fig 7.6 The EDAX of a cadmium nucleation growth showing the presence of cadmium and low oxygen content.

The lower deposition temperatures (250-260 °C) did not produce yellow deposits, which highlights that this is a temperature limited process. The oxidation of cadmium occurs readily at room temperature in the presence of air. It is unlikely that air or an oxygen source is leaking into the reactor as oxidation would occur rapidly. It is plausible that residual alcohol and oxygen species are out-gassing from the susceptor above 270 °C causing rapid oxidation of cadmium or that the cadmium is reacting with the substrate. At the lower deposition temperatures there may not be sufficient energy to allow out-gassing of residual alcohol and therefore the formation of CdO follows a temperature limited process.

7.3.2 Patterned Photo-resist

The optimum cadmium nucleation growth conditions selected from the preliminary experiments were used for the investigation of the possible beneficial effects of textured and patterned substrates. Hexagonal patterned photo-resist was supplied by Dr Vincent

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Barrioz. Optical microscopy of the patterned substrates is shown below in figure 7.7. Each hexagon is approximately 50 μm in width. The pattern is formed by etching a layer of photo-resist at the centre of the hexagon pattern, effectively leaving a web of photo-resist with hexagonal patches of bare glass substrate.
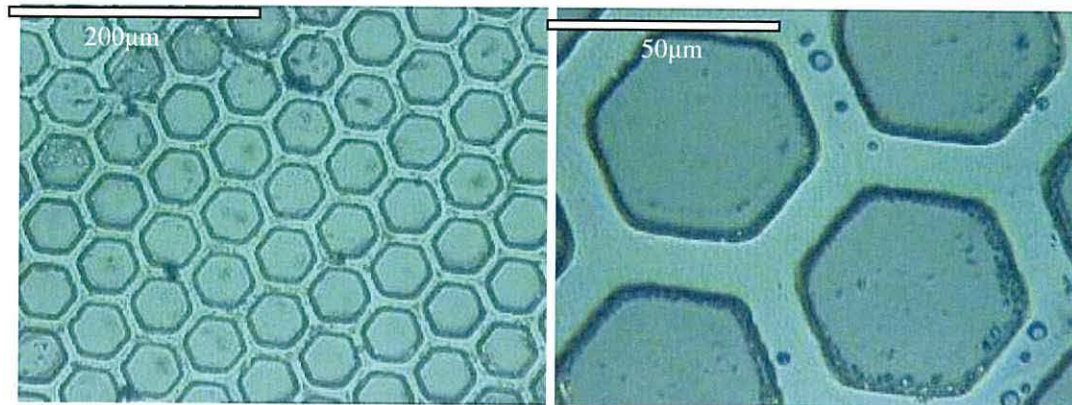

Fig 7.7 Optical micrographs of the hexagonal patterned substrate with dirt particles present on the surface despite rinsing with deionised water.

The metal-organic precursor was dimethylcadmium at a partial pressure of 4×10^{-4} atm. The deposition temperature was selected as 260 °C with a deposition time of 30 minutes. Figure 7.8 shows the hexagonal patterned substrate after the deposition of cadmium nuclei.
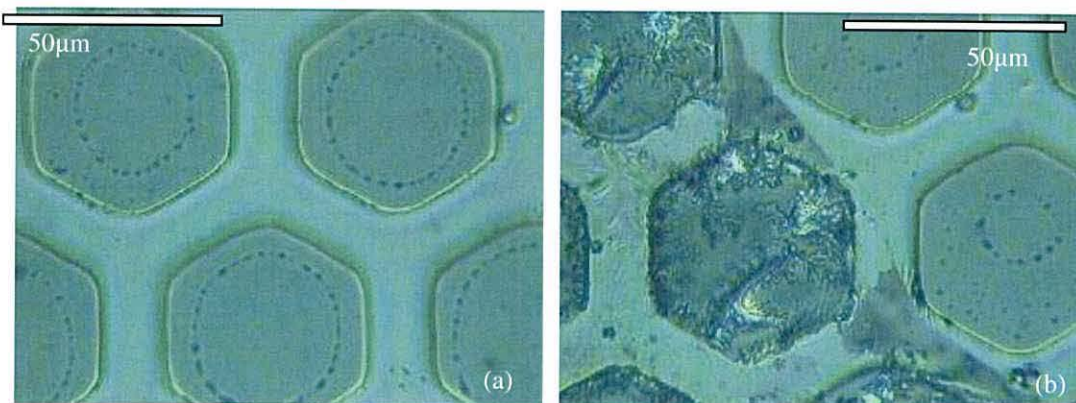

Fig 7.8 Optical micrograph of the patterned substrate showing a) ring growth of cadmium nuclei and b) feathered cadmium growth and ring growth in the hexagonal pattern.

The cadmium deposits in a ringed growth formation within the hexagonal photo-resist webbing. The nuclei are~ 0.5 μm in size with a density of 30±5 nuclei in an area of 10 μm². Figure 7.8b shows smaller rings of cadmium located near the centre of the hexagon. In Figure 7.8a the rings of cadmium nuclei are much larger and closer to the edge of the hexagon. This could be evidence that the photo-resist webbing is exerting an attractive force on the cadmium nuclei.

The regular patterned substrate does not yield a more uniform distribution of cadmium nuclei, but the ring growth within the pattern may be a pathway worth exploring as the photo-resist can be removed chemically leaving the cadmium ringed growth. This method was not explored further in the development of a uniform cadmium nuclei template due to the large amount of dirt present on the surface, which could produce misleading results as it would be difficult to determine whether templating correlated with the cadmium template or the dirt.

7.3.3 Micro-textured glass

Glass substrates were polished using two different grades of diamond polish slurries from Hyprez microtech products with 1 μm or 6 μm diamond particle size in ethylene glycol. The following process was used to texture the substrates:

- Glass substrates placed in a glass petri dish,
- Pipette slurry onto glass surface ensuring entire surface is covered,
- Use a clean piece of blue cloth and rub the slurry across the surface,
- Rinse thoroughly with deionised water and dry with nitrogen gun.

The above procedure is a crude technique, but is adequate for proof of concept in terms of texturing the surface. Optical micrographs of the textured substrates are presented in figure 7.9.
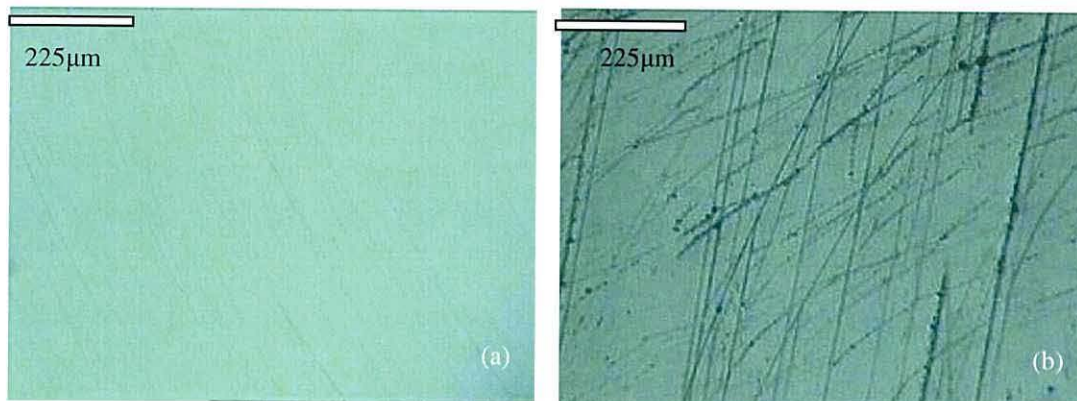

Fig 7.9 Optical micrographs of glass substrates polished with a) 1 μm diamond slurry and b) 6 μm diamond slurry.

The 1 μm diamond slurry effectively textured the glass surface with regular linear grooves into the surface. Figure 7.9b shows the glass surface polished with the 6μm diamond slurry and clearly shows a more aggressive texturing with more irregularity. The textured glass was also characterised using atomic force microscopy (AFM) as this provides improved resolution over optical microscopy and is presented in figure 7.10.
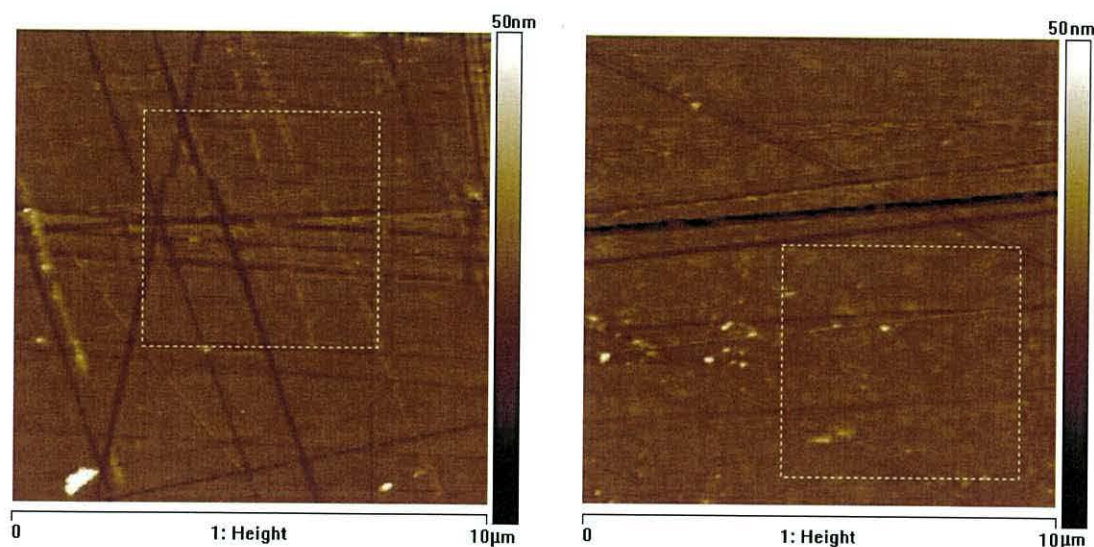
Fig 7.10 AFM images of the 1 μm and 6 μm diamond textured glass, respectively.

The 1μm diamond textured substrate shows multiple grooves into the surface with varying depths. The 6 μm textured substrate shows fewer grooves in the imaged area, but the main groove appears wider and deeper than those on the 1 μm textured substrate, which supports the observations from the optical microscopy.

To assess the affect the textured glass may have on the light capture if incorporated into a PV device UV-Vis transmission characterisation was carried out. An alumino-silicate glass substrate was used as the reference. The transmission spectra of the two textured glass samples and the reference are shown below in figure 7.11.
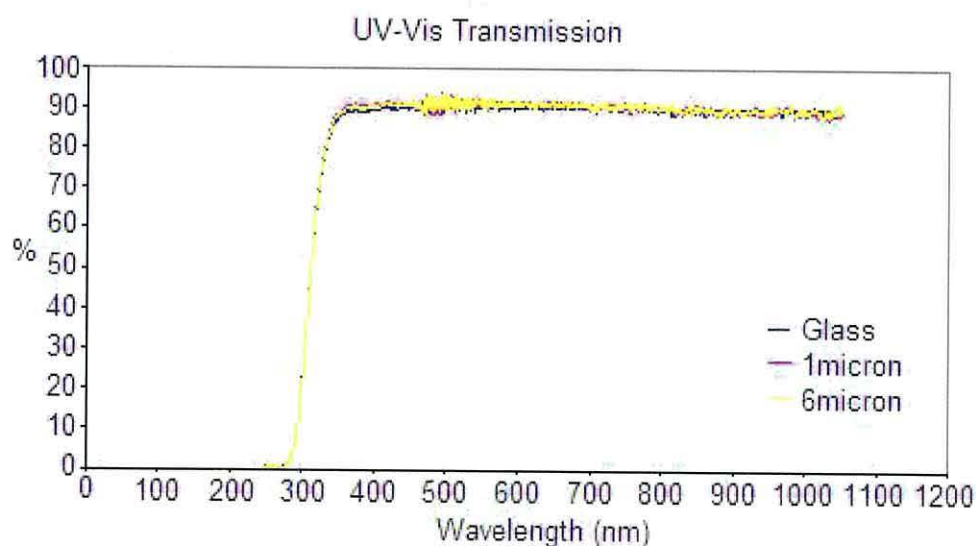

Fig 7.11 UV-visible transmission spectra of the glass reference (blue) and the two textured glass substrates.

The transmission spectrum is relatively unchanged within experimental error and therefore the effects of micro-texturing the glass substrates on device fabrication and performance would need to be explored.

The results from the nucleation study on the 1 μm textured glass substrate show a more uniform nuclei size and distribution across the substrates most likely as a result of increased surface roughness providing more favourable nucleation sites for growth to occur. Figure 7.12 shows cadmium nuclei of approximately 1 μm in size and a distribution of ~200 ± 20 nuclei in an area of 10 μm^2.
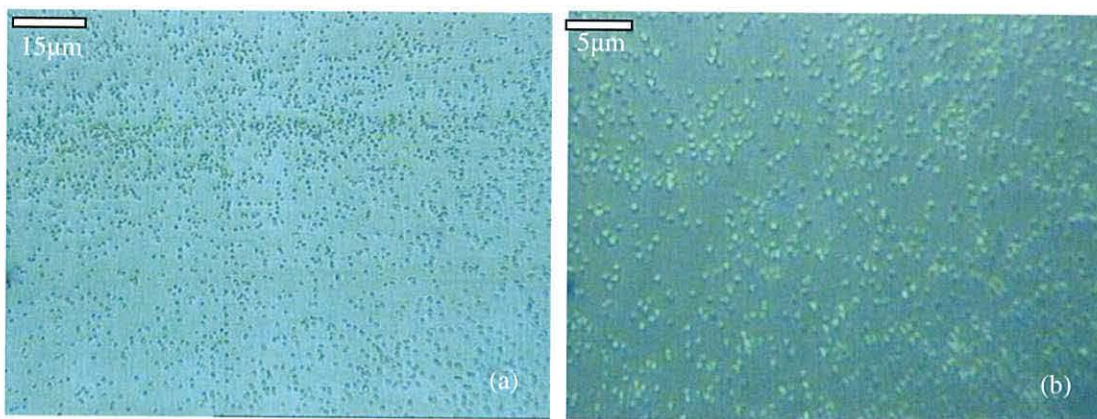

Fig 7.12 optical micrograph showing a) uniform distribution of Cd nuclei b) Cd nuclei approximately 1μm in size on the 1μm textured substrate.

This distribution was consistent across the area of the substrate unlike previous experiments where the majority of the growth was concentrated at the edges of the substrates. Individual nuclei can be clearly seen indicating the VW growth mode. Texturing the glass substrate with the 1 μm diamond slurry effectively altered the nucleation of cadmium to produce a more uniform distribution of nuclei across the substrate surface. However the Cd nuclei were considerably smaller in size (~1 μm) compared to the earlier nucleation experiments (5-10 μm). This may be due to increased nucleation sites created by the texturing and an increased sticking probability. If more of the surface sites are filled rapidly then the size of the cadmium nuclei could be limited by the growth of its neighbouring nuclei. The deposition time could be investigated to obtain larger nuclei.

The results from the nucleation study on the 6 μm textured glass substrate show a larger nuclei size compared to the un-textured glass and 1 μm textured glass, but a reduced

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distribution across the substrate compared to the 1 μm textured substrate. Figure 7.13 shows that the cadmium deposits are considerably larger than those deposited on the ITO-glass and the 1 μm textured glass substrate, but with a smaller distribution.

Fig 7.13 Optical micrograph showing growth of cadmium nuclei on a 6μm textured glass substrate.

The cadmium deposits are at various stages of growth and range in size from 2 μm to 6 μm. The density of nuclei of ~15 nuclei in an area of 10 μm^2 is considerably lower than the 1 μm textured substrate. Although there is some evidence that texturing does alter the size of the cadmium deposits there is no categorical proof that the size and density of the metallic deposits is directly related to the substrate texturing as some of the nuclei form away from the grooves in the surface. The cadmium nuclei appear to follow the VW growth mode with the formation of bulk crystallites.

In both cases the texturing procedure resulted in linear grooves into the substrate. Nucleation is effected by substrate morphology and texture and therefore it was expected that the nuclei would form along the linear grooves. The majority of the nuclei in figure 7.13 do lie along the linear grooves and for the larger nuclei a linear feature is visible across the nuclei (as highlighted in the white circles). Figure 7.14 shows the cadmium nuclei on the 1 μm textured glass. These nuclei are not aligned along the linear grooves created by the texturing.
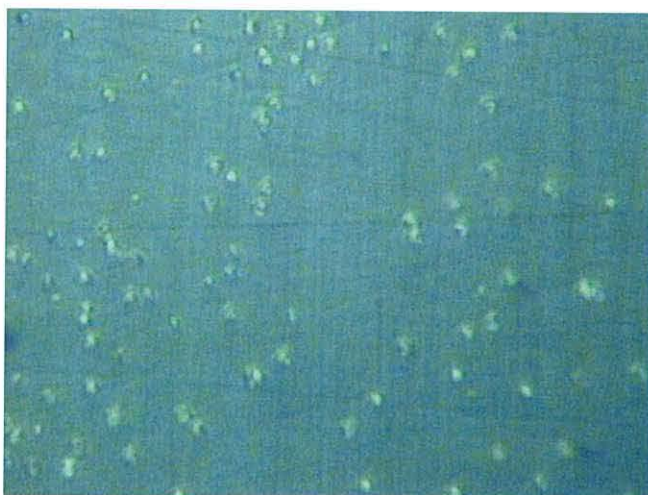
Fig 7.14 Optical micrograph of the cadmium nuclei on the 1 μm textured glass.

It is proposed that as the texturing is more uniform on this sample compared with the 6μm textured glass that nucleation is not constricted to the grooves.

7.4   The effect of different templates

This section compares the cadmium nuclei template, gold nano-structured template and a standard (alumino-silicate) substrate. The growth of CdS and CdS/CdTe onto the different templates was investigated to establish whether templating larger grain sizes in CdS and CdS/CdTe can be achieved.

The size and distribution of cadmium nuclei on the different substrates: ITO glass, textured glass (1 μm and 6 μm) and the patterned photo-resist are summarised in table 7.0.

Substrate	Nuclei size (μm)	Density ($10\mu m^2$)
Glass	1-2	10±2
1μm textured glass	~1-2	200±20
6μm textured glass	6±2	14-16
Photo-resist	~ 0.1	1280±100

Table 7.0 A summary of the cadmium nuclei size and distribution on the different substrates.

The different substrate treatments have influenced the size and distribution of the deposited cadmium nuclei. The cadmium nuclei deposited on the 1 μm textured glass was selected as the template of choice for investigation of the deposition of subsequent layers.

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Gold nano-structured template

Nanodots are often used to template other materials and may provide an alternate route to engineering larger CdTe grains [5, 6]. Gold nano-structured arrays were supplied by Tristan Temple from Southampton University to provide a comparison to the cadmium nuclei template. Figure 7.15 shows the Au nano-structured template formed by annealing Au films at 400 °C. There is a high density of nanodots across the area of the substrate.
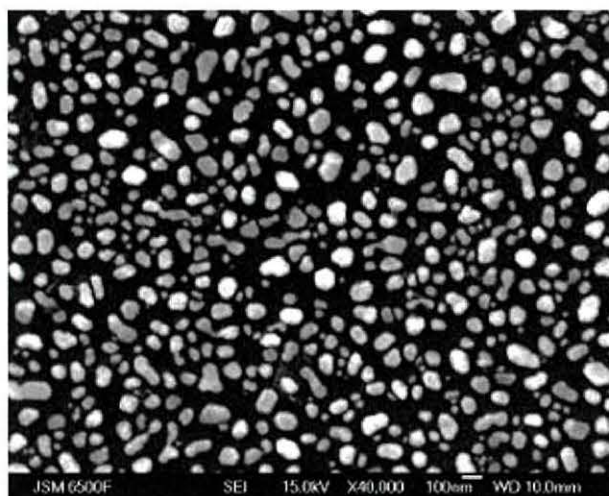

Fig 7.15 A SEM micrograph of the gold nano-structured template metallic dots of 100nm in size.

These preparation conditions were selected as they provide a good distribution of Au nanodots of ~100 nm in size (0.1 μm). The density of gold metallic deposits is 1280±100 in an area of 10 μm^2. This is a much larger density than obtained with either cadmium template, but the gold nuclei are also considerably smaller in size.

7.4.1 Cadmium Sulphide

A 120 nm layer of CdS was deposited by MOCVD at 315 °C onto the three substrates; ITO-glass, cadmium nuclei and gold nanodot array. The deposited layers were then characterised using optical microscopy, scanning electron microscopy and x-ray diffraction. The effects of the different templates on the CdS layer are discussed below.

Optical microscopy

Optical micrographs of the CdS layer deposited on the Au nano-structured template are presented in figure 7.16.
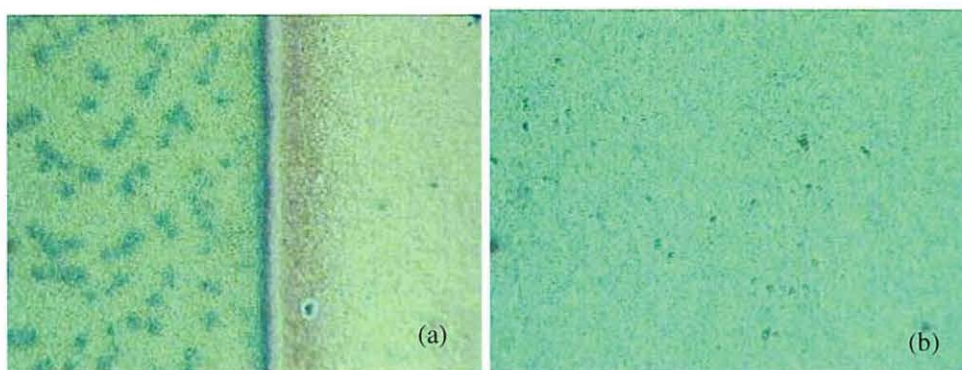
Fig 7.16 Optical micrographs showing CdS deposition onto the Au nanodot array at: a) the edge of the Au array and b) the centre of the substrate.

The dark patches visible on in figure 7.16a are the gold nanodots embedded in the CdS layer. The barrier between the gold nanodot array and the plain substrate can be clearly seen in figure 7.16 a.

X-ray Diffraction

The XRD patterns for CdS deposited on the three different substrates are presented in figure 7.17. The hexagonal form of CdS is observed with a preferred orientation along the 002 plane for each of the substrates. The diffraction pattern for the CdS layer deposited on the gold nano-structured template indicates a more random orientation than observed with the other substrates.
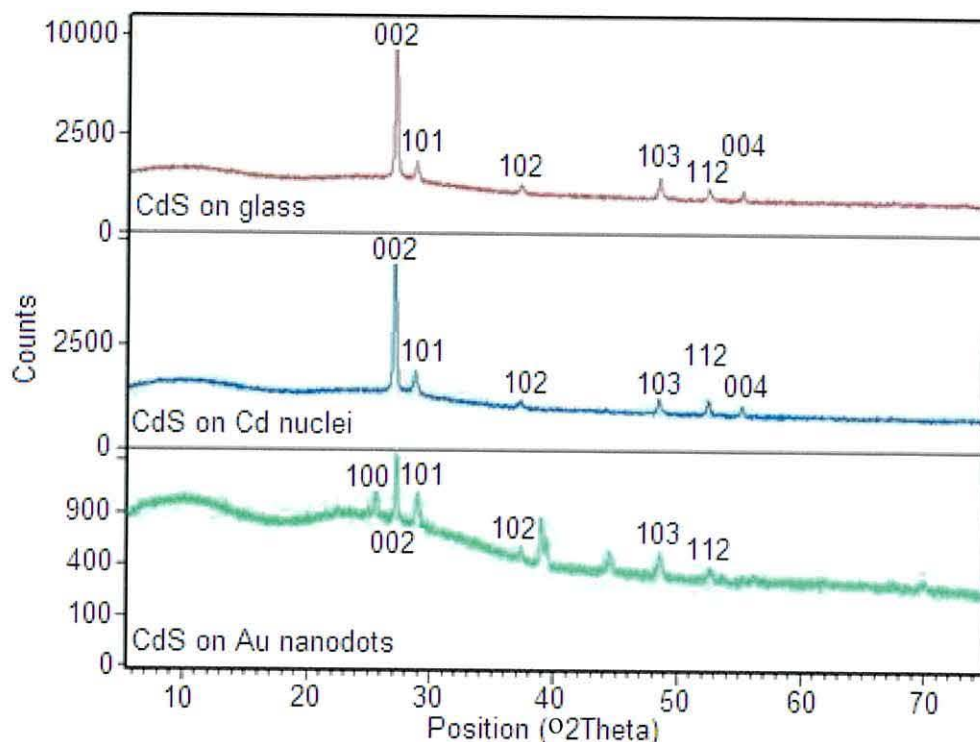
Fig 7.17 XRD patterns of the CdS layer on the three different substrates: glass, cadmium nuclei and Au nano-structured template.

Table 7.1 shows the two unassigned peaks in figure 7.17, which correlate to two planes from gold (111) and (200). The peak at 44 ° could also correlate to the (110) plane of hexagonal CdS, but this peak is not visible for the other templates. The thickness of the deposited CdS layer (180 nm) would ensure that the entire gold nano-structured template was covered and therefore these additional peaks are present in the bulk material.

Position [^{o}2 Theta]	Possible plane
39	111 Au
44	200 Au

Table 7.1 The unassigned XRD peaks for CdS deposited on the gold nanodot array.

It is possible that some of the gold may be present within the bulk material resulting in a mixed phase of CdS and CdS-Au. The optical micrographs of the CdS layer deposited on the gold template show specific areas of darker colouration which is attributed to residual gold and therefore implies that the gold is not consumed by the CdS layer.

Scanning electron microscopy

SEM of the CdS layer deposited on the three templates is presented in figure 7.18.
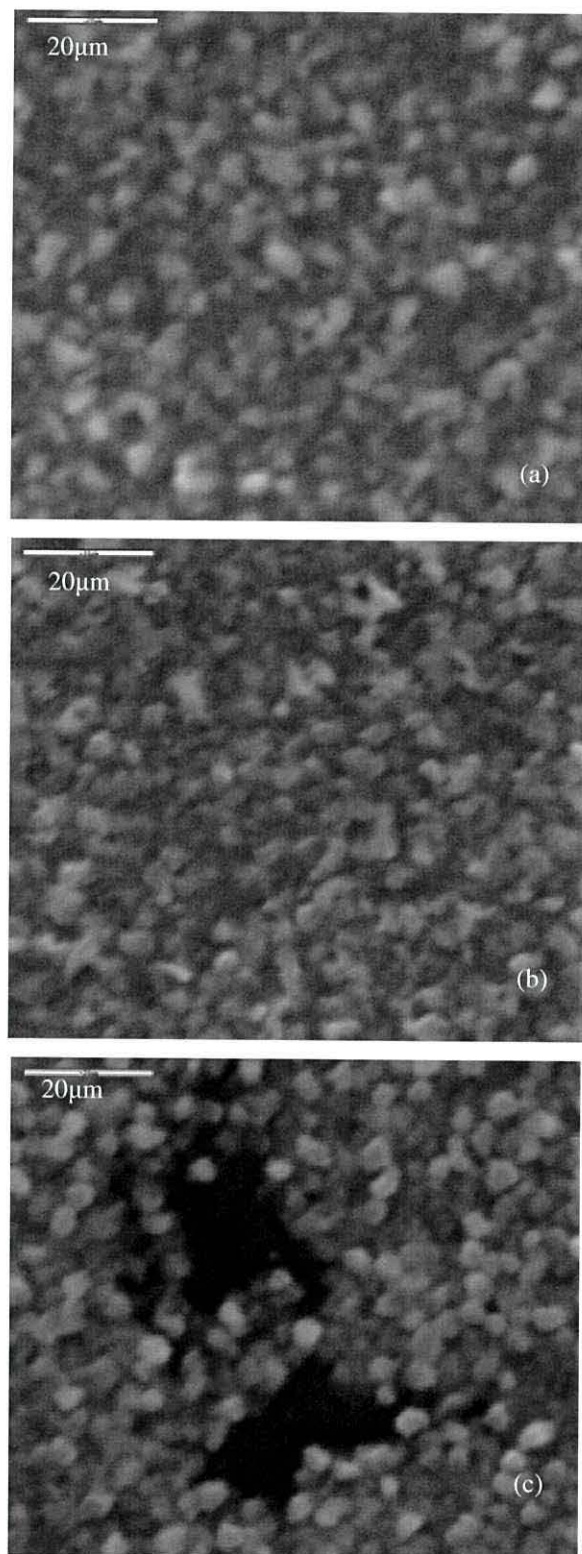

Fig 7.18 SEM of the CdS layer deposited on a) alumino-silicate glass, b) cadmium template and c) Au nano-structured template.

The CdS deposited on the Cd nuclei template has a more defined grain structure compared to the glass substrate. The CdS deposited on the Au nano-structured template shows a more spherical morphology compared to the other two substrates. There is an increase in the number of larger grains from the CdS on glass to the CdS on Cd nuclei. The CdS grain sizes are:

- ~1 μm on glass substrate.
- 1-2 μm on Cd nuclei template.
- ~3 μm on Au nano-structured template.

This is not a huge increase but provides an indication that the concept of templating larger grain sizes is feasible using this approach. The glass substrate produced the smallest CdS grain size as expected. The cadmium template showed a minimal increase in grain size, but this could not be linked directly to the template. The gold nano-structured template produced more spherical CdS grains and the largest increase in CdS grain size. This was unexpected as this template had the smallest nuclei size. The gold template had a significantly larger density of nuclei (1280±100) compared to the cadmium template (200±20) highlighting that the density of nuclei is a dominant factor in obtaining templating which may not necessarily require a large nuclei size (>1μm).

7.4.2   Cadmium Telluride

A 1μm layer of CdTe was deposited by MOCVD at 390 $^{\circ}$C onto the three substrates; ITO-glass, cadmium nuclei and gold nanodot array. The deposited films were characterised using optical microscopy, scanning electron microscopy and x-ray diffraction. The effects of the different templates on the CdTe layer are discussed below.

Optical microscopy

Optical microscopy presented in figure 7.19 confirms the presence of CdTe grains approximately 5 μm in size. Characterisation of the deposited material using optical microscopy also highlighted the occurrence of non uniform growth across the substrate including isolated large grains, areas of step growth and metallic streaks, highlighted with white circles in figure 7.19. Figure 7.19b shows an area of raised growth. This morphology is attributed to polycrystalline nucleation and the development of facets. It is conceivable that the different facet surfaces will have different growth rates and hence form different shapes.
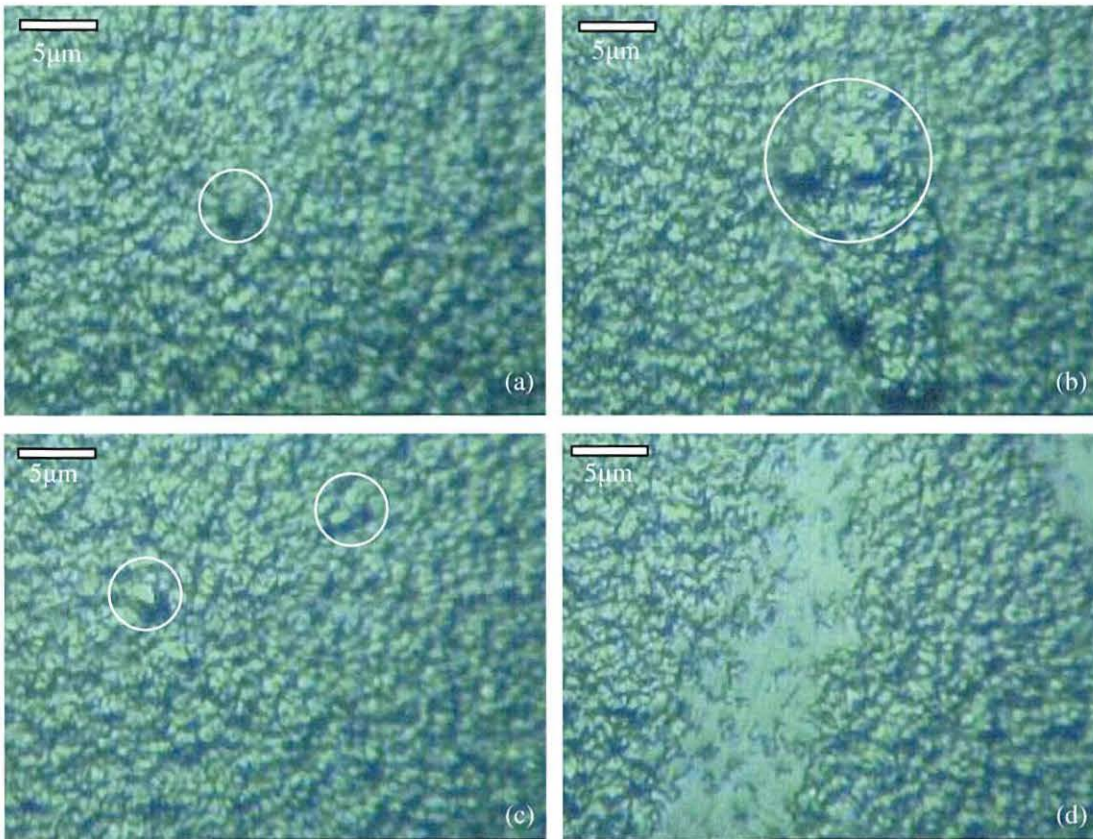
Fig 7.19 Optical micrographs of different areas on a CdTe layer deposited onto the Cd nuclei template.

The deposition of the device structure on the more uniform cadmium template did not yield conclusive results to indicate a templating affect. This has been attributed to the reduced cadmium nuclei size in the more uniform template compared to the less uniform cadmium template. The higher density of nuclei does not appear to be the dominant factor is facilitating a templating effect on the CdTe layer.

X-ray diffraction

The XRD patterns for CdS/CdTe device structure deposited on the three different substrates are presented in figure 7.20. The cubic form of CdTe is observed with a preferred orientation along the 111 plane.
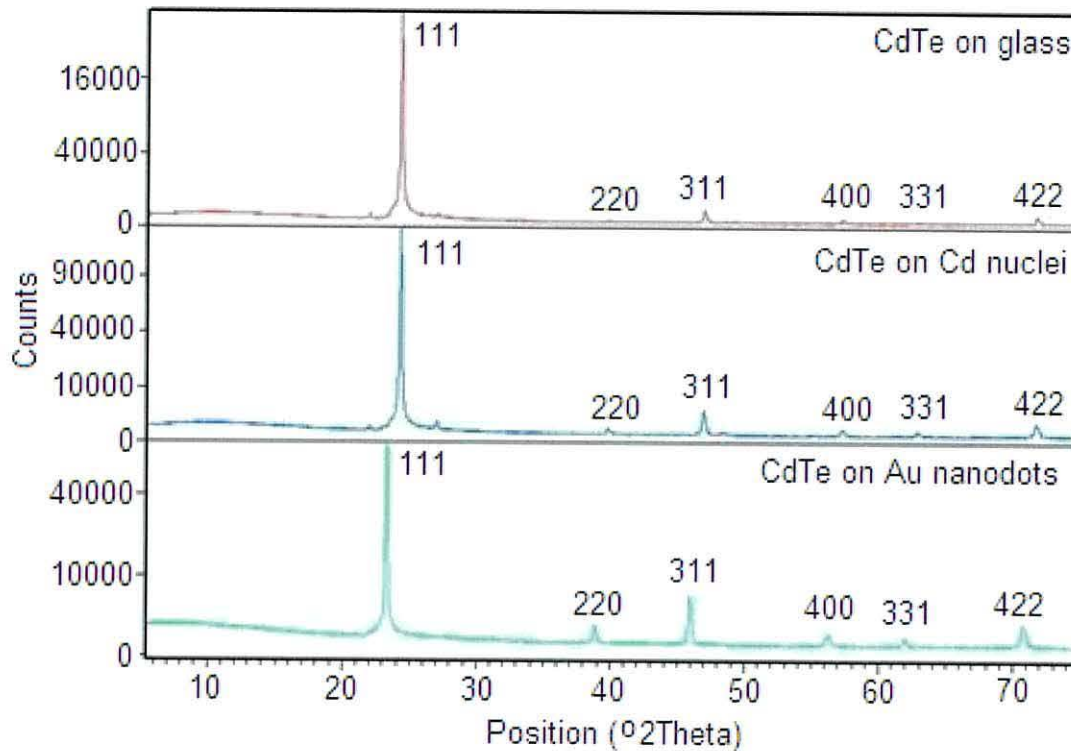
Fig 7.20 XRD patterns of the device structure on the three different substrates: glass, cadmium nuclei and Au nano-structured template.

The XRD pattern of CdTe deposited on the gold nanodot template shows evidence of a change in the preferred orientation from the 111 plane towards the 311 plane. Chandramohan *et al* observed a mixture of both cubic and hexagonal phases for CdTe deposited on stainless steel and molybdenum metallic films and suggested that the preferred orientation and grain size are dependent on the substrate. The diffraction pattern in figure 7.20 does not show evidence of a mixed phase of hexagonal and cubic CdTe, only a change in preferred orientation to the 311 plane.

This supports the observed effect of a more random orientation for CdS on the gold template. This is clear evidence that the gold nanodot template does have an observed effect on the subsequently deposited layers despite having the smallest nuclei size of all the templates. This highlights that the size of the nuclei on the template is not a dominant factor in obtaining a templating effect on the CdTe layer.

Scanning electron microscopy

SEM analysis presented in figure 7.21 identified a non-uniform distribution of areas with enlarged CdTe grains when grown over Cd nuclei template. The larger grains of the CdTe were only observed on small sections of the deposited layer most likely due to the non-uniform distribution of the Cd nuclei on the template. The CdTe grain size was calculated using the Heyn method, which yielded grain sizes in the range of 6-10 μm.
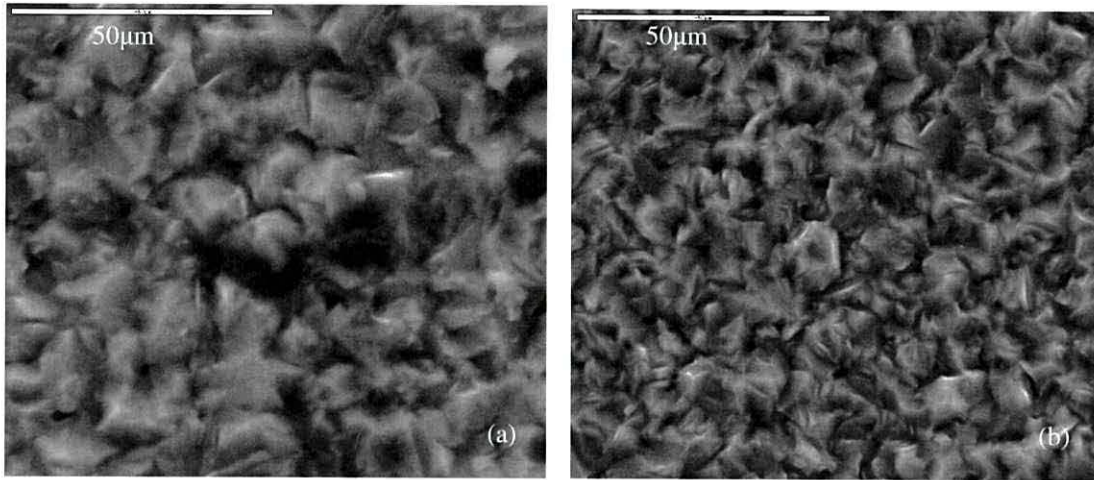

Fig 7.21 SEM of two sections of the CdS/CdTe device structure deposited on the cadmium template indicating CdTe grain growth.

SEM of the CdS/CdTe device structure deposited on the three different substrates is presented in figure 7.22. It should be noted that the scale in figure 7.22a is 5 μm, which is an order of magnitude smaller than figures 7.22b-d. SEM characterisation highlighted areas on non-uniformity in grain size. Some areas on the CdTe surface have larger densities of large CdTe grains as shown in figure 7.22b.

There is an increase in CdTe grain size between the three templates; ITO-glass, cadmium nuclei and gold nanodot array. The CdTe grain size is considerably smaller on the glass substrate (1-2 μm) compared to the cadmium nuclei and gold nano-structured templates (5-10 μm and 5-6 μm respectively). This is a significant increase but occurs in a non-uniform distribution and there is no categorical evidence that the grain enlargement is a direct result of the templates.
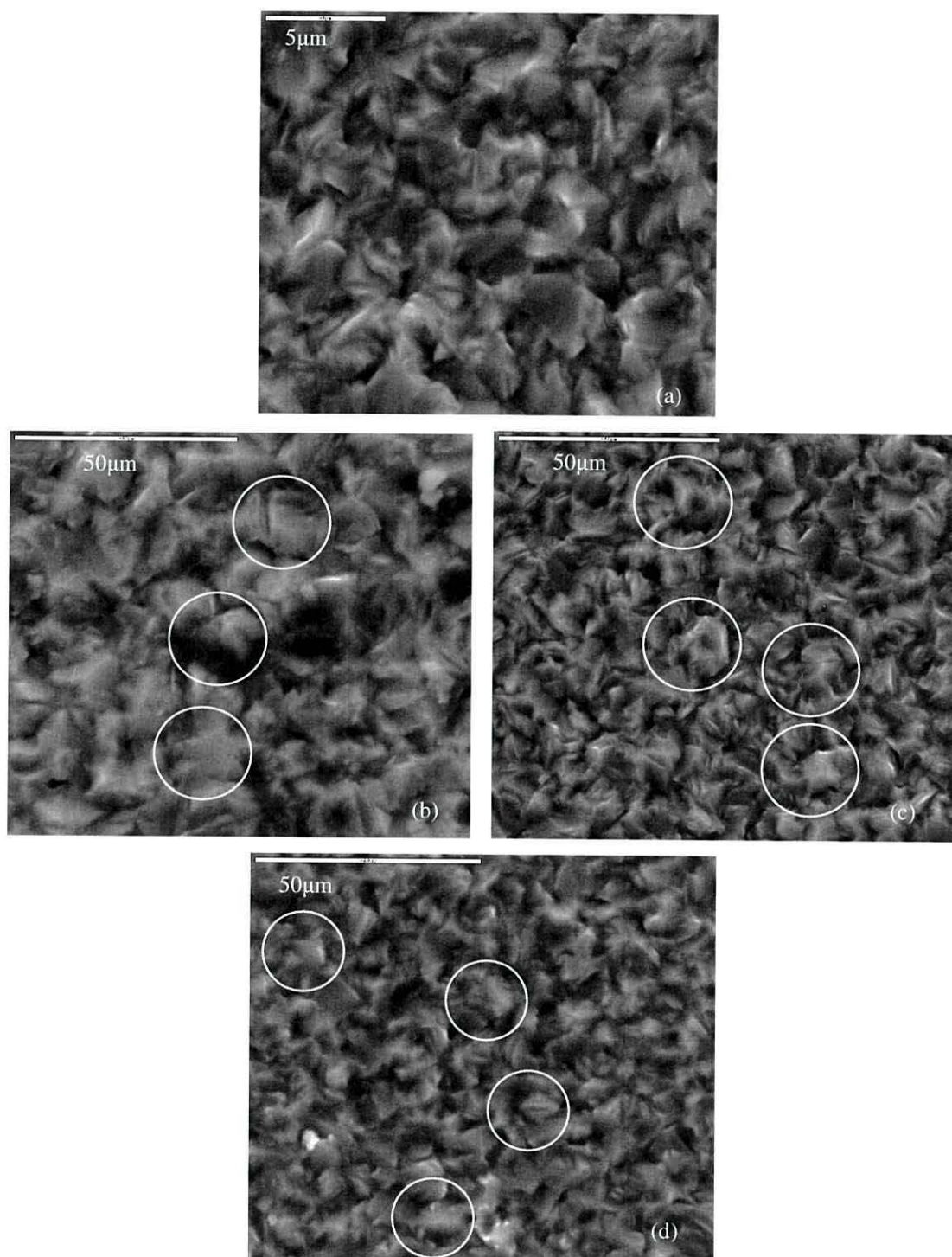
Fig 7.22 SEM of CdTe on the three substrates; (a) alumino-silicate glass, (b) and (c) cadmium template and (d) gold nano-structured template. The white circles highlight areas of larger grains.

The glass substrate produced the smallest CdTe grain size which was at the expected value of 2 μm. The cadmium template showed an increase in CdTe grain size, but this again could not be linked directly to the template as the larger grains were not evenly distributed across the substrate. The gold nano-structured template produced larger

CdTe grains compared to the glass substrate and grain sizes within the range observed on the cadmium template. There is no significant enlargement in CdTe grain size with the more uniform cadmium template deposited on the 1 μm textured glass and this is attributed to the comparatively small density of cadmium nuclei compared to the gold nano-structured template. These results highlight that the density of nuclei is a dominant factor in obtaining templating and may not necessarily require a large nuclei size (>1 μm). The gold nano-structured template altered the preferred orientation of CdTe from the (111) plane which is commonly observed for polycrystalline material to the (311) plane. The ability to alter the orientation is an interesting result as there is little evidence in the literature of the effects of orientation on the device performance; the effects of a more random orientation have not been investigated to the author's knowledge.

7.5   Summary

The effect of different substrates on the nucleation of cadmium was investigated. The use of a hexagonal patterned photo-resist template produced circular growth of cadmium in the centre of the hexagons. These results could provide a novel approach to engineering larger grains as the photo-resist pattern can be removed chemically leaving the cadmium nuclei. Texturing the glass substrate can obtain a more uniform distribution of the cadmium nuclei, but further work is needed to obtain large cadmium nuclei with a uniform distribution in order to achieve a larger templating affect, which can be categorically linked to the cadmium template. This approach has shown that increased grain size can be obtained independently of the common anneal treatments.

The gold nano-structured template also shows some promise for templating larger grain sizes in both CdS and CdTe. SEM characterisation showed that the Au nano-structured template altered the CdS morphology creating more spherical grains. XRD analysis of CdTe deposited on a gold nano-structured template highlighted a change in preferred orientation from the (111) to the (311) plane. The effect of a more random orientation on device performance has not been studied to the author's knowledge.

The use of a cadmium nuclei template can affect the grain size of subsequent layers deposited on the template, increasing grain size from 1-2 μm up to 5-6 μm. For both the CdS and CdS/CdTe layers deposited on the three different substrates (glass, Cd nuclei and Au nano-structured templates) the Cd nuclei and Au nano-structured templates both

increased the grain size, but not uniformly across the substrate area. These results provide an indication that the concept of templating larger grain sizes is feasible.

7.6 References

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8.0 Conclusion and further work

8.1 Conclusion

The design and construction of a laser beam induced current (LBIC) apparatus at the University of Wales, Bangor was discussed. The setup was largely based on the apparatus designed by Hiltner et al [1] at Colorado State University, but required several modifications. The laser diode input was connected directly to the optics setup in a vertical alignment to remove the need of beam steering mirrors, polarisers and beam choppers and this arrangement also reduced the effects of background light and reflections. The use of a pulse generator in place of the mechanical chopper could provide a pathway to improved resolution.

Initial low resolution LBIC maps clearly show an intentional X scribed into the square gold contact. The edges of the contacts were clearly defined and sharp indicating that lateral collection from outside the contact area is not a dominant factor for the investigated devices. The resolution of the setup was improved and experimental laser spot sizes were calculated using a series of line scans off a gold contact. The best experimental spot sizes achieved to date with $1/e^2$ definition were 6μm±2μm for the 658nm laser and 10μm±2μm for 808nm laser.

High resolution LBIC maps of CdS/CdTe devices have revealed complex microscopic variations in the induced current with linear defects. It is unclear whether these furrow defects correlate directly to grain boundary networks as they are larger than the grain size of polycrystalline CdTe, but this highlights that there are microscopic changes in the electrical characteristics of CdTe, which are affected by the arsenic concentration in the bulk. Understanding these microscopic non-uniformities in electrical characteristics may help to overcome the barrier to improved CdTe device efficiency deposited by MOCVD.

The Taguchi method is a useful tool in empirical investigation of MOCVD grown CdTe/CdS solar cells, but must be used in conjunction with characterisation of the device structures to understand why a particular process step is advantageous or not and

help determine why one parameter becomes more significant than another in an optimisation process. This work selected the device efficiency to be optimised and extended the approach to monitor the related device parameters; FF, J_{sc} and V_{oc} in order to help with interpretation of the matrix results. Monitoring all of the device parameters provides a deeper diagnostic investigation by highlighting which parameter has caused the overall device efficiency to change and becomes part of the subsequent characterisation of the effect of that particular parameter. A criterion for determining a threshold value for significant changes was successfully applied to the third, fourth and fifth matrix results.

The first matrix investigated the starting parameters established in earlier work and extended the investigation to include arsenic doping of the CdTe absorber layer, *in situ* CdCl$_2$ treatment and *in situ* post growth annealing. The second matrix was designed to investigate the affects of impurities observed in the first matrix. The largest benefit resulted from swapping to an alumino-silicate substrate due to a considerable reduction in impurity diffusion through the device structure. The two most relevant parameters from the third matrix were CdTe growth temperature and *in situ* arsenic doping of the CdTe layer. SEM verified that grain enlargement from 1μm to 3μm occurred when CdTe was deposited at the higher temperature of 390°C. SIMS depth profiling revealed that the arsenic concentration in the device structures was an order of magnitude greater with the higher partial pressure of 8×10^{-7} atm compared to the lower setting of 4×10^{-7} atm. The lower arsenic partial pressure was preferred, indicating an optimum arsenic concentration above which device efficiency reduces.

A series of CdS/CdTe device structures with different TDMAAs partial pressures were deposited by MOCVD to investigate the incorporation of arsenic into the bulk. The arsenic concentrations within the absorber layer were measured using SIMS depth profiling and ranged from 1×10^{16} to 1×10^{19} atoms cm^{-3}. A plot of the logarithms of arsenic partial pressure versus the logarithms of arsenic concentration in the bulk produced a linear trend with a slope of 2, indicating that above the detection limit the incorporation of arsenic rises as the square of the precursor partial pressure and therefore follows second order kinetics. It is proposed that the rate-limiting step is the formation of a dimeric arsenic species. A model for arsenic doping in polycrystalline

CdTe material was proposed which stated that although p-type grains are obtained; arsenic only partially passivates the grain boundaries compared to Cl annealed material.

The sixth matrix was an L_9 orthogonal array of experiments constructed to survey cadmium chloride layer deposition and annealing processing parameters and arsenic doping in CdTe/CdS solar cells. The dominant factor for three of the device parameters was arsenic partial pressure, favouring level 3 in each case (p.p. 4×10^{-7} atm). The anneal conditions favoured the low level settings of 10 minutes (level1) at 400°C (level1), for three of the device parameters (η, J_{sc}, and V_{oc}), indicating that a gentle anneal is required to obtain optimum conditions. A verification experiment using the selected optimum conditions produced an improved device with an average efficiency of 5.82% ± 0.38. Additional growth experiments with a $CdCl_2$ temperature of 200°C produced an average device efficiency of $\eta = 6.55\% \pm 0.73$ with the standard halogen lamp setup. The same device was tested with a class A xenon light source with an improved spectral match to AM1.5 than the standard halogen lamp setup resulting in an average device efficiency of $\eta = 10.64\% \pm 0.47$.

The use of cadmium nuclei as a template to engineer larger grain sizes in the device structure has shown potential as a grain engineering route of the subsequent layers deposited on cadmium nuclei, increasing grain size from 1-2μm up to 5-6μm without the need for a high temperature anneal step or $CdCl_2$ heat treatment. Texturing the glass substrate can obtain a more uniform distribution of the cadmium nuclei, but further work is needed to obtain large cadmium nuclei with a high distribution in order to achieve a templating affect, which can be categorically linked to the cadmium template.

8.2   Recommendations for future work

This section presents some recommendations for future work in the area of MOCVD CdTe/CdS photovoltaic devices.

8.2.1   LBIC apparatus

The LBIC setup could be used as a routine characterisation technique for the CdTe/CdS device structures and is capable of providing information on uniformity, defects and carrier lifetimes. Some specific areas of interest include:

- Identify if lateral collection occurs with the various back contacting conditions: contacting metal, etch treatment and p$^+$ layer.
- Characterisation of NP etched material, which etches toward the interface creating deep caverns in the CdTe surface.
- Characterisation to determine the role of arsenic concentration on induced current.

The observation of microscopic variations in the electrical characteristics of the CdTe material and the affect of arsenic concentration on the induced current should be investigated further as these affects have not been studied in detail and understanding these non-uniformities may be the key to overcoming the barrier to improved CdTe device efficiency by MOCVD.

The LBIC setup can be modified to incorporate a beam-splitter and photodiode to the optics setup, which can monitor the power of the laser beam incident on the device and calculate the apparent quantum efficiency (AQE) from equation 8.0.

$$AQE = \frac{I}{P} \times \frac{hc}{\lambda e} \tag{8.0}$$

Where I is the induced current and P is the power of the laser incident on the device.

8.2.2 Taguchi matrix method

The Taguchi method is a useful tool in rapidly surveying a large number of growth parameters in order to establish which growth parameters warrant further investigation. The key growth parameters highlighted in this work include:

- Arsenic concentration in the bulk.
- Deposition temperature of both the CdS and CdTe layers.
- CdCl$_2$ layer.
- II:VI of CdS and CdTe.
- Anneal temperature, time and atmosphere.

The role of Cl within the bulk material is not fully understood. SIMS analysis showed that anneal conditions altered the profile of Cl causing rapid diffusion towards the interface. The addition of the CdCl$_2$ layer does benefit the device performance but the suggested mechanisms for this are still not commonly accepted. The LBIC apparatus and other characterisation may hold the key to understanding the behaviour of chlorine in polycrystalline CdTe material.

8.2.3 Cadmium nuclei template

The initial work on cadmium nuclei templates as a pathway to engineer larger grain sizes in the device structure (CdS and CdTe) has highlighted that this approach works in principle. Further work could concentrate on establishing a good distribution of Cd nuclei whilst maintaining the larger 5-10μm nuclei size. Approaches worth exploring include: i) various substrate texturing methods and patterns and ii) the use of metal dot arrays of varying size, distribution and patterning. Another potential area of investigation is the need to establish whether the observed grain enlargement is directly related to the cadmium template.

8.2.4 Au nano-structured template

The gold nano-structured template did facilitate a minimal CdTe grain enlargement from 1-2μm to 3-4μm and also indicated an alternate orientation from the (111) to the (311) plane. An investigation into different size and density nano-structured templates may provide a clearer indication of the optimum nano-structured array for maximum grain growth in the device structures. SEM characterisation also highlighted a change in CdS morphology producing more spherical grains. These characteristics need to be explored further to establish whether this would have a positive, negative or negligible affect on the completed device. Another route of investigation involves the use of alternate metallic nano-structures templates such as Ag, In and Zn.

Appendix A

PROCEDURE FOR OPERATING THE MICRO-LBIC
[Only trained staff/students may operate the micro-LBIC]

REQUIREMENTS - CHECK BEFORE STARTING:

<u>SAFETY:</u> Laser should be fully contained within the cabinet before switching on. All devices should be handled using gloves and tweezers.

CHECK that the HP4104B unit is on, 1 hour warm-up time required. The V_A parameter should be selected (V_A LED lit). Select ⎯···· button. Set channel V_A to 0.3 V forward bias (press 0.3 and enter).

ALWAYS ensure that the scan parameters selected do not risk damage to the microscope objective!

SAMPLE SETUP

1. CHECK THAT THE LASER IS TURNED OFF

2. OPEN CONTAINMENT CABINET

3. PLACE THE DEVICE GLASS SIDE UP ON THE SAMPLE HOLDER

4. SECURE WITH THE CLIPS: Ensure the device lies flat and that the clips are outside the scan area to avoid damaged to microscope objective

5. TURN THE SAMPLE HOLDER OVER AND PLACE THE GOLD WIRE ONTO ONE OF THE GOLD CONTACTS

6. SLIDE THE SAMPLE HOLDER ONTO THE METAL RODS

7. CLOSE CABINET

ELECTRONIC SETUP

8. TURN ON THE MELLES GROIT NANOPOSITIONING UNIT: Enable both channels. The red LED's should be on

9. TURN ON THE POWER SOURCE TO THE LASER DIODE (12V DC) – Ensure cabinet is closed!

10. TURN ON THE PULSE GENERATOR: Select the square wave, 10KHz

11. TURN ON THE LOCK-IN AMPLIFIER

12. Press V_{sweep} to start voltage sweep (RED LED by digital display lit)

SETUP SCAN PARAMETERS

13. SELECT THE SHORTCUT TO THE LBIC PROG ON THE DESKTOP

14. OPEN PROJECT 1 AND PRESS ▶ : Maximise the screen

15. SELECT THE DESIRED CHANNEL SETTINGS: acceleration, max speed, min speed etc. Set channels 0 and 1 (press the corresponding set channel button)

16. SELECT THE SCAN LIMIT AND STEP SIZES: Limit / Step MUST be an integer!

17. INPUT THE DESIRED FILENAME

18. RUN THE RELEVANT LBIC SCAN: Select either AREA SCAN or LINE SCAN

19. WHEN THE SCAN IS COMPLETE the data saves automatically

20. To produce an image OPEN data file in excel, in the import wizard press NEXT, comma, NEXT, FINISH. The data should be in columns. Highlight the columns and select dplot from menu. Choose XYZ surface (area scan) or XYXY (line scan). Save image.

21. TURN OFF ALL UNITS (Lock-In, Pulse generator, DC power source, x-y stages) EXCEPT THE HP4104B: Only turn off the HP4104B if the apparatus will not be used for at least a week

22. OPEN CABINET & RETURN DEVICE TO SAMPLE BOX AND STORE AS USUAL