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Parallel Adaptive Equalizer for Alamouti-Coded Signals Recovery in Simplified Coherent PON

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***Abstract*—A simple single-polarization heterodyne optical network unit (ONU) receiver with Alamouti-coding based polarization diversity at the optical line terminal (OLT) side is a promising solution for passive optical networks (PON) beyond 50 Gbps. The special equalizer required for data recovery of such system has been demonstrated for 200 Gbps PON downstream using offline processing of serial data. In this letter, we extend such equalizer implementation with parallel processing that is required for real-time implementation. The proof-of-concept experiment for 200 Gbps downstream transmission is demonstrated to show the effectiveness of the proposed digital signal proccesing (DSP). The impact of phase noise and limitation of degree of parallelism are further investigated via numerical simulations.**

***Index Terms*—Coherent Detection, Optical Communications, Digital Signal Processing, 200 Gbps PON, Adaptive Equalizer.**

I. Introduction

THE adoption of coherent technology in short-reach and access links is a hot topic in today's research discussion [1]–[6]. Current access networks' transceivers use cost-effective intensity modulation with direct-detection (IMDD), including the recently standardized 50G-PON solutions. In 50G-PON, the operation is limited to O-band only, and DSP is added, to deal with exacerbated chromatic dispersion (CD) and bandlimited devices. Recent research works have analyzed the feasibility of 100 and 200 Gbps IMDD PON systems [5], [7], [8]. The general conclusion is that going beyond 100 Gbps using IMDD is very difficult since the reduced sensitivity and high CD and non-linear penalties make challenging to achieve the target optical path loss (>29 dB), even in O-band [5].

The use of coherent detection enables CD-compensation and improves the receiver sensitivity, thus solving the aforementioned issues. However, PON systems are very sensitive to cost, complexity and power consumption. To tailor coherent technology to these PON constraints, simplified architectures have been proposed [2]. By using single-polarization heterodyne detection and digital downconversion, a simplified coherent receiver can be constructed with only a 3 dB coupler, a local oscillator (LO), a single balanced photodiode (BPD) and one analog-to-digital converter (ADC), as depicted in Fig. 2. Such simplification comes at the expense of larger bandwidth requirements, higher ADC sampling rate and the need of a diversity technique implemented at the transmitter to make the receiver polarization-insensitive. There are different options to achieve the last requirement: Alamouti coding in two polarization tributaries [9], differential group delay predistortion, and polarization scrambling [2]. Among them, the most robust operation and better performance can be achieved using the Alamouti coding approach [2]. .

A set of DSP algorithms to recover Alamouti-coded single-carrier signals is proposed in [10], using a serial equalizer structure. Updating this DSP to a parallel version is required to enable real-time high-data rate operation, implemented in a field-programmable gate array (FPGA) or a CMOS ASIC. Recently, a real-time simplified coherent system using Alamouti coding has been reported in [11], [12]. The DSP structure is similar to [10], but the carrier phase recovery (CPR) is aided by pilot-tones. Although real-time operation with parallel DSP is stated, a description on the parallelization of the DSP algorithms is absent, as well as the penalties arising from the parallel implementation.

In this letter, we present, for the first time to our knowledge, a detailed description of a parallel adaptive equalizer to recover Alamouti-coded signals. We experimentally test its performance in a 200 Gbps PON system. Finally, we extend our analysis including numerical simulations to compute the impact of optical phase noise in the system performance for different degrees of paralellism, using 50 GBd 16-QAM format, or a future generation 100 GBd QPSK-based approach.

II. Parallel Adaptive Equalizer to Recover Alamouti-Coded Signals

The conventional 2x2 MIMO equalizer used in a standard dual-polarization (DP) intradyne receiver (RX) is not suitable for Alamouti-coded single-polarization RX. This is because redundant information is transmitted in both polarizations instead of two independent signals. The transmitter (TX) configuration is similar to a standard DP-transmitter, however, we divide a sequence of symbols into orthogonal pairs over two polarization modes. For example, if symbol-pair $[s_1\ s_2]$ is transmitted in X-polarization, in the same time slot, the symbol-pair $[-s_2^*\ s_1^*]$ is transmitted in Y-polarization [9].

An Alamouti equalizer integrated with CPR based on the least-mean squares (LMS) algorithm has been proposed in [10], with serial data processing. In this section we describe our proposed parallel implementation of the referred equalizer as shown in Fig. 1.

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The first step is separating the equalizer's input signal $x(n)$ into the even and odd symbols tributaries, $x_1(n)$ and $x_2(n)$, respectively. Each of these serial signals inputs a buffer that prepares the parallel lanes to feed the parallel processors. To describe the operation of the parallel processing, we follow the vector formulation of the LMS block equalizer presented in [13]. We start defining the vectors $\mathbf{x}_1[n]$ and $\mathbf{x}_2[n]$ as:

$$\mathbf{x}_j[n] = [x_j(n)\ x_j(n-1)\ \ldots\ x_j(n-N+1)]^T \quad (1)$$

where the index $j = 1$ identifies the even tributary and $j = 2$, the odd one; and N is the number of taps of the 2x2 FIR filters. Then, we define the matrices $\mathbf{X}_1$ and $\mathbf{X}_2$ as:

$$\mathbf{X}_j[k] = [\mathbf{x}_j[kL]\ \mathbf{x}_j[kL+1]\ \ldots\ \mathbf{x}_j[kL+L-1]]^T \quad (2)$$

where L is the bus width (i. e. the number of parallel lanes) and k is the equalizer block index (representing a complete iteration of the parallel equalizer).

The equalizer's output blocks, each composed of L signal outputs, are then obtained as follows:

$$\mathbf{y}_1[k] = (\mathbf{X}_1[k]\mathbf{w}_{11}[k]) \circ \mathbf{p}[k] + (\mathbf{X}_2^*[k]\mathbf{w}_{12}[k]) \circ \mathbf{p}^*[k] \quad (3a)$$

$$\mathbf{y}_2[k] = (\mathbf{X}_1[k]\mathbf{w}_{21}[k]) \circ \mathbf{p}[k] + (\mathbf{X}_2^*[k]\mathbf{w}_{22}[k]) \circ \mathbf{p}^*[k] \quad (3b)$$

where $\mathbf{w}_{ij}[k] = [w_{0,ij}(k)\ w_{1,ij}(k)\ \ldots\ w_{N-1,ij}(k)]^T$ $(i, j \in [1, 2])$ are the coefficient vectors of the 2x2 FIR filters, $\circ$ denotes the Hadamard product operation, and the vector $\mathbf{p}$ is defined as:

$$\mathbf{p}[k] = [p(kL)\ p(kL+1)\ \ldots\ p(kL+L-1)]^T \quad (4)$$

where $p(k)$ is a single-tap phase estimator used for CPR.

The error blocks $\mathbf{e}_1$ and $\mathbf{e}_2$, are defined and evaluated as:

$$\mathbf{e}_j[k] = [e_j(kL)\ e_j(kL+1)\ \ldots\ e_j(kL+L-1)]^T \quad (5)$$

$$\mathbf{e}_j[k] = \mathbf{d}_j[k] - \mathbf{y}_j[k] \quad (6)$$

The vectors $\mathbf{d}_1[k]$ and $\mathbf{d}_2[k]$, are the blocks of training (for initial convergence), or decided (for steady-state decision driven mode), data symbols for the even and odd tributaries, respectively, which are defined as:

$$\mathbf{d}_j[k] = [d_j(kL)\ d_j(kL+1)\ \ldots\ d_j(kL+L-1)]^T \quad (7)$$

The sequences $d_j(n)$ and $e_j(n)$, are the serial data and error signals, respectively.

Both $\mathbf{p}$ and $\mathbf{w}_{ij}[k]$ are adapted by the LMS algorithm, using the following recursions:

$$\mathbf{w}_{11}[k+1] = \mathbf{w}_{11}[k] + \mu\mathbf{X}_1^H[k](\mathbf{e}_1[k] \circ \Psi(\mathbf{p}[k])) \quad (8a)$$

$$\mathbf{w}_{12}[k+1] = \mathbf{w}_{12}[k] + \mu\mathbf{X}_2^T[k](\mathbf{e}_1[k] \circ \Psi(\mathbf{p}^*[k])) \quad (8b)$$

$$\mathbf{w}_{21}[k+1] = \mathbf{w}_{21}[k] + \mu\mathbf{X}_1^H[k](\mathbf{e}_2[k] \circ \Psi(\mathbf{p}[k])) \quad (8c)$$

$$\mathbf{w}_{22}[k+1] = \mathbf{w}_{22}[k] + \mu\mathbf{X}_2^T[k](\mathbf{e}_2[k] \circ \Psi(\mathbf{p}^*[k])) \quad (8d)$$

$$\mathbf{p}_1[k+1] = \mathbf{p}_1[k] + \mu_p\mathbf{e}_1[k] \circ (\mathbf{X}_1[k]\mathbf{w}_{11})^* \quad (8e)$$

$$\mathbf{p}_2[k+1] = \mathbf{p}_2[k] + \mu_p\mathbf{e}_1[k] \circ (\mathbf{X}_2^*[k]\mathbf{w}_{12})^* \quad (8f)$$

$$\mathbf{p}[k+1] = 0.5 \cdot \mathbf{p}_1[k+1] + 0.5 \cdot \mathbf{p}_2^*[k+1] \quad (8g)$$

where $\Psi(\mathbf{u}) = abs(\mathbf{u}) \oslash \mathbf{u}$, $abs(\cdot)$ is the element-wise absolute value of the vector $\mathbf{u}$ and $\oslash$ is the Hadamard (i.e. element-wise) division operator. μ and μ_p are the step-size parameters for the $\mathbf{w}_{ij}$ filter coefficients and phase estimator adaptation, respectively, which are independent values, and then, the $\mathbf{w}_{ij}$ and $\mathbf{p}$ adaptation is differentiated.

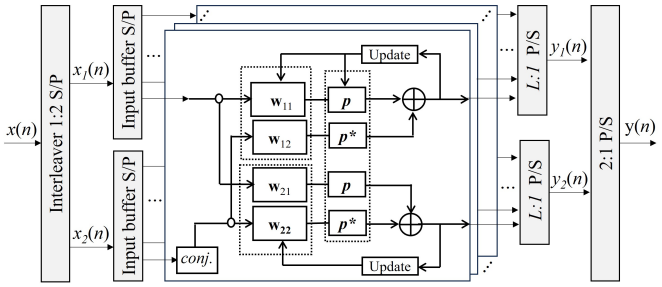

Fig. 1. Schematic of the parallel Alamouti equalizer.

Finally, the equalizer's output blocks, $\mathbf{y}_1[k]$ and $\mathbf{y}_2[k]$, are parallel-to-serial converted into the signals $y_1(n)$ and $y_2(n)$, respectively, which are combined (by symbol interleaving) to produce the equalizer's output serial signal $y(n)$.

III. Experimental and Simulation Setup

The experimental setup to test the feasibility of the parallel equalizer is shown in Fig. 2. A 200 Gbps PON system is emulated. The full details of the transmitter DSP and end-to-end transmission system can be found in [6]. At the TX, a 50 GBaud 16-QAM Alamouti-coded dual polarization [10] sequence is generated, root-raised cosine (RRC) shaped (roll-off factor of 0.01), and pre-emphasized [6] to compensate for TX impairments. The sequences are loaded into a 100 GSa/s arbitrary waveform generator (AWG), generating the driving signals of a 193.9 THz dual-polarization IQ modulator (DP-IQM). The modulated signal is then amplified using an erbium-doped fiber amplifier (EDFA), setting the launch power $P_{TX} = 11.5$ dBm (optimum value found in [6]), and launched into a 25 km standard single-mode fiber (SMF). After the SMF, a variable optical attenuator (VOA) is placed to sweep the received optical power (P_{RX}). At the receiver (RX), the signal is detected with a simplified coherent front-end composed of a 3-dB coupler, a 70 GHz balanced photodiode (BPD), and a 193.926 THz local oscillator (LO) laser having 15.5 dBm output power. The electrical signal is digitized and stored using a 256 GSa/s real-time oscilloscope (RTO) with a single 10-bit analog-to-digital converter (ADC). Then, off-line DSP is applied. First, the intermediate frequency (IF) is estimated, the signal is down-converted to the baseband and resampled at 2 Sa/symbol. Following this, the parallel adaptive equalization is performed following the methods described in the previous section. CD compensation is performed by the adaptive equalizer, since the link length is short. The number of taps N of the equalizer is 120, and the bus width L is spanned. Due to a reflection occurring in the RX, built of discrete components in our setup, the large number of taps is necessary to improve performance. However, our simulation results and experiments conducted using a single port of an integrated full coherent RX confirm that 20 taps are enough to perform the equalization

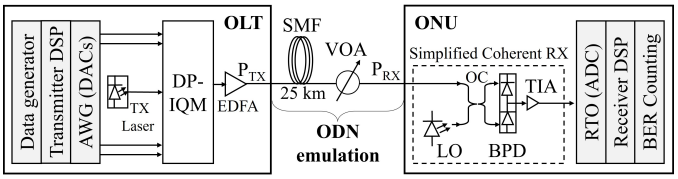

Fig. 2. Experimental and numerical simulation setup (ODN: Optical distribution network, OC: Optical Coupler, TIA: Transimpedence amplifier).

(including the CD compensation), a more suitable value for PON systems. Finally, the bit error ratio (BER) is evaluated by error counting after symbol decision.

The simulation setup emulates the experimental one. The TX and RX DSP blocks are the same as described before for the experimental setup. Both 50 GBd 16-QAM and 100 GBd QPSK sequences are generated and processed. The AWG/RTO are modelled using DAC/ADC blocks operating at 2 Sa/symbol and with 6 bits of resolution. Increasing the resolution up from 6-bits results in a negligible performance improvement [14]. The fiber is modelled through standard Manakov equations. The impact of polarization mode dispersion (PMD) is neglected. In [15], a 1-dB SNR penalty is evaluated due to 6 ps of PMD for a general Alamouti scheme. In a standard fiber, the value of PMD is 0.1 $ps/\sqrt{km}$. Thus, for a 25 km PON link, the PMD penalty is marginal (with a wide enough margin to account for statistical variations). The laser phase noise is modeled as the Wiener process with the phase noise variance given as $\sigma^2_{PN} = 2\pi\Delta\nu T_s$, where $\Delta\nu$ is the 3-dB laser linewidth and T_s is the symbol period. The components' bandwidth is set wide enough to avoid filtering penalties, assuming future technology able to support 100 GBd operation. Further details of the simulator can be found in [10].

IV. Results and Discussion

A. Experimental results

To test the performance of the proposed parallel equalizer we performed a set of experiments setting 16-QAM format and 50 GBd data rate. We measure BER curves as a function of the received optical power P_{RX}, for different degrees of paralellism, i.e. varying the bus width. The BER is evaluated after the equalizer converges and the steady state is reached, which requires around 3000 symbols. The obtained sensitivity curves are shown in Fig. 3. A couple of constellation diagrams are shown in the inset of Fig. 3, to graphically compare the performance of the serial versus the parallel equalizer with 32 parallel lanes for the same P_{RX} = -21 dBm. We then evaluate the optical power penalty with respect to the serial case, for a BER target (BER_T) of 10^{-2}, as a function of the bus width. The resulting penalty curve is plot in dashed line in Fig. 4(a).

From Figs. 3 and 4(a) we can observe increased penalty as the parallelization degree increases. This behaviour is attributed to the CPR reduction capabilities in presence of phase noise when more parallel lanes are used, which will be studied numerically and discussed in next sub-section.

A power penalty of 1.1 dB is measured when the bus width is 32. The sensitivity in this case is -22.2 dBm, thus achieving a 33.7 dB optical power budget (we remind the reader that P_{TX} = 11.5 dBm). This value fulfills the PON E1 ITU-T loss requirements (i.e. >33 dB). Therefore, a feasible operation using 32 parallel processors with a commercially available clock-speed of 3.125 GHz, is demonstrated. The clock-speed of an individual processor is obtained by dividing the serial sampling frequency by the number of parallel lanes.

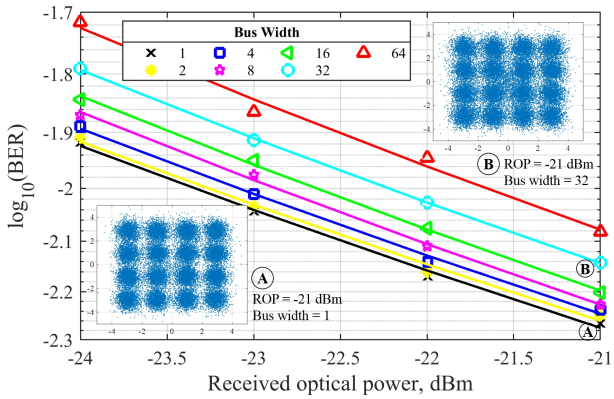

Fig. 3. Experimental BER as a function of received power for different parallel lanes, using 16-QAM (50 GBd). Inset: Constellation diagrams of two representative cases. ROP: Received optical power.

B. Simulation results

To analyse the impact of phase noise in the performance of the parallel equalizer, we performed a numerical simulation campaign. We generated BER versus P_{RX} curves for different $\Delta\nu$ values and variable number of parallel lanes. Then, we computed the power penalty with respect to the serial case, for each $\Delta\nu$, as a function of the degree of parallelism. The results for the 50 GBd 16-QAM case are shown in solid lines in Fig. 4(a). Note that the reported $\Delta\nu$ is set the same at both the TX and LO lasers. From this Figure, we can verify that the "parallel versus serial" power penalty can be attributed to the equalizer capability to handle phase noise. When phase noise is turned off (i.e., $\Delta\nu$ = 0 kHz), the equalizer performs the same irrespective of the number of parallel lanes: for up to 64 lanes, a negligible power penalty is evaluated. When laser phase noise is turned on, we observe that the power penalty increases when bus width increases, as in the experiments. Moreover, the higher the $\Delta\nu$, the stronger the performance degradation as a function of degree of parallelism. This is explained by the fact that increasing the bus width increases the equivalent symbol period of each parallel lane, making the CPR per lane less effective against phase noise [16].

From Fig. 4(a), we can observe that the simulation results corresponding to $\Delta\nu$ = 100 kHz, match well the experimental ones. Since both TX and LO lasers in our experimental setup are external-cavity lasers (ECL) having a $\Delta\nu \approx$ 100 kHz, this is a verification of our simulation models and assumptions.

The numerical simulation approach allows us to extend our analysis considering higher symbol rates, not feasible to test using our current experimental setup. The purpose of this analysis is forecasting the performance of scenarios that we envision will be feasible in the near future. We tested a 100

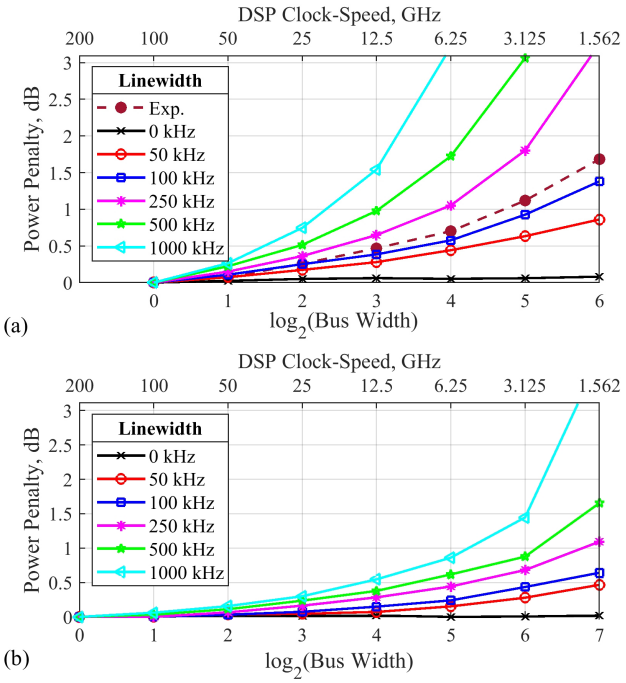

Fig. 4. Simulated (solid) and experimental (dashed) power penalty, for a BER_T=10^{-2}, versus bus width and clock-speed, for 200 Gbps transmission using (a) 16-QAM, and (b) QPSK. Different lasers linewidths ($\Delta\nu$) are set in simulations, setting the same $\Delta\nu$ at the TX and LO lasers. The power penalty is measured with respect to the serial-equalizer sensitivity for each $\Delta\nu$.

GBd QPSK transmission, thus achieving the same 200 Gbps bit rate, but using a more phase-noise resilient modulation format. The QPSK results are shown in Fig. 4(b). We can observe that the 100 GBd QPSK power penalty is significantly smaller than the 50 GBd 16-QAM one, for the same degree of paralellism. This has a double explanation. In one hand, as mentioned before, QPSK has a higher tolerance to phase-noise. On the other hand, the QPSK symbol rate is twice the 16-QAM one, i.e. the symbol period is halved. It is well known that smaller symbol periods allow a better frequency and phase recovery [16]. Note that, for the combination of parameters used here, the equalizer enhanced phase noise (EEPN) impact is negligible [17]. For instance, with a fiber length of 25 km, dispersion coefficient of 17 ps/(nm·km), 100 GBd symbol rate, $\Delta\nu$ = 1 MHz and target SNRs from 10 – 20 dB, according to [17], the EEPN power penalty is lower than 0.1 dB.

From Fig. 4(b) we observe that for QPSK a maximum power penalty of 1.45 dB is obtained when using 64 parallel processors (3.125 GHz clock-speed), and a $\Delta\nu$ = 1 MHz, which is close to that of commercial distributed feed-back (DFB) lasers. Thus, we predict that a QPSK-based 200 Gbps simplified coherent PON is feasible using cost-effective lasers.

V. Conclusions

We have presented a parallel adaptive equalizer for Alamouti-coded simplified coherent receiver suitable for real-time implementation. In a 200 Gbps 16-QAM transmission experiment over 25 km, we have demonstrated that a power budget of 33.7 dB can be achieved with 32-lane parallel processing with TX and LO laser both having a linewidth of around 100 kHz. It is also shown with numerical simulations that a laser linewidth of 1 MHz is acceptable for similar clock-speed when using 100 GBaud QPSK format.

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