DOCTOR OF PHILOSOPHY

An investigation of ultra thin CdTe solar cells grown by MOCVD

Jones, Eurig

Award date:
2010

Awarding institution:
Bangor University

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PRIFYSGOL
BANGOR
UNIVERSITY

Thesis submitted to Bangor University
in Candidature for the degree of Doctor of Philosophy

A B S T R A C T

INVESTIGATION OF ULTRA THIN CdTe SOLAR CELLS GROWN BY MOCVD
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Thin film solar cells have the potential to be an important contributor to the global energy supply by the mid-21st-century. CdTe based solar cells, achieving laboratory efficiencies of over 16 %, are highly attractive due to their near optimal band gap for conversion of the AM1.5 spectrum to electricity.

This work establishes a baseline process for CdTe solar cells grown by metal organic chemical vapour deposition, doubling device conversion efficiency to over 10 %. Work is reported towards lowering the amount of material and process steps used, particularly absorber thickness. In order to accurately control the final absorber thickness, in situ laser monitoring has been employed. This has allowed precise thicknesses to be grown, and an accurate investigation of the effect of absorber thickness with material and device performance. Several problems come about as the absorber thickness is decreased, including junction proximities (pn junction, Back contact, Conduction glass (CG)/ window layer front contact), and obtaining high layer quality and uniform thickness, which are not limited by the specific deposition method utilized (i.e. process independent). The introduction of a novel highly doped back contact layer (BCL), has been shown to lower the contact series resistance R_s of devices (from 10 $\Omega \cdot cm^2$ to 2 $\Omega \cdot cm^2$). This has allowed an all-dry process to be achieved, removing the need for any wet chemical etching.

The CdS/CdTe interface has been shown to be heavily absorbing in the blue region ($\lambda < 500$ nm) of the visible spectrum, limiting short circuit current (J_{sc}) response. To obtain maximum photocurrent, the optical band gap (E_g) of the window layer has been extended, through the use of alloying the CdS with Zn (DEZn), creating a cadmium zinc sulphide ($Cd_{1-x}Zn_xS$) ternary alloy. This has increased E_g from 2.4 eV to 2.7 eV, allowing higher transmission of ($\lambda < 500$ nm) higher energy photons to the *pn* junction, increasing efficiency to over 13 %. Results are supported by spectral response studies, and is the first reported beneficial use of $Cd_{1-x}Zn_xS$ layers in CdTe based solar cells.

It was shown that a good electron affinity (χ) match to CdTe, could be achieved for low Zn concentrations, but at high Zn concentrations (x over 0.1), junction performance deteriorated due to a positive conduction band-offset, and demonstrated an optimum Zn alloy concentration for the particular growth conditions used.

Ultra thin absorber cells (< 1 μm) do not show the classical "roll-over" behaviour at the back contact region, and has been attributed to an increased incorporated doping level. A relationship between the ZnO buffer layer and the shunt resistance is reported, improving shunt resistance for standard (2 μm) thick baseline CdTe devices, but decreases shunt resistance (lower value) for ultra thin absorber devices, decreasing performance. The closer proximity of the back contact and the *pn* junction for ultra thin devices, appear not to severely impede device performance, with only small decreases observed in the back region of the spectral response (800-900 nm).

Acknowledgements

Firstly, I would to thank my supervisor Prof. Stuart J.C. Irvine for giving me this opportunity to study towards a PhD, and for having confidence in me. His constant enthusiasm, encouragement and guidance during the PhD proved to be invaluable. Financial assistance through the PV-supergen research project/EPSRC has been highly appreciated, without which I would not have been able to complete the PhD. I also extend deepest thanks to my colleague Dr. Vincent Barrioz whose help, experience and encouragement has also been greatly appreciated and without whose assistance on maintaining the reactor, the results chapter would be empty.

Thanks also go to Dan for constant help on any topic, and whose mutual fondness of cars provided a much needed break from lab work. I would like also to mention Andy, whose presence in the lab replaced hours of silence whilst growing the devices and was appreciated. Thanks also go to Mohammed Alturkestani for assistance on data interpretation of current-volt-temperature (I-V-T) analysis of my samples, and to Dr Yuri Proskuryakov for assistance with capacitance-voltage (CV) measurements. Thanks to Will, for helping with getting an LBIC scan of one of my devices last minute.

I am indebted to my family, whose unending help and support has been greatly appreciated, especially from my mother and my brother Eilian. Finally within the school of chemistry, much appreciated assistance was given by Steve Jones, carrying out XRD scans, John Charles with designing equipment, Mike Lewis for help with computer/electronic related issues and Gwynfor with borrowing chemistry equipment. Feedback from my research committee (Prof. M. Kalaji and Dr. A. Croft) during both 1st and 2nd yearly reports proved to be very valuable.

I write this thesis in memory of my father who passed away during my final year of study.

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List of Abbreviations

$1/\alpha$	Absorption Depth
N_A	Acceptor Impurity Concentration per cm^3
E_a	Activation Energy (kJ mol^{-1})
AFM	Atomic force microscopy
AM	Air Mass
As	Arsenic
BCL	Back contact layer
$q\Phi_b$	Back Contact Barrier
E_g	Bandgap (eV)
BSF	Back surface field
k	Boltzman's Constant (eV/k)
b	Bowing parameter (XRD)
V_{bi}	Built-in Potential (eV)
ΔE_c	Conduction Band Discontinuity (eV)
IV	Current–Voltage
IVT	Current–Voltage–Temperature
CIGS	Cu(In,Ga)Se
CBD	Chemical bath deposition
W_L	Depletion Width (μm)
DEZn	DiethylZinc
L_n	Diffusion Length
DIPTe	Diisopropyltelluride
DMCd	Dimethylcadmium
A	Diode Quality Factor
DTBS	Ditertiarybutylsulphide
DC	Direct current
N_D	Donor Impurity Concentration per cm^3
DDIL	Double dilution line
N_c	Effective Density of States in the Conduction Band per cm^3
N_v	Effective Density of States in the Valence Band per cm^3
η	Efficiency (%)
q	Electron Charge (1.6×10^{-19} C)
χ	Electron Affinity (eV)
EBIC	Electron beam induced current
E_c	Energy of Conduction Band Edge (eV)
E_v	Energy of Valence Band Edge (eV)
E_F	Fermi Level Energy (eV)
υ	Frequency Of Light (sec^{-1})
FF	Fill Factor (%)
ICPE	Incident Photon to Charge Carrier Efficiency
n	Ideality Factor
ITO	Indium tin oxide

n_i	Intrinsic Impurity Concentration per cm^3
P_{in}	Input Power (W)
Φ	Ionization Potential
LBIC	Light beam induced current
I_L	Light Generated Current (mA)
V_m	Maximum Power Voltage (mV)
I_m	Maximum Power Current (mA)
MOCVD	Metal organic chemical vapour deposition
MBE	Molecular beam epitaxy
n	Number of free electrons per cm^3
p	Number of free holes per cm^3
V_{oc}	Open Circuit Voltage (mV
α	Optical Absorption Coefficient (cm^{-1})
P_{out}	Output Power (W)
εs	Permittivity of the Semiconductor, F/cm
PV	Photovoltaic
PVD	Physical vapour deposition
h	Planck's Constant (J_{sec})
QE	Quantum Efficiency
K_s	Reaction Rate Constant
I_o	Reverse Saturation Current (mA)
r_i	Refractive index
RMS	Root mean square
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
R_s	Series Resistance (Ω/cm2)
J_{sc}	Short Circuit Current Density (mA/cm^2)
I_{sc}	Short Circuit Current (mA)
R_{sh}	Shunt Resistance (Ω/cm2)
T_{sub}	Substrate Temperature (^oC)
T_{sr}	Source Temperature (^oC)
T	Temperature ($^\circ C$)
tBuCl	Tertiary Butyl Chloride
d	Thickness (μm)
TCO	Transparent conducting oxide
TDMAAs	Tris-Dimethylaminoarsine
ΔE_v	Valence Band Discontinuity (eV)
VBM	Valance Band Maximum
λ	Wavelength (μm)
W_f	Work Function (eV)
XRD	X-ray diffraction

CHAPTER 1

1.0 INTRODUCTION

The ever increasing need of humanity to consume energy at an unsustainable rate, leads to an ever increasing demand for new sources of energy. The Government's (Department of trade and industry) 2007 energy white paper [1], highlights the need for developing low carbon energy technologies and enabling a move to a low carbon economy, through the use of "*carbon capture and storage, hydrogen, advanced biofuels, solar electricity (PV), wave and tidal, and nuclear fusion*".

A recent study by Feltrin, *et al. [2]* (Fig 1.1) shows that the predicted combined energy production potential, of all current technologies, is insufficient to meet the electric energy requirements necessary for the stabilization of CO_2 emissions. The top green area represents the missing "carbon free", renewable energy necessary to meet the electricity needs of a growing global economy and population, while maintaining the 450 parts per million volume (ppmv) CO_2 agreed concentration target.

A large increase in PV generated energy (light green area), could increase the available renewable energy required for the stabilization of CO_2 emissions, but would require a rapid uptake, to make it possible.

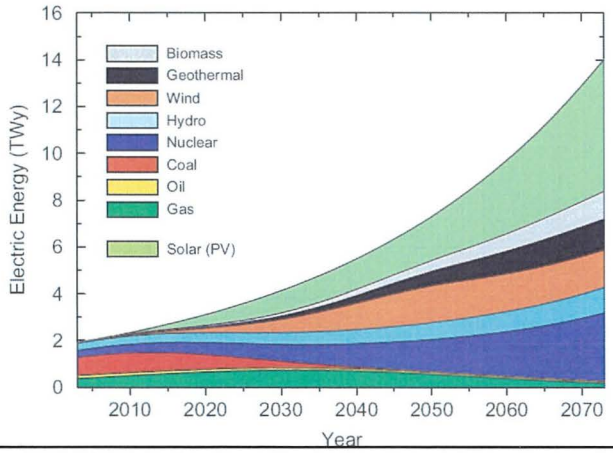

Figure 1.1: Projected electric energy production needs. after Feltrin *et al* [2].

However, the graph (Fig 1.1), does not factor in the future potential of other advances, such as CO_2 capture or storage, this assumption is appropriate given these technologies are in their infancy.

The UK is poised to reach CO_2 emission targets agreed under the Kyoto agreement, of a 12.5 % decrease in CO_2 emissions from 1990 levels by 2012. The government's own larger internal target of 20 % of 1990 levels by 2012, is not expected to be reached until after 2020 according to BBC's environment analyst, Roger Harrabin [3].

In Germany, Japan and the U.S., large financial incentives such as preferential feed-in tariffs [4], where unused solar-generated electricity is purchased back by the company at a preferential rate, have been successful in increasing adoption [5]. The tariffs are lowered each year (e.g. by 5 % in Germany [6]) to encourage more efficient production of renewable energy. In countries where tariffs have existed for years (i.e. Germany & Japan), it is becoming less financially attractive to install PV as less money is paid per kWh per year, reducing their uptake [6]. Similar feed in tariffs have been announced in the UK (1st April 2010), with 25 year programmes, where an annual 10% return will be guaranteed (http://solarfeedintariff.co.uk/).

1.1 Thesis Aims

Research within this thesis is concentrated on the deposition of a single type of thin film solar cell. The aim of this research is to investigate materials properties of CdS/CdTe based solar cells, and the effects of reducing the absorber thickness, inter-relating material properties with device parameters, towards improving understanding of limiting factors in the metal organic chemical vapour deposition (MOCVD) process.

Work in this thesis outlines the work and targets set by the PV supergen initiative towards lowering the cost of PV through process and device improvements, and the attainment of a 10% efficient thin-film device.

It should be possible for one to define optimal layer(s) conditions and properties towards optimum device performance. The problem with this approach is it requires a high level of control to make minute changes in materials properties, also a need for real in-situ monitoring

during growth exists. In-situ monitoring is advantageous as it can measure in-situ thickness, removing any reliance on estimated growth rates (G.R) or expected thickness profiles.

The CdS/CdTe device itself, can be said to have three electrical junctions, i) ITO/CdS, ii) CdS/CdTe and iii) CdTe/back contact. The relationship of performance with proximity of these junctions has not been widely described, partly due to the inability to produce the required ultra-thin material, of high enough quality not to be process limited.

MOCVD will be used to grow ultra-thin absorbers, the advantage of MOCVD is that high levels of film quality, irrespective of thickness, can be achieved allowing a comprehensive absorber layer vs. device properties to be completed.

Research will first focus on improving the device efficiency of thicker standard CdS/CdTe solar cells. A starting point of the research will be to develop a "baseline" device. This is a repeatable standard device, which allows the monitoring of the growth process, and can be used as a repeatable starting point of the research, prior to any absorber reduction investigation.

This thesis will show MOCVD as a viable and well suited technology to investigate material properties of thin film solar cells. MOCVD, due to its inherent controllability, will be used to investigate key parameters in the deposition process in a lab scale reactor, prior to its deployment to a pilot scale in-line deposition system.

Rather uniquely, this thesis will show that all required layers and post growth processes can be deposited using a single chamber [7], minimizing potential surface contamination, and decreasing production time.

1.2 Semiconductor material

The electrical properties of semiconductors arise from the covalent nature of their bonds, in which atoms are held together within the crystal. At low temperatures the individual atom's electrons cannot move through the solid crystal. As the temperature is increased, (and under the influence of an applied electric field), some valence electrons gain enough energy to escape the covalent bonds.

These 'free' electrons are responsible for the n-type (negative charge) conducting nature of a semiconductor. For every free electron created a 'hole' is left behind. These holes also contribute to the conductivity of the semiconductor. This 'hole' is filled by another electron and thus a positive hole can be seen to be moving in the opposite direction of the current. These holes are responsible for the p-type (positive charge) conducting nature of a semiconductor. This type of semiconductor is known as an intrinsic semiconductor.

Further to the intrinsic semiconductor there is the extrinsic semiconductor (of the type used in this study). The semi-conductivity in these materials arises from the presence of small amounts of impurities. Controlled amounts of these impurities are often added (doping) to a material, to enhance certain electrical properties (e.g. conductivity). Donor impurities are atoms that will replace a native atom, occupying its site in the crystal lattice.

These donor atoms contain an extra electron to the native atom they replace. This extra electron is weakly bound and can easily be ionized, forming a positive ion; the electron is then released into the conduction band. The remaining electrons of the positive ion are strongly bound, so hole (p-type) conductivity does not occur. In this case the main part of the current is carried by electrons, known as the majority carriers, and the remainder of the current is transported by holes known as minority carriers.

There are effectively three different types of imperfection which produce scattering and hence give rise to electrical resistance;

1. Ions (or more correctly phonons) in a crystal lattice cannot be thought of as occupying a stationary position. These ions are in a state of continuous thermal vibration about their equilibrium positions. Therefore at any moment in time the ions do not occupy the sites of the perfect lattice and will give rise to electrical resistance.

2. The presence of impurities incorporated within the crystal lattice gives rise to the scattering of conduction electrons. The effects of these impurity ions are greater if they are significantly larger or smaller, or if they have a different valence, to the native ions.

3. Any imperfections within the crystal lattice will act to scatter electrons. When considering a missing native atom (vacancy), the conduction electron is free to alter its direction at these vacancies; if the atoms in the lattice are thought of as containing the path of the electron. An extra native atom (interstitial) in the lattice will also act to increase scattering of the conduction electrons.

Grain boundaries are another important factor, giving rise to electrical resistance in polycrystalline thin films. The grain boundary is a zone formed at the junction between single crystals in a polycrystalline material. Impurities, increasing resistance, tend to accumulate at the grain boundary by being excluded from the normal growth of each crystal.

The grain boundary is also an area of dangling bonds; in order for one crystallite to end and another begin, it is necessary for the atoms at the edges to have unpaired electrons known as dangling bonds. Electron or hole charge carriers may be trapped by dangling bonds, and not contribute towards electrical conduction. This effect is known as recombination, and is the neutralization of free electron and hole current carriers.

1.3 Solar Cell Requirements

A solar cell, in its simplest terms, is a structure (*p-n* junction) designed to convert light into electrical current. The basic solar cell structures requirements are;

1. A volume of absorber material in which excess electron-hole pairs are generated by the absorption of light. This requires a sufficiently long path length, either by having an absorber thick enough to exceed the absorption length or by some light trapping mechanism. The absorption occurs only if the energy of the incident photon is greater than or equal to the optical band gap energy (E_g).
2. The photo-generated carriers must survive long enough to be separated, namely, carrier lifetime should be high or that the diffusion length is short. This is done through the use of moderately doped materials with low crystallographic defect densities.
3. There must be a mechanism to separate the photo-generated electron-hole pair, which can be separated by an electric field. The electric field is formed when the n-CdS and P-CdTe layers, come together and form an electrical junction. To form an electrical junction, the Fermi level of both materials must be the same, and this is facilitated by the bending of the valance and conduction energy levels. When a photon is absorbed by the CdTe, an electron-hole pair is generated, and the electrons can then travel to the n-type (i.e. negative terminal) window layers which reach the front contact.

1.3.1 The Photovoltaic Effect

The photovoltaic effect can be described as the production of a voltage between two layers of different materials when the surface is irradiated by light or other electromagnetic radiation. The *p-n* junction in the solar cell is formed when a p-type material is placed in contact with an n-type material resulting in a discontinuity in electron concentration.

The Fermi energies (E_F) of the two materials are different, in an n-type semiconductor the Fermi energy is near to the conduction band edge, whereas in a p-type material it is close to the valence band edge (Fig 1.2).

The distribution of charge at a p-n junction produces a contact potential across the junction so that the conduction band edge on the p-type side of the junction is at higher energy than that on the n-type side.

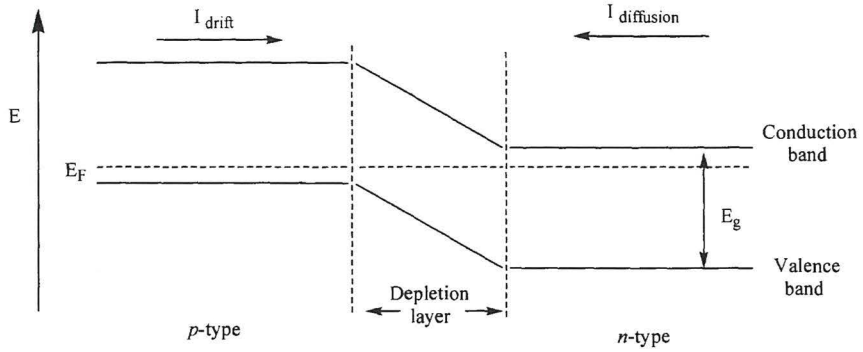

Figure 1.2: The distribution of charge at a p-n junction. After R. Turton [8]. This figure shows a simplified version of a real pn junction; see Fig 2.6 for a more accurate representation.

Initially when the two layers are placed in contact with each other, all of the conduction electrons are on one side of the junction and the holes are on the other side. The conduction electrons move about at random; some of them diffuse into the p-type material as some of the holes diffuse into the n-type material until a state of equilibrium is reached. The process is further complicated in that some of the electrons and holes can recombine with each other.

When the photovoltaic cell is in the dark, the diffusion of electrons from n-type to *p*-type (diffusion current) is in equilibrium with the electrons moving from p-type to n-type (drift current). The process of photoconductivity relies on the fact that a photon of wavelength equal to or greater than the band gap energy (E_g) of the *p*- type layer can be used to excite an electron from the valence band into the conduction band of this layer.

Once promoted to the conduction band, the electron becomes a minority carrier and is attracted across to the n-type region by the strong electric field in the depletion layer, contributing to the drift current. The drift current is now greater than the diffusion current and there is a net flow of electrons from p-type to n-type the magnitude of which is proportional to the intensity of the light. This arrangement converts light energy into electrical current and is the basis for the solar cell.

1.4 The Solar Spectrum

The solar spectrum is characterized by the air mass coefficient (AM). For analysing solar cells, only the solar spectrum after the solar radiation has travelled through the atmosphere is of interest. The spectrum outside the earth's atmosphere, is referred to as "AM0", signifying "zero atmospheres". Cells used for space power applications (on communications satellites) are characterized using AM0.

The spectrum after travelling through the atmosphere to sea level (with the sun directly overhead) is referred to as "AM1" or "one atmosphere". Solar panels do not generally operate under one atmosphere's thickness, i.e. if the sun is at an angle to the Earth's surface the effective thickness will be greater. Since much of the solar cell development is concentrated in the United States, Europe and Japan, an AM number representing the spectrum at mid-latitudes is commonly used. "AM1.5", 1.5 atmospheres, corresponds to a solar zenith angle of 48 °, and is almost universally used to characterize terrestrial solar panels. The AM1.5 solar spectrum is shown (Fig 1.3).

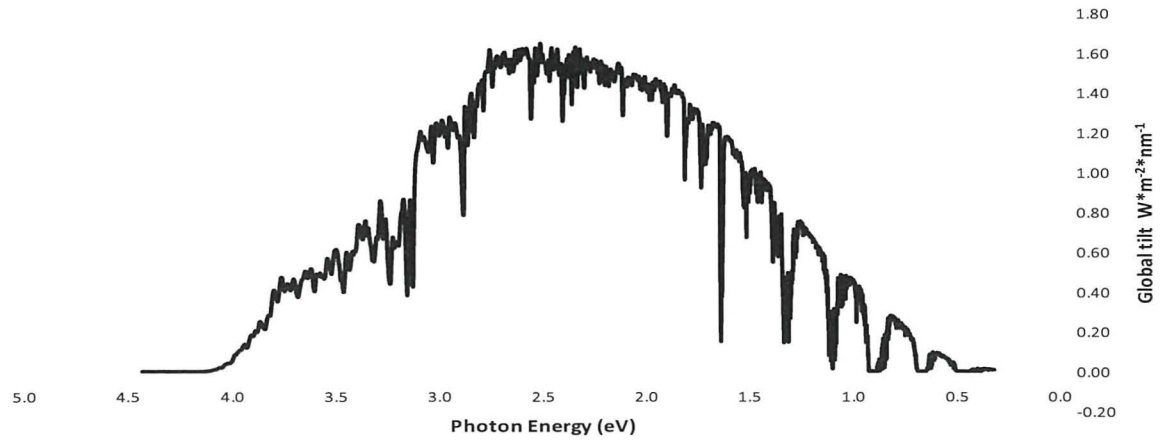

Figure 1.3: AM1.5 Solar spectrum, created using "NREL" AM1.5 data [9].

1.5 Solar Cell Technologies

1.5.1 Silicon - (c-Si)

Crystalline-silicon was the first commercially available solar cell technology, a result of the availability of high purity silicon needed for producing silicon microchips for the personal computer market. Silicon solar cells have the largest market share in PV, as it's processing and production is well understood and highly optimized after years of production. Being an in-direct band gap material for photons lower than 3.4 eV, Silicon is not an ideal material for thin-film solar cells. Despite tremendous progress in all aspects of production of Si based solar cells and the rapid decrease of production costs for PV modules from $ 5 / W_p at the beginning of the nineties to $2.55/Wp in 2004 [10]. The single most important factor in determining the production cost is the cost of the 250-300 μm thick Si wafers used. It accounts for more than 50 % of the cost of the module. Multi-crystalline modules typically have an energy payback of about 2-3 years (in southern hemisphere regions) [10].

1.5.2 Thin film solar cells

Most thin film solar cells are direct band gap semiconductors materials, which due to their higher absorption coefficients, require much less thickness to absorb most of the incident light, however, thin film silicon is also being researched. Thin film materials can be deposited on a large variety of substrates, increasing its flexibility over the single-crystal/thicker films (thin material) methods. Material utilization is also increased, with cells typically in the order of (1-5 μm) thick, increasing throughput and lowering cost. In comparison with multi-crystalline silicon solar cells, energy payback can be from as little as one year [10], at maximum insolation areas. Thin films benefit from being better suited for roof-mounted residential systems, having a lower [11] associated balance of systems (BOS); this includes structure, battery storage, regulation, control, and wiring costs. The advantage of the thin-film approach is that deposition can be done onto a substrate, allowing large area deposition, and large area cells/modules to be possible.

1.5.2.1 Amorphous / microcrystalline silicon (a-Si/mc-Si)

The advantage of amorphous silicon, over its mono-crystalline alternative is that of lower deposition temperature (as low as 75 °C). This allows for deposition on plastics, making it a good candidate for a roll-to-roll processing technique. Because a-Si:H can be doped efficiently p- and n- type, the cell structure is based on a homo-junction, where the electric field will extend all over the intrinsic layer (a result of the low doping).

As a result of the short carrier lifetime and the low carrier mobility, collection by pure diffusion of excess carriers is not very effective. Thus, the structure of the solar cell device is a p-i-n structure where an intrinsic a-Si:H layer is sandwiched between a thin n+ and p+- type layer. The properties of the material and the junction are severely affected by the Staebler-Wronski effect, which refers to light-induced meta-stable changes. These changes cause the defect density of hydrogenated amorphous silicon (a-Si:H) to increase with light exposure, causing an increase in the recombination current.

1.5.2.2 Micro-morph silicon

In micro-morph silicon, two and sometimes more junctions (each with differing band gaps) are used in a single device, maximizing the portions of solar spectrum that can be harnessed.

This allows several layers with varying optical band gaps to be combined, increasing the light capturing capability of the cell. Also, it offers the possibility, of obtaining higher open circuit voltage (V_{oc}) at the same time as working with lower current densities, so that problems with electrical series resistance are reduced. The light induced degradation (a problem with amorphous/microcrystalline Si) is also reduced, by the use of thin amorphous top cell.

The two main problems with this approach is the basic difficulty in making device grade a-Si:Ge:H intrinsic layers, with good stability and a band gap lower 1.5 eV [12]. Industrially, the first micro morph modules have been brought out by Kaneka Corp. of Japan, who have stabilized efficiencies of over 8%, and are commercially available in Japan.

1.5.2.3 Copper indium gallium selenide (CIGS)

Chalcopyrite based solar modules, uniquely combine advantages of thin film technology; (High efficiency, stability, low cost, effective use of raw materials, short energy payback time), and has a large selection of substrates, with the efficiency and stability of conventional crystalline silicon cells.

The most important chalcopyrite compounds for photovoltaic applications are $CuInSe_2$, $CuInS_2$, and $CuGaSe_2$ with band-gaps of 1.0, 1.5, and 1.7 eV, respectively. Together with related materials, they offer high optical absorption and a wide range of lattice constants and band gaps. Starting with single crystals [13], chalcopyrite based solar cells have been under investigation since 1974. Today the efficiency of lab scale thin film devices is close to 20 % [14], an efficiency comparable to the best multi-crystalline silicon cells.

1.5.2.4 Cadmium Telluride (CdTe)

The II-VI absorber material (CdTe) is the absorber of study in this thesis. It has an internal structure (grain boundaries, interfaces) and an external surface, which is intrinsically well passivated. The low recombination activity at the grain boundaries allows high solar cell efficiencies even when the material is polycrystalline with grain sizes in the order of a few μm. This is to be contrasted with crystalline Si where grain boundaries are normally characterized by a high recombination velocity.

CdTe is nearly ideally suited for solar light conversion, having a band gap of 1.5 eV, it is close to the optimum [10] black-body limit for maximum efficiency of the AM1.5 solar spectrum. Because of the higher optical absorption coefficient (higher than a-Si, and much higher than crystalline silicon), a few micrometers of CdTe is sufficient to absorb all the incident sunlight. Thus, a minority carrier diffusion length of the order of one μm is sufficient to allow all the generated carriers to be collected at the contacts, relaxing materials quality requirements. A schematic of the CdTe solar cell grown in this study is shown in Figure 1.4.

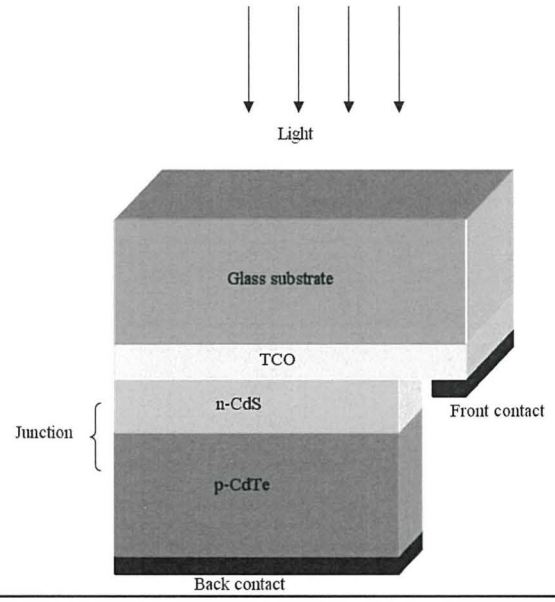

Figure 1.4: Diagram of CdS/CdTe solar cells.

For CdTe solar cells, Tellurium (a by-product of copper mining) is currently thought to be a possible limiting factor, and according to the united states geological survey (USGS), global tellurium production in 2007 was only 135 metric tons [15] .

As of 2008, the use of Cd (a by-product of Zn mining) in batteries amounted to an estimated 83% of global consumption. The remaining 17 % was distributed among: pigments, 8 %; coatings and plating, 7 %; stabilizers for plastics, 1.2 %; and nonferrous alloys, photovoltaic devices 0.8 %.

1.5.2.5 Organic semiconductors

In organic semiconductors, the absorption of photons leads the creation of a bound electron-hole pairs (excitons) with a binding energy 0.5 eV rather than free charges. The exciton carries energy but no charge, and has to diffuse to dislocation sites where their charges can be separated, and transported to the contacts. In organic solar cells, only a small portion (30 %) of the incident light is absorbed because of the majority of organic polymers have band gaps higher than 2.0 eV. The typically low charge-carrier and exction mobility require the active absorber layer thickness to be less than 100nm.

This thickness is sufficient to absorb almost the entire incident light if light trapping is used. However, problems including stability of the conjugate polymer and the matching of the band gap of the organic materials with the solar spectrum have so far limited large improvements in efficiency.

1.5.2.6 GaAs

The first GaAs heterostructure solar cells were created by the team led by Z.Alferov [16] in the USSR in the 70's. Later, dual- and triple-junction solar cells based on GaAs with germanium and indium gallium phosphide layers were developed, as the basis of a triple junction solar cell.

GaAs has some electronic properties which are superior to those of silicon. It has a higher saturated electron velocity and higher electron mobility. Another advantage of GaAs is that it is a direct band gap material, allowing it to emit light efficiently (which is why it is popularly used in LED's). It can be grown by grown using molecular beam epitaxy (MBE) or using metal-organic vapour phase epitaxy (MOVPE). Its band gap of 1.43 eV, make it nearly ideal for single-junction solar cells. Its high absorption coefficient, means only a few microns thickness is needed. Unlike silicon cells, GaAs cells are relatively insensitive to heat (ideal for concentrator systems).

1.6 Extremely thin absorber solar cells (ETA)

A highly structured substrate can substantially reduce the transport path for charge carriers in the absorber, and at the same time, increase the optical path for photon absorption [17]. The use of nano- and micro-structured substrates for a new type of cell with extremely thin absorber have been widely studied [18].

Since photo-excited electrons and holes have to be transported across the absorber to the contacting layers, a locally reduced absorber thickness significantly improves the collection probability. Typically for ETA cells, a highly structured transparent substrate layer is deposited on a conducting glass substrate. This layer is covered by a thin absorber layer. A void-filling transparent conductor and/or a reflecting metal layer is used for the back contact. Work with ETA films is relatively new, and higher device efficiencies have not yet been reported.

1.7 Fundamental Limits to Solar Energy Conversion

A solar cell (a black body) at 300 K, has physical limits to energy conversion. Landsberg and Baruch [19] states that the Carnot conversion efficiency limit can approach 94%. However, efficiencies of this magnitude cannot be achieved in real devices because of the "Shockley-Queisser" efficiency limit.

Shockley and Quessier [20], reached their theoretical maximum conversion efficiency by assuming that each photon above band-gap gives rise to just one electron-hole pair, while all photons with energy below the band-gap are lost due to thermalisation and transmission losses. This accounts for about half the energy loss. These losses are inevitable when a single band gap is used to convert a wide range of the solar energy spectrum.

If we compare the maximum obtained lab efficiencies (Fig 1.5), to the maximum calculated possible efficiency, for a given semiconductor band gap at AM1.5. IT is observed that only c-Si and GaAs are close to their maximum limit. The large gap from the maximum possible for both, CdTe and a-Si, demonstrates the lack of knowledge and understanding towards producing high efficiencies with these materials. This demonstrates the need for further fundamental studies in order to increase understanding of device physics, and performance of these devices.

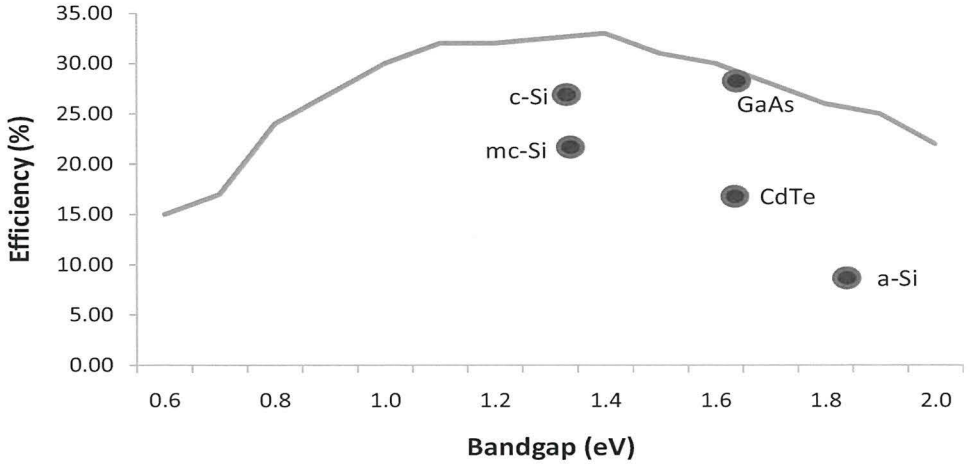

Figure 1.5: Highest reported lab efficiencies for various solar cell materials. Here, the blue line represents the Shockley-Queisser limit.

1.8 Towards decreasing the cost of PV modules

In order to decrease the cost of thin film solar cells, the current cost of production needs to be identified and understood. Bonnet [21] has created a cost model of large thin film PV manufacturing (Fig 1.6).

The model shows that at high production volumes material costs dominate. This is therefore a major area where research efforts should be focused. The €/W cost could simply be decreased if the conversion efficiency of the module itself was increased.

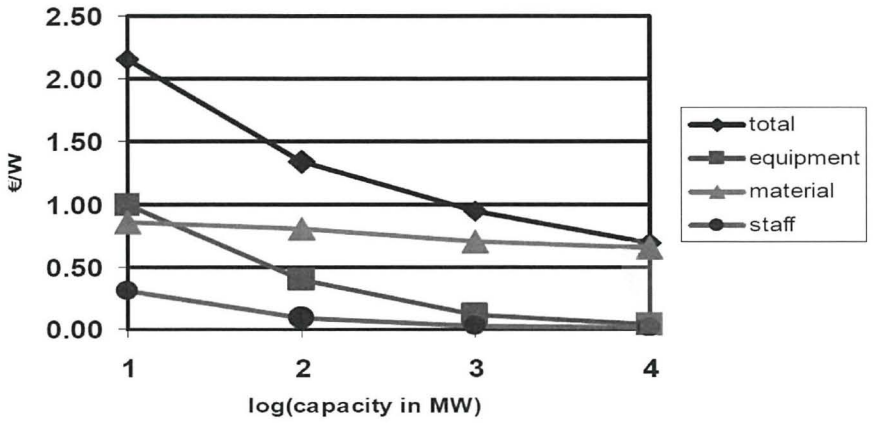

Figure 1.6: Predicted cost model of thin film PV production plant. **[21]**

Cost saving due to materials can be demonstrated by a simple example. Given a CdTe module layer thickness of 3 μm. It can be said that approx. 9 g/m^2 of Cd or Te is present by weight, using current manufacturing methods [22]. At 10% efficiency, one gigawatt (GW) can be said to require 7.32 km^2, or 66 tonnes. However, due to the large absorption coefficient of CdTe, only about 1 micrometre thickness [23] is needed to absorb 90% of the available spectrum. If the CdTe absorber layer is reduced to 500nm, six times less Te per gigawatt (11 tonnes/GW) would be required. This example demonstrates a large material cost saving that is possible, merely by decreasing the absorber layer thickness of the layer if the same efficiency can be achieved, and is a good example of why decreasing the absorber layer thickness is a valid research area..

Recently [24], thin film PV deposition technologies, have been able to lower the production cost of thin film solar cell modules prices lower than established mc-Si modules. This has led to a large increase in the production of thin film PV worldwide, and especially CdTe thin film, with the largest increase in CdTe production due to operations by First Solar [25] in the U.S.

Thin film solar cells currently share 18% of the PV market (SolarBuzz 2010). The expected "thin film" successor to established silicon solar cells, ought to have been copper indium di-selinide "CIGS", given its higher efficiency (Record efficiency of 19.9 % (modules only ca. 12%) [26]). But, the added complexity of controlling the diffusion parameters of up to four separate elements (Cu, In, Ga, Se), compared to just two species with CdTe, and the limited size of its modules is thought to have limited its use in large scale production (Outcome of discussion regarding "future of thin film production" at EMRS conference Strasbourg May 26-30 2008 - Symposium L).

1.9 Research Introduction

Firstly, the precise level of control and monitoring available needs to be assessed towards an understanding of the layer quality and end device performance, before layer thicknesses can be decreased.

When reducing the absorber thickness, it is not known whether the proximity of the main *pn* junction to the back contact will become an issue. It should also be noted that identification of these individual junctions in real devices will be increasingly difficult as they all must exist in a working device.

It is also not known, whether the number photons reaching the absorber layer can be increased. A number of approaches will be investigated, which includes increasing the optical band gap of the window layer.

Once a baseline device, with adequate conversion efficiency performance has been identified, *in situ* laser interferometry will be used to monitor and reduce absorber layer thickness.

Decreasing the CdTe layer thickness towards the CdTe absorption limit (1μm) termed "ultra thin", will allow an investigation of the limitations (i) of the material and (ii) and of the particular MOCVD reactor used in this study.

Chapter two provides a survey of the relevant current and historical literature in the field of MOCVD and in particular advances in thin film CdTe solar cells.

Chapter three describes the experimental techniques used and gives detail on the equipment, chemicals and analysis performed, along with details of the particular MOCVD system used.

Chapter four and five sets out a detailed results, and discussion, of the research. The thesis concludes with chapter six, where the main achievements and further possible research are reported. A published paper is also included in the appendix.

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CHAPTER 2

2.0 BACKGROUND LITERATURE

2.1 Comparison of PV technologies

In 2004, the American national renewable energy laboratory (NREL) [3], funded a study entitled: "Study of Potential Cost Reductions Resulting from Super-Large-Scale Manufacturing of PV Modules", where a comparison of the current available thin-film technologies and their associated costs were reported (Table 2.1).

Table 2.1: Calculated thin-film production costs [3].

Technology Approach	a-Si	CdTe	CIGS
Total panel price per W_p ($)	$0.60	$0.42	$0.52
Total installation price per W_p ($)	$0.40	$0.33	$0.36
Total price per W_p installed ($)	$1.00	$0.75	$0.88

It can be observed that thin-film CdTe, already outperforms CIGS and a-Si on a cost per watt basis. The advantages of lower cost thin film solar cells, compared to typical c-Si cells, has led to several thin-film deposition techniques to emerge. Each of the thin-film techniques have their own advantages, with the most common up-scaled and industrially selected techniques chosen for their growth speed over quality of the grown layers. The next section will cover some of the deposition methods that can be used to specifically deposit thin-film CdTe.

2.2 Thin-film CdTe deposition methods

2.2.1 Close spaced sublimation (CSS)

CSS uses a sublimation technique to deposit semiconducting layers onto a substrate. One of the largest users of this technique is Antec (based in Germany). Both the CdS and CdTe can be deposited using CSS. Approximately 0.1-0.2 μm of CdS and approx. 5-10 μm of CdTe are deposited sequentially [4]. The source and the substrate are placed at a short distance of each other (1 mm to a few cm, depending on the size of the substrate needed to coat) in a rough vacuum (10^{-3} to 10^{-2} mbar). The source is heated to a high temperature (> 500 °C). As a source, one can use CdTe in the form of a pressed tablet, or in granulate or powder form. A stoichiometric mixture of Cd and Te powder can also be used. The driving force for the deposition is the source to substrate temperature difference, and the surface energy at the substrate, which can depend on the substrate composition, crystallography and morphology.

In Figure 2.1, a sketch of a batch CSS deposition apparatus is shown. This technique has many variants, e.g. an inert carrier gas, Ar or N_2, can be used at pressure of e.g. 1 mbar, or at atmospheric pressure. This form of the sublimation technique is sometimes called close spaced vapour transport (CVT or CSVT) and of the type used by First Solar.

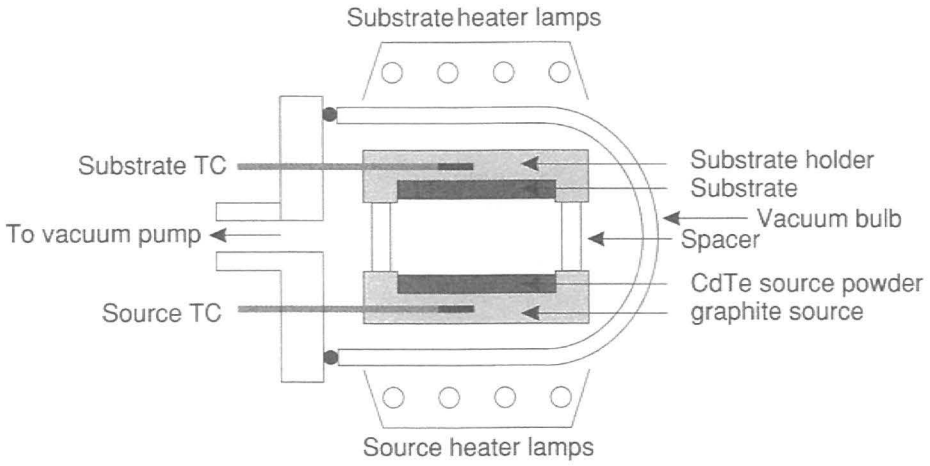

Figure 2.1: Schematic of CdTe deposition arrangement by close spaced sublimation (CSS). TC = thermocouple, after Poortmans [5]

2.2.2 Stacked Elemental Layer (SEL)

Vacuum evaporation has been used by the group at Delaware, to fabricate CdS/CdTe cells with efficiencies above 10 % [6]. In order to get the desired stoichiometry, the thickness of elemental layers must be adjusted; the relative number of atoms in the layers must be identical. This is similar to CSS where boats with the reacting material are used. Here, two boats each with separate starting materials are used. Evaporation rate of 0.3 nm/s have been reported for the deposition of CdTe [7]; a low pressure during evaporation is also used (typical values are in the order of 10^{-6}–10^{-5} Torr range [7]) and makes SEL a very slow growth process.

2.2.3 Atomic layer deposition (ALD)

In ALD, successive elemental layers are effectively limited to mono-atomic layers; the technique was originally called atomic layer epitaxy (ALE). The monatomic elemental Cd and Te layers are deposited by periodically switching a gas flow between an inert carrier gas containing Cd followed by Te. This technique allows excellent control of the CdS/CdTe intermixing region. Typical efficiencies using this technique are 14% [8].

2.2.4 Metal organic chemical vapour deposition (MOCVD)

MOCVD can be carried out in a low [9] or atmospheric pressure [10]. The precursors for the vapour phase deposition of CdTe are volatile metal organic compounds, e.g. dimethylcadmium and diisopropyltellurium. Both precursors are fed simultaneously to the substrate, entrained in a carrier gas of hydrogen. The properties of the CdTe film are determined by the process parameters (gas temperature, flow and concentration of precursors in the carrier gas, substrate and bubbler temperature) [10]. A more detailed description of the MOCVD system is described further in the chapter.

2.2.5 Sputtering

Physical sputtering is driven by momentum exchange between the ions and atoms in the material, due to collisions. Sputtering is well suited for industrial large scale production, as its deposition speed is very fast compared to some other technologies, and it has been applied successfully both to CdS and CdTe [11] and to the back contact [12].

2.2.6 Electrodeposition

Electrodeposition of CdTe was developed for industrialization by BP solar [13].The deposition of CdS and CdTe is at low temperature, and annealing at temperatures above 400 °C are used following deposition to promote grain growth. The electrolyte contains a high concentration of Cd^{2+}, but only a low concentration of TeO_2. As a consequence, deposition of 2 μm CdTe films from stirred solutions normally requires 2–3 h. Recent work however [14], through the use of a channel flow cell, has shown that high-quality CdTe films can be grown rapidly (approx. 20 min) making it a relatively faster process.

2.2.7 Chemical bath deposition (CBD)

CBD involves dipping a substrate in an aqueous solution, containing Cd^{2+} and S^{2-} ions, and is the most common technique for depositing the CdS buffer layer in $Cu(In,Ga)Se_2$ solar cells. It has also been used for CdS/CdTe cells [15]. The technique yields very thin layers and offers much less process control than numerous other deposition methods (along with solution waste issues). Its advantage is that it is a simple technique, and therefore inherently cheap and easy to scale up.

2.2.8 Solution spray

Commonly (not always) an aqueous solution is used containing a Cd precursor (e.g. $CdCl_2$) and a Te precursor (TeO_2 or an organic Te compound) can be sprayed onto a heated substrate. The CdTe compound is formed on the substrate, and the residues are vaporized. This technique was developed by Photon Energy, later Golden Photon, to yield efficient cells (12.7 %) [16]. In order to get uniform films, the solution should be atomized and spread uniformly by rotating the substrates. The solution in the form of fine droplets first hits the substrate and gets flattered even before the pyrolytic reaction takes place and hence the films obtained contain no pin-holes. The atomization and flow rates depend on the air pressure and on the design of the spray gun.

2.2.9 Screen printing and sintering

This technique has also been developed to a industrial level by Matsushita Batteries [17] and developed by the University of Gent [18]. The screen printing slurry consists of CdS or CdTe (or Cd and Te) powder, with some percentage of $CdC1_2$ powder as a flux. After screen printing and drying, the substrates are sintered at a high temperature (500-600 °C) in ambient nitrogen.

The advantages and disadvantages of each technique are summarized in Table 2.2.

Table 2.2: Advantages and disadvantages of various thin-film deposition technologies.

Deposition technique	Advantages	Disadvantages
CSS	Very fast growth rate - high throughput, - Large grain sizes, and well-defined preferential orientation.	- Limited process control, - no *in situ* monitoring, - Large grains make it difficult to grow ultra thin films. - Starting material is "CdTe" in powder form (need to control exposure as very toxic) and spread on a boat prior to deposition, very sensitive to uniformity effects (film thickness) and repeatability.
Stacked Elemental Layers (SEL)	- High deposition control	- Need to alternatively evaporate successive species in order to deposit stoichiometric layers. - Need a low pressure system for deposition, which greatly increases system cost.
Atomic layer deposition (ALD):	- Very high process controllability.	- Very low growth rate (limited by precursors switching between layers, often a few seconds) and / low precursor utilization efficiency.
Metal organic chemical vapor deposition (MOCVD)	- Very high process control. - *in situ* monitoring. - Can be done with or without a vacuum. The MOCVD used in this research is an atmospheric pressure reactor.	- Currently, metal organic sources are expensive. - Relatively slow growth rate (in the order of 0.5 nm/s for the CdTe absorber). - Prone to wedge profile growth (in horizontal chamber setup). Need to rotate to obtain uniform films.
Sputtering	- Very high growth rate - Sources easy to obtain but due to the design of the source always within reach of the surface, any contamination either from the substrate or the side walls of the chamber (possibly from previous depositions) has the potential of contaminating the source. In-situ monitoring available: micro balanced, optical ellipsometry.	- Often wedge profile growth obtained, depending on the orientation of the sputtering target relative to the source. - Requires vacuum.
Electrodeposition (ED)	- Low temperature growth of both CdS and CdTe layers.	- Produces large amount of liquid waste.
Chemical Bath Deposition (CBD)	- Relatively low cost, large area. - Low temperature - Fibre optic in-situ measurements	- In the classical beaker configuration, the material yield for film formation is very low, about a few per cent, leading to an unnecessary waste production. - Poor process control as the substrates are simply dipped into a beaker for a period of time. Difficult to obtain uniform films.
Solution Spray	- High deposition control	- Have to rotate the substrate to obtain truly uniform films.
Screen printing and sintering.	- Fast deposition rate.	- Requires a thick CdS layer for uniform film (which lowers optical transmittance.) - Relatively high temp (for sintering stage, make it an expensive option) - Low process control as slurry is used.

2.3 Large scale production of cadmium telluride solar modules

Presently (2009), CdTe solar modules are produced in two major plants: Antec Solar Energy [19] and First Solar [20]. In the Antec plant the TCO is applied by sputtering [21], with the CdS and CdTe both deposited by CSS. These steps, together with the activation of CdTe, contact treatment, sputter deposition of the contact buffer and contact metal, and the laser scribing for the series connection, are integrated in one production line. Antec's produced panels are 60 x 120 cm^2, which gives a production capacity of 100,000 m^2/yr, corresponding to 8 Mega watt peak (MWp/yr) with the present module efficiency of 8 %. In a second production line, the glass plates are encapsulated and sealed to finished modules.

First Solar uses the same module size, but the CdS and CdTe layers are deposited by high rate vapor transport deposition (HRVTD) [22]. Here vapors of subliming CdTe are brought over the substrate plates As of 2008, First Solar is the largest thin-film module manufacturer in the world [23], with the lowest module cost per watt in the industry. First solar have announced that a cost of €3.25/$4.6 ((correct as of May 2008 [23]) with a target of $1.15 Wp in the third quarter of 2008 is planned. The target cost/Wp of $0.70 would bring thin-film CdTe PV energy generation costs level with traditional electrical generation technologies [23]. First solar (www.**firstsolar**.com) have already reported grid parity in several US states (2010).

2.4 Issues with current production technology

Several undesirable issues still exists in established CdTe module manufacturing processes: namely (i) thick absorber layer (3-7 μm) are used [24], in order to obtain material of sufficient quality, and is a specific drawback of the CSS technology, which is chosen for its superior deposition speed and throughput. (ii) The n-type window layer (CdS), also needs to be thick enough to avoid incomplete surface coverage or "pin-holes", in order to avoid possible short–circuits in the device.

Despite the high optical absorption coefficient of CdS, poor photo-response can be attributed [25] to low hole lifetime and high carrier recombination in the layer. Thus, optical absorption in the CdS layer is the predominant photocurrent loss, making it necessary to minimize the CdS film thickness in the device [26].

Obtaining a good ohmic contact between the metal back contact and a material with a high electron affinity (CdTe) has proven to be difficult, as the work function of the metal needs to be higher than that for CdTe [24] (Table 2.3). The situation is made more difficult if the semiconductor also has inadequate doping.

Table 2.3: Work functions of various metals.

Material	Work function (eV)
CdTe (p-type)	5.9
Gold	5.1
Nickel	5.01
Copper	4.07
Aluminium	4.08
Silver	4.73

Generally, this problem is solved by either using a metal of high work-function contact, or generating a highly doped p^+ layer at the surface of the semiconductor, creating holes which tunnelling through the barrier. The problems for CdTe are evident for both cases: low cost metals of work functions higher than CdTe are not available, and p-doping in CdTe suffers from a strong tendency for self compensation of acceptors [24]. Furthermore, Bonnet [24] states that acceptors cannot be introduced by diffusion-doping from the surface, as the dopants generally diffuse preferentially along grain boundaries, leading to shunting of the cell before sufficient doping levels are achieved. In many cases, copper (an acceptor in CdTe) is added (however, not in our case).

Etching the CdTe surface with a nitric/phosphoric acid mixture (`NP-etch'), has been shown [27] to effectively produce a very thin Te-layer on the CdTe surface, which, has the effect of lowering the back contact barrier height. It is known that the act of Br/Methanol or NP etching, diffuses the etchant down through the grain boundaries, depositing a Te "cap" on individual grains and enlarging the contact area [27]. Presently [25], contacting generally consists of i) wet etching using either Br/methanol or NP; ii) followed by deposition of a metal film for low resistance current collection.

The band diagram of the CdTe back contact region has been proposed by Fristche *et al.[28]* (Fig 2.2). It depicts the resulting band energy diagram for both (i) thick and (ii) thin Te layer on the CdTe surface, formed by etching the surface, the mechanism by which CdTe surfaces are depleted of Cd is described by Sarlunda *et al.*[29] .

The valence band offsets show that the Te layer does not form a good Ohmic contact on CdTe. The Te thickness dependence of the valence band positions of CdTe indicates a change in the doping due to back contact formation. Therefore, it is suggested that a Te layer formed by etching leads to a tunnelling contact to CdTe if this is strongly p-doped [30].

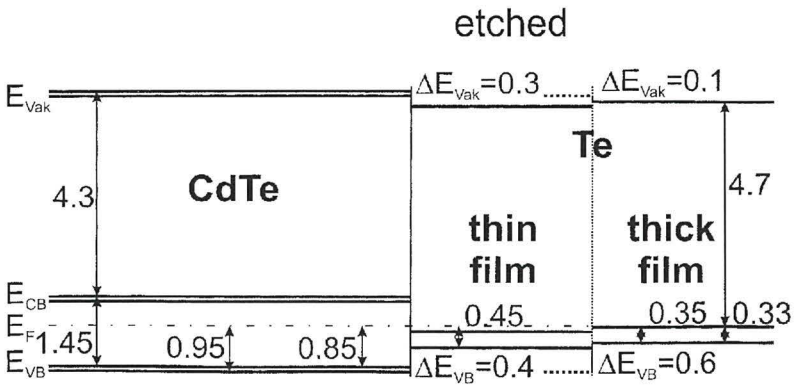

Figure 2.2: Band diagram of CdTe surface after etching. After Fritsche *et al.* [28]

The etching process is an undesirable aspect of obtaining a good Ohmic contact, as it only has limited control, and produces vast amounts of liquid waste, which needs to be taken into account in the production of CdTe modules.

More novel and recent contact approaches include; i) the investigation of the induced space charge carrier region, and ii) the charge accumulation at the metal semiconductor barrier. The charge accumulation occurs as a result of contact between a metal and a large work function (Wf) material, it is also known as the bound charge polarization effect, and is common to all high resistivity materials [31].

To minimize the bound charge polarization effect, the work function between the CdTe and metal can be matched, to reduce the polarization potential. One can also induce a charge injection effect for drifting the carriers, through decreasing the bound potential. This approach is taken by Ghosh [32], who uses a spontaneous "electroless" deposition process. The technique can be introduced in-situ during growth, and can modulate the work function of the individual material and develop an effective work function to match the semiconductor.

2.5 History of the MOCVD technique

MOCVD was conceived by Manasevit [33] in the early 60's when the need for new and emerging materials required new technologies. Today, MOCVD is used in many fields from manufacturing visible and infrared lasers, LED's, to solar cells.

Manasevit [33] was the first to use arsine (AsH_3) with trimethylgallium to deposit GaAs, along with other variations (such as GaN, using ammonia). Later, authors such as Stringfellow [2], further described detailed MOCVD growth physics and regimes possible in various reactor designs. Terms such as source/input zone, mixing zone (where the precursor gases mix) and the boundary layer (where the gases diffuse towards the heated substrate) were introduced. A vertical reactor is shown in (Fig 2.3).

Figure 2.4, shows a diagram of a typical bubbler used in MOCVD, the carrier gas is passed through the precursor containing bubbler, and picks up a small amount of precursor as it travels from the inlet to the outlet towards the reactor. The vapour pressure of the organometallics (OM)'s in the bubblers is controlled by the temperature of the bubbler (e.g. using a water bath). Evaporation of a liquid in a closed container still takes place from the surface of the liquid, and eventually equilibrium will be reached. At equilibrium, the number of particles leaving the surface is balanced by the number rejoining it. In this equilibrium, there will be a fixed number of the gaseous particles in the space above the liquid, which is termed the saturated vapour pressure.

If the external pressure is higher than the saturated vapour pressure, these bubbles are prevented from forming, and evaporation only occurs at the surface of the liquid. The pressure needs to be closely controlled in order to allow entrainment of the OM (the process of the hydrogen carrier gas picking up some OM liquid material from the bubbler and transporting it on the gas to the reactor). The gas flow is measured in standard cubic centimetres per minute at standard conditions (1atm and 0 ^{o}C).

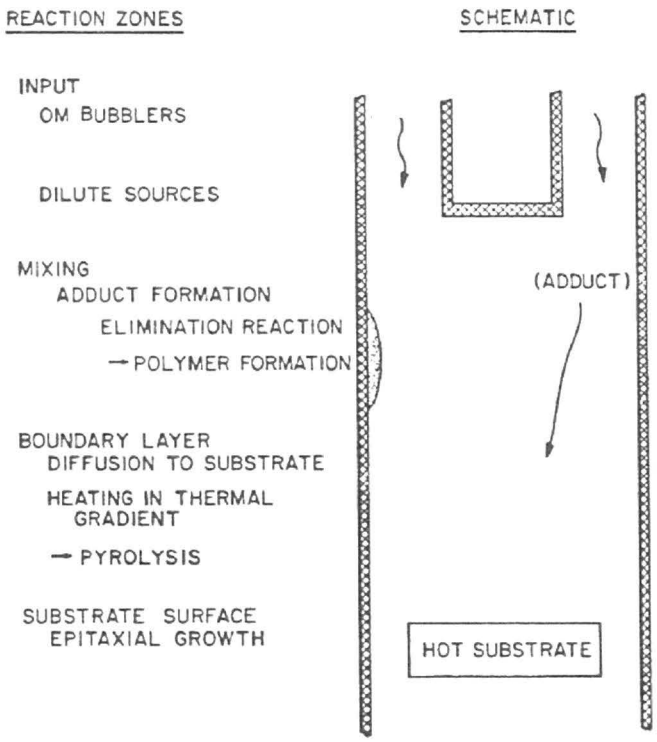

Figure 2.3: Reaction regimes for the MOCVD process. after Stringfellow [2]

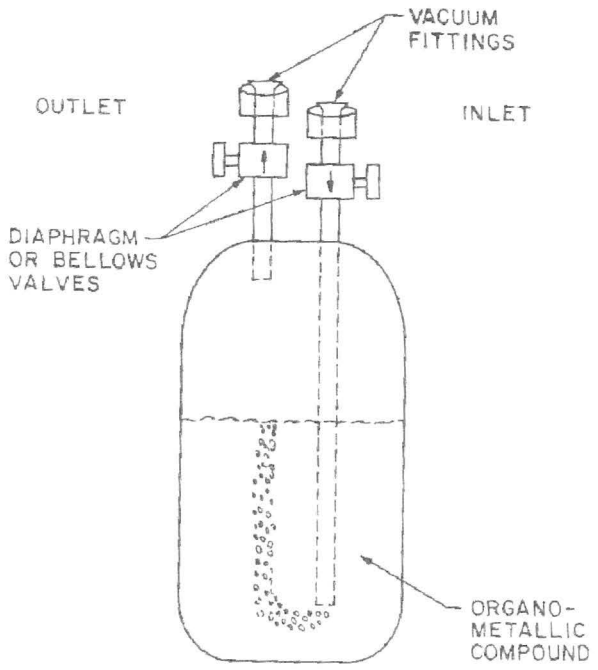

Figure 2.4: Diagram of a precursor bubbler used in MOCVD after. K Schuegraf et al. [1]

The III-V and II-VI compounds (and alloys), are usually grown using lower molecular weight metal alkyls (e.g. di-methyl cadmium 'DMCd' formula $(CH_3)_2Cd$)). The sources are introduced in the vapour phase, into the reaction chamber and thermally decompose at elevated temperatures by the hot susceptor. The reaction chamber walls are not deliberately heated and are sometimes water cooled. Being a "cold walled" process, the reactor walls do not directly influence the chemical reactions that occur in the chamber.

The overall chemical reaction that occurs during the MOCVD process can be written as (Eqn. 2.1) [34].

$$RnM(v) + ER'n = (v) - ME(s) + nRR'(v) \qquad 2.1$$

where R and R' represent a methyl (CH_3) or ethyl (C_2H_5) radical, M is a group II or group III metal, E is a group V or group VI element, and n=2 or 3 depending on whatever II-VI or III-V growth is taking place.

2.6 Reactor design

Leys [35] outlined two main types of reactors (a) vertical and (b) horizontal reactors (Fig 2.5). The type of reactor used, will depend on the desired characteristics of the final layer. A rotating vertical reactor is typically chosen to obtain a uniform coating, as the vertical design does not suffer from precursor depletion effects (where the precursor enters the inlet of the reactor, and immediately decomposes, making less precursor material available for reacting towards the outlet of the reactor). Thus, a horizontal reactor coats more preferentially (thicker) at the inlet of the precursor gases, but this can be minimized through careful control of the carrier flow. A horizontal type setup is typically chosen for its simplicity, tolerance of high temperatures, and the ability to process large numbers of layers/wafers at a time over a showerhead type deposition system.

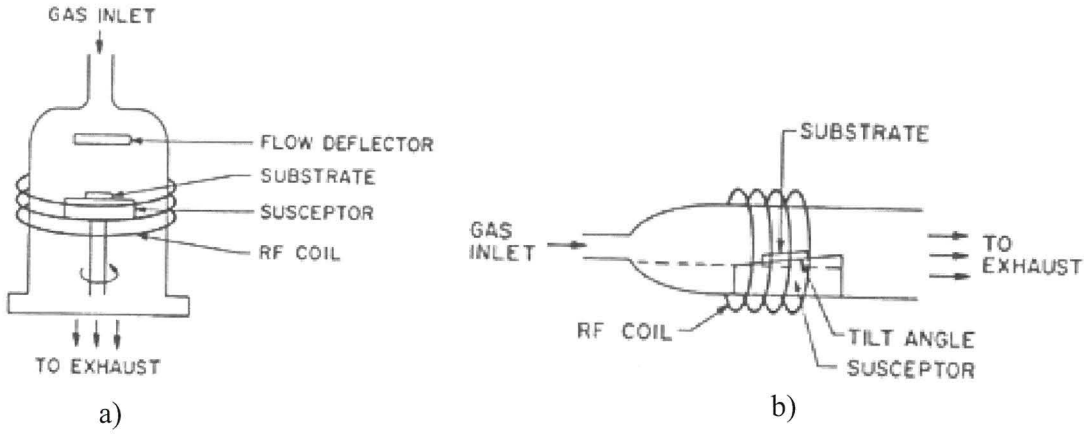

Figure 2.5: Schematic of a) vertical and b) horizontal MOCVD reactors. After Shuegraf *et al.* [1] . Manufacturers of modern MOCVD chambers, include Aixtron (Germany) and Veeco (U.S.).

2.7 CdTe solar cells by MOCVD

Since MOCVD was used for cadmium mercury telluride (CMT) infrared detectors [36], interest in CdTe for use in solar cells has been growing. In 1990, Chu *et al.* [37] showed that CdTe (grown by MOCVD), could be used for photovoltaic applications. Since then good photovoltaic conversion efficiencies have been obtained using a combination of MOCVD for the CdS and CSS to deposit CdTe [38] layers .

The potential for depositing the full CdTe/CdS junction by MOCVD using alkyl precursors was first reported in 1998 by Berrigan *et al.* [39] but only low levels of p-type doping was achieved. The occurrence of native defects in CdTe makes precise control of the doping density difficult. The interactions between these native defects and foreign elements can cause self compensation, and this renders impurity doping of CdTe difficult.

The difficulty to obtain a good p doping in thin, polycrystalline, CdTe films is a distinct disadvantage. However, several authors have reported successful p-type doping of CdTe, using various species, Sn [40], Bi [41] and Cu [42].

For MOCVD, improved p-type activation has been achieved using arsenic (As) doping by Barrioz *et al.* [9, 43, 44]. The approach of Barrioz *et al.* [9, 43, 44] and Berrigan *et al.* [39] enables all layers to be grown in the same reaction chamber. This negates the need for a multiple deposition process and techniques needed to complete a full PV device. This decreases the possibility of surface contamination, and as no sample transport is needed between successive chambers, process throughput is also increased. The progress of CdTe based solar cells and modules have been reviewed regularly [5].

2.8 Characterization of CdTe thin-film solar cells

2.8.1 Electrical characterisation - *pn* junction

When a p-n junction is subjected to *forward bias*, the electrostatic force of the charges cause the majority carriers to flow towards the junction. The strength of the built in field and the gradient of the band-bending is reduced (Fig 2.6). Thus the diffusion of the minority carriers exceeds those that tend to drift back in the opposite direction. The Fermi level, splits into quasi Fermi levels. The result of the forward bias is that majority carriers flood across the junction, and constitute the dc steady state current seen in a forward biased diode.

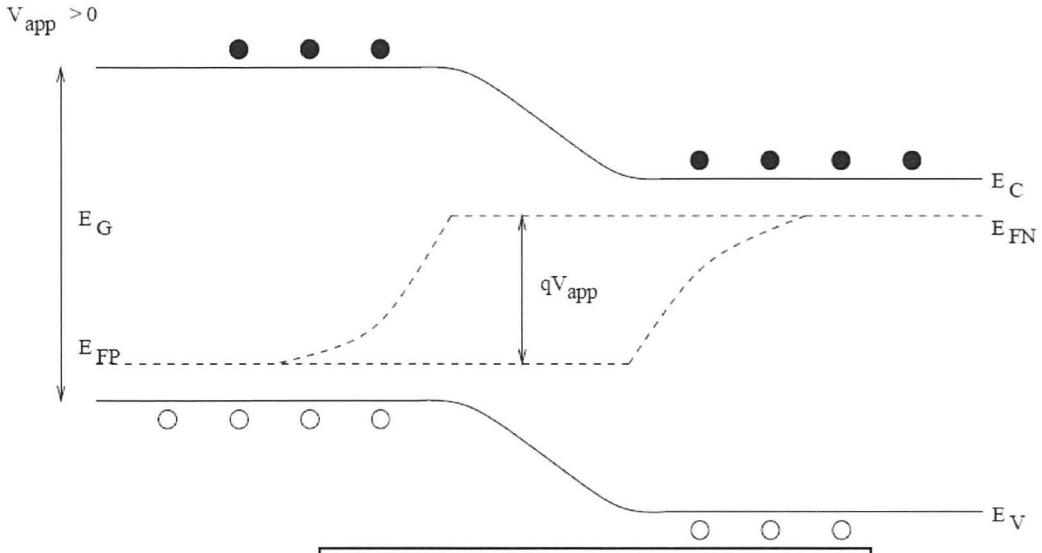

Figure 2.6: PN junction in forward bias.

Under *reverse bias* the applied potential difference causes the majority carriers to move away from the junction. This causes an increase in the built-in voltage and the band-bending (Fig 2.7). Consequently there is only minority carrier flow across the junction. The difference in the quasi Fermi levels again equals the applied voltage. The current flowing across the junction is minimal and independent of the magnitude of the applied bias. This current is the reverse saturation current observed in a reverse biased p-n diode.

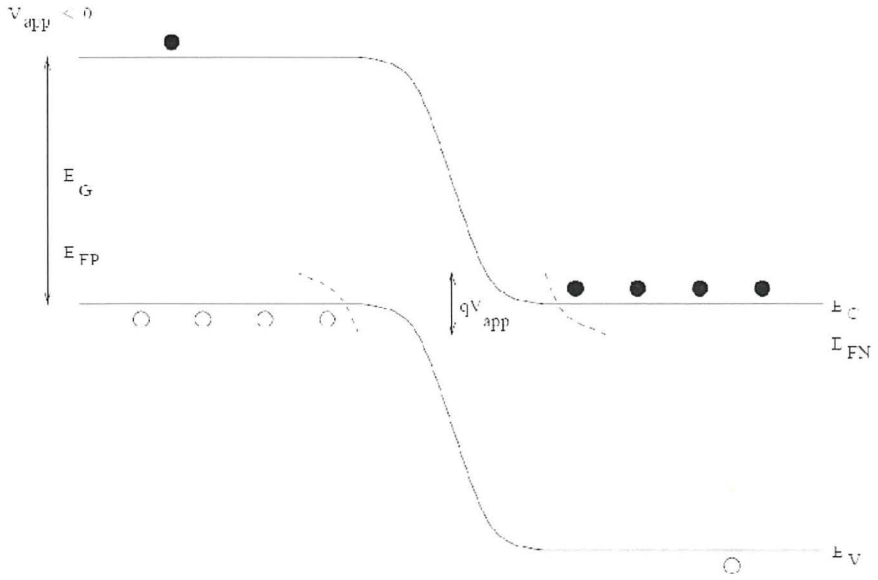

Figure 2.7: PN junction in reverse bias.

2.8.2 The Current-Voltage (I-V) characteristic

Here the current is measured as a function of applied voltage for a cell, in both light and dark. The solar cell acts as a diode. Ideally the light I-V curve is nominally the same as the dark, yet shifted so that even with no applied voltage, a negative current exists due to the motion of photo-generated carriers, however in practise this is not the case. This negative current occurs when holes move toward the back contact and electrons move toward the front contact which comprises the TCO.

As a forward voltage is applied (positive potential to the back contact, and negative potential to the TCO), carriers are moved in the opposite direction, producing a positive current. When the total current is zero, the voltage is the open circuit voltage V_{oc}, and when the applied voltage is zero, the current is the short circuit current J_{sc}. The power is simply the voltage multiplied by the current, with a maximum power density obtained at a particular point in the I-V curve where maximum values of V_{max} and J_{max} are obtained.

The series resistance R_s, can be calculated by taking the inverse of the slope of the linear portion of the curve (above V_{oc}). The shunt resistance R_{sh}, which is the inverse of the slope at J_{sc}, can also be obtained from the slope at high reverse currents. A poor back contact will yield a device with a higher series resistance and "roll-over behaviour" [30] (Fig 2.8), which is the junction voltage saturating at high bias, due to the back contact barrier.

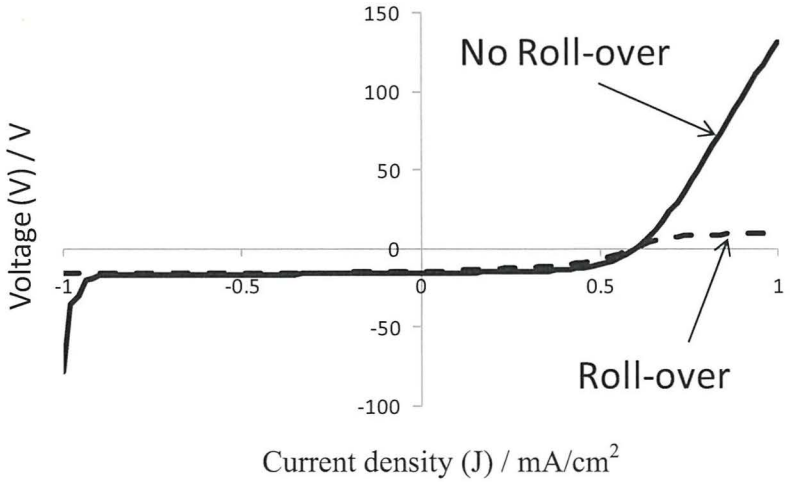

Figure 2.8: I-V curve of CdS/CdTe device showing the effect of the "roll-over".

The roll-over in I-V curves, is recognized as a result of the formation of a higher back barrier at the back contact. Many authors [45] have commented on the advantages of the use of Cu containing materials at the back contact, to lower the back barrier height. But it has now been reported [45], that roll-over is still possible with these devices that have been treated with a Cu back contact treatment, as the formation of Cu-related oxides at the back side of the device during processing, rather than the diffusion of Cu to the front side of the device causes a poor back contact.

An ideal I-V curve (shown in Fig 2.9), would have no roll-over behaviour, due to poor back contact formation. The curve in Fig 2.9, has been calculated directly from the diode equation, (Eqn. 2.2);

$$J = J_0\left(e^{\left[\frac{qV}{kT}\right]-1}\right) - J_L \quad 2.2$$

where J is the current density, V is the voltage, J_0 is the dark current density, q is the charge of an electron, k is Boltzmann's constant, T is the temperature, and J_L is the current at zero bias in light.

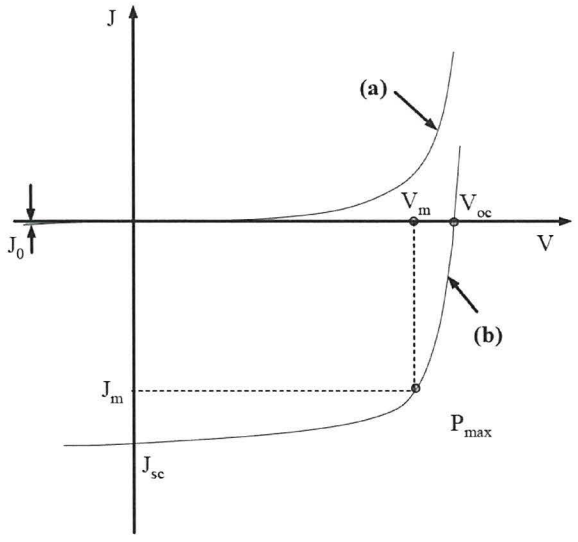

Figure 2.9: The Current density-Voltage curve of a p-n junction solar cell; (a) in the dark and (b) under illumination.

Several other parameters of interest can be derived from those obtained directly from the I-V curve. These parameters include the efficiency, η, of the cell, as well as the fill factor (FF).

The FF (Eqn. 2.3) is a measurement of the efficiency (Eqn. 2.4) of a particular cell compared with how an ideal cell (no thermionic losses/ recombination etc.) with the same V_{oc} and J_{sc} would perform.

$$FF = \frac{P_{max}}{V_{oc}J_{sc}} \quad 2.3$$

$$\eta = \frac{P_{max}}{P_{in}} \quad 2.4$$

Where P_{in} is the total irradiance of the incident illumination (100mW/cm^2).

Characterizing cells via their I-V curves is the standard method of determining the quality of a solar cell. Typical FF values for high quality devices are in the range of 70% to 85% [46].

2.9 Current world record CdS/CdTe cell

To achieve CdTe cells with an efficiency of 18 %-20 %, research at NREL has been focused on improving the V_{oc} of devices (ca. 900 mV) [47]. This can be achieved in three ways: i) improve the built-in potential by minimizing compensation and increasing doping of the CdTe film. ii) Improve the diode quality factor by minimizing the recombination-centre density in the junction region and iii) Reducing the back-contact barrier height.

To date, the best CdTe device obtained by NREL is the 16.5% obtained by Wu *et al.* [48]. Such a high efficiency has been achieved through the use of a very thick CdTe absorber layer (>6μm), the use of a novel CdO front contact, which has improved properties compared to indium tin oxide (ITO), and Oxygen has been used during CdS growth to create, oxygenated nanocrystalline CdS film (nano-CdS:O), prepared by RF magnetron sputtering [47]. The CdS:O film has a higher optical band gap (2.5-3.1 eV) than a standard CdS (2.4 eV) film.

Wu *et al.* [48] reports that the band gap of the CdS:O, increases with oxygen content, decreasing grain size. The higher oxygen content present in the nanocrystalline CdS:O films can significantly suppress the Te diffusion from the CdTe into the CdS film and the formation of a $CdS_{1-x}Te_x$ alloy, which results in a higher quantum efficiency in the short-wavelength region and an increased J_{sc} response. Photocurrent values of nearly 26 mA/cm^2 in a Cd_2SnO_4 (CTO)/ Zn_2SnO_4 (ZTO)/CdS:O/CdTe cells have been reported [48].

In a conventional CdTe device, a CdS film has been used most commonly as a window material. But it has three main issues that limit device performance.

Firstly, a $CdS_{1-x}Te_x$ alloy with a lower band gap can be formed between the CdTe and poly-CdS film, which degrades device performance. Secondly, CdS has a band gap of ~2.42 eV, which causes considerable absorption in the short-wavelength (blue region) region. Thirdly, there is a nearly 10% lattice mismatch between the poly-CdTe film and the poly-CdS film, which causes high defect density at the junction region.

Taking into consideration the increased band gap of the CdS (3.1 eV, compared to standard CdS of 2.4 eV) and using the calculated photon flux from the AM1.5 spectrum obtained from NREL website (Fig 2.10). The relative increase in available photocurrent (J_{sc}) can be accounted for (Table 2.4), and an equivalent cell (using the standard CdS band gap, 2.4 eV) can be calculated. A 12% increase can be seen as a result of widening the optical band gap of the CdS window layer to 3.1 eV, this equates to approx. 2% absolute in efficiency terms or 14% relative increase in energy.

Table 2.4: Results of Photon flux integration, showing relative available photon flux to be absorbed by the relative junctions.

Device	**Wavelength range (nm)**	**Photon flux (m^{-2} s^{-1})**	**Rel. Photon flux (%)**
CdS/CdTe	517-855	1.57×10^{30}	100
World record device	400-855	1.84×10^{30}	112

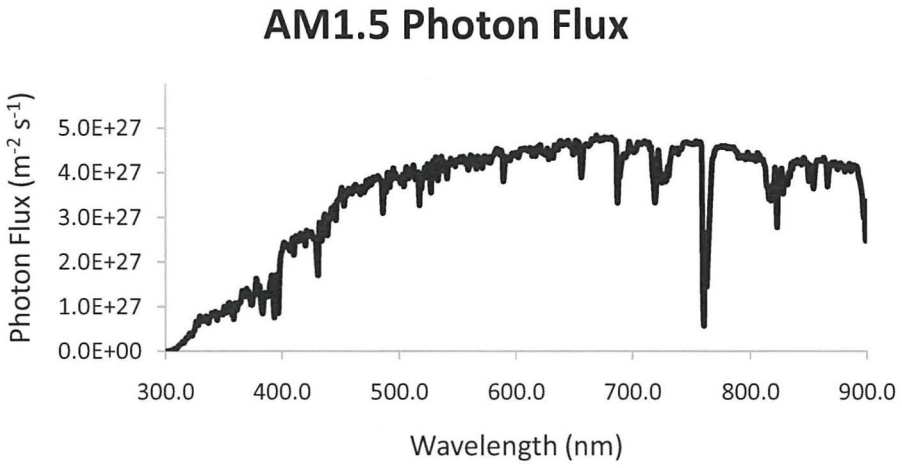

Figure 2.10: Graph of AM1.5 spectrum. Graph constructed using NREL AM1.5 data. [49].

2.10 Advanced cell structures and applications

For applications in space, the power-to-weight ratio becomes an increasingly important figure, and the heavy glass substrate should be replaced by flexible/light materials e.g. thin metal foils. The superstrate configuration can be maintained when a transparent plastic foil is used (Fig 2.11); however, the plastic material is then exposed to the high CdTe processing temperature. A metal foil can be used in a 'substrate configuration'.
The problems with the plastic superstrate were addressed by using thin spin coated polyimide film, combined with a lift off technique from a reusable glass substrate; and efficiencies of over 10% have been obtained [50].

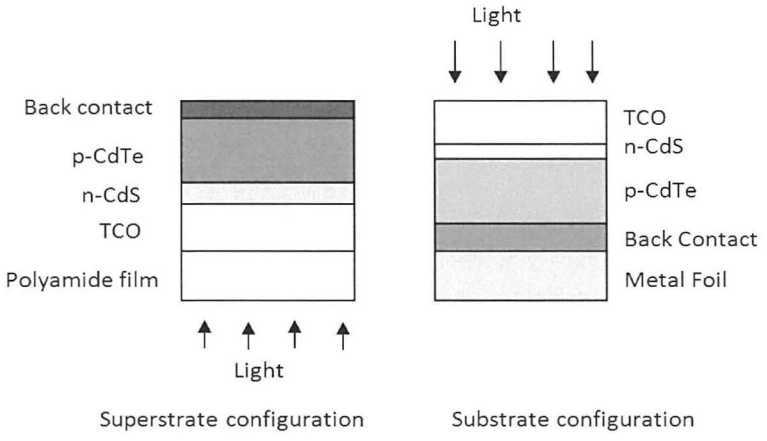

Figure 2.11: CdTe solar cells with a superstrate configuration (left) and with a substrate configuration (right).

Thin-film CdTe cells are very radiation resistant [51]: somewhat better than CIGS, and significantly better than crystalline GaAs or Si bulk cells. A simple explanation for this is that defects introduced by the electron and proton radiation only start degrading the cell's performance when they begin outnumbering the defects already present in the as-made cells.

The performance of bulk crystalline cells relies on a very high minority carrier diffusion length: it should be a factor of 100 higher than in thin- film cells, thus the trap concentration should be 100 times lower than tolerable in thin-film cells. As a consequence, thin-film cells only begin to degrade at a total fluence (radiative flux integrated over time), which is orders of magnitude higher than that for crystalline Si or GaAs cells. A comparison of the radiation degradation of different materials can be found in [52].

2.11 losses of thin-film CdTe solar cells

The following section summarizes some of the known losses in CdS/CdTe device performance. Factors that are known to influence device losses include;

- Series Resistance (R_s),
- Back contact processing [53],
- diode quality factor,
- leakage conductance and shunt resistance (R_{sh}),
- voltage dependence of photo-generated current (J_L)

2.11.1Resistivity losses

In the simplest scenario, this could be due to the resistivity of all three layers of ITO, CdS, and CdTe. However, often, the resistivity of the CdTe absorber is thought be the primary cause for resistivity losses [54]. R_{sh} is considered when there is a shunt current due to several reasons, such as thin CdS with voids and pinholes (due to incomplete surface coverage). Degradation of the main diode can result in a lowering of R_{sh} due to tunnelling pathways.

Thus R_{sh}, can be used to gauge the junction quality, and used to give an approximate measure of non-uniformity of the junction, which is thought to be more critical for ultra thin absorber thicknesses as weak diodes and non-uniformity are expected to be greater [54]. A barrier can be formed at junctions due to difference in work functions of different materials. If one looks at the etching procedure, the resistivity of a gold contact/ etched CdTe surface is typically higher [55] than reported for pure evaporated Te thin-films, which is due to the fact that the surface layer formed by etching is not a single phase Te.

2.11.2 Current (J_{sc}) losses

Song *et al.* [56] state that a 100 nm thick layer of CdS, typically absorbs 36 % of the incident radiation with photon energy higher than its band gap. J_{sc} losses also include; reflection, glass absorption, TCO absorption, mixed CdS/CdTe layer absorption and deep penetration collection losses. The short-circuit current in each case is calculated using (Eqn. 2.5) [57]. Where the QE spectrum is integrated and multiplied by the AM1.5 solar photon current I_{solar} [58].

$$J_{sc} = \int_{\lambda_{min}}^{\lambda_{max}} QE(\lambda) * I\,(\lambda) d\lambda \qquad 2.5$$

Using Eqn. (2.5), an Ideal CdTe cell with a QE of 100% will yield a photocurrent of 30.5 mA/cm^2, this can be thought of as the maximum possible current if the device had no defects, which is unrealistic in real devices. Each individual current density loss due to optical loss can be calculated (Eqn. 2.6).

$$J_{loss} = \int_{\lambda_{min}}^{\lambda_{max}} F(\lambda) * J_{solar}\, d\lambda \qquad 2.6$$

Where $F(\lambda)$ is fractional reflection or absorption at each wavelength.

Sites *et al.* [58] compared their best cell against the current world record by Wu [48]. The losses are i)Reflection of the incoming light, ii) absorption in the glass (of the light which is not reflected), iii) TCO absorption, iv) absorption in the CdS layer and finally, v) deep penetration losses, which results from incomplete absorption of the photon, and lowers the red response of the device. Sites *et al.* [58] states that considerable J_{sc} loss is due to CdS absorption.

2.11.3 Grain boundary losses

Grain boundaries are possible regions of current loss due to;

- charge carrier traps at grain boundaries
- the grain boundary barrier height,
- Possible recombination region (if poor passivation)

If the carrier concentration is not high enough, or if the mobility is too low (due to non-uniform doping, or material defects), the current collection for the entire cell will deteriorate. Carrier mobility in polycrystalline thin-films are generally several orders of magnitude smaller than mobility in single crystals of the same material. Thorpe *et al.* [59] comments on charge carrier mobility in polycrystalline materials, such as CdTe, being controlled by grain boundaries, thus there is a need to understand and passivate the grain boundaries in order to aid carrier mobility, and decrease the probability of grain boundaries becoming regions of recombination.

2.11.4 Voltage (V_{oc}) losses :

In general V_{oc} is limited by the dominant current transport mechanisms [58]. The junction barrier height, J_0 and the diode ideality factor (n), are measures of junction quality (Eqn. 2.7).

$$V_{oc} = \frac{kT}{q} ln\left(\frac{I_L}{I_0} + 1\right) \qquad 2.7$$

The quality of the junction can be dependent on several factors; such as, substrate quality, any film defects, film uniformity, doping uniformity and concentration. All of which are very difficult to accurately measure.

Improving the built-in potential by minimizing compensation and increasing effective doping in the CdTe film; In order to obtain higher V_{oc}, it would be desirable to have higher doping close to the junction (for fundamental offset between the two sides of the junction). The larger recombination velocity, the smaller V_{oc}. Hence, Improvements in V_{oc} should follow from decreased recombination in the absorber layer.

2.11.5 Fill factor losses:

The FF describes how diode like the actual device is, and measures the "squareness" of the I-V curve, or its actual power output (V_{mp} x J_{mp}) versus it's "'theoretical" power output (V_{oc} x I_{sc}). It represent the current density and voltage at the maximum power point, this point being obtained by varying the resistance in the circuit until J x V is at its greatest value (Eqn. 2.8).

$$FF = \frac{J_{mp}.V_{mp}}{J_{sc}.V_{oc}} \qquad 2.8$$

The fill factor is directly affected by the values of, the cells series and R_{sh}. Increasing R_{sh} and decreasing R_s will lead to higher FF, thus resulting in greater efficiency, and pushing the cells output power closer towards its theoretical maximum. Film thickness also affects the maximum available power, and thus the FF value.

2.11.6 Depletion region recombination losses:

Green [46], outlines the effect of traps within the depletion region on the shape of the diode curve. The result can be summed up with the addition of one parameter, called the ideality factor (n), to the Shockley diode equation (Eqn. 2.9).

$$I_a = I_b \left(e^{\frac{qV}{nkT}} - 1\right) \text{ - } J_{sc} \qquad 2.9$$

Where I_a is the diode current, I_b is the reverse bias saturation current, and n is the ideality factor. The ideality factor typically varies from 1 to 2, with the values greater than one indicating a transport mechanism dominated by recombination. However tunnelling enhanced recombination into trap states provides ideality factors greater than two, and often greater than three [60].

2.11.7 Optical losses

2.11.7.1 Blue absorption

CdS absorbs heavily in the blue region of the solar spectrum. Several authors have reported the use of $Cd_{1-x}Zn_xS$ [56, 61, 62]instead of CdS in hetero-junction cells (e.g. CdTe, $CuInSe_2$, and $CuGaSe_2$) can lead to an increase in photocurrent, by both providing a closer match in electron affinity and being capable of transmitting higher energy photons to the underlying absorber layer.

Adjusting the Zn composition from 0 to 1, one can vary the ternary alloy ($Cd_{1-x}Zn_xS$) band gap from 2.4 eV to 3.7 eV [61, 62], by reduction of the inter-atomic spacing and increasing the repulsive interaction between core electrons. The use of $Cd_{1-x}Zn_xS$ in pn junctions with no lattice mismatch, for devices based on quaternary materials like $CuIn_xGa_{1-x}Se_2$ or $CuIn(S_xSe_{1-x})^2$ have also been reported [63].

The replacement of CdS with the wider band gap ternary alloy ($Cd_{1-x}Zn_xS$) can lead to an increase in the lattice mismatch with CdTe (approx. by 16% [64]). However, the loss attributed to the increased lattice mismatch can be minimal compared to the gain achieved with lower blue absorption losses, resulting in an overall increase in the photo-current generation of the cell [65].

Yamaguchi *et al.* [66] demonstrated how $Cd_{1-x}Zn_xS$ can be used in a CdZnS/CdS/CdTe structure as a buffer arrangement, the CdS/CdTe junction was replaced by Chu [67], where a CdZnS/CdTe junction was favoured, where MOCVD was used to grow the CdZnS layer and CSS the CdTe, however at that time, CdTe device efficiencies were low, possibly due to poor achieved doping concentrations.

Early work by Chu *et al.* [68] on using the MOCVD technique to grow CdZnS layers and incorporate CdZnS layers into CdZnS/CdTe yielded significantly lower V_{oc} than devices compared with standard CdS/CdTe junction. This decrease was attributed to the interface reaction between CdS and CdTe, forming, CdS_xTe_{1-x}, shifting the electrical junction from the metallurgical interface further into the CdTe. If the V_{oc} could be increased, the potential benefit of using a window layer with a wider optical band gap could potentially increase device conversion efficiency by over 3%.

2.11.7.2Glass/ITO Reflection

Losses due to interfaces (glass, ITO) still limit maximum efficiencies; however, several authors have thought it worthwhile to investigate textured surfaces towards alleviating the problem of reflected light. Yamaguchi *et al.* [69] suggests the potential of textured front ZnO and the use of an antireflection coating to improve optical absorption in thin $Cu(In,Ga)Se_2$ solar cells.

Chu *et al.* [70] comments on using hydrogen post-treatment (on films grown by photochemical vapour deposition) to increasing the haze ratio ((scattered light transmission factor/total light transmission factor)×100(%)) or roughness of the ZnO film, in order to increase the photon scattering in photovoltaic devices.

Amin *et al.* [71] have also investigated the use of textured TCO's towards increasing the possible reflections of photons, in very thin 1 μm absorber layers. Using textured TCO's, Amin *et al.* [71] found that the largest improvement came from the most rough and therefore higher haze ratio TCO, having a haze ratio (of 37%).

2.12 Outstanding issues in CdTe

2.12.1 Cell thickness: thinner cells

In present production, the CdTe thickness grown has to be thick enough to gain full uniform surface coverage. With CSS, this is typically 5 to 10 μm. Theoretically, given CdTe's high absorption coefficient, 1-2 μm should be all that is required for the absorption of all useable photons. When the absorber thickness is reduced beyond the absorption limit (~1 μm), the cells are expected to suffer from incomplete absorption of the spectrum, especially from the infrared.

Having a very thick layer is a disadvantage for, i) materials usage, ii) deposition time, and iii) production cost. Unfortunately, thin or porous films tend to decrease the production yield, especially when wet etching processes or treatments are present. Thus when the production technique does not yield compact, closed films, a minimum thickness is required for technological reasons. Some experimental work on ultra thin CdTe absorber devices (using CSS) have been reported previously [53], but to the authors knowledge, no ultra thin work by MOCVD has been previously reported. The influence of CdTe thickness, for ideal, compact cells, has also been addressed by modeling [72, 73] and will be discussed further in the thesis.

When the CdTe thickness is further reduced to the 100 nm range and below, a planar cell concept does not allow absorbing a substantial part of the light in the CdTe.

Cells with an extremely thin absorber (ETA cells) use a porous window material, usually TiO_2, and an extremely thin CdTe layer penetrating into the TiO_2 [74].

Albin *et al.* [75] suggests that the need to reduce CdTe film thickness from a cost and material utilization perspective may require modification of the back contact etch process. The tendency of forming deep penetrating tendrils of Te-rich material using this etch is detrimental to making thinner devices. One suggested approach to increasing the stability of thinner CdTe devices is to avoid aggressive etches like NP while possibly incorporating other mechanisms, like Cu oxidation, as a means to reduce dopant mobility.

The Centre for Solar Energy Research (CSER) group, previously [76] studied planar CdTe solar cell structures with extremely thin absorbers, gaining insights into the possibility of MOCVD to grow high quality layers. Comparison of TCO/CdS/CdTe devices showed an increasing tendency for shorting in the structures with thinner CdTe. However, it was concluded that with comprehensive cleaning of the substrates, very thin absorber devices without pinhole shorting could be achieved.

Reinhardt *et al.* [77] report that a direct correlation has been found between decreasing efficiency with increasing "dark current" (the presence of the excess majority carriers at the edges of the depletion region), and as such is a quantity that needs to be curtailed.

Viswanathan [78] explains that the "dark current", has the effect of forward biasing the p-n junction. This in turn causes the potential barrier to reduce, thereby aiding the diffusion of majority carriers across the junction. Thus it can be seen that the separated photo carriers cause a current that opposes the photo-generated current. This current equals the current generated by the forward biased diode in the dark. The dark current is hence a parasitic component that needs to be minimized to obtain the maximum current from the cell. This is usually achieved by increasing the minority carrier diffusion length in the base or reducing the absorber thickness. Hence if the absorber thickness can be reduced the effect of the parasitic dark current can also be reduced.

As the cells become thinner, the electron current increases and a strong voltage dependence of the electron current causes both light and dark curves to increase faster with forward bias; the cell is now operating in the photoconductive mode, with electrons freely injected at the front contact.

Decreasing the CdTe thickness also makes the possibility of CdTe as a top cell in a tandem cell arrangement. In the polycrystalline thin-film tandem cell project, the most critical work is to make the top cell transparent in the NIR region. Wu *et al.* have been able to obtain a CdTe cell a transmission (>70%) in the NIR wavelength region [79]. This was achieved by using a thin, low-band gap Cu_xTe transparent back-contact; and a modified CdTe device structure, including three novel materials: cadmium stannate TCO, $ZnSnO_x$ buffer layer, and nanocrystalline CdS:O window layer to improve transmission in the NIR region while maintaining high device efficiency.

Reducing the thickness of the CdTe could reduce the required carrier path length, increasing the probability of the carrier reaching the junction earlier, and increasing efficiency. The expected decrease in J_{sc} at smaller thicknesses due to lessening of the absorption volume can be counteracted as surface recombination at the back contact is limited by diffusion across the field free region which is smaller for thinner cells. This suggests that effectively J_{sc} appears to stay constant as the absorber thickness is reduced, until a given point when the absorption volume is below a critical point an absorption losses become apparent.

The reduced absorber thickness inevitably mean that charge carriers are increasingly generated in proximity to the back contact, with minority charge carriers being able to reach the back contact as a result of diffusion, thereby reducing the current generated by the majority charge carriers.

2.12.2 Similarities between ultra thin and Extremely Thin Absorbers (ETA) cells

As the thickness of the absorber is reduced towards a few hundred nanometres, its thickness becomes similar to that of ETA devices. In the ETA-solar cell, the absorber layer is spread over the enlarged surface area of a porous substrate. This allows a substantial reduction of the local thickness of the absorber while the total absorber thickness remains sufficient for the absorption of solar light.

The decreased local thickness allows a proportional reduction of the carrier transport distance in the absorber, thereby relaxing requirements for the electronic quality of the absorber material. Due to the small absorber thickness the internal junction fields are expected to penetrate a substantial portion of the thin absorber layer.

In addition, the highly structured interface is favourable for optical light trapping, since it substantially reduces the specular reflectance and enhances the diffuse reflectance. This leads to a longer optical path in the absorber layer. Work by Ernst *et al.* [80] has shown, that with extremely thin absorber devices, the proximity of the back and the front contacts do not show a significant influence on the cell performance (while the interface passivation seems to be of importance for the solar cell parameters), and draws attention to the large interface area of the ETA device.

Here one would first think of the increase of the dark saturation current, i.e. decrease of the open circuit voltage when increasing the active area. Ernst *et al.* [80] report that the dark saturation current is rather determined by the involved barrier height at the junction favoured by the wide band gap semiconductor and less influenced by the junction area itself.

The results from Ernst *et al.*[80], agrees with the hypothesis, that the charge collection in the device is field supported, and indicates, that as the internal field is reduced, a strong increase in the recombination rate sets in. Since additional experiments on planar structures indicated satisfactory bulk properties of the CdTe, it is believed that recombination occurs primarily at the enlarged front and back contacts in these cell structures.

2.12.3 Grain boundary / Size effects

In polycrystalline solar cells, grain boundaries are considered important, since they potentially influence: i) carrier recombination; ii) carrier transport — by the influence of the grain boundary potentials; and iii) diffusion processes in the cell material.

A general account of possible grain boundary effects is given by Matsumoto *et al.* [17]. The grain size in polycrystalline CdTe solar cells often depend on the individual deposition technology and growth conditions, but are often in the order of a few μm thick. It is thus comparable to the various characteristic lengths of a solar cell: absorption depth $1/\alpha$, diffusion length L_n, depletion layer width W. Matsumoto *et al.* [17] states that therefore, an influence of the grain structure on the cell performance is to be anticipated.

The quantitative influence of the polycrystalline nature of CdTe cells was estimated by Sites *et al.* [58], who compared single crystalline GaAs with polycrystalline CdTe. Both materials have similar band gaps CdTe E_g = 1. 5 eV, GaAs E_g = 1. 43 eV and have thus, in principle, the similar photovoltaic potential. However, the efficiency span between the best GaAs cell (25.7 %) and the best CdTe cell (16.5 %) is 9.2 %, and between half and two thirds of that difference Sites *et al.* [58] ascribes to the polycrystalline nature of CdTe.

To understand if cell performance is limited by grain bulk, grain surface, and/or grain boundaries (GBs), Cahen *et al.* [81-83] have performed high-resolution mapping of electronic properties of single GBs and grain surfaces in poly-crystalline p-CdTe/n-CdS solar cells.

By combining results from scanning electron and scanning probe microscope, capacitance-voltage, Kelvin probe, and conductive probe atomic force microscopy, Cahen *et al.* [81-83] were able to eliminate topography-related artefacts to make the following conclusions.

1) Current is depleted *near* GBs, while photocurrents are enhanced along the GB cores; (implies that the regions around the GBs function as an extension of the carrier-collection volume, i.e., they participate actively in the photovoltaic conversion process)

2) GB cores are inverted, which explains GB core conduction. (this implies minimal recombination at the GB cores);
3) The surface potential is diminished near the GBs;
4) The photovoltaic and metallurgical junction in the n-CdS/p-CdTe devices coincide.

These conclusions, taken together with gettering (process of removing device-degrading impurities from the active regions of a semiconductor) of defects and impurities from the bulk into the GBs, explain the good photovoltaic performance of polycrystalline cells compared to their single crystal version. Cahen *et al.* [81, 82] also show that these CdTe GB features are induced by the $CdCl_2$ heat treatment.

Durose *et al.* [84] state that the grain boundary density of states is a function of the impurities in CdTe, and state that the only measurements reported for CdTe were for material containing dopants [59], which are very different to modern $CdCl_2$ -treated devices. Indeed, recent models of the electrical environment of grain boundaries in p-CdTe (in devices) invoke local upward band-bending that would act to repel minority carrier electrons. Models produced by Levi *et al.* [85] and Edwards *et al.* [86] share this feature, but differ in detail, with the former allowing for electron capture close to the boundary interface.
Lakus-wollny *et al.* [87] comments on the fact that the larger the grain, the poorer the grain/grain contact, as any gaps in-between the grains can act as a channel for the etchant solution, potentially creating a region of a weak diode.

According to Smith *et al.* [88], the final grain size in CdTe polycrystalline films increases with film thickness, as the grain size becomes larger, the relative effect of grain boundaries on recombination become less important.
The crystallographic orientation and texture of the grain of the CdTe layer depend heavily on the underlying CdS window layer. Berrigan *et al.* [89] have shown that it is possible to control the CdS nucleation by MOCVD. This would allow the possibility of "grain templating", towards control of the underlying CdS layer, which could potentially make it possible to actively manipulate the CdTe grain size.

2.12.4 P-type doping of the absorber layer

Given the native defect character of CdTe, p-type doping can be difficult to achieve. Attempts at controlling extrinsic doping, can lead to complex self-compensation mechanism which limit the effective dopant concentration.

Zunger [90] comments on the deliberate *p* doping by acceptors. The shifting of the E_F towards the valence band, will initiate (at some point) a *p*-type pinning energy, and the spontaneous formation of native ''hole killers'' such as anion vacancy or cation interstitial, at which point *p*-type doping is defeated.

Morales [91] suggests that if the doping concentration could be increased to 1×10^{18} cm^3 by extrinsic doping, one could then expect improvement in the solar cell open circuit voltage. He also notes, after comparing results from various CdTe devices grown by a variety of methods, that the effective diffusion length can be anywhere in the region of 1 μm to 8 μm, given the variety of CdTe thicknesses grown. Thus, diffusion length is device (thickness and material quality) and deposition method specific, thus requiring a large amount of doping knowledge for each separate technique.

2.12.5 Doping Compensation

Compensation is the act of one defect cancelling out the doping effect of another. The simplest version of compensation involves an electron from a shallow donor state filling a shallow acceptor state. This effect temporarily removes both the donor and the acceptor from acting on the device [92].

Undoped semi-conducting CdTe is p-type due to a slightly Te-rich Stoichiometry, which causes a [V_{Cd}] acceptor sites. If chlorine is added to an undoped p-type CdTe, compensation of the acceptors takes place, making the material semi-insulating. Cavallini *et al.* [92] postulates that this occurs through the [Cl_{Te}] sites. However, in the case of this particular thesis, as arsenic is used to dope the CdTe in-situ, the $CdCl_2$ treatment is added to an already doped CdTe bulk, thus the compensation mechanism that can takes place is likely to be more complicated and more difficult to measure.

The Arsenic doping could potentially remain in the internal structure of the CdTe grains, with the $CdCl_2$ treatment passivating the grain boundaries. If this is the case, it would separate the two treatments in terms of outcomes, but as both can be considered as dopants, it is likely that some interactions do take place between them.

2.12.6 Etching

Gilmore [93] states that unlike the $CdCl_2$ treatment, which only affected the shallower defect states, the bromine methanol etch seems to affect both the shallower defects as well as the deeper defect state densities. The bromine methanol etch lowers the defect state density for the shallower trap level or band, and increases the defect state density for the deeper trap level or band. The wet etch produces a Te-rich layer near the back contact, thereby increasing the tellurium to cadmium ratio, which results in more cadmium vacancies and in particular a higher concentration of doubly ionized cadmium vacancies [VCd''']. Since the deeper level or band is associated with VCd'', then it is consistent that samples which have undergone the bromine methanol etch would exhibit a higher concentration of these defects.

The bromine methanol etch may remove excess chlorine from the surface prior to the application of the back contact. Excess chlorine can form a compensating defect complex consisting of a cadmium vacancy and chlorine substitutional on a tellurium site [V_{CdClTe}] [93]. With less chlorine present after the methanol/bromine chemical etching, fewer of these complexes would form, and more cadmium vacancies would therefore remain.

Treatment with bromine-methanol after the deposition and anneal of the back contact (typically Cu/Au contacts), is known to increase the device's open circuit voltage (V_{oc}) [15, 26, 27] (a property normally attributed to the quality of the main junction), and decrease the device series resistance (R_s) (a property often treated as indicative of back contact quality). The etch treatment may also remove residual surface oxides beneath the back contact, resulting in Te-enrichment. When copper is used, the Te-enriched surface forms Cu_2Te.

The bromine-methanol (Br-meOH) etch also reduces roll-over in the IV curve which is expected for a contact that is doped highly p-type.

The effects observed with post contact etching are reported to be due to interactions occurring within the grain boundaries (GB's) [94], as the thin metallization layer is expected to be porous after deposition on a rough CdTe surface, the etch may "move through" the back contact, removing oxide at the CdTe/metal junction.

2.12.7 *PN junction* Location

The actual physical location of the main *pn* junction is also under much debate, the precise position of the electrical junction can vary largely depending on both the deposition technique and any post-deposition treatment. The CdS/CdTe metallurgical interface is taken as the region where the pn junction resides, but is not strictly true, as the pn junction can reside a large amount inside the CdTe.

A contactless Electro-reflectance Spectroscopy (EER) method used at the University of Bath, U.K. [95], would allow for the measurement of effective charge at varying depths of layers, and can be use towards the investigation of junction locations.

Optical measurements, using an optical beam induced current (OBIC) setup has been used by Major *et al.* [96] to investigate the effective *pn* junction location (in-situ) from cross-sectional films with some success.

2.12.8 Nature of the pn junction

Dharmadasa *et al.* [97] suggests, that the very slow progress of CdS/CdTe solar cell development is noteworthy as it has taken eight years of worldwide research to increase the efficiency by only 0.6% from 15.9% [98] to 16.5% [48]. Dharmadasa *et al.* [97] comments that the rapid development of the CdTe-based solar cell has been hampered mainly by a lack of understanding of the physics of this device structure.

The Currently accepted model based on a p–n junction consists of two semiconducting layers a wide band gap n-type CdS (E_g = 2.42 eV) layer is used as the window material and a narrower band gap CdTe (E_g =1.45 eV) layer is used as the absorber material.

If the CdTe layer is p-type, then the active junction is a simple p–n type hetero-junction, and the required internal electric field within the device is provided by this interface.

A new model for glass/TCO/CdS/CdTe/metal solar cell has been proposed by Dharmadasa *et al.* [97, 99]. This new model explains the device behaviour in terms of a combination of a hetero-junction and a large Schottky barrier at the CdTe/metal interface.

The Schottky barrier forms a metal/n-CdTe interface (Fig. 2.12), Dharmadasa *et al. [97]* states that the Schottky barrier formation is found to be governed by Fermi level pinning at one of the five possible discrete levels. Depending on the history of the material, fabrication process and the metal contact used, the Fermi level pinning will take place at one of the five pinned Fermi levels.

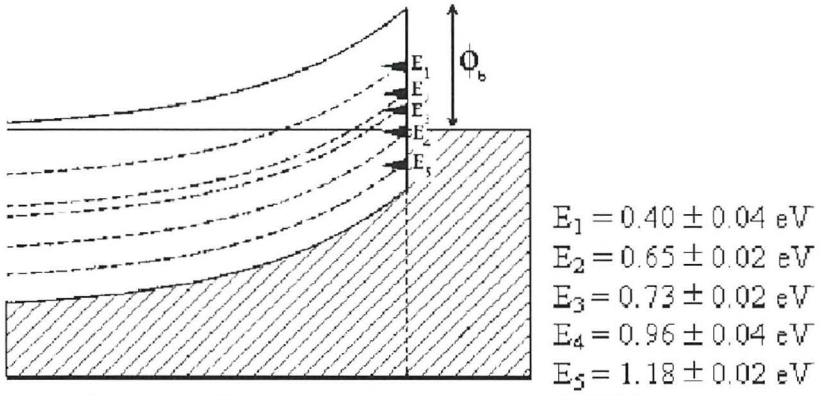

Figure 2.12: The ladder of Fermi level pinning positions. After Dharmadasa *et al. [97].*

Dharmadasa *et.al.* [97], states that the high density of these local defect states can be found in the top surface layer with a thickness of a few 10 nm, and some of these defects coincide with the native defects found in the bulk material. The thickness of this modified surface layer depends on the surface treatment and etching prior to metallization.

This model has been formulated using the complex results observed for metal/n-CdTe interfaces as summarized in Fig. 2.12. Although the photo-generation of charge carriers from different parts of the device is indicated, the energy band diagram represents the thermodynamic equilibrium under dark conditions [97]. This is a weakness of this particular model, and measured I-V of devices (MOCVD, grown for this thesis) clearly show a large change in the shape of the I-V curve between dark and light I-V curves (Fig 2.13)

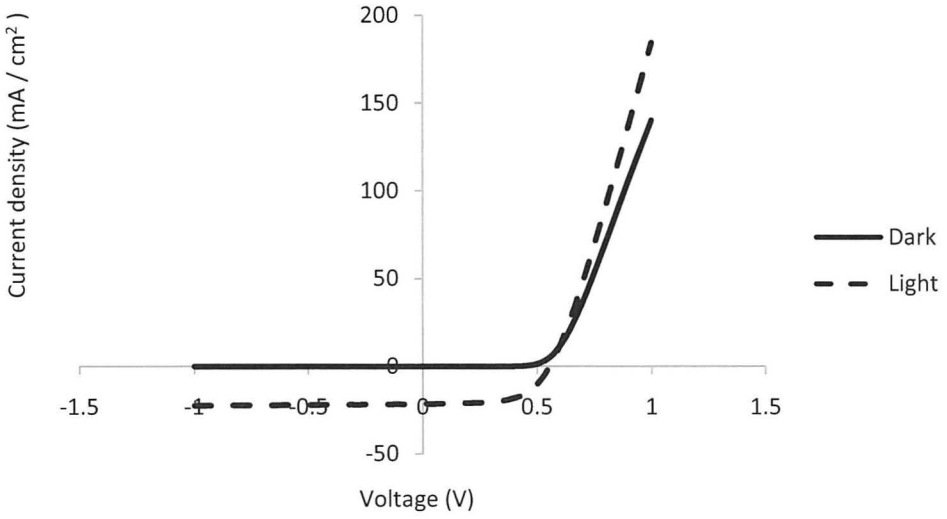

Figure 2.13: measured I-V of 7% efficient CdS/CdTe device, depicting different I-V shapes between dark and light curves.

During the annealing process, intermixing of CdS and CdTe can take place, forming a ternary compound, creating a graded band gap interface at the hetero-junction. Here, the bulk of the CdTe layer remains n-type, and the outermost layer contains high concentrations of defects responsible for Fermi level pinning, at one of the five experimentally identified levels. The thickness of the top surface layer varies in the region of a few 10 nm depending on the processing steps such as the heat treatment and etching procedure.

If one considers the Fermi pinning model, when the Fermi level is pinned close to the valence band, a large Schottky barrier will form at the metal/CdTe interface, creating the required band bending across the device for photovoltaic activity. The top surface layer of the CdTe material can then be considered as p-type, since the Fermi level is close to the valence band maximum. The final device can be completely or partially depleted depending on the doping concentration achieved for the CdTe layer during growth and subsequent processing. To produce an efficient solar cell structure, the Fermi level should be pinned close to the valence band maximum. Both materials in the device structure remain n-type, and thus can be treated as an n-n-Schottky barrier structure.

Dharmadasa *et al.* [97] states that since this is a metal/semiconductor (MS) type rectifying contact, the introduction of a thin insulating layer to form metal/insulator/semiconductor (MIS) type structure could enables further enhancement of V_{oc} and lifetime of the device.

As the Fermi-pinning model, states that both window and absorber materials are n-type, doping with n-type dopants instead of p-type dopants will improve the electrical conductivity of the device, enhancing both the J_{sc}, and FF. Dharmadasa *et al.* [97] also explains that the Fermi-pinning model would also explain the 'magic step' of empirical $CdCl_2$ treatment necessary for achieving high efficiencies, as chlorine acts as an n-type dopant to both n-CdS and n-CdTe materials reducing the series resistance in addition to observed grain growth.

In both the Fermi pinning model and the standard pn junction model, electrons flow towards the TCO, and holes flow towards the back metal contact, making the TCO layer negative and the metal contact positive in polarity. In C-V analysis, according to both models, *C–V* measurements are possible due to the presence of at least one active interface within each device structure.

Dharmadasa *et al.* [97] states that if the device is fully depleted due to low doping concentrations of CdTe, in the region of 10^{15} cm^{-3} or below, capacitance values remain almost unchanged with the applied bias voltage and approximately equal to the geometric capacitance of the structure. If the doping concentration is such that the depletion region covers only a part of the CdTe layer, then the capacitance varies according to the applied bias voltage providing linear $1/C^2$ versus voltage plots and the estimated doping concentration lies in the range 10^{16}–10^{17} cm^{-3} , which agrees well with reported values [100, 101].

Prior to the deposition of the back contact, an etch treatment is usually carried out which creates a Te rich layer on the surface of the CdTe, effectively lowering the Schottky barrier upon metallization. However, a Te-rich surface is susceptible to oxidation. Possible oxides that may form are TeO_2 [10], $CdTeO_3$ [102] or a mixture of both. Oxidation of Te and CdTe functions as a degradation mechanism in un-encapsulated CdS/CdTe cells, and is known to occur beneath the back contact itself [102].

According to the Fermi level pinning model [97], a highly doped back contact metal, with ether Cu/Au, Cu/Ni or Sb containing contacts (which are good candidates to produce low resistance contacts) should be avoided.

As the in-diffusion of a p-type dopant into the n-type CdTe layer could form a very resistive electrical contact with ageing. If this happens, and the efficiency drops considerably, it should be possible to remove the entire back contact using chemical etching (post-contact etching) and reproduce the working device again if there is no damage to the thin-film structure. This procedure should reproduce the high efficiency devices [97].

However, the Fermi-pinning model does not discuss grain boundaries and their associated effect. This is a short fall in the model, as, research carried out by Fisher *et al.* [82], provides evidence for grain boundary depletion, and as such, this model, in its current form cannot fully describe, or model, accurate device physics.

2.13 Modelling of the CdS/CdTe heterojunction

Access to the software was made available thanks to Prof. M Burgelman [103]. The software developed by his team, allows 1-D modelling of semiconductor layers and solar cell devices. In order to accurately model the CdS/CdTe junction, physical limits need to be known. The CdTe and CdS used in these cells are polycrystalline; hence the mobility will most likely be lower than that for a single crystal. Streetman [104] has identified typical intrinsic parameters for single crystal and these values can be considered to be upper limits on CdTe/CdS solar cell mobility's.

In the solar cell, all the electrical parameters such as the open circuit voltage V_{oc}, short circuit current J_{sc}, fill factor, and efficiency each have upper limits to what has been obtained and what can be obtained. For instance, in CdTe/CdS solar cells, an efficiency of 16.4% has been obtained [48], while the maximum obtainable efficiency is around 27% [46].

The amount of current flowing through the device when no bias is applied in light, J_{sc}, has an upper limit based on the amount of sunlight that can be absorbed by a material with a certain band-gap. For CdTe, the maximum J_{sc} is approximately 28 mA/cm^2 [46]. That assumes that all incident light, with energy greater than the band-gap is converted to collectable current within the device. When fundamental limitations are known, the areas to concentrate further research on for improvement of the device will become evident.

2.13.1 Modelling of ultra thin CdTe devices

Software modelling has been useful towards the investigation of the effects of reducing the absorber thickness. Amin *et al.* [71] have suggested the use of thinner absorber devices. CdTe layers are currently grown between 5-10 μm thick by presently available technologies such as CSS [105]. For further improvement in the open-circuit voltage (V_{oc}), by controlling the recombination loss at the bulk, and to make the CdTe solar cell more attractive for practical use by reducing the material used, the absorption layer of CdTe should be of minimum thickness. The minimum thickness for CdTe to directly absorb 90% of the incident spectrum, (using the absorption coefficient of $2x10^4$ cm^{-1} at 800 nm) is approximately 1 μm.

Several other computer models have been created, e.g. Amin *et al.* [73] have developed a 1-D simulation program for solar cells named NSSP (Numerical Solar Cell Simulation Program). The NSSP software program has been used to analyse reducing the absorber thickness (Fig 2.14) and calculate the expected carrier generation as a function of absorber thickness (Fig 2.15).

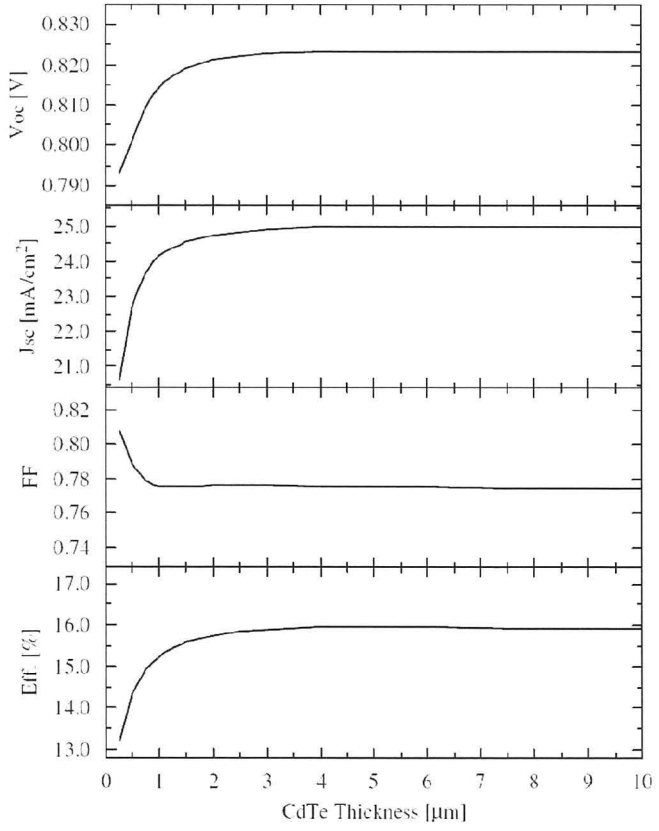

Figure 2.7: Modelled data of the effect of the CdTe thickness reduction on the solar cell characteristics from calculation. After Amin *et al.* [73].

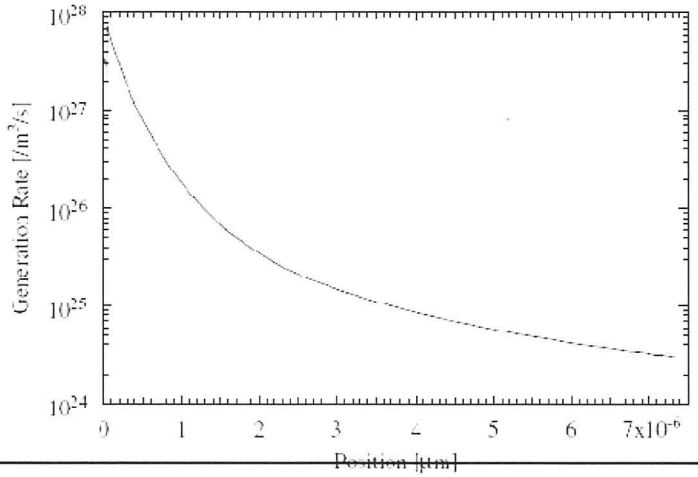

Figure 2.15: Modelled data of the calculated carrier generation rate in the CdS/CdTe solar cell with thickness. After Amin *et al.* [73].

Figure 2.15, shows that reducing the absorber thickness, and inevitably means that charge carriers are increasingly generated in closer proximity to the back contact, with minority charge carriers being able to reach the back contact as a result of diffusion. This reduced the current generated by the majority charge carriers.

A useful observation by Amin *et al.* [73], is that of the back surface field (BSF). This is the effect when a higher band gap material (e.g. ZnTe) is placed at the back contact to inhibit the minority carrier loss at the back contact. Amin *et al.* [73] observed a 20% improvement in conversion efficiency due to the BSF induced by the deposition of a ZnTe layer at the back contact (Fig 2.16). For the device which had the BSF, the V_{oc} is seen to increase when the thickness of the absorber (CdTe) is reduced below 1μm, contrary to the standard CdS/CdTe device, thus it can be a useful hint to whether some BSF effect may be present in a particular device.

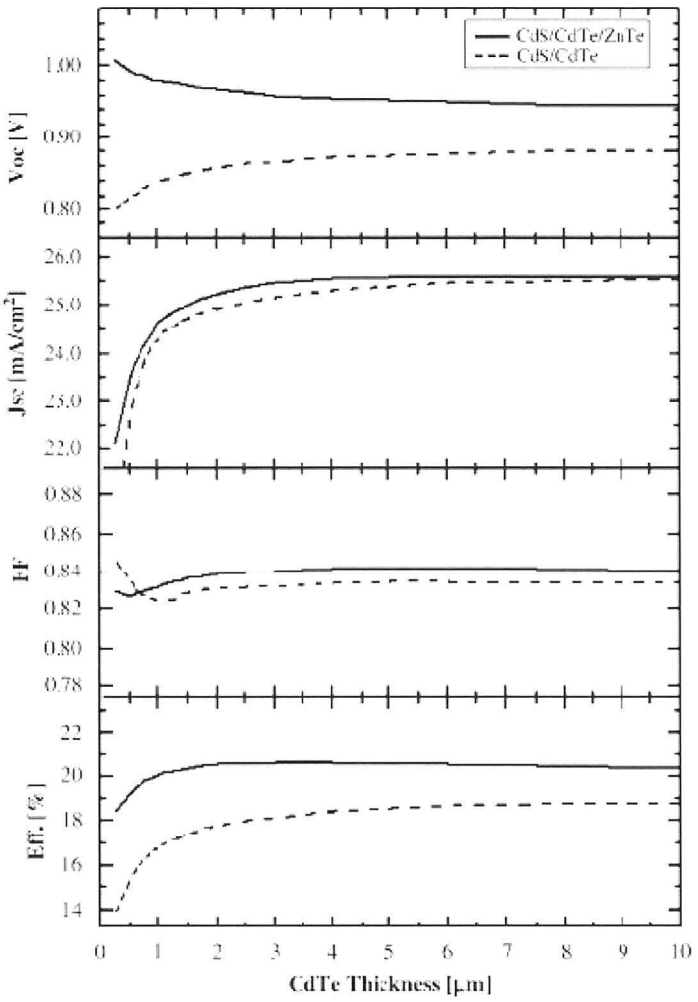

Figure 2.16: Modelled data of a CdS/CdTe device and a CdS/CdTe/ZnTe (BSF) device.

2.14 The $CdCl_2$ activation treatment

The $CdCl_2$ treatment concerns the conversion of CdTe from n- to p- type, it lowers series resistance and is accompanied by a change in current transport mechanism from a tunnelling/interface recombination to recombination in the depletion region [106].

Current transport studies, (temperature dependent I-V analysis) before and after $CdCl_2$ treatment indicate a change in the current transport mechanism. $CdCl_2$ treatment improves the microstructure of the CdTe films and eliminates active states at the CdS/CdTe interface, presumably by inter-diffusion [107], thereby changing the current transport mechanism.

Bayhem *et al.* [108] concludes that the electron transport mechanism is dominated by recombination at the CdS/CdTe interface prior to the $CdCl_2$ treatment and by depletion-region recombination after the treatment. This suggests a decrease in the density of interfacial states, partly due to the reduction in the volume fraction of material influenced by grain boundaries due to $CdCl_2$ grain growth. Bayhem *et al.* [108] also states that an additional benefit of the $CdCl_2$ treatment lies with the improvement of p-doping in the CdTe layer (by creating a shallow acceptor complex, ($V_{Cd\text{-}ClTe}$). This is a necessary step in applying an electrical contact to CdTe (back contact). Other benefits of the $CdCl_2$ treatment may include improvements in micro-uniformity [109] p-type carrier concentration in the CdTe layer, and elimination of some defects [110].

Some negative side effects of the $CdCl_2$ treatment have also been observed. These include excess inter-diffusion between the CdS and CdTe layers [111], compensation [112] introduction of defect complexes [10] and surface residues that may increase contact resistance [113].

2.15 Back contact

Producing Ohmic contacts on CdTe is difficult since a material with high enough work function is not available. For p-type material, the etch produces a surface layer rich in tellurium which results in a highly p-type region on the surface of the CdTe layer [114]. This has been the main reason why very thick absorber layers have been used, as the highest performance devices use Cu as a critical constituent, which is known to rapidly diffuse [115] into the CdTe layer, eventually decreasing operating efficiency [75].

The forward-bias enhanced diffusion of Cu^+ from the back contact region to the CdS/CdTe hetero-junction during accelerated life tests performed by heating devices under illumination and open-circuit voltage (V_{oc}), is believed to be responsible for both back contact degradation [116] as well as decreased voltage due to increased recombination [17] in devices containing Cu. Albin *et al.[75]* state that a strong possibility exists for diffusion processes to occur, affecting Cu mobility and thus, the stability of Cu containing CdTe devices.

In regards to CdS thickness, it has been [117] proposed that carrier compensation and the introduction of deep states in the CdS layer may be responsible for reduced performance. In this case, CdS thickness may also play a role.

The approach for applying an improved back contact for MOCVD grown devices was first attempted by Barrioz *et al.* [44]. Barrioz *et al.* [44] states that there are currently two main approaches for decrease the back barrier height;

1. Increasingly dope a thin layer of absorber near the back contact effectively creating a p^+ layer enabling the majority carriers to tunnel through the Schottky barrier (and lower the surface carrier recombination); and/or
2. Reduce the valence band offset at the back contact, by depositing a p-type intermediate layer (e.g. ZnTe), so that the barrier is effectively reduced.

Although CdTe is known to be a self-compensating material, being difficult to dope at high active acceptor concentrations, Barrioz *et al.* [44] has shown that it is possible to dope CdTe highly p type, using arsenic, where doping concentrations up to $10^{18}cm^{-3}$ could be substituted for Te into CdTe layers.

The possibility of using arsenic as a dopant [118] for the CdTe layers, towards inducing p+ layer near the back contact, has been investigated with some success improving the back contact series resistance (R_s from 10 Ω cm^{-2} to 1-2 Ω cm^{-2}.). However, care must be taken to optimize the level of incorporated arsenic as the V_{oc} level is also effected (Fig 2.17).

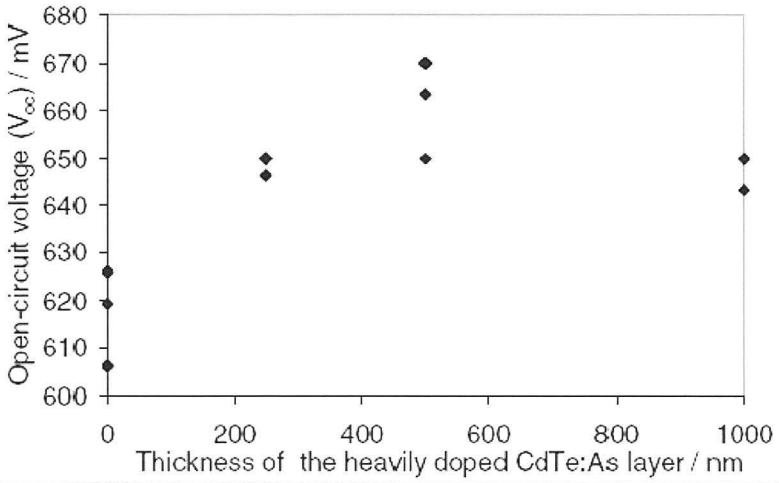

Figure 2.8: Graph showing the change in the Voc as a function of the thickness the heavily doped CdTe:As layer. The device without a BCL (zero heavily doped CdTe:As layer thickness) was etched with Bromine-Methanol etchant. after Barrioz *et al.[44].*

The use of spontaneous deposition through auto-catalytic chemical process, or ''electroless''[119] process used for depositing contacting materials. One advantage of the electroless technology is that a combination of materials can be introduced during deposition process. This combination can modulate the work function of the individual material and develop an effective work function to match with semiconductor. Gosh [119] reports that the work function and bulk resistivity of Ni composite can be modulated with other materials like, Cu, Au, Mo, W and Co.

2.16 Industrial research trends

Listed below are First Solar stated [23] future research targets and expected device increases;

- Light collection (2% expected increase)
- Glass transmission improvements (expected 5% increase)
- TCO improvements (>10% increase)
- Improved CdS uniformity
- Antireflection coating
- Reducing CdS thickness to increase high energy photon capture
- Constant drive towards thinner CdTe (purely financial)

2.17 Research Focus

Thus, the current active area of research by both industry and academia are; improved device uniformity, improved photo-current and reduce the thickness of the absorber layer (although, in industry this is merely a financial target, as less material, and the need to etch the material down can be eliminated, lowering cost).

This thesis will aim to increase the understanding of the relationship of layer quality with device quality and performance allowing a fundamental investigation towards increasing the conversion efficiency, through understanding what makes a good layer or front/back contact region will be undertaken. If the relationship between the layer quality and the end device performance can be better understood, the evolution of absorber thicknesses with device performance can be investigated.

MOCVD growth rates are currently too low to achieve the desired in-line process speed above 10 cm/min and new developments (other precursors, or increased pressure) would be needed in the deposition kinetics. Research will also focus on step changes/improvements in processes which would allow for the potential of large scale MOCVD. The advantages of large scale MOCVD would be in having an atmospheric pressure process, no wet chemical steps, materials flexibility (e.g., changing layer compositions).

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CHAPTER 3

3.0 EXPERIMENTAL METHODS

The deposition of all thin film solar cells within this research (unless otherwise stated) was carried out using a custom built MOCVD reactor. This chapter details the atmospheric pressure MOCVD system, the re-installation of the reactor, along with analysis equipment used to characterise the MOCVD grown thin films.

3.1 The MOCVD reactor

The particular reactor used in this research was loaned from QinetiQ Ltd, and is primarily used for growing CdS/CdTe layers. It consists of a gas-handling cabinet and a main reactor unit. The organo-metallic (OM) precursors (Dimethylcadmium (DMCd) for Cd, Diisopropyltelluride (DIPTe) for Te and for S, Ditertiarybutylsulphide (DTBS)) are contained in stainless steel bubblers (provided by SAFC Hitech Ltd). Hydrogen carrier gas was purified (using a palladium silver diffusion membrane). Hydrogen carrier gas was bubbled through the precursors (bubblers), entraining the saturated vapours in the hydrogen gas stream and transported to the growth chamber.

The temperatures of the bubblers were kept constant, allowing the vapour pressure of the bubbler to remain constant through constant cooling (using chillers) and controlled heating (using temperature controlled baths). This allowed the temperature to be kept at equilibrium, allowing a set pressure of the precursor to be achieved. A Thomas Swan Epison concentration meter was used to measure the concentration of the precursors before each layer growth and for flow calibration prior to growth.

In order to extrinsically dope CdTe for independent control of p-type carrier concentration, Tris-Dimethylaminoarsine (TDMAAs) was used. This is achieved using a separate double dilution line (DDIL) arrangement.

The reaction chamber itself consisted of two concentric quartz tubes (Fig 3.1). A circular outer tube held in place by stainless steel end plates, and a removable rectangular liner tube onto which the graphite susceptor is mounted. The susceptor conducts the heat evenly from the resistive graphite heater. The liner tube is etched in aqua-regia (1 HNO_3: 3 HCl) between successive growths, to remove any un-intentional deposition on the walls. This is a cold walled process, and reaction of the organo-metallics should result in deposition only on the heated susceptor and the inner wall of the liner tube.

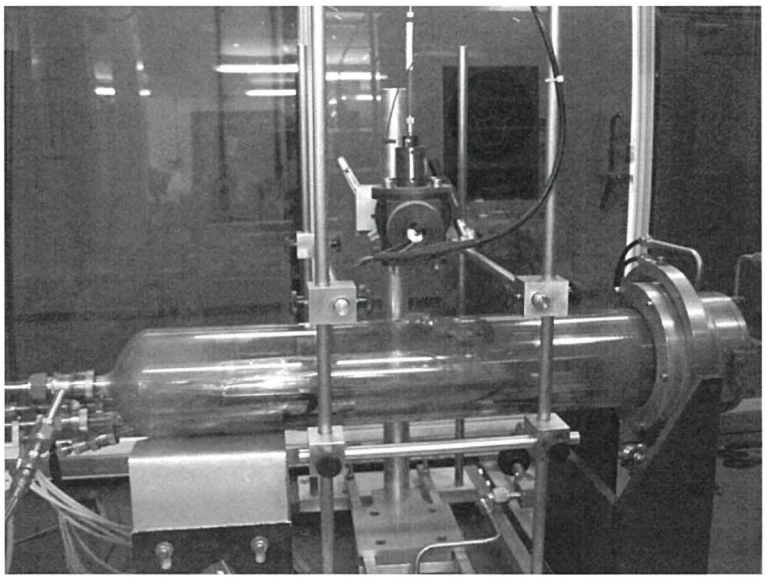

Figure 3.1: Photograph showing the MOCVD growth chamber, showing the outer reaction tube and the laser interferometer above.

3.2 Precursor control

The precursor gas path is controlled by a series of pneumatic valves, which can be toggled manually (using switches on the control panel) or by the computer. Valves can be either normally open or normally closed depending on the desired normal state for safe running of the reactor.

The precursor and carrier gas flows are controlled using mass flow controller (MFC's) (Fig 3.2). A mass flow controller has an inlet port, an outlet port, a mass flow sensor and a proportional control valve.

The MFC is fitted with a closed loop control system which is given an input signal by the operator (or an external circuit/computer) that it compares to the value from the mass flow sensor and adjusts the proportional valve accordingly to achieve the required flow.

The flow rate is specified as a percentage of its calibrated full scale flow and is supplied to the MFC as a voltage signal.

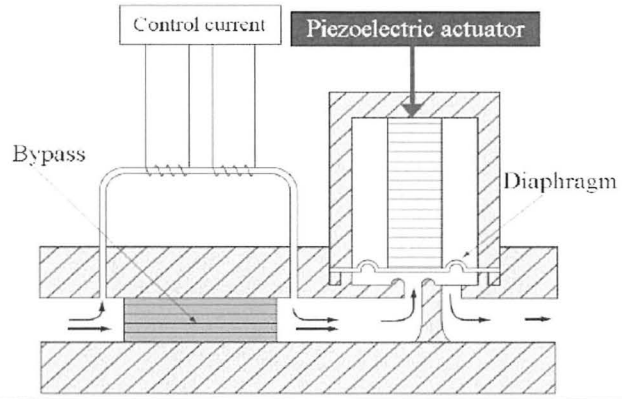

Figure 3.2: Schematic of a mass-flow controller.

Mass flow controllers require the supply gas to be within a specific pressure range. Low pressure will starve the MFC of gas and it may fail to achieve its set-point.

Before the separate group II and VI precursor gases pass over the substrate, the precursor gases need to be effectively mixed before entering the growth chamber. This is done by passing the precursor flow through a mixing chamber. This ensures a fully mixed precursor stream enters the growth chamber, and avoids the possibility of one precursor being present in larger quantities than another in different regions of the gas inlet.

3.3 Reactor setup

To avoid any back-flow of gas, the vent/run arrangement is carefully balanced. The balancing equalises the pressure of the incoming gases to avoid the possibility of back flows. The total flow remains constant in the reactor, as it affects the transport and uniformity of film thickness. The MOCVD control panel can be seen in Fig 3.3.

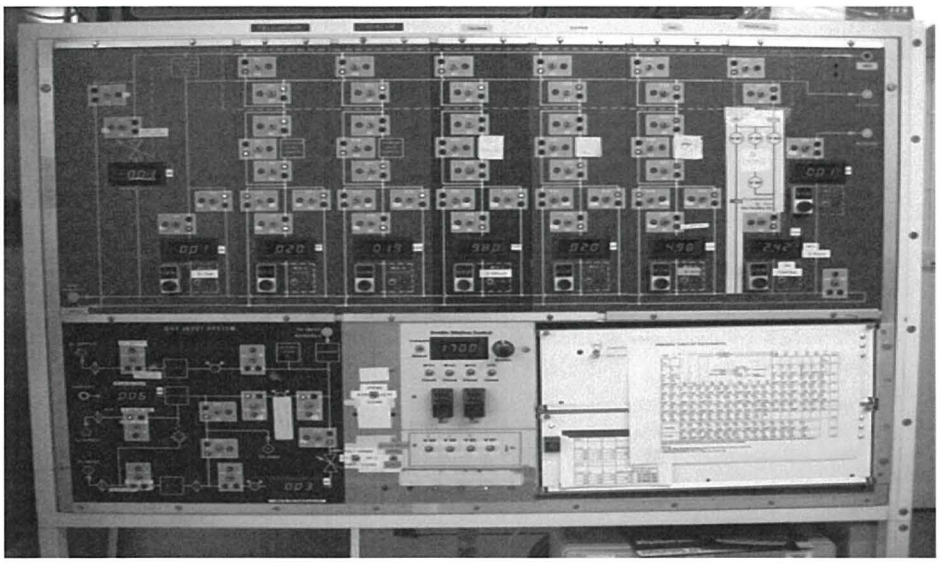

Figure 3.3: Photograph of the MOCVD control panel that enables full manual control in addition to the computer control.

The MOCVD system used, is made up of five metal-organic precursor flow lines (Fig 3.4), one double diluted line (the TDMAAs doping line), a window flow (see section 3.6) and a H_2 carrier gas line (switchable for N_2 when the growth chamber needs to be opened). Exhaust gases are passed through an EMCELL activated charcoal filter, which absorbs the remaining organic constituents of the precursor before reaching the exhaust. A vacuum line is also present and is used to vacuum down the system for bubbler changes, and test the leak tightness of the system.

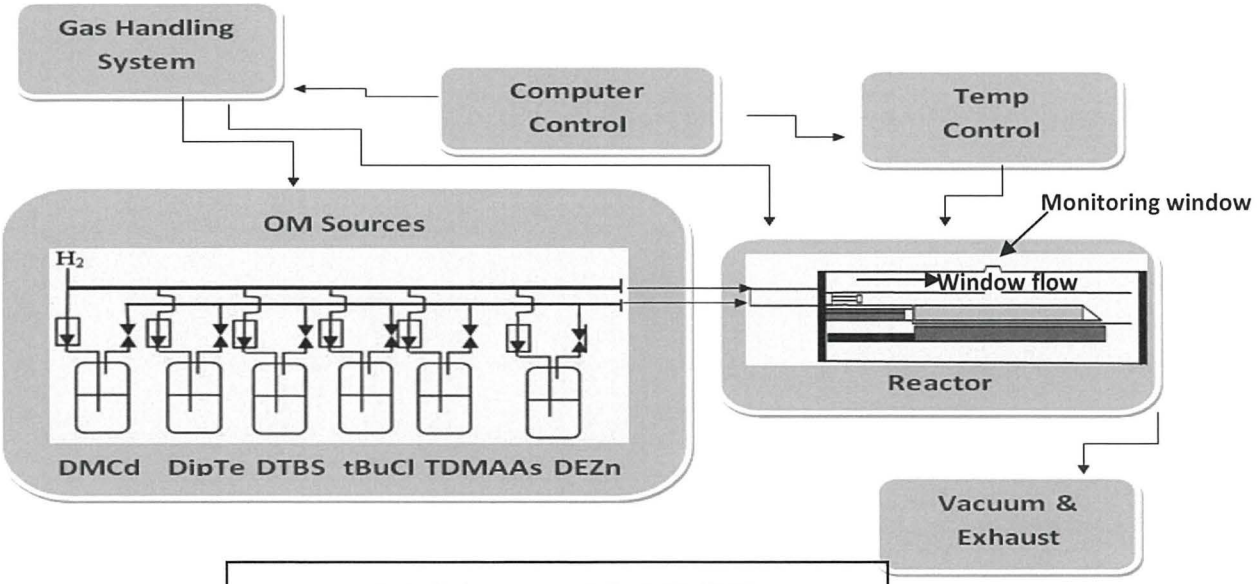

Figure 3.4: Schematic of the MOCVD system.

3.4 Calculation of the Precursor Partial Pressures

The partial pressure required for any particular deposition can be calculated using the following equations;

$$SVP\ (Torr) = \frac{Precurosr\ concentration\ (atom) \times Atm\ Press\ (Torr) \times Total\ \ gasflow\ (sccm)}{Bubbler\ flow\ (sccm)} \qquad 3.1$$

Where SVP is the saturated vapour pressure (in Torr).

Equation (3.1) can be re-arranged to give (Equation 3.2):

$$F_{Bubbler} = [C]P_{Reactor} \cdot \frac{F_{Total}}{SVP} \qquad 3.2$$

$F_{bubbler}$ (Flow of the bubbler), [C] is the concentration, $P_{reactor}$ is the reactor pressure. F_{total} is the total flow going through the reactor; at standard vapour pressure (SVP).

Leys[1] showed that the partial pressure or concentration of the precursors for MOCVD, are mostly in the order of 10^{-4} atm (1.01 mbar). The capacities of the MFCs (total sccm) were chosen with this precursor partial pressure in mind.

During a growth run, the partial pressure calculation is automatically calculated (the density of the precursor gas is proportional to the atomic number of the precursor) and measured by a Thomas Swan 'Epison' gas concentration meter. Each precursor line is sequentially switched to the Epison, allowing it to calculate the concentration present in the total flow. During the calibration before each growth run, the partial pressures are displayed in real time. This is used to calibrate the gas concentration of all the bubblers prior to deposition (which accounts for change in atmospheric pressure, temperature, amount of precursor left etc.).

3.5 In-situ monitoring

Interference can be seen as the adding together of two waves with each other. Depending on wave size (amplitude) and the degree to which they are in or out of step with each other (phase) they will reinforce or cancel one another. In the case of laser interferometry single wavelength light waves are reflected by the substrate and growing film surface creating interference patterns (Fig 3.5); which are then collected by a photo-detector. Depending on the distance *(d)* between the two reflections, destructive or constructive interference will occur.

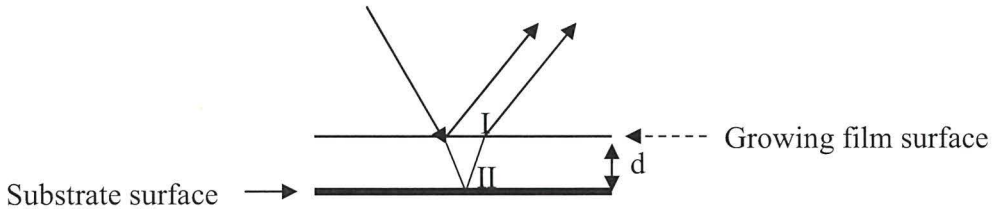

Figure 3.5: Possible film reflections.

Point I shows surface reflections of the growing layer. Point II represents reflections by the substrate surface, and the growing layer surface.

The Two slit young experiment, shows that a single coherent light source, can produce a regular pattern, caused by phase differences in the distance the light travels between the two slits. In thin film interference, the laser is reflected off the front surface, (i.e. it experiences an 180^{o} phase shift). As the light continuous its phase changes due to the index of refraction of the medium (air), it then reflects off the other interface and continuous back to interfere with the first ray. If the thickness t various across the film, so does the amount of phase shift of the light in the medium.

The Michelson interferometer, is an interferometry setup able to make measurements of distance, it consists of a laser, a beam splitter, and two mirrors. The beam splitter splits the beam into two equal intensity beams, which are reflected by two separate mirrors. The light is then passed back through the beam splitter again to produce an interference pattern. Each transition from constructive to destructive interference corresponds to a movement of the mirror by (wavelength of the laser (λ) /4), and it is this distance which is measured in laser interferometry.

Information about the film thickness *(d)* and therefore growth rate (GR) can be gained from the produced interferogram. Also, film roughening and optical properties such as the refractive index (n) and absorption coefficient can also be obtained.

The growth rate can be calculated from equation 3.3;

$$\text{half wave thickness} = \frac{\frac{\lambda}{2n_f}}{t} \qquad 3.3$$

λ = laser wavelength (nm), n_f = refractive index of thin film and t = duration in time (s) of one oscillation. This equation calculates the thickness with respect to a half wave (response from the laser monitoring), which can then be used to calculate the thickness of the growing layer.

From the number of oscillations, growth rate per unit time can be obtained. This method of measuring growth rate during deposition provides information about the reaction kinetics (e.g. nucleation time/surface quality). The effect on the growth rate of any parameter change made during deposition can be observed. As opposed to *ex situ* growth rate measurements, which rely on dividing the total thickness by the deposition time and take no account of growth rate changes during deposition.

Figure 3.6 shows an example interferometer profile for CdS n = 2.5 and CdTe n = 2.7 [2], deposited by MOCVD within this research. The features to note are: the periodicity which shows the changing growth rate between the two materials and a roughening of the surface, which increases light scattering, and decreases laser sensitivity.

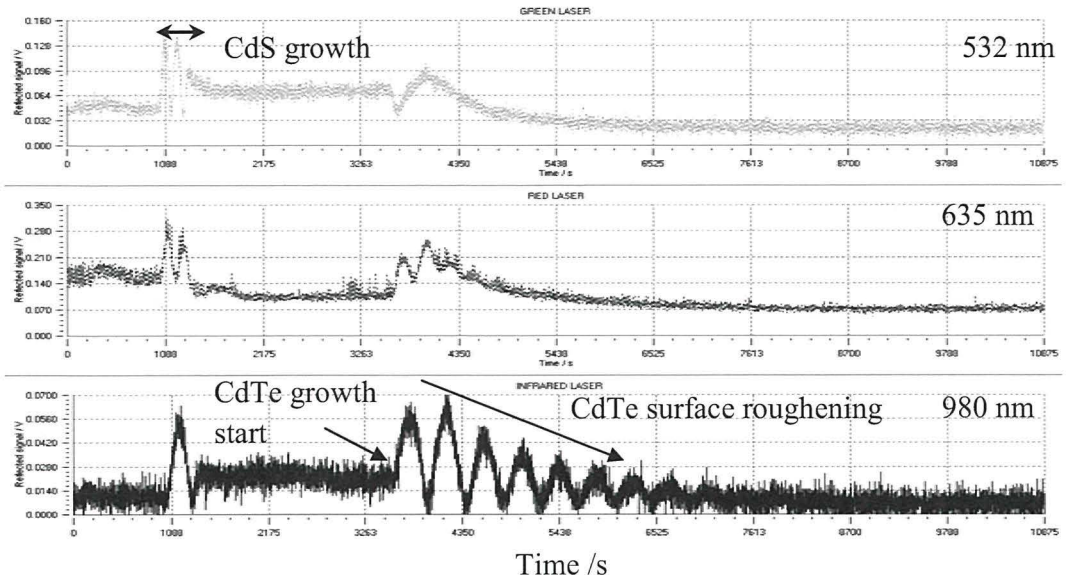

Figure 3.6: Interferometry pattern (due to Fabry-Perot interference) during a CdS/CdTe device growth. The three lasers, guided by fibre optics, operate at wavelengths of 532 nm (good for CdS), 635 nm and 980 nm (good for CdTe).

Laser interferometry in thin film deposition by MOCVD allows the following information to be obtained.

- **The nucleation time** – is indicative of initial substrate surface quality, and so can give information regarding film cleaning, blockage/ or empty bubbler if no growth is observed.
- **Growth Rate** – which can fluctuate due to; inadequate OM concentration (blockage/empty bubbler), temperature of deposition area/ OM memory effect (if the G.R. is very fast, this could hint at a change in the temperature, or OM residue in the reaction chamber due to previous growths (poor chamber cleaning)).
- **Film quality**– kinks or uneven sinusoidal waves in the interferometer signal indicate non-uniform growth, and could indicate nucleation problems (possibly due to precursor or temperature problem, or substrate cleaning issues).
- **Temperature** –is inferred from thermocouple readings placed inside the susceptor. When the glass substrate is heated, an interferometry trace is visible (as it measures the expansion and relaxation of the glass due to increased temperature). However, after the growth temperature is achieved, a steady baseline is achieved, as the glass has ceased to expand further.

3.6 Window flow

In order for the laser monitoring to effectively pick up the laser signal back from the substrate surface, laser reflections from intervening surfaces must be minimised. This is achieved by designing the liner tube with a small hole in the roof of the rectangular tube (at the same position as the monitoring window on the outer tube) to cut down on potential reflections and improving the intensity of the received laser signal, improving signal accuracy.

As a small intentional gap now exists in the liner tube, it is important that no precursor gases can escape the liner tube, and potentially deposit on the outer tube, or worse, on the optical monitoring window. Therefore, a relatively large flow (of 5 ltrs/min) (larger than the flow entering the liner tube e.g. 4.4 ltr/min) is used to stop any deposition on the monitoring window and is termed "window flow" (see Fig 3.4).

The window flow and total precursor flows were designed in such a way that the two flows were balanced at any precursor concentration. This helped maintain a laminar flow of the precursors whilst passing over the substrate. The precursor gases enter the reaction chamber in the liner tube through a diffuser, which helps to smooth out the flow on entering the reaction tube.

3.7 Re-Installation of the MOCVD reactor

During the PhD, the reactor had to be re-located and re-installed. This provided an opportunity to re-establish the baseline device, and identify the most important growth parameters which need to be controlled.

Thompson *et al. [3]* have identified important reproducibility factors in any semiconductor manufacturing system. Factors which affect reproducibility are identified as; bubbler level/ temperature, and growth rate fluctuations due to reactor wall coating. The authors also discuss how crucial *in-situ* monitoring is towards monitoring the parameters.

Much work was also completed on the installation, and modification on the main MOCVD reactor for controlling a novel in-line MOCVD reactor, which would be used as a pilot scale demonstration reactor, using knowledge gained from this thesis.

3.7.1 Reactor cooling upgrade

The water cooling setup of the reactor (Fig 3.7) is a closed-loop chiller setup. Improving the level of cooling, will have made it harder for the graphite heater to reach the previous temperature, and might require the deposition temperature to be set slightly higher than previously. Also, the area of uniform achievable growth could have also been disrupted or changed (Fig 3.7 b).

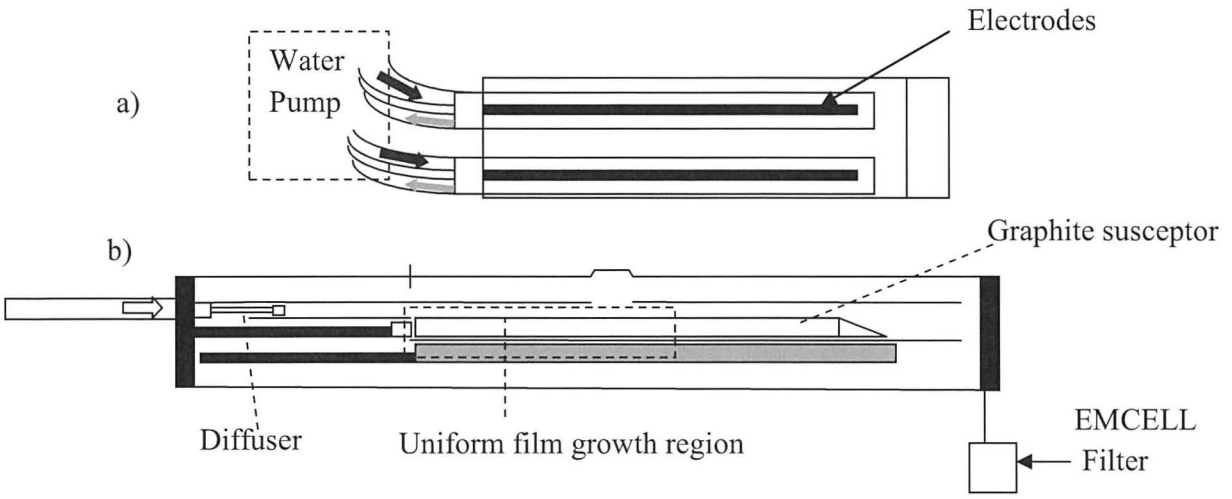

Figure 3.7: a) Schematic of the water cooling setup of the graphite heater. b) Schematic of the reactor, depicting the flow diffuser, the graphite susceptor, the monitoring window and the uniform growth region.

Upon dismantling the reactor, deposits were seen in the inlet of the outer tube (which feeds in the precursors from the gas-handling unit (mixing chamber to the reaction chamber). This suggested that some possible pre-reactions had occurred (or possibly as a result of negative flows, from a blockage further on in the system). In order to alleviate this, a larger (diameter) pipe was used, in the attempt at limiting potential future problems, of deposit accumulation.

Since a larger diameter pipe was used, the pressure balance of the inlet/exhaust needed to be finely adjusted to match the previous pressure balance setting of (+10 mbar) to give a slight positive pressure in the reactor.

This ensured adequate gas flow in the liner tube and to avoid back flows. The adjustment was made possible by inclusion of a needle valve (at the reactor inlet and on the vent needle valve), which could be adjusted accurately to the required setting.

3.7.2 Correcting for substrate temperature

Due to the location of the thermocouple (inside the susceptor), a small temperature discrepancy between the block susceptor temperature (graphite) and that of the substrates (ITO coated glass) placed on top exists. This discrepancy can be measured by monitoring pieces of pure metal wires Indium (Melting point (m.p.) 156.6 °C), lead (m.p. 327 °C) and Zn (m.p. 419 °C). Upon ramping up the temperature, the metal wire can be observed to melt and the measured temperature recorded (Table 3.1).

Table 3.1: Temperature calibration results.

Wire material	Metal m.pt. (^{o}C)	Thermocouple reading (^{o}C)
Indium	156	158.5
Lead	327	319.5
Zinc	419	428.5

The results show that a small thermocouple temperature deviation is observed for the lower temperature (156 ^{o}C), where a 2.5 ^{o}C, over estimation in the surface temperature is seen. As the temperature is increased, a larger discrepancy of - 7.5 ^{o}C and 9.5 ^{o}C under and over estimation, respectively, are observed. Initial experiments were made to correct for the growth rate of the CdS layer as an indicator of the surface temperature (Table 3.2).

The next step was to grow layers of CdS and CdTe, and repeat the previous baseline conditions, prior to relocating and reinstalling the reactor. A G.R of 0.14nm/s for the CdS (at 315 ^{o}C) and 0.44 nm/s for the CdTe (at 390 ^{o}C) were the standard. These will be used in order to replicate the growth rate (and check for deposition temperature inconsistencies).

The first growth of CdS at 315 ^{o}C gave a 0.09 nm/s G.R., increasing the temperature by 5 ^{o}C achieved the target G.R of 0.14 nm/s.

The 5 ^{o}C increase in temperature was also investigated for the CdTe (usually grown at 390 ^{o}C); this increased the G.R to 0.5-0.6 nm/s, higher than the target G.R., possibly as a result of the increased surface ad-atom mobility. Using the standard CdTe temperature (390 ^{o}C), the target G.R was achieved. This suggests that at higher temperature the improved water cooling was not causing any excess cooling compared to the previous setup.

Table 3.2: Temperature vs. Growth rates for CdS and CdTe.

Deposition temperature (thermocouple reading) (°C)	CdS growth rate (nm/s)	CdTe growth rate (nm/s)
315	0.09	
320	0.14	
395		0.55
390		0.44

3.8 Device Fabrication

The growth of a full CdS/CdTe device, within a single chamber, involves:

1. The growth of a 0.24 μm thick CdS window layer at 315 °C, on ITO coated glass substrates (Delta Technologies Rs 5-15 Ω cm^2, 0.7 mm thick) a total gas flow of 3500 sccm is used to facilitate uniform film coverage. The thickness is typically larger than those grown by other deposition techniques (typically less than 0.1 μm [4]). Earlier work within the research group, by Dr. V. Barrioz (unpublished), showed a CdS uniformity problem, when growing CdS thicknesses of ~0.1 μm or less, this has led to the use of a 0.24 μm thick standard CdS thickness in the baseline process. The increased thickness serves to avoid potential pinhole problems, but also presents a problem as the CdS absorbs highly in the energy rich region of the solar spectrum. The Cd:S precursor ratio during growth was Cd (2.7×10^{-4} atm): S (2.7×10^{-4} atm).

2. The CdTe absorber layer is then grown (at 390 °C) on top of the deposited CdS layer. Doping was achieved using in situ arsenic doping (TDMAAs), some which go to passivate the grains, and some as active dopants, a precursor partial pressure of 3×10^{-7} atm, gave a consistent As concentration of 2×10^{18} atoms cm^{-3}.

   The standard CdTe thickness grown was 2 μm, this thickness was chosen as it was sufficient to avoid the standard concern for pin holes (incomplete coverage) and sufficient to absorb all of the light within CdTe. 1.5 hrs (given a G.R. of 0.44nm/s) to grow. The DMCd:DipTe precursor ratio during growth was approx. DMCd rich 2:1 (2×10^{-4} atm : 1.1×10^{-4} atm).

3. A novel back contact layer (BCL), which is made from CdTe that is doped with an increased TDMAAs concentration ($2x10^{-6}$ atm), equivalent to a concentration in the layer of $2x10^{19}$ atoms cm^{-3} was grown immediately after the bulk absorber layer was grown. The increased arsenic doping allows for an improved Ohmic contact (Fig 3.8) to be achieved without requiring any wet etch. Hädrich *et al.* [4] have considered that a barrier height of less than 200 meV would be acceptable for device operation.

Back contact formation of low resistance back contacts to p-CdTe is needed for the fabrication of high efficiency solar cells. As CdTe has a high electron affinity (χ = 3.9 eV) and no metal exists (Table 3.3) with a sufficiently high work function (φ_m). Consequently a Schottky barrier exists, and its height calculated by (Equation 3.4).

$$\varphi_b = (\chi + E_g) - \varphi_m \qquad 3.4$$

where χ is the electron affinity and E_g is the band gap of the semiconductor [4].

Table 3.3: Metals and their associated work functions.

Metal	Work function (eV)
Ag	4.52 - 4.74
Al	4.06 - 4.26
Au	5.10 - 5.47
Cu	4.53 - 5.10
Mo	4.36 - 4.95

For a p-type CdTe layer, a metal with a work function higher than 5.7 eV is needed [5], Chemical etches and p-type doping, can be carried out to alter the band edges, as a result of a change in the interface state density. A lowering in the interface barrier height and width results and enables a quasi-Ohmic or tunnelling contact between the metal and CdTe to form (Fig 3.8) [5].

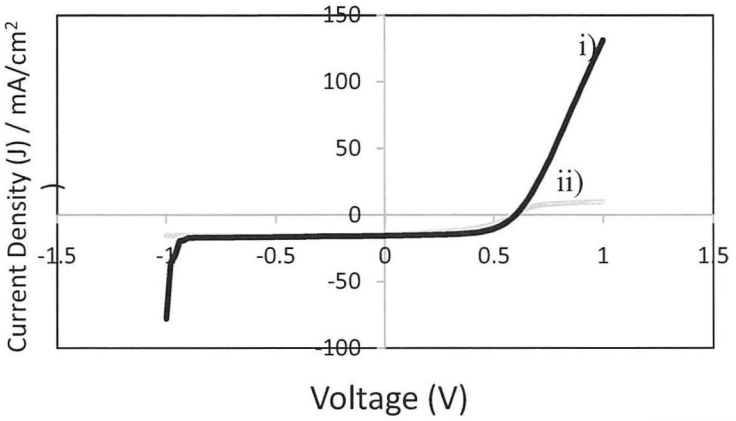

Figure 3.8: Light J-V curves of CdS/CdTe i)with a BCL (R_s of 2 Ω cm^{-2}) and ii) with no BCL (R_s of 10 Ω cm^{-2}).The i) I-V curve is indicative of a low back contact barrier whereas the ii) I-V curve shape indicative of a high back contact barrier, depicting the "roll-over" behaviour.

4. A 1 μm thick $CdCl_2$ layer is grown (at 200 °C) and is sometimes termed the "$CdCl_2$ activation treatment". The DMCd:TBuCl precursor ratio is kept at 2.5, and serves to passivate the grain boundaries, stopping those becoming regions of carrier recombination (possibly allowing electrons to propagate). The Cd:Cl precursor partial pressures during growth were Cd ($2.8x10^{-4}$ atm) and Cl ($9.65x10^{-4}$ atm).

5. The whole device is then annealed at 420 °C for 10 minutes under hydrogen. This step is termed "the passivation treatment", and promotes the diffusion of Cl along the grain boundaries.

6. A weak Br/MeOH etch (0.25%) is applied to the CdTe surface prior to contacting, improving the R_s at the back contact.

7. 3 x 0.25 cm^2 gold contacts are deposited on each CdTe device. This is done using a metal evaporator, which heats a tungsten coil (where 6cm of gold wire is placed) and evaporates the gold. Pre-cut aluminium masks ensure the contact size; with contact shadowing (at the edges of the contact) is minimal through having a minimum mask thickness.

8. Post contacted devices are washed with deionised water, and the CdTe is carefully scrapped off to reveal the ITO, where some GaIn euctetic paste is applied to improve electrical contact with the IV setup, and the average of the 3 contacts is recorded.

My research, growing complete devices (all of the above steps), including flow and concentration calibration prior to each growth run, allows only one growth run (device) to be grown in a single day, and all processes takes typically ~5 hours from start (TCO) to finish (CdS/CdTe solar cell).

2.9 Device processing

Processing into devices, involves evaporating gold metal back contacts on the CdTe surface. The Au contacts are evaporated inside a tungsten filament evaporator at 4×10^{-5} mbar. The layer is placed in the evaporator with desired mask on top. A length (6 cm) of gold wire is folded into three, and lodged inside the filament coil directly above the sample. The current is increased and the gold wire evaporates leaving the desired masking on the sample. A back contact area of 0.248 cm^2 is used to obtain device parameters from I-V curves.

Preliminary work on using laser beam induced current (LBIC) to corroborate the contact/working device area is shown. The LBIC system used had originally been designed by Rachel Rowlands as part of her PhD and later improved by Will Brooks and Dr Barrioz. A CdZnS/CdTe device was scanned (6 mm^2 scan size and 0.1 mm steps) using a 635 nm laser with a multimode fibre couple (Fig 3.9). The z-axis has been corrected to show a current response in uA.

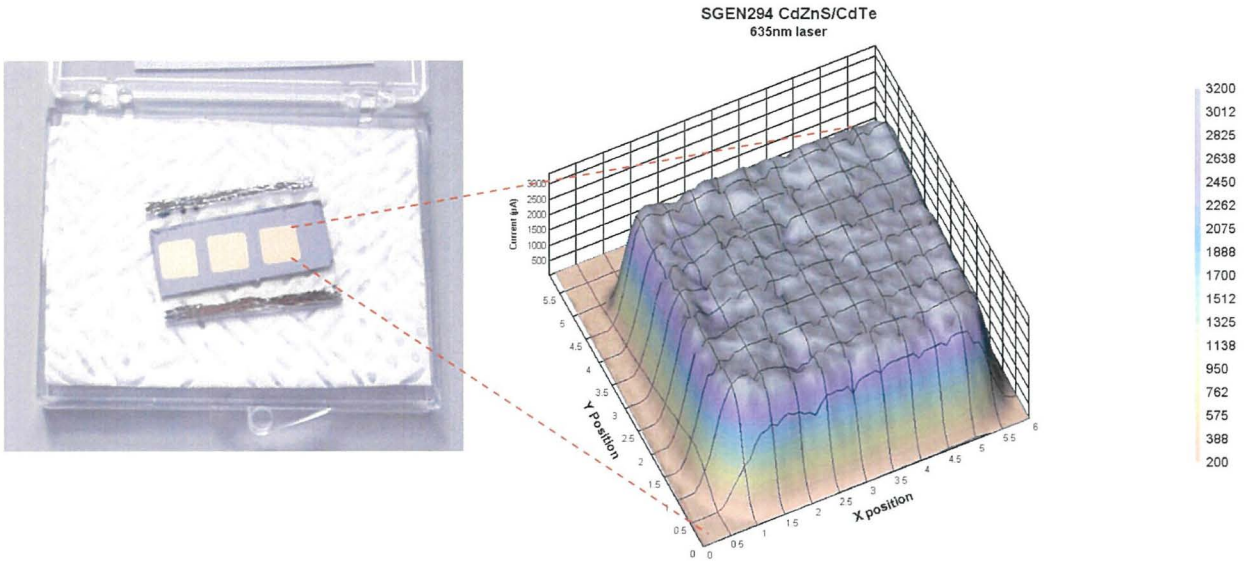

Figure 3.9: LBIC map of a gold contact of a CdZnS/CdTe (SGEN294 -) device.

The image (Fig 3.9) clearly shows, that there is a fairly abrupt junction between the off and on contact regions, and supports the notion that the device area (gold/contact area) is accurate when used in IV calculations to give device performance parameters. Gallium-Indium (GaIn) paste is also used to improve the electrical contact between the TCO in I-V measurements.
Fig 3.9 shows the 3 contacts used for IV measurement, device results in this thesis are averages of 3 contacts per device.

3.10 Characterization of Solar Cells

In order to understand why certain devices are better than others, a device must be interrogated in its constituent parts (i.e. individual layers), to determine if a physically observed phenomenon, influences the end electrical behaviour of the device, and to interrelate these findings. Firstly individual layers will be characterized by a range of physical measurements, in order to determine preferred physical characteristic of the layers for improved electrical performance in the device. Secondly, the CdS/CdTe *pn* junction will be investigated. To try and negate any contacting performance issues, gold has been used as a back contacting material in all solar cell devices (unless specifically stated).

3.10.1 Materials characterization

3.10.1.1 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) was used in the contact mode to study the surface morphology of the CdS and CdTe layers. AFM has been used to gain information regarding the surface quality and roughness of the layers. Fig.3.10 a) shows the ITO surface, and 3.10 b), shows the surface after CdS deposition. AFM was used to scan the surface of ITO, CdS and CdTe layers, and allowed calculation of grain size, and morphology, which can give information regarding growth quality, pinholes and roughness.

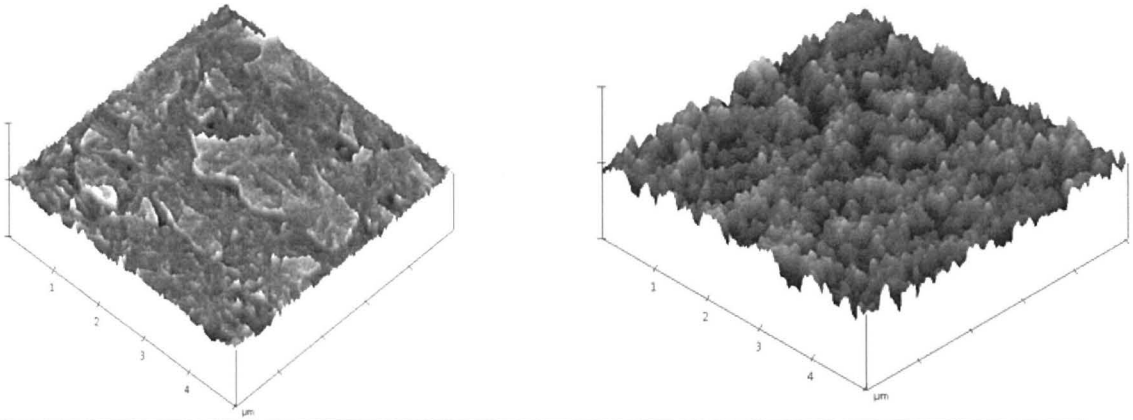

Figure 3.10: a) (Left)AFM of ITO, Root mean square (RMS) roughness of 2.17 nm and **b)** (Right) CdS window layer with RMS roughness of 36 nm deposited on ITO.

All films deposited appeared densely packed, with surface cleaning, prior to deposition, being an important factor in obtaining pin-hole free layers.

3.10.1.2 Secondary ion mass spectrometry (SIMS)

SIMS analysis was carried out at the Surrey Ion Beam Centre by Dr Chris Jeynes. SIMS is a crucial technique for determining the extent of inter-diffusion within the thin films, measuring dopant concentration, or diffusion of contact metals. SIMS depth profiles were carried out on complete device structures deposited by MOCVD. The species investigated were; the matrix elements Cd, Te and S and the intentional dopants arsenic and chlorine. The detection limits of As and Cl were in the region of low $\times 10^{16}$ atoms cm^{-3} and low to mid $\times 10^{16}$ atoms cm^{-3} respectively.

SIMS is a destructive analytical depth profile technique (Fig 3.11 a), which provides information on the thickness of the different layers (Fig 3.11 b), the amount of doping, inter-diffusion and the effect of etching. A high-energy, primary ion beam (incident beam) usually Cs+ or O^- bombards the surface, as the incident beam strikes the surface, both neutral and charged species are ejected (sputtered).

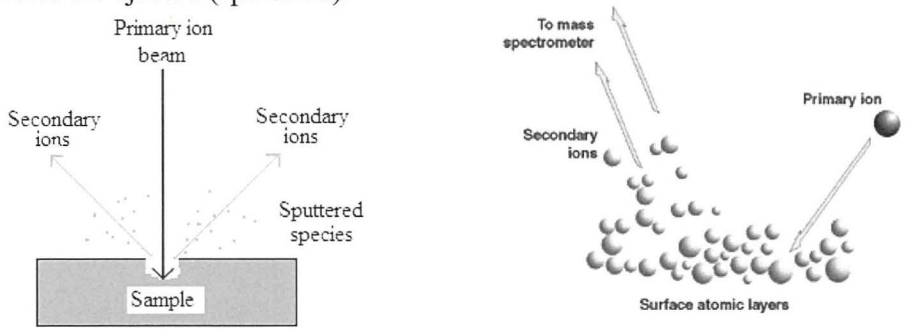

Figure 3.11: a) (Left) Diagram showing the primary ion beam milling the surface and the secondary ions ejected from the surface which are mass analysed, and **b)** (Right) Schematic showing the primary ion beam milling the surface and the secondary ions ejected from the surface which are mass analysed.

Conditions were selected to simultaneously monitor the depth profiles for; Cd, Te, and S (matrix), As, Cl, O, H, Sn, In (trace elements). The ion counts were calibrated into concentrations (atoms cm^{-3}) using supplied reference material of implants of each element into CdTe layers on glass substrates. By integrating over the concentration/ depth profile for the implants, the analysed element concentration can be measured in the layers.

The depth scales were determined by measuring the sputtered crater depths of the reference material using interference microscopy, and assuming a constant rate of erosion. The samples supplied were $1\times1cm^2$ sections cleaved from the device structure.

Other relevant issues include background correction of the measured spectra, and the modification of the film composition during the analysis, e.g. by particle beam induced ion-mixing.

3.10.1.3 Scanning Electron Microscope (SEM)

Scanning electron microscopy (SEM) was carried out on a Hitachi S-520 instrument. Samples were mounted on double-sided carbon tape on a sample stub. SEM was operated in reflection mode, where secondary electrons reflect from the surface, forming an image, top down (Fig 3.12 a) or cross-sectional (Fig 3.12 b).

Cross sectional SEM images can give information regarding the final thicknesses of individual layers, which is very useful, as some layers are expected to be consumed during annealing and other finishing steps. A voltage of 14 kV and emission current of 60 mA were used. Images were taken at varying magnifications (5-30 K), allowing the study of the general morphology and grain size, using the mean lineal intercept (Heyn) method.

The electron beam travels through a series of apertures and lenses, which focus the beam to a fine point. A set of scanning coils near the bottom of the apparatus, move the beam across the sample row by row (raster scanning).

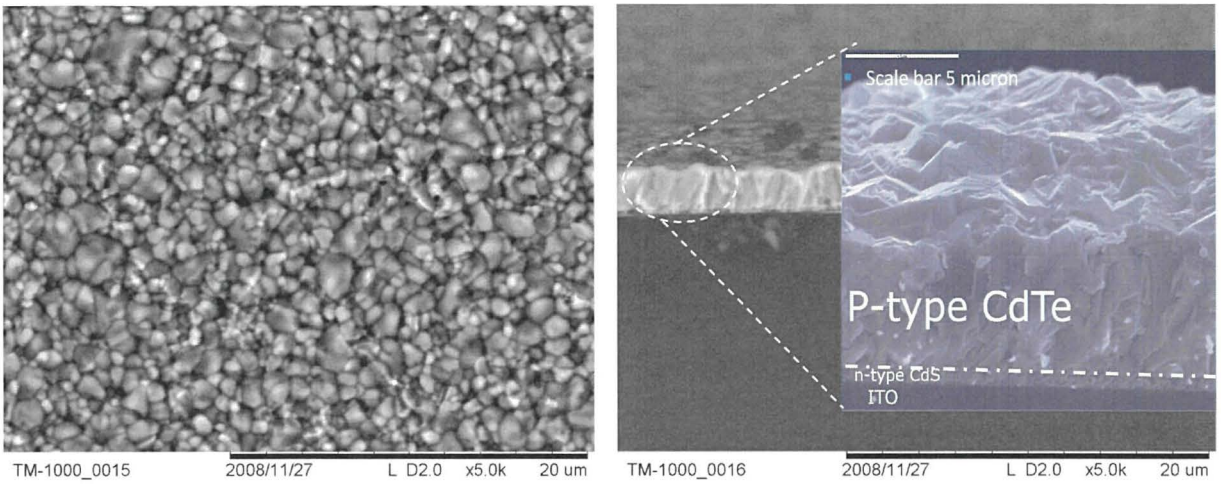

Figure 3.12: a) (Left) Surface view, of a baseline CdS/CdTe device showing variety of grain sizes and **b)** (Right) a cross-sectional SEM scan, where the sample is viewed side-on, allowing estimations of film thickness, and grain size.

3.10.1.4 Energy Dispersive Analysis of X-rays (EDX)

The secondary x-rays emitted from the sample can be used diagnostically to provide information on the composition of the sample. Detailed information on the identity of trace amounts of elements present can be determined, allowing the formation of maps of elemental distribution for the scanned area.

For this study, EDX (Fig 3.13) has been used to first corroborate the presence of Zn in layers of CdS where DEZn $(C_2H_5)_2Zn$ has been used in the attempt at alloying the Zn with the CdS to give a CdZnS solid solution.

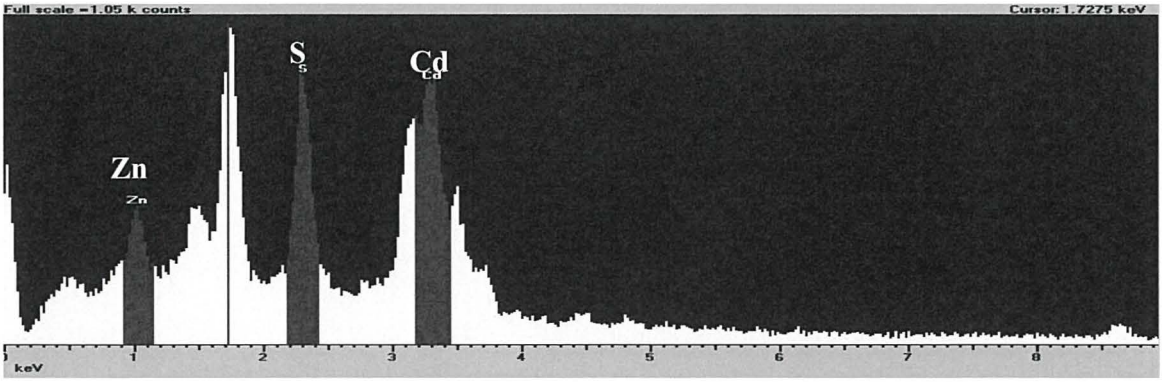

Figure 3.13: $Cd_{1-x}Zn_xS$ (x=0.1) at a raised deposition temperature of 360 °C.

3.10.1.5 Rutherford back scattering (RBS)

RBS is used to determine the structure and composition of materials by measuring the backscattering of a beam of high energy ions impinging on a sample. RBS is an accurate, powerful thin film depth profiling technique, typically carried out at 1.5 MeV using He beams.

RBS analysis was completed at University of Surrey Ion Beam Centre using a 2 MV Tandetron accelerator from High Voltage Engineering Europe. The machine is capable of generating proton beams up to 4 MeV and alpha particle beams of up to 6 MeV and is described in [6]. As RBS provides quantitative composition data directly, it can be used to quantify EDX results, compared to SIMS, which due to particle induced ion mixing can cause erroneous data collection as film modification during analysis is possible.

A 1.557 MeV $^4He^+$ beam was used with a current of 30 nA, with a beam size 1mm, the particular methodology used has been described by Boudreault *et al.* [7]. The substrates were also analyzed, to obtain a direct measure of the glass composition. This was used to guide and inform the analysis.

RBS yielded depth profiles (Fig 3.14 a) from raw data (Fig 3.14 b), and showed in what form the atoms were joined together. Looking at a result for a $Cd_{1-x}Zn_xS$ device where x was 0.1. Good film uniformity was observed. However the result, suggested that the film is made up of separate CdS (Red line) and ZnS (blue line) regions. The result of Oxygen (Green line) throughout the first layer (which would be expected to be the $Cd_{1-x}Zn_xS$ rather than the ITO is unexpected.

If this indicative of the layers, instead of a random result, it would suggest that the Oxygen intermixing (possibly from the TCO) with the top layer (CdS or $Cd_{1-x}Zn_xS$) more than previously thought, possibly during the annealing steps i) anneal after CdS/ $Cd_{1-x}Zn_xS$ growth ii) anneal after CdTe growth iii) anneal after $CdCl_2$ layer growth.

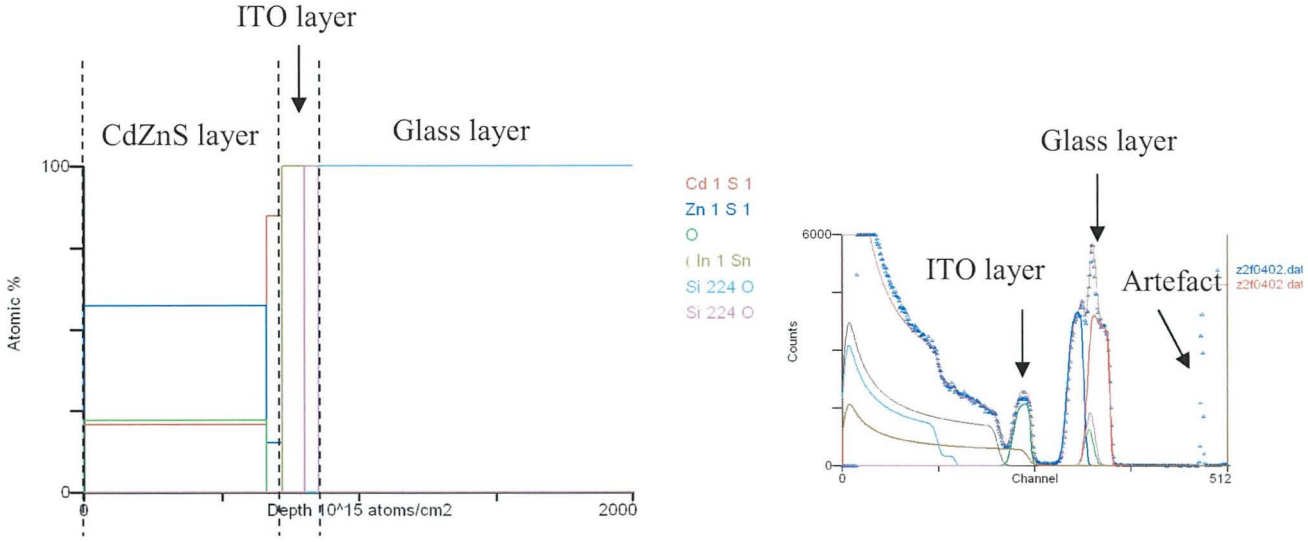

Figure 3.14: a) (left) RBS Depth profile of CdZnS layer and **b)** (Right) the raw RBS data.

3.10.1.6 X-ray diffraction (XRD)

XRD provides precise determination of the atom positions in crystalline materials and solids. X-rays interact with the planes of atoms in the 3D lattice, the separation of which is known as the d-spacing (d_{hkl}).

Crystalline solids produce X-ray diffraction patterns based on the positions and intensities of each observed reflection. In mixtures of compounds each phase forms an individual set of reflections. The relative intensities of the different phase reflections give an indication of the amount of each phase present. Several factors can affect the intensity and number of reflections. These include; lattice type, crystal class, unit cell parameters and the distribution and atom type in the unit cell.

A Phillips W3830 X-ray generator was used (in the Bragg-Brentano orientation) with a copper target the X-rays generated being filtered by a sheet of nickel to produce a monochromatic beam of Cu k_α radiation of wavelength 1.54 A.

In an X-ray diffraction measurement, a crystal is mounted on a goniometer and gradually rotated while being bombarded with X-rays, producing a diffraction pattern of regularly spaced spots known as reflections. The specific wavelength of the X-ray is determined by the metal target and the type of filter used.

Thin films can be thought of in three crystallographic terms; amorphous, polycrystalline and single crystal. Amorphous describes a material without any regular ordered structure (no preferred orientation i.e. no large peak spectrum), polycrystalline a material with many interlocking but different crystals (many different reflections with one preferred orientation) and single crystal being one with a completely regular structure throughout (one single reflection).

It is important to gain knowledge of a thin films crystallographic structure as this dictates many of the films physical properties such as; electrical and thermal conductivity, refractive index and absorption coefficient. Using the Bragg equation (Eqn.3.5) and 3.6, for hexagonal lattices, physical quantities of the layers can be found, e.g. lattice parameter, miller indices and grain size through the use of the Scherrer equation.

$$n\lambda = 2\,d\sin\theta \qquad 3.5$$

For hexagonal structures;

$$\text{Sin } 2\,\theta = \frac{\lambda^2}{4a^2}\left(\frac{4}{3}(h^2 + hk^2 + k^2) + \frac{l^2}{\left(\frac{c}{a}\right)^2}\right) \qquad 3.6$$

Where *d* is the separation between the planes, *h, k* and *I* are integers known as Miller indices and used to describe any particular plane of the unit cell. And c/a is the axial ratio in a hexagonal lattice.

The CdS X-ray diffraction patterns in this study are mainly characterised by a hexagonal wurtzite phase, with strong preferred (002) peak. Polycrystalline CdTe displays sharp (111), (220) and (311) peaks and has been indexed according to the CdTe cubic zinc-blend structure.

In order to quantify the effects of the CdTe thickness (and therefore the growth conditions) on the texture and preferred orientation of the samples, the texture coefficients C_{hkl} [8] were studied (Equation 3.7);

$$C_{hkl} = \frac{\frac{I_{hkl}}{I_{r,hkl}}}{\frac{1}{n}\sum_{n}\frac{I_{hkl}}{I_{r,hkl}}} \qquad 3.7$$

where n is the number of reflections, I_{hkl} the intensity of the hkl reflection and $I_{r,hkl}$ the intensity of the hkl reflection for a completely random sample. Hence C_{hkl} gives a measure of the enhancement of the hkl reflection in comparison to a completely randomly oriented sample.

3.10.1.7 Ultraviolet-Visible Spectrometry

Spectrometry in the UV and visible region of the electromagnetic spectrum, allowed measurement of the relative band gaps of the layers.

It is usual to see interference oscillations in the transmission spectrum of thin films; these can be used to approximate films thickness. An approximation of the optical band gap energy for a semiconductor of direct optical transitions is obtained (Eqn. 3.8).

$$\alpha \propto (h_v - \mathrm{E_g})^{\frac{1}{2}} \qquad 3.8$$

Where a = absorption coefficient as a function of frequency for a direct (allowed) transition. Thus plotting $(aE)^2$ versus energy (hv), and extrapolating the linear portion of the curve to the intercept with the energy axes, gives the band gap energy (Fig 3.15). Purica *et al.* [9] demonstrates this method, specifically with Transparent conducting oxides (TCO's).

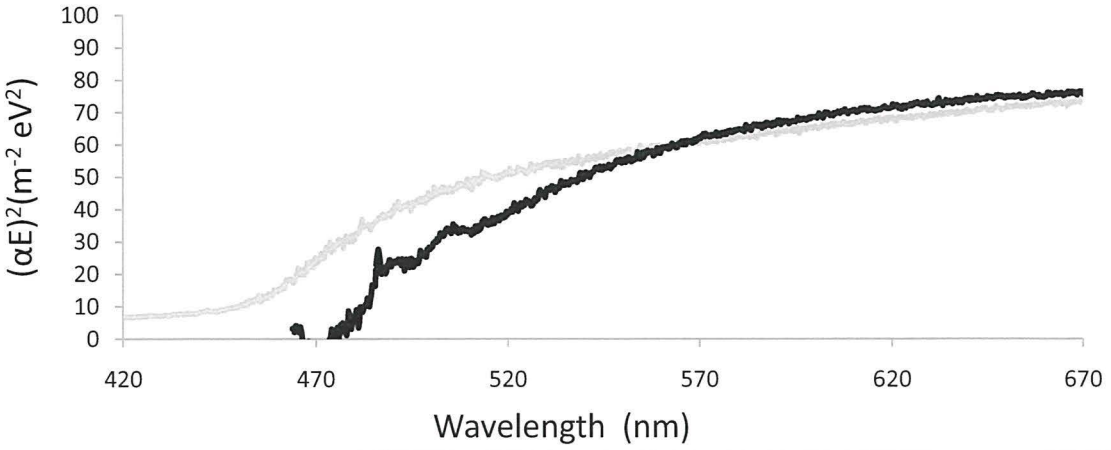

Figure 3.15: UV-Vis spectrometry of $Cd_{1-x}Zn_xS$ layers used in full *pn* junction devices, showing i) films grown at the inlet (grey line) $Cd_{1-x}Zn_xS$ (x=0.1) E_g= 2.9 eV and ii) films grown at the outlet (black line) $Cd_{1-x}Zn_xS$ (x=0.1) E_g= 2.7 eV.

Figure 3.15 shows the response of the inlet (thicker) and outlet (thinner) films. It is shown that films grown at the inlet have a slightly larger (lower) band gap. This could be due to the increased transmission of the photons in the sub 500 nm range, as the layer is thinner than the outlet layer. It could also suggest that an increased concentration of Zn is present in the inlet, and suggest a DEZn concentration gradient exists in the horizontal reactor (precursor depletion effect), with band gap changing from approximately 2.9 eV at the inlet to 2.7 eV at the outlet.

3.10.2 Electrical characterisation

3.10.2.1 Current-Voltage (I-V)

The first few devices were measured using a custom IV rig, which made use of 4 x Halogen spotlights. The light intensity (spectrum shown in Fig 3.16) was calibrated using a Melles-griot broadband power meter, and calibrated against a Fraunhofer CdTe reference cell, and checked also with a CdTe reference cell, supplied by T.Gessert of NREL, by matching the J_{sc} response of the cell.

When it came to accurately measure the improvements due to the blue region of the spectrum, due to the wider band gap of CdZnS, the spectrum of the Halogen spotlights, proved inadequate in simulating AM1.5 in the UV-sub 500 nm range (Fig 3.16). The spectrum of the halogen severely underestimated the now improved response in this region.

Towards addressing this problem, a Xenon lamp setup was purchased. The spectrum (Fig 3.16) showed an improved spectral match to the AM1.5 spectrum at sub 500 nm range.

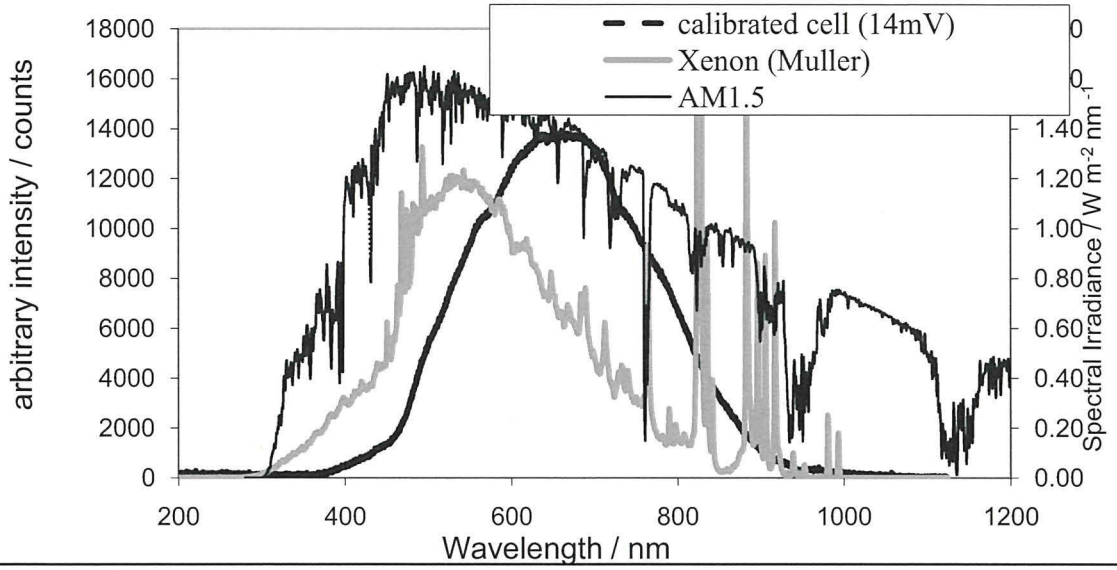

Figure 3.16: Qualitative comparison between the halogen spectrum (14mV on the calibrated cell)(left axis), the Muller-Xenon spectrum (left axis) and the Standard AM1.5 Global irradiance (right axis).

Both the halogen and xenon lamps have been initially calibrated using a Fraunhofer Reference cell, which was specifically produced with an internal filter to mimic CdTe cell response. The reading on the reference cell needed a value of 13.0 mV to have the correct light intensity, which is equivalent to the response at AM1.5 (100 mW/cm^2) illumination.

To obtain a more accurate calibration measurement, a CdTe reference device was obtained thanks to T. Gessert of NREL, which was used to match the J_{sc}. Towards the end of the research, the light source of the I-V characterisation setup was upgraded again to an ABET scientific AM1.5 solar simulator. The same calibration procedure, using the Fraunhofer and NREL cells was followed as above but had the advantage that the spectrum more closely matches the AM1.5 spectrum.

Because of the use multiple spectra in this research, in order to be able to compare the devices, device have been either i) re-measured using the IV setup in question, or ii) re-grown and then measured using the necessary IV light spectrum in order for a fair and consistent comparison of cells is made.

3.10.2.2 Current-Voltage Curve

Several parameters are used to characterise solar cells. Figure 3.17 shows a typical I-V of MOCVD grown CdS/ CdTe devices, in the dark and under illumination. Current voltage measurements were conducted using a Keithley IV source meter, voltage was swept from -1.00 V to +1.00 V, for dark measurements the cells were covered from exposure to light, and measurement temperature was kept at 25°C through the use of cooling fans.

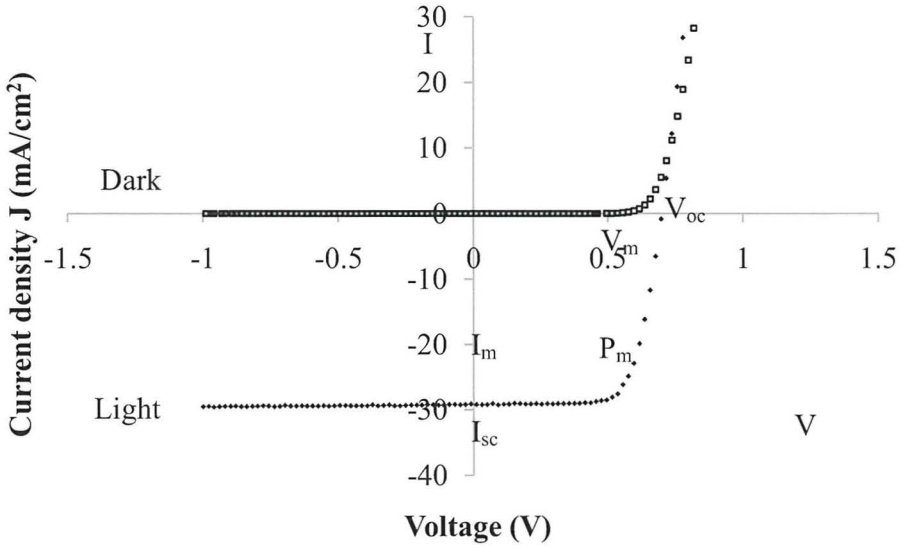

Figure 3.17: I-V curves of devices in light and dark.

3.10.2.3 Spectral Response

A Spectral response system was purchased from Bentham (a custom PVE300 PV Characterisation System). The system allows the determination of device spectral response (from which may be determined EQE).

The device to be measured is electrically connected to the system, in a similar manner to a current-voltage setup. In order to calculate the QE, the electrical performance of the device, has to be measured per wavelength. To do this, a slit is employed, this allows a narrow amount of light to impinge the device (delivered through a 5 x fibre optic cables), and concentrated onto a small spot on the contact. A prism is employed to separate the spectrum into its individual wavelengths, and is incrementally rotated to allow single wavelengths of light to impinge the sample, this is done until the necessary range of wavelengths set is reached, and the corresponding device performance is measured.

As the setup allows the cell to be analysed one wavelength at a time, this can help to determine where device losses originate, as higher energy photons absorb closer to the junction.

A well-known complication in measuring the spectral response of cells with a CdS window layer is that of "photo-doping". This is where blue light exposure increases the CdS carrier density. The resulting modification of the p-n junction alters the carrier collection for all wavelengths and can lead to misinterpretation of results. The use of a white, DC-bias light, during QE measurements is generally used to solve this problem [10], and has been incorporated.

If one plots out the AM1.5 spectrum (Fig 3.18), noting the associated optical band gap position on the wavelength axis (in nm's), one can clearly see, that increasing the band gap (towards lower wavelengths), the amount of potential photons hitting the layer is increased. This allows an increased potential area for generating photocurrent in the CdZnS/CdTe device, compared to the CdS/CdTe based device.

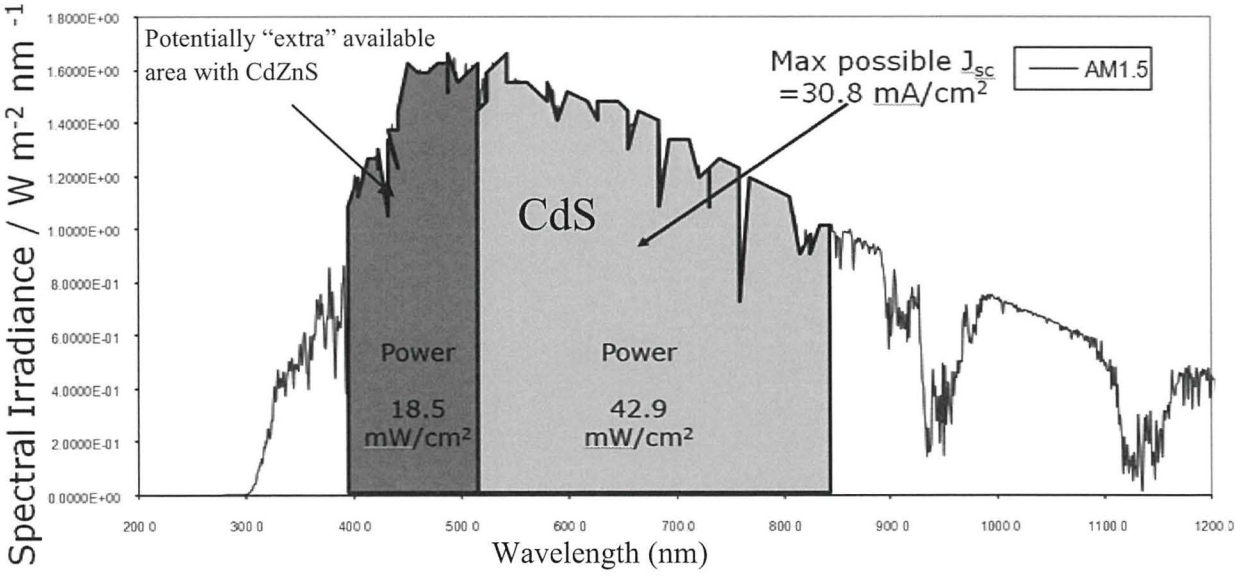

Figure 3.18: AM1.5 spectrum, showing available energies for CdS and CdZnS.

The spectral response of a typical CdS/CdTe cell is seen in Figure 3.19, where a large portion of the AM1.5 spectrum can be seen to be absorbed by the CdS, as very little energy below 500 nm is captured by the CdTe absorber.

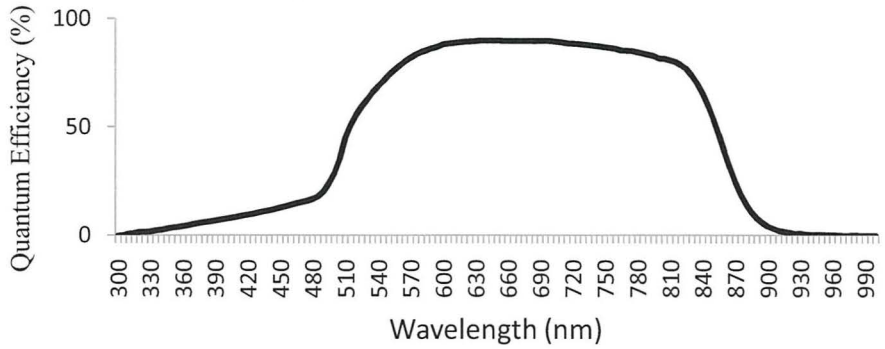

Figure 3.19: A normalized spectral response curve of CdS/CdTe device (CSER 28).

3.10.2.4 Current-Voltage-Temperature (I-V-T)

This is a variant of the standard I-V characterization, knowledge of the I-V behaviour with temperature yields the back contact barrier height, main diode barrier height, and main diode quality factor, and current transport mechanism of a cell can be determined. I-V-T analysis setup (Fig 3.20) was based at Durham University Physics Dept, and modified by Mohammed Al Turkestani.

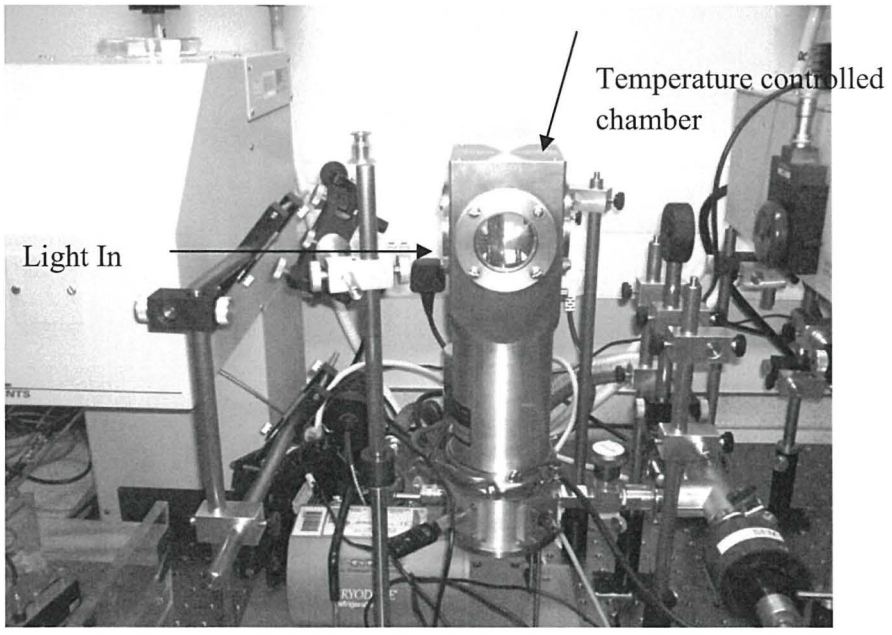

Figure 3.20: I-V-T setup. Designed by M. Alturkestani [11] (based at Durham University).

I-V characteristics were measured for these samples in dark and light. They have been mounted in a cryostat then light was deflected from the solar simulator into the chamber of cryostat containing the sample.

The temperature range was from 300 K to 200 K with a step of 10 K. A Keithley power source was used to apply voltage from -1 to 1 V and then current was measured. By connecting the source to a PC, 201 points have been recorded in this range of voltage. In order to investigate the light I-V curves, different optical filters were placed on the window of the cryostat. Light intensities, as a result, were 0%, 10%, 20%, 50%, 79% and 100%. Studying the I-V curves in different temperatures and also under different light intensities can be a very powerful tool to investigate the performance of solar cells more extensively.

3.10.2.5 Capacitance-voltage (C-V)

The C-V setup used was also located at Durham University, and was setup by Dr Yuri Proskuryakov. C-V measurements are routinely applied to assess the doping density of doped and un-doped semiconductors.

The procedure for taking C-V measurements involves the application of a DC bias voltage across the capacitor, while making the measurements with an AC signal. Commonly, AC frequencies from about 10 kHz to 10 MHz are used for these measurements. A strong DC bias causes majority carriers in the substrate to accumulate near the insulator interface. Since they cannot penetrate the insulating layer, capacitance is at maximum in the accumulation region as the charges stack up near that interface.

Dark capacitance–voltage (C–V) measurements were taken from −1.2 to + 1.2 V, at a frequency of 150 kHz and room temperature. Using this frequency avoids contributions from deep states, which can be ignored at frequencies higher than 120 kHz [12].

A Plot of the inverse square of space charge layer capacitance (C_{sc}^{-2}) versus semiconductor electrode potential (E) gives the doping density, the local slope of that plot is inversely proportional to the doping density at a position 'x' away from the junction [13].

3.11 Device modelling

In order to accurately model the CdS/CdTe junction, physical limits need to be known.
The CdTe and CdS used in these cells are polycrystalline; hence the mobility will most likely be lower than that for a single crystal. Access to the software was made available thanks to Prof. M Burgelman [16]. The software developed by his team, allows 1-D modelling of semiconductor layers and solar cell devices. In single crystal CdTe at 300K, the electron mobility e=1050 cm^2/Vs, and hole mobility h=100 cm^2/Vs, and likewise CdS exhibits, e=250 cm^2/Vs and h=15 cm^2/Vs [17]. These values can be considered to be upper limits on CdTe/CdS solar cell mobility's.

As the device behaviour of the CdS/CdTe is complex, simple extrapolation of final device result is not possible. Several authors [14, 15] have produced their own software model packages, which try and solve the continuity equations, given simple user inputs (thickness, band gap, etc.). The Solar Cell Capacitance Simulator in 1 Dimension (SCAPS-1D) program was obtained from Prof. Burgelman. SCAPS-1D, was developed at the University of Ghent by Marc Burgelman [16]. It is continuously updated and the progress is well documented in the literature.

The inner-workings of the model are complex, and are not described in detail, as it is not relevant for this research, but the SCAPS model attempts to solve the Poisson and continuity equations, and attempts to solve the equations for electrons and holes iteratively. Some advantages and disadvantages of the model are listed in Table 3.6.

Table 3.6: Advantages and disadvantages of the SCAPS modelling software.

Advantages	Disadvantages
• all input files are user-accessible text files, this includes spectral data as well as device definition files • sophisticated treatment of interface recombination and interface trapping • very fast • inclusion of series resistance, capacitance-voltage and capacitance frequency response	• can be unstable when the device is far from ideal and includes secondary barriers (which is likely in real devices) • no batch processing, every calculation (I-V, QE, etc.) of every model has to be performed "by hand"

The SCAPS software can be used to model most electrical device parameters such as, efficiency, FF, J_{sc}, and V_{oc}. Even more complex information such as spectral response curves, and C-V curves can be modelled, which allows a direct comparison with modelled and measured results. Parameters that were chosen are listed in Table 3.7.

The need for a large number of input parameters (50–100) makes convenient modelling difficult. With the need for a consistent set of parameters, with parameters depending on deposition technique and even differing with each sample, suggest, only limited modelling can be achieved. However, comparing modelled results with real experimental data, however basic, can be useful. The authors took the approach [14] of selecting a baseline parameter set, and only one parameter was varied at a time (firstly the absorber thickness).

Table 3.7: Parameters used in baseline SCAPS modelling.

Layer	CdTe	CdS
Thickness (μm)	2	0.24
Bandgap (eV)	1.5	2.4
Electron affinity (eV)	3.9	4
Dielectric constant	9.4	10
CB effective density of states (cm^{-3})	8.00×10^{17}	2.20×10^{18}
VB effective density of states (cm^{-3})	1.80×10^{19}	1.80×10^{19}
Electron thermal velocity (cm s^{-1})	1.00×10^{7}	1.00×10^{7}
Hole thermal velocity (cm s^{-1})	1.00×10^{7}	1.00×10^{7}
Electron mobility (cm^2/Vs)	1.05×10^{3}	1.00×10^{2}
Hole mobility (cm^2/Vs)	4.00×10^{1}	2.50×10^{1}
Shallow donor density (cm^{-3})	0	1.10×10^{18}
Shallow acceptor density (cm^{-3})	5.00×10^{14}	0

3.12 Electrical characterization of baseline CdS/CdTe cells

As highly efficient MOCVD grown CdTe based devices are relatively rare, it is of use to directly compare, electrically, the performance of MOCVD devices with ones deposited by CSS (grown by J.Major, Durham University). A "baseline" device from each deposition technique (each of comparable efficiency ~10%), have been investigated.

The samples investigated have various absorber thicknesses (0.5 μm - 2 μm). Cells are biased from −1.40 V to + 0.6 V as this represents transition to a regime dominated by capacitance at the back-contacts (Table 4.6).

Table 4.6: C-V results for a CdS/CdTe:As doped cell.

Samples	Actual thickness (μm)	Carrier density from C-V (Durham) (cm^{-3})	Carrier density (cm^{-3})	Resistivity (Ω cm)	Measured mobility (cm^2/Vs)	Semiconductor type
CdTe:As$^+$	0.95	$1 \times 10^{+14}$	$1.31 \times 10^{+13}$	$3.29 \times 10^{+4}$	524.2	p
CdS	0.3	-	$3.71 \times 10^{+15}$	$2.21 \times 10^{+2}$	6.8	n

3.13 Determination of Charge carrier Transport mechanism

The carrier transport mechanisms in the n-CdS/p-CdTe hetero-structure, have been studied by several research groups, each have developed their conduction models to explain the temperature dependent current–voltage behaviour [31-34].

Nevertheless, above approximately 280 K, there is general agreement on the dominance of interface recombination in the as-grown and air annealed devices and depletion region recombination in $CdCl_2$ processed devices. Below 280 K, tunnelling is identified to be the dominating transport mechanism.

The Temperature here was varied (200-300 K) and I-V curves have been measured under different light intensities, including in the dark.

Firstly, the dark (I-V-T) parameters will be investigated; In order to study the electrical transport mechanism in this sample, I-V data have been recorded at different temperatures. A general equation of the p-n junction in the dark can be expressed as (Eqn. 4.4);

$$I = I_0 \exp[\frac{q(V - IR_s)}{nkT} - 1] - \frac{V - IR_s}{R_{sh}} \qquad 4.4$$

Where I_0 is the saturation current, V is the applied voltage, n is the Ideality factor, k is Boltzmann constant, T is temperature, R_s is the series resistance and R_{sh} is the shunt resistance.

In the case where the R_{sh} is high enough, and only considering I-V curves where there is no effect of R_s (e.g. roll-over etc., (Eqn. 4.4) can be simplified to (Eqn. 4.5):

$$I = I_0 \exp[\frac{qV}{nkT} - 1] \qquad 4.5$$

I-V-T of CdS/CdTe cells grown by both MOCVD (grown at Bangor University) and CSS (grown at Durham University) have been investigated. Fig 3.21 left), shows a graph of the current density-voltage characteristics (of log I versus V), the slope, A ($\log_e$ I/V), shows good linear behaviour over the temperature range studied (200-300 K) for both samples.

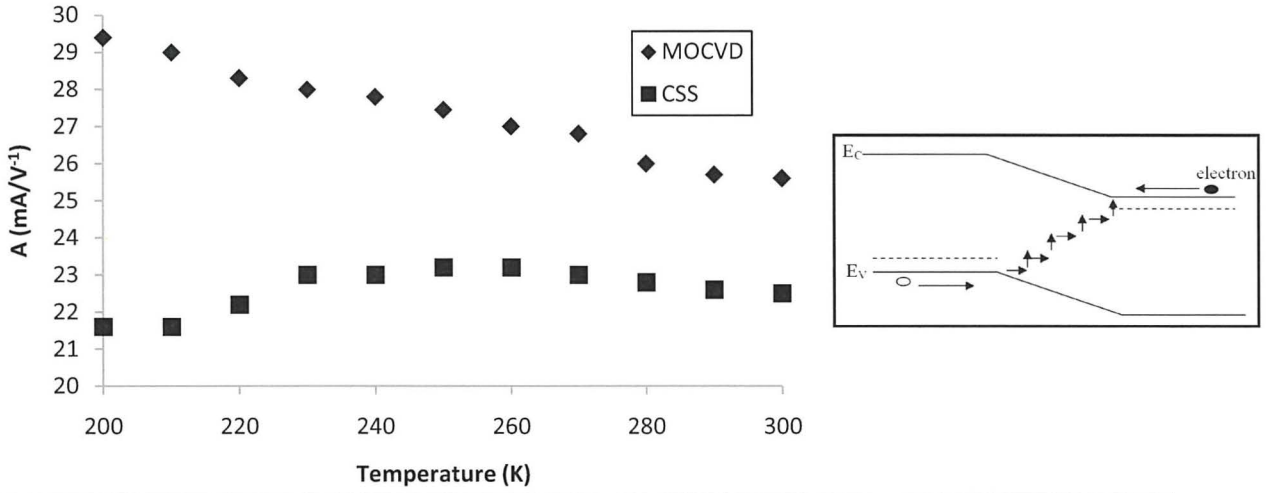

Figure 3.21: (left) Relationship between the applied voltage and the slope of (lnI)/V versus Vs Temperature and (right) A schematic of the multi-step tunnelling-recombination mechanism, Results are thanks to M. Alturkestani of Durham University.

A plot of Ln I versus V, yields information regarding the Io (intercept) and n (slope). Fig 4.13 left) shows that the slope (ln I_o/V) as a function of applied voltage, was not very sensitive, and a small slope was observed for both MOCVD and CSS devices, which stabilize at around 230 K. For both samples, since lnI_o/V is not a strong function of T, and Ercelebi *et al.* [31] have shown that the ideality factor is inversely proportional to T, thus for our case, the transport mechanism can be said to be multi-step tunnelling-recombination.

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CHAPTER 4 - RESULTS

4.1 Thin film growth uniformity

The main aim of this thesis is to investigate the effects of reducing the absorber thickness of CdS/CdTe solar cells. Thus it is crucial that the thickness of the layer is known and can be monitored. The reactor used in this study initially had a rotating graphite susceptor. A rotating susceptor is needed in order to obtain a uniform film, as the rotation allows the whole area of the substrate to receive equal concentration of the precursor [1]. However, the size of the rotating disc was small (2" wafer), only allowing small devices to be grown. The inability to produce devices with credible contact size (in the order of 0.25 cm^2) meant only a few devices per wafer, thus a move to larger substrates was warranted.

Using a non-rotational susceptor of similar size, the growth area could be increased, allowing more devices to be grown per wafer. The substrates used were 2.5 × 7.5 cm^2 in size, and typically only three substrates are used (Geometry shown in Fig 4.1, Inlet -left and outlet-right).

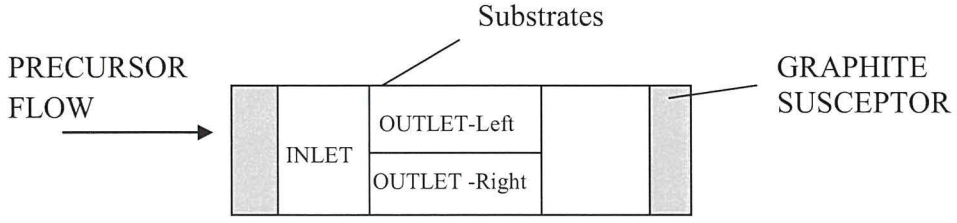


Figure 4.1: Schematic of substrates orientation in a horizontal MOCVD reactor.

The limitations of the horizontal MOCVD reactor have been discussed in the literature review chapter, where a precursor depletion effect is described. Problems common to all MOCVD reactors include, temperature gradients (which can result in convective loops), and high gas flows (which can lead to turbulence rather than laminar flow).

The distance axis can also be considered a time axis (inlet t=0). The gas-phase depletion of the active precursor (Fig 4.2) occurs over the whole length of the reaction chamber as the leading edge (inlet) experiences the fastest growth rate, as it receives the maximum concentration. The organo-metallic concentration is consumed by the growing film, leading to a decreased concentration of the precursor being available for film growth further along the substrate, resulting in a wedge shaped film thickness profile. The flow rate of the reactor can be thought of as a 1st order rate reaction (Equation 4.1);

$$\frac{d[A]}{dt} = k_1[A] \qquad 4.1$$

Where k_1 is the rate constant of a 1st order reaction, and A is the precursor concentration.

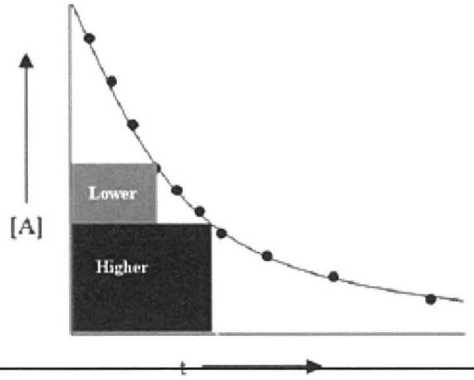


Figure 4.2: Gas flow kinetics and t is time in the reaction chamber.

Figure 4.2 shows that if the total flow rate is increased, a lower growth rate will be achieved, and the rate of depletion of the gas phase concentration with distance (or time) will be less. This will improve the overall thickness uniformity, as the effect of gas phase depletion will result in more growth on the outlet, minimizing the depletion effect. The inverse is true for the lower flow situation, where a higher growth rate will be achieved, and increase gas phase precursor depletion.

In order to investigate the extent of the thickness variation throughout the film growth region, a 4 μm thick (measured at the point of in situ optical sensor) CdTe layer was grown and its thickness measured by cross-sectional SEM and an optical profilometer (Fig 4.3) for comparison.

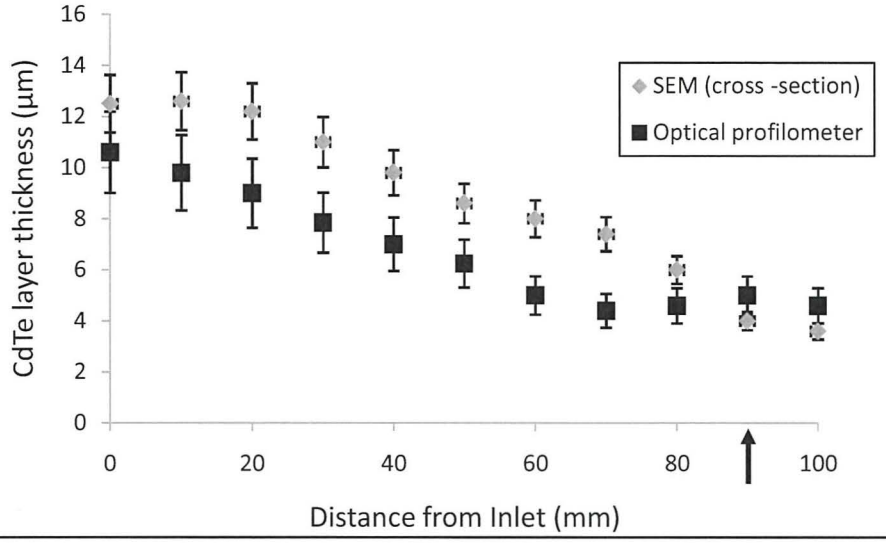


Figure 4.3: Thickness variation of a 4µm thick CdTe layer, measured using SEM and Optical profilometry. Arrow denotes laser monitoring position. Total flow rate was 3500 sccm.

Both the SEM and stylus profilometer (Optical profilemetry measurements thanks to Martin Archbold, Durham University) data show similar results. The large difference in the film thickness from the inlet to the outlet of the susceptor shows that precursor depletion is a problem for obtaining uniform film thickness over the deposition range. A general decrease in the CdTe film thickness is observed, with a possible small increase in the middle which could be due to a small temperature variation. The large difference in data is due to having to estimate the cross-sectional thickness using SEM, which is not ideally suited, as the film is viewed at an angle. The data for the optical profilimeter is closer to the real thickness trend.

One solution to lessen the extent of the observed thickness variation is to increase the total flow rate, thereby increasing the flow velocity, and reducing the transit time of the precursors from the inlet to the outlet of the susceptor. An additional 4 µm thick layer was grown, and measured. Increasing the total flow rate to 4400 sccm (An TDMA doping reference chart is located in the appendix. Table A.1), (Fig 4.4) has improved the film thickness uniformity over the whole growth range, with an overall uniform film, with depletion occurring right at the outlet edge.

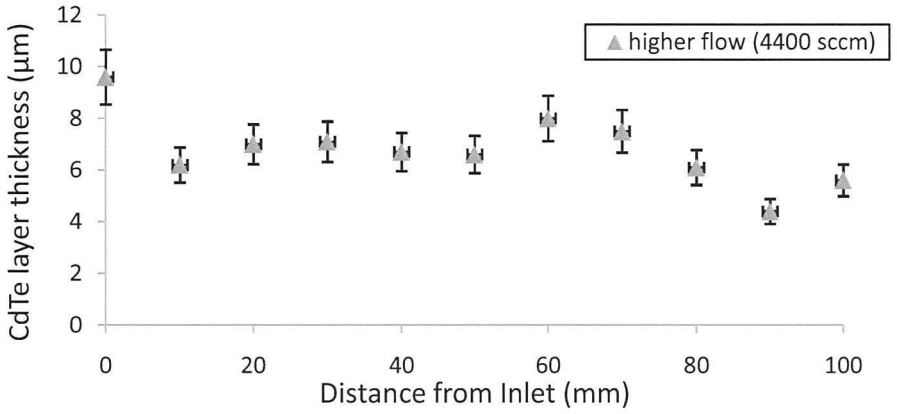


Figure 4.4: Thickness profile, measured by SEM cross section, for a 4 µm CdTe film grown at a higher total flow rate of 4400 sccm.

To counter the effect of varying thickness on device performance, devices are made from the same position (at the laser monitoring point) of the substrate.

4.2 Growth kinetics

4.2.1 CdS window layer

The initial growth of the CdS window layer is seen as very important in the determination of the final CdTe layer structure, as the CdS surface has the potential of being a grain "template"[2] for columnar growth, which may manipulate the CdTe grain size.

Early work on MOCVD of CdS window layers onto indium tin oxide (ITO)-coated glass substrates, indicated that low-temperature deposition was required for good film transmission [3]. Using the precursor's dimethylcadmium (DMCd) and ditertiarybutylsulphide (DTBS), it was found that the best film properties were obtained at 315 °C. The relative II:VI growth ratio has been investigated previously by Barrioz [2], with a ratio of 1 found to be optimal for this particular reactor geometry.

Good transmission over the range of growth temperatures from 300 °C to 350 °C. Although, Cl doping has been used previously, using the precursor tertiarybutylchloride (tBuCl) [4] and n-hexylchloride(nHexCl) [2], it was found that the undoped CdS was sufficiently n-type for junction formation.

The influence of growth temperature on CdS growth rate was investigated (Fig 4.5). k , the rate constant (or coefficient) of the reaction, varies with temperature, T as given by the Arrhenius equation;

$$k = Ae^{-E_a/RT} \qquad 4.2$$

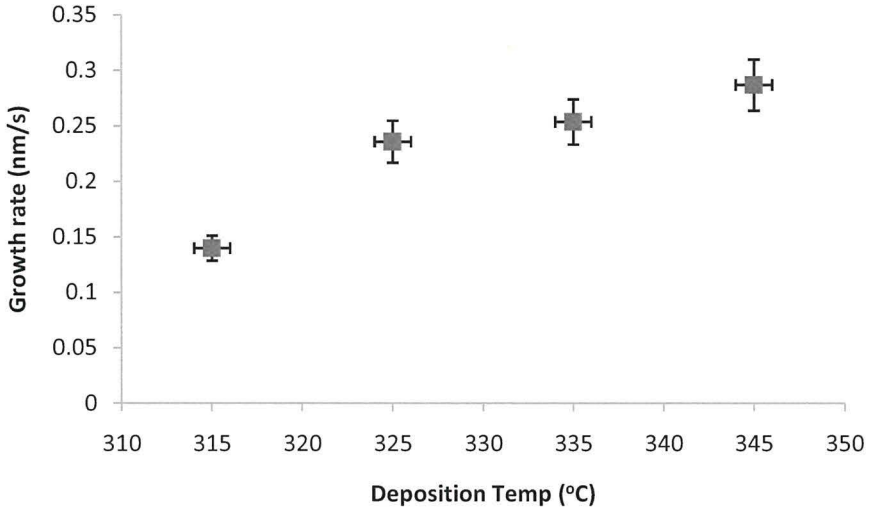


Figure 4.5: G.R. (nm/s) vs. Temperature (°C) for CdS window layer growth.

To understand the data, we need to consider the possible scenarios; in a transport limited regime (rate determined by supply of reactant to the surface), the deposition rate is independent of the surface characteristics (temperature etc.) and strongly dependant on the inlet flow rate. In a surface limited regime, the deposition rate is directly proportional to the surface reaction rate constant, which is often an exponential function of temperature.

If we consider a particular reactor with constant gas flow while increasing temperature, the rate would be slow, the consumption time large compared to the residence time (on the surface) as the adatom mobility would be increased and the precursors would have enough energy to desorb off the surface, and the reactor would be surface limited. As the temperature is increased, we would reach a condition where the residence and consumption times are equal, turning the reactor into a transport limited regime, where deposition rate is again independent on deposition temperature.

However, a near linear dependence with the temperature is observed (Fig 4.6), showing that the reaction rate is effected by the deposition temperature, thus, in the temperature range used, a surface limited kinetic regime can be said to exist.

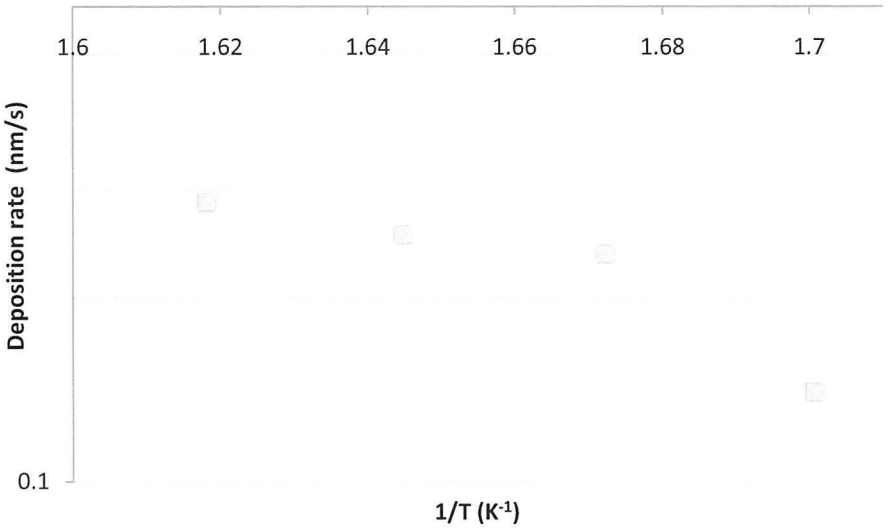


Figure 4.6: deposition rate (nm/s) vs. 1/T.

As the temperature dependence of the growth rate is Arrhenius like, a linear relationship is obtained for temperatures (325 °C, 335 °C, and 345 °C) with G.R characteristics of 315 °C slightly off a linear trajectory, with slope of –Ea/R. The line was fitted to determine the activation energy (E_a) and a value of 22 kJ mol^{-1} was obtained. As mentioned in the experimental section, 0.24 μm thick CdS layers are grown. This thickness has been chosen as a trade-off of, being thick enough to avoid potential pinholes [5], and thin enough to let sufficient light through, maximizing photocurrent [6].

4.2.2 CdTe layer

The CdTe absorber layer was doped with arsenic in situ using tris-dimethylaminoarsine (TDMAAs) using a double dilution line. The cadmium and tellurium precursors were DMCd and diisopropyltellurium(DIPTe), respectively. Early work by Berrigan *et al.* [4] showed that the arsenic concentration was very high, in the region of 6×10^{19} atoms.cm^{-3} in doped CdTe layers.

The subsequent introduction of the double dilution circuit has enabled improved control of the arsenic concentration over a wide range from 1×10^{16} atoms.cm^{-3} to over 1×10^{19} atoms.cm^{-3} [6]. Barrioz *et al.* [7] have previously identified the optimum TDMAAs doping concentration of a 2 μm "baseline" CdS/CdTe device to be 2×10^{18} atoms.cm^{-3} using the double dilution line.

Work by Rowlands *et al.* [6], showed that the reaction mechanism for the decomposition of the TDMAAs follows second order kinetics and is probably occurring due to the formation of an intermediate dimer complex. SIMS analysis showed saturation point above $1x10^{6}$ atoms cm^{-3}, consistent with filling of available sites.

The CdTe layer has been deposited under Cd-rich conditions to promote increased As doping. However, for polycrystalline CdTe layers grown onto glass, the acceptor concentration (around 1×10^{14} atoms.cm^{-3}) is far lower than the As concentration measured using calibrated SIMS [6]. This suggests that not all of the arsenic is electrically active (as acceptor) in the semiconducting material. This could suggest the presence of a compensation type effect which limits the level of extrinsic doping or that the As is going to the grain boundaries. This would suggest that if the As is present, but is not electrically active, it could hinder the mobility of charge carriers, as As, and especially interstitial As, would act as possible mini recombination regions.

The measured level of As in baseline MOCVD CdS/CdTe devices, is significantly lower than that reported by Morales-Acevedo [8] (10^{18} atoms.cm^{-3}). Morales [8] suggests that if the doping value could be increased to 1×10^{18} atoms.cm^{-3} (approx.3×10^{-8} atm partial pressure), setting on our MOCVD reactor) in polycrystalline CdTe, improvements in V_{oc} could be expected.

4.2.3 CdTe deposition temperature

A deposition temperature of 390 °C was identified as being the optimum. Preliminary investigations identified the CdTe layer was very sensitive to deposition temperature ("surface limited" – rate determined by the inlet concentration). An increase in deposition temperature of 20 °C (390 °C to 410 °C), decreased growth rate from 0.44 nm/s to 0.2 nm/s.

The drop in growth rate, can be explained if one thinks of a fast surface reaction (due to the increased reaction rate constant (K_s) of the increased temperature), which would mean that the precursor cannot be supplied quickly enough, and would act as the rate determining step lowering the overall concentration in the reactor.

Fig. 4.7, shows how the top surface of the CdTe is changes, giving larger grain sizes. This observation agrees with similar studies by Mora-sero *et al.* [9], and demonstrates the importance of precise temperature control a repeatable CdTe layer. Mora-sero *et al.* [9] concludes that there is an exponential dependence between the temperature and grain size, indicating a kinetic limited process for the CdTe growth.

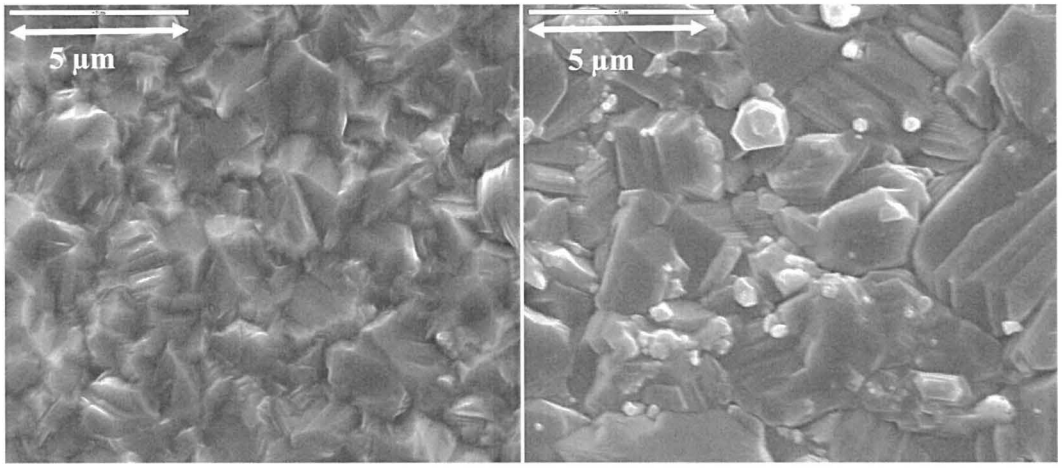


Figure 4.7: SEM images of CdTe absorber grown at varying deposition temperatures 390 °C (Left), 410 °C (Right).

4.3 CdS/CdTe device

In order to investigate and interrelate device limitations a baseline device with known process conditions, which is repeatable, must first be obtained.

The ongoing improvements in the efficiency of the CdS/CdTe cells, has been a large part of this research. This work follows on from the earlier work of Rowlands [6] and Barrioz [7]. A "baseline" cell, with the optimum parameters to date was grown to identify a starting point for my research (Table 4.1).

Table 4.1: Results of the initial baseline device

Device	η (%)	η +/-	S.D.	FF (%)	J_{sc} (mA/cm^2)	V_{oc} (V)	R_s (Ω)	R_{sh} (Ω)
Sgen 125	4.7*	0.3		50.9	20.8	0.40	1.8	11.4

*Note, Br/MeOH etching (5%) was used to etch the CdTe surface prior to gold contacting.

The device structure for this layer was; (0.24 μm thick CdS deposited at 315 °C, 2 μm thick CdTe: As (2×10^{-6} atm / 2×10^{19} atoms.cm^{-3}) deposited at 390 °C, annealed under hydrogen at 410 °C for 10 minutes. Due to the focus of the research involving the decrease of the absorber layer thickness, initial efforts will be concentrated towards increasing the device efficiency, before decreasing the absorber thickness. Results reported in table 4.1 are an average of 3 devices (from Inlet, middle, outlet positions of the graphite susceptor), each with 3×0.248 cm^2 gold contacts.

4.4 Optimizing growth conditions

4.4.1 $CdCl_2$ treatment

Previous improvements in device efficiency have been undertaken with the aim of avoiding the widely used $CdCl_2$ activation treatment [10, 11]. These efforts concentrated on the use of TDMAAs doping to control the carrier concentration and to passivate the grain boundaries.

In order to increase grain boundary passivation, growth of a thin $CdCl_2$ layer using MOCVD followed by a post growth anneal (at 410 °C) was recently attempted by Barrioz *et al.* [12] on glass. Using the precursors DMCd and TBuCl, a $CdCl_2$ layer (termed the $CdCl_2$ cap layer), has been applied after the growth of the CdTe layer, its novel application to the full CdS/CdTe structure is reported (Fig 4.8), and to the authors knowledge is the first ever reported use in full CdS/CdTe structures using MOCVD.

A series of experiments where the thickness (deposition time) of the $CdCl_2$ was varied (Fig 4.7). The $CdCl_2$ layers were grown in situ, right after the deposition of the CdTe of the baseline 2 μm thick CdTe device. Devices were then annealed at 410 °C for 10 min under hydrogen.

Results are shown with CdS/CdTe devices with high, low and no As doping, to assess the separate roles of TBuCl and TDMAAs. Device parameters are plotted against the $CdCl_2$ layer thickness.

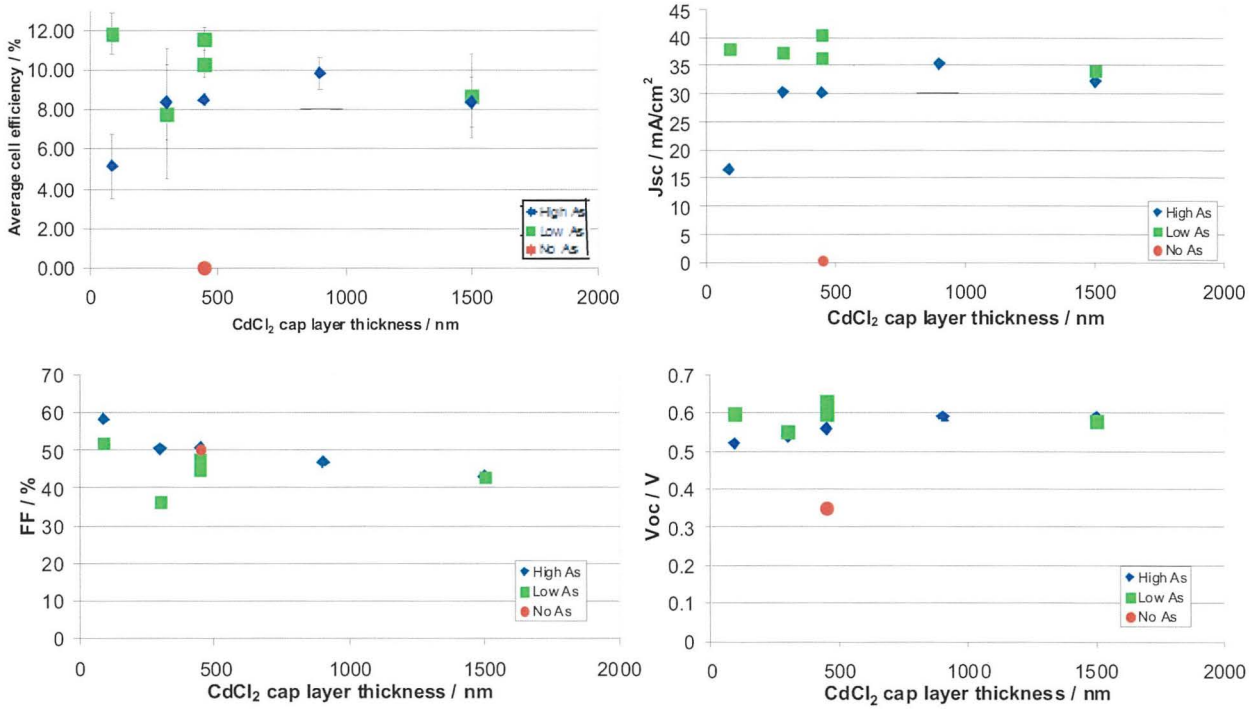


Figure 4.8: Device parameters as a function of $CdCl_2$ cap thickness for layers with no As doping, low As doping and high As doping, as shown. Each point represents an average of 3 0.25 cm2 contacts per device. The light source used here corresponded to the Halogen spectrum (Fig 3.16).

A comparison is made between treatments of layers with no TDMAAs, low As (3×10^{-7} atm / $2x10^{8}$ atoms. cm^{-3}) and high TDMAAs (1.2×10^{-6} atm / $2x10^{19}$ atoms.cm^{-3}) doping. A small peak is observed for the efficiency measurements for a $CdCl_2$ cap thickness of 1 µm (growth time of approx. 6 min), which gave the highest efficiency (with the higher TDMAAs doping concentration) of 10 %, increasing from ~ 4 % where no $CdCl_2$ treatment was applied.

The device which was not As doped, shows little or no photo-activity and suggests that the $CdCl_2$ treatment alone does not effectively 'activate' i.e. passivate the grain boundaries of the CdTe layer. It appears that the As doping is required to provide a p-type doping background in the absence of native defect doping in these layers.

The large error bars observed, shows the effect micro non-uniformities at the junction play, as these result are averages of three 0.248 cm^2 gold contacts. Surprisingly, no large decreases in either J_{sc}, or V_{oc}, are observed when the $CdCl_2$ layer thickness is increased, and perhaps, gives evidence that the layer does not act as a tunnelling layer, as the increased distance of the thicker layer, does not hinder the performance of the device.

Superior performance of the devices with lower As could suggest a possible mechanism by which the As doping / Cl doping interact, being beneficial when lower As (less As is segregated to the GB's / defects, which leaves some free for the Cl to dope) is used.

4.4.2 Growth of the baseline (CdS/CdTe) device

The improvement in the CdS/CdTe device efficiency (Table 4.4) to 10% has been a vital part of this research. Once sufficient conversion efficiency (target 10%) has been reached, the absorber thickness can then be reduced, to investigate the limitations on ultra-thin devices.

The adopted baseline device consists of;

1. A (0.24 μm) thick CdS/ (2 μm) CdTe
2. The device is then doped using As at a level of $2\times10^{18}cm^{-3}$ atoms.
3. A 0.5μm highly As doped BCL is then deposited.
4. A layer of $CdCl_2$ is subsequently grown on top of the BCL at 200 °C.
5. The entire structure is then annealed under hydrogen at 420 °C for 10 minutes.

Table 4.2 shows the results of key films which along with their deposition conditions. The inclusion of a light soaking step during I-V measurement, (10 min light soak at AM1.5 conditions, and 5 min cool) led to an increase in the average baseline device efficiency to 10.3% +/- 0.4 (Table 4.5).

Table 4.2: Device structure evolution and associated AM1.5 conversion efficiency

Device Structure	**AM1.5 Conversion efficiency (%)**
Glass/ITO/CdS/CdTe (no As doping)	0
Glass/ITO/CdS/CdTe/$CdCl_2$ (no As doping)	1
Glass/ITO/CdS/CdTe (low As doping (1×10^{17} cm^{-3})	2
Glass/ITO/CdS/CdTe (As 2×10^{18} cm^{-3})	5.7
Glass/ITO/CdS/CdTe (As 2×10^{18} cm^{-3})/$CdCl_2$	6.1

Cross-over of light /dark IV was observed in almost all devices produced. Fisher *et al.* [13] also report I-V cross-over in their devices, and attributes it to the excessive Cu doping of their CdS. However Fisher *et al.* [13] do conclude that the observed crossover does not affect the photovoltaic behaviour of the final device. Figure 4.9 shows the cross-over behaviour observed in devices (CdS/CdTe baseline) grown by MOCVD.

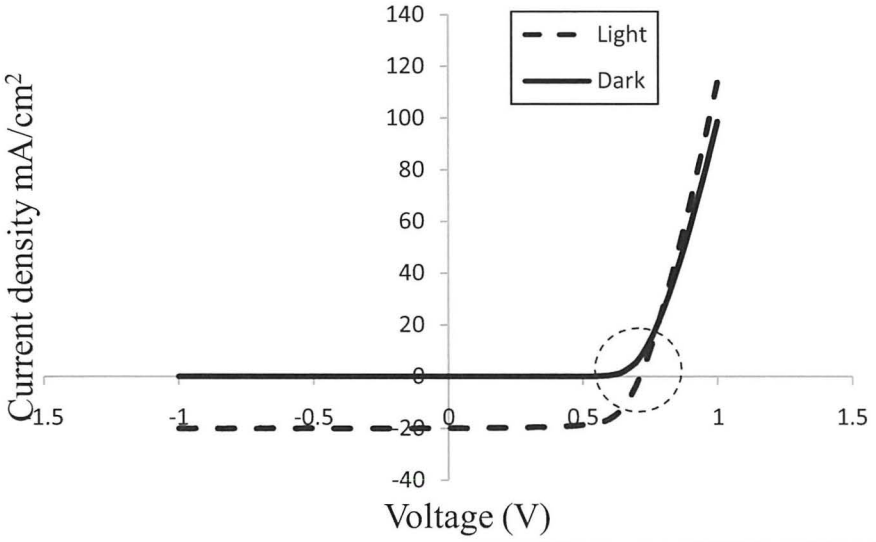


Figure 4.9: A typical light/dark crossover I-V curve, of a baseline CdS/CdTe device.

Niemeegers *et al.* [14] have put forward a theory that cross-over in I-V curves. It has been proposed that the cross-over occurs as a result of the surface recombination current of electrons at the metal surface. Transport through the Au/CdTe back contact is then limited by drift and diffusion causing this observed phenomenon.

The presence of a Schottky barriers are known to cause roll-over of the *IV* curves. However, due to the BCL, the roll-over behaviour is negated, and does not explain the continued presence of the cross-over. The presence of a minority carrier (electron) current could possibly be present at the CdTe back contact, giving rise to "cross-over" of the I-V curves, but has not been investigated. Red illumination and thinner cells (< 5 μm) favour cross-over [15] given their larger electron diffusion length [16].

4.4.3 Arsenic Doping Concentration

The dopant level has been estimated [17] from $1/C^2$ versus reverse V plots using Eqn. 4.3. (Fig 4.10)

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\varepsilon_s N_A} \qquad 4.3$$

C-V profiling induces a depletion region, a region which is empty of conducting electrons and holes, but may contain ionized donors and electrically active defects or *traps*. The depletion region with its ionized charges inside behaves like a capacitor. By varying the voltage applied to the junction it is possible to vary the depletion width.

The dependence of the depletion width upon the applied voltage provides information on the doping profile and any electrically active defect densities. The cell to be measured is connected electrically, and dark CV measurements at a frequency of 150 kHz are conducted at room temperature. This frequency has been chosen to avoid contributions from deep states, which can be ignored at frequencies >120 kHz. Cells are biased from -1.40 to +0.6 V as > + 0.6 V represents a transition to a regime dominated by capacitance at the back contacts. More details regarding the CV equipment and results are available in the attached paper at the end of this thesis.

To identify the dominant recombination process, various models will be considered; For multi step tunnelling-recombination, the forward current may be expressed using Eqn. 4.4;

$$J_f = J_0(T)\exp(AV) \qquad 4.4$$

Where A is the slope of $\ln I_0$ Vs V. The constant A can be used to determine the tunnelling steps required for carriers to pass through the depletion region as [18]. Where $A = \alpha R^{-1/2} K$, $\alpha = (\frac{\pi}{4\hbar})(\frac{m_n \varepsilon_p}{N_A})^{1/2}$, $K = 1 + (\frac{\varepsilon_p N_A}{\varepsilon_n N_D})$, R is the number of tunnelling steps, m_n is the electron effective mass, ε_n and ε_p are the dielectric constants of the n-type and the p-type respectively and N_A and N_D are the doping concentration of acceptors and donors respectively.

Assuming that N_D is much larger than N_A gives $K \approx 1$. Doping concentration was calculated to find the value of α. C-V measurements at a frequency equals to 150 KHz were used to find N_A. Figure 4.10 demonstrates the $1/C^2$-V curve and data is shown in Table 4.3.

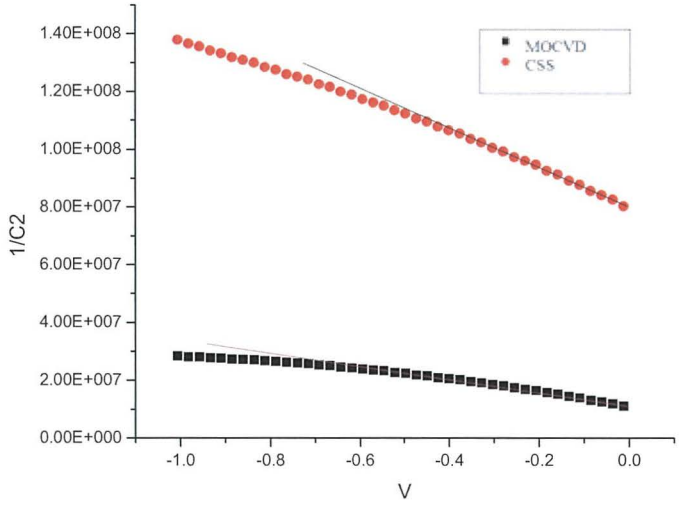


Figure 4.10: $1/C^2$ versus reverse V for samples baseline MOCVD (SGEN 254) and baseline CSS (290-3).

Table 4.3: parameters extracted from C-V curves to obtain doping information.

	Slope of $1/C^2$ vs V	N_A /m^3	Slope of LnJ vs V (dark) [A]	Number of tunnelling steps
MOCVD CdS/CdTe	2.55×10^{7}	5.36×10^{15}	25.75	125
CSS CdS/CdTe	6.57×10^{7}	2.07×10^{15}	22.29	432

Calculated doping concentrations are similar to those obtained by Al-Allak *et al.* [18]. Calculations of V_{bi} gave 0.43 V for the baseline MOCVD CdS/CdTe and 1.2 V for CSS CdS/CdTe, suggesting that the built in potential of the CSS baseline cells are slightly larger than MOCVD, despite higher doping levels being achieved by the MOCVD grown as doped baseline CdTe device.

4.5 Spectral response measurements

A monochromatic probe based on a Bentham TMc300 single monochromator and a Xenon/Quartz halogen light source, was used to illuminate the sample under test, giving coverage over the spectral range 350-950 nm. The quantum efficiency (QE) curve of a baseline CdS/CdTe device is shown in Fig 4.11.

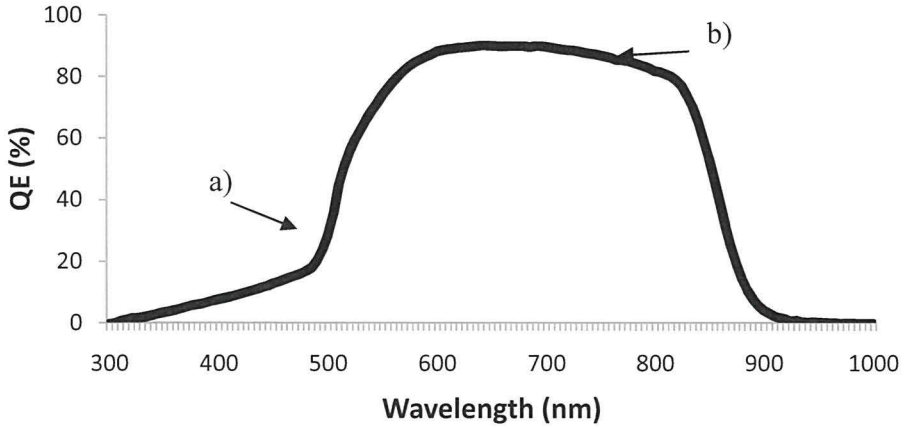


Figure 4.11: Spectral response curve of a CdS (240nm)/CdTe (2000nm) baseline device (CSER 28) showing large blue absorption between 400-500nm.

This reveals that the CdTe films were strongly absorbing throughout the wavelength region (500–800 nm) , and is in good agreement with other authors [19]. The highlighted features at a) shows the large blue absorption loss, due to the CdS thickness, b) The observed fall in QE at 700 nm towards 850 nm, can be attributed to poor grain boundary passivation.

Variation of the atomic Zn_x fraction in the ternary alloy ($Cd_{1-x}Zn_xS$), was achieved by varying the DEZn:DMCd precursor ratio, maintaining the DtBS precursor partial pressure at 3×10^{-4} atm. Uniform films with good adhesion were obtained throughout the studied composition range (Zn x=0 to x=0.55), achieving typical growth rates of 0.5 nm/s. Initial incorporation of zinc was assessed using EDX and later accurately determined by RBS elemental analysis [20] (discussed in Chapter. 3).

Growth of the $Cd_{1-x}Zn_xS$ layer, at the standard CdS temperature (315 °C) yielded very low zinc inclusion. Increase of the growth temperature to 360 °C, led to more zinc incorporation to be detected (using EDX), and could be evidence for the increased extent of ZnS formation at higher temperatures, contrary to Chu *et al.* [21].

The incorporated zinc fraction for growth at 360 °C, measured using RBS (Fig. 4.12), is seen to be markedly less than the corresponding gas phase precursor ratio, and appears to increase linearly. A maximum achievable (using current reactor setup) DEZn/DMCd precursor ratio of 0.7, gave a measured zinc concentration of $Zn_{0.55}$. This upper limit in precursor ration was only due to the maximum obtainable steady flow setting in the precursor line used.

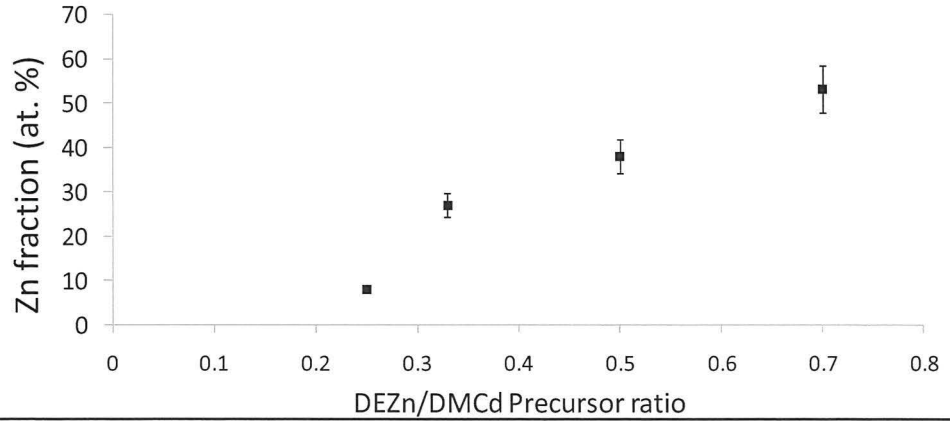


Figure 4.12: Measured Zn fraction (at. %) versus DEZn:DMCd precursor ratio.

4.6 $Cd_{1-x}Zn_xS$ ternary alloy

XRD diffraction patterns in Bragg-Brentano (θ-2θ) geometry, show that low Zn concentration solid solutions are similar to hexagonal CdS (being strongly (002) orientated). Figure 4.13 shows an XRD spectrum of $Cd_{1-x}Zn_xS$ film deposited on glass, to avoid ITO reflections. Peaks can be assigned to the hexagonal (wurzite) form of $Cd_{1-x}Zn_xS$.

The observed peak splitting, of the (002) peak (Fig 4.24) suggests the presence of multiphase material, with possible spinodal decomposition occurring in this composition range (x_0 to $x_{0.38}$). The increase in the Zinc concentration in the CdS lattice results in a loss of (002) preferred orientation and finally a conversion from a hexagonal wurtzite to a cubic zinc blende structure with higher Zn concentrations, which has also been reported by Lee *et al.* [22].

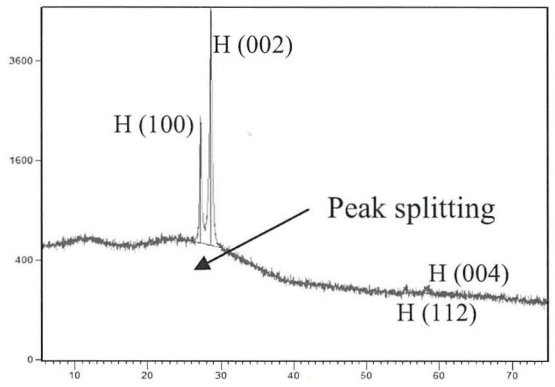


Figure 4.13: $Cd_{0.62}Zn_{0.38}S$ grown on glass (240 nm)

Preferred orientation, is calculated using Eqn. 4.5 [23].

$$p(hkl) = \frac{I(hkl)}{I_o}\frac{1}{N}\sum hkl\frac{I(hkl)}{I_o(hkl)} \quad 4.5$$

Where N is the number of peaks in the region considered, I(hkl) is the measured intensity of peak hkl and I_0(hkl) is the intensity of the corresponding peak from a powder sample. p(hkl) =1 would suggests that the peaks are randomly orientated, and >1 would indicate a preferred orientation, and <1 a loss of preferred orientation.

Figure 4.14 shows the (002) reflection, shifts to higher angles with increasing zinc concentration. The (002) preferred orientation decreases with zinc concentration. The (002) texture coefficient (TC) (Eqn. 4.4), of MOCVD grown $Cd_{1-0.1}Zn_{0.1}S$ has been calculated as 1.09, indicating a slight (002) preferred orientation. The (002) relative intensity remains at 100 (compared to 91 for a random CdS sample (JCPDS file no. 41-1049), with increasing Zn, until the cubic conversion is observed.

This cubic conversion with higher Zn concentration has been previously reported by Lee *et al.* [22]. ZnS and CdS are known to exist in either the cubic (zinc blende) or hexagonal (wurtzite) crystal structure depending on the preparation conditions [24].

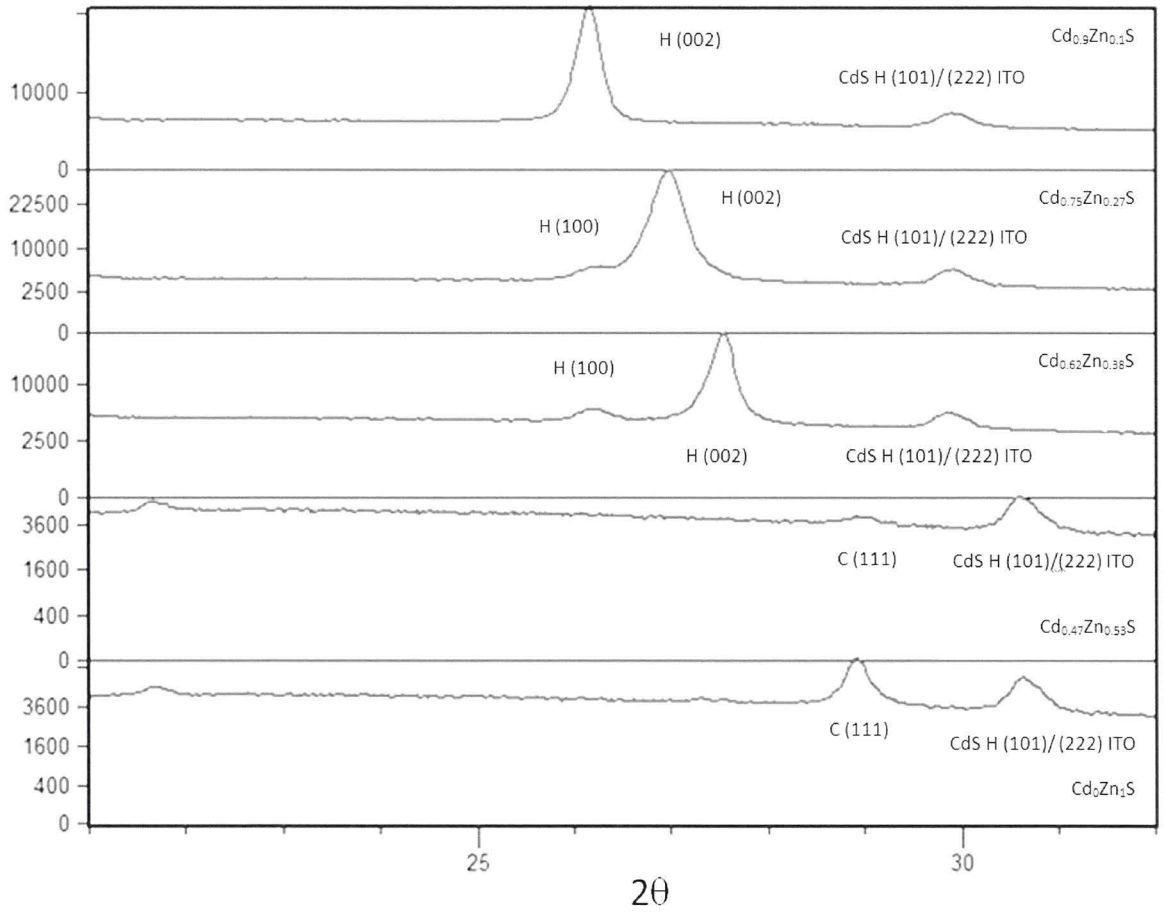


Figure 4.14: XRD pattern showing the effect of increasing the Zn content in the $Cd_{1-x}Zn_xS$ window for films grown at 360 °C. The lattice parameters of the cubic films (Zn(x=0.53) and Zn(x=1) are a= 5.37and a= 5.31 respectively.

The hexagonal lattice components (a_o and c_o) have been calculated [22] where the shift of the (002) peak is related to the decrease in the lattice constant (Fig. 4.14), the results a agree with previously reported literature [22, 25] showing a tetragonal shift. Figure 4.15, shows the relationship between lattice parameters (a_o and c_o) and Zn composition (x) showing an increased stress with higher concentrations of Zn.

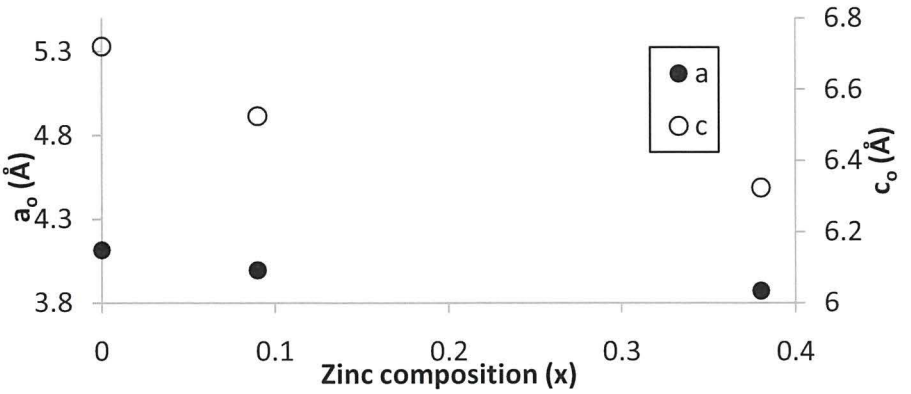


Figure 4.15: Graph showing the change in lattice parameter (for hexagonal $Cd_{1-x}Zn_xS$ layers) with increasing Zn fraction.

4.6.1 UV-Visible spectrometry of $Cd_{1-x}Zn_xS$ layers

A plot of $(\alpha E)^2$ versus energy (hv) (Fig. 4.16), and extrapolation of the linear portion of the curve to the intercept was used to approximate the band gap energy [26]. Where α is the absorption coefficient of the material as a function of frequency for a direct (allowed) transition.

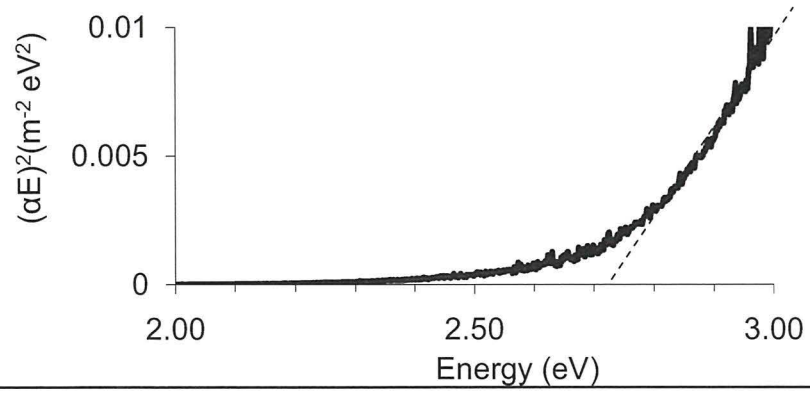


Figure 4.16: A plot of $(\alpha E)^2$ versus energy (hv) showing extrapolation of the linear portion to approximate the band gap.

Figure 4.17 shows the optical band gap increases from x = 0, (2.45 eV) to x = 0.55 (3.5 eV), having an unexpectedly large band gap, close to that of ZnS (3.55 eV). Initially very low Zn values give a gradual change in the E_g, when a higher Zn rich concentration > $x_{0.35}$ is reached, a large increase in E_g is observed, suggesting a large physical change in the material which agrees well with the XRD spectra.

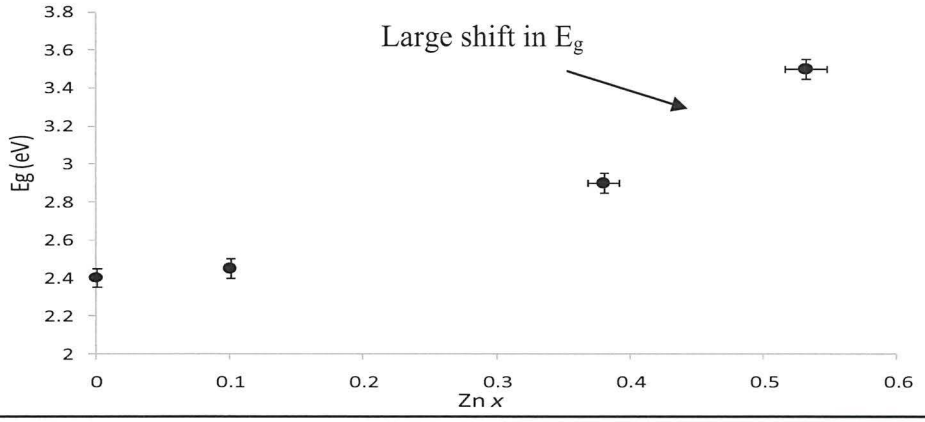


Figure 4.17: Measured $Cd_{1-x}Zn_xS$ band gap versus atomic zinc concentration.

The large observed increase in the E_g, at higher Zn(x) concentrations, supports XRD data, which shows that the crystal lattice is transforming, becoming increasingly stressed. This region is also likely to include mixed phase $Cd_{1-x}Zn_xS$ solid solution, and accurate determination of E_g in this region is consequently complex. This observation could also explain why initial attempts at making full devices with layers > $x_{0.35}$ Zn concentration gave very poor device results, especially V_{oc}, as the region will be very sensitive to small changes in Zn concentration (expected with non uniform films) which would hamper a homogeneous uniform (and constant Eg throughout the layer), increasing the variations in E_g in the film hindering uniform electrical homogeneity.

The simplest relationship of increased band gap with zinc concentration would follow Vegard's law, where a linear relationship would be found. However, the data in Fig. 4.17, displays a non Vegard type relationship, and agrees with several authors [27, 28], who have reported observing such non-vegard behaviour with increasing Zn_x concentration.

Two separate regions can be said to exist, one region at x = 0-0.4, where a gradual increase in band gap is seen, and another at x = 0.4-0.6, where a large increase in band gap is observed for a small increase in Zn. This could suggest a mixed phase region, which is consistent with spinodal decomposition.

Hill and Richardson [29] have deduced a composition dependent bowing parameter from the following equation, which describes the energy gap, $E_g(x)$, of the $Cd_{1-x}Zn_xS$ solid solution (Eqn. 4.6);

$$E_g(x) = E_g(CdS) + [E_g(ZnS) - E_g(CdS) - b]x + bx^2 \qquad 4.6$$

Where *Eg*(CdS) and *Eg*(ZnS) are the values of the energy gap for CdS and ZnS, respectively, and *b* is the bowing parameter.

However, authors [30] have previously calculated the bowing parameter with just a single band gap (when the Zn concentration is known).

The bowing parameter "b" has been calculated, for devices with 10% Zinc incorporation (measured from RBS), b =1.1 eV. More deviation in the E_g values is observed at higher zinc concentrations than in the reported literature [27], but this is not unexpected given the large relationship of the layer chemistry is dependent on the individual process (and somewhat reactor geometry, conditions and precursor used).

4.6.2 Zn rich CdZnS/CdTe devices

A range of $Cd_{1-x}Zn_xS$ devices with varying DEZn concentrations have been grown (Table 4.4). Using pre-grown CdZnS layers (240 nm), CdTe was then deposited on a number of CdZnS pre-grown layers, allowing a consistent and comparable CdTe layer to be achieved in the devices. As two separate deposition steps (as the pre-grown layers have to be removed from the chamber) is involved, increasingly the possibility of surface contamination, devices grown in this way tend to be less efficient and should only be used for comparison purposes with the other films in table 4.4.

Table 4.4: Device results of 2μm thick CdTe devices grown on top of various wider band gap window layers to investigate the effect of changing alloy composition on device performance.

DMCd:DEZn Precursor conc (10^{-4} atm) and RBS measurement (x)	Band gap (eV)	Efficiency (%)	V_{oc} (mV)	FF(%)	J_{sc} (mA/cm^2)
1.9:1.05 (x =0.10)	2.7	8.8	630	66.5	21.0
0.95:1.50 (x =0.38)	3.0	6.7	490	62.4	21.7
2:2.25 (x =0.53)	3.4	6.1	460	61.0	21.5

Preliminary experiments of devices with window layers with high DEZn (Zn x > 0.53) concentrations resulted in devices with lower V_{oc}, where its sheet resistance was too high to be measured (>1000 kΩ) by four point probe. The dark lateral resistivity of doped $Cd_{1-x}Zn_xS$ films are known to increase rapidly with increasing Zn concentration [21]. For this study, a zinc concentration of x= 0.1, gave the best devices, increasing the optical band gap of the window layer by 0.25 eV (from 2.45 eV to 2.70 eV).

Surprisingly, a higher than expected band gap was achieved for the $Cd_{0.25}Zn_{0.75}S_1$ device, which was close to the ZnS value (3.55 eV at room temp.), given the relatively low RBS measured Zn content of just x = 0.53.

Increasing the DEZn/DMCd ratio, promotes increasing the lattice mismatch, and an increased series resistance (R_s) [22, 25] at the $Cd_{1-x}Zn_xS$ /CdTe junction. This in turn increases potential junction recombination and can reduce the V_{oc} [22]. If one notes that the conduction band (CB) discontinuity at the junction, increasing the Zn content will inevitably increase the CdZnS/CdTe CB discontinuity, which will negatively, affect the V_{oc}, this agrees well with MOCVD devices made with higher Zn content.

Therefore, an optimal DEZn concentration might be reached, where the decrease in V_{oc} is offset by the increase is short-circuit current (J_{sc}) arising from the shorter wavelength photons, improving overall device conversion efficiency. Lee *et al.* [22] also report improvement in V_{oc} for x= 0 to x= 0.35, and attributed it to a reduction in the electron affinity mismatch at the CdS/CdTe interface.

Substitution of the CdS by a $Cd_{1-x}Zn_xS$ window layer has been reported to reduce electron affinity mismatch [22] at the $Cd_{1-x}Zn_xS$ /CdTe interface, but was not investigated in this study. No significant deterioration of the V_{oc}, as a result of increased sheet resistance in $Cd_{0.9}Zn_{0.1}S$ was seen as reported by other authors [21].

When the electron affinity (χ) of the window layer (CdZnS 4.4 eV, CdS 4.5 eV) is larger than the absorber (CdTe 4.28 eV), the built in voltage, and hence V_{oc} may decrease [31]. But when the χ of the window layer (ZnS 3.9 eV) is smaller than the absorber (CdTe 4.28 eV), a conduction spike is likely to occur [31], which can interfere with the minority carrier transport.

4.7 Reducing absorber thickness

4.7.1 Introduction

MOCVD, due to its capability for depositing high quality layers, has been used to reduce the absorber layer thickness (keeping a high film quality throughout). This has allowed the investigation of very thin *pn* junction devices with good conversion efficiency, where the device has not been limited by the layer quality, as the thickness is decreased. This has previously not been possible, as the high level of control (and uniform coverage) needed are only available with some techniques, where device efficiencies were previously very low. This allows the investigation where the absorber volume and device parameters can be interrelated.

Reducing the CdTe absorber thickness to below the absorption limit of 1 μm, has the beneficial consequence of reducing material usage and addresses carrier recombination loss towards the back contact, as the proximity between the back contact and the main *pn* junction comes ever closer. The absorber layer thickness for thin film CdTe solar cells, made by variety of deposition methods is normally between 2 μm and 10 μm thick. Thicker absorber layers are generally used to avoid pinholes reaching through to the window layer, which may lead to shorting from the back contact.

Not only does the reduction of the absorber layer offer an insight into the device physics and capability of the deposition technique, but can also provide flexibility in device designs including; (i) its use in tandem solar cells, with transparent back contacts (e.g. ZnTe) [32] and (ii) as potential PV glazing devices given their increased transparency.

Since CdTe is a direct band gap semiconductor, the optical absorption coefficient rapidly attains the values of 1×10^{-4} cm^{-1} and above, as the photon energy exceeds the band gap. Over the entire intrinsic absorption region, the optical penetration depth for the semiconductor is < 1 μm i.e., all the available AM1.5 photons (> 400 nm and <850 nm) can be absorbed, if the thickness *d* of the CdTe layer is larger than several micrometers, namely, ~63 % at $d = 1$ μm, ~86% at $d = 2$ μm, and ~95 % at $d = 3$ μm [10].

Theoretical calculated carrier generation by Amin *et al.* [33], has been shown to be at its highest value, near the CdS/CdTe junction, reducing by two orders of magnitude within the first 1 μm. This indicates the importance of the quality of the CdTe within the first 1 μm, which encompasses the hetero junction and the depletion region, where most of the carriers are generated and collected close to this region.

4.7.2 Baseline repeatability

Towards obtaining a repeatable process, 5 identical growths of CdS/CdTe layers was undertaken. Averaged results of five separate CdS/CdTe baseline devices (**CdS/CdTe baseline structure:** Glass/ITO/CdS/CdTe (As $2\times10^{18}cm^{-3}$)/CdTe:As BCL layer/ $CdCl_2$) are shown in table 4.5.

Table 4.5: CdS/CdTe baseline device repeatability

Efficiency* (%) (+/- S.D 0.5)	J_{sc} (mA/cm^2) ((+/- 0.5)	FF (%) (+/- 0.5)	V_{oc} (mV) (+/-) 30
10.2	23.8	66.2	655

* Efficiency here has been initially measured using the xenon lamp setup and are average cell parameters for 5 separate devices, each of average 3×0.248 cm^2 gold contacts.

The attainment of over 10 % efficiency is the fulfilment of one of the main targets of this thesis and of the PV supergen research programme which funds this research, and represents an end to baseline device improvements/optimization. What follows is the novel work of utilizing the inherent materials control offered by MOCVD, to interrelate materials quality with device quality. This is firstly done through monitoring the effects (optical and electrical) of reducing the CdTe absorber area, and later concentrates on extending the band gap of the window layer, to facilitate an increased photocurrent (to counteract the expected decrease in photocurrent when reducing absorber area to investigate the material and device limitations (both electrical and/or optical limitations/effects).

4.7.3 Growth of very thin CdTe layers

A series of CdTe layers (using baseline device growth conditions of 390 ^{o}C and annealed at 410 ^{o}C for 10 min) were grown on glass. The absorber thickness was decreased from the baseline thickness (2 μm) down to 0.2 μm.

Figure 4.18 shows a graph of grain size Vs. CdTe absorber thickness. The grain size has been estimated from the intercept approach for measuring grain size as described by Heyn (1904). In this method, one or more lines are superimposed over the structure at a known magnification. The true line length is divided by the number of grains intercepted by the line. This gives the average length of the line within the intercepted grains. This average intercept length will be less than the average grain diameter but the two are interrelated. In MOCVD grown CdTe layers, the grain size is expected to decrease, with thickness. Reducing the absorber layer thickness, so that it becomes analogous to the grain size, increases the significance of Grain/GB contributions and recombination at the GB [34], thus the effect of the $CdCl_2$ treatment is likely needed to be optimized (as using the same conditions for thicker films, the grains for thinner devices could be over treated).

The observed results show that grain size using MOCVD, develops slower than the thickness of the film (for the thicknesses and deposition temperature range used), and appears controllable. Of course, if the temperature is altered, different growth rates and grain size and orientations might be obtained, thus it can only be said that a narrow grain change is achieved given the precise deposition parameters (and somewhat reactor geometry) used.

However, it should be noted that the grains near the junctions don't change in size (unless the $CdCl_2$ treatment affects the grains), as only the grains close the surface that are affected by layer thicknesses.

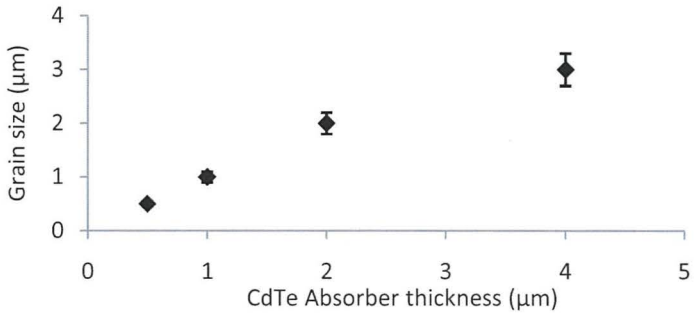


Figure 4.18: Approximated grain size profile of a CdTe layer deposited on glass taken from top down SEM images.

To investigate the change in the CdTe surface, a CdTe growth (Sgen 72), where an intentional thickness gradient has been used to obtain varying absorber thicknesses has been grown (10, 6 and 1 µm). XRD has been employed, using the theta-two theta Bragg-Brentano geometry (Fig 4.19) to determine any changes in the crystal structure of the layer with thickness.

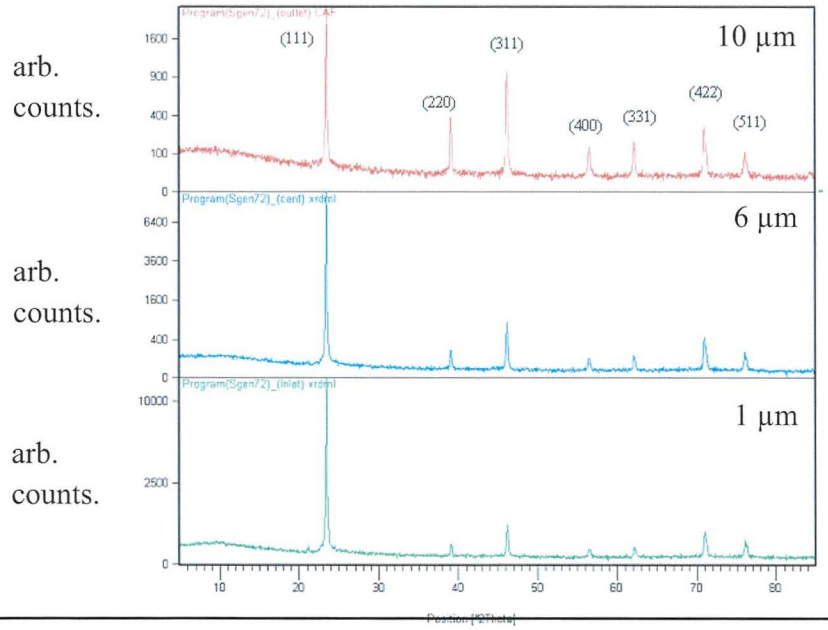


Figure 4.19: X-ray diffraction results of wedge profile film grown at a reduced flow rate to reveal different thicknesses of CdTe (Sgen 72).

Harris analysis, confirms a decrease in the texture coefficient (TC) C_{111} from 0.587 to 0.157 (10 μm to 2 μm respectively), becoming less preferentially (111) orientated as the film thickness is increased.

The prevalence of the (111) orientation for CdTe cells is explained by the kinetically limited nature of the CdTe reactions, at low temperatures [35]. For randomly orientated nuclei, the fastest growing planes normal to the substrate will grow faster, in our case this is the (111) CdTe plane [36]. The (111) plane is parallel to the substrate, thus growth occurs in the upwards direction (towards the CdTe top surface), this can be seen in cross-sectional SEM image.

The growth mechanism is thought to take the form of high density nucleation which forms a uniform surface. Thus, initially grains grow sideways (parallel to the substrate), until a uniform surface coverage is achieved. Evidence for this, is that in order for the in-situ interferometry to receive a signal (using Febry-Perot interference), a uniform surface must first be present. This is achieved slowly for the CdS (due to initial nucleation delay) and quickly for the CdTe layer, probably due to grain templating.

After the growth of the initial surface (with small CdTe grains (comparable to those of the CdS layer)), the only direction for the grains to grow is up, and thus, an inverted pyramid type grain structure takes dominance. A cross sectional SEM image has been included (Fig 4.20).

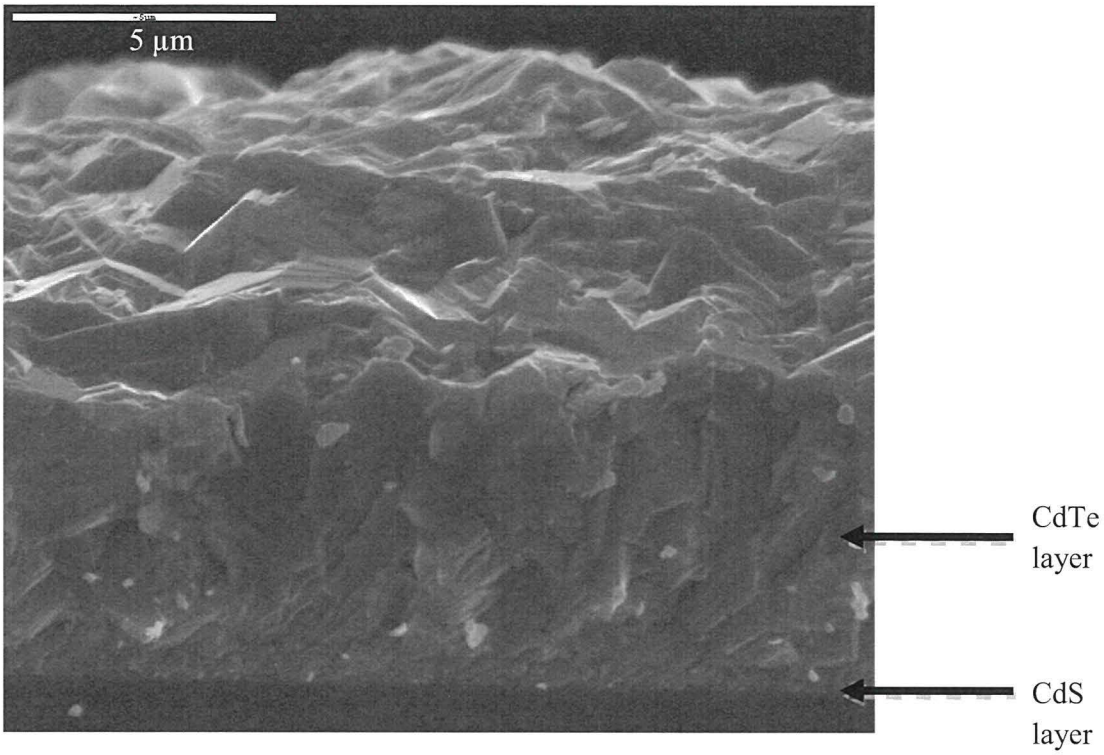


Figure 4.20: Cross-sectional SEM image of the CdS/CdTe junction.

4.7.4 Back contact formation on very thin CdTe devices

For the 2 µm thick baseline device, the BCL consist of the growth of a 250 nm highly As doped (2×10^{19} atoms.cm^{-3}) CdTe layer (which roughly represents 10 % of the overall CdTe absorber thickness).

The BCL has been shown to reduce R_s of baseline devices from ~10 Ω to ~2 Ω negating the need for etch treatment prior to back metallic contact formation (with gold). A study to determine if the BCL will have the same function for ultra thin devices was undertaken. Firstly, an investigation where the absorber layer was decreased for CdS/CdTe devices, as the CdS/CdTe junction properties are currently better understood than the $Cd_{0.9}Zn_{0.1}S$/CdTe junction.

The BCL thickness has been modified for inclusion in the ultra thin devices, and has been decreased in thickness from 250 nm to 100 nm, to represent ~10 % of the absorber thickness. It was decided to keep the BCL thickness 100 nm for all films less than 1 µm thick, too ensure a uniform BCL film is obtained.

Ultra thin (<1 μm) devices, (**Device structure:** 900 nm CdTe + 100 nm **BCL**) have been grown. To ascertain if the role of the BCL is the same in very thin devices, devices with and without the BCL have been grown. Their associated I-V curves (Fig 4.21), shows that the ultra thin devices with no BCL, showed no roll-over behaviour.

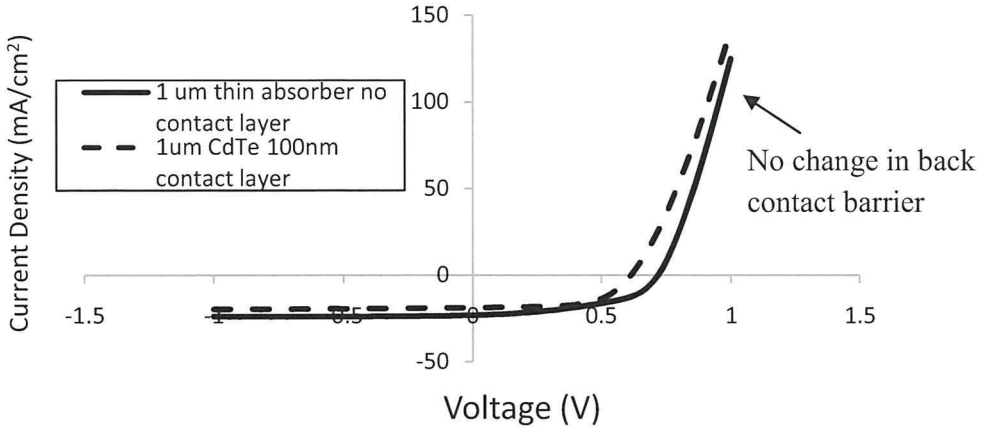


Figure 4.21: Light I-V profiles of 1 μm thick CdS/CdTe devices (i) with BCL present and (ii) NO Cl layer.

Fig 5.4, shows that the ultra thin devices do not suffer from roll-over behaviour similarly to the standard CdS/CdTe (2 μm) baseline device (Fig 4.10). This suggest that for thinner absorber devices, the TDMAAs doping level is already sufficient (3×10^{-7} atm) (at only an *in situ* dopant level of 2×10^{18} atoms.cm^{-3}) to provide a lower back barrier to improve back contact formation, possibly reducing back-contact surface recombination.

In the standard BCL for baseline devices, the CdTe doping at the back contact was increased, so that the hole current through the contact is described by drift and diffusion through the space charge layer (SCL); this effects weakens the aspect of the roll over, and eventually the room temperature I-V curve looks as if only a small barrier is present [37]. If one assumes an already high doping exists at the back contact region for thinner absorbers, this makes the apparent barrier increasingly dependent on bias voltage and illumination [37].
Though the effects render the determination of the barrier from room temperature I-V measurements doubtful, they generally influence the fill factor and the efficiency in a positive way.

If one compares the device performance of devices in Table 4.6, it is clearly seen that although the BCL is not needed on the account of the R_s for optimal back contact formation, the device performance is boosted by its presence.

Table 4.6: Device parameters for ultra thin (1 μm) absorber devices i) 1 μm thick CdTe with baseline settings (including a BCL layer at), ii) 1 μm thick CdTe with baseline settings (with NO BCL layer) and iii) 1 μm thick CdTe device which has been highly doped by a TDMAAs setting of 2×10^{-6} (atm) throughout the CdTe growth (with NO BCL layer)

TDMAAs partial pressure (atm)	BCL	Efficiency (%) +/- 0.2	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	R_s (Ω·cm^2)
i) 3×10^{-7}	Yes	11.4	20.6	0.75	74.1	2.1
ii) 3×10^{-7}	No	8.2	19.7	0.65	64.2	2.2
iii) 2×10^{-6}	No	8.9	21.5	0.65	64.2	2.0

4.7.5 Ultra thin devices: I-V results

Figure 4.22 shows I-V curves of three ultra thin CdS/CdTe devices i) 2 μm ii) 1 μm and iii) 0.5 μm, which only differ in absorber thickness.

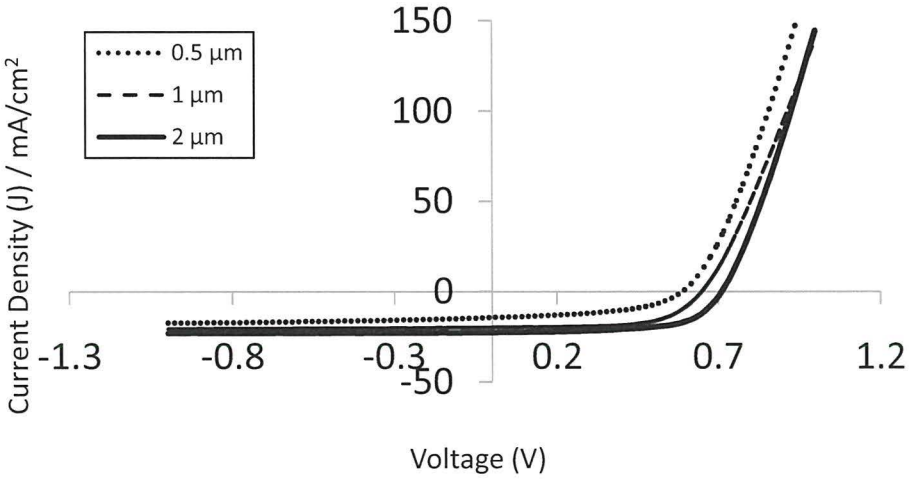


Figure 4.22: Illuminated I–V curves (under 100 mW/cm^2 xenon lamp illumination) for i) 0.5 μm, ii) 1 μm and iii) 2 μm absorber thickness.

The device behaviour shows an expected trend consistent with reduced absorber volume. Series resistances measurements (approximated from I–V curves) (Table 5.3), show that no significant change is seen, even though decreasing the absorber thickness, increases the effective electron current, and increases the voltage dependence in the back contact region [15].

This (Fig 5.6) demonstrates that the back contact barrier is unaffected by large changes in absorber thickness, and/or the closer proximity to the *pn* junction None of the grown devices display rollover features in illuminated I–V, indicating good back contact formation.
A large decrease in shunt resistance with decreasing absorber thickness is observed (Table 4.7). Such increase in R_{sh} is possibly caused by inhomogeneities in the film, creating micro-junctions, promoting localised shunting regions.

Table 4.7: Series and shunt resistance values for i) 2 μm ii) 1 μm and iii) 0.5 μm thick absorber CdS/CdTe devices.

Absorber thickness (μm)	Series resistance (R_s) Ω ·cm^2	Shunt resistance (R_{shunt}) (Ω)
2	1.9	2688
1	2.3	1062
0.5	2.0	315

Dark I–V curves (Fig 4.23), however, show how increased recombination currents occur for the thinner (0.5 μm) device in the reverse bias region. The dark I–V curves show, that when the absorber thickness is reduced below the CdTe absorption thickness (~1 μm), recombination increases and dominates device characteristics. The breakdown in reverse bias for thinner absorber layers, may indicate that the electric field, could be slightly higher for thinner devices, making it more sensitive to trap assisted tunnelling. Gupta *et al.* [38], also report no roll-over for ultra thin CdTe layer devices (0.75, 1.0, and 1.5 μm), but does not go into detail regarding possible causes.

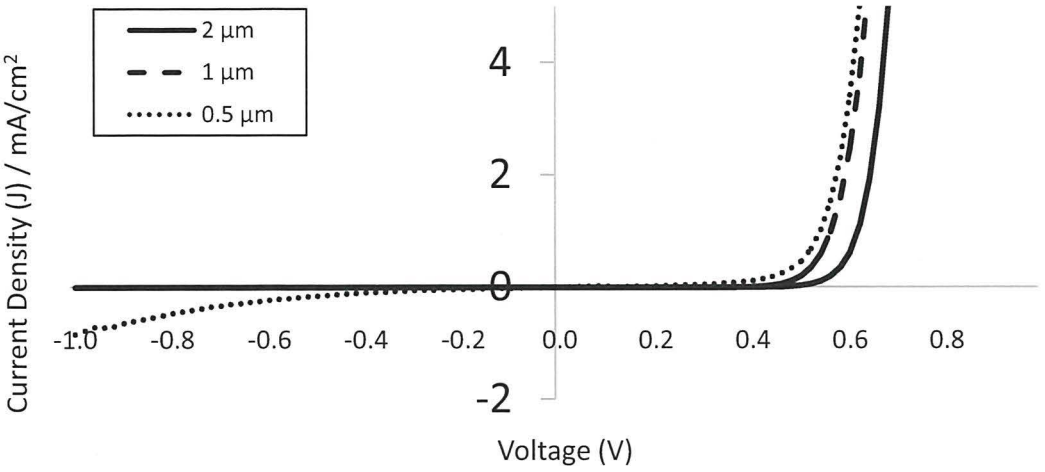


Figure 4.23: Dark J-V curves of cells with different absorber thickness showing increase recombination for the thinner cells.

Such a large lowering of the shunt resistance, for ultra-thin absorber devices, suggests that the I-V is completely dominated by shunting (even at low voltages) [39]. It is known that the shunt resistance changes dramatically with light intensity [39].

The depletion layer thickness of the ultra thin films has also been estimated, obtained from a C-V profiling study (Table 5.4).

Table 4.8: Space charge layer thickness calculation of ultra thin CdS/CdTe device (ref to. Chpt. 4.9).

Device	Doping concentration (cm^{-3})	$\emptyset_{fp}$(V)	χ_{dT}(µm)
1 µm thick CdS/CdTe baseline	10^{14}	0.38	0.29

The estimated depletion width is slightly larger than that measured for the 2µm baseline CdS/CdTe device (0.22 µm), this suggest that the depletion layer represents a much larger proportion of the device, increasing the photon collection probability.

4.7.6 C–V analysis of ultra thin devices

The C–V curve (Fig 4.24) shows an increase in the capacitance with decreasing absorber thickness, suggesting increased carrier density in the measurement region. In reverse bias, for bias voltage (V_b) lower than − 0.2 V, the capacitance in all cases saturates, where the samples are fully depleted of majority carriers. The thickest sample (i.e. 2 μm CdTe) shows a noticeably weaker increase of capacitance with increasing voltage as compared to other samples despite all having the same arsenic doping conditions, which indicates a transition to a regime dominated by capacitance at the back-contacts [40].

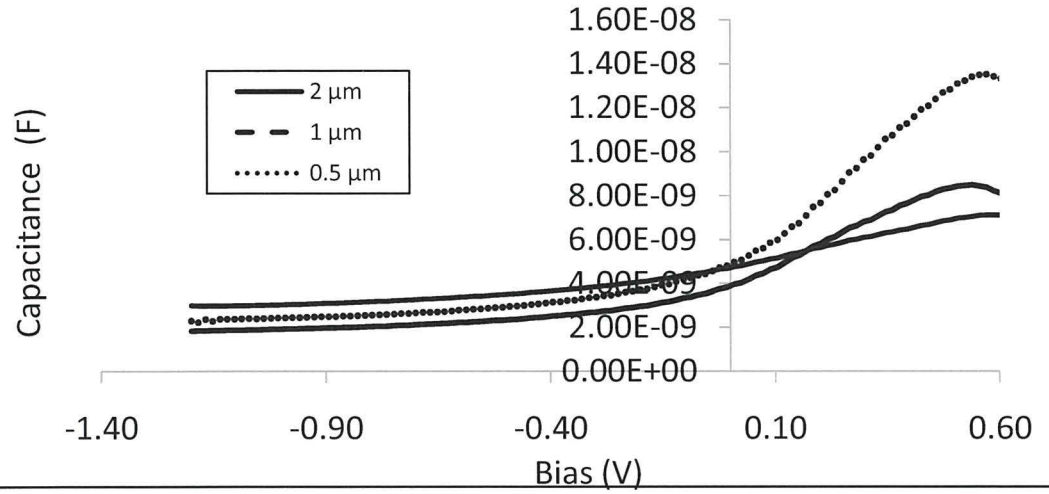


Figure 4.24: Dark C–V curve of CdS/CdTe junction devices with differing CdTe absorber thicknesses.

C–V analysis confirms the presence of a larger increased built-in field with thinner CdTe cells, having a larger capacitance value at forward bias. This should in theory be beneficial to the device, but could also be detrimental to the cell since the probability of impurity migration is also increased, thus a long term stability study of thinner cells should be investigated.

The increase in the capacitance can be thought of, if one simply sees the decrease of the absorber, as reducing the required electron/hole path length (to the back contact), or an increase in the doping concentration of the layer. However, as a result of the now reduced absorption volume, the ultra thin CdTe devices are expected to have a lower value of J_{sc} , as well as a higher value of J_0 [41]. J_0 is seen generally as an indicator of high recombination, and is usually attributed to insufficient p-type doping at the back contact. The observed

higher dark recombination for the thinner absorber devices (Fig 4.23) agrees with this observation.

4.7.7 Spectral response of ultra thin CdS/CdTe

If we consider the QE curve with illumination from the glass side, the light will pass first through the glass, then ITO, followed by CdS, and finally CdTe. The shape of the curve is similar to the shape obtained for thicker cells (Fig 4.25), with losses at 400–500nm due to CdS absorption. Figure 5.13 shows the quantum efficiency of a series of ultra thin absorber devices. The rounded shape of the QE in the region from 520 to 590 nm is characteristic of the formation of the S-rich alloy CdS_xTe_{1-x} [38].

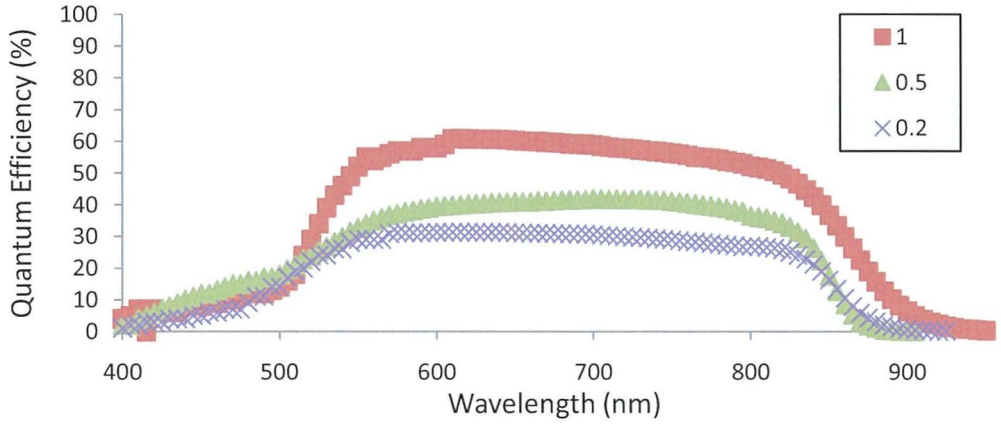


Figure 4.25: Spectral response of ultra thin CdS/CdTe devices.

All ultra thin CdS/CdTe devices show relatively high absorption in the blue region (500-550 nm), due to CdS. For thinner absorber devices, there is a decrease in the "top-hat" performance (from 550 to 850 nm) due to a lack of complete absorption of these photons. Since most of the photons are absorbed near the back contact, away from the junction and in a region where the electric field is weaker, an increased sensitivity to back surface recombination could be present for thinner absorber layers.

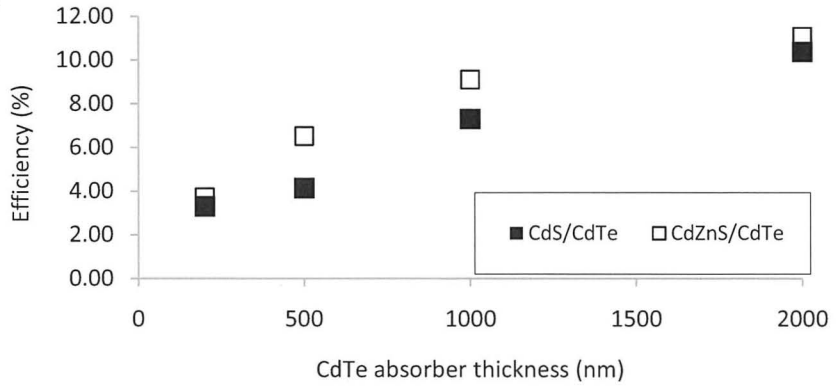
For the 0.5 μm device, a slight increase in the QE is observed throughout the "top-hat", with a peak at 730 nm. This suggests that GB passivation is high throughout the CdTe thickness, and especially at the back contact region (800-900 nm). As the proximity of the back contact to *pn* junction comes closer, it could become an issue.

It also appears that there is more inter-diffusion occurring for the ultra thin layers, as there is higher QE in the sub-500nm range, which could be occurring due to the un-optimized Cl treatment, being overly aggressive for the thinner layers, increasing inter-diffusion [29, 30].

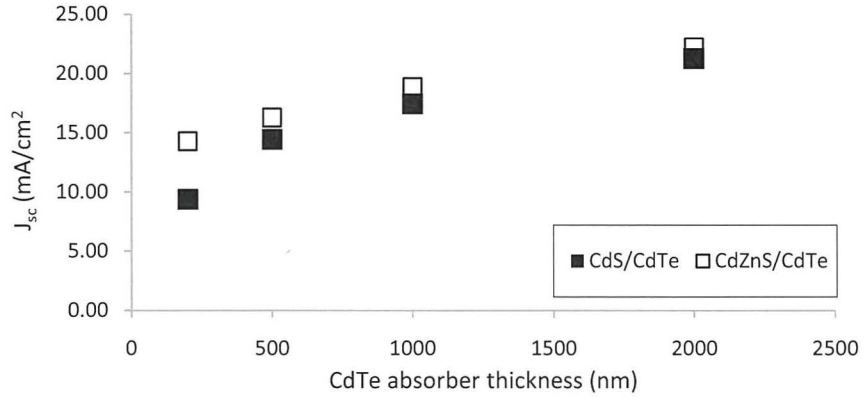
4.7.8 Ultra-thin CdZnS/CdTe device results

The device results of ultra-thin absorbers, combined with wider band gap (CdZnS) window layer have been plotted with those CdS/CdTe devices for comparison (Fig 4.26).

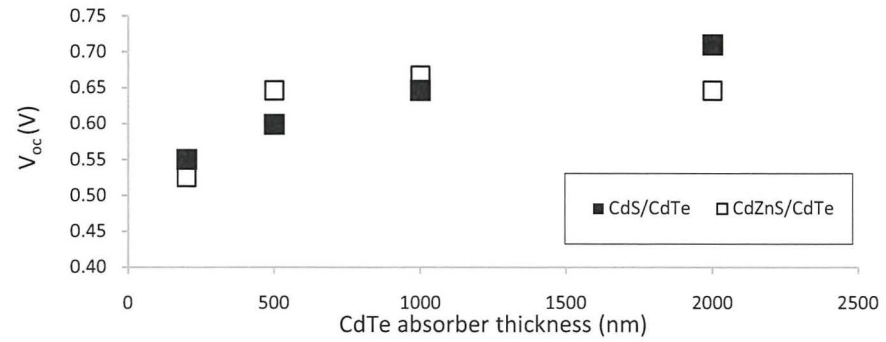
a)



b)



c)



d)

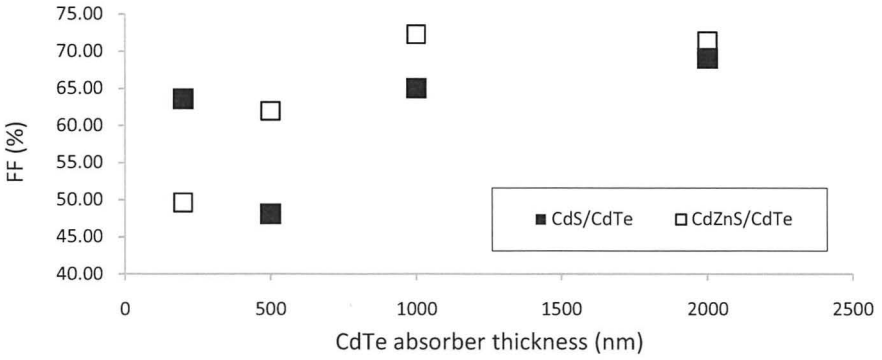


Figure 4.26: Device parameters as a function of absorber thickness, for CdS/CdTe and CdZnS/CdTe devices.

The efficiency of the CdZnS/CdTe devices seemed to improve compared with CdS/CdTe devices. The J_{sc} values indicate that an increased photo-response is observed for the CdZnS/CdTe, which is to be expected, as less absorption occurs for CdZnS.

Fig 5.14 b) shows a decreasing trend of J_{sc} with absorber thickness. A large drop in J_{sc} is observed for the thinnest device (0.2 μm). One should consider that for ultra thin devices (<1 μm), a larger proportion of the absorbed photons will be of higher energy (< 500 nm), as longer wavelength photons will not be absorbed as the absorption edge is too low. This could explain the larger drop for the thinnest baseline CdS/CdTe device.

A general decreasing trend is observed with the V_{oc} graph, with decreasing absorber thickness, possibly on the account of shunting because of weak diodes and non-uniformity [42]. Results here are similar to those in Fig 2.16, by Amin *et al.* [33], showing a general downwards trend of device parameters with absorber thickness.

No increase in V_{oc} is observed at ultra thin thicknesses (< 0.5 µm), and suggests that no favourable interaction between the back contact and the *pn* junction occurs, which could suggest a presence of a BSF.

The comparison of the CdS/CdTe and CdZnS/CdTe devices allows the effect of increased number of photons (and % of higher energy photons) to be investigated. Since no trend(s) are observed with (Fig 5.14 c, 5.14 d) concentration will be focused on Figures 5.14 a) & b). Fig 5.14 b) shows that improvement in J_{sc} due to optical effects is possible with the inclusion of the wider band gap window layer. However, the improvement in the relative J_{sc} for 0.2 µm devices, is counter acted by a decrease in the V_{oc} and FF of the device (due to shunting), resulting in no improvement in efficiency. Thus, it can be said, that ultra thin CdTe devices are not photo-limited (i.e. not limited by the photon flux hitting the device), but most probably limited by increased recombination at the CdZnS/CdTe interface.

In order to investigate the improved "blue-region" of the device, quantum efficiency analysis has been carried out (Fig 4.27).

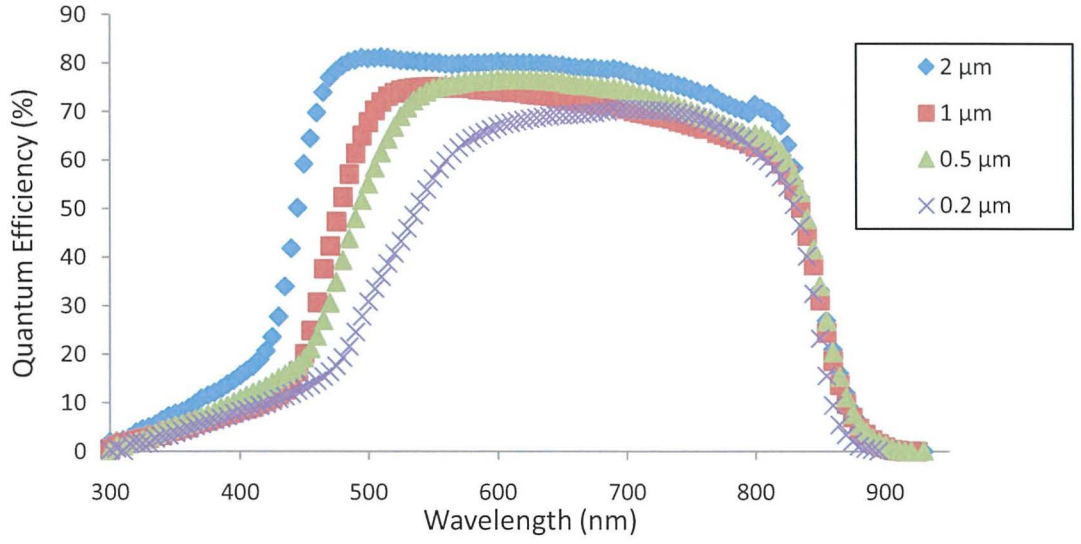


Figure 4.27: Quantum efficiency spectra of CdZnS/CdTe ultra thin devices.

4.7.9 Photon recycling using a back surface reflector

A back reflector type structure has been suggested by several authors [33, 38], where a glass/ITO/CdS/CdTe/ZnTe/Ag type configuration is discussed. This optimized structure would allow the reflection of photons which reach the back contact, and possibly be re-injected back into the device. Gupta *et al.* [38] conclude that there should be no fundamental limit to reducing the CdTe thickness to as little at ~0.75 μm in high efficiency CdTe-based cells. The use of a back reflector could reduce the required CdTe further.

Firstly it is worth investigating if any light is transmitted or currently unutilized by the device. A (Cary 5000 Varian Inc.) spectrophotometer was used to measure the transmission spectra through ultra-thin devices. The transmission spectra (Fig 4.28) of a series of absorber thicknesses, here light shone through the glass/ITO is set as the reference, so as to only measure the transmission of the CdZnS/CdTe film itself.

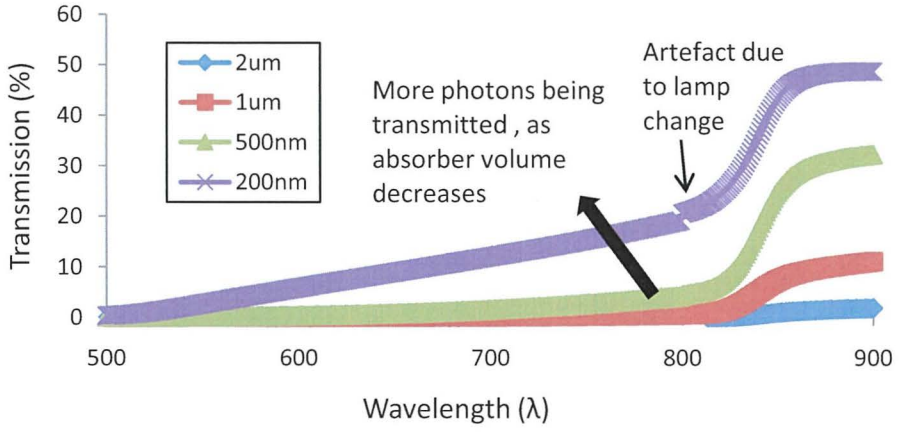


Figure 4.28: Transmission spectra of various ultra thin CdZnS/CdTe devices covering the active spectral range of these devices.

In order to test if any photons could be re-cycled and reflected back into the device, a thin film of Al was evaporated (using a metal evaporator) onto a large microscope slide, which was placed directly at the back contact of the ultra thin absorber devices for reflection analysis using an ocean optics spectrometer (Fig 4.29).

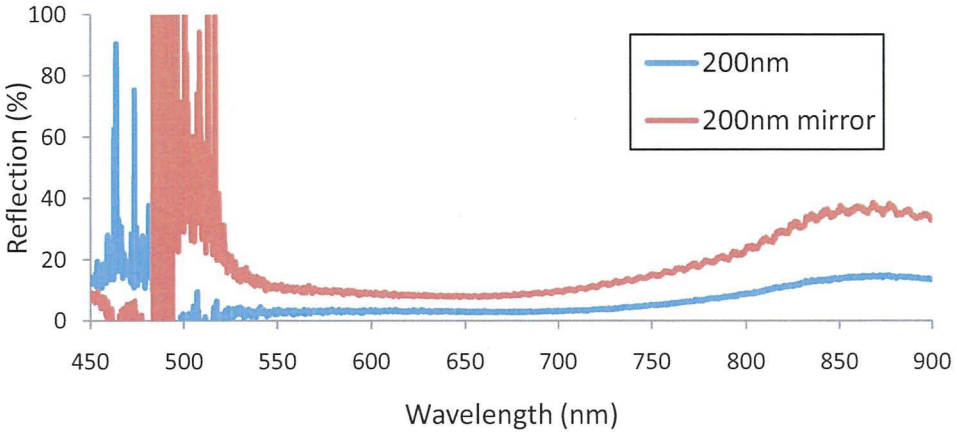


Figure 4.29: Reflection spectra for a 200nm thick absorber device.

It is can be seen that it is possible to reflect the photons which have not been completely absorbed by the CdTe layer in the first pass, similar but smaller relative increases in Al mirror reflection were seen with the 0.68 μm and 1 μm thick CdTe devices.

The next step was to devise the best strategy for including the Al coating onto the CdTe back contact. As the device itself needed to be measured, gold contact would be needed as the work function of Al (4.06-4.26 eV) is too low to form a good Ohmic back contact [43].

The result (Fig 4.29) shows that if a reliable back reflector could be employed, unabsorbed / and currently transmitted photons can be reflected into the device, towards the junction, increasing the probability of it being absorbed.

4.8 Preliminary Bi-facial Analysis (Using I-V)

Bi-facial analysis, is the illumination of the device from both sides, allowing light to reach the *pn* junction without having to travel (and not be limited by absorption losses) through the window layer. This allows the possible separation of window layer losses with device performance, and allows the separation of *pn* junction and back contact effects (Fig 4.30).

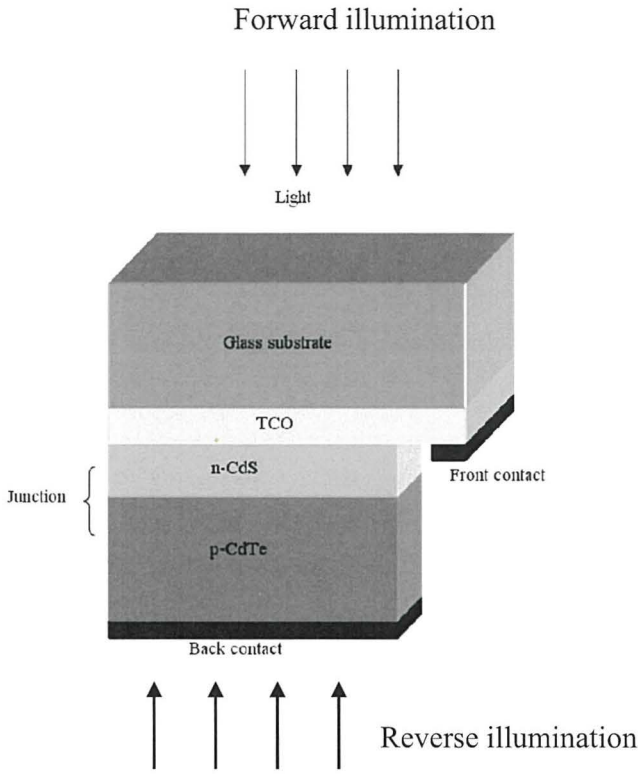


Figure 4.30: Diagram of a CdS/CdTe based solar cell, showing how a bi-facial analysis would be done.

Preliminary bi-facial results of 1 μm thick MOCVD grown CdS/CdTe (Table 5.6), showed that without any change in device structure, PV response could be obtained from illumination from both sides of the device. This shows that to a degree, the gold contact itself is semi-transparent. Ideally one would use a near transparent back contact (e.g. ZnTe) to increase the light transmission from the back.

Table 4.9: Bi-facial I-V results for an ultra thin (1 μm CdTe) CdS/CdTe device.

Device parameter	Forward illumination	Reverse illumination
Efficiency (%)	7.7	1.4
FF (%)	69.8	72
J_{sc} (mA/cm^2)	17.5	3.4
V_{oc} (V)	0.63	0.58

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CHAPTER 5 - DISCUSSION

5.0 $CdCl_2$ treatment

It should be mentioned that the relatively high observed values for J_{sc} (maximum achievable for CdTe ~30.5 mA/cm^2), is almost certainly due to the Halogen lamp, here overestimating the J_{sc} contribution of the cells. Nonetheless, adequate information is obtained which is useful as a direct sample to sample comparison for this series of experiments towards obtaining an optimum $CdCl_2$ thickness.

Interestingly, (Fig 4.8) shows that the V_{oc} remains unchanged for over-treated $CdCl_2$ devices, as an increase in recombination centres could be expected. Incident photon to current efficiency (IPCE) analysis was carried out by Dr Anura Samantilleke at the University of Bath. This allowed the measurement of devices without applying a back contact structure, as the electrolyte material used during the measurement served this purpose. Two devices were analysed, one where a higher TDMAAs doping setting (1.2×10^{-6} atm / $2x10^{19}$ atoms.cm^{-3}) (Fig 5.1 a), and one with a lower TDMAAs setting (3×10^{-7} atm / $2x10^{8}$ atoms. cm^{-3}) (Fig 5.1 b). Device parameters: 2 μm CdTe absorber, 0.24 μm CdS), both devices were treated with the same $CdCl_2$ treatment (~100 nm).

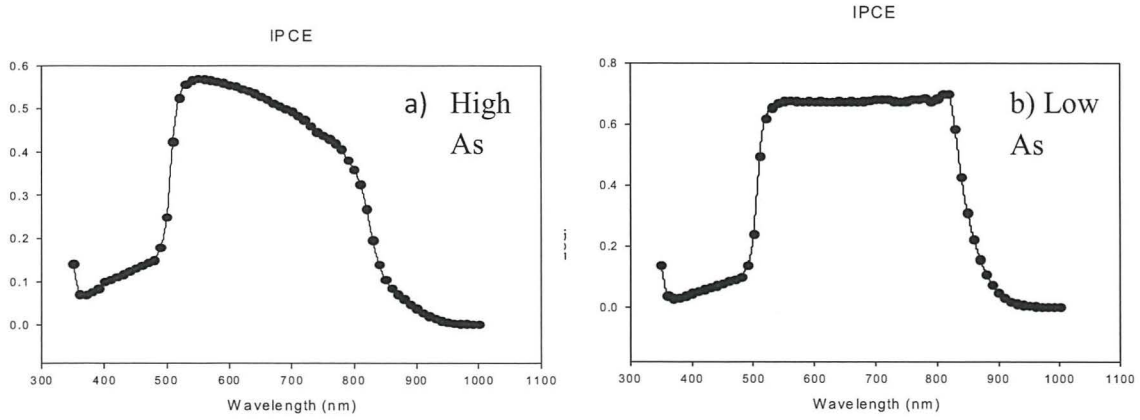

Figure 5.1: IPCE vs λ of a CdS/CdTe baseline device with a) high (1.2×10^{-6} atm / $2x10^{19}$ atoms.cm^{-3}) TDMAAs doping and b) low (3×10^{-7} atm / $2x10^{8}$ atoms. cm^{-3}) TDMAAs doping.

The IPCE spectrums also show that due to the large CdS thickness, a large portion of the high energy photons <500 nm are not transmitted to the CdTe. The observed drop in the IPCE spectrum at > 500 nm to 800 nm suggests that the higher level of arsenic doping does not effectively passivate the grain boundaries, and could suggest a mechanism where dopant compensation with the Cl [1] is possible.

Fig. 5.1 (b) shows the IPCE of a CdTe device, where the level of As doping has been decreased (3×10^{-7} atm / $2x10^{8}$ atoms. cm^{-3}). An improvement in the top level, with no drop in the IPCE for wavelengths > 500 nm is seen. A small sub-band gap response has also been observed at approximately 900 nm by Batzner *et al.* [2], where it is suggested it could be due to a back contact junction influence or other defect related features.

Zunger [3] recently presented some work towards understanding doping bottlenecks in various semiconducting materials, and has put forward seven rules one should follow. The relevant rule regarding p-type doping, states that *p*-type doping is facilitated by materials whose valance band maximum is close to the vacuum level, i.e., small bulk-intrinsic ionization potential. Conversely, *p*-type doping tends to be compensated in materials with large bulk-intrinsic ionization energies. Zunger [3] states that this proposed rule, reflects the ease of *p*-type doping of antimonides and tellurides (small bulk-intrinsic ionization potential (Φ), and the difficulty in *p*-type doping of the more electronegative oxides and sulphides (large Φ).

Early work using arsenic doping with MOCVD was carried out by Chu *et al.* [4], and reported achieving carrier concentrations between (10^{15}- 2×10^{16} cm^{-3}). Chu *et al.* [4] also notes that the incorporation of arsenic is highly ineffective compared with gallium (doping), since AsH_3 is thermally unstable, and comments on the potential for the arsenic atoms to be electrically inactive owing to self-compensation and defect formation(e.g. As at a Te vacancy – to form an acceptor defect). Complex defect relationship can also come about simply from the $CdCl_2$ process. The Cl replaces Te and becomes a shallow donor (becoming positively charged), this positively charged species open to form a complex with a doubly charged vacancy C_{cd}^{2-} which can then act as a single acceptor defect.

The $CdCl_2$ treatment (carried out at 200 °C) is currently thought to passivate the grain boundaries, facilitating a change in the appearance of the CdTe surface (Fig. 5.2) before (a) and after (b) $CdCl_2$ treatment has also been observed.

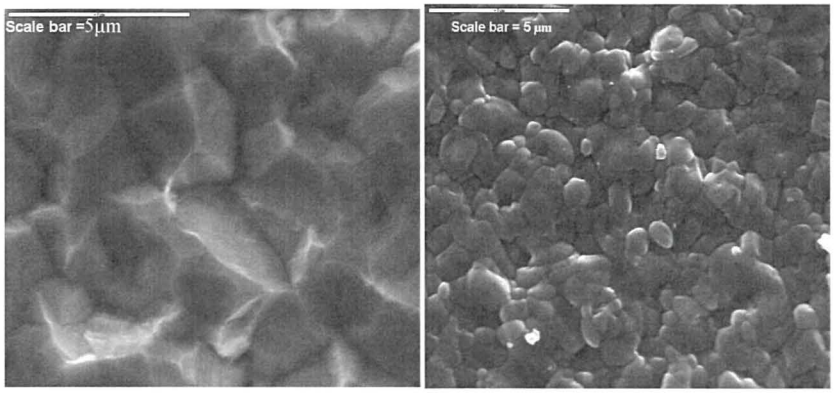

Figure 5.2: SEM images of CdTe **a)** (Left) before and **b)** (Right) after $CdCl_2$ deposition

The appearance of the CdTe surface (Fig 5.2 a) itself is left changed as a result of the $CdCl_2$ treatment. Small rounded features are clearly observed (Fig 5.2 b). The grains are more defined after treatment, and may have coalesced.

An increase in the average grain size of the CdTe has been reported with other methods after $CdCl_2$ treatment (e.g. vacuum evaporation [5]). But, it is unclear if any grains (near the surface) increase in size, as identifying individual grains after annealing is difficult (using surface methods SEM, AFM). Grain size determination using XRD, due to the inherent strain in the films; also make it difficult to gain accurate determinations of grain size. However, there are contradictory reports [6, 7], indicating substantial improvement of efficiency without observing any grain size improvements. Table 5.1 shows device result of a device with and without the $CdCl_2$ treatment.

Table 5.1: I–V characteristics of MOCVD photovoltaic CdTe solar cells (As 2 x 10^{18} atoms.cm^3), i) no $CdCl_2$ treatment and ii)after the $CdCl_2$ treatment.

Cell Structure	Contact area (mm^2)	η (%)	FF (%)	J_{sc} (mA cm^{-2})	V_{oc} (mV)
i)CdS/CdTe:As	2.5	3	47.5	12.1	510
ii)CdS/CdTe:As/$CdCl_2$	2.5	7.4	51.8	23.9	600

After the $CdCl_2$ treatment an increase in the V_{oc} and FF device parameters are observed (Table 5.1). The clear benefit of the $CdCl_2$ is clearly seen, improving device efficiency, through large improvements in J_{sc} and V_{oc}.

The current hypothesis is that for MOCVD grown CdS/CdTe solar cells, the *in situ* $CdCl_2$ treatment appears to effectively passivate the grain boundaries, while the As species segregates to the CdTe grains themselves, acting as a dopant [8].

5.1 Open circuit voltage

The V_{oc} of MOCVD devices are typically lower (< 700 mV) than films deposited via CSS (typically > 700 mV). The use of a (ZnO) buffer layer [9] as an insulating layer between the transparent conducting layer (TCO) and the window layer, was investigated to improve potential losses in this region. The addition of the ZnO insulating layer "i-layer" adds a physical barrier decreasing the probability of pinhole related problems as the absorber layer thickness is reduced.

Towards increasing the sensitivity in this region; ultra thin (1 μm) devices were employed. All devices mentioned in this section have the same structure, CdS (0.24 μm)/CdTe(1 μm):As (1700 sccm / 2 x 10^{18} atoms). Table 5.2 shows results of adding the i-layer to 1 μm thick absorber layer devices. A large increase in the conversion efficiency is observed, along with improvements in FF, J_{sc} and smaller improvements in V_{oc}.

Table 5.2 Devices results of ultra thin CdS/CdTe devices i) no i-layer ii) with the i layer.*Devices here have been etched for 5 seconds in a 0.25% Bromine/methanol solution prior to contacting.

Device Structure	Eff (%)	FF (%)	J_{sc} (mA/cm^2)	V_{oc} (mV) +/- 5
a) Glass/ITO/CdS/CdTe:As/$CdCl_2$*	6.5	50.5	22.5	580
b) Glass/ITO/ZnO/CdS/CdTe:As/$CdCl_2$*	8.3	57.8	23.7	600

C-V analysis carried out on MOCVD grown devices with the inclusion of the I-layer by Y. Proskuryakov *et al.* [10] propose that the ZnO layer depletes the CdS fully (an electric field effect). Thus, it can be assumed that the inclusion of the ZnO layer itself allows good transmission of blue light to the junction region while fully depleting the junction (CdS/CdTe) area, improving device voltage.

5.2 Ultra-thin n-type CdS window layer

The ability of MOCVD to produce accurate layer thicknesses has allowed very thin CdS window layers to be grown. Table 5.3, shows the results of a series of devices, where the CdS window layer thickness was reduced down to 50 nm. The highly resistive ZnO passivation layer was included for comparison for both CdS thicknesses. Results show that the V_{oc} of the device do improve as a result of the inclusion of the ZnO layer, but when the CdS thickness is reduced further to 50 nm, the addition of the ZnO barrier layer seems to worsen the device results, possibly on the account of increasing the depletion of the CdS layer.

Table 5.3: Device results of CdS/CdTe devices where the CdS window layer has been decreased in thickness. *All CdTe thickness was 1 μm.

CdS window layer thickness (nm)*	High resistivity i-ZnO layer	Efficiency (%)	J_{sc} (mA/cm^2)	V_{oc}(V)	FF (%)
50	No	7.8	21.7	0.59	61.2
50	Yes	6.3	16.9	0.65	57.8

The relatively high device efficiencies tend to suggest that some sort of photo-active junction is possible. Whether a standard *pn* junction, or a more complicated MIS type structure (M – ITO, I – CdS, S – CdTe) is present is not yet understood. One could consider that if the hole depletion width is nearly analogous as the CdS thickness, the absorbed photons could potentially contribute to the pn junction, and would explain why CdS layers so thin in working devices is possible. The spectral response of the ultra thin window layer (50 nm) has been investigated and is compared to that of a standard baseline device (240 nm), Fig 5.3.

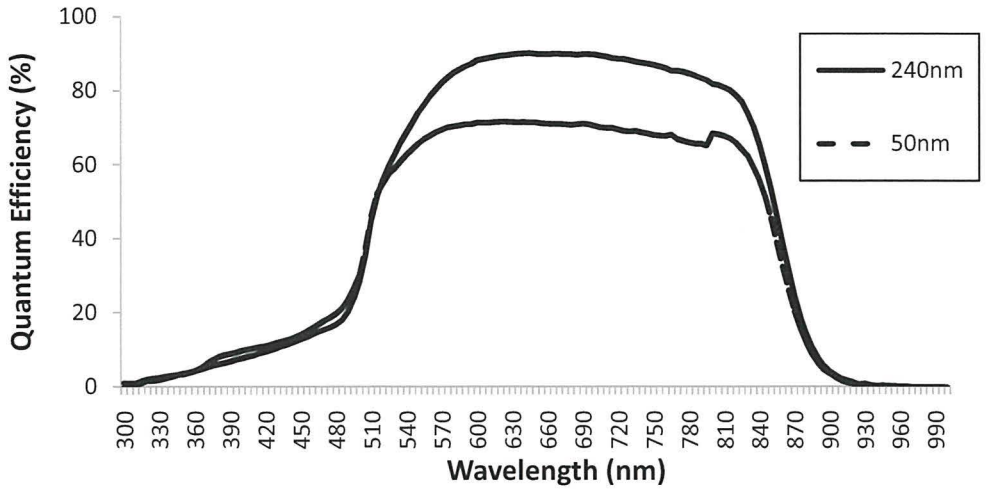

Figure 5.3: Quantum efficiency measurements of CdS/CdTe device with differing window layer thickness.

Unlike the calculated results from the modelling software (Fig 5.3), the decrease in absorption in the higher energy region (<500 nm) is not observed. Albin *et al.* [11] also reduced the thickness of the CdS layer, in order to maximise the maximum J_{sc} in their devices. Although initial performance could be improved by using thinner CdS layers (down to 60 nm), device stability was seriously impacted by an observed increase in shunting currents. Figure 4.19 shows that the ratio of QE changes, for wavelengths > 500 nm, the thicker 240 nm CdS device performs better, giving an improved "top hat" response.

In order to investigate shunting in MOCVD devices, a series of devices was grown where only the window layer thickness was changed. Devices have been made with and without the inclusion of the ZnO "i-layer", to monitor its effect as the window layer thickness is decreased. Results are summarized in Table 5.4.

Table 5.4: Shunting and series resistance values, of devices with differing CdS window layer thicknesses. Note: All CdTe absorber thickness here is 1 µm.* It should be noted, that it is expected that during the annealing step, a finite thickness of CdS may be consumed by the CdTe layer.

i-layer	*CdS Window layer thickness (nm)	Shunt Resistance (R_{shunt}) Ω	Series resistance (Rs) Ω ·cm^2
No	240	1062	2.3
Yes	240	2083	2.4
No	120	854	2.7
Yes	120	2227	2.2
No	50	253	2.1
Yes	50	393	1.7

The inclusion of the ZnO i-layer to all devices, improved the shunt current response, with smallest effect for the ultra thin (50 nm) window layer, leaving R_s relatively unchanged. A significant change in the shunting is only observed when the CdS window layer is decreased to 50 nm, giving a lower (worse) shunt current, and demonstrates a poor quality *pn* junction, only slightly improved by the inclusion of the ZnO i-layer, possibly acting as an extension of the window layer.

5.2.1 Effect of the ZnO insulating layer (for CdZnS/CdTe devices)

Two $Cd_{1-0.1}Zn_{0.1}S$/CdTe baseline devices were grown (Table 5.5), one included the ZnO "i-layer" (Device 2), and one did not (Device 1).

Table 5.5: Device results of the effect of ZnO insulating layer on the wider band gap window layer devices. *All devices have a CdZnS window layer (0.24 μm), and CdTe absorber (1 μm)

	Insulating (ZnO) layer	Efficiency (%) (+/- 0.3)	J_{sc} (mA/cm^{-2}) (+/- 0.3)	FF (%) (+/- 0.3)	V_{oc} (mV) (+/- 20)	BCL layer
Device 1	No	11.4	20.6	74.1	750	Yes
Device 2	Yes	10.2	19.9	69.2	740	Yes

Unlike baseline CdS/CdTe devices, where the inclusion of the ZnO interface layer improves device performance, the opposite is true for wider band gap layer devices. This could be due to the ZnO layer, as it is expected to fully deplete the window layer [10]. Major *et al.* [10] also comments that an increased doping level, can also have a passivating effect on charged states similar to that of a ZnO layer. This could affect the ability of the i-layer to fully deplete the window CdZnS layer.

Wu [12] also investigated the effects of ZnO inclusion in his CdTe devices. Improvements in R_{shunt}, have been reported and attributed to the high resistivity of the "i-layer".

5.3 Back contact layer (BCL)

The back contact of CdTe solar cells has long been a challenge, as even a noble metal with a very high work function (Φ_m), such as gold, results in an IV curve with rollover behaviour, due to the metal/CdTe Schottky junction. As no common metals have Φ_m high enough (5.9-6.0 eV) [13] for an ohmic contact with CdTe, two main approaches have been pursued so far;

1. Increasing the p-type doping at the back to make a thin p+ layer, enabling the majority carriers to tunnel through the Schottky barrier (and lower surface carrier recombination);

2. Reduce the band gap energy (E_g) at the back contact, by depositing an intermediate layer, so that the barrier is effectively reduced.

Other approaches have included the use of, ZnTe, despite not being a narrower band gap (2.4 eV) material. However, as it can be doped p-type by either Cu [14] or Ni [15], it is able to make an ohmic contact with noble metals.

CdTe is known to be a self-compensating material, which is difficult to dope at high active acceptor concentrations. The approach suggested by Barrioz *et al.* [8] uses the same dopant as in the absorber itself, to try and create a npp$^+$ type structure. The shallow acceptor, arsenic, has been shown to be successful for MOCVD based CdTe devices [16]. SIMS profiles have revealed that incorporation of arsenic within the CdTe matrix was controllable and able to reach values up to 1.5×10^{19} atoms·cm^{-3}, by *in situ* doping using MOCVD.

Barrioz *et al.* [17] identified the optimum BCL thickness (250 nm) for standard 2 µm thick baseline devices, giving the highest V_{oc} value. Capacitance-Voltage (CV) profiling was used to measure the TDMAAs doping concentration. It was found that the measured acceptor concentration 7×10^{13} atoms.cm^3, was less than the TDMAAs concentration used during growth (3×10^{-7} atm / 2×10^{18} atoms.cm^3). The TDMAAs concentration in the final device is 3-4 orders of magnitude less than that used during growth, and could be evidence of As segregation, from the grains to the grain boundaries (GB).

The series resistance was calculated from the slope of the IV curves (Fig 5.4), at high applied voltage e.g. 0.7-1 V, until the breakdown of the linear portion of the curve). Calculated values of R_s for devices with and without the doped layer/BCL, were ~10 $\Omega \cdot cm^2$ for the standard Br/MeOH etched devices and ~2 $\Omega \cdot cm^2$ for the devices which had the BCL). The decrease in R_s could be ascribed to tunnelling, but for the thicknesses used (250 nm), and the relatively low measured doping concentrations (7×10^{13} atoms.cm^3), it is very difficult to ascertain. Barrioz *et al.* [8] have suggested the presence of a $AsTe_2$ layer at the CdTe surface, but obtaining XRD data remains difficult as exposure to air, upon opening of the growth reactor, immediately alters any $AsTe_2$ layer present.

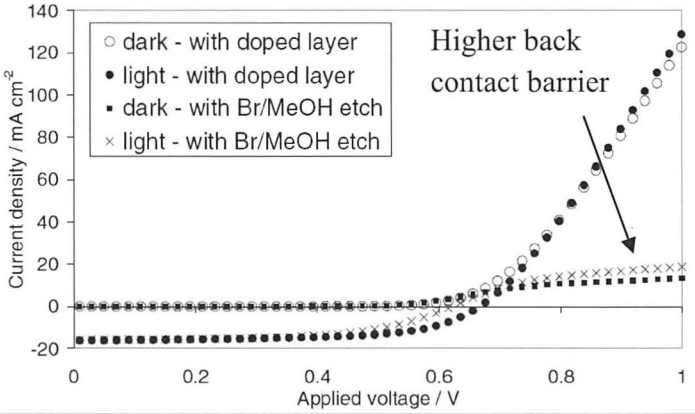

Figure 5.4: I-V curves baseline CdS/CdTe:TDMAAs device with a BCL (black, R_s 2 Ω cm^2) and without a BCL (grey, R_s 10 Ω cm^2).

No roll-over is observed for baseline devices with the BCL doped layer, while a $q\Phi_b$ of 0.38 eV is observed for the non BCL devices. The low series resistance of ~ 2 $\Omega \cdot cm^2$ for both dark and light I-V measurements (for the BCL device) indicate a high diffusion hole current with very little dependence on illumination.

Using the two-diode equivalent circuit model developed by Niemegeers and Burgelman [18], the back contact barrier heights ($q\Phi_b$) can be estimated. A MOCVD grown CdS/CdTe device (with no BCL, which was Br/MeOH etched) was deposited and used to estimate the contact barrier height. The barrier height (the difference between the equilibrium Fermi level and the top of the valence band at the metal surface) was found to be 0.38 eV, giving a back contact saturation current density (J_{sc}) of 8.3 mA$\cdot$cm^2. However, the same analysis for the cells with the doped contact layer, for which there was no I-V rollover, indicated that in such samples there was no apparent barrier present at 25 °C.

5.4 $CdCl_2$ deposition temperature

Results (Fig 5.5) show that $CdCl_2$ grown at 200 °C, followed by a 10 min anneal at 420 °C is the optimum. It showed that the important factors which were sensitive to efficiency were (in order of importance) As doping > Anneal temp > $CdCl_2$ temp > Anneal Time. The following growth was done to check the outcomes from Taguchi matrix, and involved altering the $CdCl_2$ deposition temperature and anneal time. This series included the optimized BCL at the back contact.

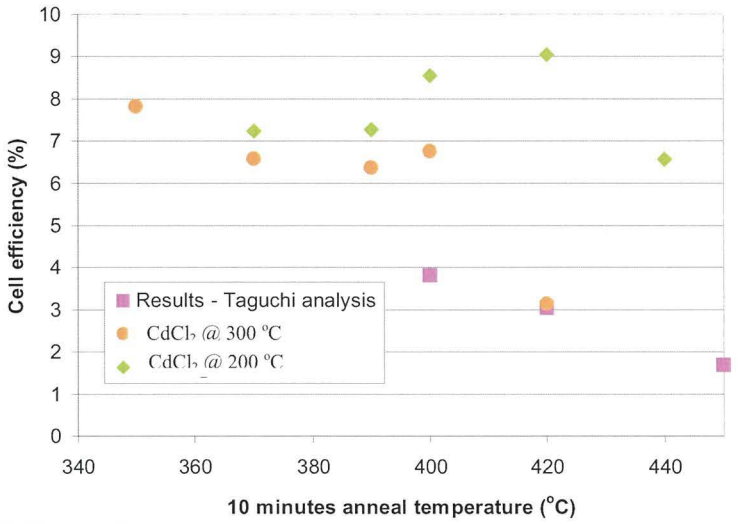

Figure 5.5: Study of $CdCl_2$ treatment on MOCVD CdS/CdTe:As/CdTe:As^+ structures

The $CdCl_2$ treatment has been optimized, using a CdS/CdTe:As/CdTe:As^+ structure, resulting in a repeatable 30% (+/- 3) increase in device efficiency after its addition.

5.5 Baseline CdS/CdTe device

Cross-over of light /dark IV was observed in almost all devices produced. Fisher *et al.* [19] also report I-V cross-over in their devices, and attributes it to the excessive Cu doping of their CdS. However Fisher *et al.* [19] do conclude that the observed crossover does not affect the photovoltaic behaviour of the final device. Figure 5.6 shows the cross-over behaviour observed in devices (CdS/CdTe baseline) grown by MOCVD.

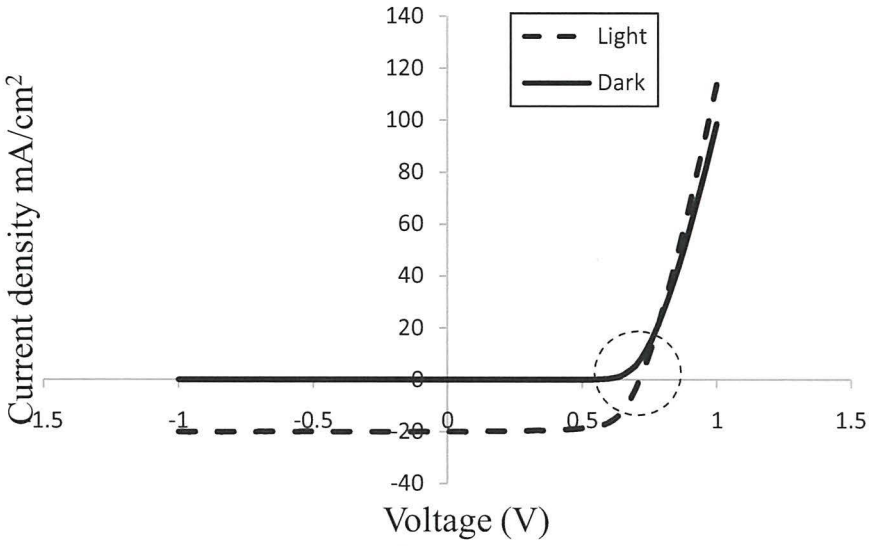

Figure 5.6: A typical light/dark crossover I-V curve, of a baseline CdS/CdTe device.

Niemeegers *et al.* [20] have put forward a theory that cross-over in I-V curves. It has been proposed that the cross-over behaviours occurs as a result of the surface recombination current of electrons at the metal surface. Transport through the Au/CdTe back contact is limited by drift and diffusion.

The presence of a Schottky barrier causes roll-over of the *IV* curves. However, due to the BCL, the roll-over behaviour is negated, and does not explain the continued presence of the cross-over. The presence of a minority carrier (electron) current could possibly be present at the CdTe back contact, giving rise to "cross-over" of the I-V curves, but has not been investigated. Niemegers states that red illumination and thinner cells (< 5 μm) [21] favour cross-over given their larger electron diffusion length [22].

5.5.1 Light Soaking of baseline CdS/CdTe

Light soaking was achieved using AM1.5 light (with constant temperature 30 °C) for 10 min. It is typically thought to fill in traps (or recombination centres [23], present in the CdTe) which have the potential to limit device efficiency. Table 5.6 reports the results of 2 μm thick baseline device, which has been light soaked and measured at recorded intervals. An optimum light soaking duration of 10 min was used at room temperature.

Table 5.6: Results of 2 μm thick CdS/CdTe baseline device which has been light soaked for 10 min.

Efficiency (%) (+/- 0.3%)	Efficiency (%) after light soak	Time after contacted (hrs)	% increase of light soaked Efficiency
9.6	10.3	0	6.55
10.0	10.1	24	0.70
10.7	11.1	48	3.17
8.5	8.9	312	4.11
10.7	10.8	360	1.41
9.9	10.0	552	0.50

*Also shown is soaked and un-soaked efficiencies measured at varying times after the back contact has been applied to monitor any degradation. The reported results are the average of three contacts.

The results seen here are similar to that reported by Romeo *et al.* [23]. Romeo *et al.* [23] observed that when their Cu containing CdTe solar cells were light soaked (1 sun illumination and a raised temperature of 80 ^{o}C, for >2 days in open circuit conditions), their performance also improving by 5% from 9.5% to 10%. But the marked improvement, in such a short time (10 min) with MOCVD devices, could suggest that a relatively lower concentration of traps exist, which are filled up nearly instantly. However, as our devices are annealed (to effectively distribute the Cl to the GB), useful comparison with non-annealed MOCVD devices has not been possible, as efficiencies obtained were very low. Romeo *et al.* [23] justified the large initial improvements after light soaking, by suggesting that the defects at the junction between the ITO and the CdS are more in the as-deposited case (for their devices) and thus light soaking fills the recombination centres at the junction, giving a larger increase after soaking.

5.5.2 Current transport mechanism

Ercelebi et al. states that, evidence of having multi-step tunnelling-recombination mechanism is the linear relation between L_n I_o versus T [24] as illustrated in Fig 3.21. The multi-step tunnelling-recombination mechanism model was proposed by Riben and Feucht in 1966 [25]. The model states that, holes tunnel from the valence band of p-side to the close localised states in the forbidden gap, and then they keep tunnelling among these states in a staircase path until they reach the valence band (Fig 4.13 b).

How the devices behave under illumination will now be investigated. Using Eqn. (4.6), If one plots the V_{oc} against T (straight line), the intercept (T=0) should yield the built-in potential V_{bi}) which is described as an upper limit to the V_{oc} of the cell under illumination.

$$V_{oc} \approx \frac{E_a}{q} - \frac{nkT}{q} \ln\left(\frac{J\infty}{J_L}\right) \qquad 5.1$$

Where J_∞ is the saturation current density prefactor.

Equation 5.1 implies that plotting V_{oc} against T should give a straight line. The intercept of the straight line, as shown in Fig 5.8, to T=0 gives the built-in potential V_{bi}.

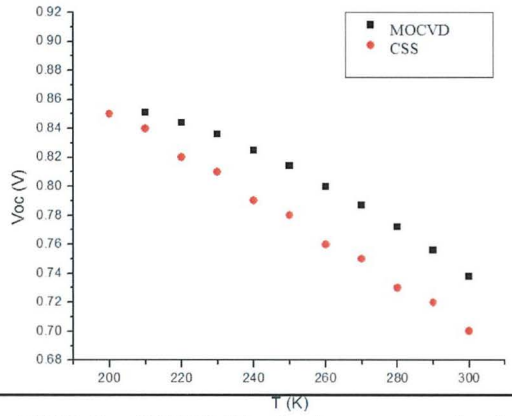

Figure 5.8: V_{oc} vs T(K) for CdS/CdTe devices grown by MOCVD and CSS.

Using Fig 5.8, V_{bi} was calculated to be 1.15 V for MOCVD CdS/CdTe and 1.26 V for CSS CdS/CdTe devices respectively. It is observed that some deviation from linearity below 230 K as the lower temperature limit is typically determined by the ionization energy of the dopants. Dopants usually require some energy to ionize and produce carriers in the semiconductor. This energy is usually thermal, and if the temperature is too low, the dopants will not be sufficiently ionized and there will be insufficient carriers to adequately increase the number of charge carriers.

Our I-V-T analysis, is similar to the work carried out by Bayhan *et al.* [26], where I-V-T of CdS/CdTe cells grown by vacuum deposition have been analyzed. Bayhan *et al. [26]* observed that a low activation energy (of about 0.77 eV, or ½ the CdTe band gap), indicated that the V_{oc} was dominated by recombination (at the CdS/CdTe interface), rather than recombination in the bulk of the absorber.

However, in MOCVD grown devices, such low values of E_a, have not been observed, and could suggest that recombination at the interface does not limit the V_{oc} in our 2 μm baseline CdS/CdTe devices.

Thus, it can be concluded that the forward current under light for all the samples is governed by *Shockley-Read-Hall* (SRH) process. Moreover, the reverse dark mechanism for both baseline samples is identified as tunnelling. SRH and tunnelling processes require high density of localised defect levels, which can result from the mismatch between CdTe and window layers which can be enhanced by the different thermal expansion coefficients of CdTe and CdS.

The barrier height (using AM1.5 illuminated I-V curves) of the junction can be evaluated by plotting V_{oc} versus T (Eqn. (5.1) [27]; Equation 5.1 implies that plotting V_{oc} against T should give a straight line. The intercept of the straight line, as shown in Fig 5.8, to T = 0 gives the activation energy Ea .An activation energy of 1.26 eV was calculated for the CdS/CdTe MOCVD baseline.

5.5.3 Space charge width

The surface potential φ_s; is the difference (in volts) between the Fermi level (of the intrinsic carrier) E_{Fi}, measured in the bulk semiconductor, and E_F measured at the surface. The space charge width can now be written in a form similar to that of a one-sided *pn* junction (Eqn. 5.2), and assumes that the abrupt depletion approximation is valid. Using equation 5.2, the space charge width (χ_d) can be estimated.

$$\chi_d = \left(\frac{2\epsilon_s \emptyset_s}{eN_a}\right)^{\frac{1}{2}} \quad 5.2$$

Where N_a, is the acceptor doping concentration, ϵ_s is the dielectric constant for the semiconductor.

Figure 5.8, shows the energy bands for the case in which $\emptyset_s = 2\emptyset_{fp}$. The Fermi level at the surface is as far above the intrinsic level as the Fermi level is below the intrinsic level in the bulk semiconductor. The maximum space charge width possible can be calculated by (Eqn. 5.3);

$$\chi_{dT} = \left(\frac{4\epsilon_s \emptyset_{fp}}{eN_a}\right)^{\frac{1}{2}} \qquad 5.3$$

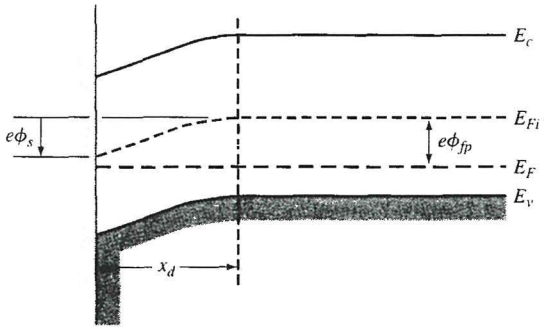

Figure 5.8: The energy-band diagram in the p-type semiconductor, indicating surface potential. After Neamen [28].

Table 5.7, shows the results of calculated depletion width for the CdS/CdTe baseline device.

Table 5.7: Estimated depletion width from C-V data for MOCVD CdTe baseline devices. For comparison the depletion width for silicon is typically around the 0.3μm region.

Device	Doping concentration (cm^{-3})	$\emptyset_{fp}$(V)	χ_d(μm)	χ_{dT}(μm)
Baseline MOCVD CdS/CdTe	10^{14}	0.37	0.22	0.29

Thus for a 2 μm device, the space charge widths is merely 0.29 μm. This means that the remaining 1.7 μm of material is not where the majority of charge separation occurs, and shows the comparatively significant region of CdTe (few hundreds of nm) close to the CdS junction is, and the role of the 'other' 1.7 μm bulk CdTe in being a region where charge carriers can simply recombine.

5.6 Increasing the numbers of photons reaching the *pn* junction

The absorption coefficients of II-VI compounds are relatively high [2], thus, the carrier generation by higher energy photons in the n-CdS layer takes place at the surface far away from the depletion region where the generated carriers can be collected.

As a result, these carriers are often lost to surface or bulk recombination current. This current increases the dark current and consequently reduces the useful current delivered by the cell to a load.

The CdS layer is required to form a hetero-junction with the CdTe layer. However, since CdS is a direct band gap semiconductor, with E_g = 2.4 eV. It strongly absorbs the majority of short-wavelength (violet to blue-green) light, before it can be usefully absorbed in the CdTe material. In a production environment it is difficult to reduce the thickness of the CdS layer due to:

i) Obtaining sufficient coverage of the rough transparent conducting oxide (TCO) layer;

ii) Uniformity issues (resulting in weak diodes) during device deposition; and

iii) Inter-diffusion of the CdS into the CdTe during a post deposition annealing step.

Two methods have been investigated in the past to reduce the parasitic absorption in the CdS layer. Firstly, the thickness of the CdS layer can be reduced and, secondly, CdS can be replaced with a higher band-gap material [29].

In CdS/CdTe cells, reducing the thickness of CdS layer [3] to less than 0.1 μm is routinely done to reduce the absorption and minimize the surface recombination current, assuming material quality is not a problem.

Modelling the expected improvement in the blue portion can be done by using SCAPS modelling software [30] (Fig 5.9).

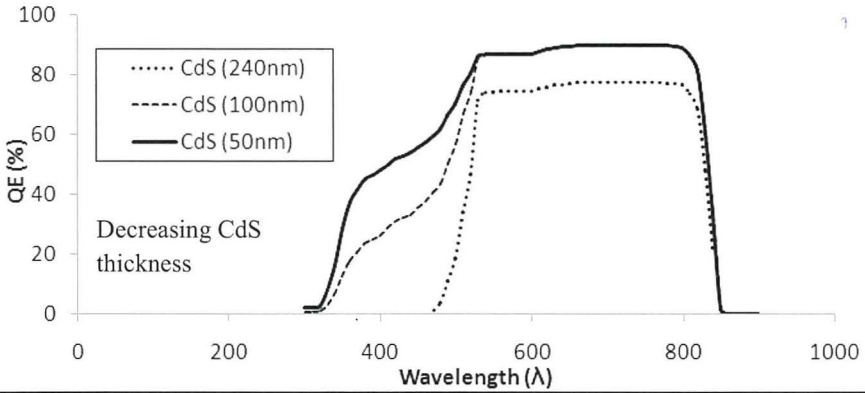

Figure 5.9: SCAPS modelled spectral response curves of thin to ultra-thin CdS window layer devices, showing increased photo activity in the blue region (300 nm-500 nm) of the spectrum.

It can be seen from Fig 5.9, that simply reducing the thickness of the CdS window layer, higher energy photons ($\lambda < 500$ nm) are no longer absorbed by the layer, and therefore are transmitted to the *pn* junction.

D. Bonnet [31] postulates that making devices with an n-type layer in the *pn* junction of only 120 nm of CdS is insufficient for a conventional *pn* junction as the layer would be fully depleted of carriers. The depletion width would be larger than the thickness of the layer itself (Table 5.7). If devices with such thin layers are grown and operate successfully, then, another junction structure must be considered.

A possible model for the junction in ultra thin (< 1 μm) absorber devices, is the Metal-Insulator-Semiconductor or MIS, where M-(ITO), I-(CdS),S-(CdTe) or MOS when a metal-silicon dioxide (SiO_2)-silicon system is used.

As one decreases the absorber thickness towards the depletion width, complications might arise, as the classical pn junction model would fail to fully explain device operation, as a point would be reached where the depletion layer would be larger than the layer thickness (if the depletion layer width remained the same).

The energy bands in the semiconductor near the oxide–semiconductor interface bend as a voltage is applied. The position of the conduction and valence bands relative to the Fermi level at the oxide–semiconductor interface is a function of the MIS voltage, so that the characteristics of the semiconductor surface can be inverted from p-type to n-type, or from n-type to p-type, by applying the proper voltage. The energy band diagram for an MIS type junction is shown (Fig 5.10).

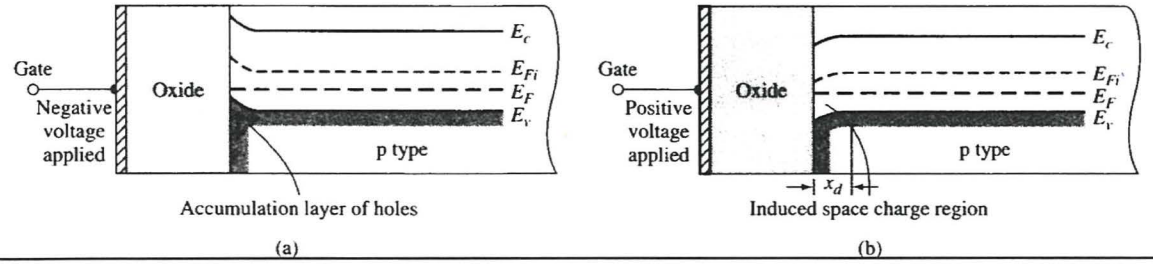

Figure 5.10: The energy-band diagram of an MIS capacitor with a p-type substrate for (a) a negative gate bias and (b) a moderate positive gate bias. After Neamen [28].

5.6.1 Extending the band gap (of the window layer)

If one looks at the AM1.5 spectral response (Fig 5.11), and calculates the available power from the CdS absorption edge at 0.5 μm to the CdTe absorption edge at ~ 0.85 μm, it is in the region of 43 mW/cm^2. However, the inclusion of a higher band gap material like CdZnS (E_g ~3.1 eV) makes an extra ~19 mW/cm^2 available for absorption in the CdTe.

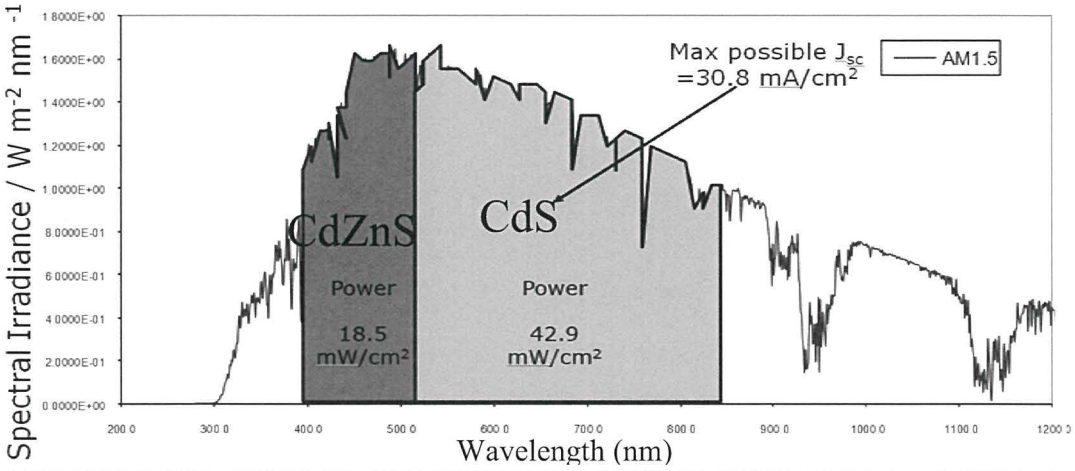

Figure 5.11: AM1.5 spectrum, showing available energies for CdS and CdZnS.

In hetero-junction solar cells using CdTe, $CuInSe_2$, and $CuGaSe_2$, the use of $Cd_{1-x}Zn_xS$ [32-34] instead of CdS can lead to an increase in photocurrent by transmitting higher energy photons to the underlying absorber layer.

Adjusting the Zn_x composition from 0 to 1, one can vary the ternary alloy (Fig 5.12) ($Cd_{1-x}Zn_xS$) band gap from 2.4 eV to 3.4 eV [2,3]. $Cd_{1-x}Zn_xS$ has also been reported in PV devices based on quaternary materials such as $CuIn_xGa_{(1-x)}Se_2$ and $CuIn(S_xSe_{(1-x)})_2$.

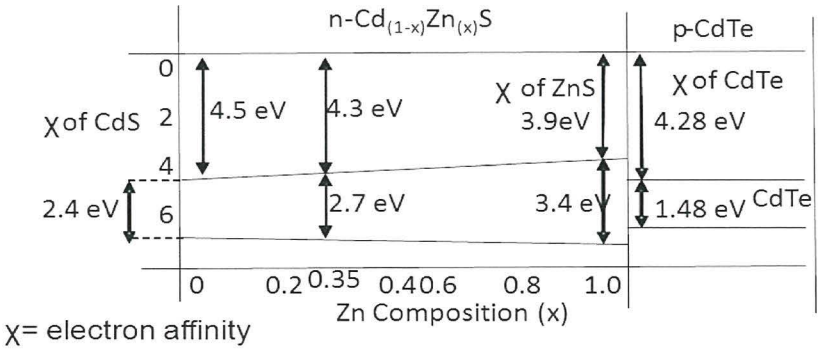

Figure 5.12: Schematic of $Cd_{1-x}Zn_xS$ window layer band gap with various Zn composition.

The CdZnS layer is an improved electron affinity match to the CdTe. An improved electron affinity match would occur at the lower Zn composition range, thus a "sweet-spot" exists, where an optimum match in electron affinity and band gap, where a wide enough gap exists to allow the high energy blue region photons through, but not too high to worsen the band gap match exists.

5.6.2 CdZnS/CdTe device results

Comparing the results in Table 5.8 to the current world record by Wu *et al.* [35], one can observe that the reported devices have a J_{sc} higher than the current world record device of 25.8 mA/cm^2; this could be attributed to the differing spectrum of the Xenon lamp, which although calibrated to the J_{sc} of the reference cell, has some deviation from an AM1.5 spectrum.

Table 5.8: Device results of: (i) baseline CdS/CdTe device (ii) baseline CdZnS/CdTe device. Device results are also shown with and without the p^+ back contact layer. All devices have 240nm thick window layers and 2 microns of CdTe absorber. *None of the CdZnS/CdTe devices had a ZnO insulating layer, as this proved detrimental to device performance.

Device Structure:	BCL	Efficiency (%) (+/- 0.3)	J_{sc}(mA/cm^{-2}) (+/- 0.3)	FF (%) (+/- 0.3)	V_{oc}(mV) (+/- 20)	R_{sh} (Ω cm^2)	R_s (Ω cm^2)
CdS/CdTe	No	9.7	22.6	60.7	710	2030	8.0
CdS/CdTe	Yes	10.3	24.4	65.4	650	1941	2.0
*$Cd_{0.9}Zn_{0.1}S$/CdTe	No	11.4	25.3	66.9	670	3154	2.4
*$Cd_{0.9}Zn_{0.1}S$/CdTe	Yes	13.3	26.1	73.7	690	5500	2.5

If one compares the standard baseline device (which includes the BCL), the addition of the $Cd_{0.9}Zn_{0.1}S$ window layer, has increased device conversion efficiency by 30%, improving J_{sc} and FF.

Interestingly, in devices where the wider band gap window layer is employed, the addition of the novel p^+ contact layer increases the R_{shunt}, which is opposite to the behaviour of CdS/CdTe based MOCVD devices, increasing FF. The increase in R_{shunt} would suggest a decrease in the probability of forming localized TCO/CdTe junctions and would usually be seen where the window layer is increased in thickness.

The larger than expected increase in shunt resistance for the wider band gap devices, could be due to the closer match in E_g between the ZnO (3.3 eV) and CdZnS (2.7 eV), compared to CdS (2.45 eV), promoting intermixing. However, it has been previously reported by Wu [12], that the $CdCl_2$ treatment could possibly introduce stress at the TCO/CdS interface, as CdS grain growth is thought to occur during the $CdCl_2$ treatment.

If one looks at the dark I-V profiles of both CdS/CdTe and $Cd_{0.9}Zn_{0.1}S$/CdTe devices (Fig 5.13), measurements show poorer forward bias characteristics for the CdZnS/CdTe hetero-junction, suggesting an increased dark series resistance. However R_s values under illumination (Table 5.8) show no back contacting problems, with R_s values only slightly larger than the CdS/CdTe device.

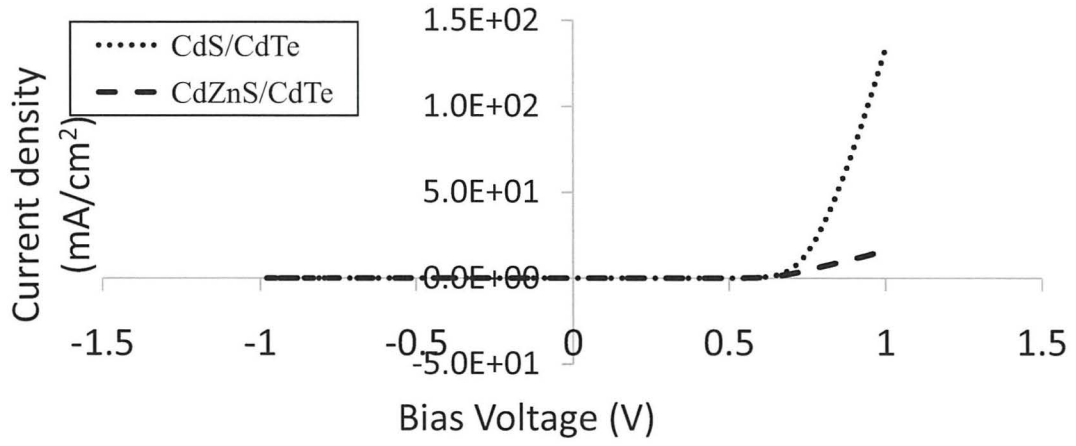

Figure 5.13: Dark I-V curves for CdTe devices with CdS and $Cd_{0.9}Zn_{0.1}S$ window layers.

In illuminated IV, the improvement in the device performance of CdZnS based devices is due to increased photo collection of higher energy photons. The absorption of high energy photons by the CdS layer has been limited (Fig 5.14).

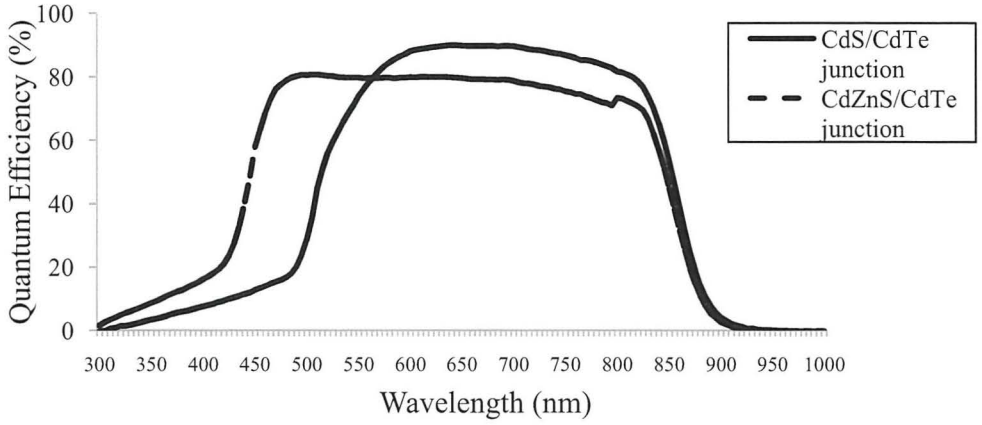

Figure 5.14: Quantum efficiency vs. wavelength for CdS/CdTe and $Cd_{0.9}Zn_{0.1}S$/CdTe device.

Interestingly, it can be seen that the top "top hat" of the QE curve, is overall lower for the cell with the wider band gap window layer, despite performing more efficiently. This could suggest a poorer junction quality as a result of the expected increase in the lattice mismatch with CdTe (approx. by 16 % [36]).

However, Gruzsecki *et al.* [37] suggest the efficiency loss attributed to the increased lattice mismatch can be minimal, compared to the gain achieved with lower blue absorption losses, resulting in an overall increase in the photo-current generation and conversion efficiency of the cell.

Integrating the range of band gap 2.7 eV for $Cd_{0.9}Zn_{0.1}S$ and 1.5 eV for CdTe, a simple integration of the absolute AM1.5 spectrum (obtained from NREL, website ww.nrel.gov). An integration between the stated band gaps yields an available increase of photon energy (compared with CdS (2.4 eV)) of up to 19 %. The measured increase in performance was 12 %, being slightly lower probably due to recombination losses in the bulk.

5.6.3 Transport mechanisms of CdZnS/CdTe devices

To compare the transport mechanism of the wider band gap devices, I-V-T has been carried out (Fig 5.15) on a baseline $Cd_{0.9}Zn_{0.1}S$/CdTe (Sgen 305). Firstly the Dark I-V-T results will be discussed. Fig 5.15 shows a graph of the current density-voltage characteristics (of log I versus V), the slope, A ($\log_e$ I/V), shows a somewhat less linear behaviour over the temperature range studied (200-300 K) compared to CdS/CdTe based devices.

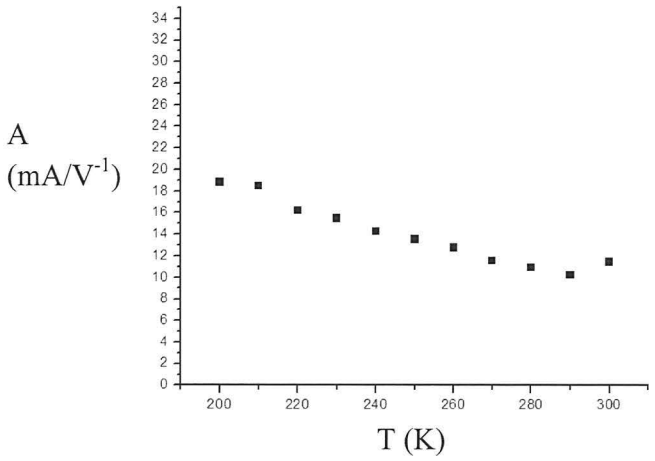

Figure 5.15: Relationship between $\ln I_o/V$ versus Temperature.

The $Cd_{0.9}Zn_{0.1}S$/CdTe baseline device is seen to vary with temperature, much more than the CdS/CdTe devices produced by either MOCVD or CSS. This suggests that the transport mechanism of the particular device is more likely to be due to a thermally activated diffusion process [38]. But behaviour under illumination gives the same transport mechanism as the baseline CdS/CdTe cells, both being governed by a Shockley Read Hall (SRH) type process.

C-V measurements have also been carried out for this cell. By using the same analysis, the doping concentration (N_B) was found to be 6.09 $\times 10^{23}$ cm^3, which is orders of magnitude larger than CdS/CdTe devices and V_{bi} was calculated to be 1.12 V.

One possible explanation for this overestimation in dopant concentration, was the high measured n values (+ 3 at room temp), which introduce the possibility that values of n and I_0 are not accurate for this device. Whilst n can be over 3, it is not likely for these samples, and some error is therefore assumed in this particular method for these devices.

One approach to estimate V_{bi} is the electro absorption technique developed by the Osaka University group [39]. Another method is the differential temperature method (DTM) developed by Hegedus *et al.*[40]. Analysing the V_{oc} response against T (Eqn. 5.1), the V_{bi} can be approximated (Fig 5.16).

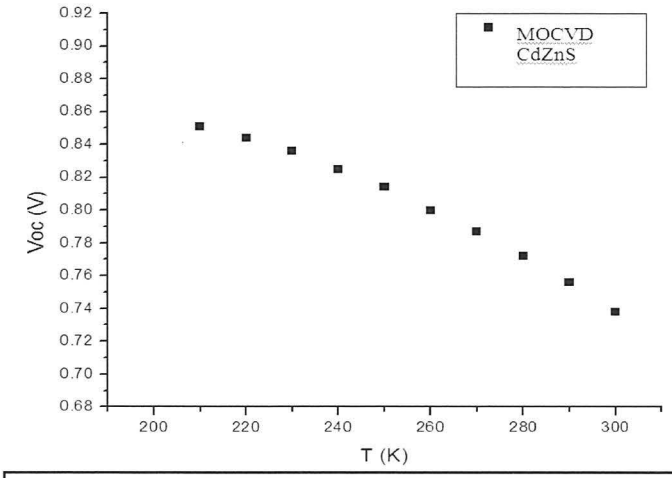

Figure 5.16: V_{oc} vs. Temperature (K) for light I-V-T

The DTM approach, assumes linearity in $V_{oc} - T$ over a limited range rather than all the way to $T = 0$. V_{bi} for the $Cd_{0.9}Zn_{0.1}S$/CdTe device was found to be 1.19 V.

If one compares this to that of baseline CdS/CdTe cells, (MOCVD (0.43 V), CSS (1.2 V)), one can immediately see the built in voltage of the $Cd_{0.9}Zn_{0.1}S$/CdTe MOCVD device is much larger than that of the baseline CdS/CdTe junction device. The inclusion of the wider band gap $Cd_{0.9}Zn_{0.1}S$ has brought the built in voltage of MOCVD devices in line with those of CSS devices.

Thanks to M. Alturkestani (Durham University), the CV technique was coupled with a temperature controlled chamber, to calculate the trap concentrations. The chamber was cooled using liquid nitrogen to reach temperatures down to 200 K, measured using a thermocouple. Results are shown in Fig 5.17.

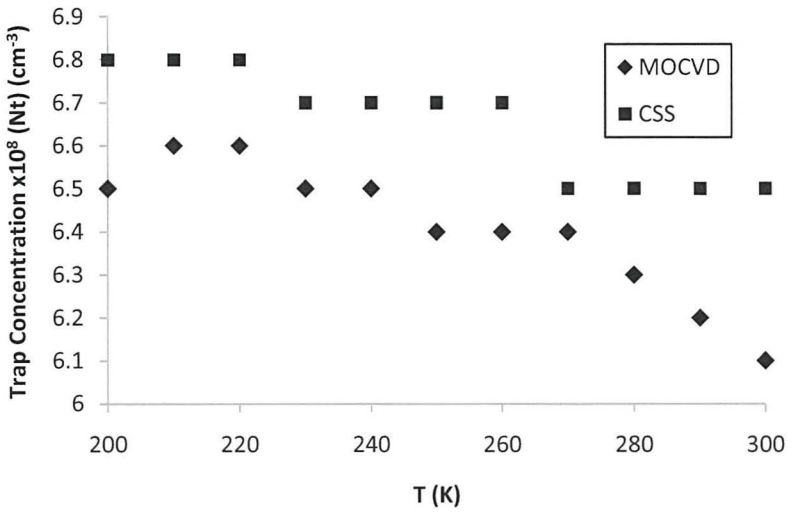

Figure 5.17: Trap concentration vs. Temperature for baseline CSS and MOCVD cells

Fig 5.17 shows that the trap concentrations in MOCVD and CSS devices are very similar. Shockley-Read-Hall (SRH) and tunnelling processes require high density of localised levels, which can result from the mismatch between CdTe and window layers. Reported trap concentrations are significantly lower than those reported by Bayhan *et al.* [26], where trap concentrations of up to 10^{15} cm^{-3} were reported for $CdCl_2$ treated vacuum deposited CdS/CdTe cells. Bayhan *et al.* [26] concludes that annealing with $CdCl_2$, lowered the density of interface states, improving the hetero-interface quality. Results here (Table 4.15) suggest that the novel $CdCl_2$ (MOCVD) treatment is working well, as the trap concentrations are similar to well established CSS $CdCl_2$ treatment.

5.7 BCL for very thin absorber devices

The BCL layer was included in the growth of all ultra thin films (100 nm thick BCL: As 2 x 10^{19} atoms.cm^3 sccm), as the increased doping from the BCL layer does improve overall device performance. An increase in the J_{sc} is observed for the higher doped bulk CdTe device, the decrease in the FF along with the V_{oc} lowers the conversion efficiency, compared to the lower doped device.

Possible suggestions why R_s is insensitive to the presence of the BCL with ultra thin absorber devices are; the presence of $AsTe_2$ at the back surface, which has previously been postulated [17], which is expected to reduce R_s at the back contact, but no direct evidence has been obtained.

The grain size at the back surface (of ultra thin devices) are a lot smaller, changing the GB:Grain ratio, which could allow improved GB passivation at the back contact region, as the $CdCl_2$ treatment could be over aggressive for the thinner layer. Other completely dry processing steps have been envisioned recently [41], but it is believed that this is the only process where no additional surface treatment prior to contacting is needed (i.e. no Br/MeOH etch).

5.8 Doping of very thin CdTe devices

Singh *et al.* [42], showed, that the resulting CdTe cell behaviour is very sensitive to variations in the doping profile near the junction. The problem of having such a low starting doping concentration at the interface can be observed if one looks at the Spectral response of the devices (Fig 5.18). Here, a 1 µm thick CdTe device, where the dopant level was started at a relatively low value (As partial preassure:1×10^{-7} atm) at the CdS/CdTe interface, and incrementally increased until the 2×10^{-6} atm (A^{+}) doping level was reached at the CdTe surface. The QE of a device where a constant 3×10^{-7} atm was applied, and another device where a higher 2×10^{-6} atm was applied throughout, are also included for comparison.

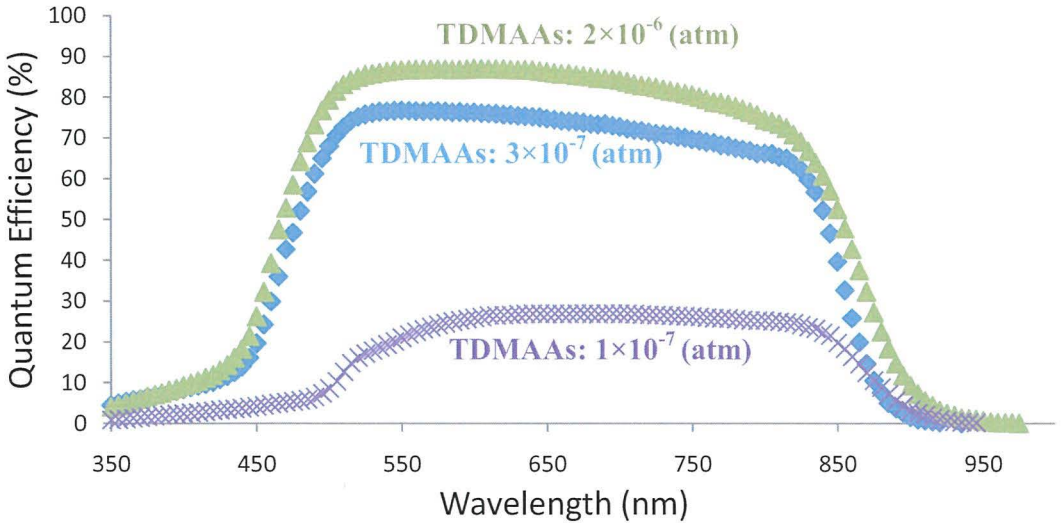

Figure 5.18: Quantum efficiency curve for various ultra thin absorbers which have been doped with different TDMAAs dopant partial pressure. Devices here did not include a separate BCL layer.

The poor performance of the QE of the graded doping device, demonstrates the importance of adequate doping close to the *pn* junction. A larger than expected change in the window layer region of the device (450-550 nm) is observed. This result suggests that the CdS is inadvertently affected by the decreased doping (i.e. or possibly given the low doping concentration, buried junctions might arise). The Cl doping of CdS is well documented [43]. It could be possible, that given a lower As dosage at the interface, that the Cl could interfere with the As doping level in the CdTe grains or grain boundaries and not simply collect at the grain boundaries, passivating them. If the carrier concentration is not high enough in the film, or if the mobility is too low (due to non-uniform doping), the current collection for the entire cell is limited.

Negative side effects of the $CdCl_2$ doping have been reported as increased inter-diffusion [44] of the CdS-CdTe layers and possible dopant compensation [1], as long as introduction of defect complexes [45], all which could explain the relatively low photon collection in this region for the graded device.

SIMS depth profiling was carried out of a series of devices (Table 5.3), to calculate the level of As doping in the layer. However, SIMS only measures the amount of As present in the layer, and does not signify that all the measured As is electrically active as acceptor dopant.

Three films were analysed by SIMS (Table 5.9), again an initially low doped device (1500 sccm/ 4 x 10^{17} atoms.cm^3), increased to 1950 sccm (2 x 10^{19} atoms.cm^3) at the back has been analysed. SIMS data for 2 x 10^{18} atoms.cm^3, bulk baseline doping level) and a highly doped bulk CdTe layer (2 x 10^{19} atoms.cm^3) (BCL doping level) has also been included for comparison purposes.

Table 5.9: SIMS doping results of CdS/CdTe devices with varying doping levels. *all samples polished chemically with BrMeOH solution.

TDMAAs partial pressure* (atm))	**H** (atoms.cm^{-3})	**O** (atoms.cm^{-3})	**Cl** (atoms.cm^{-3})	**As** (atoms.cm^{-3})
1.) no doping	1×10^{18}	6×10^{16}	9×10^{17}	1×10^{17}
2.) 2×10^{-6}	$<1\times10^{16}$	8×10^{17}	2×10^{18}	1×10^{19}
3.) 3×10^{-7}	$<1\times10^{16}$	$<1\times10^{16}$	1.5×10^{18}	1.2×10^{18}
4.) 1×10^{-7}	2×10^{18}	2×10^{16}	2×10^{18}	1.5×10^{17}

Firstly, the SIMS results of device where no *in situ* arsenic doping was used (Device 1, Table 5.2), showed an arsenic concentration of 1×10^{17} atoms cm^{-3}, suggesting a possible As memory effect exists in the reactor.

The measured As concentration of the low doped device (Device 4, Table 5.9) shows the same As concentration, as the device with no As doping in the device. This could be background interference in the SIMS setup, thus little or no active As is getting to the bulk of the grains at the CdS/CdTe interface, deteriorating performance, or an arsenic "memory" effect is present in the reactor, possibly de-gasing from the graphite susceptor,

The overall slope of the "top-hat" response suggests a worsening of the GB passivation towards the back contact region. Comparison with the QE (Fig 4.25) of 2 μm thick baseline device, shows a larger declining trend in the 500 nm – 850 nm range (Fig 5.18). The absence of the BCL layer in this series of device could potentially decrease the As doping level near the back contact. But unexpectedly, the highly doped device (Device 2, Table 5.9) which was doped with the BCL level of doping throughout, still showed a decrease in QE at long wavelengths, and could suggest the need for optimization of both, $CdCl_2$ and passivation treatments and back contact structure for thinner devices.

It should be remembered, that for these thinner absorber devices, the proximity of the back contact to the main *pn* junction is closer. It is therefore possible for these two junctions to interact and detrimentally affect the performance, and especially QE performance. However no large obvious trends are observed when the proximities of these junctions are brought closer.

5.9 Effect of the ZnO i-layer on ultra thin devices

The I-V behaviour of CdS/CdTe devices, where the absorber thickness is decreased is shown in Fig 5.19. Fig. 5.19 shows a shift in the shunting currents as a function of thickness and presence of an i-layer. For baseline cells, it is seen that the (ZnO) i-layer has lowered the shunting effect, relative to the baseline ITO device.

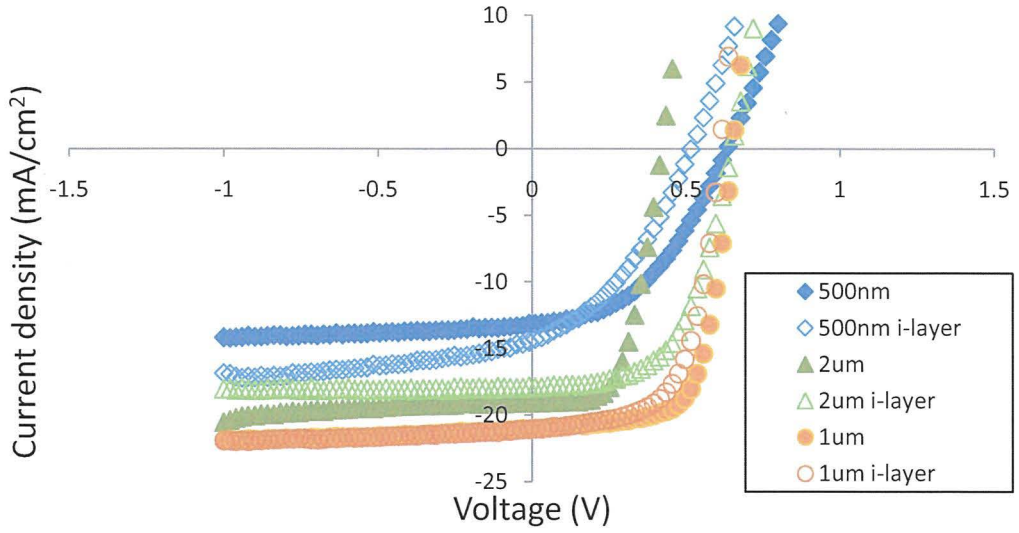

Figure 5.19: I-V of a series of different absorber thicknesses, with and without the ZnO insulating layer (i-layer).

When the absorber layer is halved from the baseline thickness of 2 μm (from 2 μm to 1 μm), no significant difference in the shunting between the ITO/ZnO and the standard ITO device is observed (at high reverse bias). The V_{oc}, is higher for the i-layer baseline (2 μm) thick devices, but for the thinner 1 μm devices, the IV curve shifts so that there is no improvement in V_{oc}, with identical reverse bias performance.

When the absorber thickness is reduced further towards ultra thin (500 nm), a clear shift in the shunting, being smaller for devices with the ZnO i-layer, consequently decreasing V_{oc}. This demonstrates a clear trend in the shifting of the shunt characteristics, simply by modifying the absorber thickness (Table 5.5.10).

The general trend of decreasing J_{sc} with absorber thickness is due to incomplete absorption (due to thickness being lower than the absorption edge of CdTe). Interestingly for the 500 nm device, the addition of the ZnO layer, seems to slightly improve the J_{sc}, possibly acting as an absorber layer extension, but given the measured depletion effect (depleting the CdS of electrons) of the ZnO layer, it is no surprise that the V_{oc} is lower.

Interestingly the V_{oc} of the best devices (at each absorber thickness) is nearly the same, this demonstrates that even with the increasingly closer proximity of both the main pn junction to the back contact, this appears not to limit the maximum achievable V_{oc}.

Maximum power appears to be achieved for the 1 μm thick device, also FF, and demonstrates that with the standard baseline growth conditions, the extra 1 μm of absorber is not totally "active" or necessarily needed in the device.

Table 5.10: Shunt resistances of CdS/CdTe devices with and without a ZnO insulating layer

Device structure	Absorber thickness (μm)	R_{sh}(Ω)
ITO/CdS/CdTe	0.5	1104
ITO/ZnO/CdS/CdTe	0.5	395
ITO/CdS/CdTe	1	1144
ITO/ZnO/CdS/CdTe	1	1164
ITO/CdS/CdTe	2	800
ITO/ZnO/CdS/CdTe	2	6711

5.10 Forming a model of the CdS/CdTe junction

Towards assisting to describe what could be occurring in ultra thin devices, the use of a software modelling package "SCAPS" has been used. SCAPS uses the analytical two diode model for cadmium telluride solar cells. In this model, the contact energy barrier (Φ_b) at the CdTe back contact structure gives rise to a Schottky diode pointing in the opposite direction to the main CdS/CdTe solar cell junction.

The analytical description of a CdTe solar cell with this 'two diode model' (Fig 5.20), is remarkably successful, because it gives a simple semi-quantitative description of some effects particular to the CdTe solar cell. The model was proposed by Stollwerck and Sites to explain the gross effects on the illuminated *I-V* characteristics [46], and was later refined at the University of Gent, to describe also the AC behavior, the influence of minority currents at the back contact, the voltage and illumination dependence at the back contact [18, 22, 47, 48]. For the solar cell junction, an ideal Shockley law is assumed with an ideality constant *n*.

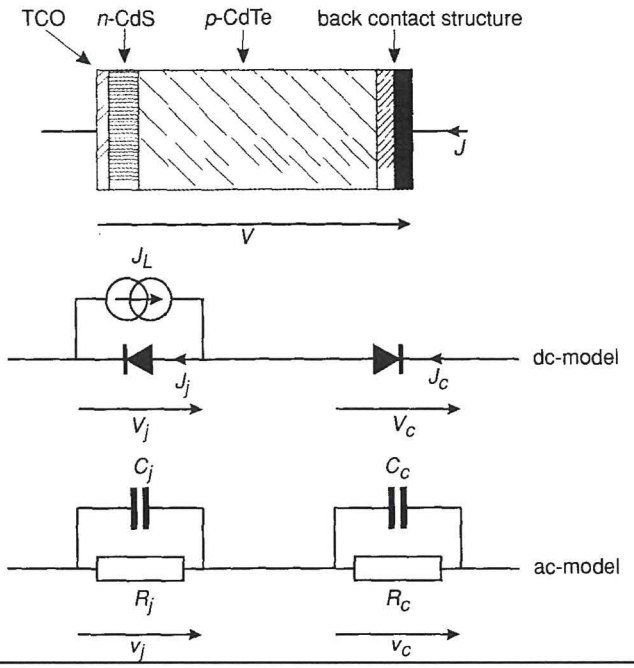

Figure 5.20: The two diode model for the CdS/CdTe junction and the back contact structure. After Kontges *et al.* [49].

5.10.1 Finding a consistent parameter set

A starting parameter set for simulating the most marked features of a broad class of CdS/CdTe thin film solar cells is the 'baseline set' given by Gloeckler and Sites [50].

A prerequisite is to find a consistent parameter set (Table 3.7), where a single parameter set is chosen for one cell, which describes all measured effects.

No assumptions are made about voltage or illumination dependence of some parameter, no presence of a "barrier", no artificial mechanisms are used (e.g. 'neutral levels' in which there is recombination, but no charge) These prerequisites, do not correspond to a physical reality, but are implemented in SCAPS and other simulation programs in order to simplify the modeling [48, 51]. Modeling parameters used can be seen in Table 3.7.

The SCAPS modelling program developed by the University of Gent by Burgelman *et al.*[48, 51] can be used for modelling, in 1D, basic TCO/CdS/CdTe structures at normal working conditions.

To simplify the simulation of the MOCVD devices, the highly doped CdTe (p^+ back contact "BCL" layer) has been omitted and a series resistance value of 2 $\Omega \cdot cm^2$ has been assumed. Data from C–V of baseline MOCVD devices were also entered into the model with acceptor concentration of 5×10^{14} cm^{-3} and minority carrier diffusion lifetime of 1 μs.

The approach used in this thesis is similar to that of Verschraegen *et al.* [52]. Where an approach of selecting a baseline parameter set, where only one parameter was varied at a time, (thickness in this case) was used. A three layered model (ITO (120–160 nm), CdS (240 nm), and CdTe (2 μm) agreed well with calculated conversion efficiencies of baseline MOCVD cells.

5.10.2 Ultra thin CdS/CdTe device modelling

A SCAPS model has been developed, and used to compare against experimental data, the effect of reducing the absorber layer of the device, keep all other parameters constant. Decreasing the absorber thickness down to 0.2 μm (Fig 5.21), one can observe a decrease in efficiency as a result of decreased absorption volume, decreasing more rapidly as the absorber thickness is decreased below 1 μm. Overall, the measured device efficiency decreases at a faster rate than predicted by the basic model.

Analysis of the device parameters showed that J_{sc} and V_{oc} (despite being overestimated by the model), agreed well at thicker absorber thicknesses but decreased more rapidly at < 1 μm. The smaller values of V_{oc} for thinner absorber layer devices suggests that the saturation current increases dramatically, as the J_{sc} is expected to decrease with decreasing absorber thickness. FF, contrarily to the model, decreased at thicknesses below 1 μm, caused by a larger decrease in shunt resistance.

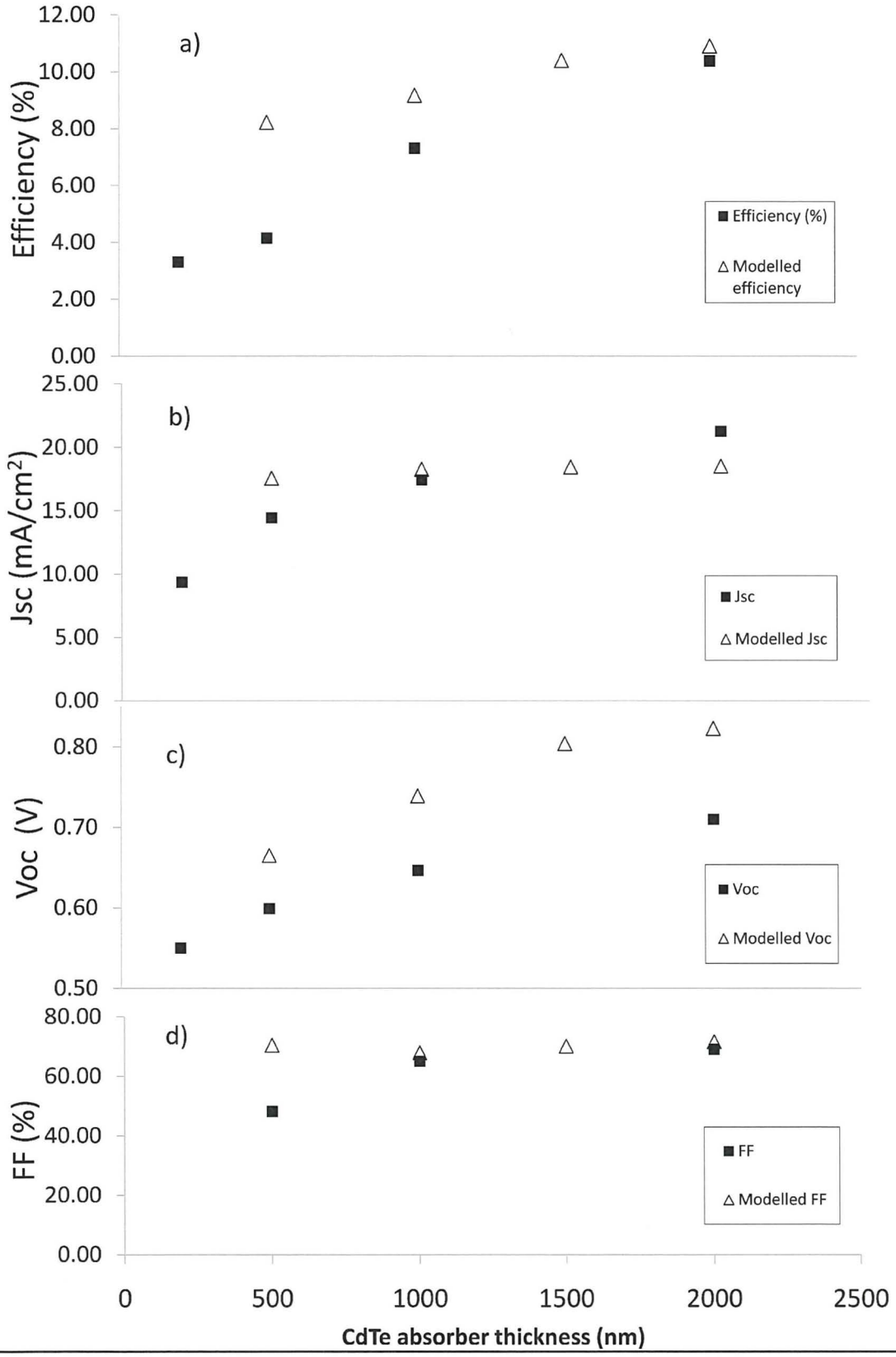

Figure 5.21: Measured and modelled device parameters as a function of absorber thickness.

The large decrease in device parameters with decreasing absorber thickness (below 1 μm) suggests the cells are not limited by optical absorption. By the basic addition of an acceptor defect between the CdS and CdTe, the agreement of the basic model with measured results improved, particularly when ultra thin absorbers were employed, possibly signifying an increase in the interface defect density with thinner absorbers. The results (Fig 5.21) show that the reduction in optical absorption appears not to be the limiting factor for ultra-thin layers, but are limited by shunting.

Optical limits can be address by approaches similar to Amin *et al.* [53], where the absorber thickness was reduced, in conjunction with introducing ITO with varying roughness or "haze ratios" which encourages increased optical confinement, increased light scattering. This work is similar to work done by Gupta *et al.* [54], where the effect of CdTe thickness reduction on the performance of CdS/CdTe solar cells (grown by sputtering). Gupta *et al.* [54] also decreased absorber thicknesses (from 3 μm down to 0.5 μm), and held the CdS thickness and back-contact-processing constant. The electrical parameters of the cells (produced by Gupta *et al.* [54].) exhibited only a gradual decrease in performance as the CdTe thickness decreased to 0.75 μm, but then a substantial decrease occurs for 0.5 μm demonstrating limitations attributed to shunting.

Shunt limitation therefore is an important goal for ultra-thin absorber devices, where a large decrease is observed at thicknesses < 1 μm. It has been suggested that the GB properties may be sufficiently different for larger grain films which explain the need to have thicker films to avoid films due to shunting [54], and presents a strong possibility that the optimized growth conditions of thicker "baseline" films, are not suited to the structure of ultra thin devices.

A clear discrepancy in the value of V_{oc} is observed (even for the thicker "baseline" 2 μm device).The model was modified to better represent ultra thin grown MOCVD devices, which are suspected of having increased shunting with thinner absorber layers (lowering of V_{oc}).
This was done, by an addition of an "acceptor" defect layer (10^{14} cm^{-2}) at the CdS/CdTe interface was added, and produced improved agreement with measured devices with thicknesses below the absorption limit, but underestimated the conversion efficiency for thicker layers (Fig. 5.22).

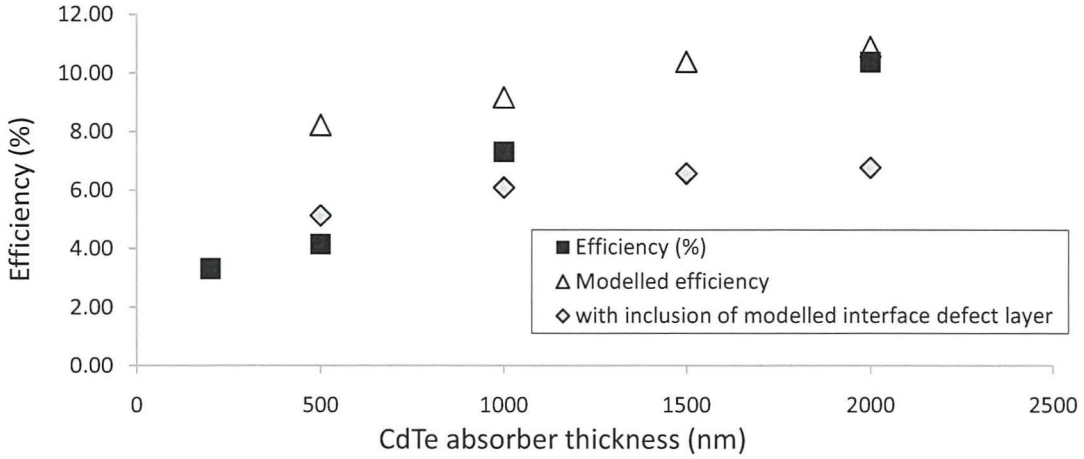

Figure 5.22: Efficiency vs. absorber thickness for a (i) measured, (ii) modelled, and (iii) after introduction of an acceptor defect at the CdS/CdTe interface.

The closer agreement with efficiency values (Fig 5.22) with the junction defect model, could suggest an increased sensitivity to defects at the CdS/CdTe interface of ultra thin devices, or more likely from pin-hole defects and increased shunting effects.

The modelling results presented, are similar to the modelling work carried out by Amin *et al.* [55] for CSS cells. Custom modelling software was used, using a 1-D simulation program named NSSP (Numerical Solar cell Simulation Program). Amin *et al.* [55] showed that all the solar cell characteristics remained almost unchanged over the thickness range of 10 down to 3 μm, until V_{oc} and J_{sc} severely decrease at thicknesses less than 2 μm.

Amin *et al.* [55] showed that recombination losses at the back surface do increase with decreased thickness. In order to investigate the back contact recombination rate, Amin *et al.* [55] modelled the effect of keeping the CdTe thickness constant at 1 μm, whilst the back surface recombination rate was modified. Amin *et al.* [55] reported a large decrease in conversion efficiency (due to decreases in V_{oc} and J_{sc}), if the back surface recombination velocity was increased, and could suggest a possible explanation for the larger than modelled decrease in efficiency observed for MOCVD devices at thicknesses below 2 μm (Fig 5.21).

To inhibit the possible recombination loss at the back contact of ultra thin (e.g., 1 μm) CdTe solar cells, a wide band-gap material ZnTe (Eg of 2.26 eV) has been proposed, giving a CdTe/ZnTe hetero-junction [55]. This wide band-gap material would act similarly to a BSF to repel the minority carriers at the CdTe/ZnTe heterojunction and thus would decrease the loss of carriers at the back contact.

Amin *et al.* [55] identified a useful indicator whether a back surface field (BSF) is present in thin devices, as the modelling shows that V_{oc} actually increases for absorber thicknesses below (<1 μm), whereas non BSF devices, the V_{oc} degrades along with all other device parameters for (<1 μm) absorber devices.

5.10.3 Discussion on ultra-thin CdZnS devices

Fig 4.27 shows increasing absorption in the blue region with thickness. This trend is indicative of the window layer becoming thicker, increasingly blocking transmission of photons, and could suggest an increased intermixing at the CdZnS/CdTe junction or the presence of a buried junction. Such a large shift was not observed for the ultra-thin CdS/CdTe devices (Fig 4.25), where less collection was observed. Several authors [56, 57] comment on the effect of a more severe $CdCl_2$ treatment enhancing CdS diffusion into CdTe, which could possibly be happening as the $CdCl_2$ has not been optimized for ultra thin films.

The overall improvement in the QE "top hat" for thicker absorbers, could be due to improvement in the bulk CdTe facilitated by an optimized $CdCl_2$ treatment. The decrease in QE between 600-800 nm is due to a lack of complete absorption of these photons. Overtreatment of $CdCl_2$ would cause a large V_{oc} loss, as it is expected to introduce deep recombination centres.

The decreased performance in the red region (ca. 600–700 nm), suggest deep penetration losses, and have been attributed to incomplete absorption of the photon, lowering the red response of the device, as the absorber thickness is decreased.

Again, no large effects are observed in the back contact region (800-900 nm), as the proximity of the back contact and *pn* junction could become a problem. Interestingly, similar to 200 nm CdS/CdTe devices (Fig 4.25), the QE improves as one moves from lower (550 nm) to higher wavelengths (800 nm), with a maximum at approx. 780 nm. This suggests increasing passivation of the GB near the back contact region, which could be facilitated its back contact proximity to the *pn* junction.

It should be noted, that since we are reducing the absorber thickness way below its absorption edges, unknown behaviour is likely to exist, as device operation could be at the limit of the material capability. Thus it should be noted that several factors which can cause misinterpretation of the QE results include, the presence of secondary barriers, and photoconductivity in the absorber layer [56].

5.10.4 Modelling $CdCl_2$ treatment with SCAPS

Work towards optimizing $CdCl_2$ for the ultra thin absorbers could not be done in the allocated time, but an attempt using software modelling has been done.

Burgelman *et al.* [30] states, that an increasing `degree of $CdCl_2$ treatment' can be modelled by an increasing density of deep acceptor states. The introduction of a CdTe "acceptor density" (from 10^{14} to 10^{16} cm^{-2}) defect has been used to model the effect of an increasing $CdCl_2$ treatment (Fig 5.23).

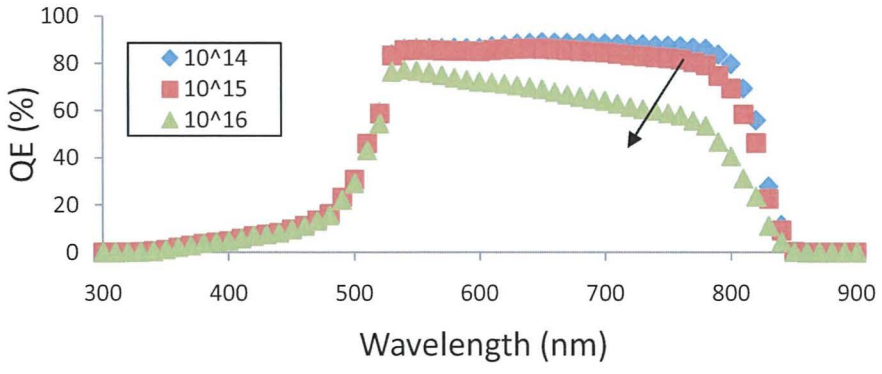

Figure 5.23: Modelled QE curves for a 1 µm thick CdTe device, where a CdTe acceptor defect has been introduced and increased.

These trend of decreasing response in the back contact region, agree well with observed drops in the 750-800 nm (Fig 4.27), and are similar to those obtained by Gupta *et al.* [58]. Gupta *et al.* [58] also reported a decrease in the back contact region was observed with decreasing absorber thickness, and suggests that a slight "overtreatment" of $CdCl_2$ exists for the ultra thin absorbers. Thus it is suggested that the $CdCl_2$ treatment time should be decreased for thinner CdTe absorbers [58], and possibly the annealing/sintering (currently 420 ^{o}C for 30 mins) also to be decreased to further improve the efficiency for thinner absorber devices.

Wu [12] also comments on the possible over treatment of $CdCl_2$, which could possibly introduce stress at the TCO/CdS interface, as CdS grain growth is thought to occur during the $CdCl_2$ treatment.

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CHAPTER 6

6.0 CONCLUSION

Using a research level MOCVD system, complete CdS/CdTe and CdZnS/CdTe, thin film PV devices have been successfully grown.

The novel use of a separate BCL towards improving the R_s has been demonstrated. Using the high controllability of MOCVD, it has been shown that the band gap of grown layers can be tuned, by close control of precursor concentration. The problem of horizontal reactors has been addressed allowing a nearly uniform layer to be grown, improving device uniformity.

Through optimization of the deposition temperature, $CdCl_2$ process, introduction of a ZnO "i-layer", and the introduction of a novel "BCL" layer (lowering R_s from 10 to 2 $\Omega \cdot cm^2$, reducing the need for wet etching prior to back contacting), the 10% efficiency target originally set out has been achieved and even surpassed, through the use of a wider band gap layer. This work reports the successful replacement of the CdS window layer by a wider band gap layer ($Cd_{0.9}Zn_{0.1}S$) has been shown to improve the photon collection in the energy rich blue region of the AM1.5 spectrum, improving J_{sc} and ultimately efficiency, increasing from 10 % to 13.3 %. A shift in the optical band gap was observed for the ultra thin CdZnS/CdTe devices as the absorber thickness is decreased and could suggest increased intermixing or the presence of a buried junction as the absorber thickness is reduced.

It is reported that for ultra thin absorber devices (<1 μm), no roll-over behaviour is observed with the standard TDMAAs doping level (3×10^{-7} atm / 2×10^{18} atoms cm^{-3}), indicating no presence of a Schottky barrier for ultra thin devices. The shunt resistance decreases considerably as the absorber thickness is decreased. It is known that degradation of the main diode can result in a lowering of R_{shunt} due to tunnelling pathways, therefore R_{shunt}, can be used to gauge the junction quality and used to give an approximate quality meter on the non-uniformity of the junction, which has been shown to be more critical in ultra thin absorber devices, as possibly weak diodes and non-uniformity issues are expected.

The apparent lack of the BCL to improve the R_s for ultra thin devices can be explained by the apparent increase in doping level for the ultra thin devices, which could lead to a decrease of the depletion layer width, increasing the probability of tunnelling at the back contact region. The possible $CdCl_2$ overtreatment of the ultra thin layers is also discussed, and shown to be likely, given the change in the grain/GB structure of ultra thin devices, which also have a measured increase in As doping concentration.

The estimated depletion layer width has been calculated as slightly larger for 1μm ultra thin devices, which represents a larger fraction of the device, possibly increasing field assisted charge collection. The close proximity of the gold back contact to the pn junction in ultra thin devices seems not to adversely affect device performance as very thin devices have been made.

The ZnO layer has been shown to be beneficial to the standard 2 μm thick CdTe baseline device, improving (increasing) shunt resistance, decreasing sensitivity from pin holes which can short the device. Conversely, its inclusion in ultra thin absorber (< 1 μm) devices, have not produced favourable results, A possible explanation could be due to inadvertently Cl doping of the ZnO/CdS junction region, as the $CdCl_2$ treatment has only been optimized for the 2 μm baseline devices. This could decrease the resistivity of the ZnO, limiting any potential improvements in the shunt characteristics of the device, as the benefits of the ZnO is due to its high resistivity [1].

The improvements in device parameters (η, FF, and J_{sc}) with doping, using a p-type (TDMAAs) dopant, brings into question the proposed junction model proposed by Dharmadasa *et al.* [2]. Dharmadasa *et al.* model ascribes a CdS (n-type)/CdTe (n-type) junction, where improvements in device parameters would be expected by an n-type dopant. The use of a p-type dopant such as (TDMAAs) in this research, and the apparent improvements in device parameters (J_{sc}, FF), brings into question this model for MOCVD grown CdS/CdTe devices.

However, the successful growth of a ultra thin 0.2 μm thick CdTe absorber device brings into question the traditional *pn* structure of CdS/CdTe interface, as 200nm p-type CdTe alone is not sufficient for a *pn* junction [3].

Towards understanding the limiting factor for ultra thin devices, the wider band gap layer has been inserted into the ultra thin devices, increasing the proportion of higher energy photons to improve J_{sc}. Small improvements in J_{sc} was observed, but the general trend of decreasing J_{sc} with decreasing absorber thickness is still observed. Results (Fig 5.14) show, that the ultra thin devices are not limited by the number of photons, as the decrease of efficiency with absorber thickness of ultra thin CdZnS/CdTe devices is occurring at an increasing rate as the absorber thickness is decreased. This assertion is supported by the SCAPS modelling results (Fig 5.11), which show that the modelling results agree with thinner absorber devices after the addition of a defect layer, suggesting an increased sensitivity to defects at the CdS/CdTe interface. In the absence of direct evidence to support this assertion, it is likely that the thinner layer deviation from the original SCAPS model (Fig 5.10) prediction is occurring due to pin-hole defects and increased shunting, lowering FF, at the CdS/CdTe and CdZnS/CdTe junction region.

Finally preliminary work has demonstrated that unabsorbed photons (in ultra thin devices), can be reflected by the use of a back reflector. It is possible that the gold contact to some extent, already facilitates this, but a modified back reflector structure could re-inject photons not absorbed by the device.

The results obtained in this thesis, has identified several material and device structure limits (e.g. absorber thickness, micro non-uniformities, G.R. dependence on Temp etc.). These can be used as a reference when the focus of research will shift from the horizontal MOCVD reactor, and towards the larger, in-line MOCVD reactor.

6.1 Main findings

- First growth of all in one CdS/CdTe including the $CdCl_2$ in a device using MOCVD, demonstrating the possibility of a complete all in once manufacturing solution.
- To the authors' knowledge, the first reported beneficial use of $Cd_{1-x}Zn_xS$ layers in CdTe based solar cells, by any deposition method.
- Shown no Schottky barrier present for ultra thin absorber devices <1 μm, avoiding the need to grow a separate highly doped "back contact layer" / or to chemically treat the surface to improve the electronic junction (lower the effectively Schottky barrier) when contacting with a metal with a high enough χ (electron density).
- Shown by I-V-T, that CdZnS based devices have an intrinsically different electron transport mechanism in the dark, compared to the standard CdS/CdTe device.
- Shown that the high control and measurability of MOCVD, has allowed the growth of ultra thin CdS (240 nm)/CdTe (200 nm) devices, which defy the traditional device physics of a CdS/CdTe pn junction [3].
- Shown that ultra thin absorber devices are limited by recombination, and not purely by active absorber area.
- Used experimental results and modelling to show that reducing the absorber thickness from 4000 to 200 nm, where junction proximities become more of an issue; (Back contact junction), TCO/ window layer (CdS) junction, and the main pn CdS/CdTe junction, do not appear to obstruct efficient device operation.

6.2 Implications for scale up / current manufacturing

CVD is already setup in many large scale manufacturing plants e.g. Pilkington, and if one considers that if this technology was applied to a factory which already made float glass, MOCVD could simply be bolted on the line. The main issue with the adaption of this technology is the requirement for a "sealed system", given the pyrophoric nature of the precursors used.

If one considers an inline process, the reactor size would only need to be as wide as the glass / module. However, the slow nature of the deposition speed in MOCVD, which gives it its high level of quality and controllability, is its disadvantage, and would be needed to be sped up orders of magnitude before consideration by many industrial companies.

Work is currently underway of optimizing this roll-to-roll and inline MOCVD solutions for upscale, and the main priorities will have to tackle; deposition uniformity and speed.

6.3 Further possible work

It should be noted that the lowering of the R_s for ultra thin cells, by using the same doping concentration as the standard baseline devices, has not been explained fully, and the closer proximity of the back contact and the main *pn* junction could hold a clue for further research.

The Optimization of $CdCl_2$ and anneal conditions for ultra thin devices should be done, where a less aggressive $CdCl_2$ treatment and anneal could improve the performance of ultra thin CdZnS/CdTe further, and could highlight relationships between As and Cl doping with the grain/grain boundary (GB) ratio, which is likely to change with absorber thickness.

The need for sufficient p-type doping of the CdTe near the surface (Fig 5.5), has demonstrated the complex nature of CdTe doping, where it is postulated that the As is used to dope the CdTe grains, and the $CdCl_2$ treatment to passivate the grain boundaries. It is therefore possible for interactions between these two dopant mechanisms, if complex dopant compensation exists. Therefore it is suggested to conduct an accurate p-type doping study to determine the critical doping concentration, then, more complicated interactions with Cl doping can be studied, where the As concentration is monitored relative to the Cl incorporated concentration.

It has been shown that a good electron affinity (χ) match to CdTe, could be achieved for low Zn concentration, but at high Zn concentrations, junction performance deteriorated due to a positive conduction band-offset, and demonstrated an optimum Zn alloy concentration. Even though poor performance was achieved with Zn rich window layers, it is suggested that if the resistance of the Zn rich-CdZnS could be limited (by doping), further device performance improvements could be seen with higher Zn alloy concentrations.

Given access to other techniques the author believes the following could give a major insight into the improvement of MOCVD CdS/CdTe devices and particularly ultra thin devices.

X-ray Photoelectron Spectroscopy (XPS)

Towards understanding what could be limiting the ultra thin layers, an in-depth investigation using XPS, one could measure the band bending at the interface of CdS/CdTe, and could determine if the *pn* junction is improved.

Electron Beam Induced Current (EBIC)

Cross-sectional analysis of full devices using an EBIC, could allow the physical measurement of the junction region, which would allow an improved investigation of doping and absorber thickness effect on the *pn* junction location and proximity.

Laser Beam Induced Current LBIC

As LBIC can be used to directly measure the photo-current, a highly accurate map of the photo-response could be obtained. Ultra thin layers should show increased lateral non-uniformity, and could suggest an optimum thickness, where the minimum absorber thickness is used for the best shunting and device performance, potentially increasing the materials utilization.

BI-facial Analysis

Preliminary results have shown that bi-facial analysis can be done already using an un-optimized back contact structure. It is suggested that QE measurements to be used to carry on research in this area, separating *pn* junction limitations with back contact effects, possibly highlighting what is happening to the device, when their proximity is changed.

References

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[2] A. P. Samantilleke, I. M. Dharmadasa, N. B. Chaure, J. Young, *Semicond. Sci. Technol.* **2002**, *17*.
[3] D.Bonnet, *Private communication*.

APPENDIX

Table 1: TDMAAs doping reference table

TDMAAs partial pressure (atm)	Corresponding Arsenic Concentration (atoms cm^{-3})
3×10^{-9}	1×10^{16}
3×10^{-8}	1×10^{16}
6×10^{-8}	1×10^{17}
1×10^{-7}	4×10^{17}
3×10^{-7}	2×10^{18}
5×10^{-7}	6×10^{18}
2×10^{-6}	2×10^{19}