DOCTOR OF PHILOSOPHY

Electrical and Optical Response of Organic MIS and Related Structures

Watson, Colin Peter

Award date:
2011

Awarding institution:
Bangor University

BANGOR UNIVERSITY

Electrical and Optical Response of Organic MIS and Related Structures

by

Colin Peter Watson

A thesis submitted in partial fulfillment for the
degree of Doctor of Philosophy

in the
College of Physical and Applied Sciences
School of Electronics

June 2011

Contents

List of Figures

List of Tables

Abstract

The properties of organic semiconductors provide opportunities for low-cost optical sensors. In the first part of this work, the suitability of organic metal-insulator-semiconductor (MIS) capacitors as elements in optical sensing arrays and charge-coupled devices (CCD) has been investigated. Of utmost importance in MIS devices is the interface between the insulator and semiconductor, where interface traps can lead to device instabilities and poor charge transfer in CCD-type structures. MIS capacitors with either polysilsesquioxane (PSQ) or photoresist (SU8) as the insulator were fabricated under ambient conditions, with poly(3-hexylthiophene) as the organic semiconductor. Electrical characterisation of devices was performed both in the dark and under illumination with bandgap light.

Admittance measurements obtained in the dark at temperatures of 125–375 K revealed both PSQ and SU8 devices had good stability up to ~325 K; the capacitance-voltage (*C*-*V*) plots showed consistent behaviour with both PSQ and SU8 devices exhibiting fairly constant flatband voltage, doping density $\sim 10^{15}$ cm^{-3}, and interface state density $\sim 10^{10}$ cm^{-2} eV^{-1}. However, the bulk mobility in PSQ and SU8 devices deviated from both Arrhenius and T^{-2} temperature dependencies. Bulk mobility of a further set of SU8 devices, fabricated under nitrogen, exhibited an Arrhenius temperature dependency, indicating that despite undergoing several annealing cycles, atmospheric dopants were still present in devices fabricated in air.

C-*V* plots of both PSQ and SU8 devices revealed increased depletion layer capacitance and anti-clockwise hysteresis when irradiated with light of energy greater than or equal to the HOMO/LUMO energy gap. Up to $\sim 10^{12}$ photo-generated electrons were trapped at the interface resulting in large shifts in flatband voltage. De-trapping of electrons was found to be much slower in SU8 devices, and followed a stretched exponential decay in both PSQ and SU8 devices. The optical response of MIS capacitors was found to depend on the intensity and wavelength of the incident light and the bias voltage scan rate. A basic model accounting for these factors was developed which simulated the *C*-*V* response of MIS capacitors during exposure to light. Transfer of photo-generated electrons between adjacent MIS capacitors, as in a single charge-injection-device, was demonstrated in both *C*-*V* and displacement current measurements. This result indicates the possible use of organic materials in CCD-like structures.

Chapter 6 reports the successful application of an organic photo-voltaic (OPV) cell as the near-field detector in a surface plasmon resonance (SPR) bio-sensor. Photo-current generated by the OPV during specific binding events at the sensor surface correlated well with reflectivity measurements made with a silicon photodiode. Sensitivity was found to be lower than a conventional bio-sensor, but could be enhanced by improved device structure and surface functionalization.

Acknowledgements

First of all I would like to thank my supervisor, Professor Martin Taylor for all his support and encouragement over the last few years. I would especially like to thank him for arranging my visit to MIT, for which I would also like to thank the Drapers Livery Company for the award of the Professor Wyn Humphrey Davies Bursary.

Thanks to Hmoud, Janet, Penny, James, Mohamed, Dan and latterly JK and Eifion at the Plastic Electronics Research Centre for their discussions, support, encouragement and friendship. Dr. Paul Sayers deserves a special mention for his never-ending patience, help, and advice.

During my studies I have had the pleasure of meeting, working and collaborating with many interesting people. It has been a privilege to work with Mervat, Marie, Rene and the Brazilians - Jose, Neri, Elder, Fernando and Alex on many different projects.

Many thanks must go to Associate Professor Marc Baldo at the Soft Semiconductor Group for his warm welcome and for hosting me at MIT. It was an exciting and enjoyable experience working alongside Mihai, whose project I collaborated on. Thanks also to the other group members, Jiye, the two Michaels, Shlomi, Carlijn, Tim, Priya and Kaveh for their helpful discussions and camaraderie.

Last, but most definitely not least, a big thank you to all my family, especially Allison and Matthew, for all their love and support.

Chapter 1

Introduction

1.1 Introduction

The optical and electronic properties of π–conjugated polymers provide the basis for low cost, low-temperature processing of novel electronic devices. The ability to deposit them from solution allows circuits to be fabricated on large, flexible substrates using various methods such as ink-jet printing, nano-imprinting [1], gravure [2] and high speed roll-to-roll printing [3]. Small molecule semiconductors tend to be deposited by thermal sublimation, where the heated organic material evaporates on to a substrate in a vacuum chamber [1].

Researchers in the field have developed several electronic components, analogous to inorganic devices, such as organic field-effect transistors (OFETs) [4, 5], organic memory [6, 7], solar cells [8], photo-detectors [9], sensors [10–12] and organic light emitting diodes (OLEDs) [13]. OLED technology has matured and gained tremendous commercial success as display panels in, for example, mobile phones [14] and televisions [15].

Chemical modification of polymers can change their morphology, electronic and chemical characteristics. For example, the energy gap between the highest occupied molecular orbit (HOMO) and lowest unoccupied molecular orbit (LUMO) in OLEDs can be tuned to specific wavelengths of light [16].

Electronic conduction in organic materials has been known for some time. Early studies were made using phthalocyanine and anthracene crystals [17].

However, it was not until 1977 when Shirakawa *et al.* [18] doped polyactylene with iodine that metallic-like conduction was obtained, achieving a conductivity of 105 S/m. This led to the development of rectifying organic p-n junctions [19], Metal-Insulator-Semiconductor (MIS) diodes [20] and OFETs based on a polythiophene semiconductor [21]. Interest in organic optoelectronic devices increased when Tang and van Slyke reported the first OLED in 1987 [13]. Research continued into OFETs with the use of conjugated small molecule (or oligomer) compounds and conjugated polymers. Oligomers such as α–sexithienyl [22] and metallophthalocyanines [23] were used as the semiconductor. These oligomers are insoluble and were deposited by vacuum sublimation onto silicon wafers. In fact most early work used heavily doped silicon for the gate structure with silicon dioxide (SiO_2) as the insulator. Amongst the small molecules is pentacene which provides the best recorded results for OFETs. Mobilities of about 3 cm^2/Vs [24] have been achieved which outperforms that of hydrogenated amorphous silicon (a-Si:H), typically $\sim$1 cm^2/Vs [25].

Conduction in these OFETs was obtained in accumulation, with the ability to conduct only positive charge carriers (holes). These organic semiconductors are deemed to be p-type. Successful integration of OFETs into electronic circuits arrived when researchers at Philips constructed logic gates and ring oscillators, indicating that such devices can perform logic functions [26]. Other examples of inverters and logic gates based on p-type semiconductors soon followed [27, 28].

N-type behaviour in OFETs was demonstrated by Hadden *et al.* at Bell Labs [29]. These OFETs used a thin-film of Buckminsterfullerene (C_{60}) as the active layer providing a field-effect mobility of up to 0.081 cm^2/Vs. With the advent of n-type devices it became possible to build complementary circuits, the idea being to produce low power, low noise circuits with improved stability, similar in concept to CMOS technology. Initially inverters, ring oscillators and simple logic devices were developed [30, 31]. Following the successful implementation of these devices, Crone *et al.* created more complex circuits such as row decoders and shift registers with 864 transistors [32]. Typically, these circuits operated at voltages up to 100V (see, for example, reference [31]). More recently Klauk *et al.* fabricated inverters, NAND gates and ring oscillators operating at the low supply voltages of 1.5 to 3 V [33]. These state of the art circuits used a self-assembled monolayer (SAM) gate dielectric combined with pentacene (p-channel device) and hexadecafluorocopperphthalocyanine ($F_{16}CuPC$, n-channel device) as the organic semiconductors. This result demonstrated the suitability of organic based devices for low-power applications. A drawback of these complementary circuits, though, is the extra processing required in depositing and patterning two different semiconductors.

Chua *et al.* [34] demonstrated that conjugated polymers are capable of ambipolar conduction. Using a suitable organic gate dielectric, divinyltetramethylsiloxane-bis(benzocyclobutene) (BCB), they found the trapping of electrons at the semiconductor/dielectric interface was reduced, and OFETs were able to form a conducting channel of electrons. Other dielectric/semiconductor combinations also revealed ambipolar conduction in p-type materials [35]. Ambipolar OFETs with well-balanced hole and electron mobilities using heterogeneous blends of p-type and n-type materials enabled the implementation of complementary circuits [36, 37].

1.2 Organic Semiconductors

Not all organic compounds are semiconductors. Only those which have alternating single and double bonds, known as conjugated polymers, exhibit this property. Carbon possesses six electrons, whose electronic ground state is $1s^2 2s^2 2p^2$. Electrons occupying the 1s orbital are closest to the nucleus and have the least potential energy, however the four electrons held in the 2s and 2p orbits can bond with other elements forming various compounds. In the bonding process three hybrid sp^2 orbitals are formed which are planar with 120° separation. In ethene (C_2H_4), for example, the three sp^2 orbitals in each carbon atom form three σ bonds, one to each hydrogen and one to the other carbon atom. This leaves a free electron on both carbon atoms which now occupy the p_z orbital in the vertical plane. Being more loosely coupled, these two electrons form a π–bond between the atoms, giving rise to the 'double' bond (Figure 1.1).

Due to the coupling of these electrons, the energy levels split into π molecular orbitals (bonding states, lowest energy level) and π^* molecular orbitals (anti-bonding states, highest energy levels) [38]. In conjugated polymers, containing many π–bonds, interactions between p_z orbitals cause the energy levels to split into bands. An energy gap (henceforth referred to as the band gap), analogous to the band gap in inorganic semiconductors, exists between the highest occupied

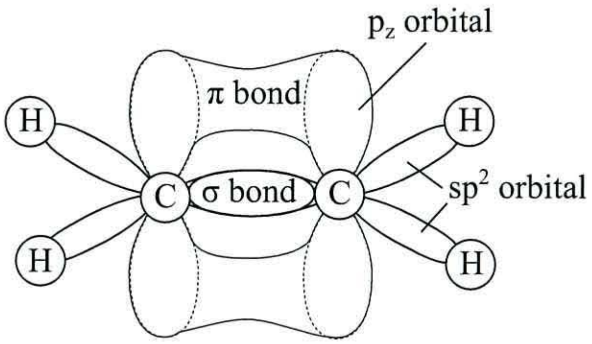


FIGURE 1.1: Bonding orbitals in ethene. The backbone consists of σ-bonds formed by the three sp^2 orbitals on each carbon atom. The π–bond is formed by overlap of the p_z orbitals.

molecular orbit (HOMO: corresponding to the valence band) and the lowest unoccupied molecular orbit (LUMO: the conduction band). Conjugated organic semiconductors have band gaps of ~1–4 eV [38], and electronic transitions readily occur between the HOMO and LUMO.

Charge injection, either by photo-excitation, via electrodes or by chemical doping, into the organic semiconductor produces deformations or defects in the polymer chain, and are known as polarons and bipolarons. The bond alternation surrounding the defect changes to reduce the overall energy of the chain, resulting in localized states in the band gap (Figure 1.2). If energetically favourable, two polarons may combine to form a bipolaron.

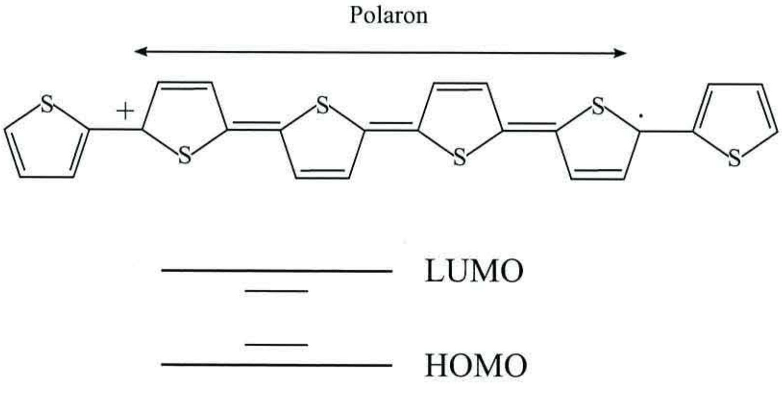


FIGURE 1.2: A polaron on a segment of polythiophene. Top shows deformation of the chain (Quinonoid structure), bottom shows localized states created by the polaron in the band gap. Adapted from [39].

Polymers are highly disordered; polymer chains, held together by weak Van der Waals forces, form molecular solids which tend to exhibit low mobilities

($< 10^{-3}$ cm^2/V s). Because of the structure of the polymer, charge is localized on each molecule with inter-molecular transport occurring via a hopping mechanism [39].

1.3 Photoelectric properties

As mentioned above, the band gap in organic semiconductors varies between 1–4 eV, thus they are able to absorb, or emit, photons of wavelengths in the range ~300–1500 nm, covering the electromagnetic spectrum from ultraviolet to infra-red.

In an inorganic semiconductor, if a photon with energy $h\nu$ (where ν is the frequency and h is Plancks constant) is absorbed by an electron in the valence band then it may be excited to the conduction band, provided $h\nu > E_g$ (where E_g is the energy band gap of the semiconductor) [40]. However in organic semiconductors the charge generated by photon excitation is a two part process as shown in Figure 1.3.

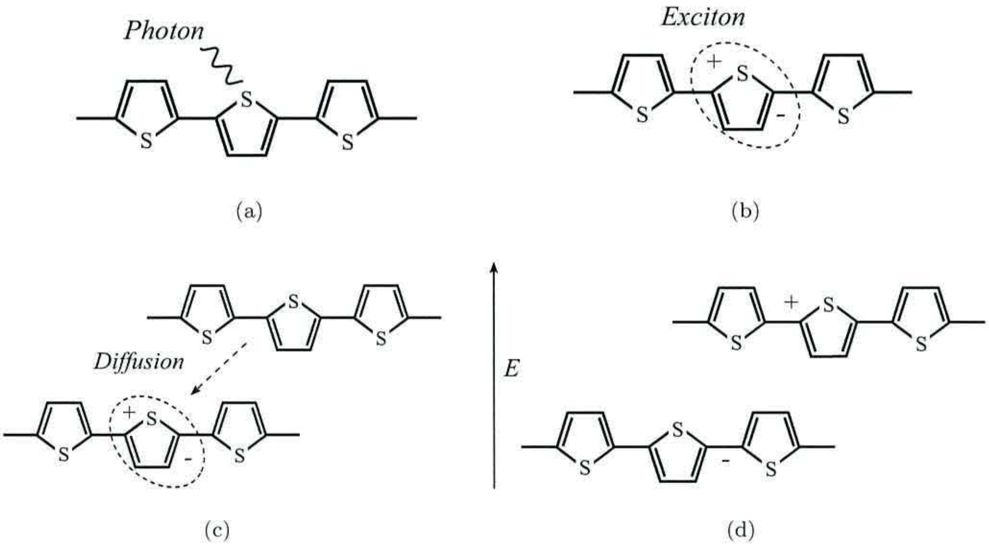


FIGURE 1.3: Exciton formation in an organic semiconductor. In (a) a photon is absorbed, (b) an exciton is formed. (c) shows the exciton diffusing to a molecule with lower energy and in (d) charge is transferred by application of an electric field. Adapted from [41].

When a photon is absorbed (Figure 1.3(a)) a strongly bound, due to Coulombic attraction, electron-hole pair called an *exciton* is created, which is localized on a molecule (Figure 1.3(b)). The excited state of the molecule is at a higher energy than its neighbours, and the exciton will diffuse toward a molecule at a lower energy (Figure 1.3(c)). Eventually the electron and hole will recombine. However, if the exciton is subjected to an electric field of sufficient strength to overcome the Coulombic binding energy, recombination is avoided, and the exciton separates enabling the electron and hole charges to contribute to the photo-current (Figure 1.3(d)).

Typically the exciton diffusion length ($L_D = \sqrt{\tau D}$ where τ is the exciton lifetime and D is the diffusion coefficient) is ~10 nm, thus requiring that for separation of excitons they must be formed within 10 nm of a region in which an electric field exists. This length is only ~10 % of the absorption length for photons in the semiconductor layer [39], consequently very little of the incident light would be converted to charge.

1.4 Organic Photo-Electronic Devices

Early organic photo-conductive devices such as photovoltaic cells (OPV) and photodiodes (OPD) were fabricated with a single organic layer between two metal electrodes. In 1986 Tang used two layers of different semiconductors where the charges were separated at the interface between them [42]. When semiconductors with different HOMO and LUMO energies are brought together heterojunctions are formed. The difference in HOMO and LUMO energy levels is sufficient to favour exciton separation at this junction (Figure 1.4). One semiconductor, known as the acceptor (A) has a high electron affinity, the other, having a high ionization potential is termed the donor (D).

Further improvements were made using spatially distributed blends of carefully chosen polymers producing bulk heterojunctions throughout the active region This allowed the semiconductor layer to be thick enough to absorb the incident light, with the photo-induced excitons being close enough to heterojunctions for charge separation. Following this approach enabled the conversion efficiencies of organic PVs to reach ~6.8 % [44]. Ideally the acceptor/donor mix should form an inter-digitated structure with a feature size of ~10 nm to enable efficient separation/dissociation of excitons (Figure 1.5). Where planar molecules are mixed a percolating path for charge transport is necessary, although

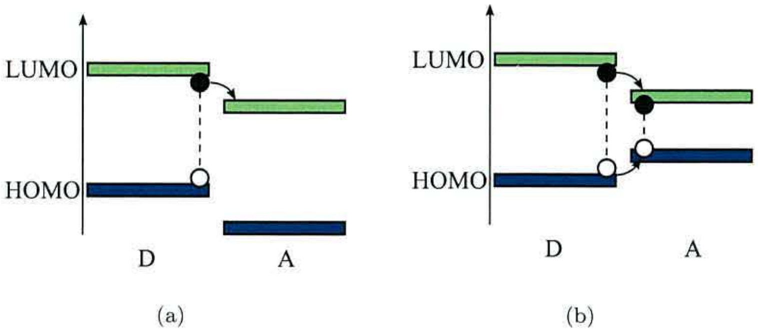


FIGURE 1.4: (a) Charge transfer at the acceptor (A) donor (D) interface occurs if the potential difference between the ionisation potential of the donor and electron affinity of the acceptor is greater than the exciton binding energy allowing the electron to jump from the LUMO of the donor to the LUMO of the acceptor and the hole remains in the donor material. (b) If the HOMO of the acceptor is higher than the donor then the bound electron and hole transfer to the acceptor. The dashed lines between electrons (•) and holes (○)represent excitons. Adapted from [43].

such pathways may not stretch across the entire film leading to electron-hole recombination. Percolating pathways can be formed by mixtures which phase separate into small domains during deposition, allowing efficient diffusion of excitons. By stacking two photovoltaic cells in series, researchers have developed so-called tandem cells. Cells with different energy gaps enable the tandem devices to absorb a wider range of the available spectrum [45].

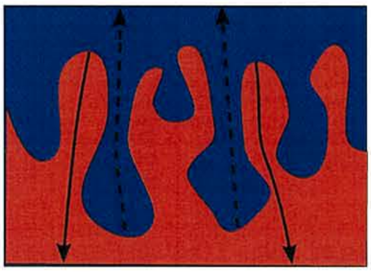


FIGURE 1.5: Charge transport in an ideal bulk heterojunction where the interdigitated donor (red) / acceptor (blue) structure has formed with feature sizes equivalent to the exciton diffusion length. The structure ensures good transport for both electrons (dotted lines) and holes (solid lines).

Organic photodiodes (OPD) are essentially the same as OPVs, but have a reverse bias applied. Similar methods to improve dissociation of photo-generated excitons have been applied, for example using acceptor/donor mixes [46]. The thin organic layers, typically $<\sim$200 nm in OPVs [47], necessary for optimizing efficiency result in high dark currents when reverse-biased. Dark current in OPDs has been reduced by using thicker films, up to 4 μm thick [48], which also ensures most of the incident light is absorbed in the active layer. These diodes require higher reverse biases to achieve efficient collection of photo-generated charges, however prolonged operation at high biases stresses the device causing a reduction in photo-current. Low noise OPD arrays fabricated on flexible substrates are suitable for use in conformal medical x-ray imaging devices [49]. OPDs have also been incorporated into large area image sensors [50, 51].

Illumination of OFETs with band gap light induces photo-generated charges in the channel, increasing the source-drain current [52, 53]. Pulsing the light on and off results in modulation of the drain current indicating that optical illumination can control the operation of OFETs. In some p-type semiconductors photo-induced electrons can become trapped at the semiconductor/insulator interface, effectively shifting the threshold voltage to more positive voltages resulting in a persistent photo-induced current [54, 55]. Relaxation of these trapped charges, in the dark, follows a decay which can be described either by a stretched exponential function (Kohlrausch's law) [54] or by a single exponential decay [56].

Bias-stressing of OFETs can also result in shifts of the threshold voltage. Mobile ions in the insulator cause the threshold voltage to shift in a direction opposite to the polarity of the applied gate voltage [57]. Defects, impurities and structural disorder in the semiconductor, either in the bulk or at the semiconductor/insulator interface act as traps, causing instabilities in the threshold voltage [58]. Charges trapped in shallow states recover quickly upon removal of the bias stress. Trap states deeper in the band gap take much longer to de-trap, with the decay tending to follow Kohlrausch's law [59].

Bias stressing of OFETs in the *on* state results in some of the majority carriers becoming trapped in interface states, and they no longer contribute to the current. To maintain the same source-drain current the gate bias must be increased. Stressing OFETs in the *off* state results in minority carrier trapping at the interface. For p-type materials electrons becoming trapped at the interface results in the threshold voltage shifting towards higher positive values, effectively ensuring a semi-permanent *on* state. Such shifts of the threshold voltage are detrimental to device performance. A detailed study by Veres *et al.* has shown that insulators with a high dielectric constant increase the disorder at the interface, reducing the performance of the semiconductor due to increased interfacial trap states [60].

Capacitance-voltage (C-V) plots of organic MIS capacitors under illumination result in large shifts of the C-V plot to more positive voltages [61, 62]. During a voltage sweep the devices are biased from the accumulation regime through to depletion. Little effect is seen for accumulation voltages, but as the device is biased into depletion photo-generated electrons become trapped at the semiconductor/insulator interface causing the flatband voltage to move to more positive voltages. Both the density and energetic depth of the interface traps were found to be dependent upon the insulator used [61]. A further effect on the photo–C-V plot was observed; the minimum capacitance in depletion was seen to increase and was associated with photo-generated electrons accumulating at the semiconductor surface.

MIS capacitors are the basic component of the ubiquitous charge-coupled-device (CCD), invented by Smith and Boyle [63], and used extensively in imaging arrays. MIS devices are simple structures, and the photo-response of organic semiconductors to visible light promotes the idea for an organic CCD, which have yet to be demonstrated.

1.5 Outline of the Thesis

This work is split into two parts. The main theme is an investigation into MIS based organic imaging systems including CCD and charge injection device (CID) structures. The response of these devices is dependent on the properties of the semiconductor/insulator interface. CCD's and CID's are both reliant on the transfer of charges between coupled MIS capacitors; a low density of traps and minimal disorder will allow efficient charge transfer. Admittance measurements are ideally suited to the characterisation of semiconductor/insulator interfaces [64] and are employed in this work.

The theoretical aspects relating to electrical and optical characterisation of MIS capacitors are presented in Chapter 2.

An overview of the organic materials and device fabrication is given in Chapter 3. This chapter also provides details of the experimental equipment used to characterise MIS devices.

Chapter 4 presents the experimental results obtained from admittance measurements of MIS devices in the dark and used for determining the stability and characteristics of the semiconductor/insulator interface.

The responses of MIS capacitors and a simple charge-coupled device to optical excitation are reported in Chapter 5. A simple model describing the photo-C-V response is also presented.

Chapter 6 is a stand-alone chapter which reports the results of a collaboration with The Soft Semiconductor Group at MIT and forms the second part of this thesis. It provides details of a near-field surface plasmon bio-sensor in which the optical detector had been replaced with an organic photovoltaic cell.

The main conclusions drawn from this work, together with suggestions for further investigations are given in Chapter 7.

Chapter 2

Literature Review

2.1 Introduction

Metal Insulator Semiconductor (MIS) capacitors provide the basis for many different types of electronic devices from field-effect transistors to charge-coupled devices. Because of their simple device structure, they have been widely used in the analysis of the electrical and interfacial properties of the MIS system. For example, the use of Metal Oxide Semiconductor (MOS) capacitors as analytical tools has proven to be beneficial in the understanding and improvement of silicon based devices. Consequently, the physics of MIS capacitors was essentially developed for inorganic semiconductors as explained in several text books [40, 64, 65].

Similar studies of MIS capacitors with organic semiconductors are also beneficial in the further understanding of the interfacial properties of the active material and insulator layer. This chapter reviews the theory and characterisation relating to MIS capacitors in the dark and under illumination. Theoretical aspects of charge-coupled-devices and charge-injection-devices is also included.

2.2 The Metal Insulator Capacitor

The MIS capacitor structure (Figure 2.1) is similar to the familiar parallel plate capacitor in which a dielectric layer separates two electrodes or plates. In the MIS system, however, one electrode, the gate, is metallic and the other is the semiconductor. For electrical connectivity an ohmic contact is made with the semiconductor. Varying the voltage applied to the gate modulates the population of charges within the semiconductor layer, altering its conductivity, and the overall capacitance of the MIS device.

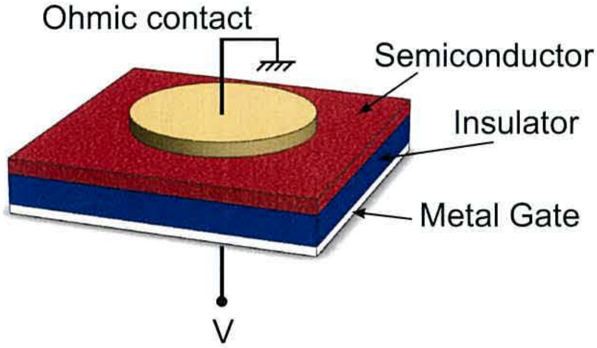


FIGURE 2.1: Thin-film MIS capacitor. A voltage, V, applied to the gate electrode determines the population of charge carriers in the semiconductor, and, consequently, the overall capacitance of the MIS capacitor.

2.2.1 Ideal MIS Capacitor Energy Band Diagrams

Although molecular organic crystals have been shown to exhibit band-like transport at low temperatures [66], the high degree of disorder in polymeric semiconductors results in hopping transport between localized states. Models describing charge transport in disordered organic semiconductors assume either a Gaussian or an exponential density of states (DOS) [67, 68] rather than the parabolic DOS associated with crystalline silicon. Figure 2.2 shows an energy diagram for a disordered semiconductor with a Gaussian density of states.

For organic materials containing impurities Fermi level alignment, leading to band-bending, is possible, although this occurs within the context of an exponential or Gaussian DOS [70].

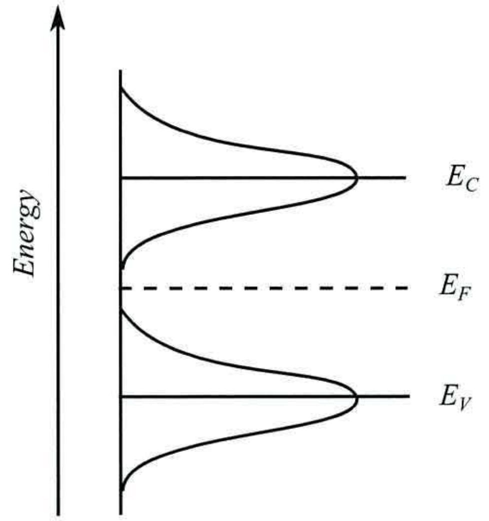


FIGURE 2.2: Energy diagram for a Gaussian DOS in a disordered organic semiconductor. Adapted from [69].

However, in the following sections, band diagrams based on conventional semiconductors are used as the basis for explaining the operating regimes of MIS capacitors.

2.2.1.1 Flatband

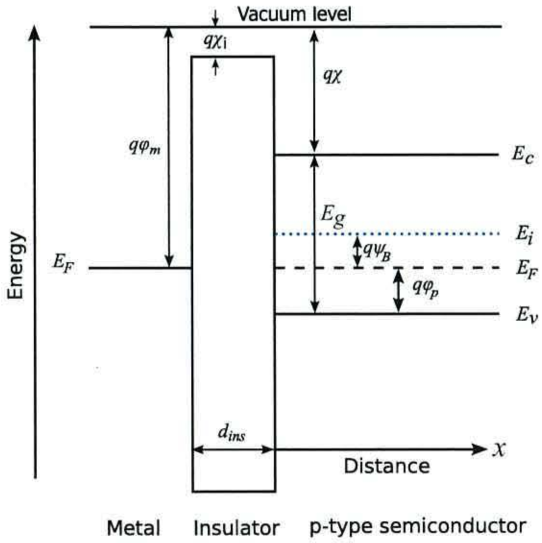


FIGURE 2.3: Energy band diagram of an ideal p-type MIS capacitor at flatband with $V = 0$.

The energy band diagram for an ideal MIS capacitor with no applied bias ($V = 0$), in thermal equilibrium, is shown in Figure 2.3. An ideal MIS device is one in which there are no interface traps or fixed charges in the insulator, the insulator has infinite resistance, and there is no difference in the work function of the metal gate and the semiconductor. From Figure 2.3 it can be deduced that [40]

$$\phi_{ms} \equiv \phi_m - (\chi + \frac{E_g}{2q} + \psi_B) \tag{2.1a}$$

$$= \phi_m - (\chi + \frac{E_g}{q} - \phi_p) = 0 \tag{2.1b}$$

where χ represents the electron affinity of the semiconductor, ψ_B is the Fermi potential with respect to the midgap, E_i, and ϕ_p is the Fermi potential with respect to the band edge E_v. As can be seen the bands are flat, and this is known as the flatband condition.

The insulator presents a large energy barrier between the metal and semiconductor, preventing conduction of carriers through the device. Because no current can flow through the device, a bias applied to the gate electrode results in surface charge layers in the metal and semiconductor, producing an electric field in the insulator.

2.2.1.2 Accumulation

Biasing a p-type semiconductor with a negative voltage applied to the gate ($V < 0$) causes the valence band edge, E_v, to bend upwards at the surface bringing it closer to the Fermi level (Figure 2.4). As the concentration of carriers at the surface depends exponentially on the band-bending, this results in an accumulation of majority carriers (holes) near the surface. The accumulation layer screens the bulk semiconductor from the applied electric field with band-bending increasing for higher accumulation voltages.

In the energy band diagram of Figure 2.4 ψ_s is defined as the total band-bending or surface potential with respect to the bulk of the semiconductor. It is the potential difference between φ_B and φ_s. φ_B is the potential difference between the intrinsic Fermi level E_i and the doped Fermi level E_F in the bulk, and φ_s is the difference in potentials between E_i and E_F at the semiconductor surface. The potential at a distance x from the surface is then

$$\psi(x) = \varphi(x) - \varphi_B = \frac{E_i(x) - E_i(\infty)}{q}. \tag{2.2}$$

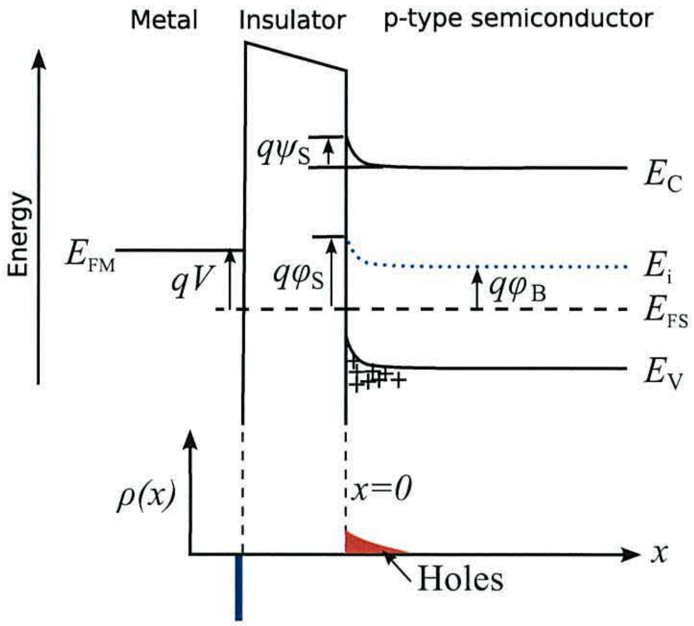


FIGURE 2.4: Energy band and charge distribution diagrams of an ideal p-type MIS capacitor biased in accumulation, $V < 0$. Upward arrows denote negative potentials, downward arrows denote positive potentials.

The concentrations of holes as a function of $\psi(x)$ is given as [40]

$$p(x) = N_A exp\left[-\frac{q\psi(x)}{kT}\right], \tag{2.3}$$

where k is Boltzmann's constant, T is the absolute temperature and N_A is the density of acceptors. Thus in accumulation the density of holes at the surface is $p(x) > N_A$.

2.2.1.3 Depletion

If the applied bias is now increased such that it has a small positive value ($V > 0$), the bands bend down resulting in a reduction in the concentration of majority carriers near the interface: a condition known as depletion (Figure 2.5).

Charge neutrality is maintained by a space charge region of negatively charged acceptors in the depletion layer. The depletion width, w, increases with increasing gate bias such that charge neutrality is maintained overall in the device. The transition between the depletion edge and bulk semiconductor occurs over a Debye length. However in the *depletion approximation* this is approximated as a step function, where the free carrier concentration is $p = n = 0$ in the depletion region and charge neutrality is maintained in the bulk semiconductor. The surface

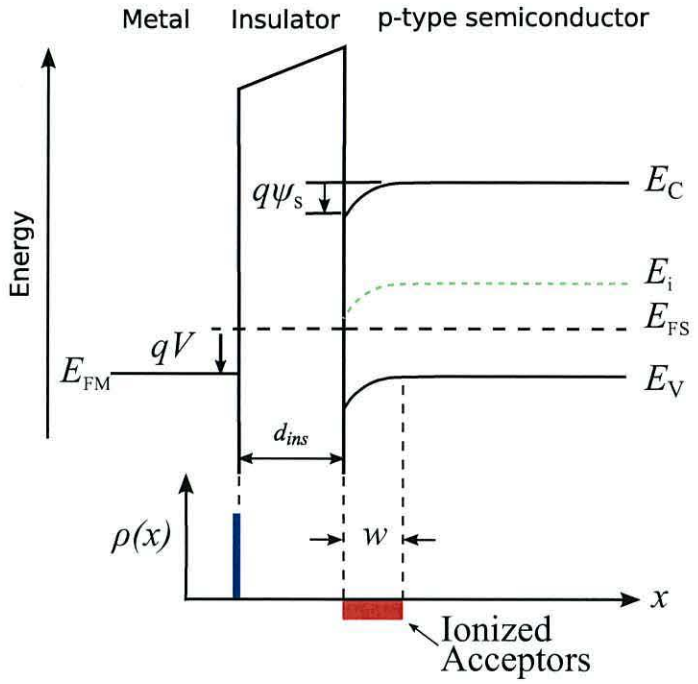


FIGURE 2.5: Energy band and charge distribution diagrams for an ideal *p*-type MIS capacitor biased in depletion. Application of a small positive voltage ($V > 0$ causes the bands to bend down and the surface is depleted of majority carriers. Charge neutrality is maintained by ionized acceptors.

charge in the depletion region is

$$Q_s = -qN_A w, \tag{2.4}$$

from which the electric field E_S in the semiconductor layer is

$$E_S = \frac{qN_A w}{\varepsilon_s}, \tag{2.5}$$

where ε_s is the absolute permittivity of the semiconductor. Integrating the electric field provides the potential at the surface of the semiconductor, ψ_s

$$\psi_s = \frac{qN_A w^2}{2\varepsilon_s}. \tag{2.6}$$

It is apparent from Figure 2.5 that the applied voltage V appears across both the insulator and semiconductor, i.e.

$$V = V_I + \psi_s, \tag{2.7}$$

where

$$V_I = \frac{Q_s}{C_i} \tag{2.8}$$

and C_i is the capacitance per unit area of the insulator. Combining Equations 2.6, 2.7 and 2.8 results in a quadratic expression for the depletion width, whose solution is

$$w = -\frac{\varepsilon_s}{C_i} + \sqrt{\frac{\varepsilon_s^2}{C_i^2} - \frac{2\varepsilon_s V}{qN_A}}. \tag{2.9}$$

If the bias is now made much more positive, the bands bend further downward and the intrinsic Fermi level, E_i, crosses the Fermi level, E_{FS}. Now the concentration of minority carriers (electrons) at the surface can become greater than that of holes in the bulk so that the surface becomes inverted. Minority carriers help maintain charge neutrality in the MIS capacitor, and shield the depletion layer from further penetration of the applied electric field. In organic semiconductors, however, inversion is not commonly observed although in intrinsic ambipolar materials electron accumulation is observed for positive gate voltages [34].

2.2.2 Admittance of MIS Capacitors

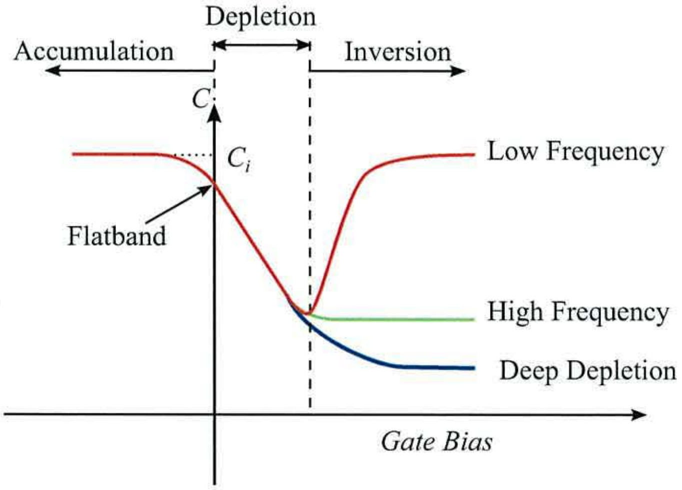


FIGURE 2.6: *C-V* response of an ideal MIS capacitor at low frequencies (red curve). At high frequencies (green curve) minority carriers can only respond to slow changes in the gate bias and the MIS capacitor realises a minimum capacitance at the bottom of the transition from accumulation to depletion. When minority carriers are unable to respond to changes in the gate bias the device enters deep depletion (blue curve).

When an ac voltage is superimposed upon the gate voltage of an MIS device, biased in the accumulation regime, the band-bending will vary with time as it follows the applied ac voltage. To maintain equilibrium, charges will flow in and out of the semiconductor surface. Under strong accumulation the density of holes at the surface is contained within a very thin layer, creating a large differential capacitance, C_s, in the semiconductor. As $C_s \gg C_i$ the measured capacitance per unit area, $C_m \approx C_i$ (Figure 2.6). At frequencies where the device is able to follow the ac voltage C_m can be modelled as a parallel plate capacitor with its capacitance per unit area given by

$$C_m = \frac{\varepsilon_i}{d_i} \tag{2.10}$$

where ε_i is the absolute permittivity of the insulator and d_i its thickness.

Driving the gate bias to more positive voltages, reduces the density of holes at the surface, decreasing the value of C_s. When the bias is greater than the flatband voltage, holes are repelled from the surface, forming a depletion layer of ionized acceptors with an associated depletion capacitance per unit area, C_d. The total measured capacitance per unit area decreases and is the series sum of C_i and C_d given by

$$\frac{1}{C_m} = \frac{1}{C_i} + \frac{1}{C_d}. \tag{2.11}$$

As the depletion layer width increases, C_d decreases in value. The minimum value of C_m coincides with the minimum value of C_d where the depletion layer width is at its maximum.

In silicon an inversion layer of minority carriers forms as the bias is further increased. Response time for minority carriers in silicon is ~0.01–1 seconds and, provided the frequency is low enough (< 100 Hz), minority carriers can follow the ac signal [64]. The differential capacitance of the inversion layer increases with bias and eventually exceeds C_i so that $C_m \approx C_i$ (red curve in Figure 2.6). At high frequencies, minority carriers are unable to respond to the ac voltage, but can still follow slow changes in gate bias. Consequently the minority carriers screen the semiconductor bulk from further increases in gate bias and C_m remains at its minimum value (green curve in Figure 2.6). If the response time of minority carriers is too slow to even follow changes in the gate bias, the depletion region continues to grow until it fills the entire semiconductor bulk. The MIS capacitor is now in deep depletion (blue curve in Figure 2.6).

Generation of minority carriers in wide band gap organic semiconductors is very inefficient, with a response time $\sim 10^7$ seconds due to the low intrinsic carrier density [71, 72]. Therefore inversion is not observable in organic MIS capacitors, even at the lowest measurable frequencies ($\sim 10^{-3}$ Hz), and C-V curves obtained for organic MIS capacitors resemble the deep depletion curves of inorganic devices, with the semiconductor layer becoming fully depleted of charge, where C_m becomes constant.

From the above discussion it is seen that C_d is bias dependent and the MIS device can simply be represented as a variable capacitor in series with the insulator capacitance C_i (Figure 2.7).

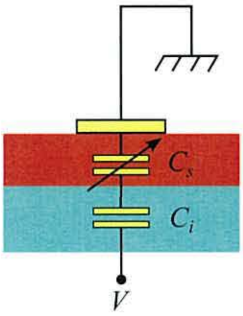


FIGURE 2.7: Simple equivalent circuit of a MIS capacitor showing series connection of the insulator (C_i) and semiconductor (C_s) capacitances. C_s is variable to indicate its bias dependence.

2.2.3 Doping Density

The doping density of doped organic semiconducting materials may be found by following the Mott-Schottky analysis. However, as noted by Meijer *et al.* [73], the temperature and frequency ranges over which the doping density can be determined is limited due to the low response time of majority carriers . Following the standard Mott-Schottky analysis the doping density profile ($N(w)$) may be obtained using the equation [64]

$$N(w) = -2\left[q\varepsilon_s \frac{d}{dV_G}(\frac{1}{C_m})^2\right]^{-1}, \tag{2.12}$$

where w is the depletion layer width, q is the elementary charge, ε_s the absolute permittivity of the semiconductor, and C_m is the measured capacitance per unit area at a gate bias V_G. Doping density can then be found from the slope of a plot of $1/C_m^2$ versus V_G in depletion. A positive slope of the plot indicates the dopants are acceptors, a negative slope indicates they are donors. A uniform distribution of dopants results in a straight line with slope proportional to $N(w)$. For a non-constant doping density, the profile as a function of w may be obtained by calculating $N(w)$ at each value of V_G using Equation 2.12. The corresponding value of w can be found using the expression

$$w = \varepsilon_s \left(\frac{1}{C_m} - \frac{1}{C_i} \right). \tag{2.13}$$

2.2.4 Equivalent Circuits of MIS Capacitors

Equivalent circuits provide a means to model the behaviour of MIS capacitors. In the previous section a simple series arrangement of capacitors was shown to model the device, with the assumption that the majority carriers are able to follow the ac voltage. However, this is only true when the period of the applied ac signal is much longer than the dielectric relaxation time of the semiconductor τ_D. At higher frequencies where the majority carriers can no longer respond, thermal equilibrium is not maintained resulting in an energy loss supplied by the ac voltage source. This loss is modelled by an R-C time constant where the loss occurs in the resistive element. Figure 2.8 shows the equivalent circuit for the MIS capacitor in accumulation where the bulk semiconductor capacitance C_B is in parallel with the bulk resistance R_B [73].

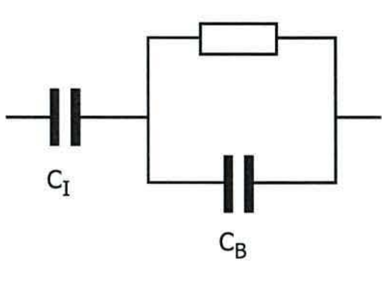


FIGURE 2.8: Equivalent circuit for a MIS capacitor in accumulation.

The measured admittance, Y_M, of the MIS capacitor is

$$Y_M = G_M + j\omega C_M \tag{2.14}$$

where G_M and C_M are the parallel conductance and capacitance respectively and $j = \sqrt{-1}$. From Figure 2.8 and Equation 2.14 the capacitance C_M and loss G_M/ω are given as [74]

$$C_M = C_G + \frac{C_I - C_G}{1 + (\omega\tau_R)^2} \tag{2.15a}$$

$$\frac{G_M}{\omega} = \frac{\omega R_B C_I^2}{1 + (\omega\tau_R)^2} \tag{2.15b}$$

where C_G is the series sum of the insulator capacitance, C_I, and C_B, and τ_R is the circuit relaxation time given by

$$\tau_R = R_B(C_I + C_B), \tag{2.16}$$

from which the relaxation frequency is

$$f_R = \frac{1}{2\pi R_B(C_I + C_B)}. \tag{2.17}$$

Equation 2.17 is valid for a MIS capacitor in accumulation. When the device is biased into depletion a capacitance C_D associated with the depletion layer width, x_d, must be included in the equivalent circuit as in Figure 2.9.

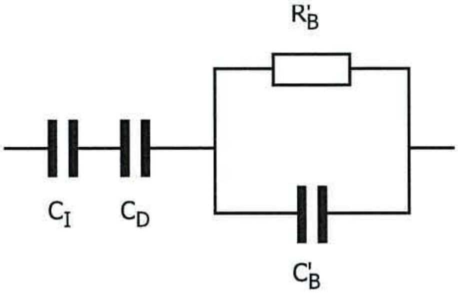


FIGURE 2.9: Equivalent circuit for a MIS capacitor in depletion.

The depletion width, and hence C_D, C_B and R_B, are all bias dependent, and are given by the following equations [75]

$$R'_B = \rho_s \frac{L - x_d}{A} \tag{2.18a}$$

$$C'_B = \varepsilon_s \frac{A}{L - x_d} \tag{2.18b}$$

$$C_D = \frac{\varepsilon_s A}{x_d} \tag{2.18c}$$

where L is the semiconductor thickness and ρ_s the semiconductor resistivity.

The relaxation frequency can now be calculated as

$$f_R = \frac{1}{2\pi R'_B(C'_I + C'_B)}, \tag{2.19}$$

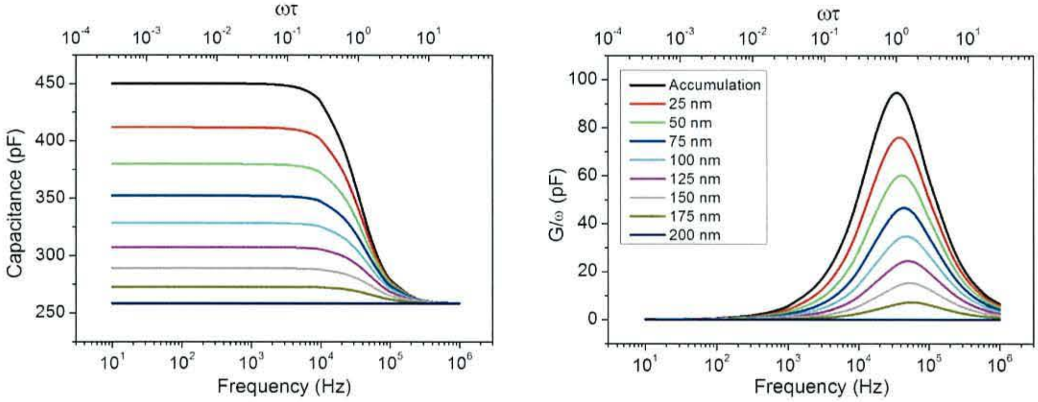
where C_I has been replaced by the series sum (C'_I) of C_I and C_D, and C_B and R_B replaced with C'_B and R'_B respectively.

As the depletion region grows the relaxation frequency will increase between the value in accumulation and full depletion [75]

$$\frac{1}{2\pi R_B(C_I + C_B)} < f_R < \frac{1}{2\pi R'_B C'_B} = \frac{1}{2\pi \tau_D} \tag{2.20}$$

where $\tau_D = \rho_s \varepsilon_s$ is the relaxation time of the undepleted semiconductor.

The effect on the capacitance and loss as a function of frequency and depletion width are simulated in Figure 2.10 using Equation 2.19. The black curve in



(a)

(b)

FIGURE 2.10: Simulated frequency response of (a) capacitance and (b) loss of a MIS capacitor as it is biased from accumulation to full depletion. Semiconductor layer thickness is 200 nm with C_I = 450 pF, C_B = 600 pF and R_B = 4400 Ω.

Figure 2.10(a) shows the frequency response of the MIS capacitor when biased in the accumulation regime. For frequencies where $\omega\tau_R \ll 1$ the total measured capacitance $C_M \approx C_I$ because the reactance ($X_{C_B} = 1/j\omega C_B$) of C_B is high and shunted by the semiconductor bulk resistance R_B. X_{C_B} decreases with increasing frequency and makes an increasing contribution to the admittance. As the frequency approaches the relaxation frequency, f_R (Equation 2.17), X_{C_B}

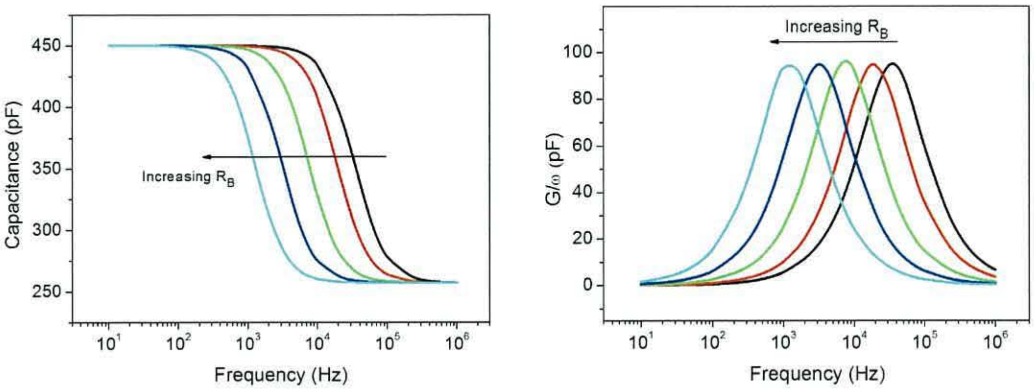
decreases and is no longer shunted by R_B. Consequently C_B is now in series with C_I and C_M decreases with increasing frequency.

The corresponding loss plot (black curve in Figure 2.10(b)) reveals a classical Maxwell-Wagner dispersion, typical of a two layer dielectric structure where the layers have different conductivities [76]. At low frequencies majority carriers respond to the ac signal and there is no associated energy loss. As the frequency increases majority carriers lag behind the ac voltage and the loss increases until a maximum occurs at $\omega\tau_R = 1$. At higher frequencies majority carriers are unable to respond to the signal and make no contribution to the energy loss, which decreases. At frequencies where $\omega\tau_R \gg 1$ none of the majority carriers are able to follow the ac voltage and there is no energy loss from the majority carriers.

As the depletion layer width grows, the low frequency capacitance decreases with C_D becoming increasingly influential (see Figure 2.10(a)). When the semiconductor is fully depleted the measured capacitance remains at the geometric capacitance of C_I in series with C_D over the whole frequency range (dark blue curve in Figure 2.10(a)). Both the C-f and G/ω-f plots show the relaxation frequency increasing with depletion layer width, as predicted by Equation 2.20.

The preceding analysis relates to doped semiconductors in which a depletion layer forms in the semiconductor adjacent to the insulator when suitably biased. However, if depletion voltages only reduce the free charge carrier concentration in the bulk semiconductor and there is no depletion region, the bulk resistivity will increase and both C_I and C_B will remain constant. Analysis of Equation 2.17 reveals that as R_B increases f_R shifts to lower frequencies as plotted in Figure 2.11. In contrast to a semiconductor where a depletion region exists, there is no decrease in the low frequency capacitance or loss peak with further increases in depletion bias.

The relaxation frequency associated with the circuit in Figure 2.8 implies that all the majority charge carriers have a single relaxation time (τ_R). However, the hopping nature of thermally activated charge transport in organic semiconductors emanates from structural disorder. This results in a dispersion of majority carrier response times to an ac voltage, so that the experimental Maxwell-Wagner dispersion is much broader and lower than modelled in Figure 2.10 but still centred around τ_R. Cole and Cole introduced a complex impedance to model the distribution of relaxation times in dielectrics [77]. Torres applied this model



(a) (b)

FIGURE 2.11: Frequency dependency of (a) capacitance and (b) loss for a MIS capacitor where 'depletion' voltages only reduce the free carrier concentration. Simulated with $C_I = 450$ pF, $C_B = 600$ pF and R_B increases from $4 \times 10^3\ \Omega$ (black) to $1 \times 10^8\ \Omega$ (cyan).

to the broad dispersions seen in organic semiconductors, where the equivalent circuit of Figure 2.8 was replaced by that shown in Figure 2.12 [78]. C_1, C_2 and

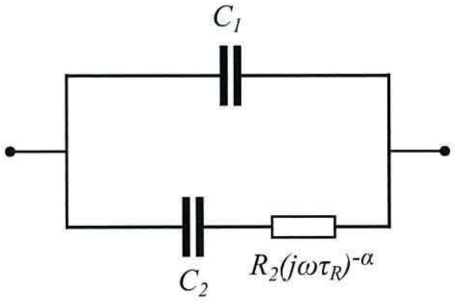


FIGURE 2.12: Modified equivalent circuit for MIS capacitor to account for time constant dispersion.

R_2 in Figure 2.12 are related to C_I, C_B and R_B by equations [78]

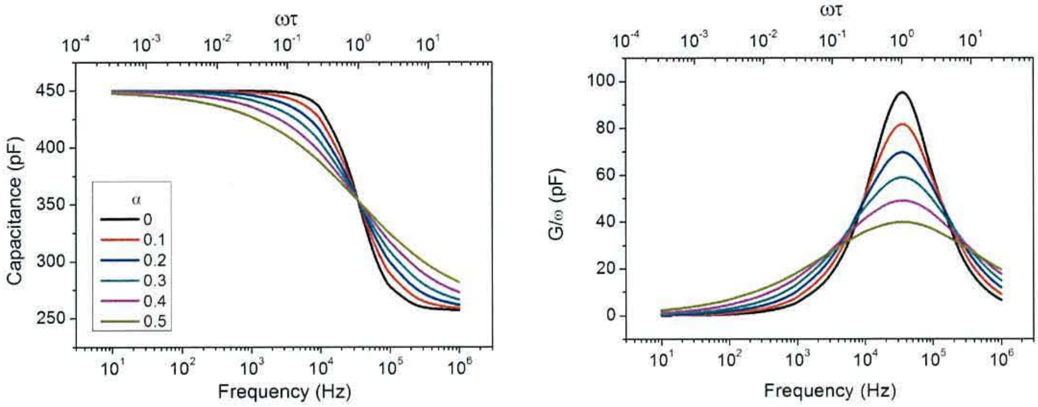
$$C_1 = \frac{C_I C_B}{C_I + C_B} \tag{2.21a}$$

$$C_2 = \frac{C_I^2}{C_I + C_B} \tag{2.21b}$$

$$R_2 = \frac{R_B(C_I + C_B)^2}{C_I^2} \tag{2.21c}$$

and $0 < \alpha < 1$ is a fitting parameter.

Figures 2.13(a) and 2.13(b) illustrate the effects of time constant dispersion on the C-f and G/ω-f plots with different values of α. As α increases, the loss peak clearly reduces in magnitude and the dispersion broadens. Concomitantly the transition slope in the C-f curve stretches out.



(a) (b)

FIGURE 2.13: Simulated frequency response of (a) capacitance and (b) loss of a MIS capacitor in accumulation for different values of α. When $\alpha = 0$ there is no time constant dispersion and the circuit reverts to Figure 2.8.

Bulk resistance can be determined using Equation 2.17 from the relaxation frequency measured with the MIS capacitor in accumulation. Bulk conductivity, σ_B, can then be determined using the equation

$$\sigma_B = \frac{L}{R_B A}. \tag{2.22}$$

If the doping density (N_A) has been found from C-V measurements (Equation 2.12), the bulk mobility can be calculated, since

$$\mu_B = \frac{\sigma_B}{q N_A}. \tag{2.23}$$

This method has been used by various workers to determine the temperature dependence of conductivity in MIS capacitors. Measurements made over a range of temperatures allow the extraction of activation energies for thermally activated conductivity and mobility of organic semiconductors [73, 79, 80]. Lada found a transition in an Arrhenius plot of the conductivity of P3HT based devices which was attributed to a phase transition in the semiconductor [81]. Deviations from Arrhenius behaviour have also been reported for P3HT and polyarylamine transistors and ascribed to water related traps [82]. Extraction of the bulk mobility from admittance measurements has been used to monitor the effect of annealing on P3HT MIS capacitors [75].

2.3 Real MIS Capacitors

The previous section introduced the basis for the characterisation of MIS capacitors. The deviation of real devices from the ideal behaviour provides an insight into the various factors which affect device performance. Such factors include trapped charges and work function differences. Charges may be trapped within the insulator, bulk semiconductor, or at the interface between them, all of which affect the measured admittance. Further problems arise from work function differences, lateral conduction and contact resistance.

2.3.1 Flatband Voltage

In an ideal MIS capacitor the work function difference, φ_{ms}, is assumed to be zero and there are no charges present in the insulator. The flatband voltage, V_{FB}, is also zero. A non-zero value of φ_{ms} results in a shift of the experimental C-V plot from the ideal value by φ_{ms}. Similarly any charges, Q_i (in Coulombs per unit area), present in the insulator will cause a shift along the voltage axis dependent upon the polarity of charge present. For example, in a p-type MIS device, negative Q_i results in a shift of V_{FB} to higher positive bias. This is because negative charges in the insulator will screen some of the positive charges on the gate when the device is biased into depletion, effectively reducing the depletion layer width. The polarity of charges in the insulator can therefore be deduced from the direction of the shift of the C-V curve from its ideal location. The total shift in flatband voltage is

$$\Delta V_{FB} = \varphi_{ms} - \frac{Q_i}{C_i}, \tag{2.24}$$

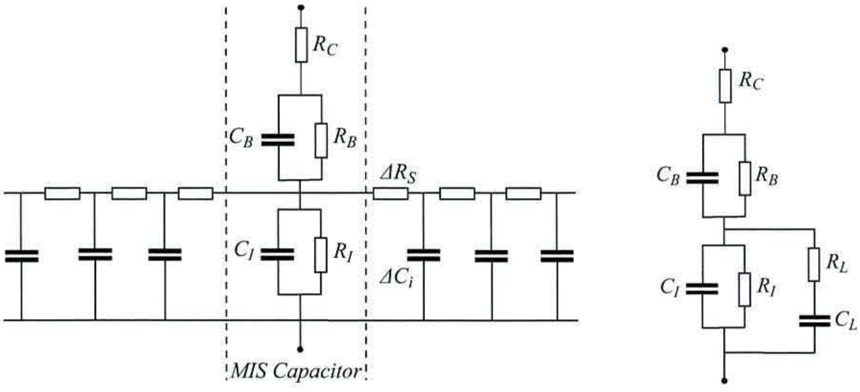
where C_i is the insulator capacitance per unit area.

As organic MISFETs mostly operate in the accumulation regime, the turn-on or threshold voltage of these devices has been defined as the flatband voltage [83]. Instabilities in flatband voltage result in unreliable transistor operation, and may be caused, for example, by charge trapping at the interface or in the insulator [62, 84] or by mobile ions in the insulator [80]. However, the ability to control the threshold voltage in MISFETS allows 'pseudo-complementary metal-oxide semiconductor circuits' to be fabricated using single carrier organic transistors

[85]. C-V measurements are an effective way to study the stability, and effect of setting, V_{FB} in organic MIS devices.

2.3.2 Lateral Conduction

Fabrication of organic MIS devices generally results in semiconductor layers which extend beyond the perimeter of the electrodes. Also the gate electrode is either not patterned or its area is greater than the ohmic top contact. Biasing such devices in the accumulation regime results in the accumulation layer extending beyond the periphery of the defining contact [86, 87]. Such effects can be modelled as a distributed R–C network as shown in Figure 2.14(a), where R_S is the sheet resistance ($\Omega/\square$) of the semiconductor and C_i is the insulator capacitance per unit area [87]. The R–C network can be approximated by the simplified circuit in Figure 2.14(b) [81].



(a) (b)

FIGURE 2.14: (a) Equivalent circuit of MIS capacitor with a distributed R–C network due to excess semiconductor surrounding the top electrode. (b) Simplified circuit where the distributed R–C network is replaced by R_L and C_L.

When a device is biased in accumulation the resistive elements are low in value and ac currents can flow laterally beyond the top contact, effectively increasing the device area [88]. At low frequencies, holes accumulated in this region can respond to the ac signal and the measured capacitance and loss both increase. As the frequency increases the contribution of the peripheral region to the total measured capacitance diminishes, and $C_M \approx C_I$ when the ac current no longer flows into the R–C network. When the device is partially depleted the semiconductor layer is much more resistive, consequently only a reduced current flows beyond the patterned electrode, and there is little effect on the admittance.

Note the equivalent circuits also include additional elements R_C and R_I. R_C represents the series resistance arising from contact effects at the gate and top electrodes. The presence of R_C gives rise to a dispersion in the frequency response at a relaxation frequency given by

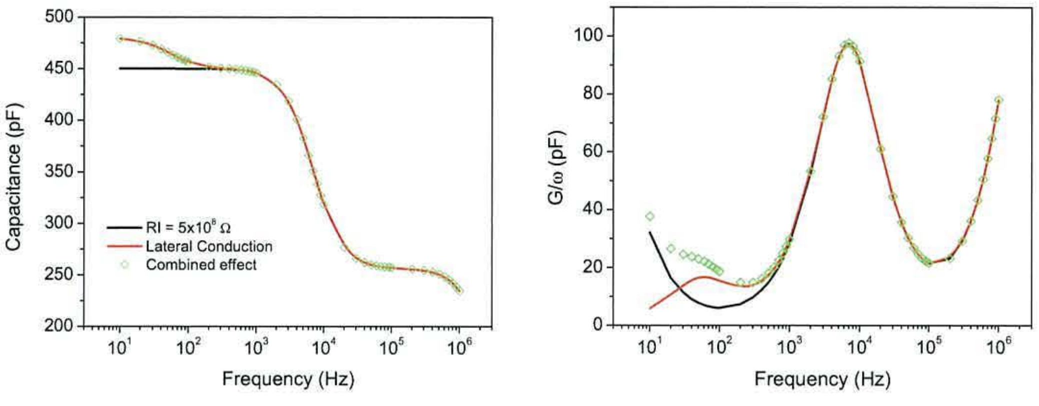
$$f_R = \frac{1}{2\pi R_C C_S}, \tag{2.25}$$

where C_S is the series sum of C_I, C_B and C_D [75, 81, 87].

R_I in Figure 2.14 represents the finite resistance of the insulator. Normally $R_I \gg R_B$ and its effect on the MIS capacitor admittance can be ignored. However, where the insulators are *leaky*, the loss at low frequencies, especially with the MIS capacitor biased in accumulation, can be very high.

Figure 2.15 shows the effects of lateral conduction, contact resistance and insulator resistance on the frequency response of a MIS capacitor. R_I can be seen to mainly affect the loss plot at low frequencies (black lines), but has little effect on the capacitance. Lateral conduction (red lines) clearly increases the capacitance with a corresponding dispersion at low frequencies in the loss. The green curves in the figures show the combined effects of lateral conduction and the insulator resistance. A contact resistance, present in all plots, of 200 Ω causes the high frequency capacitance to fall, and the associated loss to peak at a frequency $\gg$ 1 MHz. As all these dispersions are well separated they have negligible effect on the main Maxwell-Wagner dispersion at ~7 kHz.

To avoid cross-talk in organic circuits various techniques have been used to pattern the organic semiconductor in an effort to reduce or eliminate lateral conduction between active devices. These include photo-lithographic patterning [89], photo-bleaching [88], evaporation through shadow masks [90], inkjet printing [91] and micro-contact printing [92]. Guard rings have been shown to be effective in reducing lateral conduction in organic MIS capacitors [75]. By keeping the guard ring, which surrounds the ohmic contact, at the same potential as the ohmic contact no current can flow between them. Therefore the effect of lateral conduction is minimized. This technique, though, has been shown to introduce a parasitic field-effect transistor into the structure [74]. The gap between the guard ring and ohmic contact form the channel of the transistor, which, similarly to



(a) (b)

FIGURE 2.15: Effects of lateral conduction (red line), insulator resistance (black line) and contact resistance (all curves) on the frequency dependence of (a) capacitance and (b) loss of a MIS capacitor in accumulation. Frequency response simulated from the equivalent circuit of Figure 2.14(b) with $C_I = 450$ pF, $R_I = 5 \times 10^8\,\Omega$, $C_B = 600$ pF, $R_B = 22$ kΩ, $R_L = 1 \times 10^8\,\Omega$, $C_L = 25$ pF and $R_C = 200\,\Omega$.

the un-patterned device, can be represented by a distributed *R*-*C* network at accumulation voltages [74]. Experimental results revealed two loss peaks in the loss-voltage curve; the first occurring at accumulation voltages, and the second when the device was driven into depletion. Although these peaks were originally attributed to two separate distributions of interface states [75], it was later found that the one appearing in accumulation was caused by a contribution to the admittance from the parasitic transistor [74].

2.3.3 Bulk Trap States

Bulk trap states refer to those charges trapped in the semiconductor bulk, with one or more energy levels in the bandgap. In silicon, bulk traps are efficient recombination-generation centres for mobile carriers. Alternate emission of electrons and holes (generation) and alternate capture of electrons and holes (recombination) by bulk traps are the processes by which semiconductors regain equilibrium after a disturbance has been applied [64]. Bulk traps arise from impurities or structural defects in the bulk semiconductor.

Bulk traps will only contribute to the admittance if the trap energy level is within a few kT/q of Fermi level, where carriers interacting with trap states lag the ac voltage. In silicon bulk traps located near midgap act as the most efficient centres for the generation/recombination of mobile carriers, and their influence on the admittance is seen in inversion. However, bulk traps close to the Fermi level, located closer to the band edges, will contribute to the admittance with the device biased in depletion [93].

In organic devices bulk traps are usually located at the band edges [94]. Simulations by Scheinert *et al.* show that recharging of bulk traps can lead to degradation of the sub-threshold slope in transfer characteristics of OFETs [95, 96]. They also show that these traps are located near to the valence band.

Figure 2.17 shows the energy band diagram for a p-type MIS capacitor in depletion with a depletion width w. The Fermi level, E_F, crosses the bulk trap level, E_T, a distance x_c from the semiconductor/insulator interface and l from the depletion layer edge. Bulk traps located at x_c, within a few kT/q of E_F, respond to the ac gate voltage, and contribute to the measured admittance.

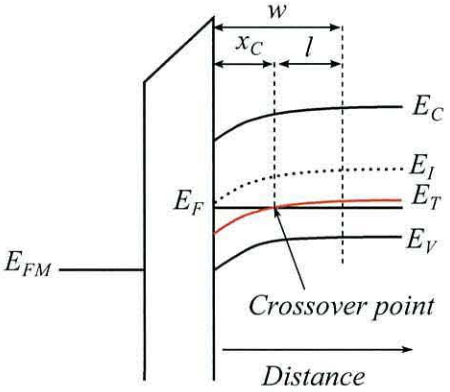


FIGURE 2.16: Energy band diagram of a p-type MIS capacitor biased in depletion with a bulk trap energy level, E_T (red line). The arrow indicates the *crossover point* where the Fermi level, E_F, and E_T coincide.

Interestingly, as the bias voltage is increased, such that the MIS capacitor is driven further into depletion, x_c moves further away from the interface, but the distance from x_c to the depletion edge, l, remains constant. Thus the crossover point is always at the same energy level. Because the crossover point is always at the same energy, the majority charge density is constant and independent of gate voltage. As the time constant associated with bulk traps is proportional to the majority charge density, the bulk trap loss will peak at the same frequency irrespective of the gate voltage [93]. However, the magnitude of the loss peak will be dependent upon gate bias if the distribution of bulk states is not uniform.

Bulk states are modelled within the framework of Shockley-Read-Hall (SRH) statistics. This requires that: (1) bulk traps may only change occupancy by one unit of charge, (2) each trap has only one energy level which is independent of occupancy, and (3) capture of charge is instantaneous [64].

Following Nicollian and Brews, the hole capture, r_c and emission rates, r_e, are proportional to the concentrations of holes $p(x,t)$ and bulk traps, n_T, and the occupancy of states $f(x,t)$ through the equations [64]

$$r_c(x,t) = c_p p(x,t) n_T f(x,t), \tag{2.26a}$$

$$r_e(x,t) = e_p n_T [1 - f(x,t)], \tag{2.26b}$$

where c_p and e_p are the probabilities of hole capture and emission respectively. Capture and emission of charges gives rise to an admittance

$$Y_p(x,t) = j\omega \frac{q^2 n_T f_o (1 - f_o)}{kT[j\omega(1 - f_o)/c_p p_o(x) - 1]} \tag{2.27}$$

where k is Boltzmann's constant and T is the absolute temperature. $p_o(x)$ and f_o are the hole density per unit volume at x, and bulk trap occupancy Fermi function established by the gate bias [64]. Y_p is the admittance of an R-C network, with a capacitance and conductance per unit area given by

$$C_T = \frac{q^2}{kT} n_T f_o (1 - fo) \tag{2.28a}$$

$$G_T = \frac{q^2}{kT} n_T f_o c_p p_o(x), \tag{2.28b}$$

with a time constant $\tau = C_T/G_T$.

An equivalent circuit of a MIS capacitor in depletion with bulk traps is provided in Figure 2.17. C_{BT} and G_{BT} are the capacitance and conductance for bulk traps located within a few kT/q of the crossover point. The depletion capacitance has been split at crossover into C_{x_c} and C_{w-x_c}.

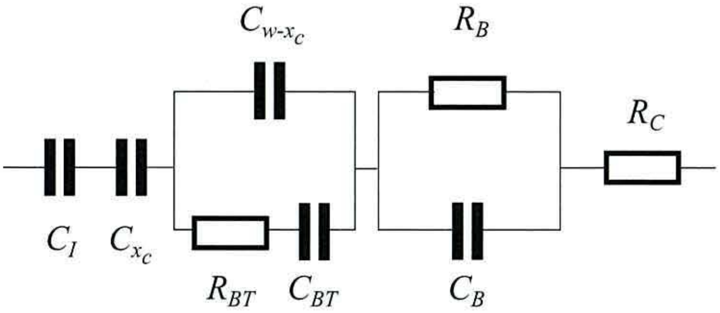


FIGURE 2.17: Equivalent circuit diagram of a MIS capacitor in depletion with bulk trap states.

2.3.4 Interface States

Interface states are traps located at the interface between the insulator and semiconductor layers, with energy levels within the band gap. The presence of these states leads to device instabilities such as hysteresis and threshold voltage shifts in OFETs [58, 97]. Trap states may be formed by structural defects [98], energetic disorder due to polar insulators [60, 99], functional groups and chemical reactions of the semiconductor with oxygen or moisture [58, 82]. For example, the Cavendish group showed that hydroxyl groups at the interface act as electron traps. They demonstrated that elimination of hydroxyl groups allows ambipolar conduction in organic semiconductors [34].

In p-type semiconductors *donor-like* states, located near the valence band, are hole traps which are neutral when empty and positively charged when full. Conversely *acceptor-like* states or traps are neutral when filled and negatively charged when empty, and are located in the upper half of the band gap. Only those traps located within a few kT/q of the Fermi level interact with the valence band by capture and emission of holes. The occupancy of interface traps is determined by the Fermi Level; traps below the Fermi level are empty and those above are full, as shown in Figure 2.18.

The change in occupancy of interface traps in response to a small ac voltage results in a measurable change in admittance depending upon the response time and density of the states. In the mid frequency range where capture/emission of majority carriers by interface traps lags the applied ac signal an energy loss results. However, at sufficiently low frequencies where interface traps can easily follow the applied signal and at high frequencies where they are unable to respond

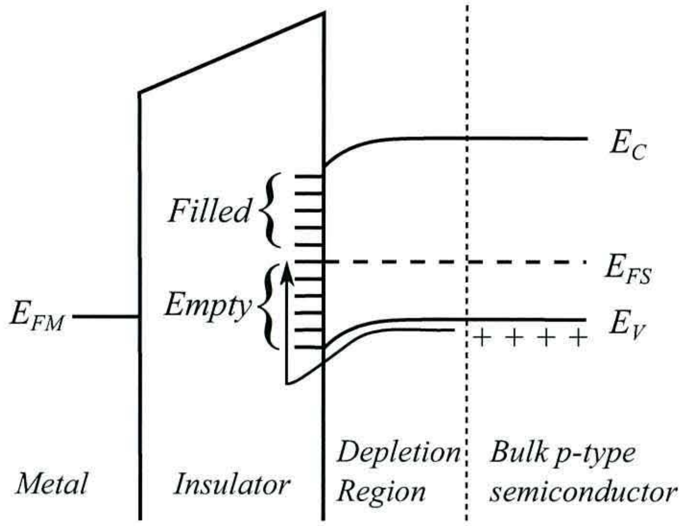


FIGURE 2.18: Energy band diagram of p-type MIS capacitor biased in depletion. Interface states below E_{FS} are empty, and those above are full. The arrow indicates charge exchange between interface states and the valence band.

no loss is seen. Because interface traps store charge for some time after capture, a capacitance is also associated with the density of interface traps.

Capture rates of interface traps depend on the concentration of majority carriers at the semiconductor surface, which in turn is determined by the band-bending. A peak in the loss is observed when capture rates equal the frequency of the applied ac signal. Because the density of majority charge carriers, and hence capture rate, is modulated by the band-bending the loss peak will occur at different frequencies determined by the gate voltage. The magnitude of the loss peak depends on both the density and capture rate of interface states interacting with majority carriers.

If the admittance of a MIS capacitor is obtained at a fixed frequency, with the gate bias swept from accumulation to depletion, the ac loss associated with interface states will be seen to peak with the device in depletion. For p-type devices biased into accumulation the Fermi level is close to the valence band and hole capture rates are very fast due to the high density of majority carriers. However, with the device biased in depletion the valence band moves further away from the Fermi level and the density of majority carriers reduces. Consequently capture rates also reduce and interface state response lags the ac signal, producing an energy loss. The maximum loss is observed when the ac frequency equals the capture and emission rate of the interface states.

The capacitance associated with the interface states also has an effect on the *C-V* response, where *stretchout* along the gate bias axis is observed [64]. In a trap-free MIS capacitor charge neutrality is maintained because charges on the gate are compensated by charges at the surface. Changing the gate bias changes the density of charge, Q_G on the gate, consequently band-bending in the semiconductor changes the surface charge population, Q_S to maintain charge neutrality. In MIS devices with interface states both Q_S and trapped charge density, Q_{IT}, change with bias. Charge neutrality is now maintained when $Q_G + Q_S + Q_{IT} = 0$. Thus the induced change in band-bending is less for devices with traps than those without, and the transition from accumulation to depletion occurs over a wider range of gate voltages. This results in stretchout of the *C-V* curve if interface states are distributed in energy over the semiconductor bandgap [64, 100]. However, if the trap has a discrete energy level, a small step or plateau will be seen in the *C-V* curve [101].

One of the most sensitive methods for determination of interface traps is the conductance method developed by Nicollian and Goetzberger [102]. This technique has also been used for extracting interface state densities in organic devices [103–105].

2.3.4.1 Single Level Interface Traps

Nicollian and Goetzberger determined the admittance for interface traps using the same Shockley-Read-Hall model used for bulk traps (Section 2.3.3). The capacitance, C_{IT}, and conductance, G_{IT}, of the interface traps can be represented by equations which resemble those for bulk traps (Equations 2.28)

$$C_{IT} = \frac{q^2}{kT} N_T f_o(1 - fo) \tag{2.29a}$$

$$G_{IT} = \frac{q^2}{kT} N_T f_o c_p p_s, \tag{2.29b}$$

where N_T is the density of interface traps per unit area, p_s is the hole density per unit volume at the interface and f_o is the Fermi function for interface trap occupancy in thermal equilibrium [102].

In deriving the admittance for single level interface traps, Nicollian and Goetzberger assumed that trap energy levels are well separated in energy [102]. The presence of these traps introduce a capacitance, C_{IT}, and resistance, R_{IT}, into the equivalent circuit of Figure 2.9 as shown in Figure 2.19.

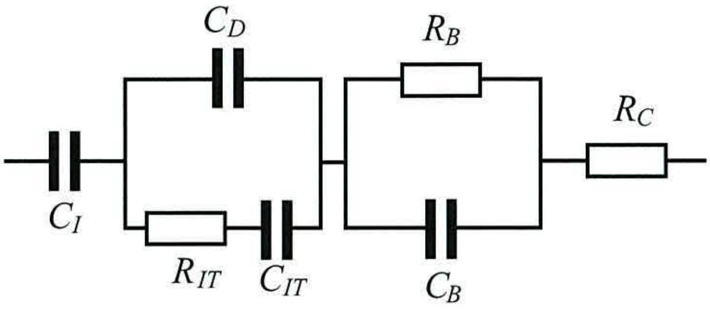


FIGURE 2.19: Equivalent circuit for a MIS capacitor with a single level interface state.

The equivalent parallel capacitance and loss derived from the admittance of the depletion branch of the equivalent circuit are [64]

$$C_P = C_D + \frac{C_{IT}}{1+(\omega\tau)^2} \tag{2.30a}$$

$$\frac{G_P}{\omega} = \frac{C_{IT}\omega\tau}{1+(\omega\tau)^2} \tag{2.30b}$$

where the time constant of the interface state is given by

$$\tau = C_{IT}R_{IT} = (v_{th}\sigma_p N_V)^{-1} exp\left(\frac{E_T - E_V}{kT}\right) \tag{2.31}$$

and v_{th} is the thermal velocity of holes, σ_p their capture cross section and N_V the density of states. From Equations 2.30 the maximum in the loss occurs when $\omega\tau = 1$, with a peak value of $C_{IT}/2$.

2.3.4.2 Distribution of Interface States

Interface states are not normally found at single energy levels, but in a distribution of energy levels which are so closely spaced that they form a continuum of states. Each energy level can be represented by the parallel combination of *R-C* branches as shown in the equivalent circuit diagram in Figure 2.20(a). C_{ITi} and R_{ITi} represent the capacitance and resistance of the *ith* energy level. Equivalently, the *i* *R-C* elements representing each trap can be represented by the frequency dependent components $R(\omega)$ and $C(\omega)$ in Figure 2.20(b).

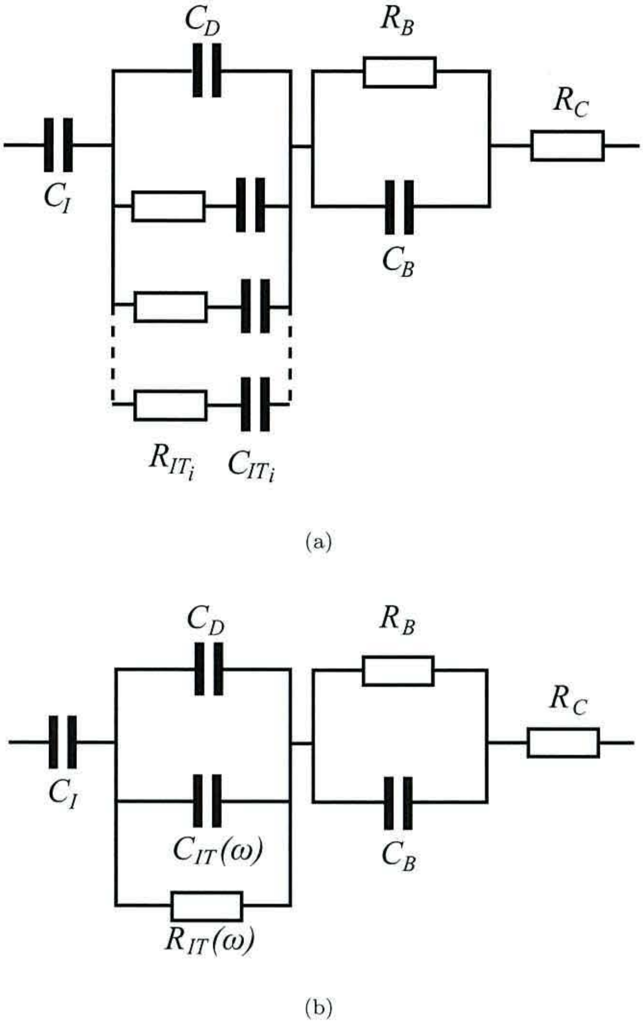


FIGURE 2.20: (a)Equivalent circuit for a MIS capacitor with a continuum of interface state energy levels. (b) Simplified circuit of (a) where the *R-C* branches have been lumped into frequency dependent components.

Despite the continuum of states only those interface states within a few kT/q of the Fermi level change occupancy and contribute to the circuit admittance. The interacting interface states will respond to an ac signal with different time constants resulting in a broader loss peak than that observed for a single interface state energy level.

For a continuum of states the equivalent parallel capacitance and loss are now [64]

$$C_P = C_D + \frac{C_{IT}}{\omega\tau} arctan(\omega\tau) \tag{2.32a}$$

$$\frac{G_P}{\omega} = \frac{C_{IT}}{2\omega\tau} ln[1 + (\omega\tau)^2], \tag{2.32b}$$

where $C_{IT} = q^2 D_{IT}$ is the interface state capacitance and D_{IT} is the density of interface states per unit area per eV. The loss peak, from Equation 2.32(b), now occurs when $\omega\tau = 1.98$ and has a peak value when $G_p/\omega = 0.4C_{IT}$.

In order to extract interface state properties using the method described by Nicollian and Goetzberger, the measured admittance must first be converted to an impedance, $Z_M = 1/Y_M$. Z_M is the series sum of the impedances of the insulator, $Z_I = 1/j\omega C_I$, and semiconductor. Subtraction of Z_I from Z_M yields the admittance, $Y_P = G_P + j\omega C_P$, of the semiconductor, where C_P and G_P are defined by Equations 2.30 and 2.32 for single energy level traps and distributions of traps respectively. D_{IT} is then determined from the loss peak in the G_P/ω plot.

The conductance method for extracting the interface state density profile entails detailed analysis of admittance measurements obtained over a range of frequencies and biases. Hill and Coleman (HC) introduced a simpler technique to approximate the density of interface states directly from the measured admittance. Their approach only requires a C-V and corresponding G/ω-V measurement obtained at a single high frequency. This method is valid for trap densities less than 1×10^{11} cm^{-2}eV^{-1} [106, 107]. Provided the frequency of measurement is sufficiently lower than the Maxwell-Wagner dispersion, D_{IT} is approximated from

$$D_{IT} = \frac{2}{qA}\frac{G_{M(max)}/\omega}{\left(\frac{G_{M(max)}}{\omega C_I}\right)^2 + \left(1 - \frac{C_{M(max)}}{C_I}\right)^2}, \tag{2.33}$$

where $G_{M(max)}$ is the peak loss in the G/ω-V plot and $C_{M(max)}$ is the associated capacitance at the same bias obtained from the corresponding C-V plot.

The interface state energy level, E_{IT}, can be determined from the surface potential, ψ_S, when the loss in a G/ω-V plot is at its maximum [40, 105]

$$\psi_S = E_{IT} - E_{Fb} = \frac{qN_A\varepsilon_s\varepsilon_0 A^2}{2}.\frac{1}{C_D^2}, \tag{2.34}$$

where E_{Fb} is the bulk semiconductor Fermi level.

2.3.5 Insulator States

Defect states within the insulating layer may also exchange charge carriers with the semiconductor via a tunnelling process [108]. The distribution in depth of these states leads to a range of response times resulting in a broad loss peak. The highest probability for tunnelling into the insulator occurs with the MIS capacitor in accumulation, and this corresponds to the maximum contribution of insulator states to the admittance.

Insulator traps located a distance x from the interface have a capture cross section which decays exponentially with their distance $\sim e^{-2Kx}$ (K is the wavevector of carriers in the insulator) [109]. Hence losses due to these traps exhibit both a time constant dispersion and an asymmetric loss peak, where the loss decays faster on the high frequency side of the dispersion. These traps also contribute to the capacitance in accumulation, making the measured value higher than the insulator, C_I. As the MIS device is biased toward depletion, the surface carrier density decreases and the associated time constant for these traps increases, causing the loss to peak at lower frequencies.

The equivalent circuit corresponding to a MIS device with insulator states is shown in Figure 2.21, from which the admittance of the insulator is

$$Y_I = G_T + j\omega(C_I + C_T), \tag{2.35}$$

where G_T and C_T are the conductance and capacitance of the insulator states.

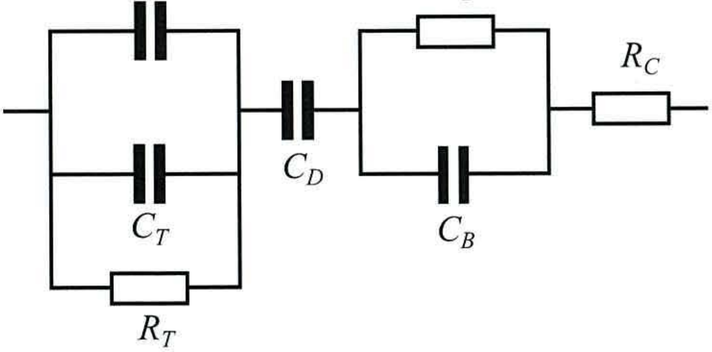


FIGURE 2.21: Equivalent circuit for a MIS capacitor with insulator states. From ref. [78].

2.4 Photo-Assisted Admittance

Determination of interface state properties in the dark using the conductance technique is limited to those which interact with majority carriers [64]. In a complementary method, described by Poon and Card, steady state illumination of the semiconductor by bandgap light allows the interface state density and capture cross sections for minority carriers to be determined [110].

For a p-type semiconductor in depletion the combination of gate bias and irradiance will move the electron quasi-Fermi level closer to the conduction band [110]. Photons absorbed in the space charge region will generate mobile charges and minority carriers within a diffusion length of the semiconductor surface will respond to an ac signal. Interaction of minority carriers with interface states will contribute to the measured admittance. The density and cross section of interface states can then be extracted from the measured admittance following the method of Nicollian and Goetzberger.

Photo-generation of minority carriers has also been used in the determination of interface states of wide bandgap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) [111–113]. Thermal generation of minority carriers in these materials has been estimated to be of the order of years, hence researchers use a photo-assisted C-V method to generate minority carriers. Initially the gate voltage of MIS capacitors is swept from accumulation to depletion in the dark. At the end of this forward sweep, the bias is held constant and the device illuminated so that an inversion layer of minority carriers populates the surface. After the capacitance reaches an equilibrium value the light is extinguished and the gate bias is swept back to accumulation. This results in hysteresis caused by carriers trapped in interface states. The average density of states is then deduced from the voltage shift, ΔV, via the relation [111]

$$D_{IT} = \frac{C_i \Delta V}{q E_g}, \tag{2.36}$$

where D_{IT} is the average interface state density per unit area per eV, C_i the insulator capacitance per unit area, q the electronic charge and E_g the bandgap of the semiconductor.

Steady state illumination of organic devices has been used to assess the effect of interface states on minority carriers [62, 114]. Both an increase in the minimum depletion capacitance and hysteresis were observed when the devices were subjected to bandgap light. In this case the number of trapped electrons per unit area, N_T, was estimated from the shift in flatband voltage ΔV_{FB} using the relation [62]

$$N_T = \frac{C_i \Delta V_{FB}}{q}. \tag{2.37}$$

The increase in minimum capacitance was related to a reduced depletion layer width Δd caused by an inversion layer of minority carriers. The number of minority carriers is therefore [62, 115]

$$n_f = N_A \Delta d, \tag{2.38}$$

because charge neutrality is maintained by a reduction in the depletion layer width to compensate for the increased population of minority carriers.

2.5 Charge-Coupled Device

The Charge-Coupled Device (CCD) was invented by Boyle and Smith at Bell Labs in 1969 [63]. Originally designed as a shift register for use in a bubble memory device, they realised that charge could be injected by the photoelectric effect enabling images to be stored electronically. CCD arrays consist of a number of MIS capacitors in close proximity, which can collect and store minority charge [116].

A cross-sectional view of a CCD structure with three cells is shown in Figure 2.22. For a device with a p-type semiconductor, a potential well is formed under the gate when positively biased. The adjacent gates are negatively biased to create potential barriers. When a photon of light with sufficient energy to produce an electron-hole pair is absorbed by the semiconductor, the electron is confined to the well and the hole diffuses away. During the integration period of light exposure photo-generated carriers are collected in the well. Thus across an array of CCDs the pattern of stored charge corresponds to the pattern of light detected.

Careful manipulation of the gate biases move the potential wells, with the charge following [116]. In this manner the charge can be directed toward an output node whereupon it is detected by a charge amplifier. A schematic of a three-phase

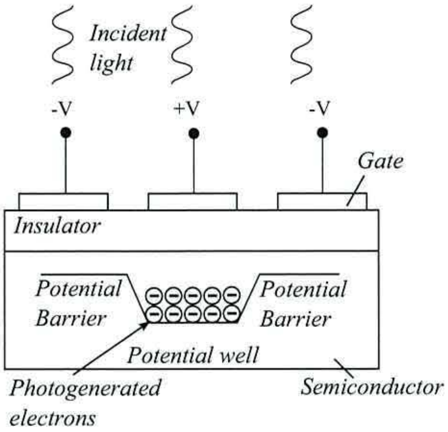


FIGURE 2.22: Cross-section of a CCD structure. Photo-generated electrons are confined to a potential well.

CCD, where every third gate is connected to the same clock, is shown in Figure 2.23. Referring to Figure 2.23(b), at $t = t_1$ photo-generated charge is confined in potential wells under the ϕ_1 electrodes. After the integration period, at $t = t_2$, the ϕ_2 electrodes are biased positively beneath which potential wells form and the stored charge migrates into the ϕ_2 wells. At $t = t_3$ the bias on ϕ_1 is gradually reduced and the charge remaining under the ϕ_1 electrodes drift into the ϕ_2 wells. At $t = t_4$ all the charge has been transferred and is stored in the wells under the ϕ_2 electrodes. At $t = t_5$ the ϕ_3 electrodes are positively biased forming potential wells in the semiconductor. The stored charge under the ϕ_2 wells now migrate to the wells under the ϕ_3 electrodes. This process continues until the charge has moved along the array of MIS capacitors. The timing diagram for this process is shown in Figure 2.23(c).

The *depth* of the potential well depends on the applied gate bias. As described in Section 2.2.1.3, when a positive voltage is applied to the gate electrode of a p-type MIS capacitor the bands in the semiconductor bend down and a depletion region is formed. The band-bending at the surface, ψ_s, defines the depth of the potential well [116]. Photo-generated electrons collected in the potential well reduce the level of band-bending resulting in a change in ψ_s.

The maximum density of electrons that can be stored in a MIS capacitor is [116]

$$N_{max} \simeq \frac{C_i V_G}{q}, \tag{2.39}$$

where C_i is the insulator capacitance per unit area and V_G is the voltage applied to the gate electrode.

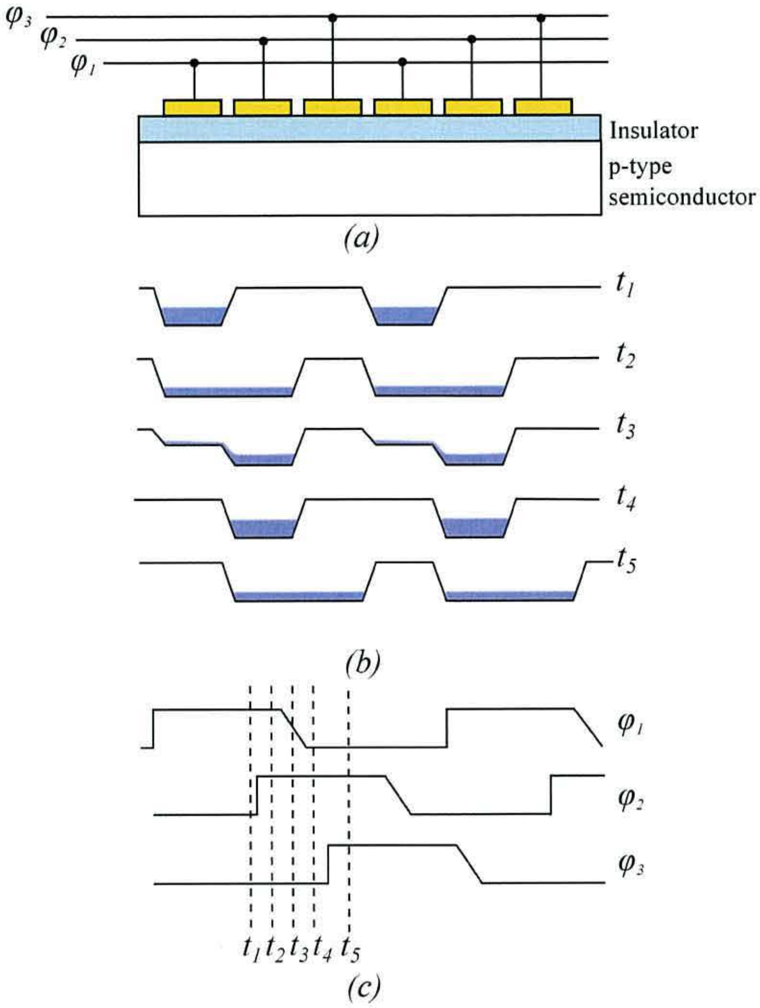


FIGURE 2.23: Charge transfer in 3-phase CCD. (a)Gate bias scheme, (b) Potential well profile during charge transfer, (c) Clock timing waveforms. Adapted from Ref.[40].

The mechanisms for charge transfer between MIS capacitors in a CCD array are [40]

- Self-induced drift caused by an electric field resulting from the uneven distribution of charge in the well. This is the dominant mechanism for a large signal charge density, Q_{sig}. The transfer time due to drift is given by [40]

  $$t_0 = \frac{\pi L^2 C_I}{2\mu_n Q_{sig}}, \tag{2.40}$$

  where L is the length of the electrode, μ_n is the mobility of the minority charge carriers.

- Fringing field drift caused by the potential difference between the gates. When a bias is applied to adjacent gate electrodes, the electric potentials give rise to an electric field between them. This fringing field ensures all the charge carriers are transferred.

- Thermal diffusion is the dominant process for small densities of charge, and has a time constant given by

  $$t_{th} = \frac{4L^2}{\pi^2 D_n}, \tag{2.41}$$

  where D_n is the minority charge carrier diffusion constant[40].

These time constants for charge transfer provide some of the constraints relating to the clock frequency. The clock period has to be long enough to allow charge transfer. It can be noted from Equation 2.40 that for short transfer times the minority mobility, μ_n, should be high and both the electrode spacing and C_I should be minimised. Another consideration is the dark current which contributes to the total charge in the CCD, and impacts upon the storage time of the MIS capacitor. The ratio of the maximum charge density to dark current density, J_{da}, defines the maximum storage time, i.e. [116]

$$t_s = \frac{C_I \Delta V}{J_{da}}, \tag{2.42}$$

where ΔV is the height of the barriers between potential wells.

As the CCD operates as a shift register, the amount of charge transferred from the CCD cells to the output is crucial to the device response. For a useful device its Charge Transfer Efficiency (CTE) must be better than 99.9999 % which results in a loss ($(1 - CTE^n) \times 100\,\%$, where n is the number of transfers) of only 0.01% of charge in 100 transfers. An efficiency of 99 % would result in 63 % of charge being lost. For silicon CCDs, CTE is limited by charge traps at the semiconductor-insulator interface.

Interface states in MIS structures trap charges at the interface as discussed in Section 2.3.4. The effect of interface traps on the charge transfer efficiency depends on the clock frequency (f_c). Charges which are released quickly from their traps (i.e. $\ll 1/f_c$) rejoin the charge packet; charges which are released after a long period (i.e. $\gg 1/f_c$) are considered to be permanently trapped. Neither of these two conditions contribute to transfer inefficiency. However if the release period $\approx 1/f_c$, the trapped charge will be released into following packets and contribute to transfer inefficiency [116]. The charge transfer inefficiency due to trapping at the interface is [40]

$$\varepsilon \approx \frac{qkTD_{IT}}{C_i \Delta\psi_s} ln(N_p + 1), \tag{2.43}$$

where $\Delta\psi_s$ is the change in surface charge caused by the signal charge, D_{IT} the interface trap density, C_i insulator capacitance per unit area and N_p is the number of clock phases.

The buried channel CCD (BCCD) avoids interface traps by forming a channel beneath the surface. A layer of n-type semiconductor separates the p-type substrate from the insulator. This layer is fully depleted with the charge kept away from the interface, resulting in higher mobility and lower dark current. The capacity of the potential wells, though, is reduced due to their increased distance from the gates [116].

A related device, the charge injection device (CID), also consists of an array of MIS capacitors. As with the CCD, photo-generated minority charge is collected in potential wells under the gates during an integration period. Arrangement of the capacitors in pairs, as in Figure 3.5 enables x-y addressing of pixels. During the integration period the electrodes are biased such that $V_{Row} > V_{Col}$, where V_{Row} and V_{Col} are the voltages applied to the row and column electrodes respectively. Consequently a deeper potential well exists under the row electrode where all the photo-generated charges are stored (Figure 3.5(a)). Assuming the flatband voltages of the capacitors are both ~0 V, a pixel is selected by setting V_{Row} to 0 V, whereupon the associated potential well collapses and the stored charges transfer to the column capacitor (Figure 3.5(b)). When V_{Col} is also set to zero, its well collapses and a displacement current can be detected, either at the gate or at the semiconductor contact, as the stored charge is injected into the semiconductor bulk (Figure 3.5(c)) [117].

In a subsequent paper Burke and Michon described an alternative non-destructive readout method (called parallel injection) wherein the stored charge could be read a number of times (at 30 frames per second) over an extended period of 3 hours without detectable loss [118]. In this case the displacement current was sensed at the gate whilst the charge was transferred from one potential well to the other. As

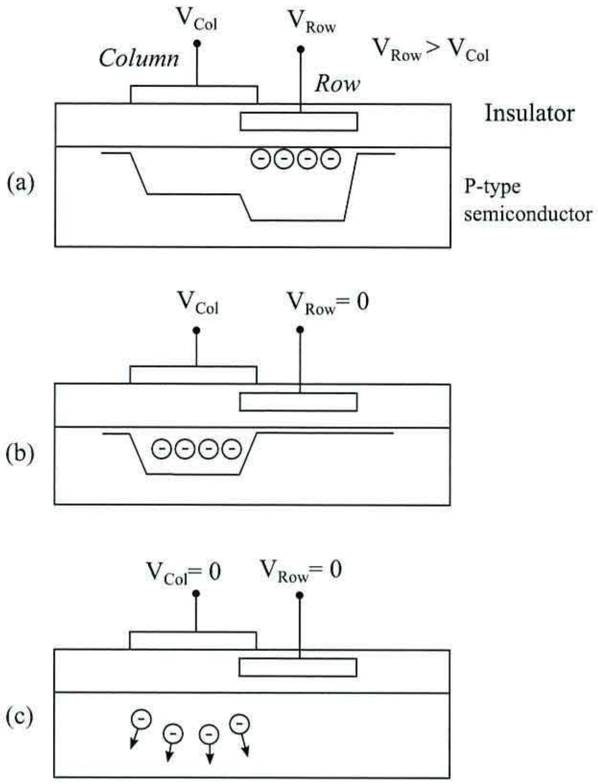


FIGURE 2.24: CID device cell. Two potential wells are controlled by the column and row gates. (a) Photo-generated charges are stored under the row electrode. (b) V_{Row} is set to zero and the stored charge transfers to the column capacitor. (c) The potential well collapses when V_{Col} to zero and the stored charges are injected to the semiconductor bulk. Adapted from [65].

this process is similar to charge transfer in a CCD it provides a relatively simple test structure to determine if charge transfer is possible in organic materials.

Although there are many examples of photo-detector arrays using organic photodiodes as the sensor [48, 119, 120], there are few, if any, articles regarding CCDs using an organic semiconductor. In his thesis, Huang concludes that an organic CCD would be viable, and capable of producing images at a high clock rate due to the short lifetime of the charge carriers. Photo-lithographic masks were designed, but there were no experimental results given [121].

2.6 Absorption of Light in Semiconductors

The response of photo-detectors to light depends upon absorption of photons with energy greater than the semiconductor bandgap E_g, i.e. photons with wavelength

$$\lambda \leq hc/E_g, \tag{2.44}$$

where h is Planck's constant and c is the speed of light. Absorption of bandgap light creates coulombically bound electron-hole pairs (excitons) which may recombine or dissociate into free charges if subjected to an electric field of sufficient strength [9]. The number of excitons generated depends on the number of photons absorbed within the semiconductor layer. In this work, knowledge of the number of absorbed photons enabled the development of a simple model to help explain the effect of light on the *C-V* response of MIS capacitors.

In Figure 2.25 light of irradiance I_0 is incident onto a semiconductor surface. Some of the incident light will be reflected. The proportion rI_0, reflected from the surface is given by the semiconductor reflection coefficient r [122]

$$r = \left(\frac{n-1}{n+1}\right)^2, \tag{2.45}$$

where n is the refractive index of the semiconductor.

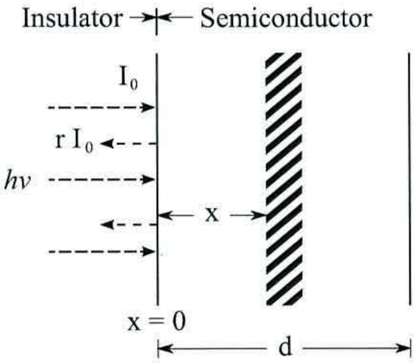


FIGURE 2.25: Schematic illustrating optical absorption in a semiconductor layer.

The remaining light is either absorbed by the semiconductor, or passes through it. Light intensity decays exponentially through the semiconductor layer, and (from the Beer–Lambert–Bouguer law of absorption) at a distance x from the insulator/semiconductor interface is given by [122]

$$I(x) = I_0(1 - r)e^{-\alpha x} \tag{2.46}$$

where $e^{-\alpha x}$ is the proportion of light transmitted and α is the absorption coefficient which can be written in terms of the Imaginary part of the complex refractive index, k

$$\alpha = \frac{4\pi k}{\lambda}. \tag{2.47}$$

Applying Equation 2.46 to n–k data for P3HT (kindly provided by Dr. T. Jenkins at Aberystwyth University) reveals the dependence of absorption at different wavelengths on both distance, x and n–k values. This is presented in Figure 2.26, where the fraction (I/I_0) of light has been plotted as a function of distance (x) in to the semiconductor.

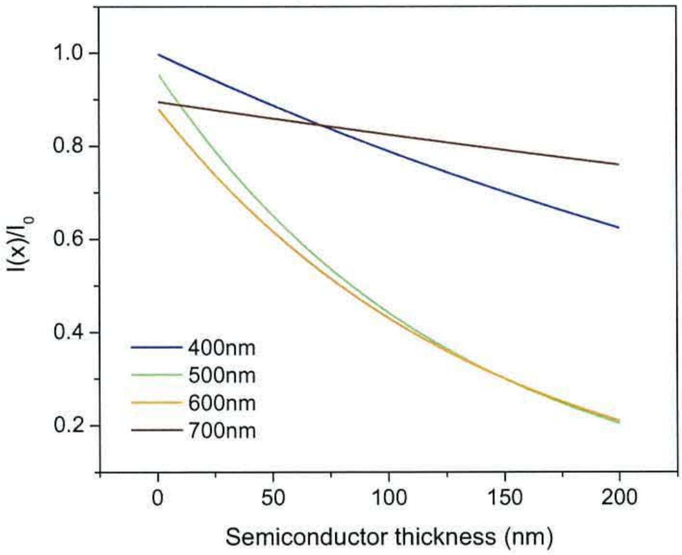


FIGURE 2.26: Fractional intensity of light as a function of distance calculated using Equation 2.46 for P3HT.

It follows from Equation 2.46 that the proportion of light absorbed in the semiconductor is $(1 - e^{-\alpha x})$. For monochromatic light the photon flux incident on the device (per unit area per second) is

$$\Phi_\lambda = \frac{I_0\lambda}{hc}. \tag{2.48}$$

Thus the fraction of photons per unit area per second, N_λ, of wavelength λ absorbed in a semiconductor layer of thickness d is [122]

$$N_\lambda = (1-r)\Phi_\lambda(1-e^{-\alpha d}). \tag{2.49}$$

However it should be noted that this analysis does not include the contribution of photons absorbed following reflection from the rear surface.

2.7 Summary

The theory and operation of MIS capacitors has been reviewed. Although based on standard MOS capacitors, it serves as a basis for the characterisation of MIS structures with an organic semiconducting layer. Depending upon the applied DC bias the MIS device operates in accumulation, flatband or depletion. Inversion in organic MIS capacitors is not observed due to the extremely long generation time for minority carriers.

Admittance measurements are sensitive to the effects of defects within an MIS device. Capacitance and loss as functions of frequency exhibit dispersions relating to semiconductor conductivity, defect states, lateral conduction, insulator and contact resistances. The main relaxation observed is the Maxwell-Wagner (M-W) dispersion, caused by the majority carrier response time. Bulk conductivity and mobility can be determined from this relaxation frequency. In low mobility semiconductors the M-W relaxation generally occurs at frequencies below 1 MHz and should increase as the MIS capacitor is biased into depletion. Also, the maximum capacitance at low frequencies reduces for depletion voltages. These changes in capacitance and loss are characteristic behaviour for a MIS capacitor driven into depletion. Dispersion of carrier response times results in a broadening and decrease in magnitude of the M-W loss peak.

In devices with unpatterned gates and semiconductor layers, lateral conduction effectively increases the device area, leading to an increase in the low frequency capacitance and loss. Guard rings reduce lateral conduction effects but introduce a parasitic FET. Increased loss is also seen where the device has a *leaky* insulator. The presence of a resistance associated with the contacts leads to a dispersion with a relaxation frequency $\gg$ 1 MHz.

Interaction of majority carriers with defect states also affects the admittance with the MIS capacitor in depletion. A distribution of interface states causes stretchout of the C-V curve, and the corresponding loss peaks at a bias where the interface state capture rate equals the ac frequency. Interface states also display a peak in the G/ω-f curves with a time constant and magnitude dependent on the bias. As the device is driven further into depletion the time constant increases and the peak magnitude decreases.

Bulk states only affect the admittance when devices are biased in depletion, where a dispersion occurs, independent of bias, at a fixed frequency in G/ω-f curves. The magnitude of the loss peak only changes with bias for a non-uniform density of traps in the bulk. In G/ω-V curves, measured at a frequency that probes the bulk states, the associated loss will be constant. Bulk states will also make a contribution to the capacitance in depletion.

The loss peak associated with insulator states is both frequency and bias dependent. Capture and emission of majority carriers by insulator states occurs via a tunnelling process. The maximum loss occurs in accumulation when the probability for tunnelling is highest.

Irradiation of wide bandgap semiconductors with light of suitable energy generates electron-hole pairs. In depletion, photo-generated minority carriers can form an inversion layer and interact with states at the interface. There is, though, a lack of evidence that inversion layers are formed in organic semiconductors. The density of interface states for minority carriers can be extracted from hysteresis in C-V curves or from the loss peak in G/ω-V curves using the conductance method.

Charge-coupled devices (CCD) are arrays of MIS capacitors. Depending on the biases applied, minority carriers are stored in potential wells or transferred to an adjacent MIS capacitor. Charges drift between capacitors under the influence of an electric field due to the potential difference between their gate voltages. Trapping of charges in interface states causes a smearing of the charge packet between capacitors during the transfer process, and therefore affects the charge transfer efficiency. Thus the semiconductor/insulator interface must have a low density of traps. The charge injection device (CID) is very similar to the CCD, and allows x-y addressing of pixels. There are no experimental results for an organic CCD published in the literature, although a photo-lithographic design has been reported. A device structure based on the CID provides the opportunity to investigate charge transfer between two organic MIS capacitors, from which the viability of an organic CCD array can be assessed.

It is clear from this chapter that implementation of an organic CCD depends upon a number of issues which require further investigation, for example:

- The stability of the flatband voltage.
- Charge trapping either at or near the semiconductor/insulator interface.
- Conductivity and mobility of the semiconductor.
- Optical response of the MIS capacitor.
- Minority charge trapping under illumination.
- Transfer of minority carriers between adjacent MIS capacitors.

These are the subject of the subsequent chapters.

Chapter 3

Materials and Methods

3.1 Introduction

The materials, fabrication techniques and experimental methods used during the work undertaken at Bangor are provided in this chapter. Poly(3–hexylthiophene) was used as the active layer in Metal-Insulator-Semiconductor (MIS) capacitors, Charge Injection Devices (CID) and capacitor arrays. The insulating layers for these devices (as well as the Metal-Insulator-Metal (MIM) capacitors) were either the epoxy resin SU8 or a spin-on-glass (polysilsesquioxane). All these materials have been extensively studied, so a brief overview of them is provided here.

3.2 Materials

3.2.1 Poly(3-hexylthiophene-2,5-dilyl)

Poly(3–hexylthiophene) (P3HT) belongs to the group of polymers known as polythiophenes (PTs). One of the first PT's, poly(2,5-thienylene) (synthesized independently by both Yamamoto *et al.* [123] and Lin *et al.* [124]), exhibited high conductivity. This was due to the strong π-orbital overlap of neighbouring thiophene rings, whose conjugated backbone was similar in structure to both *trans*–polyacetylene and poly (p-phenylene). The unsubstitued PT is insoluble, however addition of alkyl side chains provided poly(3-alkylthiophene) (P3AT) derivatives which were soluble in organic solvents [125], leading to solution processed organic FETs with poly(3–hexylthiophene) as the semiconducting layer [126]. There are three possible ways in which thiophene units can couple: head-to-tail (HT), head-to-head (HH) and tail-to-tail (TT). Steric hindrance in HH and TT couplings twists the structure resulting in reduced π-orbital overlap [127]. M^{c}Culloch (and later, Rieke [128]) synthesized highly regioregular P3ATs (RR-P3AT) with a HT regioregularity of $> 98\,\%$ [129], which led to improved field-effect devices with mobilities ~0.045 cm^2/Vs [130].

Solution deposition of HT RR–P3HT (Figure 3.1) results in a crystalline film, ordered as a two–dimensional lamella structure due to interchain stacking [131]. Being soluble in organic solvents such as chloroform, toluene and xylene, various solution deposition techniques can be used [132]. It has been used for various organic electronic devices, e.g. OFETs, Schottky diodes, photovoltaic cells and photodiodes [8, 133–135].

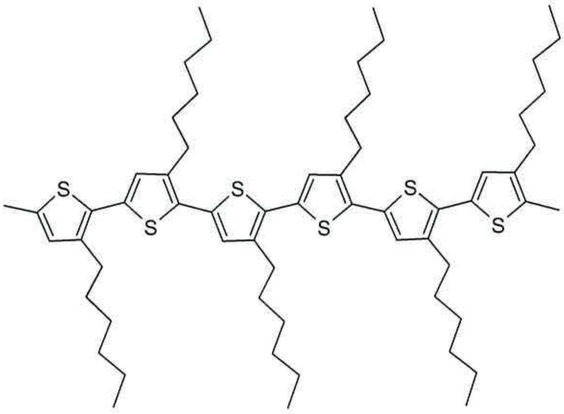


FIGURE 3.1: Structure of regioregular P3HT.

P3HT is a p-type material, i.e. one in which the majority carriers are holes (positive charges), although ambipolar conduction has been demonstrated [34, 136]. When left in the ambient P3HT is prone to oxidative doping; a high doping concentration makes it unsuitable as a semiconductor. Annealing devices under vacuum to remove dopants is common practice, and leads to improved device performance [137]. More recently Baeg and co-workers fabricated optimized top gate OFETs in which P3HT was spin-cast on to high work-function electrodes (platinum) and subsequently annealed, resulting in devices with mobilities as high as 0.4 cm^2/Vs. These top-gate devices also exhibited improved air stability due to the encapsulating effect of the low permeability gate dielectric [138].

3.2.2 SU8

SU8 is a negative near-UV epoxy photo-resist developed by IBM (US Patent No. 4882245 (1989)) and has found widespread use in MEMS and micro-fluidics applications [139]. SU8 has also been used as the dielectric in flexible single crystal silicon thin-film transistors [140] and both pentacene and P3HT OFETs [141].

SU8 photoresist is a liquid containing the SU8 epoxy resin, solvent (either cyclopentanone or gamma butyrolactone (GBL)) and a photo-acid generator. When exposed to UV light Lewis acids (HSbF6) are produced, which, during a postexposure bake, cause the epoxy groups to cross-link. Each SU8 molecule (Figure 3.2) has eight epoxy groups which, upon photopolymerization, yields a high degree of crosslinking, enabling the resin to form an extremely robust ladder-like structure [142].

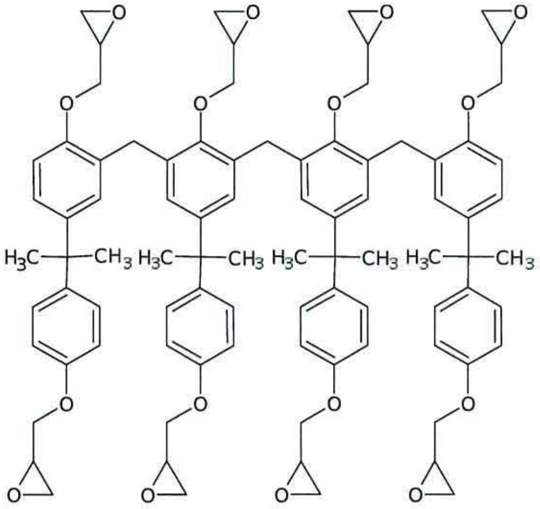
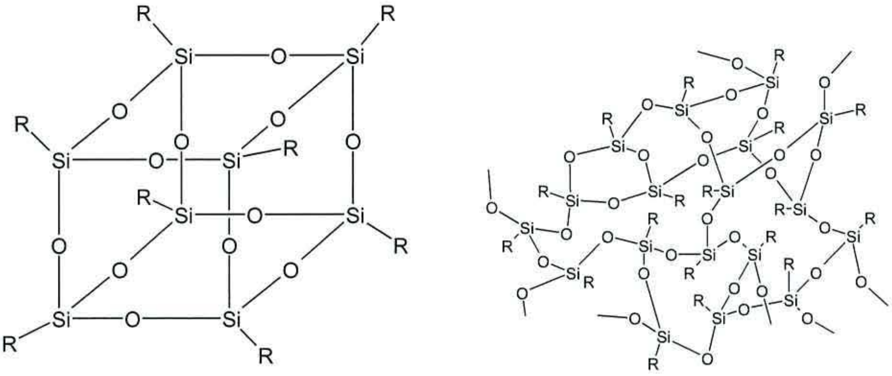


FIGURE 3.2: SU8 molecule with eight epoxy groups.

Coating of substrates with SU8 is performed by the conventional spin coating technique, which leads to film thicknesses ranging from 0.5 μm up to 2 mm, although thinner layers may be obtained by thinning the resist in the appropriate solvent.

3.2.3 Polysilsesquioxane

Polysilsesquioxanes are inorganic–organic compounds which contain silicon and oxygen in each moiety (sequence) in the ratio 1:1.5 (sesqui). Their empirical formula is $RSiO_{1.5}$, where R is an organic functional group such as an alkyl or aryl [143]. They are solution processible (being soluble in common organic solvents) and thus can be spun on to produce thin films, and are often referred to as spin-on-glass. The structure of PSQ changes from a mixture of cage/network forms (Figure 3.3(a)) to a more network-like form upon curing (Figure 3.3(b)).



(a) Cage form of PSQ.

(b) Network form of PSQ.

FIGURE 3.3: Different forms of cured PSQ.

After deposition, films may be cured at various temperatures; temperatures up to about 350 °C result in soft films, whereas temperatures up to 550 °C provide hard porous films. Bao *et al.* used poly(methylphenyl)siloxane as the dielectric layer in organic field-effect transistors (OFETs) [144]. These films were partially cured at only 135 °C, leaving a few hydroxyl groups (–OH) at the surface, improving the effectiveness of surface modification with silanes. Curing at 400 °C will remove most of the hydroxyl groups leaving an inorganic layer with properties similar to SiO_2 [143].

3.3 Fabrication of MIS and MIM Capacitors

This section details the fabrication (within a class 1000 cleanroom) of MIS and MIM capacitors used for electrical characterisation. The structure of MIS devices is shown in Figure 3.4.

Indium Tin Oxide (ITO) coated glass ($R_s = 5$–$15\,\Omega/\square$, Delta Technologies) were cleaned in a solution of 20 % ethanolamine in ultrapure water, following the manufacturer's recommended procedure. The ITO provided a common gate for several devices on each substrate. Prior to deposition of the insulator, substrates

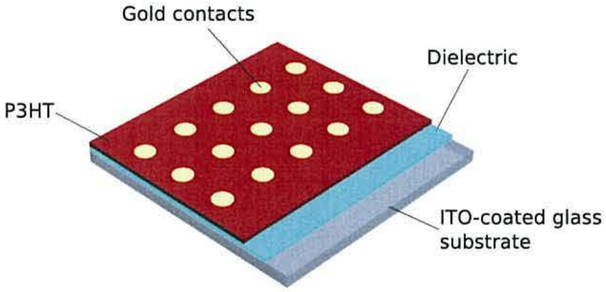


FIGURE 3.4: MIS capacitor structure illustrating how the layers were cleaned to provide access to the ITO layer.

were dried by baking at 200 °C for 30 minutes, and used immediately after cooling to room temperature.

The organic layers were then processed as detailed in the following sections.

3.3.1 SU8 Dielectric Layer

Initially, for devices with SU8 as the insulating layer, SU8 2002 (Microchem) was used[1]. This provides layers approximately 2 μm thick. Thinning with cyclopentanone in a 50:50 ratio produced layers ~500 nm thick. After filtering using 0.2 μm PTFE filters, the SU8 resist was spin coated in two steps: an initial spreading phase at 500 rpm for 5 seconds, followed by a faster 'thinning' phase at 2000 rpm. Prior to curing, a small area was cleaned off using cyclopentanone to facilitate electrical connection to the ITO gate. Finally the SU8 was cured as detailed in Table 3.1.

Stage	Detail
1	Soft bake on a level hotplate at 95 °C for 1 min
2	Irradiate with UV at 120 mJ/cm^2
3	Post exposure bake at 95 °C for 1 min
4	Ramp to 200 °C and bake for 30 min

TABLE 3.1: Curing process for SU8 dielectric layer.

---

[1] Microchem now produce SU 8 2000.5 for 500 nm thick layers, which was used in the latter stages of this project.

3.3.2 PSQ Dielectric Layer

The PSQ insulator was prepared by dissolving phenyl-methyl-silsesquioxane (90% phenyl, 10% methyl, Gelest Inc.) flakes in 2-butanone (10% wt.). The flakes dissolved readily within a few minutes and no agitation was necessary - care must be exercised to prevent formation of micro-bubbles in the solution, which would result in pin-holes in the film. The prepared mixture was either used immediately or kept in a refrigerator until required. Prior to spin-coating for 60 s at 1000 rpm, the PSQ solution was filtered through a 0.2 μm PTFE filter and heated on a hotplate at 60 °C for 1 minute. A small portion of the film was removed with solvent to allow connection to the ITO after which the film was cured in stages as detailed in Table 3.2.

Stage	Detail
1	Ramp to 90 °C (on level hotplate) and dwell for 1 min
2	Ramp to 130 °C, dwell for 1 min
3	Ramp to 250 °C, dwell for 1 min
4	Place in nitrogen oven (preheated to 250 °C
5	Ramp to 425 °C, dwell for 1 hour
6	Cool to room temperature overnight in nitrogen oven

TABLE 3.2: Curing stages for PSQ dielectric layer.

3.3.3 Surface Treatment

Surface treatment of the dielectric layers is known to improve the ordering of the semiconductor layer[133]. In these studies hexamethyldisilazane (HMDS, Sigma Aldrich) was deposited on to the cured dielectric layers and left for 1 minute before being spun at 1000 rpm to provide a hydrophobic surface.

3.3.4 Poly(3-hexylthiophene) Film

The organic semiconductor, > 98.5% regioregular P3HT (Sigma Aldrich), was dissolved in filtered (0.2 μm Millipore PTFE filter) anhydrous chloroform at a 1%wt. concentration by placing in an ultrasonic bath at 40 °C for ~20 mins. The freshly prepared solution was filtered (again using 0.2 μm PTFE filters) and spin-cast, immediately after deposition of the HMDS layer, at 1000 rpm for 1 minute.

The dried P3HT film was removed from the edges of the substrate as well as the gate contact area with chloroform. Devices were then placed in a vacuum oven (Buchi) and annealed for 1 hour at 90 °C to remove any remaining solvent.

3.3.5 Contacts

Devices were completed by thermally evaporating (Edwards 306 Turbo Evaporator) 50 nm gold, through a shadow mask, on to either the semiconductor, for MIS devices, or the dielectric, for MIM devices, to provide 2 mm diameter circular contacts.

3.4 Charge Injection Device and Capacitor Array

This section details the fabrication of the charge injection devices (CIDs) and capacitor arrays deployed as optical sensors. The structure of both the CID and capacitor array are shown in Figures 3.5 and 3.6 respectively.

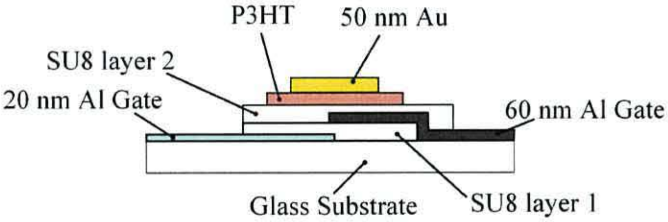


FIGURE 3.5: Charge Injection Device structure.

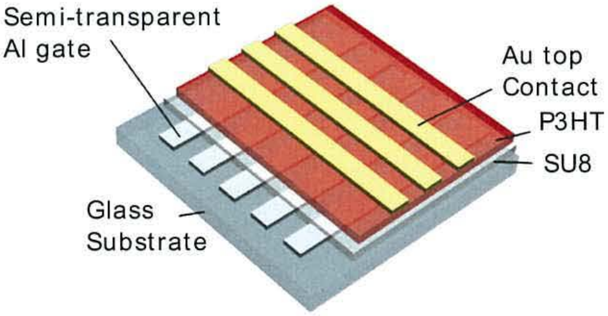


FIGURE 3.6: Capacitor array structure.

3.4.1 Substrates

3×5 arrays of 4 mm^2 addressable capacitors were fabricated on borosilicate glass slides cut to provide 25 mm × 25 mm square substrates (Figure 3.6). CID devices were fabricated onto borosilicate glass slides cut into 13 mm × 13 mm squares using an EC-400 dicer (MTI Corporation).

Substrates were gently cleaned by hand using Decon 90 and rinsed in ultrapure water (UPW) to remove any contamination due to the dicing process. They were then transferred to a substrate holder for further cleaning as outlined below (Table 3.3):

Stage	Solvent / Solution	Detail
1	1% Decon 90 in UPW	Ultrasonicate for 5 mins
2	UPW	Ultrasonicate for 5 mins
3	UPW	Ultrasonicate for 5 mins
4	Acetone	Ultrasonicate for 2 mins
5	Acetone	Ultrasonicate for 2 mins
6	Methanol	Ultrasonicate for 2 mins
7	Methanol	Ultrasonicate for 2 mins
8	Boiling 2-propanol	2 mins
9	Boiling 2-propanol	2 mins
10	–	O_2 plasma 5 mins

TABLE 3.3: Glass substrate cleaning process.

3.4.2 Film Deposition

Once cleaned, the substrates were immediately placed into a substrate holder with self aligning mask holder and placed in a Leybold 350 E-Beam evaporator for deposition of a semi–transparent aluminium gate (~20 nm) at a base pressure of $< 10^{-5}$ mbar.

For the CID devices (Figure 3.5) SU82000.5 (Microchem) was mixed 50:50 with cyclopentanone to provide layers ~100 nm thick and cured following the same process to that described in Section 3.3.1, except the UV dose was lowered to 60 mJ/cm^2. A second, opaque (~60 nm) aluminium gate was then evaporated through a shadow mask (E-Beam) and subsequently coated with a further layer of SU8. P3HT was deposited as described in Section 3.3.4 to provide the active layer.

Capacitor arrays (Figure 3.6) followed a similar procedure to the MIS devices described previously.

Finally, ohmic contacts were formed by thermal evaporation (Edwards 306 Turbo) of 50 nm gold through self-aligning shadow masks.

3.5 Electrical Characterisation

Electrical characterisation, taken under controlled conditions, provided the raw data necessary for detailed analysis of the devices employed in this research. Prior to each measurement, devices were kept un-biased for at least 10 minutes with the terminals grounded. This should minimize both long-lived optical effects (which occur whilst placing the devices in the measurement system) and the effects of previous measurements [145]. However, it was found that, in some cases, devices had to be annealed (with the contacts grounded) to reduce the effects of previous measurements and return them to a 'pristine' state.

All measurements, except for the capacitor arrays (see Section 5.6) were performed with the samples mounted on the substrate holder in an Oxford Instruments Optistat DN-V Cryostat. MIS and MIM devices were electrically connected using 25μm diameter gold wire (Advent Research Materials Ltd) 'glued' on to the contacts with conductive silver paint (Electrolube, H K Wentworth Ltd.). CIDs were mounted in a bespoke sample holder with electrical connection made via spring-loaded gold plated probes (Interconnect Devices Inc.) (Figure 3.7).

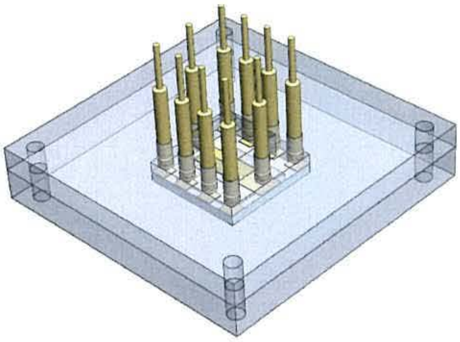


FIGURE 3.7: Sample holder test jig used for charge injection device measurements.

3.5.1 Experimental Set-Up

Experiments were performed in a dark room to eliminate stray sources of light during testing. The experimental set-up is shown in Figure 3.8 and was utilised for measurements on samples either in the dark or under illumination.

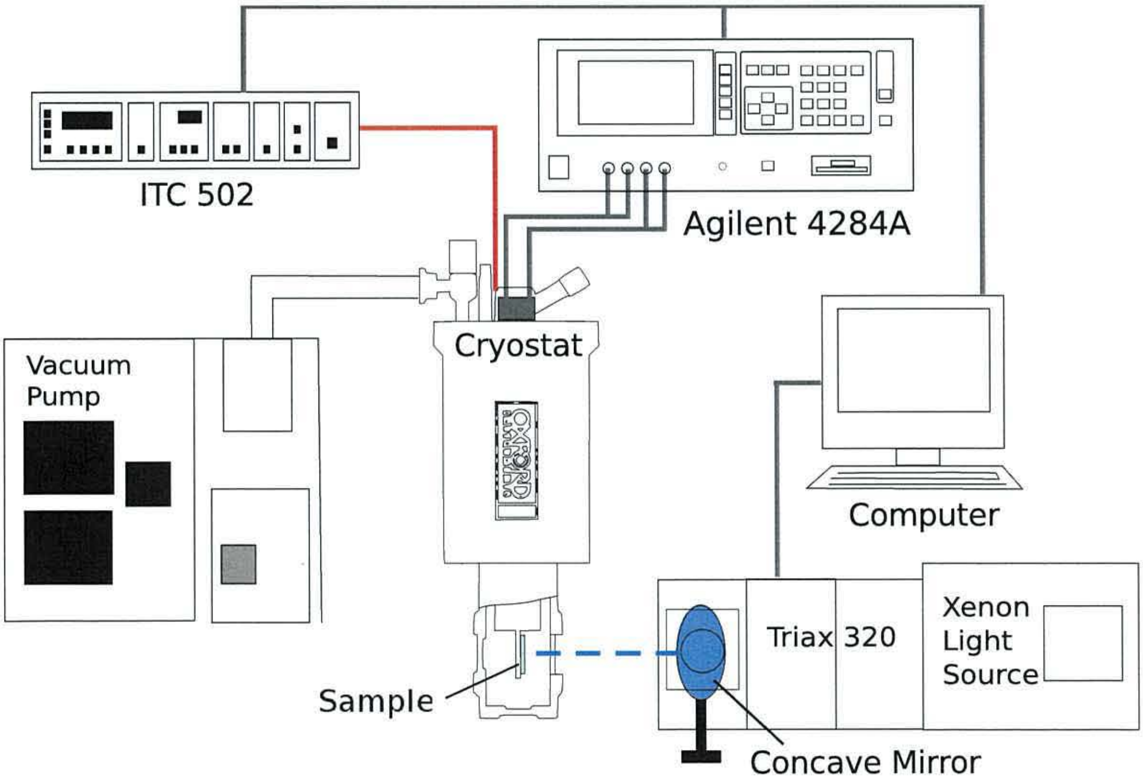


FIGURE 3.8: Diagram of experimental setup used for electrical characterisation of MIM, MIS and CID samples.

Optical experiments were performed at various wavelengths between 300–800 nm. Light output from a Xenon discharge lamp was passed through a Jobin Yvon

Triax 320 monochromator (HORIBA Jobin Yvon Ltd.) to provide monochromatic light of the required wavelength. The resultant light then passed through a quartz window in the Cryostat to illuminate the devices through either the ITO (MIS/MIM devices) or the semi-transparent gate. The power of the light reaching the samples was measured using an Anritsu Optical Power Sensor MA9411A1 and Anritsu Optical Power Meter M-9001A (Anritsu Electric Co., Ltd.).

The temperatures at which samples were characterised were maintained with an Oxford Instruments Intelligent Temperature Controller (ITC502). The ITC502 was easily programmed to control temperatures in the range ~77–425 K. This arrangement allowed the annealing of samples under vacuum $< 10^{-5}$ Torr, typically at ~100°C for 1 hour, after which they slowly cooled down to 30°C. All devices were annealed in this manner.

3.5.2 AC Admittance

AC admittance was measured with a 100 mV a.c. signal at frequencies ranging from 1 Hz to 1 MHz . The a.c. signal was superimposed onto d.c. biases between ±40 V applied to the gate electrode. All measurements were performed using either an Agilent 4284A Precision LCR meter (Agilent Technologies UK Ltd.) or Solartron Frequency Response Analyser (1255) combined with the 1296 Dielectric Interface (Solartron Analytical).

3.5.3 Constant Capacitance

The transient response of semiconductor devices after, for example, photo-excitation can be measured by tracking the time dependence of the capacitance at a fixed bias. Alternatively, the time dependence of the bias necessary to maintain a constant capacitance can be tracked. These techniques are used in deep level transient spectroscopy (DLTS) to determine the characteristics of deep level impurities in inorganic Schottky and MIS diodes [146–148]. DLTS involves biasing a device into depletion whereupon carriers resulting from an excitation pulse can charge the traps. Subsequently, thermal emission of charges from these traps results in a measurable signal. Constant capacitance was first applied to organic MIS diodes by Taylor *et al.* to study de-trapping dynamics in P3HT [114].

In the constant capacitance method band bending (and hence depletion width) is kept constant by varying the bias using a feedback arrangement. Tracking the bias is accomplished using a proportional-integral-derivative (PID) controller in conjunction with an LCR meter (Figure 3.9). An error signal, determined as the difference between the measured and set capacitances is minimized by the PID controller by adjusting the DC bias applied to the sample. The output of the PID controller depends on three parameters:

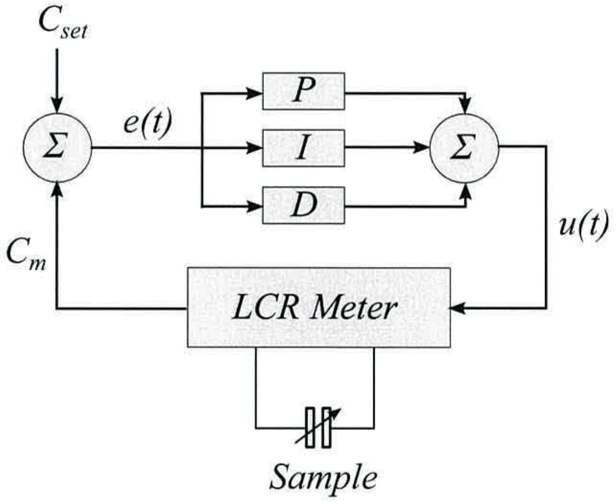


FIGURE 3.9: Block diagram of PID control system used in constant capacitance experiments.

- A proportional term, P, adds an element to the PID output proportional to the error, $e(t)$, at time t:

  $$P = K_p e(t), \tag{3.1}$$

  where K_p is the proportional gain.

- An integral term, I, which adds an element to the PID output derived from the integral of the error up to time t:

  $$I = K_i \int_0^t e(t)dt \tag{3.2}$$

  where K_i is the integral gain.

- A derivative term D, determined from the slope of the error at time t:

  $$D = K_d \frac{d}{dt} e(t), \tag{3.3}$$

  where K_d is the derivative gain.

These terms are summed to provide the output $u(t)$ of the PID controller:

$$u(t) = P + I + D \tag{3.4}$$

3.5.4 DC Measurements

Current–Voltage (IV) characterisation of samples were performed using the same set-up as in Figure 3.8, except that the IV measurements were recorded with either a Keithley Model 617 Electrometer or Keithley SCS 4200 Semiconductor Characterisation System (Keithley Instruments, Inc.). Current was measured at the semiconductor contact whilst the gate was subject to a d.c. bias swept between ±40 V.

Chapter 4

Electrical Characterisation of MIS Capacitors

4.1 Introduction

In this chapter the (dark) properties of metal-insulator-capacitor (MIS) devices are determined from their admittance spectra. MIS capacitors were made from regioregular poly(3-hexylthiophene) (P3HT) spin cast onto two different polymeric dielectrics; the epoxy photoresist SU8 (using both a thinned solution of SU8 2002 (SU8-1) and the newer SU8 2000.5 (SU8-2) and an organosilane, polysilsesquioxane (PSQ). Devices with PSQ and SU8-1 insulators were fabricated as detailed in Chapter 3. For the devices with SU8-2 insulators, the P3HT layer was spin-cast and annealed in a nitrogen glovebox. Devices were then transferred, without exposure to air, into a Kurt Lesker thermal evaporator, whereupon a 50 nm thick gold layer was evaporated through a shadow mask to form 2 mm diameter circular ohmic contacts.

Before annealing, excess P3HT surrounding the electrodes was carefully removed in an attempt to reduce the effects of lateral conduction. As P3HT is known to be highly sensitive to both oxygen and water [137, 149, 150], samples were annealed by heating at 100 °C for 1 hour under vacuum. Samples were left to slowly cool to 30 °C prior to measurement.

All measurements were performed in the dark and under high vacuum ($< 10^{-5}$ Torr) in an Oxford Instruments cryostat. Sample temperature was controlled using an Intelligent Temperature Controller (Oxford Instruments ITC503). Impedance measurements were taken using either a Solartron 1255A Frequency Response Analyzer (FRA) with 1296A Dielectric Interface System, or an Agilent 4284A precision LCR bridge. Current-Voltage measurements were made using either a Keithley SCS4200 Semiconductor Parameter Analyzer or Keithley model 617 Electrometer.

4.2 MIM Capacitors

The frequency dependence of capacitance and dissipation factor (tan δ) of Metal-Insulator-Metal (MIM) capacitors, fabricated as detailed in Section 3.3 with PSQ, SU8-1 and SU8-2 as the dielectric layers, are shown in Figure 4.1. The results for SU8-1 only cover the frequency range 100 Hz to 1 MHz as they were obtained with the Agilent 4284A (which provided noisy data at frequencies below 100 Hz), whereas the results for SU8-2 and PSQ were recorded over a broader spectrum from 1 Hz to 1 MHz using the FRA. However the capacitance plots for both SU8-1 and SU8-2 are parallel up to ~400 kHz indicating a weak frequency dependence of the dielectric constant for SU8 and good electrical consistency between batches. A much weaker dispersion was displayed by the PSQ MIM. At frequencies above ~10 kHz the decreasing capacitances of all devices coincide with increasing tan δ, which can be attributed to the series resistance of the ITO gate and contact effects. At frequencies below 1 kHz, tan δ is fairly constant (although small dispersions are evident at mains frequency harmonics) for all MIM structures. Tan δ for the PSQ device ranged between $\sim 1 \times 10^{-3}$ and $\sim 3 \times 10^{-3}$ between 1 Hz and 1 kHz, whereas both SU8-1 and SU8-2 had slightly higher tan δ values from $\sim 5 \times 10^{-3}$ to $\sim 8 \times 10^{-3}$. The capacitance for the PSQ MIM at 1 kHz was 173 pF from which the layer thickness was estimated to be ~482 nm (assuming $\varepsilon_r \sim 3$ for PSQ [151]). Capacitances of 188 pF and 172 pF yield layer thicknesses of ~517 nm and ~565 nm for the SU8-1 and SU8-2 MIMs respectively (assuming $\varepsilon_r = 3.5$ at 10 kHz for SU8 [152]).

I-V characteristics (Figure 4.2) also revealed the D.C. leakage current through the SU8-2 MIM was ~100 × the leakage current through the PSQ layer (at gate voltages of ±30 V). The D.C. resistance of the PSQ MIM, R_{dc}, was found to be $\sim 1.5 \times 10^{11}\,\Omega$, from which its D.C. resistivity, ρ_{dc} was calculated to be $\sim 9.8 \times 10^{13}\,\Omega$cm. This was approximately an order of magnitude higher than the

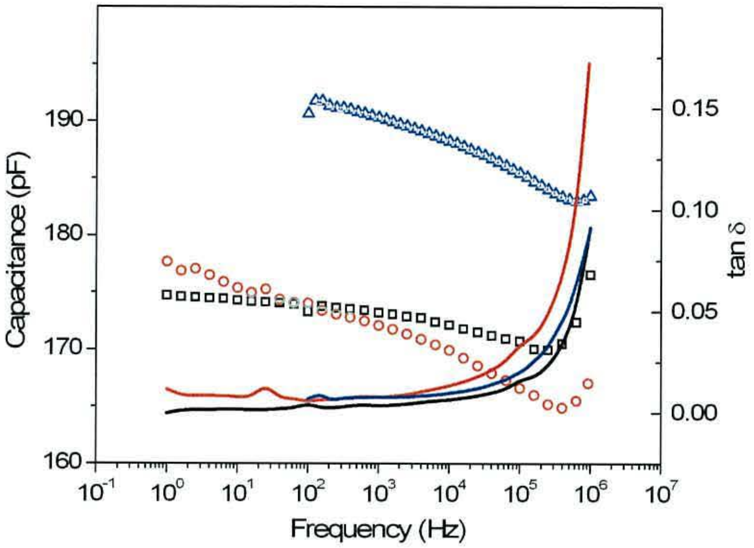


FIGURE 4.1: Frequency dependence of capacitance and tan δ of PSQ (black squares and line), SU8-1 (blue) and SU8-2 (red) MIM capacitors.

dc resistance of the SU8-2 MIM, with R_{dc} estimated to be $\sim 1.2 \times 10^{10}\,\Omega$ and ρ_{dc} to be $\sim 6.7 \times 10^{12}\,\Omega$cm. The low frequency (10 Hz) a.c. resistances, R_{ac}, of both the PSQ and SU8-2 layers are similar in value to their respective D.C. resistances. For the PSQ MIM R_{ac} was estimated to be $\sim 5.7 \times 10^{10}\,\Omega$ which was approximately 5× higher than the a.c. resistance of the SU8-2 MIM device ($\sim 1.2 \times 10^{10}\,\Omega$).

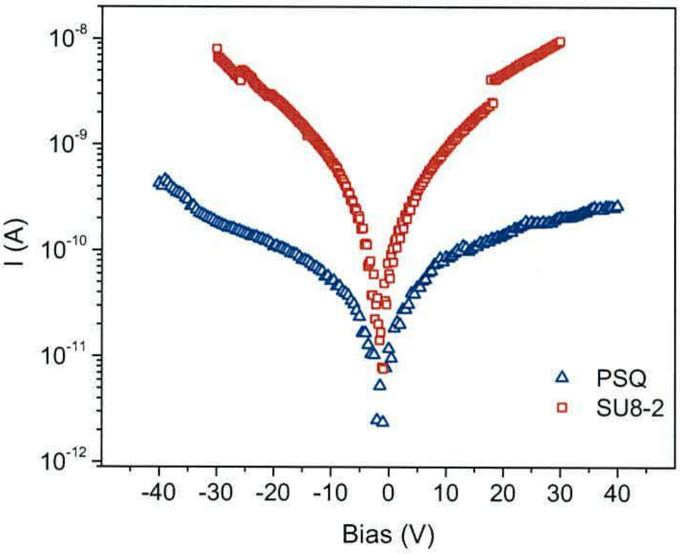


FIGURE 4.2: Current-Voltage I-V plots of PSQ (blue) and SU8-2 (red) MIM capacitors, acquired at 0.5 V/s.

4.3 PSQ/P3HT MIS Capacitors

This section provides electrical characterisation of the PSQ/P3HT MIS capacitors used in the photo-capacitance experiments reported in Chapter 5.

4.3.1 Voltage dependence of Capacitance and Loss

Capacitance and loss *vs.* voltage plots, where the bias was swept from -10 V to 20 V and back to -10 V, for a typical PSQ/P3HT MIS capacitor are shown in Figure 4.3 and are reminiscent of similar PSQ/P3HT MIS devices reported by Torres and Taylor [75]. The *C-V* plot (blue line) shows a transition from accumulation to depletion, characteristic of p-type semiconductor devices, which occurred between ~0 V and ~7.5 V for the device shown. Minimal anti-clockwise hysteresis between forward and reverse *C-V* sweeps suggests a small number of electrons had become trapped in the insulator at high positive biases. The depletion slope of the return sweep also broadened slightly, and coincided with a slight increase in the height and width of the loss peak (red line) implying the trapped electrons had increased the density of interface states interacting with the majority carriers (holes).

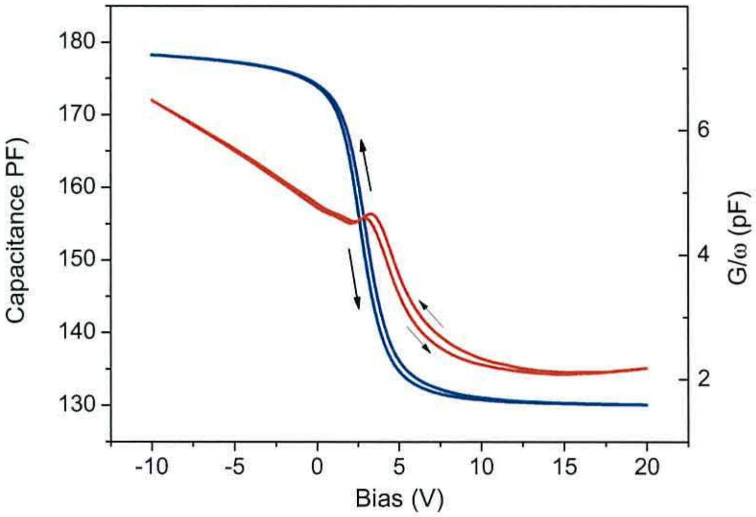


FIGURE 4.3: Capacitance (blue) and loss (red) of the PSQ MIS capacitor with the bias swept from -10 V to 20 V and back to -10 V, with a small signal frequency of 1 kHz.

At biases > 10 V the semiconductor reached full depletion with the measured capacitance reaching a minimum value, ~130 pF, remaining virtually constant as the bias was swept to higher positive voltages. This capacitance is the series sum of the insulator capacitance, C_I ~178 pF, and depletion capacitance, C_D, from which C_D is estimated to be ~480 pF. In fully depleted thin film devices the depletion width corresponds to the thickness of the active layer [79, 114], hence the P3HT layer thickness is estimated to be ~170 nm (assuming a dielectric constant of ~3 for P3HT [153]).

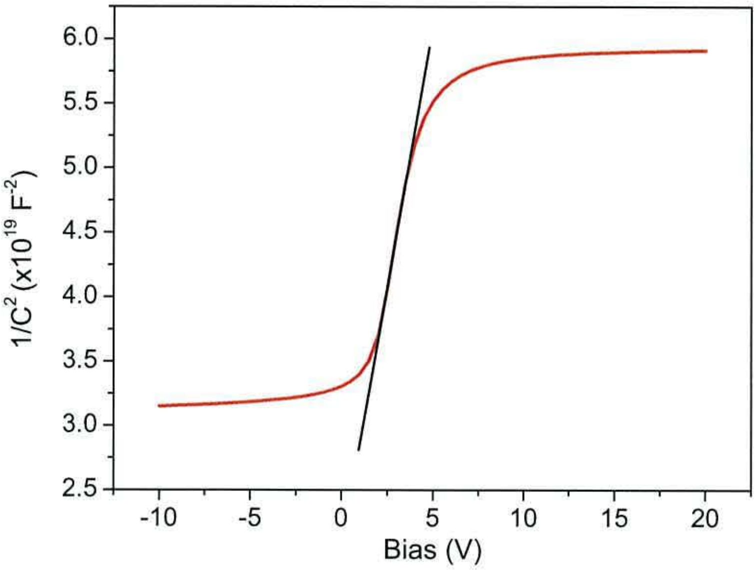


FIGURE 4.4: Mott-Schottky plot of forward sweep of *C*-*V* data from Figure 4.3, indicating slope from which N_A was determined to be $\sim 9 \times 10^{15}$ cm^{-3}.

As outlined in Chapter 2, the acceptor doping density, N_A, of the P3HT layer can be determined from a Mott-Schottky plot, provided the measurement frequency is at least an order of magnitude below the Maxwell-Wagner (M-W) dispersion [73]. Analysis of the *C*-*f* data, detailed below, revealed a M-W relaxation at ~40 kHz, thus N_A can be extracted from the *C*-*V* data obtained at 1 kHz. Here N_A was determined from the forward sweep of the *C*-*V* data, replotted in Mott-Schottky format ($1/C^2\, vs.\, V$) in Figure 4.4, to be $\sim 9 \times 10^{15}$ cm^{-3}. This is comparable to densities of $\sim 5 \times 10^{15}$ cm^{-3} reported in the literature (for example refs [73, 75, 154]).

The small peak in the loss-voltage plot is a characteristic feature of interface states [64]. As explained in Chapter 2, the loss peak occurs at a bias and, consequently, majority carrier concentration, where the capture rate of interface traps is comparable to the applied frequency. As the bias is swept from accumulation to depletion, the majority carrier density at the interface reduces, causing capture rates of interface traps within a few kT/q of the Fermi level to slow down producing a loss peak. With further increases in bias, the capture and emission of carriers from traps is negligible, and the loss is low. The density of interface states, D_{IT}, was estimated to be $\sim 8 \times 10^9$ cm^{-2}eV^{-1} using the Hill and Coleman (HC) approximation. D_{IT} determined at this frequency is at the lower threshold of densities for which the approximation is valid [106], and an order of magnitude lower than values reported by Alves and Taylor [105] using the conductance method advocated by Nicollian and Goetzberger [102]. Alves and Taylor commented that semiconductor bulk conduction losses can distort the loss peak at frequencies near the M-W dispersion, making it difficult to extract the peak from the background, which may be the reason such a low value for D_{IT} was obtained for this device. Figure 4.5 shows the C-V (blue line) and G/ω-V (red line) for the same device measured with an a.c. frequency of 105 Hz. Although the background loss is slightly higher at this frequency, the loss peak is much better defined from which D_{IT} is estimated to be $\sim 1.22 \times 10^{10}$ cm^{-2}eV^{-1} using HC analysis. D_{IT} obtained at this frequency is higher than the value determined at 1 kHz. It should be noted, though, that the loss peaks occurred at different gate biases, indicating traps at different energies were being probed. D_{IT} at 105 Hz corresponded to a trap depth of $\sim$0.36 eV, whereas at 1 kHz shallower traps at $\sim$0.22 eV were being probed. It is interesting to note that at 105 Hz the device exhibited no hysteresis in the C-V curve.

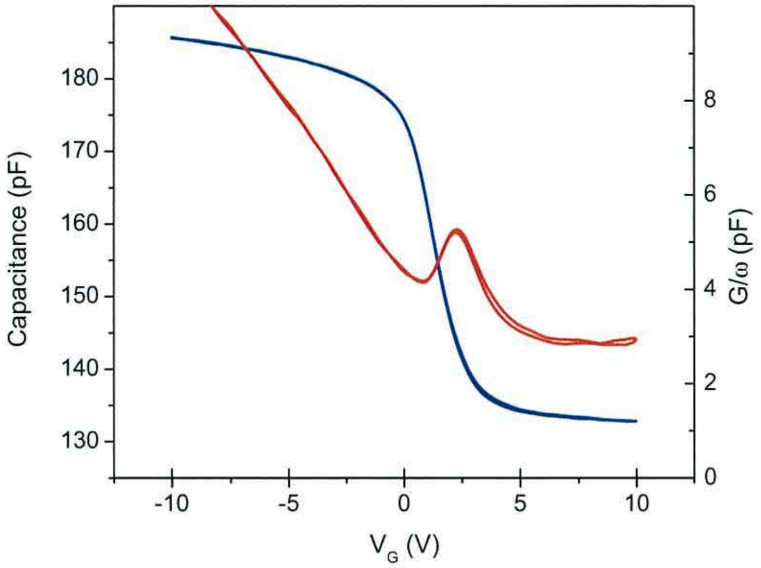


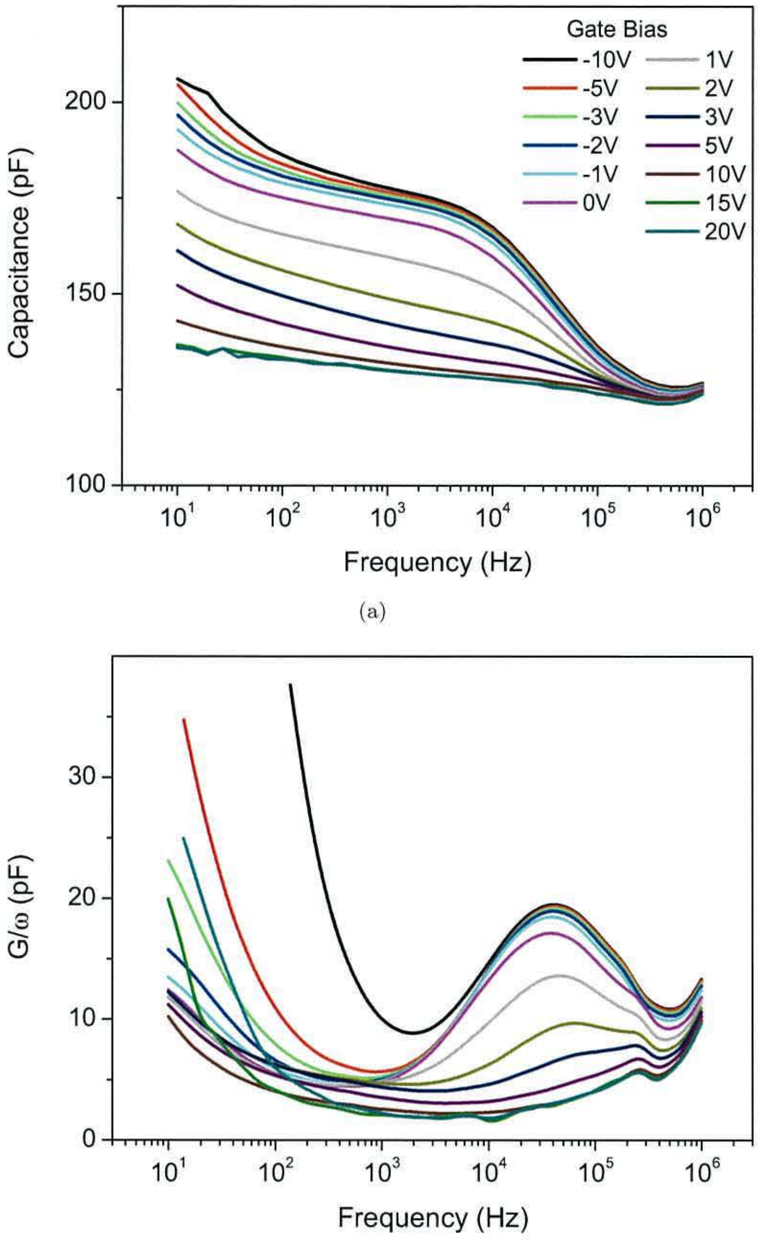
FIGURE 4.5: C-V (solid blue line) and G/ω-V (solid red line) for PSQ/P3HT MIS capacitor obtained at an a.c. frequency of 105 Hz.

4.3.2 Frequency Dependence of Capacitance and Loss

The frequency dependence of capacitance and dielectric loss of a PSQ/P3HT MIS capacitor obtained over a range of gate bias voltages are presented in Figure 4.6. The response features a classic Maxwell-Wagner dispersion, typical of a two-layer capacitor. As discussed in Chapter 2 such a response can be represented by the equivalent circuit in Figure 2.8 with a relaxation frequency, f_R, given by Equation 2.17. The loss curves in Figure 4.6(b) show f_R to be virtually constant, ~40 kHz, for accumulation voltages between -10 V and -2 V, indicating the semiconductor resistance, R_B, was not affected by the applied voltages. In the accumulation regime, any charges injected into the semiconductor from the ohmic contact would cause R_B to decrease with a corresponding increase in f_R [87].

The loss curves in Figure 4.6(b) show that the device began depleting at ~0 V. Further positive increases in bias drove the device deeper into depletion, with the corresponding M-W peaks shifting to higher frequencies due to the growing depletion layer, in agreement with Equation 2.20. Correspondingly, the measured capacitance at low frequencies was seen to decrease, confirming the evolution of a depletion layer. At bias voltages > 10 V, little further reduction in the measured capacitance was seen, indicating the device had fully depleted.

At 1 kHz, with the device in accumulation, the measured capacitance increased from ~178 pF to over 206 pF at 10 Hz. This was accompanied by a large increase in loss over the same frequency range, which may be attributed to a combination of lateral conduction in the P3HT surrounding the gold contact and DC conduction through the insulator. Assuming the capacitance measured in accumulation ($V_G = -10$ V) at 1 kHz is C_I, ~178 pF, the insulator layer thickness was calculated to be ~470 nm. At frequencies above ~10 kHz majority carriers are unable to follow the ac signal and the capacitance falls to the geometric capacitance of the device (series sum of C_I and C_B), ~130 pF, from which C_B was estimated to be ~480 pF and the P3HT layer thickness ~170 nm. These results are in agreement with the parameter values extracted from the C-V curves above. With the device in accumulation f_R was ~40 kHz, from which R_B was determined using Equation 2.17 to be ~6 kΩ. Bulk conductivity, σ_B, was calculated to be ~8.9×10^{-8} S cm^{-1} using Equation 2.22. Similar conductivities were reported for P3HT MIS devices with a Novolac® dielectric [73, 81].



(a)

(b)

FIGURE 4.6: (a) C-f and (b) G/ω-f response of PSQ/P3HT MIS capacitor at different gate biases, measured at 303 K.

Despite the high loss at low frequencies, a small dispersion is evident at ~400 Hz for biases ~2–3 V, i.e. when the device was biased into depletion. These are the same voltages at which the loss peaks were seen in the C-V plots in Figures 4.3 and 4.5, and confirm the presence of interface states.

A further dispersion is seen at high frequencies > 500 kHz caused by a contact resistance R_C associated with the ITO and gold contacts in series with the device, with a relaxation frequency $\gg$ 1 MHz, indicating $R_C \ll 1$ kΩ (from Equation

2.25). The peaks appearing at ~300 kHz at all applied biases is attributed to artefacts within the measurement system.

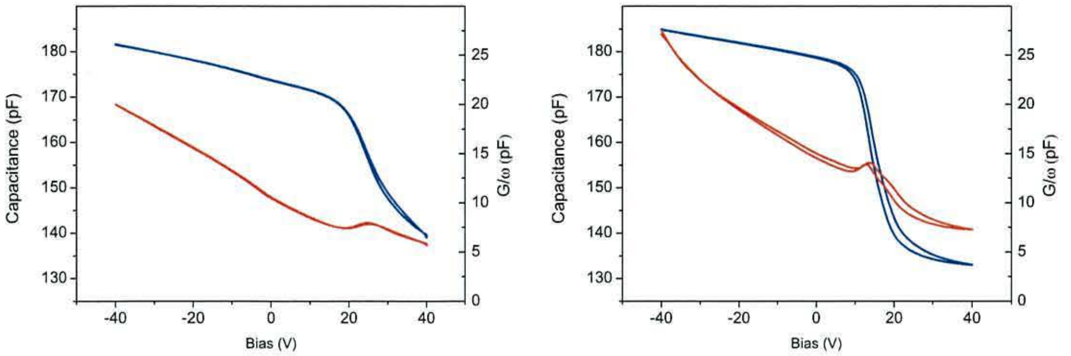
4.4 SU8/P3HT MIS Capacitors

The electrical characteristics, measured in the dark, of SU8/P3HT MIS capacitors used for the photo-experiments in Chapter 5 are presented in this section.

4.4.1 Admittance Results of SU8-1/P3HT Capacitors

SU8/P3HT MIS capacitors were fabricated using thinned SU8-2002 photoresist (SU8-1) as the insulating layer. Cross-linking of the SU8-1 layer was initiated by exposure to UV light from an old mask aligner (OMA), for which the light power was unknown. The capacitance-voltage and loss-voltage curves in Figures 4.7(a) and 4.7(b) show the results of two devices whose SU8-1 layers had been exposed under the OMA for (a) 1 minute (device SU8-1A) and (b) 2 minutes (device SU8-1B). Both devices had completed four annealing cycles under high vacuum for 1 hour at 100 °C prior to the *C-V* measurements shown in the figures. Both *C-V* plots (blue line in Figure 4.7) show the behaviour typically seen in p-type MIS capacitors where the device transitions from accumulation through to depletion as the gate bias is swept to more positive voltages. However these plots revealed high flatband voltages in both devices, ~20 V and ~11.5 V for the SU8-1A and SU8-1B devices respectively. Neglecting the difference in work functions between the ITO gate and semiconductor, such that an ideal MIS capacitor has $V_{FB} = 0$ V, then approximately 7.2×10^{11} electrons cm^{-2} were trapped, either in the insulator or at the SU8-1/P3HT interface in device SU8-1A and ~4.2×10^{11} cm^{-2} in device SU8-1B. Due to the high V_{FB} device SU8-1A did not fully deplete within the available voltage range. Interestingly, organic FETs utilising SU8 as the dielectric layer and P3HT as the semiconductor exhibited high positive threshold voltages ~75 V [141].

Anticlockwise hysteresis in the *C-V* plot of SU8-1B (blue line in Figure 4.7(b)) is a result of electron trapping either in the insulator or at the SU8-1/P3HT interface. The depletion slope on the reverse sweep (+40 V to -40 V) exhibits a shallower slope, which is reflected by the broader, and slightly higher, peak in



(a) (b)

FIGURE 4.7: C-V (blue lines) and G/ω-V (red) plots for SU8 MIS capacitors (a) with SU8-1 layer exposed to UV light for 1 minute (device SU8-1A) and (b) exposure for 2 minutes (device SU8-1B). Both plots were obtained after four annealing cycles, measured at a temperature of 303 K, with an a.c. frequency of 1 kHz.

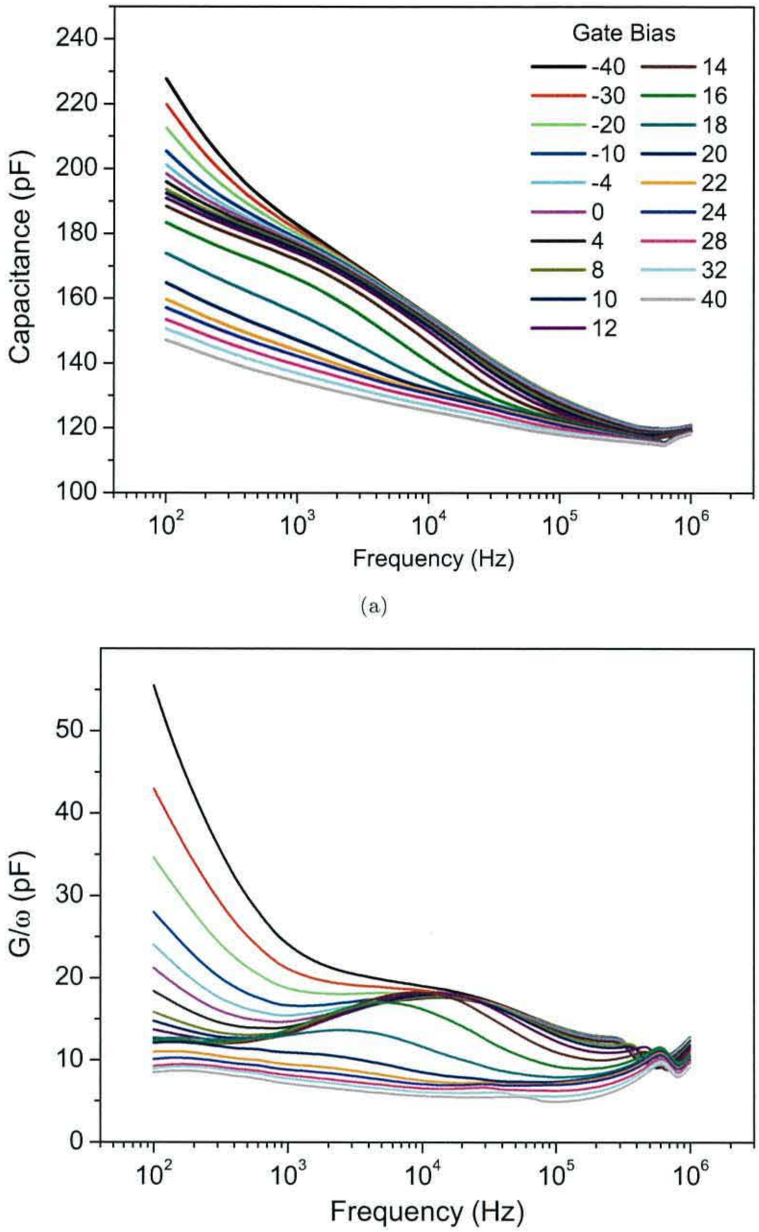
the accompanying loss curve (red line), indicating increased interaction between holes and interface states.

In accumulation both the capacitance and loss increased with increasing accumulation voltages. Such an effect can be attributed to lateral conduction [87, 88]. Also visible in the loss curves are small peaks coincident with the depletion slope in the C-V plots, indicating the presence of interface states.

The capacitance measured in accumulation was ~181 pF for SU8-1A and ~184 pF for SU8-1B. Assuming these values $\approx C_I$, then the thicknesses of the insulating layers were estimated to be ~560 nm and ~520 nm respectively. As discussed above SU8-1A did not reach full depletion, however at biases > ~25 V device SU8-1B approaches full depletion and taking the minimum capacitance at 40 V, ~133 pF, C_D is estimated to be ~480 pF, corresponding to a maximum depletion layer width of ~170 nm.

The C-f and G/ω-f plots for SU8-1B are provided in Figure 4.8. Four dispersions are evident in the loss curves:

(1) High loss dominates the response at low frequencies. As the applied voltage biases the device from strong accumulation (-40 V) towards V_{FB}, both the magnitude and relaxation frequency of the dispersion decreases due to lateral conduction in the excess P3HT surrounding the gold contact and DC losses through the insulator at accumulation voltages up to 12 V.



(a)

(b)

FIGURE 4.8: Frequency dependence of capacitance (C-f) and loss (G/ω-f) for device SU8-1B, obtained over a range of voltages from -40 V to +40 V.

(2) A second dispersion, between 100 Hz and 200 Hz, appears with the device in depletion. However, the dispersion described in (1) could be masking any contribution from this process in the accumulation regime. This dispersion occurs at the same frequency for biases in the depletion regime which is the signature for bulk traps in silicon MOS capacitors [64]. As detailed in Chapter 2, when a device is biased into depletion, traps located within a few kT/q of the energy where the Fermi level crosses the bulk trap level (crossover point) can contribute to the

admittance, and the associated loss occurs at the same frequency, independent of bias.

(3) A broad Maxwell-Wagner (M-W) dispersion, whose relaxation frequency, f_R ranged from ~20 kHz in accumulation to ~3 kHz in depletion. The broad M-W dispersion can be ascribed to energetic disorder and the hopping nature of charge transport in organic semiconductors, which cause charge carriers to respond to an ac signal with a distribution of relaxation times centred around f_R [78]. For accumulation voltages, -40 V to +8 V, the loss peaks superimposed. However, as the device was driven into depletion, the M-W peak shifted to lower frequencies, contrary to the expected response described in Chapter 2. This behaviour is similar to that reported by Torres and Taylor for P3HT MIS capacitors with a PSQ insulator, which was attributed to increasing disorder in the active layer upon moving away from the interface, resulting in increased resistivity and time constant dispersion in the P3HT layer [75]. For P3HT diodes with a polyimide dielectric, though, the shift in f_R to lower frequencies was attributed to the influence of interface states as the device was driven into depletion [78].

(4) A final dispersion can be seen for all curves at frequencies above the M-W peaks, caused by a series resistance associated with the contacts with a relaxation frequency $\gg$1 MHz.

Doping density, N_A, was determined to be ~2.6 $\times 10^{16}$ cm^{-3} from the linear part of the slope of the Mott-Schottky plot (not shown).

A further set of devices (SU8-1C) were fabricated where the SU8-1 layer was exposed to UV light using an EVG620 mask aligner at a known dosage of 120 mJ cm^{-2}. The C-V and G/ω-V plots in Figure 4.9 show V_{FB} was ~0 V after annealing. This result suggests that the high V_{FB} recorded in devices SU8-1A and SU8-1B resulted from under-exposure to UV light. SU8 contains triarylsulfonium salts of hexafluoroantimonate (SbF_6^-) used as photo-initiators for the cross-linking process, which form neutral or positively ionized products upon exposure to UV light [155]. The negative charges responsible for the high V_{FB} found in SU8-1A and SU8-1B could be a result of un-reacted photo-initiator remaining in the SU8 layer after exposure and thermal curing.

C_I for this device was ~99 pF from which the dielectric layer thickness was determined to be ~970 nm. In depletion the capacitance fell to a minimum value ~81 pF, from which C_D was deduced to be ~446 pF corresponding to a P3HT

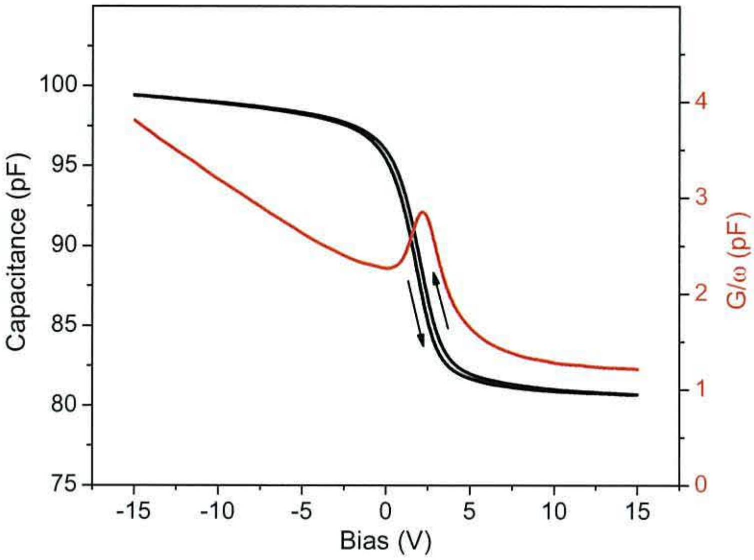


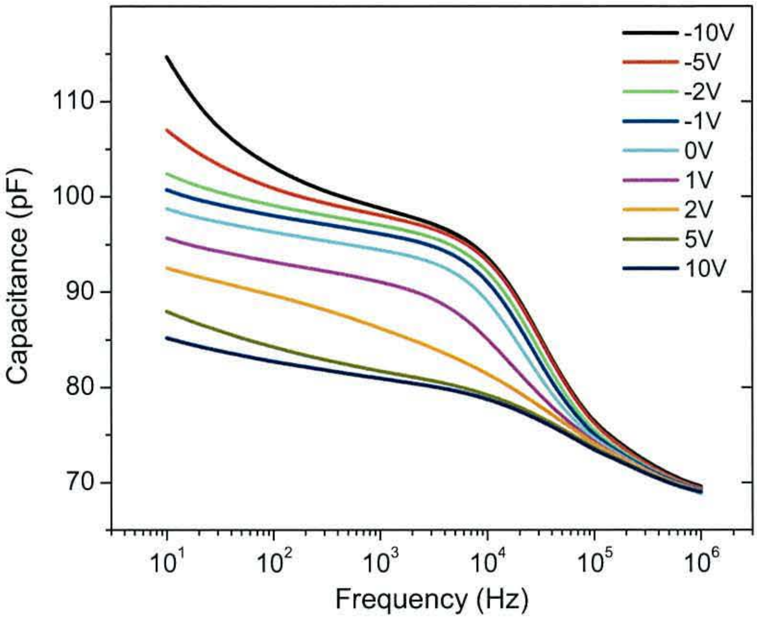
FIGURE 4.9: C-V (solid blue line) and G/ω-V (solid red line) for the UV-exposed device SU8-1C, measured after annealing with an a.c. frequency of 1 kHz, at a temperature of 303K.

layer thickness of ~187 nm. Acceptor doping density, N_A, was determined from the Mott-Schottky plot to be ~3.5×10^{15} cm^{-3}. The low value of N_A for this device indicates that dopants from the insulator may be responsible for the higher N_A deduced for the SU8-1B device. The peak in the G/ω-V plot at depletion voltages indicates the presence of interface states. D_{IT}, was estimated, using the HC approximation, to be ~2.4×10^{10} cm^{-2} eV^{-1}.

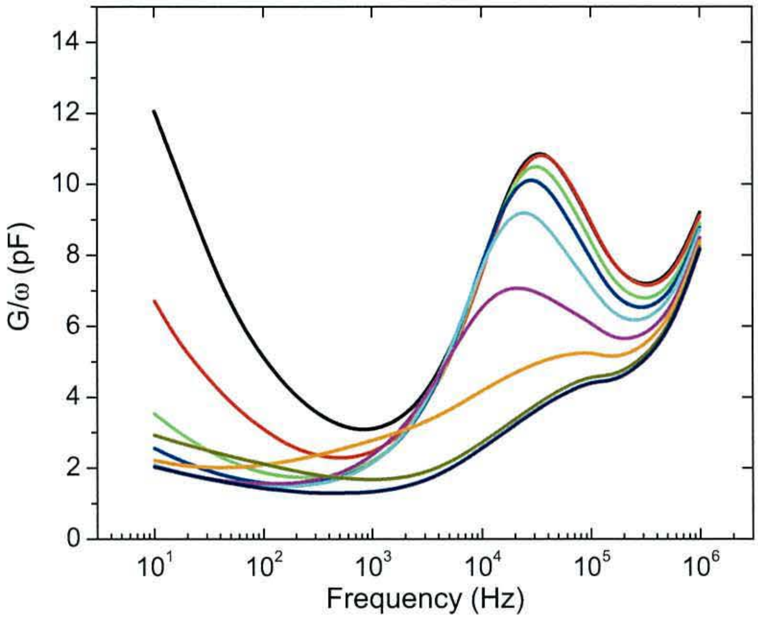
The frequency dependence of capacitance and loss are plotted in Figure 4.10 for a range of voltages where the device was biased from accumulation at -10 V, through to full depletion at + 10 V. Three main dispersions are apparent:

1. At low frequencies (< ~500 Hz) both the capacitance and loss increase, especially at accumulation voltages, consistent with a combination of lateral conduction and DC conduction through the SU8 layer.

2. A classical Maxwell-Wagner dispersion in the frequency range ~33 kHz to ~100 kHz. At a bias of > ~0 V the C-f plot shows the measured capacitance had decreased, indicating the formation of a depletion region. With increasing positive voltages, the depletion layer extends further into the semiconductor and f_R of the M-W dispersion shifts to higher frequencies, as predicted by Equation 2.20. In accumulation the M-W peaks moved to higher frequencies with increasingly negative gate voltages. This suggests, from Equation 2.17, that the resistivity of the P3HT layer was decreasing.



(a)



(b)

FIGURE 4.10: Frequency dependence of capacitance (C-f) and loss (G/ω-f) for device SU8-1C. Gate voltages ranged from -10 V to +10 V.

3. At ~10 kHz the loss rises to a peak centred around a frequency greater than 1 MHz resulting from a series resistance at the contacts, and is accompanied by a corresponding decrease in capacitance.

4.4.2 MIS Capacitors with SU8 2000.5 as Dielectric

MIS capacitors with SU8 2000.5 photoresist (SU8-2) as the insulating layer were fabricated as described under an inert atmosphere in an N_2 glovebox. The SU8 layer was subjected to a UV dosage of 60 mJ cm^{-2}, according to the datasheet [156]. Capacitance and loss *vs.* voltage plots are shown in Figure 4.11. The measurement frequency was set at 83 Hz due to the low frequency of the M-W dispersion in Figure 4.12. V_{FB} for this device was ~3 V, confirming the high V_{FB} seen in previous SU8-1 devices was indeed caused by under exposure of the SU8.

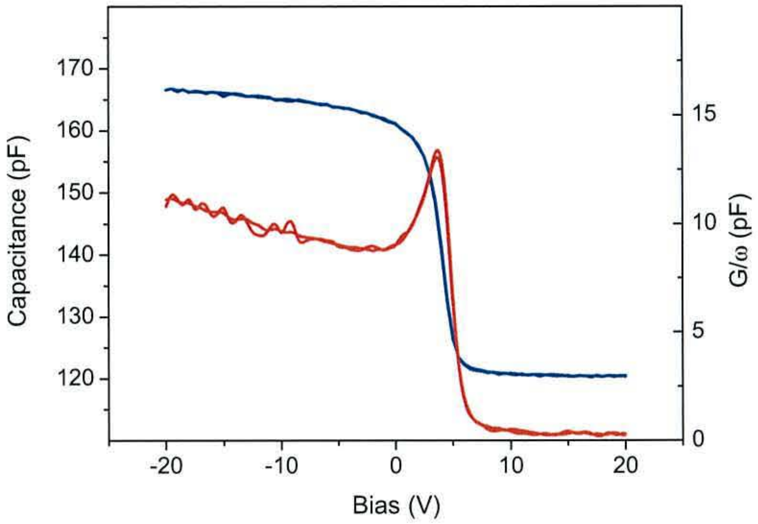
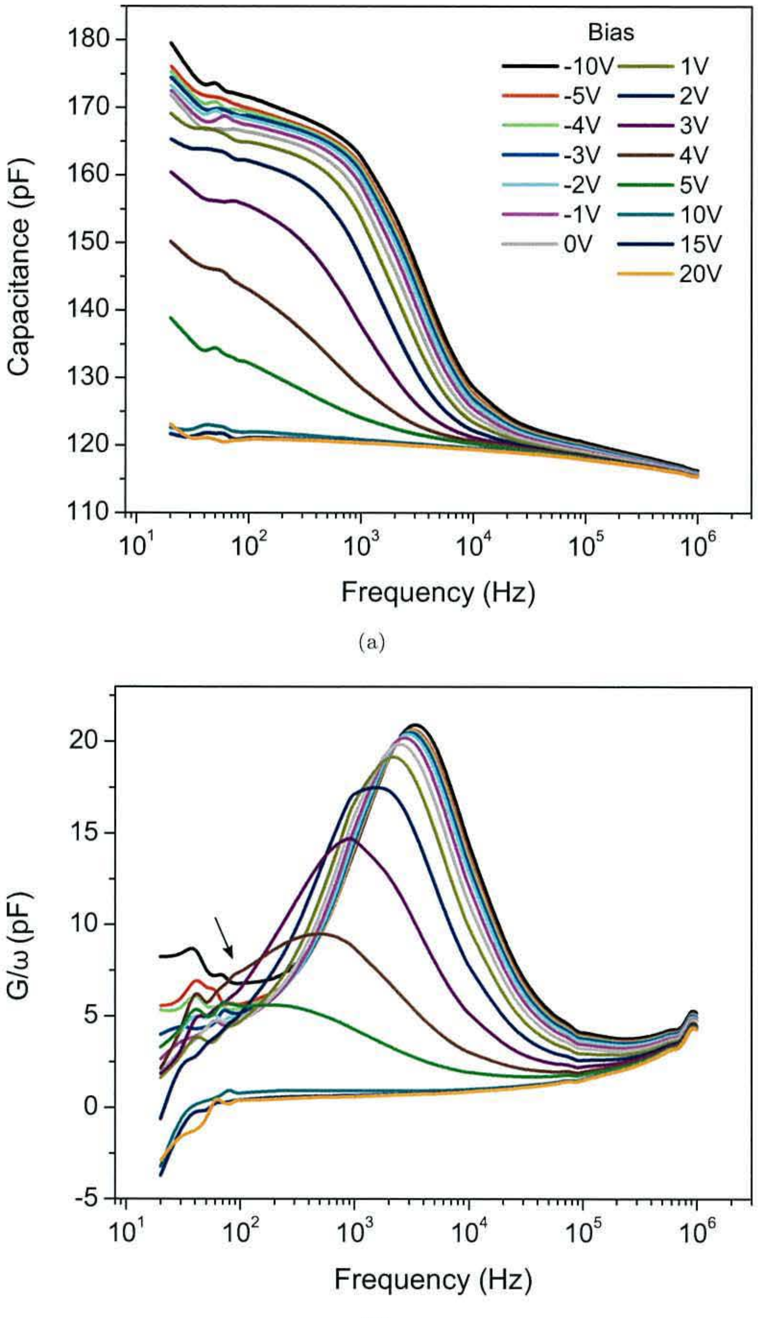


FIGURE 4.11: C-V (solid blue line) and G/ω-V (solid red line) for device SU8-2, obtained after annealing and then cooling to 303 K. The bias was swept from -20 V to +20 V and back to -20 V. The a.c. frequency was 83 Hz.

From the maximum capacitance in accumulation, ~167 pF, corresponding to C_I, the insulator thickness was ~570 nm. C_D was deduced to be ~426 pF from the series sum of C_I and the minimum measured capacitance (~120 pF). The thickness of the P3HT is then estimated to be ~195 nm. Acceptor doping density, determined from the Mott-Schottky plot was ~3.8×10^{15} cm^{-3}. The density of interface traps was estimated to be ~$1.3 \times 10^{11} cm^{-2}$ eV^{-1}, located ~0.5 eV above the bulk Fermi level.

The M-W relaxation frequency in this device was ~3.5 kHz in accumulation, decreasing to ~200 Hz in depletion, which again is in disagreement with analysis of the equivalent circuit in Chapter 2 (Figure 2.20). As the applied bias drives the MIS device further into depletion the peak broadens and becomes more asymmetric for voltages >3 V, suggesting the loss is dominated by interface states [97]. A possible second dispersion can be seen at ~100 Hz (indicated by an arrow



(a)

(b)

FIGURE 4.12: Frequency dependence of capacitance (C-f) and loss (G/ω-f) for device SU8-2. Gate voltages ranged from -10 V to +10 V.

in the figure). Noting that the loss peak in Figure 4.11 occurs at ~3.5 V, this second dispersion appears to arise from the interaction of majority carriers (holes) with interface states.

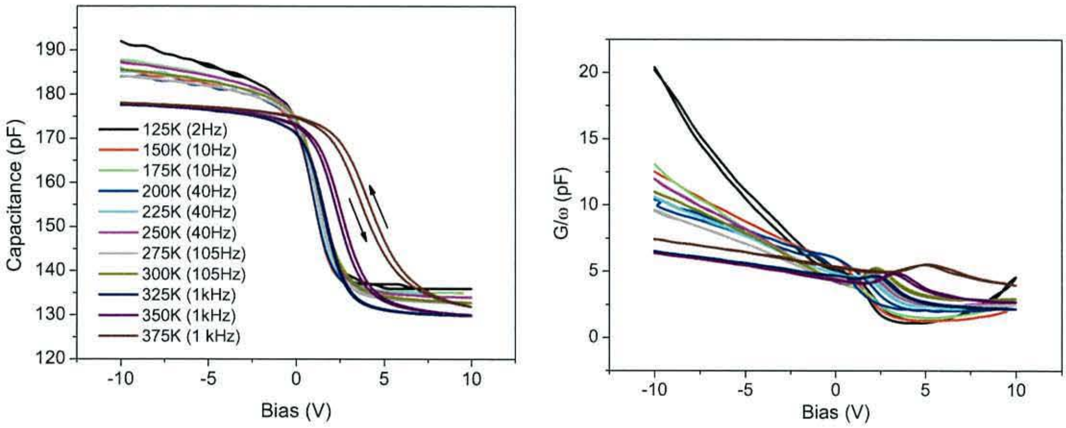
4.5 Thermal Stability of MIS Capacitors

In this section the thermal stability of MIS capacitors, with PSQ, SU8-1 and SU8-2 as the insulator and P3HT as the active layers, is reported, based on admittance measurements over a range of temperatures from 125 K to 375 K.

After reaching the desired temperature, the devices were left for at least 30 minutes, with the contacts shorted, prior to measurement. Each device was characterized starting at the lowest temperature, collecting the C-f and G/ω-f data first. The frequency of the C-V measurement was chosen to be at least an order of magnitude below the M-W peak in the G/ω-f plot, but high enough to avoid the low frequency losses caused by lateral and DC conduction.

4.5.1 Temperature Dependence of C-V and G/ω-V

4.5.1.1 PSQ/P3HT Capacitors



(a) (b)

FIGURE 4.13: Temperature dependence of (a) C-V and (b) G/ω-V of PSQ/P3HT MIS capacitor at temperatures ranging from 125 K to 375 K. Measurement frequency was set at least one order of magnitude below the M-W peak. Bias was cycled from -10 V to +10 V.

The temperature dependence of the C-V and G/ω-V curves over the range 125 K to 375 K of the PSQ/P3HT MIS capacitor are shown in Figure 4.13. For temperatures up to 325 K, the transitions from accumulation to depletion had very similar slopes, very little shift in V_{FB} was apparent and there was negligible hysteresis. Above 325 K V_{FB} shifted to slightly higher voltages, with anti-clockwise hysteresis also becoming noticeable. Shifts in V_{FB} and increasing hysteresis, with rising temperature, have been attributed to mobile ions in the dielectric [71, 80, 157]. Mobile ions in the insulator can be ruled out here as the observed shift in V_{FB} would be to more negative voltages, opposite to the applied voltage, whereas the positive shift in V_{FB} is consistent with negative charge trapping at the PSQ/P3HT interface [97]. At 375 K the observed shift of ~2.4 V is equivalent to ~8 $\times 10^{10}$ electrons trapped at the interface.

At temperatures < 225 K, the loss peaks are difficult to locate. Between 225 K and 325 K the loss peaks have similar magnitudes and occur at ~2–3 V. The width of the loss peaks increased at higher temperatures, accompanied by the stretching-out of the associated depletion slopes, suggesting interface states were active over a broader energy range. D_{IT} was estimated to be ~1.2 $\times 10^{10}$ cm^{-2}eV^{-1}, increasing only slightly to ~1.3 $\times 10^{10}$ cm^{-2}eV^{-1} at 375 K, as shown in Figure 4.14.

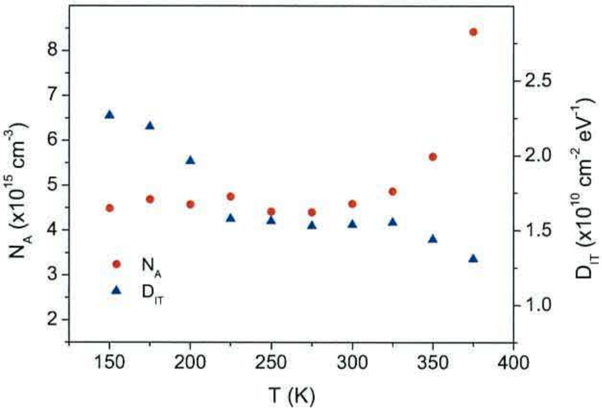
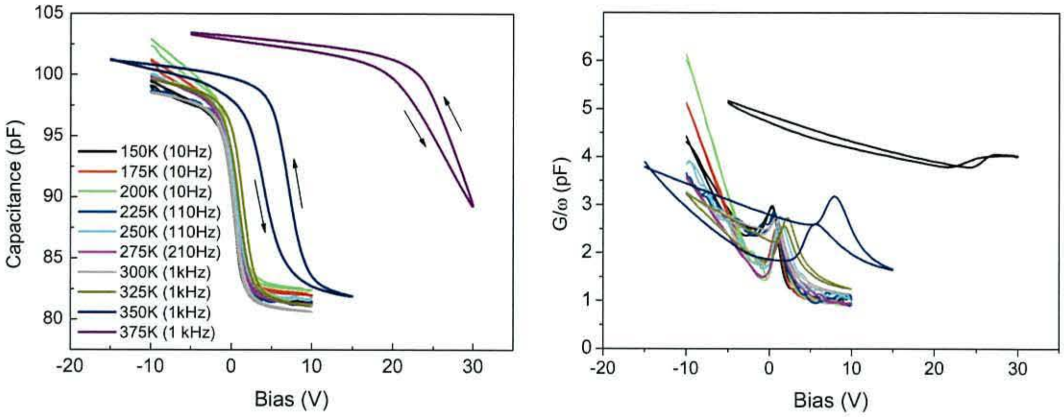


FIGURE 4.14: Acceptor doping density, N_A, and interface state density, D_{IT}, of PSQ MIS device determined from the C-V and G/ω-V curves at temperatures between 125 K and 375 K.

Mott-Schottky analysis of the C-V data reveals N_A remains fairly constant at ~4.6×10^{15} cm^{-3} up to 325 K (see Figure 4.14). Above 325 K, N_A increased to ~5.6×10^{15} cm^{-3} and ~8.4×10^{15} cm^{-3} at 350 K and 375 K respectively, however, these values are most likely over-estimated due to the influence of interface states at these temperatures.

4.5.1.2 SU8/P3HT MIS capacitors



(a) (b)

FIGURE 4.15: Temperature dependence of (a) *C*-*V* and (b) *G*/*ω*-*V* of SU8-1/P3HT MIS capacitor at temperatures ranging from 125 K to 375 K. Measurement frequency was set at least one order of magnitude below the M-W peak.

Capacitance-voltage and loss-voltage plots, obtained at temperatures between 150 K and 375 K, for an SU8/P3HT MIS capacitor are provided in Figure 4.15. This MIS device was similar to device SU8-1C reported in the previous section. Good stability is exhibited with the very little change in V_{FB} up to 325 K, where V_{FB} increased by ~0.5 V and some hysteresis became apparent. Above 325 K increases in V_{FB} are much larger, ~4 V at 350 K and ~29 V at 375 K, measured at the mid-point of the depletion slope, equivalent to $\sim 7.8 \times 10^{10}$ cm^{-2} and $\sim 5.7 \times 10^{11}$ cm^{-2} negative charges trapped at the interface. Such large increases in V_{FB} were not found in the PSQ/P3HT devices, and could therefore be caused by a thermally activated process in the insulator. Although based on a limited dataset, an activation energy of ~0.75 eV was estimated from an Arrhenius plot (Figure 4.16) of V_{FB}. Such a large value could indicate a mobile ionic species was responsible for the shift in V_{FB} [80, 157], however as remarked previously, mobile ions would cause a negative shift in V_{FB}. Remnant Lewis acids and/or water or other contaminants remaining within the SU8 after curing could be possible sources of negative charges resulting in the positive shift of V_{FB}. ITO has also been reported to interact with organic molecules [158], and the high activation energy found here could, perhaps, indicate a chemical reaction between the ITO gate and SU8 layer.

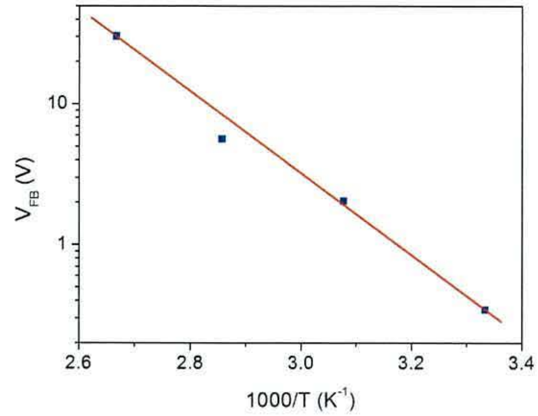


FIGURE 4.16: Arrhenius plot of flatband voltage, V_{FB}.

Peaks in the G/ω-V curves (Figure 4.15(b)) are apparent at all temperatures and remained fairly similar in magnitude up to 325 K. Above 325 K the loss peaks moved to more positive biases in unison with the shift in V_{FB}, together with a broadening of the width of the peaks, indicating that interface states with a broader range of energies were interacting with majority carriers at elevated temperatures. D_{IT} was estimated to be $\sim 2\times10^{10}$ cm^{-2}eV^{-1} at energies ~0.1-0.17 eV above the bulk Fermi level, over the temperature range 125 K to 375 K (Figure 4.17).

Figure 4.17 also shows the acceptor doping density was $\sim 2.9\times10^{15}$ cm^{-3} for temperatures up to 350 K. At 375 K, N_A increased to $\sim 1.7\times10^{16}$ cm^{-3}, which, similar to the PSQ/P3HT device, indicated the influence of interface states at higher temperatures.

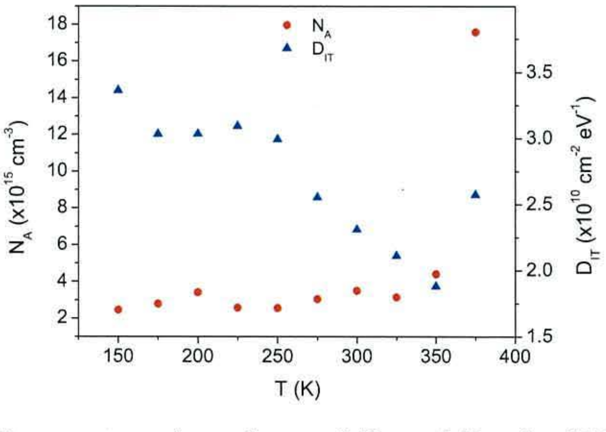
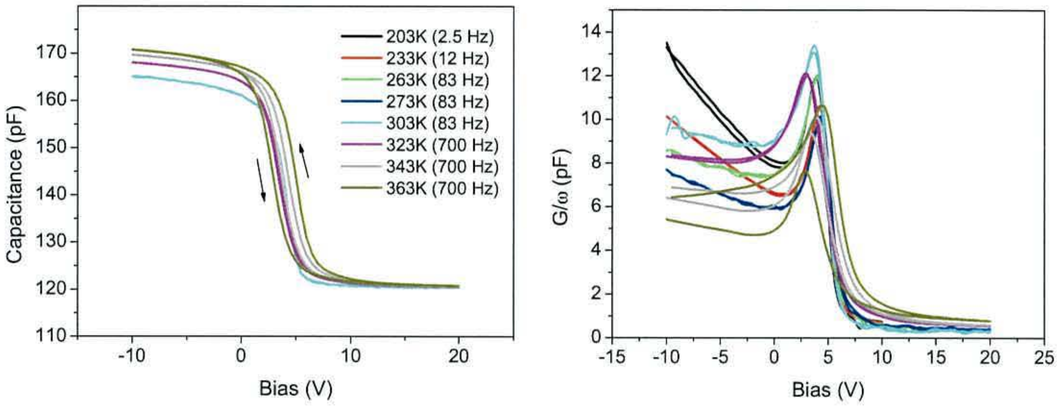


FIGURE 4.17: Temperature dependence of N_A and D_{IT} for SU8-1 MIS device.

4.5.1.3 SU8-P3HT Capacitor fabricated under N_2

The P3HT based MIS devices in Sections 4.5.1.1 and 4.5.1.2 were prepared and spin-coated under ambient conditions. During the latter stages of this work it became possible to deposit the P3HT in a nitrogen glovebox. The dielectric layer of SU8 2000.5 (SU8-2) and solution of P3HT in chloroform were prepared under ambient conditions as described in Chapter 3, before being transferred to the glovebox. P3HT solution was spin-coated and dried at 100°C for 1 hour in the glovebox. Samples were then transferred to a Kurt Lesker thermal evaporator, without exposure to air, whereupon 2 mm diameter, 50 nm thick, gold contacts were deposited.



(a) (b)

FIGURE 4.18: (a) *C*-*V* and (b) *G*/*ω*-*V* plots of SU8-2/P3HT MIS capacitor at temperatures between 200 K and 363 K. The P3HT layer was deposited under a N_2 atmosphere. Measurement frequency was set at least one order of magnitude below the M-W peak.

The *C*-*V* and *G*/*ω*-*V* plots recorded at temperatures between 203 K and 363 K are shown in Figure 4.18. As noted in the following section, the M-W relaxation frequency of these devices was lower than for either of the devices prepared under ambient, resulting in the need for much lower frequencies for the *C*-*V* measurements to avoid interaction with the M-W dispersion. Due to this constraint, measurements below 200 K were not possible.

Both the *C*-*V* and *G*/*ω*-*V* plots clearly show the device has much improved stability compared to the PSQ and SU8-1 devices. In the *C*-*V* plot, both the depletion slope and V_{FB} remain fairly constant over the entire temperature range, with negligible hysteresis ~0.5 V occurring at 343 K, increasing to ~2.1 V at

363 K. N_A was estimated to be $\sim 3.5\times10^{15}$ cm^{-3} up to 303 K after which it increased to $\sim 5\times10^{15}$ cm^{-3}, as presented in Figure 4.19.

The loss peaks in the G/ω-V plots are all of similar height, with D_{IT} estimated to be between $\sim 1\times10^{11}$ and $\sim 1.5\times10^{11}$ cm^{-2}eV^{-1} (Figure 4.19). These values are an order of magnitude higher than the density of interface states found in the devices fabricated under ambient, however these are shallower states, located ~0.04–0.06 eV above the bulk Fermi level. Increasing D_{IT} with decreasing trap depth has also been reported for P3HT based MIS capacitors by Torres and Taylor [75], where the density of shallow states was found to be two orders of magnitude higher than the density of deeper states.

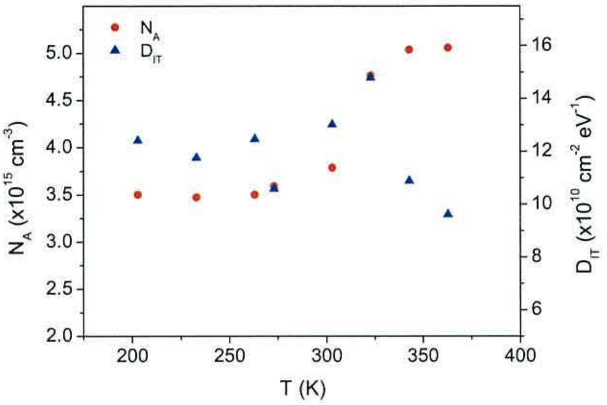


FIGURE 4.19: Temperature dependence of N_A and D_{IT} for SU8-2 MIS device.

4.5.2 Temperature Dependence of the Bulk Mobility

Conductivity, σ_B and mobility, μ_B, of the bulk semiconductor were extracted from the M-W relaxation frequencies, with the devices biased at flatband. Under this condition, there is no band-bending; the device will not be in accumulation when injection of charges into the bulk semiconductor is possible, or depletion. Injection of majority carriers (holes) would cause a reduction in the bulk resistivity and a corresponding increase in f_R, leading to overestimates of the bulk conductivity and mobility. The density of holes in the semiconductor will now be equal to the acceptor doping density, as determined from Mott-Schottky analysis of the C-V data. σ_B is then determined from the bulk resistance via Equation 2.22. Once σ_B is known, μ_B may be derived from the conductivity using Equation 2.23.

The frequency dependence of loss (G/ω-f) over a range of temperatures from 125 K to 375 K for the PSQ, SU8-1 and SU8-2, with the devices biased at V_{FB}, are plotted in Figures 4.20(a), 4.20(b) and 4.20(c) respectively. The plots clearly show a strong temperature dependence of the M-W relaxation frequency, which changes by more than four orders of magnitude over the temperature range for each device. Such behaviour is typical of the thermally activated hopping nature of charge transport in disordered semiconductors [73, 81, 154].

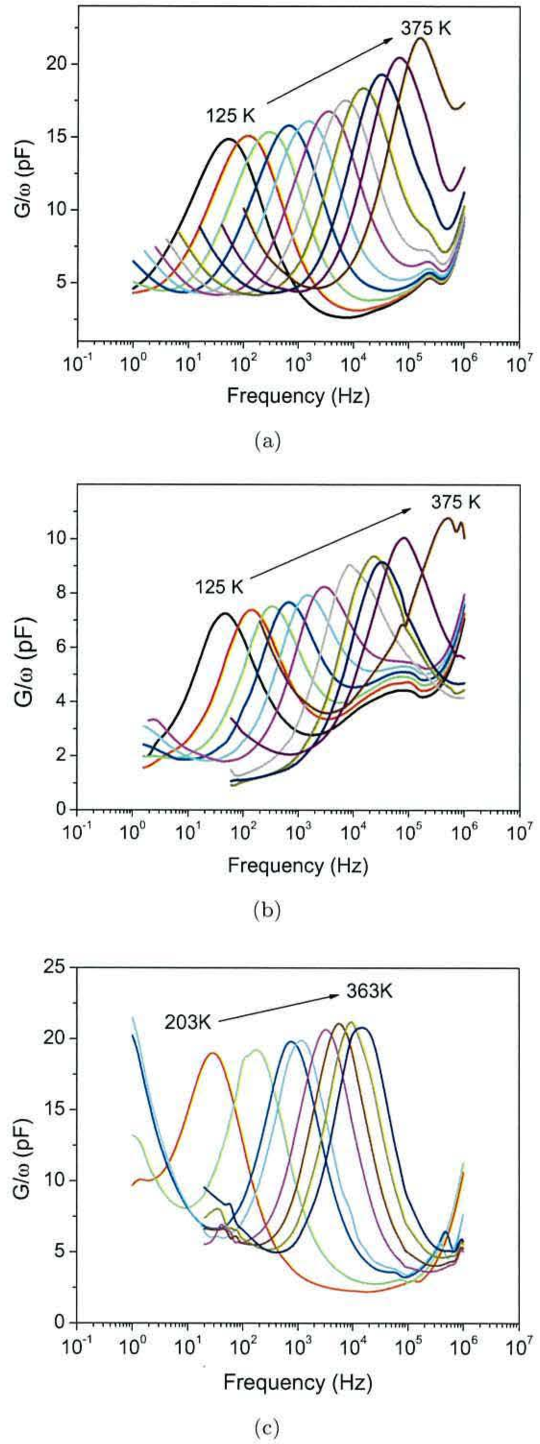
Arrhenius plots of f_R, R_B and σ_B, extracted from the experimental data for the PSQ, SU8-1 and SU8-2 based MIS capacitors, are provided in Figure 4.21. f_R was very similar for the PSQ and SU8-1 devices prepared in air, and were an order of magnitude greater than for the SU8-2 device with the P3HT deposited in an inert environment. Transitions in the Arrhenius plots of the PSQ and SU8-1 devices are evident, however the SU8-2 device exhibited a singly-activated Arrhenius dependence on temperature.

In the multiple trapping and release model (MTR) transport is characterised by recurrent trapping of charge carriers in shallow trap states, which are then released via a thermally activated process into de-localized bands [159]. The temperature dependence of the mobility follows an Arrhenius dependency of the form [159–161]

$$\mu = \mu_0 e^{-\Delta/k_B T} \tag{4.1}$$

where Δ is the activation energy, corresponding to the energy difference between the trap level and the de-localized band edge, k_B is Boltzmann's constant and T is the absolute temperature. As Δ increases with disorder, it can be used as an indicator of the degree of disorder.

Bulk mobilities of the three samples was calculated using N_A $\sim$4.6 $\times 10^{15}$ cm^{-3}, $\sim$2.9 $\times 10^{15}$ cm^{-3} and $\sim$3.5 $\times 10^{15}$ cm^{-3} for the PSQ, SU8-1 and SU8-2 devices respectively. Arrhenius plots of the bulk mobilities of the samples are shown in Figure 4.22. Quite clearly μ_B in device SU8-2 has a singly-activated Arrhenius dependence on temperature, with an activation energy of 0.25 eV and μ_0 $\sim$0.1 cm^2/Vs. Craciun *et al.* reported Δ $\sim$0.3 eV with μ_0 much higher at $\sim$30 cm^2/Vs for P3HT diodes [162]. A distinct transition is present in the Arrhenius plots of the PSQ and SU8-1 devices, occurring at 200–225 K. Transitions of this type have been noted in disordered semiconductors, reflecting transitions between different transport mechanisms [163], for example between dispersive and non-dispersive transport [164]. Lada suggested transitions of this nature observed at room temperature are caused by phase transitions in the P3HT [81]. Gomes *et al.*



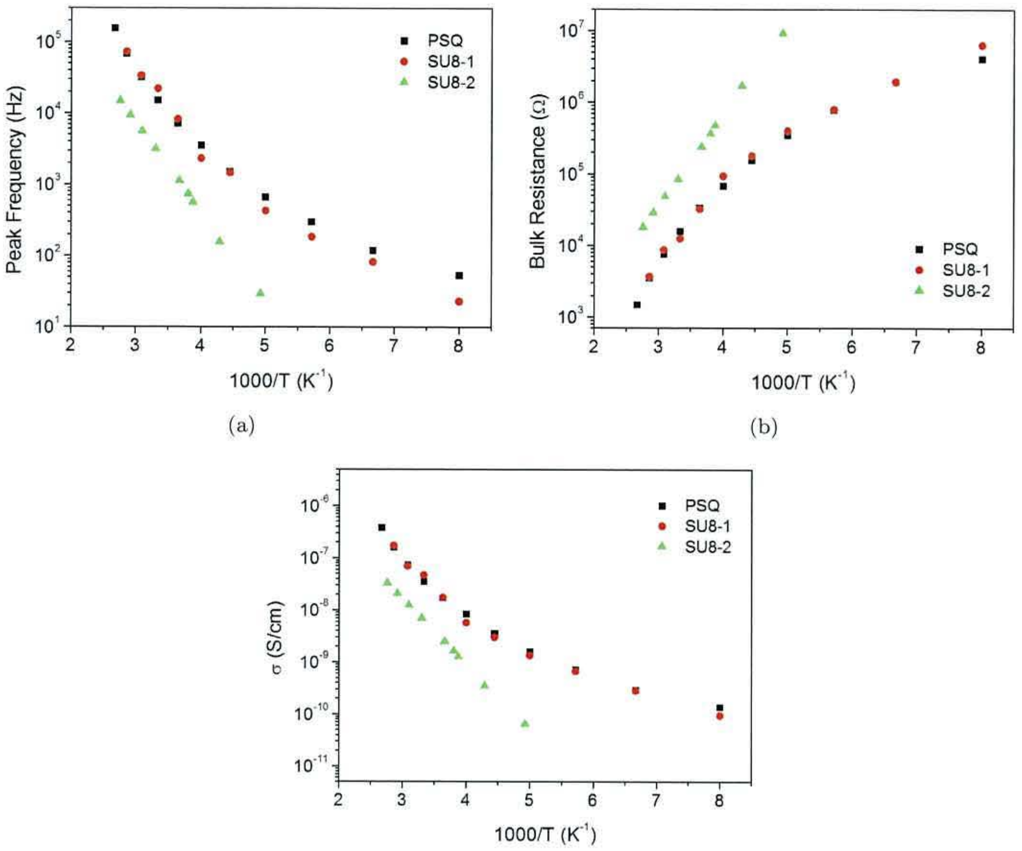
(a)

(b)

(c)

FIGURE 4.20: Frequency dependence of loss for (a) PSQ/P3HT, (b) SU8-1/P3HT MIS capacitors for temperatures ranging from 125 K to 375 K and (c) SU8-2/P3HT MIS devices for temperatures from 203 K to 363 K. Measurements were obtained with all devices biased at V_{FB}.

showed that, at temperatures between 200 K and 300 K, water related traps are responsible for changes in device behaviour [82]. Activation energies were determined to be in the range ~0.2 eV to 0.22 eV for temperatures $>$ 200 K and



(a)

(b)

(c)

FIGURE 4.21: Arrhenius plots of (a) the relaxation frequencies extracted, (b) bulk resistance and (c) bulk conductivity for PSQ (black), SU8-1 (red) and SU8-2 (green) based MIS capacitors derived from the G/ω-f plots in Figure 4.20.

between 0.094 eV and 0.082 eV in the low temperature regime for both the PSQ and SU8-1 devices.

Bässler *et al.* modelled the density of states (DOS) distribution of localized states with a Gaussian distribution. Energetic disorder in the semiconductor determines the width of the DOS. For a Gaussian DOS mobility can be described by the expression [67]

$$\mu = \mu_0 e^{-(T_0/T)^2} \tag{4.2}$$

where T_0 is a parameter which describes the energetic disorder, and is related to the width, σ, of the Gaussian DOS by $T_0 = 2\sigma/3k$. Mobility of the PSQ, SU8-1 and SU8-2 devices are plotted versus $1/T^2$ in Figure 4.23. These plots show the experimental data deviates from the straight line behaviour of Equation 4.2 (dashed lines in Figure 4.23) below ∼200 K for all devices. Fitting values for the dashed lines in Figure 4.23 are provided in Table 4.1.

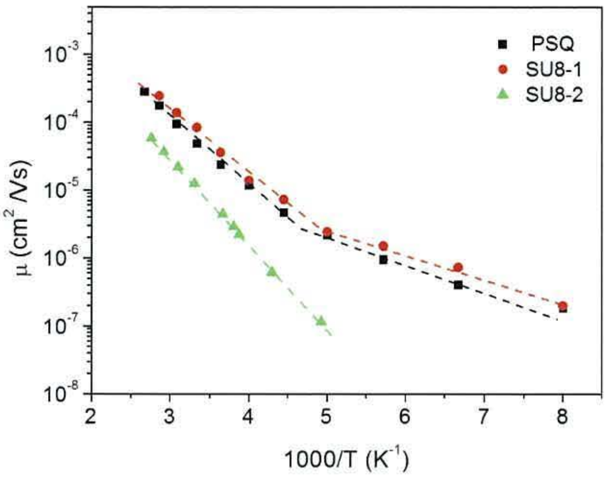


FIGURE 4.22: Arrhenius plot of the bulk mobility of the P3HT layer in the PSQ, SU8-1 and SU8-2 MIS devices (symbols). Dotted lines correspond to the best fits to the Arrhenius equation.

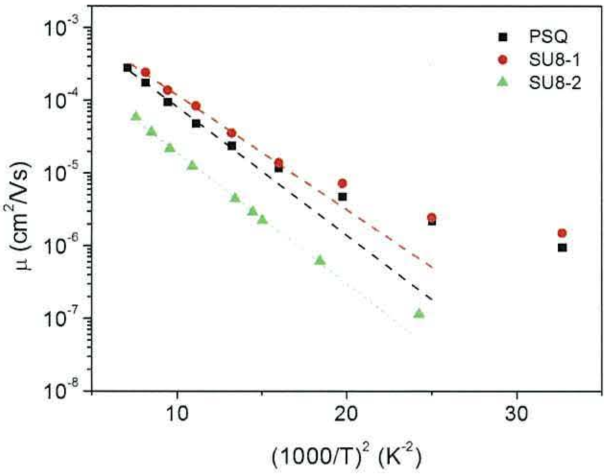


FIGURE 4.23: Semi-log plot of the temperature dependence of the bulk mobility plotted against $1/T^2$ of the PSQ, SU8-1 and SU8-2 MIS devices (symbols). Dotted lines correspond to the best fits to Equation 4.2.

Device	T_0 K	μ_0 $\mathrm{cm}^2/\mathrm{Vs}$)	σ meV
PSQ	638	4.8×10^{-3}	82
SU8-1	603	4.5×10^{-3}	78
SU8-2	648	7.24×10^{-4}	84

TABLE 4.1: Fitting parameters for Equation 4.2.

Both the Arrhenius and Gaussian expressions provide reasonable fits to the data. The higher activation energy, determined from the Arrhenius plot, and slightly higher value of σ imply there was slightly more disorder in the P3HT layer of the SU8-2 device. However the instabilities reported in the C-V measurements at higher temperatures for the devices prepared in air could indicate that adventitious dopants, such as atmospheric oxygen and water, were still present after several annealing cycles, increasing the bulk conductivity of the P3HT film.

4.6 Summary

MIS capacitors with PSQ and SU8 dielectrics and P3HT as the active layer have been characterized by measuring their admittance in the dark. Two types of SU8 were used, thinned SU8 2002 (50:50 in SU8 solvent, cyclopentanone) and SU8 2000.5.

Initial measurements on MIM structures revealed PSQ as the best insulator with high DC resistivity $\sim 10^{13}\,\Omega$, compared to $\sim 10^{12}\,\Omega$ for the SU8 layers. The SU8 material also exhibited a stronger dependence of its dielectric constant on frequency.

The C-V plots obtained with the P3HT semiconductor revealed classical p-type behaviour on all dielectrics, with a transition from accumulation to depletion at positive bias voltages. All devices also exhibited classical Maxwell-Wagner (M-W) dispersions in the C-f and G/ω-f plots.

All the PSQ devices exhibited V_{FB} $\sim$0 V with negligible hysteresis in the C-V plots, indicating minimal injection of electrons into the insulator at high positive voltages. The frequency dependence of the capacitance and loss revealed a fairly constant relaxation frequency for accumulation voltages. Driving the device into depletion caused f_R to move to higher frequencies. The low frequency capacitance decreased with increasing depletion voltages, which, together with the decreasing magnitude of the loss peak indicated the formation of a space-charge layer in the P3HT film.

MIS capacitors with the thinned SU8 dielectric (SU8-1) initially revealed a high flatband voltage $\sim$20 V. Increasing the UV exposure dose during the photo-polymerization step reduced V_{FB} down to $\sim$11.5 V. Further UV exposure resulted in a flatband voltage near 0 V. A possible reason for the decrease in V_{FB} is the reduction of un-reacted photo-initiator remaining in the SU8 after UV exposure. Devices with an SU8 2000.5 dielectric (SU8-2) had V_{FB} of $\sim$3 V, after correct UV dosage. The M-W dispersions in devices with high V_{FB} were very broad, and moved to lower frequencies as the depletion region increased. A distribution of time constants, due to the dispersive nature of charge transport, is responsible for the broad M-W dispersions.

Acceptor doping density also varied with UV exposure for the SU8 devices. Devices with a low exposure revealed N_A ~2×10^{16} cm^{-3}, whereas those with the correct exposure resulted in lower N_A, ~3.5×10^{15} cm^{-3}. Dopants originating from the insulator may be a cause of the increased doping density in the under-exposed devices. N_A in the PSQ devices was determined to be ~4.5-9 $\times 10^{15}$ cm^{-3}, similar to the correctly exposed SU8 devices.

A comparison of the properties of MIS capacitors with different insulators are summarised in Table 4.2.

Property	PSQ	SU8-1A	SU8-1B	SU8-1C	SU8-2
d_I (nm)	470	560	520	970	570
d_s (nm)	170	-	170	187	195
D_{IT} (cm^{-2} eV^{-1})	1.2×10^{10}	-	1.3×10^{11}	2.4×10^{10}	1.3×10^{11}
N_A (cm^{-3})	9×10^{15}	5×10^{16}	2.6×10^{16}	3.5×10^{15}	3.8×10^{15}
V_{FB} (V)	+0.2	+20	+11.5	0	+3
f_R (kHz)	40	-	20	33	3.5
μ_B (cm^2 /Vs)	6.2×10^{-5}	-	1.1×10^{-5}	1.1×10^{-4}	1.2×10^{-5}

TABLE 4.2: Summary of properties of MIS capacitors with various insulators.

C-f plots revealed the extent of lateral conduction and resistive losses through the insulator at low frequencies. The probe frequencies for the *C-V* measurements were chosen from the G/ω-f plots to be at least an order of magnitude below the M-W peak, but higher than those frequencies where lateral conduction was evident.

A further dispersion was evident in the *C-f* and G/ω-f plots at frequencies higher than 1 MHz caused by the series resistance of the contacts.

Both PSQ and SU8 based devices were found to be stable at temperatures up to 325 K, with N_A, D_{IT} and V_{FB} remaining approximately constant. Above 325 K, shifts in V_{FB} and increased hysteresis were seen in both the PSQ and SU8-1 devices, together with stretch-out of the depletion slopes, where capture and emission of holes by interface states was affecting the measurements. V_{FB} hardly altered in the SU8-2 device, with slightly increased hysteresis the only observable change. As the P3HT layer in the SU8-2 device was deposited under an inert environment, the decreased stability in the PSQ and SU8-1 devices at elevated temperatures could be due to the presence of atmospheric dopants, despite undergoing several annealing cycles.

Bulk conductivity and mobility were extracted from the M-W relaxation frequency. Both the PSQ and SU8-1 devices revealed similar values of σ_B and μ_B for the P3HT film over the temperature range 125 K to 375 K. These parameters were an order of magnitude lower in the SU8-2 device. Temperature dependence of μ_B could be described by either a $ln(\mu_B) \propto 1/T$ or $ln(\mu_B) \propto 1/T^2$, although the Arrhenius fit was marginally better at higher temperatures. The activation energy, Δ, for the SU8-2 device, 0.25 eV, indicated a slightly higher degree of disorder than in the PSQ and SU8-1 devices (Δ ~0.2 eV).

Chapter 5

Photo-Excitation of MIS Capacitors

5.1 Introduction

The effect on the *C*-*V* characteristics during monochromatic illumination of MOS devices has been studied, for example, by Pierret and Sah [115], and Poon and Card, who developed a technique for extracting interface state density from photo-admittance measurements [110]. Photo-admittance studies have also been performed on organic devices [62, 114, 165].

In this chapter both *C*-*V* and constant capacitance measurements were used to analyse the responses of organic MIS capacitors to monochromatic light. Also included are the responses of MIS capacitor arrays and charge-injection devices (CIDs). All device measurements were made at 303K using the setup described in Section 3.5.1.

5.2 P3HT Absorption spectrum

The absorption spectrum of P3HT, measured with a Cecil Instruments CE 9500 spectrophotometer, is shown in Figure 5.1. As reported in the literature, P3HT absorbs light of wavelengths between ~400 and 650 nm, the onset of strong absorption at ~650 nm revealing a bandgap of ~1.9 eV. Thus P3HT has a useful photo-response throughout the visible spectrum.

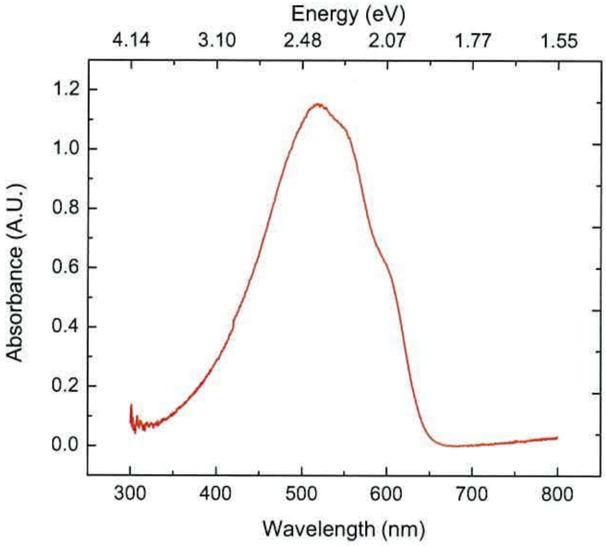


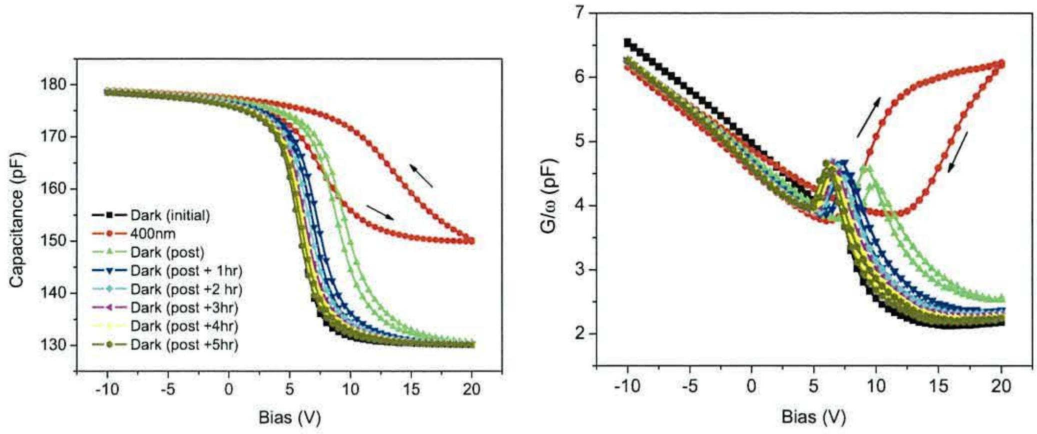
FIGURE 5.1: Absorption spectrum of P3HT.

5.3 Organic MIS Capacitors under Illumination

To determine the optical response of organic MIS capacitors both C-V and G/ω-V measurements in the dark and under illumination at various wavelengths were recorded.

5.3.1 Polysilsesquioxane-based MIS Capacitors

The initial 'dark' C-V and accompanying G/ω-V curves of a PSQ/P3HT capacitor are shown in Figure 5.2. Assuming the accumulation capacitance in Figure 5.2(a), ~178 pF, is C_I and that the minimum capacitance, ~130 pF, is the series sum of C_I and C_D, C_D is estimated to be ~482 pF and the P3HT layer thickness to be ~173 nm. Acceptor doping density, N_A, was estimated to be $\sim 6\times10^{15}$ cm^{-3} from the linear part of the C^{-2} *vs* V plot as detailed in Chapter 2. The red curve in Figure 5.2(a) shows the typical response of the PSQ/P3HT device during illumination at a wavelength of 400 nm. During illumination the minimum capacitance increased from 130 pF to 150 pF, corresponding to a decrease in the depletion width from ~173 nm to ~87 nm. Also noticeable was the positive shift in V_{FB}, ~7 V on the reverse sweep, corresponding to $\sim 2.5\times10^{11}$ cm^{-2} electrons trapped either at the P3HT/PSQ interface or in the insulating layer, increased hysteresis and stretch-out of the depletion slope. Similar behaviour was observed during photo-capacitance measurements on MIS capacitors by Fernandez *et al.* [61, 114]. The figure also shows C-V plots obtained in the dark at various times after illumination.



(a)

(b)

FIGURE 5.2: (a) C-V and (b) G/ω-V plots for PSQ/P3HT capacitors taken at 1 kHz initially in the dark, under illumination at 400 nm and at various times thereafter.

Stretch-out of the depletion slope observed in the photo-C-V plot coincided with an increase in the loss, as seen in the corresponding G/ω-V plot (Figure 5.2(b)). However the loss did not exhibit a sharp peak (as in the dark plots) but increased rapidly, initially to ~6 pF after which it continued to increase slowly. This latter phase coincided with the bias range (12.5–20 V) coincident with the increased minimum capacitance. Upon commencement of the reverse sweep, the loss dropped to a minimum of ~3.8 pF coincident with the increasing depletion slope of the measured capacitance. This implies that the loss curve had shifted to more positive bias voltages in unison with the shift in V_{FB}. Normally the loss peak is due to majority holes interacting with interface traps. Under optical excitation photo-generated electrons becoming trapped at the interface could create more states for holes to interact with, leading to an increased loss peak in depletion. Alternatively, photo-generated electrons within a diffusion length of the semiconductor surface, able to respond to an ac signal, could interact with electron traps producing the loss peak [110]. Taking the peak value at +20 V, the density of interface states was estimated to be $\sim 5.5 \times 10^9$ cm^{-2} eV^{-1} using the Hill-Coleman approximation. This is approximately 5 × the estimated dark value ($\sim 1 \times 10^9$cm^{-2} eV^{-1}).

Immediately after illumination the minimum capacitance recovered to its initial (dark) value, and V_{FB} decreased to ~6.8 V; a change in flatband voltage, ΔV_{FB}, of ~1.9 V, corresponding to ~6.6×10^{10} cm^{-2} electrons remaining trapped at the interface. The loss peak in the corresponding G/ω-V plot also recovered to approximately its initial dark plot value. Thus the density of interface states also recovered to its original quantity. Following this initial relaxation, the series of plots post illumination indicate a slower de-trapping process as V_{FB} shifted back to its initial (dark) value.

No significant differences were observed in the dark and illuminated (λ=400 nm) current-voltage plots (Figure 5.3) discounting any notable photo-conduction in the insulator layer. When biased in accumulation the applied voltage appears across the insulator where most leakage current occurred. In depletion the applied voltage appears across both the insulator and depletion region, reducing the field across the insulator and the resultant leakage current.

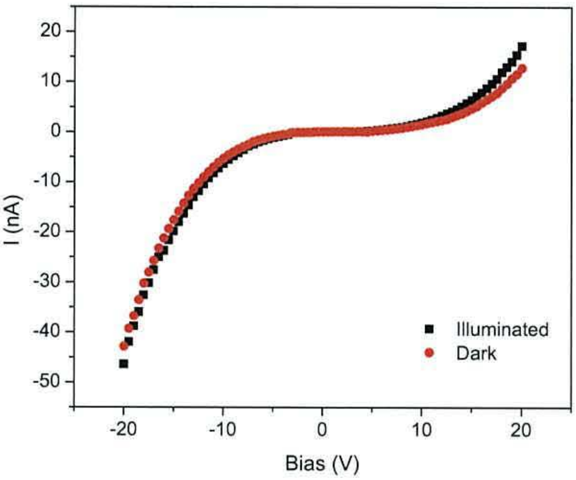


FIGURE 5.3: I-V characteristic of PSQ/P3HT MIS capacitor in the dark and under illumination of light. λ=400 nm, T = 303K.

5.3.2 SU8 based MIS capacitors

The C-V and G/ω-V plots for SU8-based MIS capacitors in Figures 5.4 reveal a similar response to that obtained with the PSQ/P3HT capacitors. As noted in Chapter 4, the dark C-V plots for devices with thinned SU8 2002 as the dielectric layer exhibited high flatband voltages; ~13.5 V for this device. When fully depleted the minimum measured capacitance fell to ~133 pF. Thus the depletion capacitance, C_D, was found to be ~480 pF from which the width of the P3HT layer was estimated to be ~174 nm. From the linear part of the slope of the $1/C^2$ vs. V plot the doping density was calculated to be 1.9 x 10^{16} cm^{-3}.

The response to 400 nm light resulted in a positive shift in V_{FB} beyond the range of the LCR bridge (+40 V). The forward sweep, in the depletion regime, did not reach a minimum, but fell gradually to ~165 pF over the available voltage range. However the initial stage of the reverse sweep shows that the depletion slope is similar to the *dark* plots. No loss peak in the accompanying G/ω-V plot was seen due to the limited voltage range of the LCR bridge (Figure 5.4(b)).

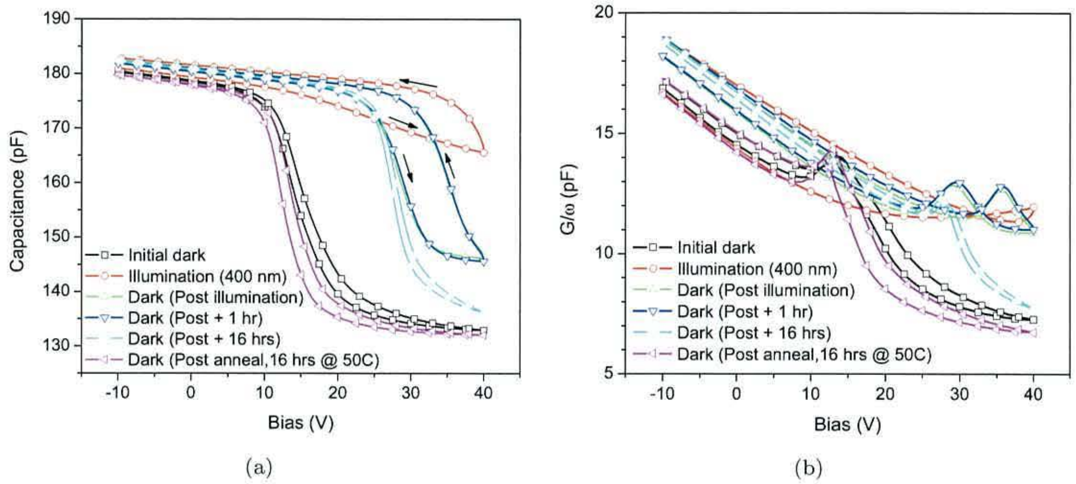


FIGURE 5.4: (a) C-V and (b) corresponding G/ω-V plots for SU8/P3HT capacitors taken at 1 kHz initially in the dark, under illumination at 400 nm and at various times thereafter. The final plots were taken after heating the device at 50°C for 16 hours to restore it to its initial dark condition. Hysteresis is anti-clockwise in all cases.

In the subsequent measurement in the dark, V_{FB} relaxed back to ~29 V indicating $\sim 5.3 \times 10^{11}$ cm^{-2} electrons were trapped either in the insulator or at the P3HT/SU8 interface. Interestingly, this plot shows that, unlike the PSQ-based device, the capacitance had not returned back to the minimum measured prior to illumination. This must therefore be related to the insulator or some other artefacts in it which act as electron traps. In Chapter 4 it was found that the high flatband voltages in SU8 devices was related to the UV exposure dose of the SU8 layer, possibly caused by remnant photo-initiator or other chemical by-products of the photo-polymerization process. It is possible, then, that electrons had become trapped in states within the insulator which have long relaxation times. Also noticeable is the large anti-clockwise hysteresis. After an hour the C-V (and G/ω-V) plots were almost identical to the previous measurement, with just a slight reduction in the minimum capacitance.

After a further 16 hours in the dark, V_{FB} was still ~29 V, although the minimum capacitance had fallen nearer to its original (dark) value. There is also a reduction in the hysteresis. At this point the MIS capacitor was heated overnight at 50°C, with a C-V characteristic taken the following day. V_{FB} had decreased to a value lower than the initial dark measurement, with the capacitance again falling to approximately the same minimum value. A similar process is seen for the series of G/ω-V plots where the loss peak slowly shifted back to its original value.

Due to the long relaxation of trapped charges a further experiment involved exposing a device to 400 nm light during a C-V which produced a response (not shown) similar to that recorded previously (*cf* Figure 5.4). After this measurement, the dynamics of the de-trapping process was characterised by tracking the dc bias required to maintain the device at a constant capacitance in the dark, using the PID feedback system described in Section 3.5.3. A suitable value of capacitance was chosen from the devices' dark C-V measurement, such that it was initially biased into depletion. Upon illumination the capacitance increases due to photo-generated charge, the PID controller then adjusts the bias voltage to keep the device at the required capacitance. Thus this process effectively tracks the shift in flatband voltage seen in the photo C-V response.

From the initial (dark) measurement the gate bias required to maintain the MIS capacitor at 170 pF was determined to be ~11.5 V (biasing further into depletion resulted in PID instability). Figure 5.5 reveals that, at the start of the tracking experiment, the necessary bias had increased to ~31.5V (note that the tracking program didn't start immediately upon turning off the light, consequently the initial decay was not recorded), which 50,000 seconds later had relaxed to approximately 27.5 V. The inset of Figure 5.5) shows that the tracked bias remained fairly constant for ~1000 seconds before relaxing due to de-trapping of electrons. Even after 5 hours more than 93% of the charges were still trapped. Retention times of this length are comparable to other MIS based organic floating gate memory devices [7].

The experimental data in Figure 5.5 was fiited to a stretched exponential decay or Kohlrausch's law (green symbols), which is defined as

$$V(t) = V_0 e^{-(t/\tau)^{\beta}} + V_{\infty} \tag{5.1}$$

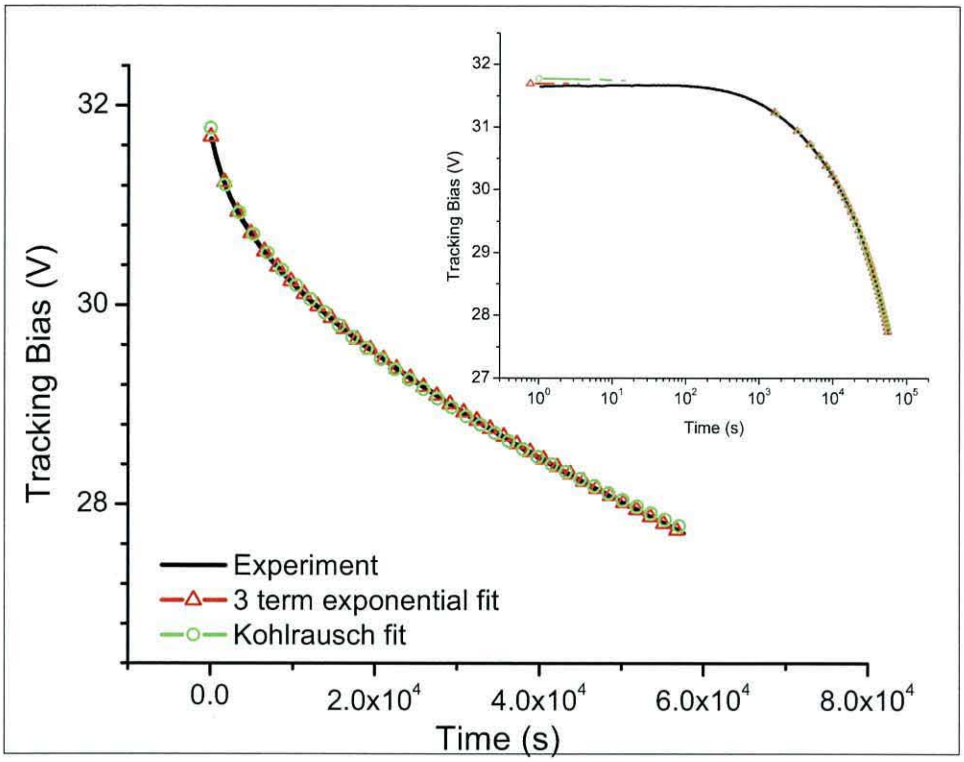


FIGURE 5.5: Relaxation of bias for a SU8/P3HT device capacitance of 170 pF at 303K, after illumination with 400 nm light. Also shown is the fitted data using a three-term exponential decay function (red symbols) and Kohlrausch's law (green symbols). Inset shows a lin-log plot for the same data.

where τ is the relaxation lifetime and β is a parameter indicating the degree of disorder and distribution of activation energies. The same data could also be fitted to a three term exponential decay (red symbols) of the form

$$V = V_\infty + V_1 e^{-t/\tau_1} + V_2 e^{-t/\tau_2} + V_3 e^{-t/\tau_3} \tag{5.2}$$

where τ_1, τ_2 and τ_3 are characteristic time constants for three exponential decay curves.

For the Kohlrausch fit in Figure 5.5 $\tau = 7.5 \times 10^7$ s and $\beta = 0.58$. The value of β is similar to that (0.47) determined for poly(phenylenevinylene) (PPV) [166].

The use of multiple term exponential functions generally indicates the presence of a continuum of trap states. In the case that the three-term exponential is real, then the trap depths, E_T, may be estimated from the equation

$$\tau = \tau_0 e^{E_T/kT} \tag{5.3}$$

where k is Boltzmann's constant, T the temperature and τ_0 is the time between attempts to escape, and if related to the phonon frequency is ~10^{-12}–10^{-13} s [61]. The fitting parameters and trap depths calculated from Equations 5.2 and 5.3 are provided in Table 5.1. The resultant values for E_T place the traps approximately in the middle of the bandgap of P3HT (E_G ~1.9 eV).

Exponential term	V_x	τ s	$E_T\,(\tau_0 = 10^{-12}s)$ eV	$E_T\,(\tau_0 = 10^{-13}s)$ eV
V_1	18.77	389996	1.06	1.12
V_2	0.95	12421	0.97	1.03
V_3	0.47	2017	0.92	0.98

TABLE 5.1: Characteristic time constants and fitting parameters obtained from Equation 5.2 together with trap depths calculated with Equation 5.3.

An estimate of the time required for the bias to relax back to 11.5 V was found to be ~400 hours using Equation 5.2. Linear extrapolation of the relaxation results in a decay time of ~125 hours. Confirmation of relaxation over these time scales was found in a further experiment where, after a C-V plot in the dark, an MIS device was biased into depletion (V_G = +20 V) and exposed to 400 nm light for ten minutes. A second C-V measurement was obtained immediately after illumination, after which the device was left in the dark, under vacuum, for 8 days (192 hours). A further C-V plot revealed the device had not fully recovered, with V_{FB} still ~2 V higher than the initial measurement (Figure 5.6).

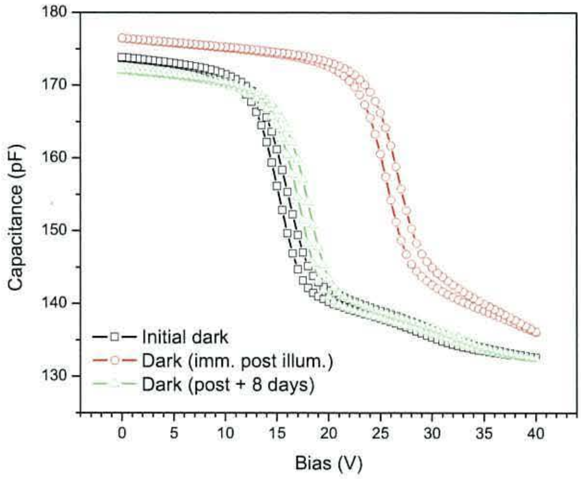


FIGURE 5.6: C-V plots of SU8/P3HT MIS capacitor obtained in the dark both prior to, immediately, and 8 days after illumination of monochromic light (λ=400 nm) demonstrating slow relaxation of V_{FB}.

As was found for the PSQ-based device, comparative I–V plots of the SU8/P3HT capacitor both in the dark and under illumination with 400 nm light indicated there was no significant photo-conduction in the insulator (Figure 5.7)

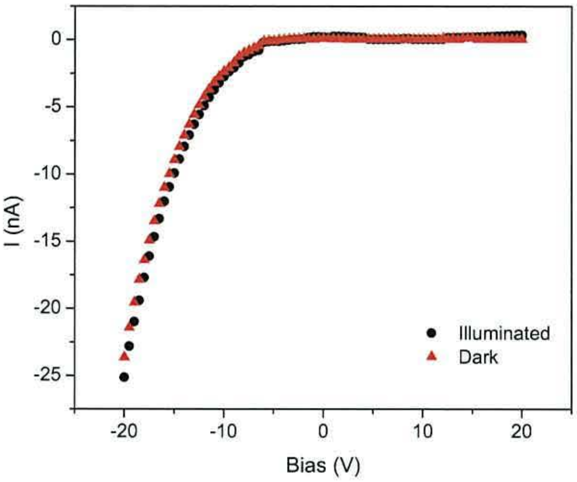


FIGURE 5.7: I–V characteristic of SU8/P3HT MIS capacitor in the dark and under illumination of light (λ=400 nm) taken at 303K.

5.3.3 Discussion

Both the PSQ and SU8 based MIS devices produced similar results during photo-excitation, although the effect was much more pronounced in devices with the SU8 dielectric. An increase in minimum capacitance has also been observed in similar P3HT based MIS capacitors where such behaviour was seen as possible evidence of a photo-induced inversion layer [62, 114]. It is interesting to note that high frequency C-V plots of wide band gap inorganic MIS capacitors exhibit a similar response to illumination [112, 113, 167]. As the time constant for thermal generation of minority carriers in wide band gap semiconductors far exceeds the dc bias sweep rate used for C-V measurements, the MIS devices are driven into deep depletion. Upon illumination, photo-generated minority carriers can respond to the ac probe voltage, and the resultant C-V plot reveals increased minimum capacitance, typical of a normal high frequency (inversion) response [113]. In the case of an inversion layer, the population of electrons at the interface is balanced by a reduction in space charge in the depletion region, correlating with a decreased depletion width and increased minimum capacitance [62, 115], thus the number of *free* electrons can be calculated using Equation 2.38 defined in Section 2.4.

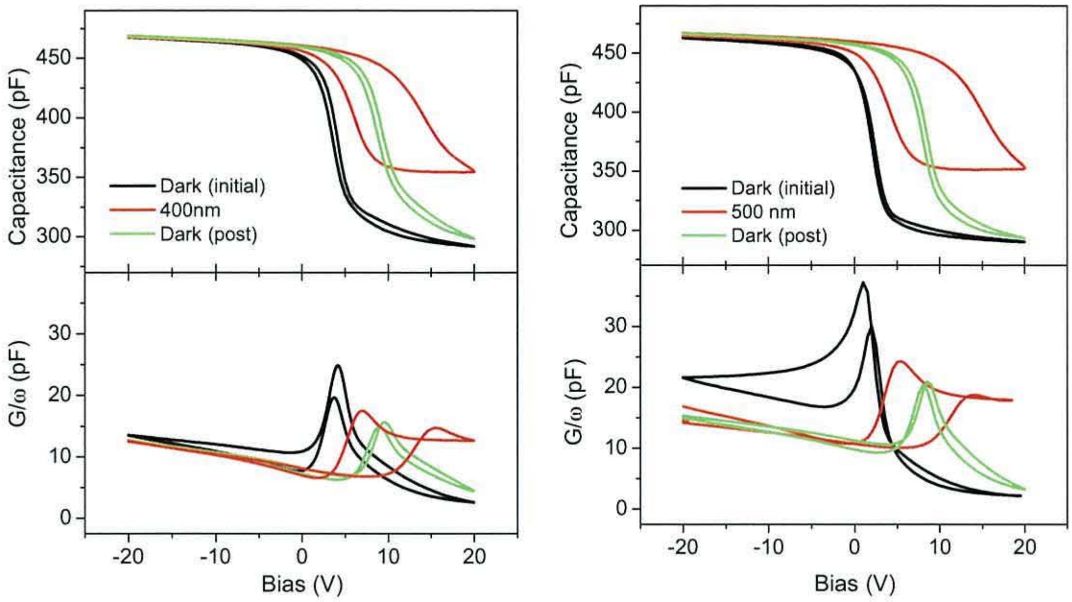
If the increase in minimum capacitance of the PSQ device was due to formation of an inversion layer then an estimated $\sim 5.1 \times 10^{10}$ cm^{-2} *free* electrons were present at the P3HT/PSQ interface. Due to the measured capacitance of the SU8 devices not reaching a constant minimum value, only a maximum value of $\sim 2.3 \times 10^{11}$ cm^{-2} *free* electrons can be determined from the *C*-*V* plot.

However the admittance results for both types of MIS device indicate that the increase in minimum capacitance during illumination could also be due to a shift of the flatband voltage to more positive values at a rate equal to the voltage scan rate, as shown in Section 5.4. Photo-generated electrons becoming trapped at the interface (or in the insulator) under constant illumination would cause a positive shift in V_{FB} at a rate dependent on the photon flux and bias scan rate. The trapped electrons effectively shield the semiconductor from the increasing bias, reducing its effect until the band-bending required to maintain charge neutrality becomes pinned, resulting in a constant measured capacitance. The corresponding 'plateau' in the loss peaks can also be seen as evidence of this due to the ac signal probing the same energy level in the band gap.

5.4 Effect of measurement parameters on *C*-*V* photo-response

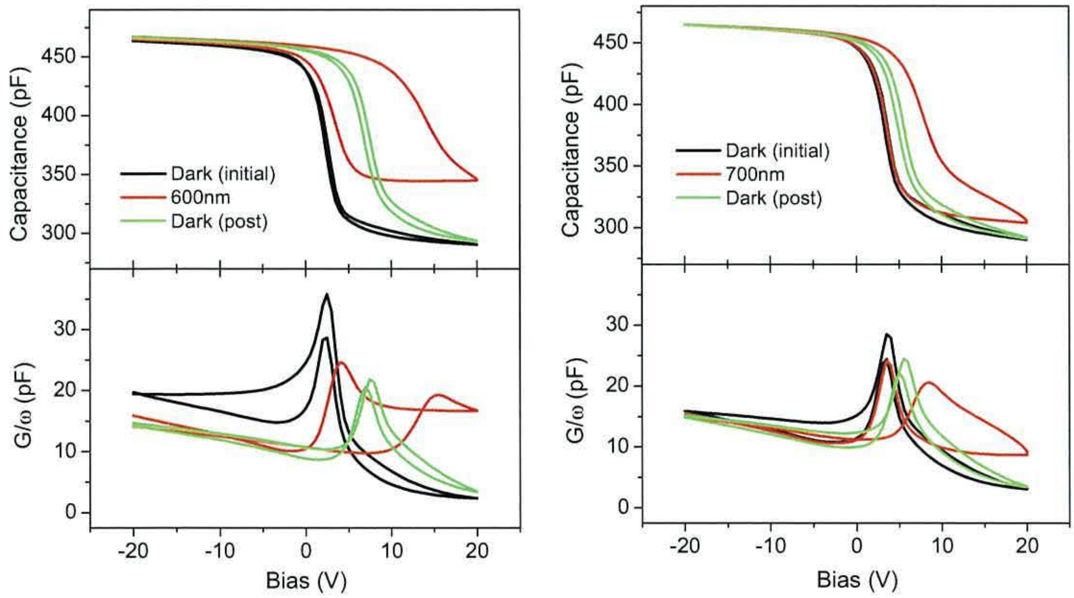
In the previous sections the response of both PSQ/P3HT and SU8/P3HT capacitors have been examined using the same experimental parameters. In this section the responses of SU8/P3HT MIS devices are analysed under varying experimental conditions. The parameters were wavelength, incident power and bias scan rate (i.e. the rate at which the *C*-*V* response is measured). The devices used in these measurements were fabricated with SU8 2000.5 to provide a ~194 nm thick dielectric layer. P3HT was spun on at 3000 r.p.m. resulting in a layer ~106 nm thick. Doping density, determined from the (dark) Mott-Schottky plot, was found to be 3×10^{16} cm^{-3} after annealing under vacuum at 100°C for 10 hours. Each measurement cycle consisted of a measurement in the dark, under illumination and then immediately after excitation in the dark. Devices were then annealed after each measurement cycle for 10 hours to return them to their initial states.

5.4.1 Wavelength



(a) C-V response at $\lambda = 400$ nm

(b) C-V response at $\lambda = 500$ nm



(c) C-V response at $\lambda = 600$ nm

(d) C-V response at $\lambda = 700$ nm

FIGURE 5.8: C-V and associated G/ω-V characteristics of an SU8/P3HT MIS capacitor in the dark both before (initial), during and immediately after (post) photo-excitation with light of wavelength (a) 400 nm, (b) 500 nm, (c) 600 nm & (d) 700 nm. (Measurement frequency 1 kHz, scan rate 0.2 V/s, T=303K).

The responses of the MIS capacitor to photo-excitation at wavelengths between 400 and 700 nm are illustrated Figure 5.8. Qualitatively the device responds strongly to wavelengths where the photon energy ($E_{ph} = hc/\lambda$) is greater than the optical bandgap. Common to all the results is the increase in C_{min} seen in the C-V plots and corresponding plateaus in the the G/ω-V curves. However, this effect is not as strong when illuminated with $\lambda = 700$ nm light, where only a small increase in C_{min} is observed (Figure 5.8(d)). Indeed as the gate bias was swept to more positive voltages, the 700 nm curve followed the dark curve beyond the depletion slope, before C_{min} increased. The reverse sweep shows some hysteresis, indicating a positive shift in V_{FB}. This is confirmed by the G/ω-V plots where, in the forward sweep, the loss peak under illumination lies exactly on top of the initial dark peak, however during the reverse sweep, the peak broadened and shifted to a more positive bias in unison with V_{FB}. At $\lambda = 600$ nm (Figure 5.8(c)) the increase in C_{min} is much larger, as is the shift in V_{FB}. It is also interesting to note that V_{FB} appears to have shifted to a slightly more positive value (from the initial dark value) during the forward sweep of the C-V measurement, indicating electron trapping may have occurred whilst the device was biased in the accumulation regime. A congruent shift in the corresponding loss peak can also be seen in the G/ω-V plots. Similar results were obtained at 400 and 500 nm (Figures 5.8(a), 5.8(b)). The increase in C_{min} was almost the same in both experiments, although the observed hysteresis was greater with 500 nm light, as was the increase in V_{FB} during the C-V forward sweep.

A widely used figure of merit for photodiodes and photo-transistors is their *Responsivity* (R) defined as the photo-current generated per unit light power (A/W) [122]. For the purposes of this work it is useful to similarly define the *Responsivity* (R) of the MIS capacitors as $\Delta C_{min}/P_0$, where P_0 is the incident power of light at the device surface and ΔC_{min} is the increase in C_{min}. The *Responsivity* together with ΔC_{min} and the corresponding change in depletion width, Δd, obtained at each wavelength are provided in Table 5.2.

These results indicate *Responsivity* effectively follows the absorption spectrum of P3HT (as shown in Figure 5.1), except at 400 nm: both ΔC_{min}, and hence Δd, obtained at 400 nm were similar to the values obtained at 500 nm.

A further comparison of the response at each wavelength can be made by relating the increase in V_{FB} to the number of photons incident on the device. As noted in Section 2.6, for monochromatic light of wavelength λ and incident irradiance,

λ nm	P_0 μW	ΔC_{min} pF	Δd nm	R pF/μW
400	6.03	63	50.7	10.45
500	5.84	62	50.7	10.62
600	5.81	54	45.9	9.47
700	3.24	14	13.2	4.32

TABLE 5.2: Responsivity of SU8/P3HT MIS capacitor under illumination at different wavelengths.

I_{opt}, the photon flux Φ_λ arriving at the MIS capacitor is

$$\Phi_\lambda = \frac{I_{opt}\lambda}{hc}. \tag{5.4}$$

An estimate of the total number of photons incident on the device may be obtained by integrating Φ_λ over the duration of the *C*-*V* measurement. Neglecting the fraction of excitons decaying radiatively and assuming the increase in V_{FB} is due to photo-generated electrons becoming trapped, the 'trapping efficiency' can be defined as

$$\eta_{tr} = \frac{N_T}{\int \Phi_\lambda \, dt} \tag{5.5}$$

where $N_T = \Delta V_{FB} C_I / qA$ is the density of trapped charges.

λ nm	I_{opt} μWcm^{-2}	ΔV_{FB} V	N_T cm^{-2}	η_{tr} $\times 10^{-6}$
400	192	7.9	7.33×10^{11}	4.79
500	186	10.1	9.31×10^{11}	5.03
600	185	9.7	8.92×10^{11}	4.04
700	103	3.4	3.13×10^{11}	2.18

TABLE 5.3: Trapping efficiency of SU8/P3HT MIS capacitors under illumination at T = 303K.

The results in Table 5.3 reveal fairly constant trapping efficiency of ~4–5×10^{-6} for $E_{ph} > E_g$. This result represents the effective external quantum yield of trapped charge carriers. These values are relatively low. However no account has been taken of the fraction of light absorbed within the thin (~100 nm) semiconductor layer. To determine the internal trapping efficiency the absorption of light within the active layer should be considered. It was shown in Section 2.6 that the fraction of incident photons absorbed in the semiconductor per unit area per second is

$$N_\lambda = (1-r)\Phi_\lambda(1-e^{-\alpha d}), \tag{5.6}$$

where r and α are the reflection and absorption coefficients respectively. Thus the internal trapping efficiency may be defined as

$$\eta_{int} = \frac{N_T}{N_{ph(abs)}}, \tag{5.7}$$

where $N_{ph(abs)} = \int N_\lambda dt$ is the total number of photons per unit area absorbed in the semiconductor layer.

Using Equation 5.6 to calculate the absorbed photon density yields very low efficiencies for the quantum yield of charge carriers (see Table 5.4), with η_{int} some three orders of magnitude lower than the intrinsic quantum yield of charge carriers (~0.017) for E_{ph} in the range 1.9–3.0 eV obtained by Dicker *et al.* [168].

The *C*-*V* plots for this device, presented in Figure 5.8, indicate that when biased into accumulation, there is either little or no effect from the incident irradiation. This may be due to efficient recombination of photo-generated charges in the semiconductor as, in accumulation, excess holes would rapidly combine with negative charges. Thus it is not until the device is driven into depletion that efficient trapping of electrons occurs. Interestingly, the efficiencies at 700 and 400 nm are more than double those obtained at 500 and 600 nm. This is similar to the behaviour of pentacene phototransistors where their response to 365 nm light was much greater than at 650 nm, despite the absorbance at 650 nm being 3× greater [169].

λ nm	α cm^{-1}	N_T cm^{-2}	$N_{ph(abs)}$ cm^{-2}	η_{int} $\times10^{-6}$
400	2.3×10^4	7.33×10^{11}	3.2×10^{16}	22.9
500	7.7×10^4	9.31×10^{11}	9.58×10^{16}	9.72
600	7.2×10^4	8.92×10^{11}	1.00×10^{17}	8.89
700	8.2×10^3	3.13×10^{11}	1.02×10^{16}	30.8

TABLE 5.4: Internal trapping efficiency of SU8/P3HT MIS capacitors under illumination at T = 303K. Values for α calculated from P3HT n-k data kindly provided by Dr. T. Jenkins, Aberystwyth University.

Analysis of the density of interface states, D_{IT}, (see Table 5.5) estimated from the loss peaks (using the Hill and Coleman approximation [106]) of the G/ω-V

plots in Figure 5.8, indicate a reduction in D_{IT} during illumination with light (where $E_{ph} > Eg$). This contrasts with the results noted in Section 5.3 where an increase was found. D_{IT} estimated from the subsequent dark G/ω-V plots (labelled 'post') show further reductions. Conversely there was no change in D_{IT} when the device was subjected to 700 nm light, however D_{IT} increased slightly during the post-illumination G/ω-V measurement.

	D_{IT} (cm^{-2} eV^{-1})		
λ (nm)	Dark (initial)	Illuminated	Dark (post)
400	1.63×10^{11}	1.41×10^{11}	1.02×10^{11}
500	1.98×10^{11}	1.59×10^{11}	1.39×10^{11}
600	2.0×10^{11}	1.81×10^{11}	1.48×10^{11}
700	1.4×10^{11}	1.4×10^{11}	1.54×10^{11}

TABLE 5.5: Density of interface states determined from G/ω-V curves in the dark and under illumination.

For each measurement cycle the post-illumination C-V plots show C_{min} recovering to its pre-illumination level, except for the 400 nm experiment (Figure 5.8(a)) where C_{min} was still ~6 pF higher at a gate voltage of +20 V. The depletion slopes in each case had shifted to higher positive biases, indicative of negative charges still trapped at the P3HT/SU8 interface resulting in large positive shifts in V_{FB}.

5.4.2 Incident power

Increasing the incident power results in an increase in the number of photons interacting with the semiconductor. Thus an increase in the population of photo-generated charges in the P3HT layer leads to an increase in the minimum capacitance, and V_{FB}. Figure 5.9 shows the response of a MIS device to different intensities of light of the same wavelength (500 nm). At low intensities (Figure 5.9(a)) the forward sweep of the C-V plot follows the (initial) dark plot, before peeling off at a new C_{min} (309 pF). The reverse scan reveals some hysteresis with V_{FB} increasing by + 4.70 V. Similarly the loss plot under illumination follows the initial dark plot - the loss peaks coinciding. Immediately after the peak the (illuminated) loss plateaus over the same bias range as the increased C_{min}. During the reverse sweep the loss peak broadened, coinciding with the stretched depletion curve observed in the C-V plot. When the irradiance was increased to 108 μW cm^{-2} (Figure 5.9(b)), the forward sweep diverged from the initial dark plot as the bias approached V_{FB} , and C_{min} increased by ~40 pF. The increase in intensity also produced larger hysteresis in the device. A similar response was seen at the highest intensity (186 μW cm^{-2}, Figure 5.9(c)), except that an increase in V_{FB} is now evident in the forward sweep. Larger increases in C_{min} (to 352 pF) and hysteresis were also seen. The loss plots in Figures 5.9(b) and 5.9(c) both show the loss peaks moving to higher gate voltages corresponding to the shifts in V_{FB} in the *C-V* plots. Also noticeable is the broadening of loss peaks and increases in loss plateaus in depletion (to the right of the loss peaks) whose values increased with intensity.

In each experiment the post illumination dark plots show C_{min} returning back to the initial dark value. V_{FB}, though, remained more positive, the extent of the shift in V_{FB} being dependent upon the intensity of the light during the photo–*C-V* measurement.

Responsivity of the MIS capacitor at each intensity is summarized in Table 5.6, and reveals that, at $\lambda = 500$ nm, low intensities resulted in a greater response. At 108 and 186 μW cm^{-2} the R values are both similar and much lower than that obtained at 1.1 μW cm^{-2}, indicating that as the incident irradiation increases, the response appears to saturate. Similar responses were found by Lancaster [170] with ITO/ATO[1]/P3HT based MIS capacitors. Saturation effects in the photo-response of poly(3, 3"'-didodecylquarter-thiophene) (PQT-12) transistors was also reported by by Wasapinyokul *et al.* [171].

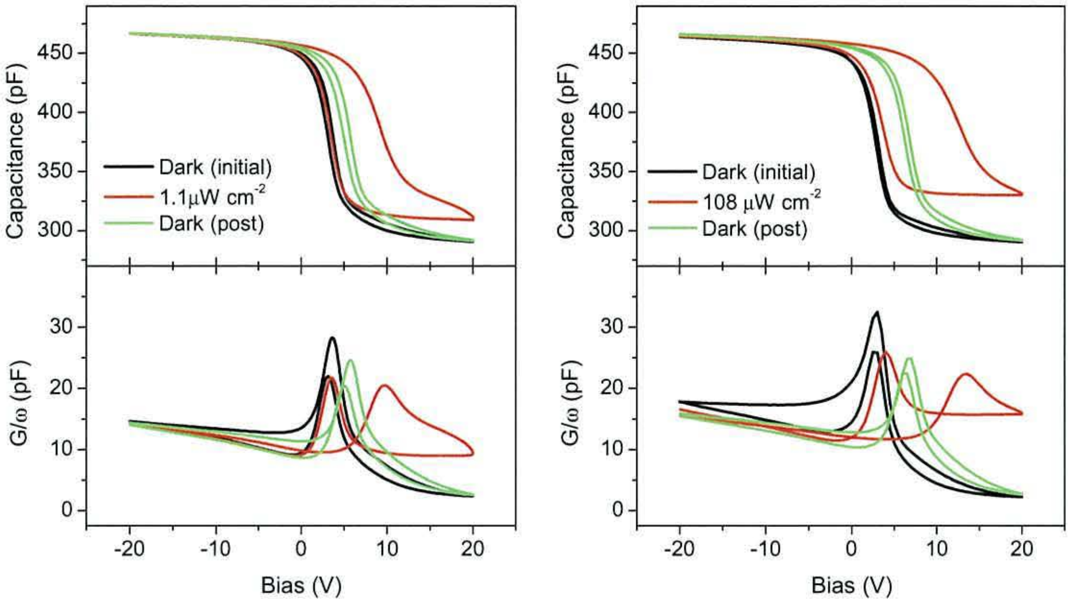
I_{opt} μW cm^{-2}	C_{min} pF cm^{-2}	R pF μW^{-1}	ΔV_{FB} V	N_T cm^{-2}	η_{int} $\times 10^{-6}$
1.1	604	549.8	4.7	4.35×10^{11}	768
108	1273	11.8	7.8	7.19×10^{11}	13.6
186	1973	10.6	10.1	9.27×10^{11}	9.68

TABLE 5.6: Responsivity and trapping efficiency of SU8/P3HT MIS capacitor to different intensities of light of the same wavelength (λ =500 nm).

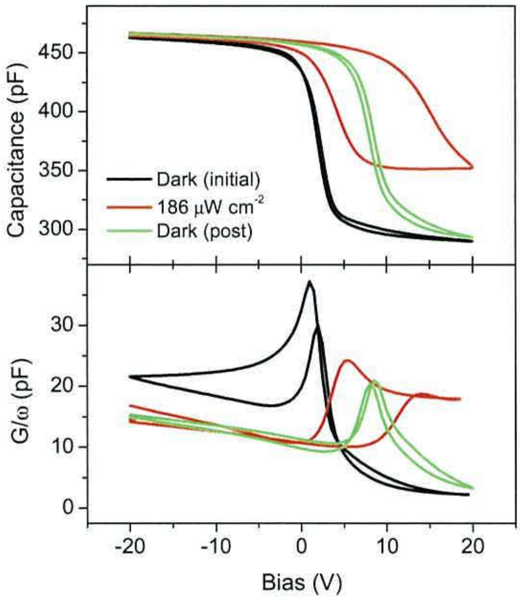
Analysis of the internal trapping efficiency η_{int} also reveals the same trend (Table 5.6), where trapping efficiency for electrons increases with decreasing light intensity. The density of interface states (Table 5.7) reveals a reduction in D_{IT} from the initial dark to the post illumination G/ω-V plots, the percentage change

---

[1] Atomic layer deposited aluminium titanium oxide.



(a) C-V response at $I_0 = 1.1\,\mu$W cm^{-2} (b) C-V response at $I_0 = 108\,\mu$W cm^{-2}



(c) C-V response at $I_0 = 186\,\mu$W cm^{-2}

FIGURE 5.9: C-V and associated G/ω-V characteristics of a SU8/P3HT MIS capacitor in the dark both before (initial) during and after (post) photo-excitation of light of wavelength $\lambda = 500$nm, at intensities of (a) $1.1\,\mu$W cm^{-2}, (b) $108\,\mu$W cm^{-2} and (c) $186\,\mu$W cm^{-2}. (Measured at 1 kHz at a scan rate of 0.2 V/s; T = 303 K).

in D_{IT} ranging from ~12% at the lowest intensity to ~30% at the highest. However, given that the values of D_{IT} presented in Table 5.7 were calculated using the approximation introduced by Hill and Coleman, the differences in D_{IT}

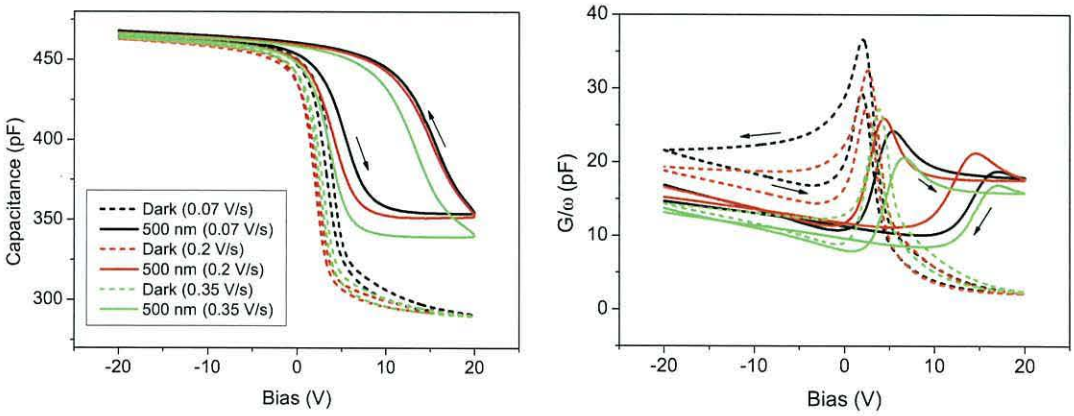
	D_{IT} (cm^{-2} eV^{-1})		
I_{opt} (μW cm^{-2})	Dark (initial)	Illuminated	Dark (post)
1.1	1.55×10^{11}	1.52×10^{11}	1.36×10^{11}
108	1.57×10^{11}	1.62×10^{11}	1.27×10^{11}
186	2.01×10^{11}	1.59×10^{11}	1.39×10^{11}

TABLE 5.7: Density of interface states determined from G/ω-V curves in the dark and under illumination at different intensities (λ= 500 nm, T=303K, frequency = 1 kHz).

between initial and post measurements may not be of significance.

5.4.3 Scan Rate

In this experiment the effect of the dc bias scan rate on the admittance was measured with the MIS capacitor in the dark and under illumination of light (λ=500 nm, I_{opt}=186 μW cm^{-2}). The results of varying the scan rate from 70 mV/s to 350 mV/s are shown in Figure 5.10. Both C_{min} and the positive shift in V_{FB} decreased with increasing scan rate, although there is only a small difference in the (overall) shift in V_{FB} and C_{min} at the two slowest rates (0.07 and 0.2 V/s). As the scan rate decreases the initial shift in V_{FB} moves to slightly more positive values. Thus the MIS device response at each scan rate reflects the reduction in time at each measurement point for the photo-generated charge to accrue.



(a) C-V plots at scan rates 0.07, 0.2, 0.35 V/s.

(b) Corresponding G/ω-V plots.

FIGURE 5.10: C-V response of SU8/P3HT MIS capacitor in the dark and under photo-excitation of light (λ=500 nm, I_{opt}=186 μW cm^{-2}) at different scan rates (measured at 1 kHz).

Table 5.8 shows that the responsivity, R, of the device decreases with increasing scan rate. Conversely the trapping efficiency increases with scan rate. This is equivalent to the results obtained by changing light intensity; increasing the number of photons the device is exposed to results in a reduction in the efficiency of the device.

Scan Rate V/s	C_{min} pF cm	R pF μW^{-1}	ΔV_{FB} V	N_T cm^{-2}	η_{int} $\times 10^{-6}$
0.07	64	10.95	9.9	9.12×10^{11}	3.59
0.2	62	10.61	9.5	8.94×10^{11}	9.07
0.35	49	8.38	8.7	8.02×10^{11}	14.35

TABLE 5.8: Responsivity and trapping efficiency of SU8/P3HT MIS capacitor to 500 nm light at an intensity of 186 μW cm^{-2} for different bias scan rates.

5.4.4 Model for the *C-V* response under illumination

The results of the previous sections show the measured *C-V* response of the MIS capacitor is dependent upon wavelength, intensity and scan rate. In this section a simple model considering these parameters is presented.

From Equation 5.6 the number of photons absorbed in a semiconductor layer of thickness d per unit area per second is N_λ. If we now consider only those photons absorbed within the depletion layer, width d_p, then the total number of photons, n_p, absorbed per unit area per second will be

$$n_p = (1 - r)\Phi_\lambda(1 - e^{-\alpha d_p}). \tag{5.8}$$

These photons generate excitons in the depletion layer which are subject to an electric field, and electrons will be generated at a rate given by

$$\frac{dn(t)}{dt} = \beta n_p \frac{dV}{dx}\bigg|_{x=d_p}, \tag{5.9}$$

where dV/dx is the field at the edge of the depletion region determined by the surface voltage V_s, $x = d_p$ is the depletion width and β is a parameter that determines the field dependence of exciton dissociation.

The electric field at the depletion region edge was defined in Section 2.2.1.3 by Equation 2.5 and so the electron generation rate is now

$$\frac{dn(t)}{dt} = \beta n_p \frac{qN_A d_p(t)}{\varepsilon_s}. \tag{5.10}$$

Assuming all these electrons become trapped so that

$$\frac{dn_t(t)}{dt} = \frac{dn(t)}{dt} \tag{5.11}$$

where n_t is the concentration of trapped electrons per unit area. It was shown in Chapter 2 that $V_{FB} = \phi_{MS} - Q_i/C_i$ where Q_i are the charges trapped in the insulator. For dynamic trapping of electrons and assuming $\phi_{MS} = 0$, V_{FB} can be rewritten as

$$V_{FB}(t) = \frac{q}{C_i} n_t(t) \tag{5.12}$$

Recalling that the measured MIS capacitance is given as the series sum of the insulator and semiconductor capacitances:

$$\frac{1}{C(t)} = \frac{1}{C_i} + \frac{d_p(t)}{\varepsilon_s} \tag{5.13}$$

where the depletion width at time t is given by

$$d_p(t) = -\frac{\varepsilon_s}{C_i} + \frac{\varepsilon_s}{C_i}\sqrt{1 + \frac{2C_i^2}{\varepsilon_s q N_A}(V_G(t) - V_{FB}(t))}. \tag{5.14}$$

Equation 5.12 shows that V_{FB} is dependent on $n_t(t)$ which can be determined by substituting for $d_p(t)$ into Equation 5.10:

$$\frac{dn_t(t)}{dt} = \frac{\beta q N_A}{C_i}\left(\sqrt{1 + \frac{2C_i^2}{\varepsilon_s q N_A}(V_G(t) - \frac{q n_t(t)}{C_i}} - 1\right). \tag{5.15}$$

Equation 5.15 is difficult to solve analytically, however it can be solved numerically to provide $n_t(t)$ from which $d_p(t)$ can be calculated and substituted into Equation 5.13 to determine $C(t)$ as a function of $V_G(t)$ where $V_G(t) = Kt$ and K is the gate voltage ramp rate.

5.4.4.1 Simulation Results

In all the following simulations, the insulator capacitance, C_i was set to 14.6 nF/cm^2 and N_A to 1×10^{16} cm^{-3}. Due to their low values, the reflection coefficients, r, were ignored. Absorption values, α, were taken from n-k data for P3HT (see Table 5.4).

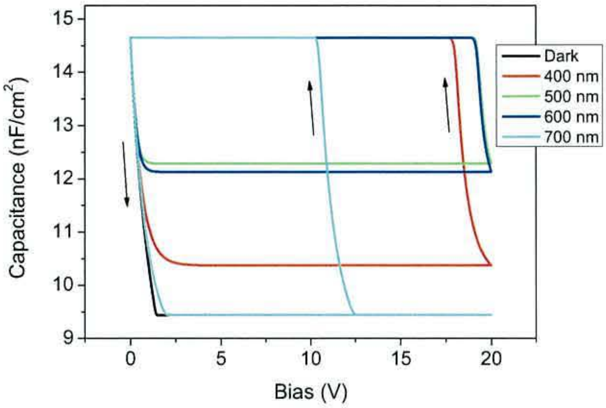


FIGURE 5.11: Simulated effect of wavelength on the C-V response of an MIS capacitor. Scan rate = 0.2 V/s, incident photon flux = 1×10^{14} photons/cm^2/s and $\beta = 1 \times 10^{-8}$ for all wavelengths.

In Figure 5.11 the effect of wavelength on the photo-C-V of the MIS capacitor can be seen to be dependent on the absorption coefficient of the semiconductor at the wavelength of the incident light. This contrasts with the experimental results where the response at 400 nm exhibited a higher trapping efficiency and was almost the same as that obtained for 500 nm light. This may be because a higher proportion of excitons generated with 400 nm light are located near the insulator / semiconductor interface than those generated with 500 nm light. Excitons located near the interface are subject to a stronger electric field and more likely to dissociate into separate charge carriers, whereas excitons located further away from the interface will experience a weaker electric field and be less likely to dissociate.

The simulated responses of the MIS capacitor irradiated with 500 nm light at incident intensities of 1–100 μW/cm^2 are shown in Figure 5.12. In these plots the values of β were increased from 5×10^{-8}, for an incident power of 100 μW/cm^2, to 5×10^{-7}, for 1 μW/cm^2, to account for the increased trapping efficiency at low intensities seen in the experimental data in Section 5.4.2.

Figure 5.13 presents the simulations for the C-V responses of an MIS capacitor irradiated with 500 nm light at bias scan rates from 0.1 V/s to 0.5 V/s. Values of

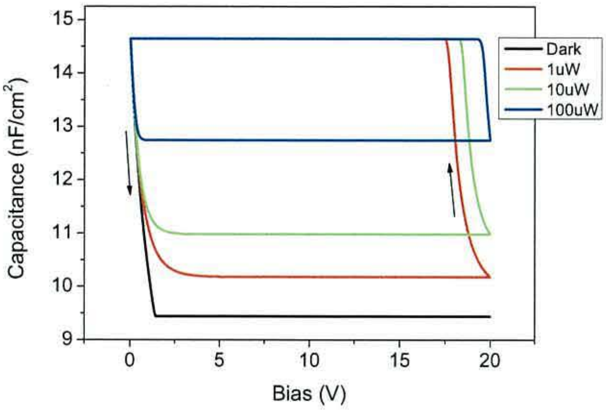


FIGURE 5.12: Simulation of the *C*-*V* response of an MIS capacitor to irradiation of 500 nm light at various intensities. Scan rate = 0.2 V/s.

β were varied between 3×10^{-9} at 0.1 V/s and 6×10^{-9} at 0.5 V/s to simulate the increased efficiency at higher scan rates seen in the experimental results (Section 5.4.3).

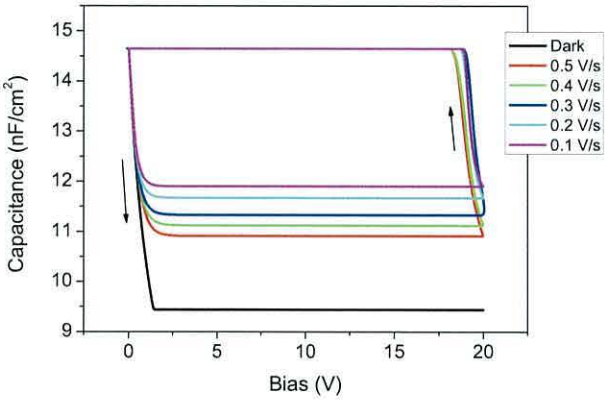


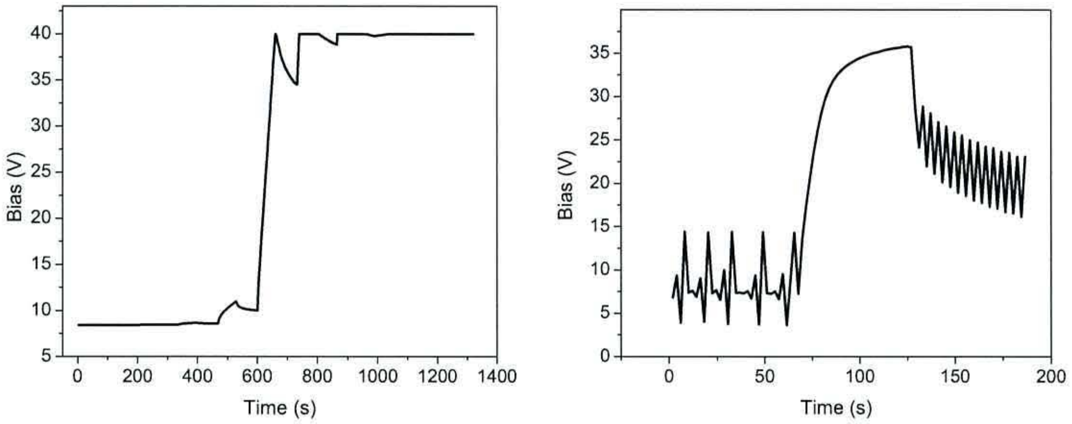
FIGURE 5.13: Simulation of the *C*-*V* response of an MIS capacitor to irradiation of 500 nm light at different bias scan rates. Incident power was set to 100 μW/cm^2.

The general pattern of behaviour in the simulations is very similar to the experimental results, suggesting that the basic model is correct. Increased minimum capacitance and anti-clockwise hysteresis is observed in all the simulations. However, before attempting any realistic curve fitting, improvements are required in the model to include effects arising from recombination, de-trapping of electrons and the presence of free electrons in the semiconductor. These are clearly topics for further study.

5.5 Temporal Response to Photo-excitation

The temporal response of organic MIS capacitors to photo-excitation at various wavelengths was recorded using a modified version of the PID control system described in Section 3.5.3. The program was changed here, though, to enable complete control of the sample exposure to light. In particular, a number of different wavelengths could be set, with the devices monitored alternately in the dark and under illumination. Prior to each measurement cycle, samples were kept in the dark and the dc bias adjusted until the chosen capacitance was obtained.

Capacitance values with the device either fully depleted or close to full depletion, were found to require changes in bias which were either beyond the range of the LCR bridge (Figure 5.14(a)) or caused the PID controller to become unstable (Figure 5.14(b)). Thus the following experiments were performed with devices biased to avoid such problems.



(a) Bias beyond control range.

(b) Unstable PID response.

FIGURE 5.14: PID system responses obtained when tracking capacitance chosen at (a) bottom of depletion slope, where bias voltages beyond the range of the LCR bridge are required to maintain the constant capacitance and (b) half way down depletion slope causing instabilities in the PID control.

5.5.1 PSQ/P3HT MIS Capacitors

The *C*-*V* response of the PSQ/P3HT MIS capacitor obtained in the dark and used in this experiment can be seen in Figure 5.15. Noting the constraints mentioned above a capacitance of 160 pF corresponding to an initial bias of ~2.7 V was chosen as the capacitance to be maintained constant.

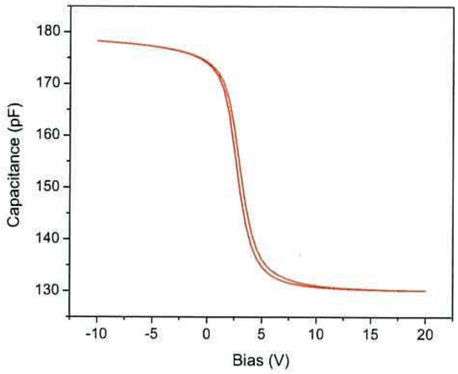


FIGURE 5.15: PSQ/P3HT MIS capacitor C-V response in the dark from which a capacitance of 160 pF was chosen for the tracking experiment.

This device was subjected to light with wavelengths ranging from 1000 nm to 400 nm, in steps of 50 nm, for 60 s each. After each photo-excitation the device was left in the dark for 60 s prior to illumination at the next wavelength. The results of this experiment are shown in Figure 5.16 (the inset shows the full experimental results obtained over 6000 s to monitor the device relaxation after the final illumination).

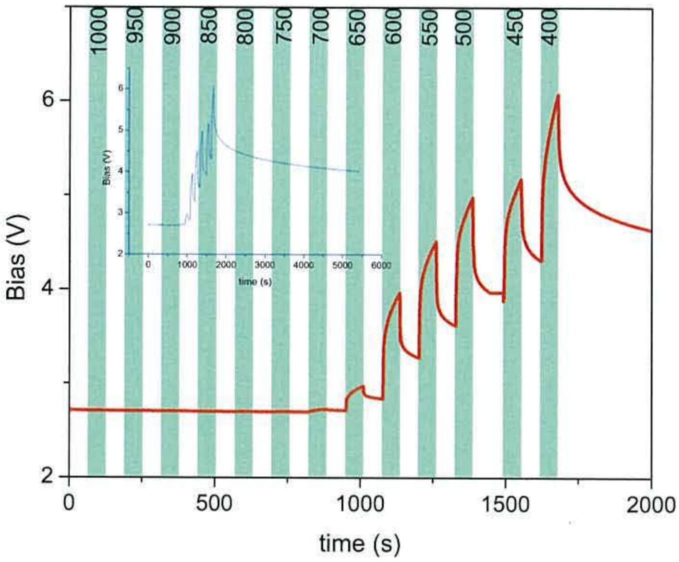


FIGURE 5.16: PSQ/P3HT tracking 160 pF under photo-excitation at wavelengths from 1000 nm down to 400 nm in steps of 50 nm (shaded stripes indicate light on). Inset shows device relaxation after illumination.

Very little effect of the illumination was found at wavelengths longer than the absorption edge of P3HT (650 nm), although a slight increase was observed at 700 nm. At shorter wavelengths the response was much greater; the bias required to maintain a capacitance of 160 pF increased in a similar manner at each excitation wavelength.

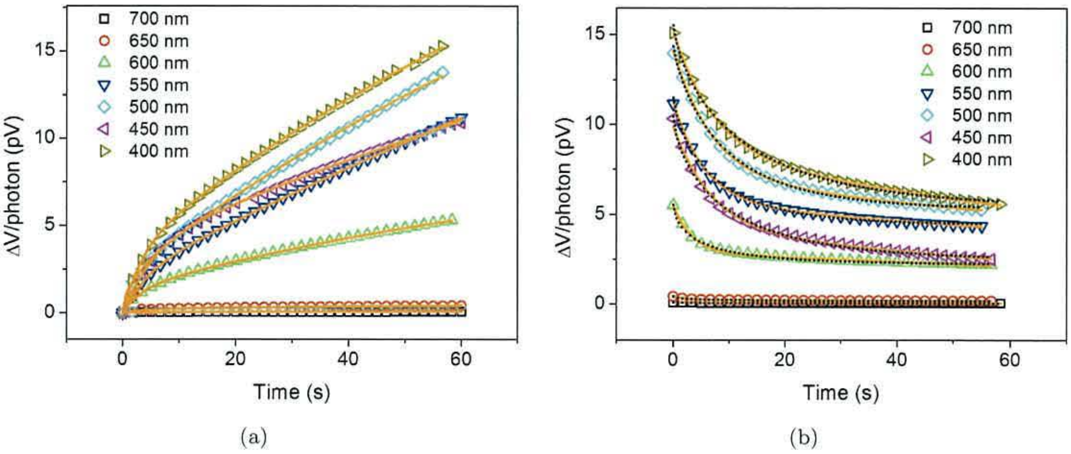


FIGURE 5.17: Normalised response of PSQ/P3HT MIS capacitor extracted from data in Figure 5.16. (a) Growth curves under illumination (symbols) were fitted to Equation 5.16 (solid orange lines). (b) Decay curves in the dark could be fitted to both a double exponential (Equation 5.17, orange lines) and Kohlrausch's law (Equation 5.1, black lines). Symbols are experimental data.

The growth and decay curves for photo-excitation at wavelengths 400–700 nm in Figure 5.16 are replotted in Figure 5.17 where the change in bias (ΔV) has been normalised with respect to the number of incident photons/s. These plots show the device responded more strongly with increasing photon energy. Interestingly, during illumination the increase in ΔV follows two phases; an immediate increase at the onset of illumination followed by a more gradual increase in ΔV. For two processes causing a shift in bias $\Delta V(t)$ then,

$$\begin{aligned} \Delta V(t) &= A_1(1 - e^{-t/\tau_1}) + A_2(1 - e^{-t/\tau_2}) \\ &= V_0 - A_1 e^{-t/\tau_1} - A_2 e^{-t/\tau_2}, \end{aligned} \tag{5.16}$$

where $V_0 = -(A_1 + A_2)$ and τ_1 and τ_2 are characteristic time constants. The bias transients during illumination have been fitted to Equation 5.16, as shown in Figure 5.17(a). Fitting parameters for the growth curves at each wavelength are provided in Table 5.9 which indicates one exponent has a fast time constant (order of a few seconds), and the other a longer time constant of the order of tens of seconds, which appears to be dependent upon the absorption properties of the semiconductor at the wavelength of the incident light.

Upon cessation of illumination, the bias required to keep the device at 160 pF initially falls quickly due to a rapid decrease in V_{FB} (Figure 5.17(b)); this could be due to fast de-trapping of electrons from shallow trap states. A much slower

λ	τ_1	τ_2	A_1	A_2	V_0
400	3.3	121	3.30×10^{-12}	3.18×10^{-11}	3.51×10^{-11}
450	5.2	218	3.71×10^{-12}	3.05×10^{-11}	3.42×10^{-11}
500	7.5	257	2.28×10^{-12}	5.63×10^{-11}	5.83×10^{-11}
550	4.3	367	2.06×10^{-12}	6.04×10^{-11}	6.25×10^{-11}
600	3.3	92	1.26×10^{-12}	8.54×10^{-11}	9.83×10^{-12}
650	3.1	57	2.14×10^{-13}	3.19×10^{-13}	5.31×10^{-13}
700	3.6	55	2.41×10^{-14}	9.13×10^{-14}	1.19×10^{-13}

TABLE 5.9: Parameters used to fit data in Figure 5.17(a) to Equation 5.16.

λ	τ_1	τ_2	B_1	B_2	$\Delta V(0)$
400	7.3	141	6.78×10^{-12}	8.36×10^{-12}	1.5×10^{-11}
450	6.7	109	5.62×10^{-12}	4.23×10^{-12}	9.85×10^{-12}
500	7.05	196	7.14×10^{-12}	6.93×10^{-12}	1.41×10^{-11}
550	5.6	203	5.58×10^{-12}	5.64×10^{-12}	1.12×10^{-11}
600	3.3	199	2.62×10^{-12}	2.86×10^{-12}	5.48×10^{-12}
650	2.6	189	1.8×10^{-13}	2.41×10^{-13}	4.2×10^{-13}
700	6.4	256	3.01×10^{-14}	5.99×10^{-13}	9.0×10^{-14}

TABLE 5.10: Parameters used to fit decay curves in Figure 5.17(b) to Equation 5.17.

relaxation of V_{FB} then followed.

The time dependence of decay curves was fitted to the stretched exponential (Equation 5.1), and are plotted in Figure 5.17(b) (black curves). The characteristic time constants obtained using Kohlrausch's relation were in the range ~5–12 s. Values for β ranged between ~0.5 and ~0.8, with the highest value occurring after illumination with 500 nm light.

The fit to the Kohlrausch relation, however, starts to diverge at ~50 s and a better fit to the decay curves was obtained using a double exponential of the form

$$\Delta V(t) = B_1 e^{-t/\tau_1} + B_2 e^{-t/\tau_2}, \tag{5.17}$$

where $B_1 + B_2 = \Delta V(0)$, and is also plotted in Figure 5.17(b) (orange line). Fit parameters for the decay process are provided in Table 5.10 from which it is seen that the time constants extracted for the initial decay, τ_1, are all very similar, ~3–7 s. Extracted values for τ_2 were also found to be approximately the same, ~200 s, except for the decay after illumination at 450 nm which is much lower, corresponding to the faster decay seen in Figure 5.17(b).

The long relaxation seen in Figure 5.16, after exposure to 400 nm light was fitted to both the stretched exponential decay law (Kohlrausch law, Equation 5.1) as well as a three term exponential decay (*cf* Equation 5.2), from which the time dependence of the de-trapping process was obtained. As can be seen in Figure 5.18 both provide an excellent fit to the measured data, indicating, perhaps, that Kohlrausch's law provides a better fit over much longer time scales. Fitting parameters for the Kohlrausch function are $\beta = 0.214, \tau = 3399, V_0 = 3.32$ and $V_\infty = 2.82$. β determined for the PSQ device is lower than that for the SU8 device in Section 5.3.2, indicating a higher degree of order in the PSQ device. The relaxation process is also much quicker in the PSQ device than for the SU8 device, as indicated by the much smaller value of τ. Trap depths were calculated from Equation 5.3, using the characteristic time constants derived from the three-term exponential fit. τ_0, the time between attempts to escape, was again taken to be in the range 10^{-12}–10^{-13} s. The calculated trap depths are provided in Table 5.11, and show the traps to be deeper than the range 0.45–0.57 eV determined by Fernandez *et al.* for PSQ [61]. The table also lists the fitting parameters used for Equation 5.2.

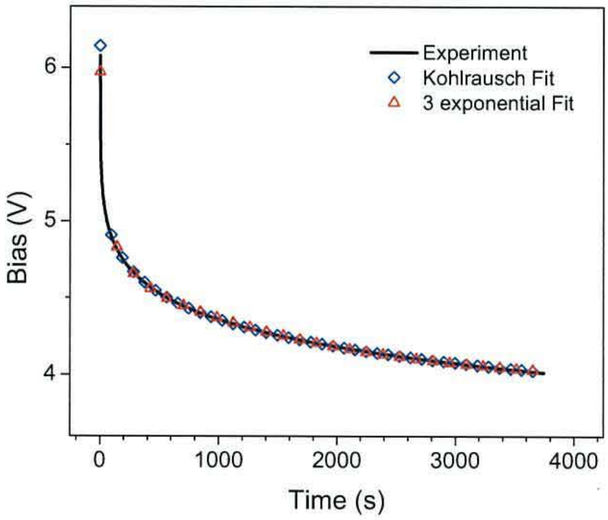


FIGURE 5.18: Shift in the bias of a PSQ/P3HT MIS capacitor whilst tracking a capacitance of 160 pF after illumination with 400 nm light. T=303K.

The time constants determined here are smaller than those obtained for the SU8 device in Section 5.3.2, as are the values of E_T, indicative of a faster decay mechanism for PSQ devices.

Exponential term	V_x	τ s	$E_T\,(\tau_0 = 10^{-12}s)$ eV	$E_T\,(\tau_0 = 10^{-13}s)$ eV
(V_1)	0.777	6.13	0.77	0.83
(V_2)	0.51	152	0.85	0.91
(V_3)	0.76	1843	0.92	0.98

TABLE 5.11: Fitting parameters from Equation 5.2 and trap depths in PSQ/P3HT MIS capacitors calculated using Equation 5.3.

5.5.2 SU8/P3HT MIS Capacitors

The *C-V* response, measured in the dark at 1 kHz, of the SU8/P3HT capacitor is shown in Figure 5.19 from which a tracking capacitance of 165 pF was chosen. The temporal response of this device to 60 s pulses of monochromatic light at wavelengths between 400 and 700 nm is shown in Figure 5.20. As expected the device responded most strongly to wavelengths ≤ 650 nm, with each successive illumination at wavelengths down to 450 nm causing an increase in V_{FB}, due to photo-generated electrons becoming trapped at the SU8/P3HT interface. Both the increase in bias (to maintain the device at 165 pF) during illumination, and the decay, with the light off, appeared to be very similar at wavelengths between 450 and 600 nm. Prior to illumination at 400 nm the bias to track 165 pF had increased to ~14.8 V, which for the first ~15 s during illumination at 400 nm increased further to 16.1 V. However, instead of increasing further, as observed at longer wavelengths, the bias plateaued and then fell slightly for the remaining 45 s. During the following dark period (60 s) the bias necessary to maintain constant capacitance decayed to ~14.3 V.

Normalizing these results by dividing ΔV with the incident photon flux provided the plots in Figure 5.21, from which it is apparent that, except during illumination at 400 nm, ΔV increased with decreasing wavelength - the maximal response was recorded at a wavelength of 450 nm.

As seen in the response of PSQ based devices, the growth in ΔV during photo-excitation comprises two exponents, which could be fitted using Equation 5.16 at all wavelengths except 400 nm (Figure 5.21(a)). At 400 nm the initial transient follows the same fast rise seen at other wavelengths for which a single exponential term provided the best fit, with a time constant ~5 s (similar to the fast time constants obtained at the other wavelengths). After the initial rise the response

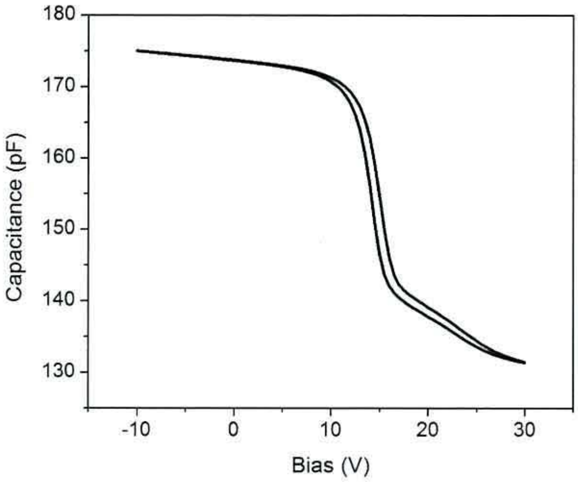


FIGURE 5.19: Dark C-V response for SU8/P3HT MIS device from which a capacitance of 165 pF was chosen for the tracking experiment.

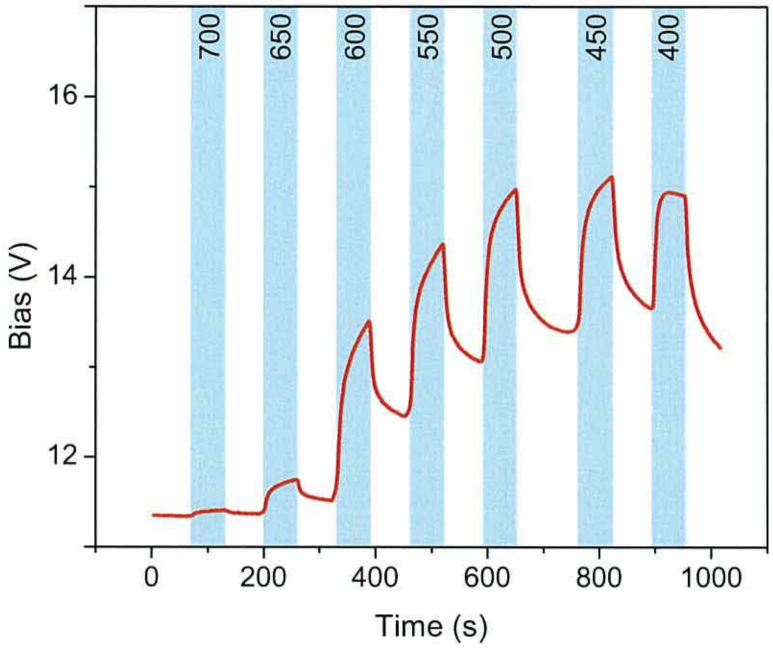


FIGURE 5.20: Change in bias to track a capacitance of 165 pF during photo-excitation at wavelengths from 700 nm down to 400 nm. Shaded areas indicate each 60 s illumination.

rapidly changes to a decay, where the photo-generated charges recombine (or are annihilated) at a faster rate than they become trapped.

For wavelengths 450–600 nm the normalized decay curves (Figure 5.21(b)) indicated ΔV recovers faster after irradiation with shorter wavelengths. At 400 nm the decay curve exhibits a much steeper slope with ΔV becoming negative, and the bias required to maintain the constant capacitance had decreased to a value lower than before illumination at 400 nm. This indicates the de-trapping

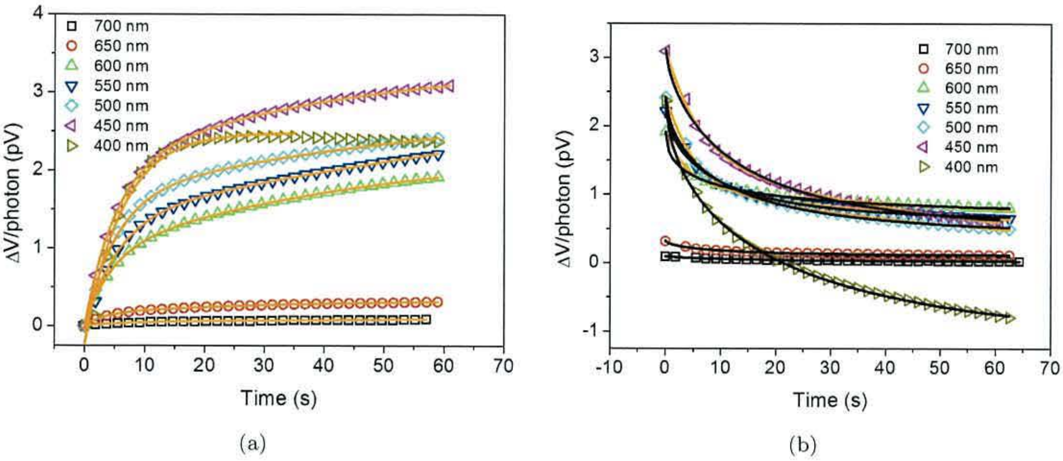


FIGURE 5.21: Normalized response of SU8/P3HT capacitor to light at wavelengths between 400 nm and 700 nm. (a) Experimental growth curves (symbols) were fitted using Equation 5.16 (orange lines), except at 400 nm (see text). (b) Experimental decay curves (symbols) were fitted to both the Kohlrausch (black line) and Equation 5.17, except at 400 nm.

λ	τ_1	τ_2	A_1	A_2	V_0
400	5.7	-	-2.4×10^{-12}	–	2.4×10^{-12}
450	5.1	41.0	2.0×10^{-12}	1.41×10^{-12}	3.4×10^{-12}
500	5.1	67.9	1.68×10^{-12}	1.31×10^{-12}	2.97×10^{-12}
550	5.5	179.7	1.43×10^{-12}	2.94×10^{-12}	4.33×10^{-12}
600	4.4	49.5	9.32×10^{-13}	1.4×10^{-12}	2.33×10^{-12}
650	3.0	30.5	1.51×10^{-13}	1.88×10^{-13}	3.39×10^{-13}
700	5.2	60.5	4.24×10^{-14}	7.44×10^{-14}	1.17×10^{-13}

TABLE 5.12: Parameters used to fit data in Figure 5.21(a) to Equation 5.16.

rate in the SU8 device is dependent on wavelength. The normalised data was also fitted to Kohlrausch's relation (5.1) and the two-term exponential of Equation 5.17. A good fit to Equation 5.17 for the decay seen after irradiation with 400 nm light was not possible due to ΔV becoming negative. Fits to the Kohlrausch equation resulted in values of the time constant, τ, in the range 9–20 s which increased with photon energy. The values of β, $\sim$0.5–0.9, are similar to those obtained for the PSQ device. As one might expect, the time constants determined from Equation 5.17 reveal shorter time constants for shorter wavelength light, reflecting the faster decay kinetics seen in Figure 5.21(b). The time constants and fitting parameters for Equation 5.17 are given in Table 5.13.

Following the response observed at 400 nm further tests revealed that the reduction in tracking bias was enhanced at shorter wavelengths. Together with the long retention times found in the SU8/P3HT capacitors, this effect led to

λ	τ_1	τ_2	B_1	B_2	ΔV_0
400	-	-	-	-	-
450	6.1	65	1.61×10^{-12}	1.49×10^{-12}	3.11×10^{-12}
500	5.2	76.9	1.33×10^{-12}	1.08×10^{-12}	2.41×10^{-12}
550	5.4	127	1.18×10^{-12}	1.04×10^{-12}	2.24×10^{-12}
600	4	187	8.1×10^{-13}	1.08×10^{-12}	1.91×10^{-12}
650	4.7	142.8	1.69×10^{-13}	1.45×10^{-13}	3.14×10^{-13}
700	8.9	109	4.9×10^{-14}	4.57×10^{-14}	9.11×10^{-14}

TABLE 5.13: Fitting parameters obtained from Equation 5.17 for the decay curves.

the idea of a memory device in which data could be written with 500 nm light, and then erased with 300 nm light. In a further experiment, an MIS device was illuminated for 120 s with 500 nm light, kept in the dark for 120 s, illuminated with 300 nm light and finally left in the dark for >10 mins. As expected the bias necessary to maintain 165 pF increased due to the photo-generated trapped electrons (Figure 5.22). When the light was extinguished an initial rapid decay was followed by a much slower de-trapping process, similar to that recorded in Section 5.3.2. Irradiation with 300 nm light produced an almost linear reduction in the bias to keep the capacitance at 165 pF - indicating a reduction in the overall charge within the MIS device.

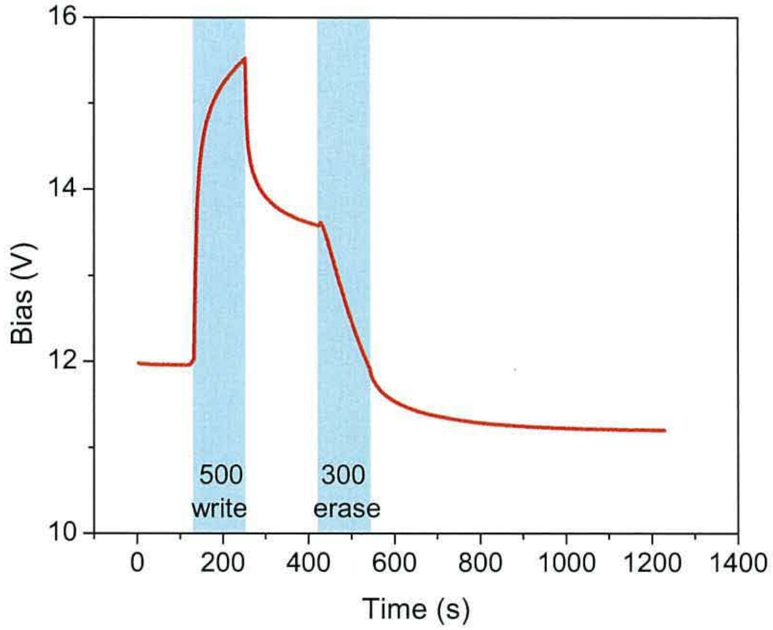
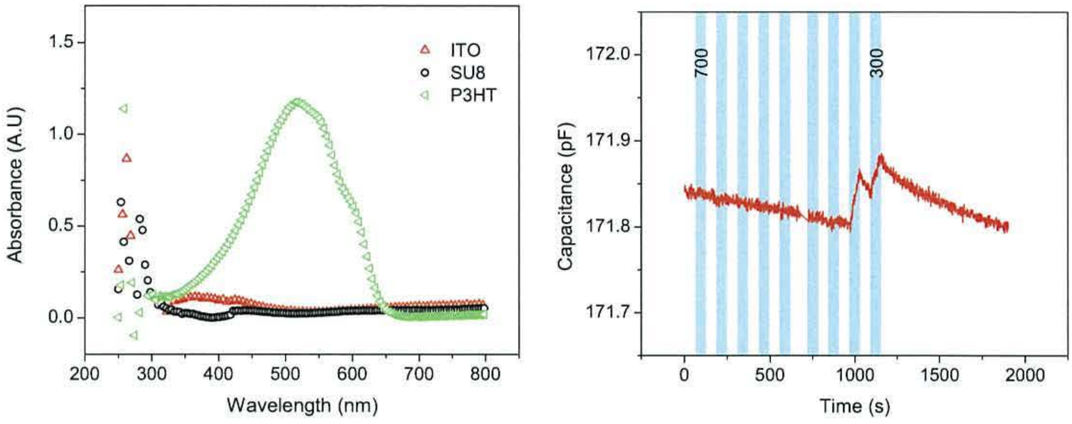


FIGURE 5.22: SU8/P3HT memory device showing change in bias voltage to track a capacitance of 165 pF during write (exposure to 500 nm light) and erase (300 nm) operations.

In order to establish whether any of the device materials absorbed light at $\lambda < 400$ nm, the absorbance spectra of the materials were individually measured at wavelengths between 250–800 nm. Layers of SU8 and P3HT were spun onto separate soda-lime glass substrates and cured as described in Section 3.3. Cleaned ITO substrates were also measured. Unfortunately the absorption spectra of these samples below 350 nm were too noisy to draw any reasonable conclusions as to which materials were responding to 300 nm light (Figure 5.23(a)). However, capacitance measurements of SU8 MIM structures (with the bias kept at 0V) revealed an increase in capacitance during exposure to 300 nm light (Figure 5.23(b)).



(a) Absorption spectra of SU8, ITO and P3HT. (b) SU8 MIM response to photo-excitation.

FIGURE 5.23: (a) Absorption spectra of SU8, ITO and P3HT layers reveal noisy data below 350 nm. (b) SU8 MIM device response to illumination at wavelengths between 300 and 700 nm.

The change in capacitance of the MIM device at 300 and 350 nm is minimal ($< 0.05\%$), indicating that photo-generated charges within the insulator are unlikely to result in the reduction in ΔV observed in the MIS devices.

MIS devices fabricated with the newer SU8 2000.5 resist did not produce the same results. Initially, irradiation with 300 or 350 nm light resulted in an increase in the tracking voltage similar to those at longer wavelengths. However repeated doses of 550 nm and 350 nm light produced a gradual increase in the tracking voltage (Figure 5.24) indicating electron trapping and associated increase in V_{FB}. As the tracking voltage approached $\sim +10$ V the device response to 350 nm light altered; after a slight increase, the tracking voltage fell slightly. As V_{FB} increased further, 550 nm light produced larger increases in the tracking voltage, whereas 350 nm caused a corresponding drop in the voltage, similar to the response seen with the previous devices (with the SU8 2002 dielectric). The inset in Figure 5.24 reveals a close-up of the response where the tracking voltage increased to ~15 V; the leading edge is due to irradiation with 550 nm light, and the trailing edge due to 350 nm light, the relatively 'flat' regions reveal the response during the dark periods.

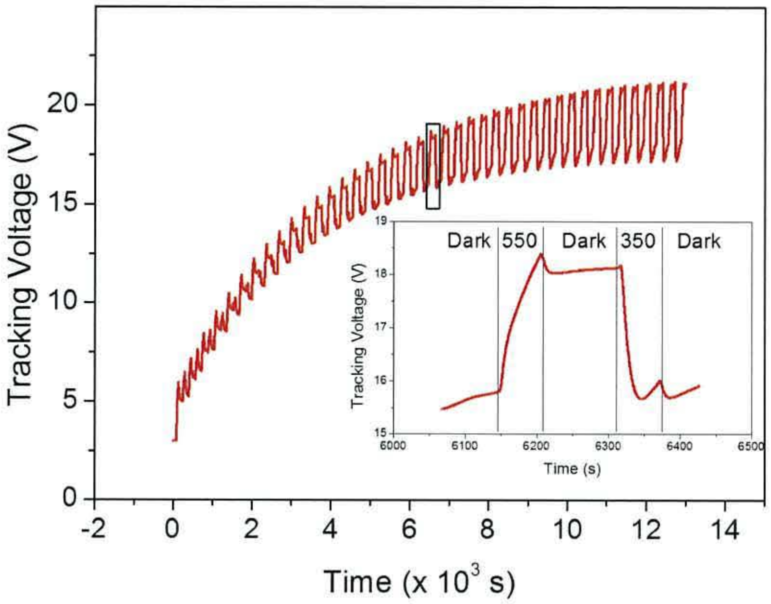


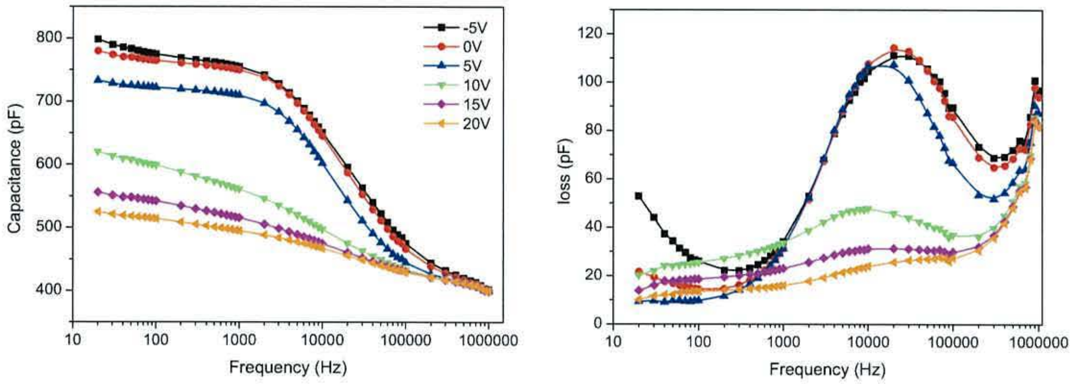
FIGURE 5.24: Constant capacitance response of SU8 2000.5/P3HT MIS capacitor when subjected to repeated doses of 550 and 350 nm light for 60 s each, with a 60 s relaxation in the dark between doses. Inset shows a close-up of the response (bounded area on main graph) after ~6000 s measurement time.

As noted in Chapter Four the MIS devices fabricated using the thinned SU8 2002 exhibited high flat band voltages, generally greater than +10 V, whereas devices made with SU8 2000.5 as the insulator had much lower flat band voltages of ~0 V. This difference was ascribed to the dosage of UV light during photo-polymerization of the SU8 layer. It is possible therefore that for devices with initially high V_{FB} irradiation with UV light below 400 nm results in further further polymerization of the SU8, reducing V_{FB}. However irradiation of SU8 2000.5 based devices with light gradually increases V_{FB} to some critical point after which UV light ($\lambda < 400$ nm) causes recombination or neutralization of trapped negative charges, reducing V_{FB}. Thus the response of SU8 devices to short wavelengths of light is dependent upon the density of trapped charges at the insulator/semiconductor interface.

5.6 MIS capacitor array

An array of MIS capacitors was fabricated as shown in Figure 3.6. SU8 was used for the dielectric layer as PSQ provided poor quality films when spun onto the aluminium gates. Prior to experiment the array was placed under vacuum in the cryostat and annealed for an hour. Upon cooling to 293 K C-V measurements were made to check the functionality of the capacitors. Unfortunately, a maximum of three devices could be tested at any one time in the cryostat, so testing of the array as an 'imaging' device was performed under ambient conditions.

Figures 5.25 and 5.26 show the results obtained from admittance measurements on a typical capacitor in an array. The C-V plot was obtained at 130 Hz, and therefore well below the Maxwell-Wagner peak observed in the G/ω–f plot (~20 kHz) in Figure 5.25(b). From the C-V plot in Figure 5.26 the active layer is estimated to be ~77 nm thick and the SU8 layer ~150 nm.



(a) C-f of MIS array.

(b) Corresponding G/ω-f plots.

FIGURE 5.25: Frequency response of SU8/P3HT MIS capacitor array under vacuum in the dark.

Increasing capacitance and loss at low frequencies in the C-f and G/ω-f plots was seen as evidence of lateral conduction in the capacitors. This was expected due to the electrodes extending across the un-patterned P3HT.

The imaging properties were tested by careful placement of a shadow mask over the array, whilst ensuring that both dark and light areas lined up over the imaging 'cells'. The shadow masks were fabricated by printing patterns, based on a 3 × 3 matrix, onto transparent overhead projector sheets (Figure 5.27). Arrays were exposed to white light from a Schott KL 1500 electronic light source. Prior to

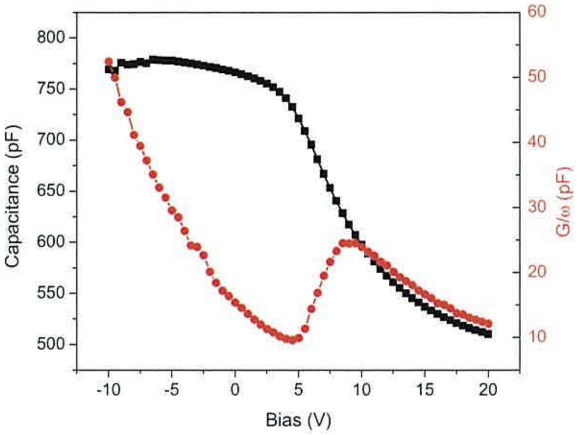


FIGURE 5.26: SU8/P3HT MIS capacitor C-V and G/ω-V response under vacuum, in the dark with an a.c. frequency of 130 Hz.

irradiation the dark capacitance of each cell was measured using the Agilent LCR meter. Measurements were made with the devices biased into depletion with a gate voltage of +20 V. Upon irradiation the capacitance of each cell was again measured.

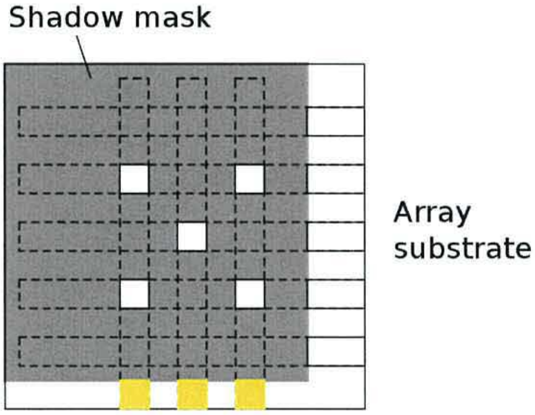
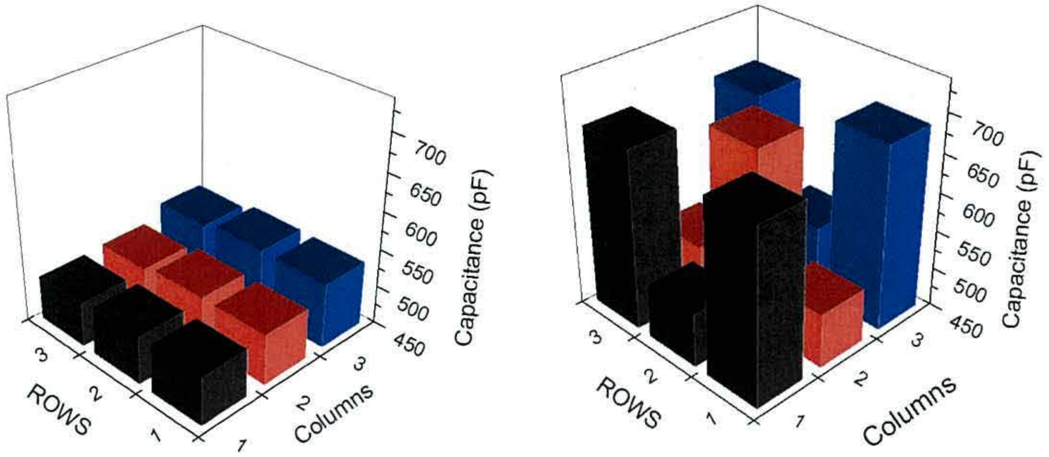


FIGURE 5.27: Schematic showing capacitor array with shadow mask attached to glass substrate.

Figures 5.28(a) and 5.28(b) are 3D representations of the array capacitances in the dark and under illumination respectively with the shadow mask aligned over the array. These results show that those devices which were exposed to the light provided an increased capacitance, whereas those under the shaded areas of the mask revealed little or no response. Various designs of shadow mask (based on the 3 × 3 matrix) were used; as expected, devices exposed to light revealed an increase in measured capacitance, whereas those in the shadows retained their 'dark' values. Thus the measured capacitances of the array cells provided an



(a) (b)

FIGURE 5.28: 3D histograms of the 3×3 array capacitance, measured (a) in the dark, and (b) under illumination with the shadow mask in place. The response under illumination reveals an image of the shadow mask. All measurements were obtained at a bias of +20 V and frequency of 1 kHz.

'electronic' image of the shadow mask. Due to the photo-oxidative doping of P3HT [137], and the longevity of trapped charges in these devices, each array was only used once for these experiments.

5.7 Charge Injection Device

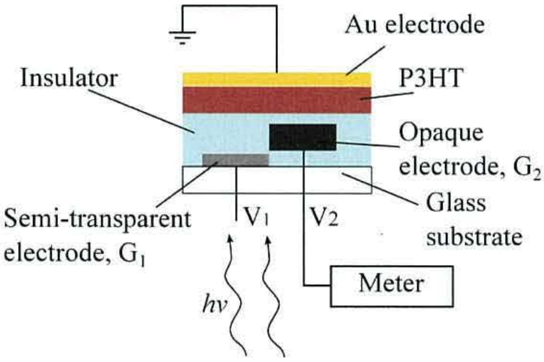


FIGURE 5.29: Schematic of charge-transfer experimental set-up.

The charge injection device (CID) as introduced in Chapter 2 is an array of MIS capacitor pairs. Here such devices were used to establish whether any charge generated during photo-excitation in one capacitor cell can be transferred to an adjacent cell. The CIDs used in this study were fabricated as described in

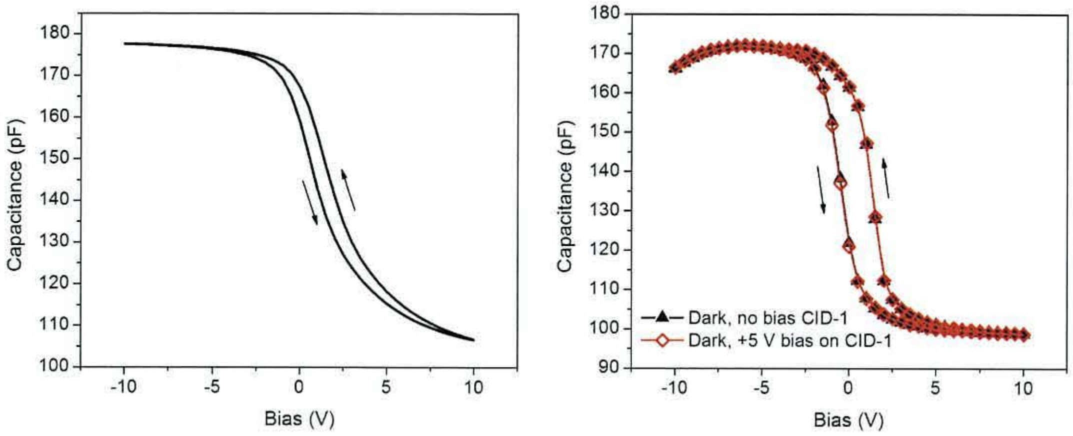
Section 3.4; as a brief recap, one cell (CID-1) had a semi-transparent electrode to allow photo-excitation, the other (CID-2) an opaque electrode to prevent charge generation due to stray light. Referring to the schematic of the experimental set-up (Figure 5.29), when a bias V_1 is applied to the gate, G_1, of CID-1, a potential well is formed under the gate. Upon illumination, photo-generated charge should accumulate above the gate. When the bias V_2 is increased to the same or preferably higher value than V_1, a *deeper* potential well is formed above G_2. The resultant potential gradient between the wells should cause any 'free' electrons to drift from CID-1 to CID-2, increasing the measured capacitance of CID-2. Thus, during a C-V measurement, when the bias applied to CID-2 is swept beyond the bias applied to CID-1 a change in the C-V plot, when compared to its 'dark' plot, would be expected if sufficient charge is transferred.

In Section 5.4.2 it was shown that the MIS capacitors produced a greater responsivity at low intensities of light. Hence as a further safeguard against the incident light affecting CID-2 (even though CID-2 was fabricated with an opaque gate) the light intensity was kept low, and the beam focused onto the gate of CID-1.

Despite fabricating the devices as described in Section 3.4, the dark C-V plots in Figure 5.30 for the first batch of devices revealed very similar capacitance values in accumulation. Even though the dielectric layers of each cell were expected to be of different thicknesses, the SU8 layers for both cells were estimated to be ~160 nm thick, and the P3HT layer ~100 nm. From Equation 2.39, the maximum storage capacity of these cells is estimated to be $\sim 1.1 \times 10^{12}$ electrons/cm^2 at a gate bias of 10 V.

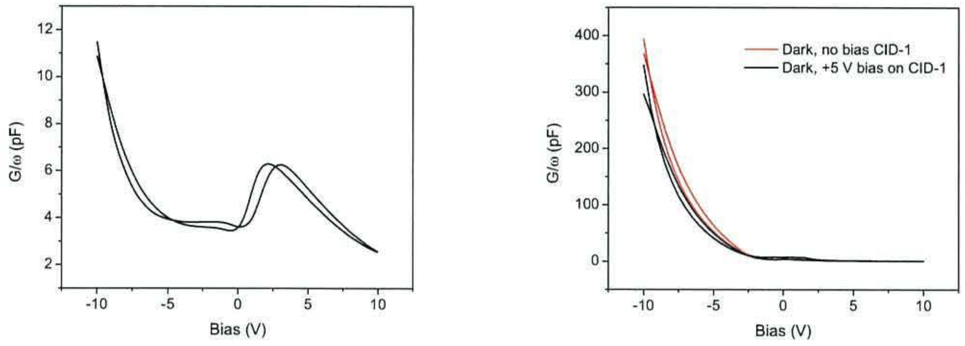
As shown in Figure 5.30(b) a further C-V plot of CID-2 (red line/diamond) was obtained with CID-1 biased at +5 V. This resulted in the measured response coinciding exactly with the measurement taken with no bias on CID-1, indicating that there were no parasitic effects from biasing CID-1 into depletion. However the C-V plots revealed CID-2 suffered from gate leakage when biased into accumulation at voltages between -6.5 and -10 V. This effect was also seen in the G/ω–V characteristics of both CID-1 and CID-2 (Figure 5.31) where the loss increased rapidly as the cells were biased further into accumulation.

Prior to any charge transfer experiments both cells were illuminated with 550 nm light (incident power of 25 μW). Figure 5.32(a) shows the response obtained



(a) (b)

FIGURE 5.30: C-V plots of adjacent cells in a Charge Injection Device. (a) C-V plot of CID-1 measured in the dark at a frequency of 500 Hz, (b) C-V plots of CID-2 measured in the dark with CID-1 un-biased (black) and CID-1 biased at +5 V (red).

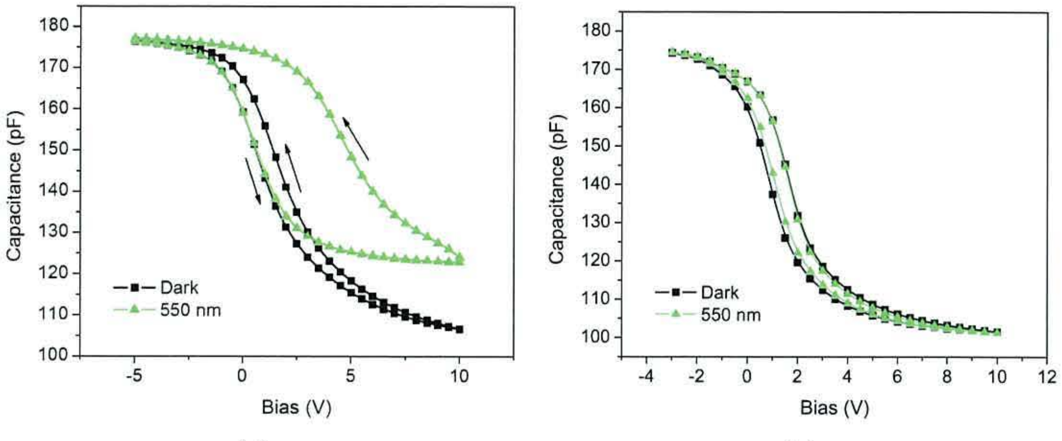


(a) (b)

FIGURE 5.31: G/ω–V plots of (a) CID-1 measured in the dark at a frequency of 500 Hz and (b) CID-2 measured in the dark with CID-1 un-biased (black) and CID-1 biased at +5 V (red). CID-2 revealed high loss values for accumulation voltages greater than -3 V.

for CID-1, where the C-V plot during illumination revealed both increased minimum capacitance and hysteresis. An estimated $\sim 4.2 \times 10^{11}$ cm^{-2} electrons were responsible for the increased hysteresis. No such response was seen in CID-2 (with CID-1 not biased, Figure 5.32(b)), the gate electrode being thick enough to prevent light transmission into the active region.

The preceding results indicated that the CID structure was suitable for the charge transfer experiment. With CID-1 biased into depletion (+5 V on the gate) and illuminated with 550 nm light, a C-V measurement was made on CID-2. The



(a) (b)

FIGURE 5.32: *C-V* responses of CID-1 and CID-2 both in the dark and under illumination with λ=550 nm. In (a) CID-1 was illuminated through the semi-transparent electrode and provided the expected response to illumination. (b) The opaque electrode of CID-2 prevented any photo-excitation. Measurement frequency was 1 kHz.

resultant plot is shown in Figure 5.33. As a comparison, plots obtained in the dark both immediately prior to, and after, illumination are also shown. The plot (red line and symbol) taken during illumination follows the initial dark plot until CID-2 is almost fully depleted, after which the minimum capacitance is seen to be slightly higher. This small increase in the minimum capacitance (2.6 pF) corresponds to a decrease in depletion width of ~7 nm, indicating there had been a migration of mobile electrons through the semiconductor from CID-1 to CID-2. During the reverse sweep a large increase in hysteresis was seen, indicating a positive shift in V_{FB} of ~2.9 V, corresponding to ~3.2×10^{11} cm^{-2} trapped electrons at the interface. This is ~76 % of the number of electrons estimated to be trapped at the interface of CID-1 in Figure 5.32(a). The subsequent dark *C-V* plot obtained immediately after illumination shows that there were still ~9.2×10^{10} cm^{-2} electrons trapped at the SU8/P3HT interface. As previous experiments had shown CID-2 did not respond to direct illumination, the result of the charge transfer experiment indicated that electrons had been transferred to CID-2 during illumination of CID-1.

Because the devices from the first batch did not have a 'stepped' gate structure, as depicted in Figure 5.29, the subsequent batch were made with un-thinned SU8 2000.5 as the dielectric. This resulted in much thicker dielectric layers; ~1.38 μm and ~500 nm for CID-1 and CID-2 respectively as calculated from their dark *C-V* plots (Figures 5.34, 5.35). The P3HT layer was estimated to be ~80 nm thick

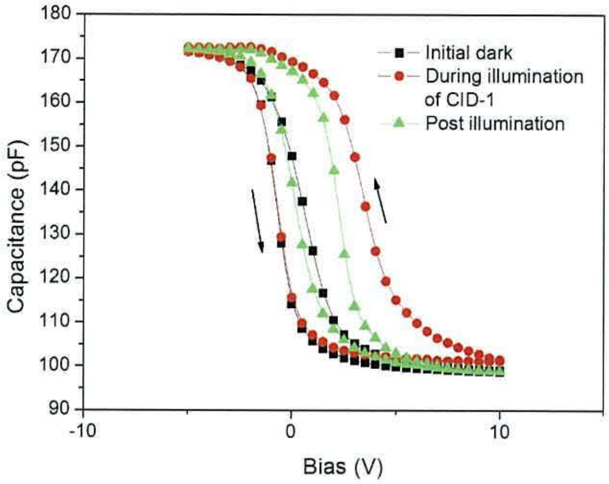


FIGURE 5.33: *C-V* plots of CID-2 taken in the dark prior to, during illumination of CID-1 with 550 nm light and post illumination in the dark. CID-1 was biased at +5 V. AC measurement frequency was 1 kHz.

for CID-1 and ~95 nm for CID-2. The maximum storage capacity was estimated to be ~2.8 $\times 10^{10}$ electrons cm^{-2} for CID-1 and ~7.7 $\times 10^{10}$ electrons cm^{-2} for CID-2.

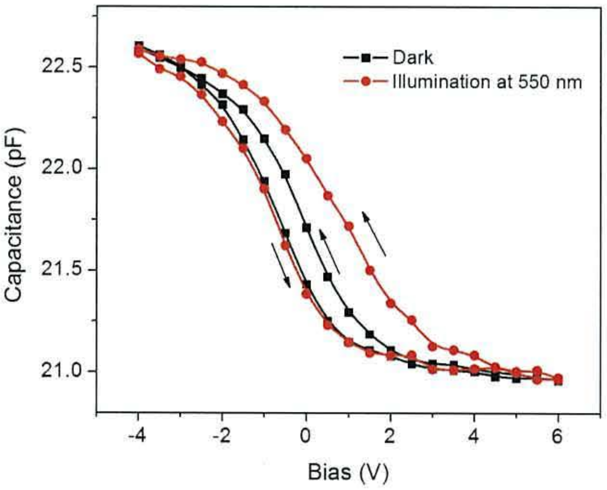


FIGURE 5.34: *C-V* plots of CID-1 taken in the dark prior to, and during illumination with 550 nm light at an intensity of 140 μW. AC measurement frequency was 500 Hz.

The initial dark *C-V* plot of CID-1 revealed the device was fully depleted with ~2 V bias on the gate. The response of CID-1 to illumination of 550 nm light with an incident power of 140 μW is also seen in Figure 5.34. Unlike the first batch of devices, no increase in the minimum capacitance was observed during illumination. This may be due to the much thicker dielectric layers in these devices compared to the first batch, resulting in lower electric fields in the insulator and depletion layer. However the observed increase in hysteresis equates to ~1.55 $\times 10^{10}$ cm^{-2} electrons trapped at the insulator/semiconductor interface. During preliminary tests, similar to those described for the first batch of devices, CID-2 did not respond either to illumination or biasing CID-1 at +5 V.

During the charge transfer experiment the gate of CID-1 was held at 0 V. As was the case for the previous batch of devices, the *C-V* plot for CID-2 (red line and symbol in Figure 5.35) shows increased hysteresis during illumination of CID-1, although an increase in the minimum capacitance was not observed. The increased hysteresis, compared to the initial dark plot, can be attributed to ~1.42 $\times 10^{10}$ cm^{-2} electrons trapped at the semiconductor/insulator interface, which is ~70 % of the estimated number of trapped electrons responsible for the increased hysteresis seen in CID-1 when under illumination (Figure 5.34). The increase in hysteresis in CID-2 can be seen as evidence of photo-generated electrons which had drifted from CID-1 to CID-2, and becoming trapped at the semiconductor/insulator interface in CID-2.

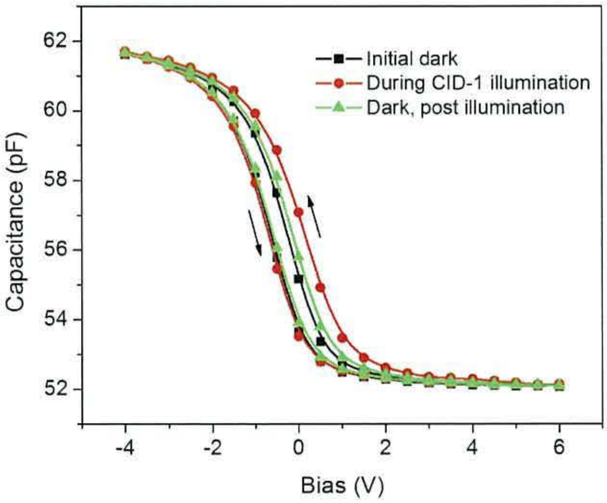


FIGURE 5.35: *C-V* plots of CID-2 taken in the dark and during illumination of CID-1 with CID-1 held at a bias of 0 V. AC measurement frequency was 500 Hz.

Further evidence of charge transfer was obtained by measuring the displacement current during illumination of CID-1. For this experiment the gate electrodes of CID-1 and CID-2 were connected in series with a Keithley 617 and 6517B electrometer respectively, as shown in Figure 5.36. A voltage of -5 V was applied to the ohmic contact, biasing both devices into depletion. Due to the structure of the CID, the field in cell CID-2 is greater than in CID-1, and thus any free electrons should drift from CID-1 to CID-2.

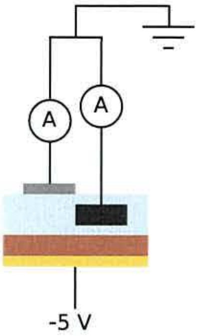


FIGURE 5.36: Experimental set-up to measure displacement current.

To minimize the effect of the initial transient (due to the application of the bias), measurements commenced 5 minutes after the bias was applied. As the resultant plots show (Figure 5.37) this transient was still present in CID-1, at the start of the illumination when light of wavelength 550 nm and incident intensity 140 μW, from the monochromator was focused onto CID-1, and cycled on and off for periods of 60 seconds each. The red plot in Figure 5.37 shows the response of CID-1, which clearly responds to the illumination phase. Although superimposed on the transient response, an initial 'step', with a magnitude of ~1.09 pA, is evident in the plot. Successive cycles of illumination produced similar responses from CID-1, although the photo-enhanced current decreased with each successive exposure to light. As soon as the light was extinguished the current decayed back to the underlying baseline. CID-2 also produced a sharp initial increase in current, ~0.83 pA during the first cycle. Following the initial response the current decayed during the light-on period to ~0.4 pA above the baseline. During the dark phases an initial reduction in current could be seen followed by gradual decrease in the current decay to ~3.3 pA.

The ratio of the displacement currents during illumination, I_2/I_1, was 0.76, where I_1 and I_2 are the currents in CID-1 and CID-2 respectively. This ratio is almost the same as that found for the ratio of trapped electrons in the C-V measurement above (0.7). A correlation between the ratios of trapped electrons and displacement currents can be found by relating the displacement current to the change in capacitance caused by electron trapping at the semiconductor/insulator interface. The displacement current in a capacitor is defined as

$$I = C\frac{d(V)}{dt} + V\frac{d(C)}{dt}, \tag{5.18}$$

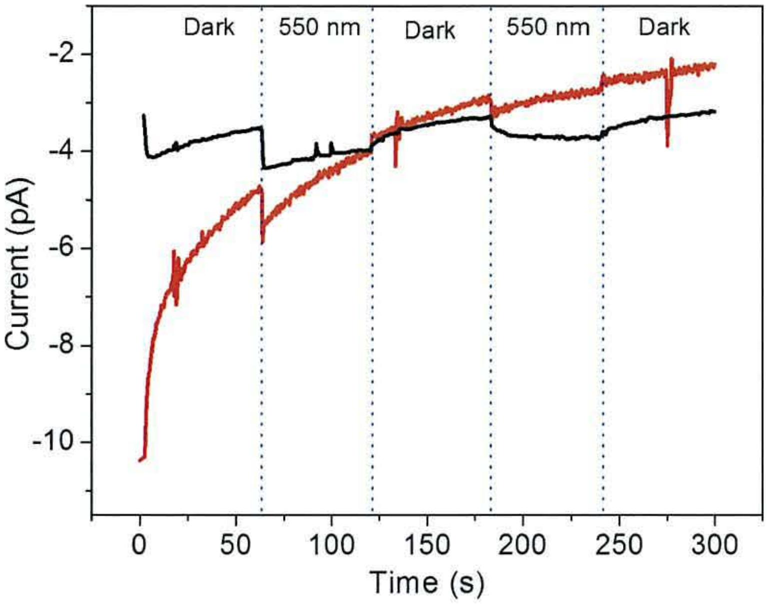


FIGURE 5.37: Displacement currents measured in CID-1 (red) and CID-2 (black).

however in this experiment the voltage V is constant and Equation 5.18 reduces to

$$I = V\frac{d(C)}{dt}. \tag{5.19}$$

In depletion the capacitance, $C(t)$, of the semiconductor at a time t is dependent on the depletion width $d(t)$:

$$C(t) = \frac{\varepsilon_0 \varepsilon_s}{d(t)}, \tag{5.20}$$

where ε_s is the relative permittivity of the semiconductor and ε_0 is the permittivity of free space.

If there are n_t electrons trapped at the semiconductor/insulator interface at time t then the depletion width reduces by (from Equation 2.38)

$$\Delta d = \frac{n_t(t)}{N_A}, \tag{5.21}$$

therefore the depletion width at time t is

$$d(t) = d - \frac{n_t(t)}{N_A}. \tag{5.22}$$

Thus the capacitance is now

$$C(t) = \varepsilon_0 \varepsilon_s N_A \frac{1}{N_A d - n_t}, \tag{5.23}$$

and

$$\frac{d}{dt}C(t) = \varepsilon_0\varepsilon_s N_A \frac{d}{dt}\left(\frac{1}{N_A d - n_t}\right)$$
$$= \varepsilon_0\varepsilon_s N_A \left(\frac{1}{(N_A d - n_t)^2}\right)\frac{dn_t}{dt}. \tag{5.24}$$

At time $t = 0$ there are no trapped electrons, $n_t = 0$, and

$$\frac{d}{dt}C(t) = \frac{\varepsilon_0\varepsilon_s}{d^2 N_A}\frac{dn_t}{dt}$$
$$= \frac{C}{dN_A}\frac{dn_t}{dt}. \tag{5.25}$$

The ratio of initial displacement currents in CID-1 and CID-2 should therefore be

$$\frac{I_2}{I_1} = \frac{\dfrac{C_2}{d_2 N_{A2}}\dfrac{dn_{t2}}{dt}}{\dfrac{C_1}{d_1 N_{A1}}\dfrac{dn_{t1}}{dt}}, \tag{5.26}$$

where the subscripts 1 and 2 refer to CID-1 and CID-2 respectively. Rearranging Equation 5.26 provides the ratio of electron trapping rates:

$$\frac{\dfrac{dn_{t2}}{dt}}{\dfrac{dn_{t1}}{dt}} = \frac{I_2}{I_1}\frac{C_1 d_2 N_{A2}}{C_2 d_1 N_{A1}}. \tag{5.27}$$

The acceptor doping density N_A for CID-1 and CID-2 was determined to be ~9×10^{15} cm^{-3} and ~5.4×10^{15} cm^{-3} respectively, as deduced from Mott-Schottky plots. Assuming that CID-1 and CID-2 are both in depletion when biased at 5 V, and using the magnitude of the peak currents obtained for CID-1 and CID-2 from Figure 5.36, Equation 5.27 yields an electron trapping ratio of 0.66 which is very close to the ratio determined from the *C-V* plots.

5.8 Summary

C-V measurements have shown PSQ and SU8 based MIS capacitors responded to monochromatic light of wavelengths in the range ~700 nm and ~400 nm as the devices enter depletion. The response manifests itself as an increase in the minimum measured capacitance in depletion as well as a shift to more positive values of the flatband voltage, which is seen as increased hysteresis in the *C-V* plot. Shifts in V_{FB} are caused by photo-generated electrons becoming trapped at the semiconductor/insulator interface. The increased flatband voltage was caused by photo-generated electrons trapped either at the semiconductor/insulator interface or in the insulator. Also the trapped electrons effectively shield the semiconductor from further increases in bias. Consequently charge neutrality is maintained at the same degree of band bending and the depletion region stops growing consistent with an increased minimum capacitance in depletion.

Relaxation of V_{FB} to its initial dark value was found to be dependent upon the dielectric used. *C-V* measurements obtained immediately after and at various times thereafter revealed the relaxation took much longer in the thinned SU8 devices than the PSQ devices. Constant capacitance measurements revealed relaxation of V_{FB} for the SU8 device took in excess of 125 hours at room temperature after exposure to 400 nm wavelength light. In comparison relaxation of charges in the PSQ device took ∼5 hours after illumination. The kinetics of the relaxation process was found to follow a non-exponential decay which could be described either by Kohlrausch's law or a three-term exponential function, from which trap depths were estimated to be deeper in the SU8 device.

The characteristics of the *C-V* response were seen to depend on wavelength, incident power and bias scan rate. A *Responsivity* was defined as the ratio of the change in minimum capacitance and incident light power, from which the responsivity was seen to increase with photon energy. The MIS capacitors were also found to be sensitive to the incident power, being more responsive at lower intensities, and was measured in terms of trapping efficiency. Trapping efficiency was defined as the ratio of trapped electrons (determined from the increase in V_{FB}) to the number of photons absorbed in the semiconductor layer. As the incident intensity increased, the trapping efficiency decreased indicating the device was reaching saturation, and recombination of carriers exceeds the electron trapping rate. Increasing the bias scan rate decreases the effect of illumination on the *C-V* response. At slower scan rates the integration time for photo-generated electrons is proportionately longer, increasing the number of electrons becoming trapped. However as the scan rate decreased the trapping efficiency increased, which is also indicative of saturation effects. A basic model for the *C-V* response of MIS capacitors under illumination was developed. Simulated responses were similar to the experimental results, indicating the basic model is correct. However the model requires further improvement to account for recombination, de-trapping of electrons and the presence of free photo-generated electrons in the semiconductor.

The loss peaks also shifted to more positive biases corresponding to the shifts seen in the C-V plots, although they were broader under illumination, indicating a wider distribution of traps could respond to the ac signal. Analysis of the loss peaks revealed that illumination did not significantly alter the density of interface states.

Generally the increase in V_{FB} during 60 s pulses of light could be described by a two-term exponential function. The initial response of both PSQ and SU8 MIS capacitors was similar with characteristic time constants of $\sim$5 s. After this initial growth the SU8 devices tended to saturate, whereas in the PSQ devices V_{FB} continued to increase at a slower rate. This difference is probably due to the chosen value of capacitance to track. The value chosen for the PSQ placed the device further into depletion than the SU8 device resulting in a wider depletion region in which excitons can dissociate. Decay characteristics also revealed a two stage process which were fitted to the stretched exponential or Kohlrausch equation, although a better fit was obtained from a two-term exponential function over the duration of the measurement. Initial decays in both PSQ and SU8 devices were similar with time constants of $\sim$3–5 s. Time constants for the second phase of the decay in the SU8 device decreased after irradiation of light with shorter wavelengths, indicating a correlation between photon energy and the decay kinetics after irradiation. This effect was not seen in the PSQ device which generally exhibited similar time constants after illumination with different wavelengths.

Irradiation with sub 400 nm light effectively erased the charge from the SU8 device, thus irradiating the device with 500 nm light injected charge and a subsequent pulse of 300 nm light reduced the overall charge within the device; a write/erase process for a memory device. It was supposed that remnant photo-initiator within the insulator, sensitive to UV light, initiated further polymerization of the SU8 reducing V_{FB} as seen in Chapter 4.

An array of 3 × 3 MIS capacitors was fabricated and shown to be able to act as an imaging device using a simple shadow mask. These arrays were tested in air but degraded fairly quickly.

Finally, charge injection devices indicated that some charge had been transferred between adjacent MIS capacitors in a charge injection device structure. Using a thick opaque electrode, control experiments revealed that the CV response of the receiving capacitor (CID-2) was unaltered during irradiation, whereas the capacitor with a semi-transparent electrode (CID-1) did respond. A C-V measurement on CID-2 whilst CID-1 was irradiated with light and biased into depletion, revealed an increase in minimum capacitance and hysteresis, indicative of charges flowing from CID-1 into CID-2. The ratio of the increase in hysteresis between CID-1 and CID-2 was estimated to be 0.76. A further experiment measured the displacement currents during illumination of the structure. The ratio of displacement currents between CID-1 and CID-2 was 0.66 which correlates well with the shifts seen in the C-V plots.

Chapter 6

Organic Photo-Detector for Integrated Surface Plasmon Resonance Biosensors

6.1 Inroduction

This chapter presents the results of work undertaken in collaboration with Dr. M. Bora of the Soft Semiconductor Group, Massachusetts Institute of Technology, under the supervision of Associate Professor Marc Baldo and published in Optics Express [172].

Surface plasmon resonance (SPR) is a highly sensitive and powerful technique allowing real-time, label-free measurement of biomolecular interactions. Current techniques for SPR biosenesing involve the use of carefully aligned optics, often resulting in large, costly systems. This work demonstrates progress towards an integrated, inexpensive mobile device.

6.1.1 Surface Plasmon Resonance

Surface plasmon polaritons or surface plasmon waves (SPW) are electromagnetic waves that propagate parallel to a metal/dielectric interface, and decay exponentially into both media (see Figure 6.1). The SPW is a transverse magnetic

(TM) polarized wave (i.e. the magnetic vector is perpendicular to the direction of propagation), with a wavevector k_{sp} given by [173]

$$k_{sp} = \frac{\omega}{c}\sqrt{\frac{\epsilon_d \epsilon_m}{\epsilon_d + \epsilon_m}} \tag{6.1}$$

where ω is the angular frequency, c the speed of light, $\epsilon_d = \epsilon_d^{'} + j\epsilon_d^{''}$ and $\epsilon_m = \epsilon_m^{'} + j\epsilon_m^{''}$ are the complex dielectric constants of the dielectric and metal respectively. Thus k_{sp} is also complex, with the imaginary part representing losses in the materials. For a lossless device $\epsilon_d^{''} = \epsilon_m^{''} = 0$ and, provided $\epsilon_d^{'}$ and $\epsilon_m^{'}$ are of opposite sign and $\epsilon_m^{'} < -\epsilon_d^{'}$, k_{sp} is positive and surface plasmon modes exist [174]. These conditions imply $\epsilon_m^{'}$ must be negative as $\epsilon_d^{'}$ is usually positive, and are fulfilled by metals such as gold, silver and aluminium at optical frequencies [173].

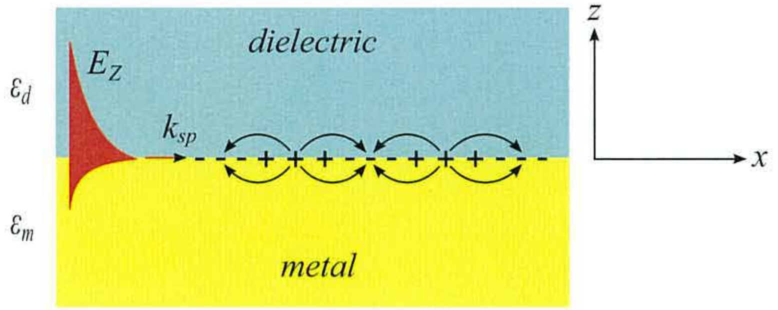


FIGURE 6.1: The charges and electromagnetic fields of surface plasmons propagating along the metal/dielectric interface in the x direction. The E_z field decays exponentially into both media. Adapted from Ref. [174].

Surface plasmons are excited into resonance by an optical wave provided the wavevector of the light, k_{ph}, matches that of the SPW at the metal/dielectric interface. However direct excitation is not possible as k_{sp} is larger than k_{ph}. The momentum of the incident light can be enhanced through either diffraction, or attenuated total reflection (ATR) using prism couplers [173, 174]. The most common arrangement is the Kretschmann configuration, Figure 6.2(a). Light coupled through a high refractive index prism in the Kretschmann configuration is totally reflected at the base of the prism, inducing an evanescent wave which propagates along the metal/dielectric interface, where

$$k_{ph} = \frac{2\pi}{\lambda} n_p sin(\theta) \tag{6.2}$$

and θ is the angle of incidence, n_p the refractive index of the prism and λ the wavelength of the incident light. Thus, adjusting the angle of incidence changes the wavevector of the evanescent wave and the condition for surface plasmon resonance (SPR), $k_{sp} = k_{ph}$, can be met. At resonance, energy is transferred from the light wave to a surface plasmon; this process is accompanied by a dip in intensity of the reflected light (Figure 6.2(b)). As indicated in Figure 6.1 the electromagnetic field associated with the SPW extends further into the dielectric medium than into the metal layer, resulting in the SPR condition being highly sensitive to the optical properties of the dielectric adjacent to the metal film [175]. Thus variations in the optical properties of the dielectric can be measured by sensing changes in the SPR condition. Small changes in the refractive index of the dielectric alters the angle of resonance. Absorption of biological or chemical species increases the refractive index at the sensor surface producing a change in k_{sp} and consequently a shift in the angle of resonance. If the angle of incidence is maintained, a change in reflectivity, ΔR, can be measured. Detection of specific species is facilitated by functionalization of the metal surface with a suitable receptor. Analytes in a buffer solution, with a refractive index lower than the prism, flowing over the functionalized surface bind to the receptors causing changes in the local refractive index producing a measurable signal.

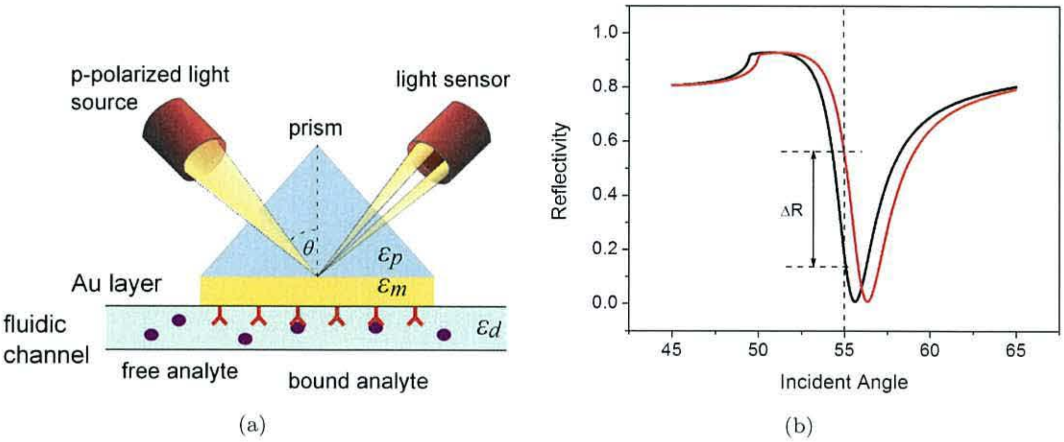


FIGURE 6.2: (a)Surface plasmon resonance in the Kretschmann configuration. Resonance occurs at the incident angle where the wavevectors of the light and SPW are matched, resulting in a dip in the reflectivity. Bound analytes change the refractive index of the adjacent dielectric, increasing the resonant angle. (b) Sensorgram of reflectivity vs. incident angle illustrating shift in resonance and measurement of ΔR.

The SPR electromagnetic field penetrates further into the dielectric when silver is used as the metal layer rather than gold, and provides the highest sensitivity. Silver, though, is prone to oxidation so that gold is the preferred choice [175].

6.1.2 Near-field detection of surface plasmons

Conventional SPR spectroscopy uses a far-field detector in the form of a photodiode or CCD array positioned to measure the intensity of the reflected light beam. Integration of a near-field detector with the sensing gold layer would reduce the optical complexity and lead to more compact devices. Optimum sensitivity in a conventional SPR sensor is obtained with ∼50 nm thick gold layers [174]. As previously stated the electromagnetic field extends into the dielectric, which is enclosed within a microfluidic chamber, whereas the field at the other surface of the gold layer is negligible, preventing placement of a near-field detector on the external surfaces. Maple *et al.* have demonstrated SPR detection in a ∼100 nm thick organic photovoltaic cell (OPV) by splitting the SPW supporting layer in two and sandwiching the OPV between the layers [176]. Figure 6.3 illustrates how near-field detection of surface plasmons can be implemented by inserting an OPV between two thin gold layers.

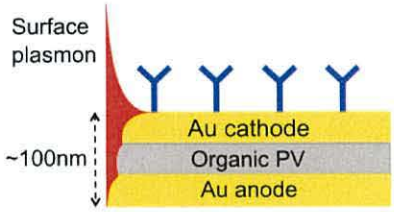


FIGURE 6.3: Cross-section of a near-field plasmon detector. The conventional far-field detector has been replaced by an organic photovoltaic cell sandwiched between two gold layers.

The function of the detector is to convert plasmon modes into an electrical signal. This requires a strong electromagnetic field extending through the OPV, forming excitons which dissociate into free mobile charges. Following the method reported by Celebi *et al.* [177], simulation of the electric field within a model OPV as a function of incident angle, indicates that a strong field extends through the OPV at resonance (Figure 6.4). For off-resonance angles, incident light is mainly reflected.

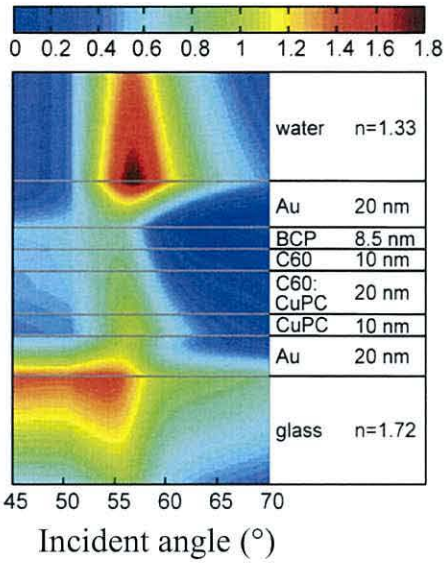


FIGURE 6.4: Simulation showing the relative amplitude of the electric field for the transverse magnetic mode. The field extends through the organic layers with a maximum amplitude observed at the gold/water interface. Simulation courtesy of M. Bora.

6.1.3 Photocurrent generation

The mechanism of photocurrent generation within the SPR sensor is illustrated in Figure 6.5. Upon illumination at the critical angle, surface plasmons are excited into resonance. Energy from the plasmonic modes is absorbed in the organic layers forming excitons (bound electron-hole pairs). Excitons which diffuse towards a donor/acceptor interface dissociate generating charges. As the potential difference between the ionisation potential of the donor and electron affinity of the acceptor is greater than the exciton binding energy, the bound pair dissociates with the electron hopping to the LUMO of the acceptor. The hole stays in the donor material and the resultant charges diffuse to the contacts where they can flow into an external circuit.

6.2 Experimental

13 mm ×13 mm square substrates of high refractive index glass, n=1.72 (SF10, Schott AG), were cleaned following the cleaning process outlined in Chapter 3, and then transferred to a N_2 glovebox. Devices were grown in an Angstrom thermal evaporator under high vacuum $< 3\times10^{-6}$ Torr. A 3 nm chrome adhesion layer and 20 nm gold film were evaporated, at 0.5 Å/s and 1 Å/s

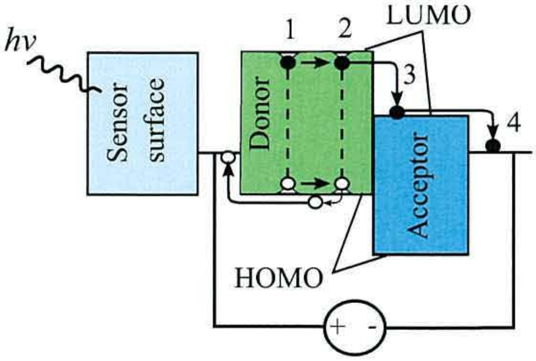


FIGURE 6.5: Four steps in the process of photocurrent generation. The boxes represent the relative energy gaps of the donor and acceptor. The dashed lines between the electrons (•) and holes (∘) represent excitons. In step 1 the surface plasmon has been absorbed by the OPV forming an exciton, with a binding energy ~0.5–1 eV within the donor bandgap. During step 2 the exciton diffuses to the donor/acceptor interface where it dissociates (step 3). In step 4 electrons and holes diffuse to the contacts . Adapted from Ref.[178].

respectively, through a shadow mask to form the anode (four per substrate). The organic materials, copper phthalocyanine (CuPC), buckminsterfullerine (C_{60}) and bathocuproine (BCP) (Sigma Aldrich), were purified by thermal sublimation prior to thermal evaporation [179]. Three organic layers: 10 nm CuPC, 20 nm bulk heterojunction of CuPC and C_{60}, 10 nm C_{60} were deposited at 1 Å/s through a shadow mask. An 8.5 nm BCP film acts not only as an exciton blocking layer [180], but also protects the C_{60} layer from penetration of evaporated metal [176, 181]. Finally a 20 nm gold top electrode was patterned through a third shadow mask. This resulted in devices ~100 nm thick, with an active area ~0.79 mm^2 as shown in Figure 6.6. Polydimethylsiloxane (PDMS, Dow Corning) microfluidic flow chambers, with a volume of 1.2 μL, were moulded from SU8 masters using a mixture of 10:1 elastomer to primer and baked overnight in a vacuum oven at 65 °C. Flow chambers were fitted to the top gold contact of the fabricated photovoltaic cells. PEEK^{TM} bio-compatible tubing (Upchurch Scientific) and associated connectors were used to connect the flow chamber to an Agilent 1100 HPLC autosampler.

The completed biosensor (Figure 6.7) was attached to a hemi-cylindrical prism (fabricated from SF10 glass) using index matching fluid (Cargille Laboratories). The whole assembly was mounted on a motorized rotation stage (AF Optical) such that the rotational axis and symmetrical axis of the prism were in alignment. Thus the incident angle of the light source could be altered by rotating the stage. A 1 μW 670 nm wavelength laser provided the light which was collimated,

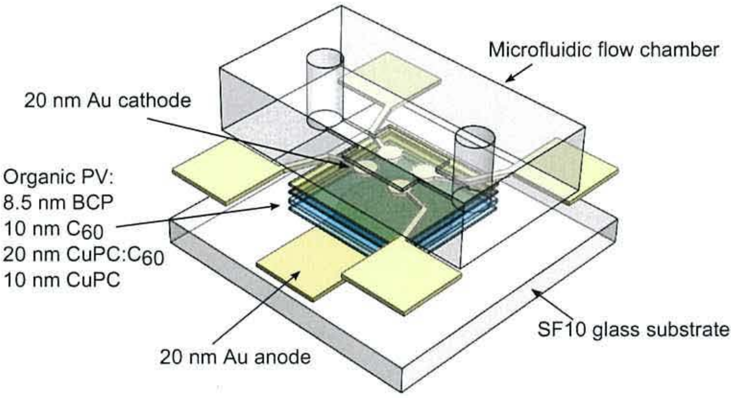


FIGURE 6.6: Device structure of organic photo-detector for surface plasmon resonance biosensing applications. A thin organic photovoltaic cell is sandwiched between two thin gold electrodes to provide near-field detection of SPR. The PDMS flow chamber sits on the top gold electrodes, which act as the biosensing surfaces.

p-polarized and focused onto the sample. Reflectivity was tracked by measuring the photo-current from a silicon photo-diode. Photo-current from both the organic photovoltaic and silicon detector were measured with a Keithley 2602 dual source-meter at a sampling period of 1 s, with the sensor surface (cathode) grounded.

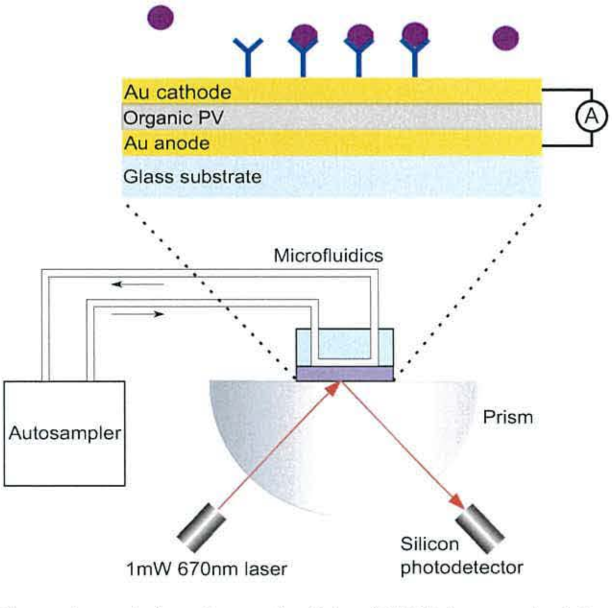


FIGURE 6.7: Experimental setup. A thin OPV is sandwiched between two thin gold layers. Analytes in a buffer solution flow through the microfluidic circuit under the control of the autosampler. P-polarized light is provided by a 1 mW laser at a wavelength of 670 nm. Binding events at the gold surface cause changes in the intensity of reflected light and photocurrent which are monitored as a function of incident angle.

Programmed pulses of water and bio-molecular solutions were delivered to the sensor in a saline buffer by an Agilent 1100 autosampler. The flow rate of the buffer solution was set at 250 μl/min and the injection volume of the pulses was set at 125 μl. Prior to injection of any pulses the microfluidic system was flushed with the buffer solution.

6.3 Results

The current-voltage (I-V) characteristics of a typical device, obtained both prior to, and during HEPES buffer flow through the microfluidic system under ambient conditions, are shown in Figure 6.8. The curves reveals typical diode behaviour with good rectification indicated by high current under forward bias and low current under reverse bias. Negligible photocurrent is observed as expected for such a thin OPV [176].

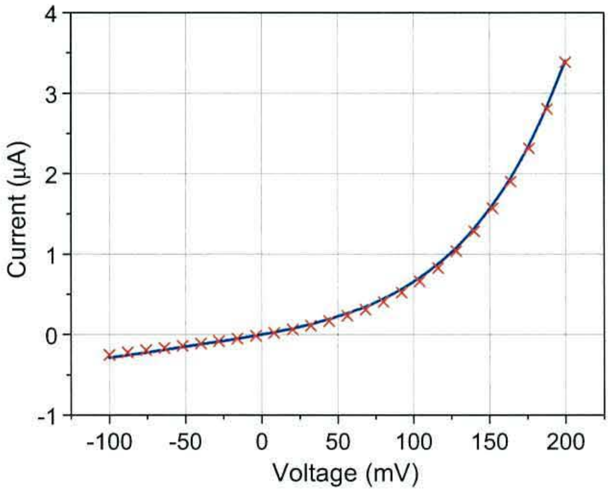


FIGURE 6.8: Current-voltage characteristic for a typical OPV measured under ambient conditions (×) and with HEPES buffer solution flowing through the microfluidic chamber (solid blue line). The diode exhibits low reverse bias current and high current in the forward direction indicating good rectification, under both conditions.

C_{60} has been shown to suffer from photo-induced degradation in the presence of oxygen [182], however no instabilities were observed in these devices.

6.3.1 Angular Dependence of Photocurrent and Reflectivity

The angular dependence of photocurrent and reflectivity of the sensor was measured by immersing the sensor surface in a saline buffer solution (HEPES, GE Healthcare). A collimated, p-polarized light beam from a 1 μW, 670 nm wavelength laser was directed at the surface of the sensor whilst rotating the prism and sensor (Figure 6.7). The measured reflectivity (output of the silicon photodiode) and photocurrent from the sensor show a maximum in sensor current coinciding with the minimum in reflectivity at the resonant condition, which occurred at an incident angle of ~58° (Figure 6.9).

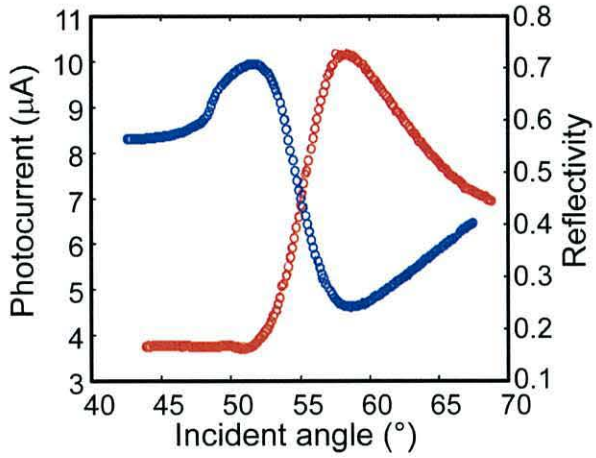


FIGURE 6.9: Angular dependence of photocurrent (○) and reflectivity (○) of the SPR sensor. Sensor photocurrent increases coincident with decreasing reflectivity as the angle of incidence passes through the condition for resonance.

At resonance the photocurrent from the OPV was ~2.5 × higher than the minimum current measured off-resonance, due solely to the enhanced field generated at resonance. Thus the photocurrent from the near-field detector is analogous to reflectivity in the detection of surface plasmon resonance. The width of the resonance is broader than the simulated response (Figure 6.2(b)), indicative of a reduced sensor sensitivity. Reduced sensitivity and broadening of the resonance is caused by the scattering of surface plasmons on rough surfaces [183]. The gold layers in these devices had a surface roughness of ~10 nm, thus the sensitivity of the sensor may be enhanced by preparing smoother gold surfaces.

6.3.2 Sensor Response

Prior to functioinalization of the sensor, its stability was determined by injecting 30 and 60 s pulses of water into the constant flow of the saline buffer solution (HEPES). For this test the incident angle was set to the angle corresponding to the maximal slope of the leading edge of the resonance dip in Figure 6.9. Figure 6.10 shows the photocurrents obtained from near-field detection with the OPV and reflected light measured with the silicon photodiode. As the water pulses reach the sensor surface the slight change in refractive index resulted in increased current from the OPV proportionate to the decreased current from the silicon photodiode. The difference in peak currents for the two pulses was possibly caused by intermixing of the water with the buffer solution; the 30 s pulse becoming more dispersed resulting in a smaller change in refractive index. The sensor exhibited good stability, with negligible change in the baseline current after each water pulse.

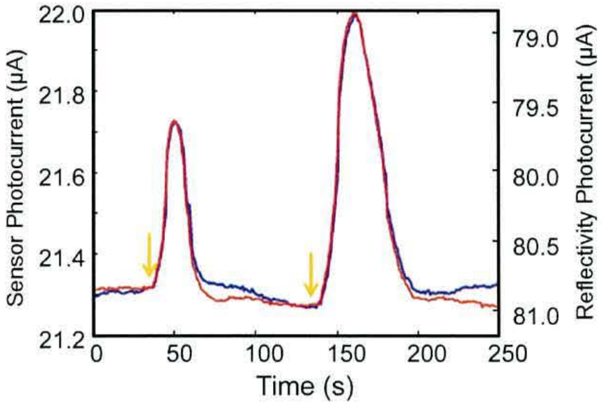


FIGURE 6.10: Sensor response to two water pulses in constant flow of HEPES buffer. Arrows indicate time of injection of water. The reflectivity scale has been inverted to show equivalence of OPV current (red line) and reflectivity (blue line).

6.3.3 Specific Binding

In order to perform a specific binding assay for biotin-neutravidin, the gold surface had to be functionalized with a suitable receptor. This is usually accomplished by the covalent attachment of the biological sensing element to the gold layer via a linker, which is usually a self-assembled monolayer of thiol molecules. The thiol group attaches to the gold, with a suitably reactive group at the other end (ligand molecule). Assembly of thiols is usually performed in ethanol. However the organic materials are weakly soluble in ethanol and an alternative method was necessary. Functionalization was achieved by immersing the sensor in water for 2 hours with a 5:1 molar mixture of PEG (polyethylene glycol) acid disulphide and biotin PEG disulphide (Polypure, Norway). Neutravidin binds to the biotin moieties, which are spaced out by the PEG to prevent steric hindrance between binding sites [184]. PEG also helps to prevent non-specific binding with the gold surface [185].

After functionalization the gold surface was exposed to pulses of 1 mg/ml solution of casein to passivate any non-specific binding sites [186]. Following this, 125 μL pulses of 250 μg/mL neutravidin (Pierce Biotechnology, USA) were injected into a constant flow of the HEPES buffer. The response to three casein and two neutravidin pulses are shown in Figure 6.11, where both reflectivity and OPV current respond to the binding events at the sensor surface.

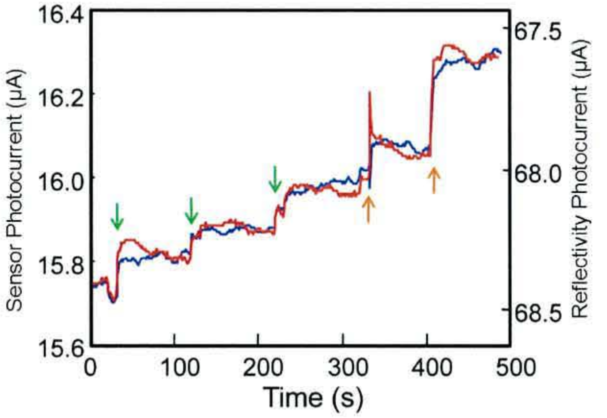


FIGURE 6.11: Sensor response to injections of casein (green arrow) to passivate non-specific binding sites and specific binding of neutravidin (orange arrows).

The same binding experiment was performed using a conventional SPR sensor with a 50 nm thick gold layer, functionalized with PEG/biotin in an ethanol solution. The estimated sensitivity of the conventional sensor was approximately three times better than the near-field sensor. This could be due to surface functionalization using water for the near-field device. Functionalization in water results in decreased surface coverage due to the hydration volume of the ethylene glycol moieties. Removal of water from these moieties is thermodynamically unfavourable, preventing close packing of the monolayer [187]. Better sensitivity may be obtained if surface functionalization is performed using carboxylmethyl dextran, which provides a higher density of binding sites [173, 188].

6.4 Summary

The far-field detector in conventional SPR sensors has been replaced by a near-field detector, namely an organic photovoltaic cell, sandwiched between two gold layers. Concurrent measurements of the reflectivity and photocurrent from the OPV demonstrated that the OPV is capable of producing photocurrent from surface plasmon resonance and that the current is modulated by binding events at the sensor surface. Thus the two measurements are equivalent.

The sensitivity of the detector was lower than a conventional SPR sensor. However the sensitivity of the near-field device was probably affected by inferior surface functionalization. Further scope to improve the performance of the sensor include using longer wavelength light [189], using silver/gold bimetallic films [190] and careful preparation of the metal layers to reduce their surface roughness.

Chapter 7

Conclusions and Further Work

7.1 Conclusions

The main work in this thesis was to assess the possibility of fabricating light sensing arrays similar in concept to charge-coupled devices. In pursuit of this objective, MIS capacitors were fabricated from two different insulators, PSQ and SU8, and the archetypal organic semiconductor P3HT. These devices were characterised in the dark and under illumination with monochromatic light using admittance spectroscopy and current-voltage measurements. Their transient responses were also monitored using a constant capacitance technique.

Initial measurements were performed on MIM structures which showed that PSQ had a higher DC resistivity $\sim 10^{13}\,\Omega$cm than the $\sim 10^{12}\,\Omega$cm for the SU8 layers. The dielectric constant of the SU8 layers also exhibited a stronger frequency dependence.

Classical p-type semiconductor behaviour was observed in C-V plots of the MIS devices, with a transition from accumulation to depletion at positive gate voltages. Very little hysteresis was evident in the C-V plots at a temperature of 303 K for devices with either dielectric. V_{FB} in PSQ MIS devices was $\sim$0 V indicating few, if any, trapped charges at the interface. Acceptor doping density of the P3HT film was determined to be ~ 4.5–9×10^{15} cm^{-3} for the PSQ based devices. V_{FB} was found to be dependent on the UV dosage applied to the SU8 layers during fabrication. Low UV dosage resulted in high V_{FB} $\sim$20 V. Increased doses eventually resulted in devices with V_{FB} $\sim$0 V. The dependence of V_{FB} on

UV dosage was related to remnant photo-initiator in the SU8. N_A in devices with high V_{FB} was found to be $\sim 2\times 10^{16}$ cm^{-3}, reducing to $\sim 3\times 10^{15}$ cm^{-3} for devices with V_{FB} ~0 V. Dopants originating from the insulator were cited as a possible cause for the increased N_A.

The frequency dependency of the capacitance and loss revealed the classic Maxwell-Wagner (M-W) dispersion at high frequencies for devices with either insulator. SU8 devices with high V_{FB} featured a broader M-W dispersion indicative of a distribution of time constants and higher disorder in the semiconductor. The low frequency capacitance decreased with increasing depletion voltages, which combined with the decreasing magnitude of the associated loss peaks provided clear evidence of the formation of a space charge layer in the semiconductor. For accumulation voltages the low frequency loss increased, as did the capacitance caused by the parasitic effects of lateral conduction and losses in the insulator. Bearing in mind the increased losses at low frequencies, the probe frequencies for the C-V measurements were chosen to be at least an order of magnitude below the M-W peak frequency. Series contact effects were also evident in the C-f and G/ω-f plots with a dispersion appearing at frequencies higher than 1 MHz.

MIS devices with both PSQ and SU8 insulators exhibited good stability over a range of temperatures up to 325 K. N_A, D_{IT} and V_{FB} were all found to remain fairly constant. Shifts to more positive biases and increased hysteresis were observed at temperatures above 325 K. In contrast it was found that when the P3HT layer was applied and cured under an inert atmosphere, the stability of the device improved, with only a minimal change in V_{FB} and slightly increased hysteresis at elevated temperatures. This implies that despite undergoing several annealing cycles atmospheric dopants were still present in devices fabricated under ambient conditions. The density of interface states was lowest in the PSQ and SU8 devices prepared in air, $\sim 10^{10}$ cm^{-2} eV^{-1} compared to $\sim 10^{11}$ cm^{-2} eV^{-1} for devices prepared under nitrogen. However in the devices prepared in nitrogen the interface states had lower energy suggesting that in these devices the probed states were closer to the valence band.

Bulk mobility and conductance were extracted from the M-W peak frequencies of the devices when biased at flatband. This was to avoid the possible effects of charge injection under accumulation voltages. Both devices fabricated in air revealed deviations from an Arrhenius dependency at low temperatures, although the device fabricated under nitrogen revealed a much stronger Arrhenius dependency. All three deviated from a $1/T^2$ dependency.

Photo-capacitance measurements revealed useful responses of the MIS capacitors to wavelengths in the visible region of the spectrum. Shifts of V_{FB} to more positive voltages and increased minimum capacitance resulted from irradiation of monochromatic light at wavelengths between 400 nm and 700 nm. C-V measurements obtained in the dark after illumination revealed slow relaxation of trapped charges from both the PSQ and SU8 devices. Relaxation times were much longer in the SU8 devices, taking over a week to relax back to its initial dark state. Charge retention times in these SU8 devices were comparable to those seen in organic memory devices. Relaxation of trapped charges in the PSQ device was considerably quicker, taking approximately 5 hours for V_{FB} to attain its prior dark value. The increased flatband voltage was caused by photo-generated electrons trapped either at the semiconductor/insulator interface or in the insulator. Further positive increases in gate bias are shielded from the semiconductor by the trapped electrons. Charge neutrality is maintained at the same level of band bending; the depletion region width remains constant resulting in an increased minimum capacitance compared to its value in the dark.

Further evidence of the slow detrapping process in the MIS capacitors was found in the constant capacitance experiments. These measurements recorded the change in voltage necessary to maintain a constant capacitance while the capacitors are subjected to pulses of light for 60 s followed by a period in the dark. The increases during illumination and decreases in the dark of the voltage were fitted with two and three-term exponential functions. Decay curves were also found to follow Kohlrausch's law, which describes relaxation processes in disordered systems. Interestingly the characteristic time constants for the relaxation in SU8 devices decreased with wavelength. This led to a further experiment in which the SU8 device performed like a memory device where charges were stored during irradiation with 500 nm light and erased by irradiation with 300 nm light. It was thought that the reduction in trapped charges was related to the observed dependency of V_{FB} on UV dosage of the SU8 during fabrication.

The responsivity of MIS capacitors during a C-V measurement was found to be dependent on wavelength, incident light intensity and bias scan rate. The response at different wavelengths was found to increase with photon energy. However the

MIS devices were more sensitive to lower intensities of light. The response tended to saturate at higher intensities, possibly due to higher recombination rates. Slower scan rates resulted in increased minimum capacitance and hysteresis; the C-V measurement takes a longer time and more photons are absorbed during the experiment, which is equivalent to increasing the light intensity.

Despite the extent of electron trapping in the MIS capacitors, transfer of photogenerated electrons between adjacent capacitors was demonstrated using a CCD-like structure: a charge injection device (CID). C-V measurements showed electrons had been transferred to the 'dark' device when its gate voltage exceeded that applied to the irradiated device. Transfer of charges was confirmed by a measurement of displacement currents during illumination of the CID structure. The ratio of the increase in hysteresis between CID-1 and CID-2 during C-V measurements was 0.76. This corresponded to the ratio of 0.66 for the displacement currents in CID-1 and CID-2.

Simulations of the photo-C-V response of MIS capacitors showed similar behaviour to the experimental results, with increased minimum capacitance and hysteresis shown to be dependent on wavelength, intensity and bias scan rate. The results indicated that the basic model is correct.

Successful implementation of an organic photovoltaic cell, as a near-field detector, for an SPR bio-sensor was achieved. Concurrent measurements of the reflectivity and photocurrent from the OPV demonstrated that the OPV is capable of producing photocurrent from surface plasmon resonance. Binding events at the sensor surface were shown to modulate the OPV current.

7.2 Further Work

The dependence of V_{FB} on the degree of polymerization of the SU8 layer could be further investigated and exploited to produce OFETs with controllable threshold voltages. Such devices could be used as pre-programmed memory for example.

Further studies on the transient response of MIS capacitors could be undertaken over a range of temperatures. An Arrhenius plot of the time constants will show whether the relaxation times are thermally activated; both the activation energy and attempt to escape frequency could then be determined from Equation 5.3.

The demonstration of charge transfer certainly needs further investigation. Using low-k dielectrics such as benzocyclobutene (BCB), CYTOP® or PTFE-AF® should result in less disorder at the semiconductor surface. This should reduce trapping effects and improve the effective mobility of electrons between adjacent capacitors. Other solution based semiconductors, for example poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT), should be considered due to their improved structural order and higher mobility. The varied optical properties of different organic semiconductors can also be used to provide sensors which respond to different, or more specific, regions of the electromagnetic spectrum. Following on from improving the transfer of charge between capacitors, the device structure could be expanded to produce an array of CCD cells.

If an optimal combination of organic insulator and semiconductor are found, simple MIS arrays can be fabricated for x-y addressable light sensing or imaging applications.

The basic model for the photo–C-V requires further development to include effects such as recombination, de-trapping of carriers and the presence of free electrons in the semiconductor.

Further integration of the SPR biosensor should include the incorporation of a light source such as a microcavity OLED to provide a fully integrated low-cost thin-film device. Improvements in sensitivity could be achieved by improving the aqueous functionalization of the gold surface and reducing its surface roughness. Replacing the gold film with a bi-metallic silver/gold layer could also enhance the performance of the sensor.

Publications

M. Bora, K. Celebi, J. Zuniga, C. Watson, K. M. Milaninia and M. A. Baldo, "Near field detector for integrated surface plasmon resonance biosensor applications," *Optics Express*, vol. 17, pp. 329–336, 2009.

M. M. Ibrahim, A. C. Maciel, C. P. Watson, M-B. Madec, S. G. Yeates and D. M. Taylor, "Thermo-mechanical stabilisation of a crystalline organic semiconductor for robust large area electronics", *Organic Electronics*, vol. 11, iss. 7, pp. 1234–1241, 2010.

Conferences

"Electron trapping at the interfacial boundary in organic MIS diodes", C. P. Watson and D. M. Taylor, International Conference on Organic Electronics, Liverpool, UK, June 15–17, 2009.

"Organic Photo-detector for Integrated Surface Plasmon Resonance Biosensors", C. P. Watson, M. Bora, K. Celebi, J. Zuniga, K. Milaninia and M. Baldo, Symposium N, International Conference on Materials for Advanced Technologies, Singapore, June 28 - 3 July, 2009.

"Admittance Measurements on Polymeric MIS Structures", C. P. Watson and D. M. Taylor, Early Career Research in Electrostatics and Dielectrics, Institute of Physics, London, December 15, 2009.

"Stable Organic MIS Devices", C. P. Watson, J. Giacometti and D. M. Taylor, International Conference on Organic Electronics, Paris, June 22–25, 2010.

Bibliography

[1] S. R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," *Nature*, vol. 428, pp. 911–918, Apr. 2004.

[2] K. E. Lilja, T. G. Bcklund, D. Lupo, T. Hassinen, and T. Joutsenoja, "Gravure printed organic rectifying diodes operating at high frequencies," *Organic Electronics*, vol. 10, pp. 1011–1014, Aug. 2009.

[3] F. C. Krebs, T. Tromholt, and M. Jrgensen, "Upscaling of polymer solar cell fabrication using full roll-to-roll processing," *Nanoscale*, vol. 2, no. 6, p. 873, 2010.

[4] G. Horowitz, "Organic Field-Effect transistors," *Advanced Materials*, vol. 10, no. 5, pp. 365–377, 1998.

[5] H. Sirringhaus, "Device physics of Solution-Processed organic Field-Effect transistors," *Advanced Materials*, vol. 17, pp. 2411–2425, Oct. 2005.

[6] W. Wang, J. Shi, and D. Ma, "Organic Thin-Film transistor memory with nanoparticle floating gate," *Electron Devices, IEEE Transactions on*, vol. 56, pp. 1036–1039, May 2009.

[7] M. F. Mabrook, Y. Yun, C. Pearson, D. A. Zeze, and M. C. Petty, "Charge storage in Pentacene/Polymethylmethacrylate memory devices," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 632–634, 2009.

[8] H. Al-Dmour, D. M. Taylor, and J. A. Cambridge, "Effect of nanocrystalline-tio 2 morphology on the performance of polymer heterojunction solar cells," *Journal of Physics D: Applied Physics*, vol. 40, no. 17, p. 5034, 2007.

[9] P. Peumans, A. Yakimov, and S. R. Forrest, "Small molecular weight organic thin-film photodetectors and solar cells," *Journal of Applied Physics*, vol. 93, no. 7, p. 3693, 2003.

[10] L. Wang, D. Fine, D. Sharma, L. Torsi, and A. Dodabalapur, "Nanoscale organic and polymeric field-effect transistors as chemical sensors," *Analytical and Bioanalytical Chemistry*, vol. 384, pp. 310–321, Nov. 2005.

[11] T. Someya, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *Proceedings of the National Academy of Sciences*, vol. 101, pp. 9966–9970, June 2004.

[12] I. Manunza, A. Sulis, and A. Bonfiglio, "Pressure sensing by flexible, organic, field effect transistors," *Applied Physics Letters*, vol. 89, no. 14, p. 143502, 2006.

[13] C. W. Tang and S. A. VanSlyke, "Organic electroluminescent diodes," *Applied Physics Letters*, vol. 51, no. 12, p. 913, 1987.

[14] R. So-eul and M.-F. Han, ""Samsung mobile unit sees 2010 recovery"." http://www.reuters.com/article/2009/05/20/us-summit-samsungmobile-idUSTRE54J10H20090520[Accessed: 07-Jun-2010].

[15] "XEL-1 (XEL1, XEL1BU): Overview: TV & home cinema: Sony." http://www.sony.co.uk/product/tv-28-11-oled/XEL-1[Accessed: 20-Nov-2009].

[16] V. Bulovic, R. Deshpande, M. E. Thompson, and S. R. Forrest, "Tuning the color emission of thin film molecular organic light emitting devices by the solid state solvation effect," *Chemical Physics Letters*, vol. 308, pp. 317–322, July 1999.

[17] F. Gutmann and L. Lyons, *Organic Semiconductors.* Wiley series on the science and technology of materials., New York: Wiley & Sons, 1967.

[18] C. K. Chiang, C. R. Fincher, Y. W. Park, A. J. Heeger, H. Shirakawa, E. J. Louis, S. C. Gau, and A. G. MacDiarmid, "Electrical conductivity in doped polyacetylene," *Physical Review Letters*, vol. 39, p. 1098, Oct. 1977.

[19] C. K. Chiang, S. C. Gau, C. R. Fincher, Y. W. Park, A. G. MacDiarmid, and A. J. Heeger, "Polyacetylene, (CH)x: n-type and p-type doping and compensation," *Applied Physics Letters*, vol. 33, no. 1, p. 18, 1978.

[20] F. Ebisawa, T. Kurokawa, and S. Nara, "Electrical properties of polyacetylene/polysiloxane interface," *Journal of Applied Physics*, vol. 54, no. 6, p. 3255, 1983.

[21] A. Tsumura, H. Koezuka, and T. Ando, "Macromolecular electronic device: Field-effect transistor with a polythiophene thin film," *Applied Physics Letters*, vol. 49, no. 18, p. 1210, 1986.

[22] G. Horowitz, D. Fichou, X. Peng, Z. Xu, and F. Garnier, "A field-effect transistor based on conjugated alpha-sexithienyl," *Solid State Communications*, vol. 72, pp. 381–384, Oct. 1989.

[23] M. Madru, G. Guillaud, M. A. Sadoun, M. Maitrot, C. Clarisse, M. L. Contellec, J. J. Andr, and J. Simon, "The first field effect transistor based on an intrinsic molecular semiconductor," *Chemical Physics Letters*, vol. 142, pp. 103–105, Dec. 1987.

[24] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "High-mobility polymer gate dielectric pentacene thin film transistors," *Journal of Applied Physics*, vol. 92, no. 9, p. 5259, 2002.

[25] E. A. Schiff, "Drift-mobility measurements and mobility edges in disordered silicons," *Journal of Physics: Condensed Matter*, vol. 16, pp. S5265–S5275, Nov. 2004.

[26] A. R. Brown, A. Pomp, C. M. Hart, and D. M. de Leeuw, "Logic gates made from polymer transistors and their use in ring oscillators," *Science*, vol. 270, pp. 972 –974, Nov. 1995.

[27] M. Matters, D. de Leeuw, M. Vissenberg, C. Hart, P. Herwig, T. Geuns, C. Mutsaers, and C. Drury, "Organic field-effect transistors and all-polymer integrated circuits," *Optical Materials*, vol. 12, pp. 189–197, June 1999.

[28] G. H. Gelinck, T. C. T. Geuns, and D. M. de Leeuw, "High-performance all-polymer integrated circuits," *Applied Physics Letters*, vol. 77, no. 10, p. 1487, 2000.

[29] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming, "C60 thin film transistors," *Applied Physics Letters*, vol. 67, no. 1, p. 121, 1995.

[30] A. Dodabalapur, J. Laquindanum, H. E. Katz, and Z. Bao, "Complementary circuits with organic transistors," *Applied Physics Letters*, vol. 69, no. 27, p. 4227, 1996.

[31] Y. Lin, A. Dodabalapur, R. Sarpeshkar, Z. Bao, W. Li, K. Baldwin, V. R. Raju, and H. E. Katz, "Organic complementary ring oscillators," *Applied Physics Letters*, vol. 74, no. 18, p. 2714, 1999.

[32] B. Crone, A. Dodabalapur, Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, "Large-scale complementary integrated circuits based on organic transistors," *Nature*, vol. 403, pp. 521–523, Feb. 2000.

[33] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, pp. 745–748, Feb. 2007.

[34] L. Chua, J. Zaumseil, J. Chang, E. C. Ou, P. K. Ho, H. Sirringhaus, and R. H. Friend, "General observation of n-type field-effect behaviour in organic semiconductors," *Nature*, vol. 434, pp. 194–199, Mar. 2005.

[35] T. B. Singh, P. Senkarabacak, N. S. Sariciftci, A. Tanda, C. Lackner, R. Hagelauer, and G. Horowitz, "Organic inverter circuits employing ambipolar pentacene field-effect transistors," *Applied Physics Letters*, vol. 89, no. 3, p. 033512, 2006.

[36] E. J. Meijer, D. M. De Leeuw, S. Setayesh, E. V. Veenendaal, B. H. Huisman, P. W. M. Blom, J. C. Hummelen, U. Scherf, and T. M. Klapwijk, "Solution-processed ambipolar organic field-effect transistors and inverters," *Nature Materials*, vol. 2, pp. 678–682, Sept. 2003.

[37] H. Wang, J. Wang, X. Yan, J. Shi, H. Tian, Y. Geng, and D. Yan, "Ambipolar organic field-effect transistors with air stability, high mobility, and balanced transport," *Applied Physics Letters*, vol. 88, no. 13, p. 133508, 2006.

[38] M. Jaiswal and R. Menon, "Polymer electronic materials: a review of charge transport," *Polymer International*, vol. 55, pp. 1371–1384, Dec. 2006.

[39] G. Malliaras and R. Friend, "An organic electronics primer," *Physics Today*, vol. 58, no. 5, p. 53, 2005.

[40] S. M. Sze and K. K. Ng, *Physics of semiconductor devices.* Wiley-Blackwell, 2007.

[41] M. C. J. M. Vissenberg, *Opto-electronic properties of disordered organic semiconductors.* PhD thesis, Leiden University, 1999.

[42] C. W. Tang, "Two-layer organic photovoltaic cell," *Applied Physics Letters*, vol. 48, no. 2, p. 183, 1986.

[43] T. Kietzke, "Recent advances in organic solar cells," *Advances in OptoElectronics*, p. 40285, 2007.

[44] H. Chen, J. Hou, S. Zhang, Y. Liang, G. Yang, Y. Yang, L. Yu, Y. Wu, and G. Li, "Polymer solar cells with enhanced open-circuit voltage and efficiency," *Nat Photon*, vol. 3, pp. 649–653, Nov. 2009.

[45] J. Y. Kim, K. Lee, N. E. Coates, D. Moses, T. Nguyen, M. Dante, and A. J. Heeger, "Efficient tandem polymer solar cells fabricated by All-Solution processing," *Science*, vol. 317, pp. 222 –225, July 2007.

[46] J. J. M. Halls, C. A. Walsh, N. Greenham, E. A. Marseglia, R. Friend, S. C. Moratti, and A. Holmes, "Efficient photodiodes from interpenetrating polymer networks," *Nature*, vol. 376, pp. 498–500, Aug. 1995.

[47] A. J. Moulé, J. B. Bonekamp, and K. Meerholz, "The effect of active layer thickness and composition on the performance of bulk-heterojunction solar cells," *Journal of Applied Physics*, vol. 100, no. 9, p. 094503, 2006.

[48] T. N. Ng, W. S. Wong, M. L. Chabinyc, S. Sambandan, and R. A. Street, "Flexible image sensor array with bulk heterojunction organic photodiode," *Applied Physics Letters*, vol. 92, no. 21, p. 213303, 2008.

[49] J. Blakesley, P. Keivanidis, M. Campoy-Quiles, C. Newman, Y. Jin, R. Speller, H. Sirringhaus, N. Greenham, J. Nelson, and P. Stavrinou, "Organic semiconductor devices for x-ray imaging," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 580, pp. 774–777, Sept. 2007.

[50] I. Nausieda, K. Ryu, I. Kymissis, A. Ibitayo (Tayo) Akinwande, V. Bulovi, and C. G. Sodini, "An organic Active-Matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, pp. 527–532, Feb. 2008.

[51] T. Someya, Y. Kato, S. Iba, Y. Noguchi, T. Sekitani, H. Kawaguchi, and T. Sakurai, "Integration of organic FETs with organic photodiodes for a large area, flexible, and lightweight sheet image scanners," *IEEE Transactions on Electron Devices*, vol. 52, pp. 2502–2511, Nov. 2005.

[52] K. S. Narayan and N. Kumar, "Light responsive polymer field-effect transistor," *Applied Physics Letters*, vol. 79, no. 12, p. 1891, 2001.

[53] F. Yakuphanoglu and W. A. Farooq, "Flexible pentacene organic field-effect phototransistor," *Synthetic Metals*, vol. 161, pp. 379–383, Mar. 2011.

[54] M. Y. Cho, S. J. Kim, Y. D. Han, D. H. Park, K. H. Kim, D. H. Choi, and J. Joo, "Highly sensitive, photocontrolled, organic Thin-Film transistors using soluble star-shaped conjugated molecules," *Advanced Functional Materials*, vol. 18, pp. 2905–2912, Oct. 2008.

[55] S. Dutta, T. B. Singh, and K. S. Narayan, "Photoinduced relaxation effects in three-terminal polymer based device structures," *Synthetic Metals*, vol. 139, pp. 553–556, Oct. 2003.

[56] T. P. I. Saragi, R. Pudzich, T. Fuhrmann, and J. Salbeck, "Organic phototransistor based on intramolecular charge transfer in a bifunctional spiro compound," *Applied Physics Letters*, vol. 84, no. 13, p. 2334, 2004.

[57] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, "Bias stress in organic thin-film transistors and logic gates," *Applied Physics Letters*, vol. 79, no. 8, p. 1124, 2001.

[58] H. Sirringhaus, "Reliability of organic Field-Effect transistors," *Advanced Materials*, vol. 21, no. 38–39, pp. 3859–3873, 2009.

[59] G. Dicker, M. P. de Haas, D. M. de Leeuw, and L. D. Siebbeles, "Origin of the stretched-exponential hole relaxation in regioregular poly(3-hexylthiophene)," *Chemical Physics Letters*, vol. 402, pp. 370–374, Feb. 2005.

[60] J. Veres, S. Ogier, S. Leeming, D. Cupertino, and S. M. Khaffaf, "Low-k insulators as the choice of dielectrics in organic Field-Effect transistors," *Advanced Functional Materials*, vol. 13, pp. 199–204, Mar. 2003.

[61] Fernandez, Taylor, Drysdale, and Ellis, "Photogenerated minority carrier trapping and inversion layer formation in polymer field-effect structures," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 13, no. 5, pp. 1093–1100, 2006.

[62] J. Lancaster, D. M. Taylor, P. Sayers, and H. L. Gomes, "Voltage- and light-induced hysteresis effects at the high-k dielectric-poly(3-hexylthiophene) interface," *Applied Physics Letters*, vol. 90, no. 10, p. 103513, 2007.

[63] W. S. Boyle and G. E. Smith, "Charge coupled semiconductor devices," *Bell Systems Technical Journal*, vol. 49, no. 4, pp. 593–600, 1970.

[64] E. H. Nicollian and J. R. Brews, *MOS Metal Oxide Semiconductor Physics and Technology*. New York: Wiley, 1982.

[65] K. N. Kwok, *Complete Guide to Semiconductor Devices*. New York: McGraw-Hill, international ed., 1995.

[66] N. Karl, "Charge carrier transport in organic semiconductors," *Synthetic Metals*, vol. 133-134, pp. 649–657, Mar. 2003.

[67] H. Bässler, "Charge transport in disordered organic photoconductors a monte carlo simulation study," *physica status solidi (b)*, vol. 175, no. 1, pp. 15–56, 1993.

[68] M. Vissenberg and M. Matters, "Theory of the field-effect mobility in amorphous organic transistors," *Physical Review B*, vol. 57, pp. 12964–12967, MAY 15 1998.

[69] W. Brütting, "Introduction to the physics of organic semiconductors," in *Physics of Organic Semiconductors* (W. Brütting, ed.), pp. 1–14, Weinheim, FRG: Wiley-VCH Verlag GmbH & Co., May 2005.

[70] H. Ishii, N. Hayashi, E. Ito, Y. Washizu, K. Sugi, Y. Kimura, M. Niwano, Y. Ouchi, and K. Seki, "Kelvin probe study of band bending at organic semiconductor/metal interfaces: examination of Fermi level alignment," *physica status solidi (a)*, vol. 201, pp. 1075–1094, May 2004.

[71] S. Scheinert and G. Paasch, "Fabrication and analysis of polymer field-effect transistors," *physica status solidi (a)*, vol. 201, pp. 1263–1301, May 2004.

[72] T. Lindner and G. Paasch, "Inversion layer formation in organic field-effect devices," *Journal of Applied Physics*, vol. 102, no. 5, p. 054514, 2007.

[73] E. J. Meijer, A. V. G. Mangnus, C. M. Hart, D. M. de Leeuw, and T. M. Klapwijk, "Frequency behavior and the Mott–Schottky analysis in poly(3-hexyl thiophene) metal–insulator–semiconductor diodes," *Applied Physics Letters*, vol. 78, pp. 3902–3904, June 2001.

[74] D. M. Taylor and N. Alves, "Separating interface state response from parasitic effects in conductance measurements on organic metal-insulator-semiconductor capacitors," *Journal of Applied Physics*, vol. 103, no. 5, p. 054509, 2008.

[75] I. Torres and D. M. Taylor, "Interface states in polymer metal-insulator-semiconductor devices," *Journal of Applied Physics*, vol. 98, no. 7, p. 073710, 2005.

[76] A. von Hippel, *Dielectrics and Waves.* Wiley, New York, 1954.

[77] K. S. Cole and R. H. Cole, "Dispersion and absorption in dielectrics i. alternating current characteristics," *The Journal of Chemical Physics*, vol. 9, no. 4, p. 341, 1941.

[78] I. Torres, *Interfacial Effects in Polymer MIS Devices.* PhD thesis, University of Wales, Bangor, 2004.

[79] S. Scheinert and W. Schliefke, "Analyzes of field effect devices based on poly(3-octylthiophene)," *Synthetic Metals*, vol. 139, pp. 501–509, Sept. 2003.

[80] S. Grecu, M. Bronner, A. Opitz, and W. Brutting, "Characterization of polymeric metal-insulator-semiconductor diodes," *Synthetic Metals*, vol. 146, no. 3, pp. 359–363, 2004.

[81] M. Lada, "Correlation between the glass-rubber transition and ionic conductivity in poly(3-hexylthiophene)," *Applied Physics Letters*, vol. 93, no. 14, p. 143308, 2008.

[82] H. Gomes, P. Stallinga, M. Cölle, F. Biscarini, and D. de Leeuw, "The effect of water related traps on the reliability of organic based transistors," *Journal of Non-Crystalline Solids*, vol. 352, pp. 1761–1764, June 2006.

[83] E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B. Huisman, D. M. de Leeuw, and T. M. Klapwijk, "Switch-on voltage in disordered organic field-effect transistors," *Applied Physics Letters*, vol. 80, no. 20, p. 3838, 2002.

[84] M. Yun, S. Gangopadhyay, M. Bai, H. Taub, M. Arif, and S. Guha, "Interface states in polyfluorene-based metal-insulator-semiconductor devices," *Organic Electronics*, vol. 8, pp. 591–600, Oct. 2007.

[85] K. Baeg, Y. Noh, H. Sirringhaus, and D. Kim, "Controllable shifts in threshold voltage of Top-Gate polymer Field-Effect transistors for applications in organic nano floating gate memory," *Advanced Functional Materials*, vol. 20, pp. 224–230, Jan. 2010.

[86] K. Jung, S. Jin, C. Lee, C. Park, B. Park, H. Shin, and J. Lee, "Effects of peripheral region on cv characteristics of organic mis capacitors," in *Proc Int Disp Workshops*, vol. 2, pp. 1053–1056, 2005.

[87] M. Ullah, D. M. Taylor, R. Schwödiauer, H. Sitter, S. Bauer, N. S. Sariciftci, and T. B. Singh, "Electrical response of highly ordered organic thin film metal-insulator-semiconductor devices," *Journal of Applied Physics*, vol. 106, no. 11, p. 114505, 2009.

[88] E. Itoh, I. Torres, C. Hayden, and D. Taylor, "Excimer-laser micropatterned photobleaching as a means of isolating polymer electronic devices," *Synthetic Metals*, vol. 156, pp. 129–134, Feb. 2006.

[89] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "Patterning pentacene organic thin film transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 3, p. 956, 2002.

[90] J. Lee, J. Kim, B. Ju, J. Kim, M. Oh, and J. Jang, "Electrical properties of shadow-mask patterned organic thin film transistor fabricated on plastic substrate," *Journal of the Korean Physical Society*, vol. 45, pp. S612–S614, DEC 2004. 12th Seoul International Symposium on the Physics of Semiconductors and Applications, Gyungju, South Korea, MAR 14-16, 2004.

[91] K. Baeg, D. Khim, J. Kim, M. Kang, I. You, D. Kim, and Y. Noh, "Improved performance uniformity of inkjet printed n-channel organic

field-effect transistors and complementary inverters," *Organic Electronics*, vol. 12, pp. 634–640, Apr. 2011.

[92] D. Li and L. J. Guo, "Micron-scale organic thin film transistors with conducting polymer electrodes patterned by polymer inking and stamping," *Applied Physics Letters*, vol. 88, no. 6, p. 063513, 2006.

[93] K. M. Brunson, D. Sands, C. B. Thomas, and H. S. Reehal, "The contribution of bulk states to the ac conductance of metal-insulator-semiconductor diodes," *Journal of Applied Physics*, vol. 62, no. 1, p. 185, 1987.

[94] A. Takshi and J. D. Madden, "Study the effect of distribution of density of states on the subthreshold characteristics of an organic field-effect transistor (OFET)," *Journal of Computational Electronics*, Oct. 2010.

[95] S. Scheinert, K. P. Pernstich, B. Batlogg, and G. Paasch, "Determination of trap distributions from current characteristics of pentacene field-effect transistors with surface modified gate oxide," *Journal of Applied Physics*, vol. 102, no. 10, p. 104503, 2007.

[96] S. Scheinert, G. Paasch, M. Schrodner, H. Roth, S. Sensfuß, and T. Doll, "Subthreshold characteristics of field effect transistors based on poly(3-dodecylthiophene) and an organic insulator," *Journal of Applied Physics*, vol. 92, no. 1, p. 330, 2002.

[97] I. Torres, D. M. Taylor, and E. Itoh, "Interface states and depletion-induced threshold voltage instability in organic metal-insulator-semiconductor structures," *Applied Physics Letters*, vol. 85, no. 2, p. 314, 2004.

[98] R. P. Ortiz, A. Facchetti, and T. J. Marks, "High-k organic, inorganic, and hybrid dielectrics for Low-Voltage organic Field-Effect transistors," *Chemical Reviews*, vol. 110, pp. 205–239, Jan. 2010.

[99] K. Shin, S. Y. Yang, C. Yang, H. Jeon, and C. E. Park, "Effects of polar functional groups and roughness topography of polymer gate dielectric layers on pentacene field-effect transistors," *Organic Electronics*, vol. 8, pp. 336–342, Aug. 2007.

[100] J. Simmons and L. Wei, "Theory of dynamic charge current and capacitance characteristics in MIS systems containing distributed surface traps," *Solid-State Electronics*, vol. 16, pp. 53–66, Jan. 1973.

[101] J. Simmons and L. Wei, "Theory of dynamic charge and capacitance characteristics in MIS systems containing discrete surface traps," *Solid-State Electronics*, vol. 16, pp. 43–52, Jan. 1973.

[102] E. H. Nicollian and A. Goetzberger, "The Si-SiO$_2$ interface-electrical properties as deterimed by the metal-insulator-silicon conductance technique.," *Bell Systems Technical Journal*, vol. 46, p. 1055, 1967.

[103] M. Çakar, A. Türüt, and Y. Onganer, "The conductance- and Capacitance-Frequency characteristics of the rectifying junctions formed by sublimation of organic Pyronine-B on p-Type silicon," *Journal of Solid State Chemistry*, vol. 168, pp. 169–174, Oct. 2002.

[104] P. Stallinga, H. L. Gomes, M. Murgia, and K. Müllen, "Interface state mapping in a schottky barrier of the organic semiconductor terrylene," *Organic Electronics*, vol. 3, pp. 43–51, Mar. 2002.

[105] N. Alves and D. M. Taylor, "Determining the interfacial density of states in metal-insulator-semiconductor devices based on poly(3-hexylthiophene)," *Applied Physics Letters*, vol. 92, no. 10, p. 103312, 2008.

[106] W. Hill and C. Coleman, "A single-frequency approximation for interface-state density determination," *Solid-State Electronics*, vol. 23, pp. 987–993, Sept. 1980.

[107] J. Singh and R. Srivastava, "Comment on hill and coleman's single high frequency approximation for interface state density determination," *Solid-State Electronics*, vol. 25, pp. 967–968, Sept. 1982.

[108] H. Preier, "Contributions of surface states to MOS impedance," *Applied Physics Letters*, vol. 10, no. 12, pp. 361–363, 1967.

[109] F. Heiman and G. Warfield, "The effects of oxide traps on the MOS capacitance," *IEEE Transactions on Electron Devices*, vol. 12, pp. 167–178, Apr. 1965.

[110] T. C. Poon and H. C. Card, "Admittance measurements of Si-SiO2 interface states under optical illumination," *Journal of Applied Physics*, vol. 51, no. 11, p. 5880, 1980.

[111] J. Tan, M. K. Das, J. A. Cooper, and M. R. Melloch, "Metal–oxide–semiconductor capacitors formed by oxidation of polycrystalline silicon on SiC," *Applied Physics Letters*, vol. 70, no. 17, p. 2280, 1997.

[112] Y. Q. Wu, T. Shen, P. D. Ye, and G. D. Wilk, "Photo-assisted capacitance-voltage characterization of high-quality atomic-layer-deposited Al_2O_3/GaN metal-oxide-semiconductor structures," *Applied Physics Letters*, vol. 90, no. 14, p. 143504, 2007.

[113] T. Hashizume, E. Alekseev, D. Pavlidis, K. S. Boutros, and J. Redwing, "Capacitance–voltage characterization of AlN/GaN metal–insulator–semiconductor structures grown on sapphire substrate by metalorganic chemical vapor deposition," *Journal of Applied Physics*, vol. 88, no. 4, p. 1983, 2000.

[114] D. M. Taylor, J. A. Drysdale, I. Torres, and O. Fernández, "Electron trapping and inversion layer formation in photoexcited metal-insulator-poly(3-hexylthiophene) capacitors," *Applied Physics Letters*, vol. 89, no. 18, p. 183512, 2006.

[115] R. Pierret and C. Sah, "Quantitative analysis of the effects of steady-state illumination on the mos-capacitor," *Solid-State Electronics*, vol. 13, pp. 289–302, 1970.

[116] D. F. Barbe, "Imaging devices using the charge-coupled concept," *Proceedings of the IEEE*, vol. 63, no. 1, pp. 38–67, 1975.

[117] H. Michon and G. Burke, "Charge injection imaging," in *Solid-State Circuits Conference. Digest of Technical Papers. 1973 IEEE International*, vol. 16, p. 138139, IEEE, 1973.

[118] G. Burke and H. Michon, "Charge-injection imaging: Operating techniques and performances characteristics.," *Electron Devices, IEEE Transactions on*, vol. 23, no. 2, p. 189196, 1976.

[119] G. Yu, J. Wang, J. McElvain, and A. J. Heeger, "Large-area, full-color image sensors made with semiconducting polymers," *Advanced Materials*, vol. 10, no. 17, pp. 1431–1434, 1998.

[120] T. Someya, Y. Kato, S. Iba, Y. Noguchi, T. Sekitani, H. Kawaguchi, and T. Sakurai, "Integration of organic fets with organic photodiodes for a large area, flexible, and lightweight sheet image scanners," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 2502 – 2511, nov. 2005.

[121] S. Huang, *Development and design of polymer circuits based on polymer thin-film transistors*. PhD thesis, University of Liverpool, 2006.

[122] J. Wilson and J. Hawkes, *Optoelectronics*. Prentice Hall, third ed., 1998.

[123] T. Yamamoto, K. Sanechika, and A. Yamamoto, "Preparation of thermostable and electric-conducting poly(2,5-thienylene)," *Journal of Polymer Science: Polymer Letters Edition*, vol. 18, no. 1, pp. 9–12, 1980.

[124] J. W. Lin and L. P. Dudek, "Synthesis and properties of poly(2,5-thienylene)," *Journal of Polymer Science: Polymer Chemistry Edition*, vol. 18, no. 9, pp. 2869–2873, 1980.

[125] R. Elsenbaumer, K. Jen, and R. Oboodi, "Processible and environmentally stable conducting polymers," *Synthetic Metals*, vol. 15, no. 2-3, pp. 169 – 174, 1986. Proceedings of the Workshop on Conductive Polymers.

[126] A. Assadi, C. Svensson, M. Willander, and O. Inganäs, "Field-effect mobility of poly(3-hexylthiophene)," *Applied Physics Letters*, vol. 53, no. 3, p. 195, 1988.

[127] P. Barta, F. Cacialli, R. H. Friend, and M. Zagrska, "Efficient photo and electroluminescence of regioregular poly(alkylthiophene)s," vol. 84, no. 11, pp. 6279–6284, 1998.

[128] T. A. Chen and R. D. Rieke, "The first regioregular head-to-tail poly(3-hexylthiophene-2,5-diyl) and a regiorandom isopolymer: nickel versus palladium catalysis of 2(5)-bromo-5(2)-(bromozincio)-3-hexylthiophene polymerization," *Journal of the American Chemical Society*, vol. 114, pp. 10087–10088, Dec. 1992.

[129] R. M^{c}Culloch and R. Lowe, "Enhanced electrical-conductivity in regioselectively synthesized poly(3–alkylthiophenes)," *Journal of the Chemical Society-Chemical Communications*, pp. 70–72, JAN 1 1992.

[130] Z. Bao, A. Dodabalapur, and A. J. Lovinger, "Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility," *Applied Physics Letters*, vol. 69, no. 26, p. 4108, 1996.

[131] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, and D. M. de Leeuw, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, no. 6754, pp. 685–688, 1999.

[132] C. Dimitrakopoulos and P. Malenfant, "Organic thin film transistors for large area electronics," *Advanced Materials*, vol. 14, no. 2, pp. 99–117, 2002.

[133] H. Sirringhaus, N. Tessler, and R. Friend, "Integrated, high-mobility polymer field-effect transistors driving polymer light-emitting diodes," *Synthetic Metals*, vol. 102, pp. 857–860, June 1999.

[134] K. Kaneto and W. Takashima, "Fabrication and characteristics of schottky diodes based on regioregular poly(3-hexylthiophene)/Al junction," *Current Applied Physics*, vol. 1, no. 4-5, pp. 355 – 361, 2001.

[135] L. Bürgi, R. Pfeiffer, M. Mücklich, P. Metzler, M. Kiy, and C. Winnewisser, "Optical proximity and touch sensors based on monolithically integrated polymer photodiodes and polymer LEDs," *Organic Electronics*, vol. 7, pp. 114–120, Apr. 2006.

[136] J. Zaumseil and H. Sirringhaus, "Electron and ambipolar transport in organic Field-Effect transistors," *Chemical Reviews*, vol. 107, pp. 1296–1323, Apr. 2007.

[137] G. Wang, J. Swensen, D. Moses, and A. J. Heeger, "Increased mobility from regioregular poly(3-hexylthiophene) field-effect transistors," *Journal of Applied Physics*, vol. 93, no. 10, p. 6137, 2003.

[138] K. Baeg, D. Khim, D. Kim, J. B. Koo, I. You, W. S. Choi, and Y. Noh, "High mobility top-gated poly(3-hexylthiophene) field-effect transistors with high

work-function pt electrodes," *Thin Solid Films*, vol. 518, pp. 4024–4029, May 2010.

[139] "SU-8: Thick Photo-Resist for MEMS." http://memscyclopedia.org/su8.html.

[140] E. Menard, R. G. Nuzzo, and J. A. Rogers, "Bendable single crystal silicon thin film transistors formed by printing on plastic substrates," *Applied Physics Letters*, vol. 86, no. 9, p. 093507, 2005.

[141] F. Yildirim, R. Schliewe, W. Bauhofer, R. Meixner, H. Goebel, and W. Krautschneider, "Gate insulators and interface effects in organic thin-film transistors," *Organic Electronics*, vol. 9, pp. 70–76, Feb. 2008.

[142] M. K. Gunde, N. Hauptman, M. Maček, and M. Kunaver, "The influence of hard-baking temperature applied for SU8 sensor layer on the sensitivity of capacitive chemical sensor," *Applied Physics A: Materials Science & Processing*, vol. 95, pp. 673–680, June 2009.

[143] R. H. Baney, M. Itoh, A. Sakakibara, and T. Suzuki, "Silsesquioxanes," *Chemical Reviews*, vol. 95, no. 5, pp. 1409–1430, 1995.

[144] Z. Bao, V. Kuck, J. Rogers, and M. Paczkowski, "Silsesquioxane resins as High-Performance solution processible dielectric materials for organic transistor applications," *Advanced Functional Materials*, vol. 12, no. 8, pp. 526–531, 2002.

[145] "IEEE standard for test methods for the characterization of organic transistors and materials," *IEEE Std 1620-2008*, pp. 1 –14, dec. 2008.

[146] G. Goto, "Determination of deep-level energy and density profiles in inhomogeneous semiconductors," *Applied Physics Letters*, vol. 23, no. 3, p. 150, 1973.

[147] N. M. Johnson, D. J. Bartelink, R. B. Gold, and J. F. Gibbons, "Constant-capacitance DLTS measurement of defect-density profiles in semiconductors," *Journal of Applied Physics*, vol. 50, no. 7, p. 4828, 1979.

[148] Y. Oyama, J. ichi Nishizawa, and K. Dezaki, "Deep levels in te-doped GaAs prepared by annealing under controlled arsenic vapor pressure," *Journal of Applied Physics*, vol. 70, no. 2, p. 833, 1991.

[149] S. Hoshino, "Influence of moisture on device characteristics of polythiophene-based field-effect transistors," *Journal of Applied Physics*, vol. 95, no. 9, p. 5088, 2004.

[150] Y. Liu, L. Wu, P. T. Lai, and Q. Zuo, "Air-stability analysis and improvement of poly(3-hexylthiophene) field-effect transistors," *Semiconductor Science and Technology*, vol. 24, no. 9, p. 095013, 2009.

[151] M. R. Baklanov and K. Maex, "Porous low dielectric constant materials for microelectronics," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 364, pp. 201 –215, Jan. 2006.

[152] J. Xu and C. Wong, "Photodefinable high-k su8 nanocomposite for embedded capacitors," in *Advanced Packaging Materials: Processes, Properties and Interface, 200611th International Symposium on*, pp. 133–138, 2006.

[153] D. Chirvase, Z. Chiguvare, M. Knipper, J. Parisi, V. Dyakonov, and J. C. Hummelen, "Electrical and optical design and characterisation of regioregular poly(3-hexylthiophene-2,5diyl)/fullerene-based heterojunction polymer solar cells," *Synthetic Metals*, vol. 138, no. 1-2, pp. 299 – 304, 2003. Organic Materials for Device Applications. Proceedings of Symposium F, E-MRS Spring Meeting 2002, June 18-21, 2002, Strasbourg, France.

[154] S. Grecu, M. Roggenbuck, A. Opitz, and W. Brtting, "Differences of interface and bulk transport properties in polymer field-effect devices," *Organic Electronics*, vol. 7, no. 5, pp. 276 – 286, 2006.

[155] T. Sikanen, S. Tuomikoski, R. A. Ketola, R. Kostiainen, S. Franssila, and T. Kotiaho, "Characterization of su-8 for electrokinetic microfluidic applications," *Lab on a Chip*, no. 8, p. 888, 2005.

[156] MicroChem, "SU-8 2000, Permanent Epoxy Negative Photoresist." Datasheet, 2010.

[157] M. Egginger, M. Irimia-Vladu, R. Schwödiauer, A. Tanda, I. Frischauf, S. Bauer, and N. S. Sariciftci, "Mobile ionic impurities in poly(vinyl alcohol) gate dielectric: Possible source of the hysteresis in organic Field-Effect transistors," *Advanced Materials*, vol. 20, pp. 1018–1022, Mar. 2008.

[158] H. Peisert, M. Knupfer, T. Schwieger, and J. Fink, "Strong chemical interaction between indium tin oxide and phthalocyanines," *Applied Physics Letters*, vol. 80, no. 16, p. 2916, 2002.

[159] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors," *Journal of Applied Physics*, vol. 87, no. 9, p. 4456, 2000.

[160] V. Coropceanu, J. Cornil, D. A. da Silva Filho, Y. Olivier, R. Silbey, and J. Brédas, "Charge transport in organic semiconductors," *Chemical Reviews*, vol. 107, pp. 926–952, Apr. 2007.

[161] J. A. Letizia, J. Rivnay, A. Facchetti, M. A. Ratner, and T. J. Marks, "Variable temperature mobility analysis of n-Channel, p-Channel, and ambipolar organic Field-Effect transistors," *Advanced Functional Materials*, vol. 20, no. 1, pp. 50–58, 2010.

[162] N. I. Craciun, J. Wildeman, and P. W. M. Blom, "Universal arrhenius temperature activated charge transport in diodes from disordered organic semiconductors," *Physical Review Letters*, vol. 100, p. 056601, Feb. 2008.

[163] N. Mott, *Electronic processes in non-crystalline materials,*. Oxford: Clarendon Press, 1971.

[164] A. J. Mozer and N. S. Sariciftci, "Negative electric field dependence of charge carrier drift mobility in conjugated, semiconducting polymers," *Chemical Physics Letters*, vol. 389, pp. 438–442, May 2004.

[165] E. J. Meijer, A. Mangnus, B. Huisman, G. 't Hooft, D. M. de Leeuw, and T. Klapwijk, "Photoimpedance spectroscopy of poly(3-hexyl thiophene) metal-insulator-semiconductor diodes," *Synthetic Metals*, vol. 142, pp. 53–56, 2004.

[166] C. H. Lee, G. Yu, and A. J. Heeger, "Persistent photoconductivity in poly(p-phenylenevinylene): Spectral response and slow relaxation," *Physical Review B*, vol. 47, p. 15543, June 1993.

[167] D. Kim, H. Kim, and H. Kim, "Photonic high-frequency capacitance-voltage characterization of interface states in metal-oxide-semiconductor capacitors," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 526–528, 2002.

[168] G. Dicker, M. de Haas, L. Siebbeles, and J. Warman, "Electrodeless time-resolved microwave conductivity study of charge-carrier photogeneration in regioregular poly(3-hexylthiophene) thin films," *Physical Review B*, vol. 70, JUL 2004.

[169] Y. Noh, D. Kim, and K. Yase, "Highly sensitive thin-film organic phototransistors: Effect of wavelength of light source on device performance," *Journal of Applied Physics*, vol. 98, no. 7, p. 074505, 2005.

[170] J. Lancaster, *Organic MIS Devices Based on a High-k Dielectric.* PhD thesis, School of Electronics, Bangor University, 2010.

[171] K. Wasapinyokul, W. I. Milne, and D. P. Chu, "Photoresponse and saturation behavior of organic thin film transistors," *Journal of Applied Physics*, vol. 105, no. 2, p. 024509, 2009.

[172] M. Bora, K. Çelebi, J. Zuniga, C. Watson, K. M. Milaninia, and M. A. Baldo, "Near field detector for integrated surface plasmon resonance biosensor applications," *Opt. Express*, vol. 17, pp. 329–336, Jan 2009.

[173] J. Homola, "Surface plasmon resonance sensors for detection of chemical and biological species," *Chemical Reviews*, vol. 108, pp. 462–493, Feb. 2008.

[174] H. Raether, "Surface-plasmons on smooth and rough surfaces and on gratings," *Springer Tracts in Modern Physics*, vol. 111, pp. 1–133, 1988.

[175] J. Homola, S. S. Yee, and G. Gauglitz, "Surface plasmon resonance sensors: review," *Sensors and Actuators B: Chemical*, vol. 54, pp. 3–15, Jan. 1999.

[176] J. K. Mapel, M. Singh, M. A. Baldo, and K. Celebi, "Plasmonic excitation of organic double heterostructure solar cells," *Applied Physics Letters*, vol. 90, no. 12, p. 121102, 2007.

[177] K. Çelebi, T. D. Heidel, and M. A. Baldo, "Simplified calculation of dipole energy transport in a multilayer stack using dyadic green's functions," *Optics Express*, vol. 15, pp. 1762–1772, Feb. 2007.

[178] S. R. Forrest, "The limits to organic photovoltaic cell efficiency," *MRS Bulletin*, vol. 30, no. 1, pp. 28–32, 2005.

[179] S. R. Forrest, "Ultrathin organic films grown by organic molecular beam deposition and related techniques," *Chemical Reviews*, vol. 97, pp. 1793–1896, Oct. 1997.

[180] P. Peumans and S. R. Forrest, "Very-high-efficiency double-heterostructure copper phthalocyanine/C_{60} photovoltaic cells," *Applied Physics Letters*, vol. 79, no. 1, p. 126, 2001.

[181] K. Suemori, M. Yokoyama, and M. Hiramoto, "Electrical shorting of organic photovoltaic films resulting from metal migration," *Journal of Applied Physics*, vol. 99, no. 3, p. 036109, 2006.

[182] A. Hamed, Y. Y. Sun, Y. K. Tao, R. L. Meng, and P. H. Hor, "Effects of oxygen and illumination on the in situ conductivity of C_{60} thin films," *Physical Revue B*, vol. 47, pp. 10873–10880, Apr 1993.

[183] S. Zhang, L. Berguiga, J. Elezgaray, T. Roland, C. Faivre-Moskalenko, and F. Argoul, "Surface plasmon resonance characterization of thermally evaporated thin gold films," *Surface Science*, vol. 601, no. 23, pp. 5445 – 5458, 2007.

[184] E. T. Castellana, S. Kataoka, F. Albertorio, and P. S. Cremer, "Direct writing of metal nanoparticle films inside sealed microfluidic channels," *Analytical Chemistry*, vol. 78, no. 1, pp. 107–112, 2006.

[185] P. Harder, M. Grunze, R. Dahint, G. M. Whitesides, and P. E. Laibinis, "Molecular conformation in oligo(ethylene glycol)-terminated self-assembled monolayers on gold and silver surfaces determines their ability to resist protein adsorption," *The Journal of Physical Chemistry B*, vol. 102, no. 2, pp. 426–436, 1998.

[186] A. Akkoyun and U. Bilitewski, "Optimisation of glass surfaces for optical immunosensors," *Biosensors and Bioelectronics*, vol. 17, no. 8, pp. 655 – 664, 2002.

[187] E. Ostuni, R. G. Chapman, R. E. Holmlin, S. Takayama, and G. M. Whitesides, "A survey of structureproperty relationships of surfaces that resist the adsorption of protein," *Langmuir*, vol. 17, no. 18, pp. 5605–5620, 2001.

[188] S. Lofas and B. Johnsson, "A novel hydrogel matrix on gold surfaces in surface plasmon resonance sensors for fast and efficient covalent immobilization of ligands," *J. Chem. Soc., Chem. Commun.*, pp. 1526–1528, 1990.

[189] J. Homola, "On the sensitivity of surface plasmon resonance sensors with spectral interrogation," *Sensors and Actuators B: Chemical*, vol. 41, no. 1-3, pp. 207 – 211, 1997.

[190] S. H. Choi and K. M. Byun, "Investigation on an application of silver substrates for sensitive surface plasmon resonance imaging detection," *Journal of the Optical Society of America A*, vol. 27, pp. 2229–2236, Oct. 2010.