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A high-yield vacuum-evaporation-based R2R-compatible fabrication route for organic electronic circuits

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ABSTRACT

Advances are described in a vacuum-evaporation-based approach for the roll-to-roll (R2R) production of organic thin film transistors (TFTs) and circuits. Results from 90-transistor arrays formed directly onto a plasma-polymerised diacrylate gate dielectric are compared with those formed on polystyrene-buffered diacrylate. The latter approach resulted in stable, reproducible transistors with yields in excess of 90%. The resulting TFTs had low turn-on voltage, on–off ratios $\sim 10^6$ and mobility ~ 1 cm^2/V s in the linear regime, as expected for dinaphtho[2,3-b:2′,3′-f] thieno[3,2-b]thiophene the air stable small molecule used as the active semiconductor. We show that when device design is constrained by the generally poor registration ability of R2R processes, parasitic source–drain currents can lead to a >50% increase in the mobility extracted from the resulting TFTs, the increases being especially marked in low channel width devices. Batches of 27 saturated-load inverters were fabricated with 100% yield and their behaviour successfully reproduced using TFT parameters extracted with Silvaco's UOTFT Model. 5- and 7-stage ring oscillator (RO) outputs ranged from ~120 Hz to >2 kHz with rail voltages, V_{DD}, increasing from −15 V to −90 V. From simulations an order of magnitude increase in frequency could be expected by reducing parasitic gate capacitances. During 8 h of continuous operation at $V_{DD} = -60$ V, the frequency of a 7-stage RO remained almost constant at ~1.4 kHz albeit that the output signal amplitude decreased from ~22 V to ~10 V. Over the next 30 days of intermittent operation further degradation in performance occurred although an unused RO showed no deterioration over the same period.

1. Introduction

Over the last few years, considerable progress has been made in the design and synthesis of printable, organic semiconductors whose charge carrier mobilities are comparable with that of amorphous silicon, thus enhancing their potential for application in low-cost electronic circuitry. Examples include small molecules [1], polymers [2] and polymer/small molecule blends [3,4]. Achieving the goal of low-cost, large-area electronics, however, requires that the progress in materials development is matched by developments in manufacturing processes which are compatible with the roll-to-roll (R2R) production of, for example, printed packaging materials.

Following an early demonstration of its capability [5,6], inkjet printing was an early contender and is still under active consideration for the partial [7–9] and complete

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[10] fabrication of organic thin film transistors (OTFTs). In 2007 Huebler et al. [11] showed that a combination of offset, gravure and flexographic printing (a faster process than inkjet but of lower resolution) could be used to fabricate an OTFT-based 7-stage ring oscillator at a webspeed of 60 m/min. In 2010, gravure printing of batches of 50,000 OTFTs with ~75% yield at 30 m/min was reported by Hambsch et al. [12]. In the same year, Voigt et al. [13] reported the gravure printing of OTFTs with modest performance at 40 m/min while Verilac et al. [14] used a combination of screen and inkjet printing to fabricate a 5-stage ring oscillator (RO). Subsequently, Noh et al. reported the gravure printing of half adder [15], full adder [16] and D-flip-flop [17] circuits fabricated entirely by gravure printing at a web speed of 10 m/min.

While the above represents significant progress towards realising low-cost electronic circuits using mass printing technologies, there are still many problems to overcome where such methods are used for *all* fabrication steps. Of concern is the relatively low carrier mobility, typically less than ~0.04 cm^2/V s even for small-molecule formulations [10]. This may result from the ink formulation itself, from the semiconductor morphology or from factors such as the surface roughness of (a) the gate insulator in bottom-gate or (b) the semiconductor surface in top-gate devices. When low mobility is combined with the relatively thick gate dielectric layers (typically ~ 2–3 μm) and long channel lengths (typically > 40 μm) found with mass-printing methods, operating voltages in the range 50–100 V are necessary to demonstrate functioning circuits. For example, ROs typically operate at a few Hz [11,12,18], although a frequency of 300 Hz at 50 V was reported by Verilac et al. [14], for ROs fabricated on single sheets using a combination of screen and inkjet printing. Similarly, the digital circuits reported by Noh et al. [15–17] operated at low frequencies with stage delays >10 ms.

Although not generally considered to be a low-cost process, OTFT fabrication by vacuum thermal evaporation of the various layers has considerable attraction. Firstly, patterned metal coatings with a resolution of 30–50 μm can be applied to plastic webs, under vacuum, at web speeds of ~200 m/min using a printed oil film followed by metal evaporation in a type of lift-off process [19,20]. Furthermore, thin, uniform polymer films and hybrid polymer-inorganic barrier-layers may be applied to plastic sheets at high-speed in a R2R process [20–22]. Generally, such layers behave as electrical insulators, thus providing an established route to the deposition of, arguably, the most critical layer in any TFT fabrication process. Vacuum processing removes the need to identify orthogonal solvents and the attendant problems of drying times, handling, recovery and disposal. Other problems are also minimised such as layer interdiffusion, pinhole defects, non-uniform film thickness and surface roughness – all of which lead to device degradation and modest yield, the latter resulting in reduced production efficiency, material wastage and higher cost. When all such factors are considered, if vacuum-processing can deliver reproducible and stable transistors at high yield, it has the potential for providing an attractive route to large-area organic electronic circuit production.

We have already demonstrated that vacuum-based methods, compatible with R2R manufacture can yield OTFTs with promising performance [22–25]. We now report detailed investigations into the performance of OTFTs with dimensions compatible with high-speed, vacuum-based R2R resolution and registration capability, typically 30–50 μm and ±150 μm respectively. The consequence of this approach is that OTFT designs are not optimal. Nevertheless, an opportunity is provided for studying the influence of parasitic effects arising from such limitations which are unavoidable in high-speed R2R processes. Specifically, we report on yield, reproducibility, the dependence of field-effect mobility on channel geometry and the extraction of model parameters from output and transfer characteristics for use in circuit-simulation. We also report on progress made in fabricating and characterising inverters and ring oscillators. In particular, we apply our extracted device model for the first time to simulate inverter and RO performance and show that RO frequency could be increased by almost an order of magnitude above the observed ~2 kHz by eliminating parasitic gate overlap capacitance that arises as a result of the imposed limits on registration.

2. Materials and methods

Substrates used for this work were pre-cleaned, 50 mm × 50 mm squares of polyethylene naphthalate (PEN, Dupont –Teijin). Onto these substrates an 18 × 5 array of 90 bottom-gate, top-contact OTFTs and 5 capacitors were arranged in 5 rows with channel length L increasing in steps from 50 μm to 200 μm. Each row comprised of two blocks of 9 TFTs formed on a common gate. In one of these blocks the channel width, W, was 2 mm, yielding W/L ratios ranging from 40 in the first row down to 10 in the fifth row. In the second block of 9 TFTs in each row, a constant W/L ratio of 20 was maintained so that W ranged from 1 mm in the first row to 4 mm in the fifth row. The 5 capacitors (one in each row) were arranged along a diagonal from one corner of the substrate to the other to provide a multi-point measure of the gate-insulator capacitance. Arrays of inverters and ring oscillators were prepared on other PEN substrates using the fabrication protocols developed for the OTFTs.

The gate level metallisation for both the individual OTFTs and the circuit demonstrators was achieved by thermally evaporating aluminium through appropriate Kapton shadow masks (Laser Micromachining Ltd.) onto the PEN substrates. These were then fixed onto the water-cooled drum of a R2R vacuum web coater (Aerre Machines) and rotated at a linear speed of 25 m/min. Following our previously reported procedures [22–25] tri(propyleneglycol) diacrylate (TPGDA) monomer vapour was flash-evaporated onto the metallized substrate where it condensed forming a thin liquid layer of uniform thickness which immediately passed under a plasma source where it cross-linked to form a robust insulating layer. For the present study, the substrate passed under the TPGDA nozzle several times as the drum rotated, resulting in a ~500 nm thick film after 6–7 cycles. In actual R2R production, we have

demonstrated that reliable dielectric films can be made by single pass deposition and curing [23]. When fabricating ring oscillators, the TPGDA was deposited through a Kapton shadow mask, the 1 mm wide gaps between rectangular islands of dielectric acting as vias for later interconnection between gate and source-drain level metallisations in the final circuit. In an eventual R2R facility such islands of dielectric could be formed by pulsing the monomer vapour supply in an additive-type process.

It is well-recognised [26] that the high-polarity surfaces associated with high dielectric constant dielectrics are detrimental to carrier mobility in OTFTs. Inevitably during the cross-linking of TPGDA, residual ester groups will be present at the insulator surface. We [25] and others [11,27] have shown that such groups may be passivated by applying a thin, non-polar buffer layer such as polystyrene (PS) to the surface prior to depositing the semiconductor. In the present case, PS (M_W = 350,000; Sigma Aldrich) was spin-coated in a nitrogen glove box from a 3% solution in toluene at 1000 rpm and heated on a hot plate at 100 °C for 10 min to form a buffer layer ~300 nm thick. The substrates were then transferred into an integrated evaporator (Minispectros, Kurt Lesker) for the vacuum-deposition (2.4 nm/min) onto the insulator of highly pure, recrystallised dinaphtho [2,3-b:2′,3′-f] thieno[3,2-b]thiophene (DNTT) [28], a high-mobility, air-stable organic semiconductor [29,30]. (Although the semiconductor deposition rate is slow for a R2R process, organic vapour jet printing [31] is an additive technique that has the potential for depositing organic molecules in localised areas at far higher deposition rates and could readily be incorporated into a R2R system). After DNTT deposition and without exposing the substrates to ambient air, the gold source/drain metallisation layer was deposited through a Kapton shadow mask in the same evaporator.

Measurements are reported on TFT arrays formed on (a) unbuffered TPGDA (substrate 1) and (b) PS-buffered TPGDA (substrates 2 and 3). Substrates 1 and 2 were manufactured in the same batch while substrate 3 was manufactured in a second batch at the same time as the substrates for the inverters and ROs.

OTFT characteristics were measured using a Keithley model 4200 Semiconductor Characterization System in ambient dark conditions. Inverter transfer characteristics were obtained using the same system. The time responses of inverters and ring oscillators were recorded by connecting the output of each circuit to a digital oscilloscope (Agilent DSO-X 2014A) via a buffer amplifier to minimise oscilloscope loading effects on the circuits.

Device parameter extraction and circuit simulations were undertaken using Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model (Level = 37) and Gateway Circuit Simulator.

3. Results and discussion

3.1. General observations

When tested in air immediately after fabrication, transistor transfer (I_D vs V_G) characteristics were poor, see Fig. 1. However, dramatic improvements occurred overnight with OTFT performance eventually stabilizing after ~40 h. We surmise that the effect was related to oxygen take-up in the DNTT, the resultant doping increasing either the actual hole mobility [32] or the effective mobility by reducing the resistance of the bulk DNTT between contact and channel. Although no obvious change in morphology was observed, it is possible that slow, beneficial changes in crystal structure may also have occurred in the semiconductor as a result of exposing the vacuum-deposited semiconductor to atmospheric pressure in order to measure device characteristics [33]. Consequently, measurements on the 90-transistor arrays were all undertaken sequentially between 40 and 48 h after fabrication.

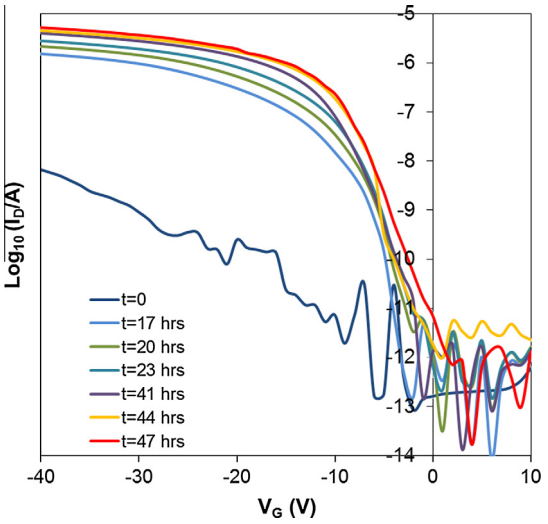

Fig. 1. A series of transfer characteristics obtained at different times after fabrication. On testing immediately after fabrication, the OTFT barely displayed any transistor action but improved significantly over time.

The capacitance of the test capacitors on the OTFT substrates varied by no more than ~5% over the substrate area thus confirming the excellent thickness uniformity of the TPGDA gate dielectric produced in our process. However, there were differences between batches of insulator produced at different times. For example, for substrates 1 and 2 the average capacitance per unit area, C_i, was 3.29 nF/cm^2 while for the second batch of substrates, thinner TPGDA films were targeted leading to an increase in average C_i to 4.83 nF/cm^2.

Microscope examination of the channel length, L, from a sample of devices on each substrate showed that departures from the designed value were no more than ±5 μm.

3.2. Effect of polystyrene buffer on OTFT performance

In a recent publication [25] we showed that by applying a PS buffer layer to the TPGDA, the performance of the resulting pentacene TFTs was significantly improved. Preliminary data was also given showing that a similar improvement may also be possible for DNTT devices. In this section, we provide statistical data from our 90-TFT arrays to support this earlier finding.

In Fig. 2 are the linear and saturation transfer characteristics of blocks of 9 adjacent transistors with common gate (see inset of Fig. 2(a)) formed on (a) TPGDA (1 device failed) and (b) on PS-buffered TPGDA. Without buffering, strong hysteresis is observed when sweeping V_G from 10 V to −60 V and back again. This, and the lack of overlap between linear and saturation characteristics in the lower current regimes, are symptomatic of an unstable threshold voltage. Nevertheless, turn-on voltages are in the range ±10 V and even though off-currents are relatively high, especially in saturation, on–off ratios are $\sim 10^5$.

In contrast, the off-currents of the PS-TPGDA devices in the linear regime are below the noise floor of our measurement system (~1 pA) and increase to only ~10 pA in saturation, leading to on–off ratios in excess of 10^6. Some of these devices displayed a shallower subthreshold slope at low currents, probably arising from a higher interface trap density [34]. However, no hysteresis was observed between the forward and reverse voltage sweeps, as evidenced by the transfer characteristics in Fig. 3 of one of the devices from Fig. 2(b). In almost all PS-buffered devices the gate leakage current, I_G, was independent of source–drain voltage, V_D, but greater than the off-current, suggesting that gate–source leakage dominated gate current.

Device current, I_D, in the linear regime is given by

$$I_D = \frac{W}{L}\mu_{lin}C_i(V_G - V_T)V_D \quad (1)$$

and in saturation by

$$I_D = \frac{W}{2L}\mu_{sat}C_i(V_G - V_T)^2 \quad (2)$$

where V_T is the threshold voltage. The mobilities in the linear (μ_{lin}) and saturation (μ_{sat}) regimes were extracted from the local slopes of the transfer plots using, respectively, the equations [35]

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G}\cdot\frac{L}{WC_iV_D} \quad (3)$$

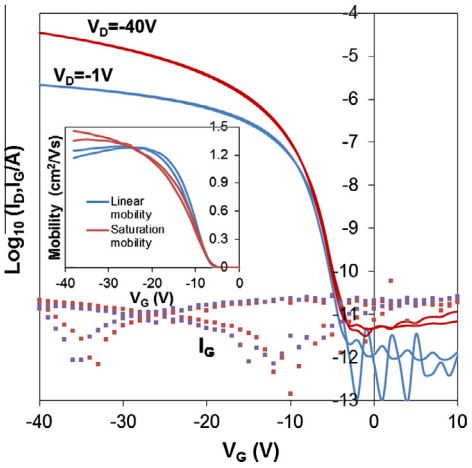

Fig. 3. Transfer characteristics in the linear and saturation regimes for one of the devices from Fig. 2(b) formed on PS-TPGDA. Also shown are the gate leakage current, I_G, (dotted curves) and the gate voltage dependence of mobility in both regimes (inset).

and

$$\mu_{sat} = \left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2\cdot\frac{2L}{WC_i} \quad (4)$$

It should be noted, though, that these equations are only valid when the mobility is weakly dependent on gate voltage and can lead to an over-estimate when mobility increases strongly with V_G while under-estimating when mobility decreases with V_G [36].

With this caveat, extracted mobilities from the transfer characteristics in Fig. 3 are plotted as a function of V_G in the figure inset. Both μ_{lin} and μ_{sat} begin to increase rapidly at about −7 V following similar paths. As V_G becomes more negative, μ_{lin} rises more rapidly, eventually reaching a maximum of 1.29 $cm^2/V\,s$ before decreasing to 1.24 $cm^2/V\,s$

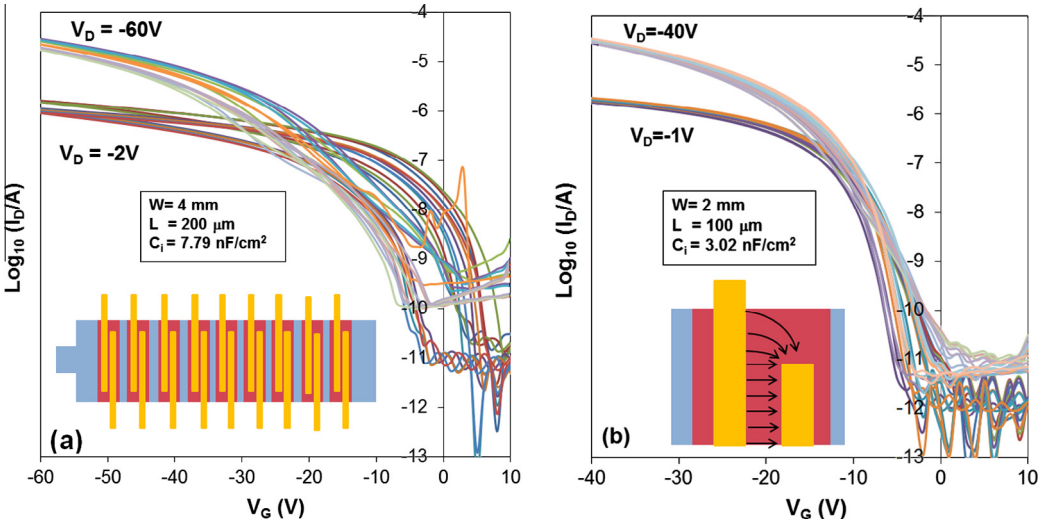

Fig. 2. Transfer characteristics in the linear and saturation regimes for blocks of 9 × DNTT TFTs fabricated on (a) TPGDA (1 device failed) and (b) PS-TPGDA gate insulators. The inset in (a) shows a schematic plan view of one of the 10 blocks of 9 TFTs with common gate on each substrate while that in (b) illustrates the current flow lines between source and drain near the tip of one electrode.

when $V_G = -40$ V. This slight decrease may be real and caused by carrier scattering at the higher gate voltages. However, such an effect is thought to occur at much higher channel carrier densities (>10^{13} cm^{-2}) [36] than is the case here (~10^{12} cm^{-2}). A second possibility is the presence of contact/series resistances at the source and drain. By reducing the effective potentials experienced by the accumulation channel, I_D and hence the extracted mobility are lower than expected for the given applied voltage conditions [37]. Unexpectedly, after lagging behind initially, μ_{sat} increased above μ_{lin} and continued to increase for increasingly negative V_G.

Fig. 4(a) is a histogram of the maximum values of μ_{lin} and μ_{sat} for all working devices fabricated on the TPGDA and PS-TPGDA insulators. In Fig. 4(b) and (c) the maximum values for μ_{lin} and μ_{sat} for all 81 working PS-TPGDA devices on one substrate are plotted as a function of the channel length L. Owing to a problem associated with the common gate of the block of 9 devices corresponding to $L = 200$ μm, $W = 2$ mm, no values were available for this group. However, values have been included (open circles) for two devices with the same geometry fabricated on a second batch of PS-TPGDA devices. These latter devices were also the ones used for parameter extraction – see next section. From these combined data we notice some important trends.

(a) Polystyrene buffering of the TPGDA produces a clear improvement in hole mobility (Fig. 4(a)) in addition to reducing threshold voltage instabilities as discussed above.

(b) μ_{lin} and μ_{sat} in the TPGDA-only devices are similar but for the PS-TPGDA devices μ_{sat} exceeds μ_{lin} in all devices.

(c) For PS-TPGDA devices with constant $W/L = 20$, μ_{lin} and μ_{sat} increase on average by ~50% and ~30% respectively as L decreases from 200 μm to 50 μm (W decreasing from 4 mm to 1 mm). This effect is readily explained by the increased area in which a parasitic source–drain fringe current can flow between the tip of one electrode and its counter-electrode (see insets in Fig. 2). As W decreases, the parasitic current then provides a greater fraction of the total device current. The larger values of μ_{sat} in the PS-TPGDA devices suggest that the higher source–drain voltage, $V_D = -40$ V, applied during these measurements causes the fringe currents to increase even after the main channel has saturated. Although not shown here, this is reflected in the saturation region of the output characteristics, which display a finite and decreasing output resistance (increasing slope) as W and L decrease to lower values. Similar trends were observed in TPGDA-only devices and are responsible for the high mobility tails in the distributions in Fig. 4(a). However, the similar values for μ_{lin} and μ_{sat} suggest that parasitic currents in these devices are less sensitive to V_D. This probably reflects the lower mobility and/or poorer turn-on characteristics in these devices, which in turn results in a weaker V_G-dependence of the DNTT sheet conductance in the regions outside the main channel.

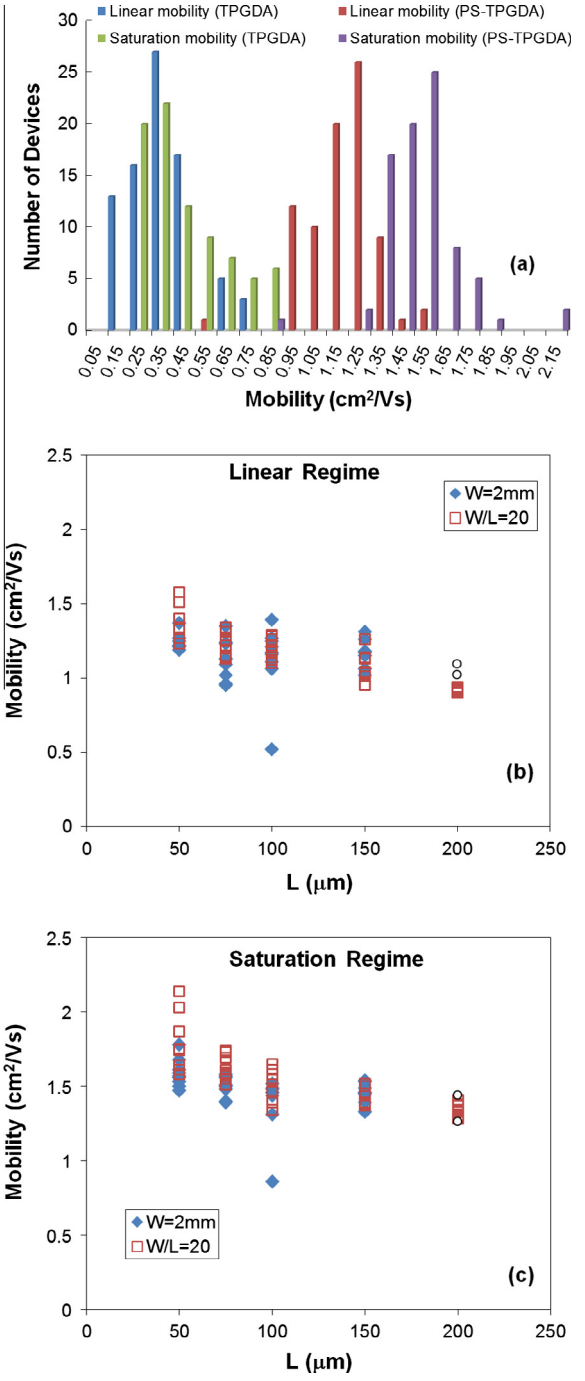

Fig. 4. (a) Histogram showing the number of devices with mobility in the range ±0.05 cm^2/V s of the values indicated on the horizontal axis. The improvement achieved by buffering the TPGDA surface with polystyrene is clear. Maximum mobilities extracted in (b) linear and (c) saturation regimes of all the functioning devices on the PS-TPGDA substrate. Also provided for comparison (two open circles) are the mobilities extracted from two devices ($W = 2$ mm, $L = 200$ μm) from another substrate.

(d) For devices in which $W = 2$ mm, both μ_{lin} and μ_{sat} increase by ~18% as L decreases from 200 μm to 50 μm. Since the area in which parasitic currents

can flow are identical in all these devices, then the relative contribution of the parasitic fringe currents must also increase slowly as L decreases.

(e) Mobilities extracted for the two devices from the second batch of PS-TPGDA substrates (open circles in Fig. 4(c)) fit well with the pattern observed for devices from the first batch confirming the reproducibility of the fabrication process even using thinner PS-TPGDA films.

(f) Detailed analysis of the spatial distribution over the substrate area of the mobility values in Fig. 4(b) and (c) indicated a systematic decrease towards the middle of the substrate suggesting the presence of a process-dependent parameter. Since we did not measure insulator thickness and insulator capacitance for every device on the substrate, it is possible that changes in dimensions may be responsible. However, the small variations found in the test capacitors (see above) and observed departures from the designed channel length would be insufficient to explain the mobility differences observed. Other possibilities include differences in DNTT thickness and/or morphology leading to changes in mobility either directly or indirectly e.g. through the effects of parasitic series resistance between the contacts and the active channel.

From the above considerations, we deduce, therefore, that the true hole mobility in our TFTs is likely to be $\sim$1 cm^2/V s. This being the case, it is clear that parasitic source–drain currents can inflate μ_{lin} by $\sim$40% and μ_{sat} by $\sim$80% when channel dimensions, especially W, are small relative to the gate and semiconductor dimensions. Clearly, careful device design will reduce such effects. However, while achieving the ideal structure (self aligned gates and appropriately patterned semiconductor) is possible for low-speed, small batch production, this is unlikely in a high speed R2R process until significant advances are made in web control.

3.3. Extraction of OTFT parameters

In a recent publication [24] we showed that the Silvaco UOTFT parameter extraction software was effective in allowing relevant device parameters to be extracted. That work was mainly concerned with TPGDA-based devices with one example given for a PS-TPGDA/DNTT transistor measured under vacuum. Here we use the same software to extract parameters for PS-TPGDA/DNTT devices measured in air. The model card thus extracted was then used for the first time to simulate the performance of circuits assembled using our TFT fabrication protocols. Based on the discussion in the previous section, the two devices represented by the open circles in Fig. 4 were considered the most likely to provide representative device parameters since they are the least affected by parasitic currents. In Fig. 5, therefore, we show the results of simulating both the transfer and output characteristics of these two adjacent devices (L = 200 μm, W = 2 mm) fabricated on the second batch of PS-TPGDA substrates.

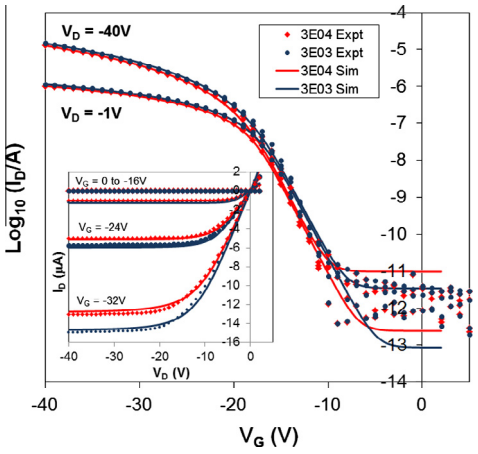

Fig. 5. Transfer and output (inset) characteristics of two adjacent devices (data points) formed on the second batch of PS-TPGDA. The solid lines are simulations obtained using the Silvaco UOTFT software. The main fitting parameters are given in Table 1.

As can be seen, the characteristics of both devices follow each other closely confirming the reproducibility of adjacent devices. Not surprisingly, they can also be simulated accurately with only minor changes in device parameters (see Table 1). It should be noted that the linear and saturation regimes of the output and transfer plots were fitted *simultaneously* thus testifying to the electrical stability of the devices.

Some of the parameter values extracted here are close to those published earlier for device O-D04 [24]. In particular μ_{ACC}, the mobility at the onset of strong channel accumulation, is $\sim$1 cm^2/V s and very close to the maximum linear mobility extracted using Eq. (3). The gate-voltage dependence of mobility represented by the power-law parameter, γ, is weak in buffered devices ranging from 0 to 0.03 compared with 0.3 for the unbuffered device, B-D12. In all cases good saturation of the output characteristics was observed, $\lambda = 0$. The output characteristic shape parameters, M_{SAT} (the knee-shape parameter) and A_{SAT} (a parameter that modulates the voltage corresponding to the onset of saturation) were similar in all cases. This good agreement between the different PS-buffered devices again confirms the reproducibility of device production – device O-D04 was fabricated at a different time and in a different laboratory to the two devices reported here. Where significant differences in fitting parameters do occur, these we may attribute to the fact that, although previously exposed to air for some time, device O-D04 was actually measured under vacuum. The non-zero source/drain series resistances R_S and R_D extracted in this case supports the argument that the improved device performance observed in the 2 days after fabrication (Fig. 1) is, at least partially, the result of air-doping. Furthermore, the threshold voltage, V_T, and the density of states parameter, V_0, are both lower in the device measured under vacuum, again suggesting that atmospheric air or moisture influences both the insulator and the insulator/semiconductor interface.

Table 1
Fitting parameters for DNTT devices with different gate dielectrics. The parameters are described in the text except for σ_0 the minimum bulk conductance. It was assumed in all the simulations that, the characteristic voltage of the effective mobility, $V_{ACC} = 1$ and the leakage saturation current, $I_{OL} = 3$ fA. The parameters for devices B-D12 and O-D04 were reported previously [24].

Parameter	B-D12	O-D04	This work	
			Device 1 (3E03)	Device 2 (3E04)
Insulator	TPGDA	TPGDA/polystyrene	TPGDA/polystyrene	TPGDA/polystyrene
Ambient	Air	Vacuum	Air	Air
W (μm)	3000	2400	2000	2000
L (μm)	150	200	200	200
C_i (F/cm^2)	5.84×10^{-9}	1.28×10^{-8}	4.83×10^{-9}	4.83×10^{-9}
V_T (V)	−4.78	−1.31	−17.86	−18.4
V_O (V)	3.12	0.307	0.948	0.893
V_{ACC}	1	1	1	1
μ_{ACC} (cm^2/V s)	0.0391	1.05	1.07	1.08
γ	0.362	0	0.031	0
λ	0	0	0	0
M_{SAT}	3.41	2.58	3.90	3.57
A_{SAT}	1.421	1.41	1.19	1.16
σ_0 (S)	1×10^{-20}	1×10^{-13}	8.66×10^{-15}	2.44×10^{-14}
R_S (Ω)	0	7.39×10^4	0	0
R_D (Ω)	0	8.66×10^4	0	0

3.4. PS-TPGDA/DNTT inverter

Using PS-buffered TPGDA as the gate insulator and a similar transistor design to that in Fig. 2, batches of 27 unipolar, saturated-load inverters (inset Fig. 6) were fabricated on each of 10 substrates (2nd batch of PS-TPGDA) with a 100% yield being achieved. The W/L ratios for the driver and load transistors were (2500 μm)/(50 μm) and (625 μm)/(100 μm) respectively. The inset in Fig. 6 demonstrates the inverter response to a slowly varying square wave and confirms stable device operation. The main figure shows the experimentally obtained voltage transfer characteristics for the device (points) for different supply voltages (V_{DD}). For comparison we also give the simulated response (lines) based on the model card in Table 1 for Device 1 but with the appropriate values for W and L substituted for the driver and load transistors.

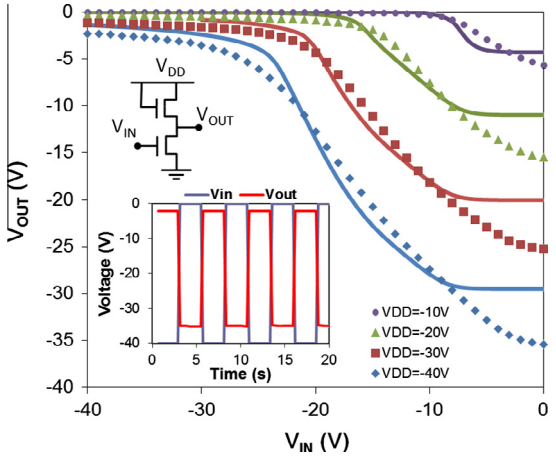

Fig. 6. Experimentally-measured inverter voltage transfer characteristics (points) for different supply voltages, V_{DD}. Also shown (lines) are simulations based on the model card for transistor 3E03 (see Table 1). The insets show the saturated load inverter circuit and the inverter response to a square wave input signal with $V_{DD} = -40$ V.

The simulated plots obtained using Silvaco's Gateway SPICE-modeller, provide a reasonable match to the experimental results over much of the operational range. However, they clearly underestimate the 'pull-up' ability of the load transistor. This is not surprising given the effect of device geometry on the saturation mobility in Fig. 4(c). While the relative magnitude of the parasitic source–drain current effect will be small in the driver transistor ($W = 2.5$ mm) compared to Device 1 ($W = 2$ mm), it will be much greater in the saturated load transistor ($W = 0.625$ mm). To achieve improved simulations, therefore, it would be necessary to include in the TFT model a description of the additional V_D-dependent parasitic source–drain current depicted in Fig. 2(b). Alternatively, the simulation could be validated in additional experiments in which the semiconductor is appropriately patterned as discussed earlier.

3.5. PS-TPGDA/DNTT ring oscillators

Using the same high-yield fabrication protocols established for the TFTs and inverters, both 5- and 7-stage ring oscillators (ROs) were fabricated, again on the 2nd batch of PS-TPGDA substrates. As shown in the inset of Fig. 8, the ROs were based on inverters composed of a driver transistor, W/L = (4000 μm)/(50 μm), and a saturated transistor load, W/L = (400 μm)/(50 μm). Measurements on the 7-stage device were commenced some 21 h after the final fabrication step i.e. during the period when transistor performance was close to, but not in, the stable range following the initial increase (Fig. 1). The 5-stage device was kept in a sealed, translucent plastic box under laboratory conditions for 1 month prior to measurements. For both cases, the devices began to generate an output signal >100 Hz even with V_{DD} as low as −15 V (Fig. 7). On increasing V_{DD}, device frequencies increased non-linearly. With $V_{DD} = -90$ V the 5-stage RO achieved an output frequency

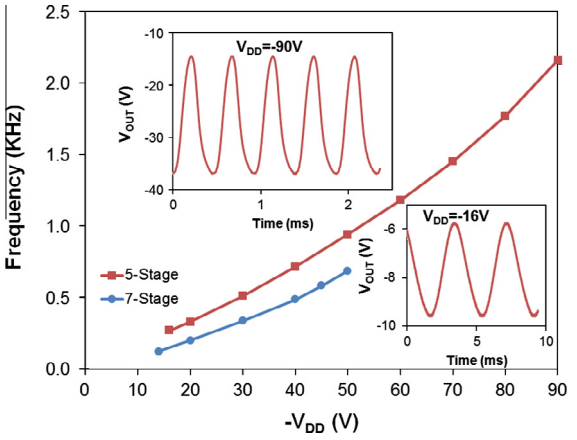

Fig. 7. Output frequency of 5- and 7-stage ring oscillators as a function of the rail voltage V_{DD}. The 7-stage device was tested 21 h after fabrications while the 5-stage device was tested 1 month after fabrication. The insets show the outputs from the 5-stage ring oscillator with $V_{DD} = -16$ V, the minimum operating voltage, and at -90 V the highest applied voltage.

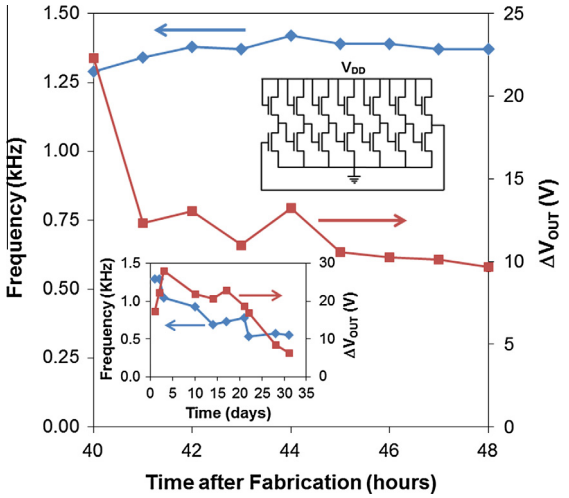

Fig. 8. Performance of a 7-stage ring oscillator during 8 h of continuous operation beginning 40 h after fabrication ($V_{DD} = -60$ V). Also shown as an inset, is the performance measured intermittently over 1 month starting 21 h after fabrication.

of 2.16 kHz, corresponding to a stage-delay of 46 μs. Examples of the approximately sinusoidal output waveforms of the 5-stage RO obtained at $V_{DD} = -16$ V and -90 V are shown as insets in Fig. 7.

The frequencies attained in our devices are significantly higher than previously reported values (a few Hz up to 300 Hz) for ring oscillators fabricated entirely using mass printing technologies [11,12,14,18] and highly competitive with ROs fabricated from an inkjet-printed small molecule blend onto OTFT structures with 5 μm channel length defined photolithographically [7]. This is particularly encouraging since all our processes, apart from the polystyrene buffer layer, are compatible with a vacuum-evaporation-based R2R process.

Subsequent to obtaining the results shown in Fig. 7 and reflecting the improvement in transistor characteristics seen in Fig. 1, the performance of the 7-stage RO also improved with time. When measured with $V_{DD} = -60$ V, the RO frequency had increased after 1 h to 980 Hz and 3 h later to 1.33 kHz.

Commencing 40 h after fabrication, the 7-stage RO was run continuously with $V_{DD} = -60$ V for 8 h – equivalent to each inverter undergoing $\sim 3 \times 10^7$ switching cycles over the period. The performance during that time is given in Fig. 8 where the output frequency is seen to remain essentially constant, rising slowly to a maximum of 1.42 kHz before falling slightly to 1.37 kHz after 8 h of operation. The biggest change in device performance occurred in the peak-to-peak output voltage swing, ΔV_{OUT}. One day after fabrication $\Delta V_{OUT} = 17.3$ V, increasing to 22.4 V on day 2. However, during the first hour of continuous operation, ΔV_{OUT} fell to $\sim$12 V, thereafter decreasing only slowly to $\sim$10 V (Fig. 8).

Following the period of continuous operation the device was turned off but subsequently tested intermittently during a period of 31 days after fabrication. The results are shown in the inset to Fig. 8. Here we see a continuous degradation in performance with the output frequency tending to stabilize at $\sim$500 Hz but with ΔV_{OUT} decreasing steadily from a high of 28 V to $\sim$6 V.

Clearly, since 1 month in storage did not adversely affect the 5-stage RO, the degradation in the performance of the 7-stage device we presume is linked to the 8-h period of continuous operation on day 2. Further work is needed to confirm whether this arises simply from charge trapping or from subtle, electrically-induced chemical changes at the insulator–semiconductor interface such as those described by Di Pietro and Sirringhaus [38] for n-type organic semiconductors.

Simulations of the 5-stage ring oscillator were also carried out using Silvaco's Gateway modeller and the model card for Device 1 (Table 1). Interestingly, these showed that for V_{DD} set to -40 V and -60 V our ROs should be capable of providing operating frequencies of 7 kHz and 20 kHz respectively i.e. more than an order of magnitude higher than observed in practice (Fig. 7).

To investigate the reason for this discrepancy, soon after completing the test measurements in Fig. 7, an inverter from the 5-stage RO was isolated and its response to a -60 V, 1 kHz input square-wave examined (Fig. 9). The 'spikes' seen at the leading and trailing edges of the inverter output arise from capacitive breakthrough from the input signal and are not of interest. The more important features arise from effects related to the load transistor.

(a) The 'pull-up' ability of this transistor is weak. The inverter output reached only -27 V, less than half the rail voltage ($V_{DD} = -60$ V). Since the load TFT operates in saturation, from Eq. (2) $I_D(load)$ is given by

$$I_D(load) = \frac{W}{2L}\mu_{sat}C_i[(V_{DD} - V) - V_{TL}]^2 \quad (5)$$

where V_{TL} is the threshold voltage of the load TFT, V_{DD} is the rail voltage and V the output voltage of the inverter. In the ideal case of the driver transistor being fully turned off when $V_G(driver) = 0$ V, then the

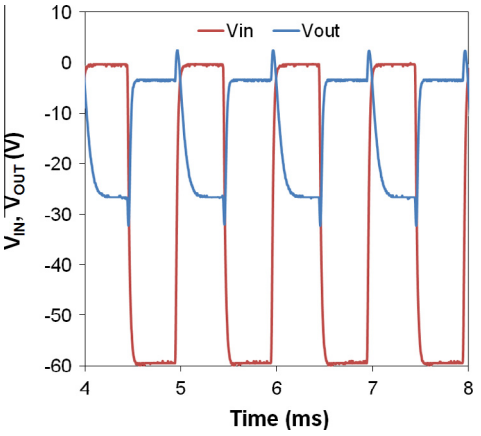

Fig. 9. Response of an inverter stage from the 5-stage ring oscillator (V_{DD} = −60 V).

inverter output of −27 V would correspond to the condition ($V_{DD} - V - V_{TL}$) = 0, suggesting a shift in V_{TL} to −33 V as a result of bias stress while acquiring the results in Fig. 7. This is likely to be an over-estimate, however, owing to the non-zero off-current of the driver TFT.

(b) When measuring the inverter response in Fig. 9, the buffer amplifier and coaxial cable presented a load capacitance of ~48 pF at the inverter output. Owing to the lower on-conductance of the load transistor, the time to charge this capacitance via the load TFT, ~0.3 ms, is longer than for discharging through the driver TFT, ~0.1 ms. In the case of the RO, the relevant capacitance is the channel capacitance, WLC_i ~ 10 pF, of the driver TFT of the following stage, suggesting that the RO should be capable of operating well above 10 kHz. However, such considerations neglect the effect of parasitic capacitances, especially gate–source, C_{gs}, and gate–drain, C_{gd}, overlap capacitances.

In Fig. 10 we show the results of simulations in which the effect of these capacitances on the 5-stage RO frequency was investigated. In the simulations it was assumed that V_{DD} = −60 V and that, based on the transistor designs, the gate overlap in the driver transistors was symmetrical so that $C_{gsD} = C_{gdD}$ and that for the load TFT $C_{gsL} = 0.2C_{gdD}$.

It is obvious that overlap capacitances seriously impair RO operation, with the simulated output frequency decreasing from 20 kHz with no parasitic capacitance to less than 1 kHz when $C_{gdD} > 22$ pF. When measured directly, C_{gdD} = 35 pF and C_{gsD} = 50 pF owing to slight registration errors during fabrication. According to Fig. 4(c), the aspect ratio of the load transistors in the ring oscillator, W/L = (400 μm)/(50 μm), is such that parasitic currents would make an even greater contribution to the overestimate of saturation mobility than was observed for the devices in which W/L = (1000 μm)/(50 μm). The true conductance of the load TFTs would have been much greater, therefore, than expected from the designed width, W. In a first approximation to account for this effect, the conductance

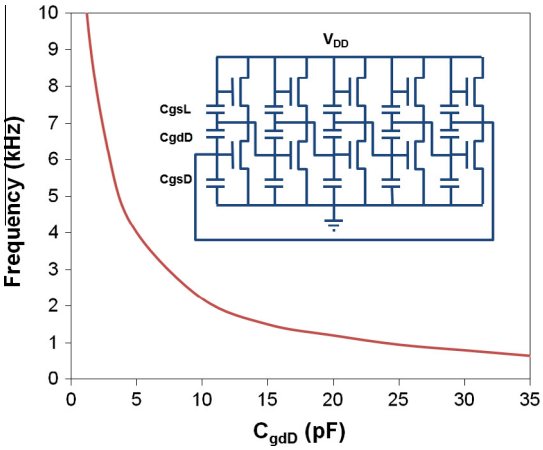

Fig. 10. Effect of parasitic capacitances on the 5-stage ring oscillator frequency deduced from simulations with V_{DD} = −60 V. The inset shows the ring oscillator circuit including parasitic gate–source, C_{gs}, and gate–drain, C_{gd}, capacitances added to the driver (D) and load (L) OTFTs. In the simulation it was assumed that $C_{gdD} = C_{gsD} = 5C_{gsL}$.

of the load transistors was doubled by increasing the effective W to 800 μm. With these more realistic values included in the model, the simulated RO oscillated at 1 kHz and close to the measured frequency of 1.12 kHz. Interestingly, had the misalignment error led to a reversal in the values of C_{gdD} and C_{gsD}, the simulated RO frequency would have decreased below 500 Hz i.e. gate–drain overlap capacitance of the driver TFT, C_{gdD}, has a greater degrading effect than the gate-source capacitance, C_{gsD}. Not unexpectedly, therefore, registration and gate overlap capacitances will be important issues to manage in a high-speed R2R process.

4. Conclusions

We have demonstrated that bottom-gate DNTT transistors with mobility ~1 cm^2/V s can be fabricated routinely and reproducibly with yields ⩾90%. Apart from the polystyrene buffer layer applied to the TPGDA all fabrication steps were based on vacuum-evaporation and compatible with a R2R process. Interestingly, optimum device performance was achieved some 40 h after removing the devices from the evaporator following the final metallisation step. By characterising 90-transistor arrays on each substrate we have obtained statistical information on the likely spread in mobility values as well as on the effect of parasitic source–drain currents which, in smaller devices $W \leqslant 1$ mm results in the mobility in saturation being overestimated by more than 50%. By choosing TFTs in which parasitic currents were considered negligible, a model card of relevant parameters was derived by simultaneously fitting transfer and output characteristics using Silvaco's UOTFT model. The model card was then applied successfully to simulate inverter operation using Silvaco's Gateway simulator.

Unipolar inverters based on a saturated-transistor load and coupled to a buffer amplifier presenting a load capacitance of 48 pF and with V_{DD} = −60 V, were shown to be capable of undergoing a full switching cycle in ~0.4 ms

corresponding to a switching frequency of 2.5 kHz. When coupled in series with other inverters to form 5- and 7-stage ring oscillators, significantly shorter switching times corresponding to operational frequencies >10 kHz were anticipated owing to the lower load capacitance, ~10 pF, presented by the accumulation channel of the driver transistor of the following stage. In the event, the output frequencies of a 5-stage RO ranged from 270 Hz at $V_{DD} = -16$ V to 2.16 kHz when $V_{DD} = -90$ V. Simulations showed that the degradation in performance was caused by gate–source and gate–drain overlap capacitances, with the latter having the greater effect because of the smaller size of the load transistor. When these are taken into account, together with an allowance for the parasitic-current-enhanced performance of the load TFTs, a reasonable match between experimental and simulated frequencies was obtained.

We have also shown that a ring oscillator based on DNTT/PS-buffered TPGDA TFTs can operate continuously for 8 h at $V_{DD} = -60$ V with relatively little change in output frequency albeit that a reduction in amplitude occurs. When tested intermittently over the following month, the RO continued to operate but displayed reductions in both the frequency and amplitude of the output signal. A non-encapsulated RO stored without bias under atmospheric conditions for a month performs as well as a pristine device. We conclude from these observations that continuous operation for long periods initially, can lead to enhanced atmospheric degradation during later storage.

In conclusion, we have demonstrated that functional, environmentally stable organic electronic circuits can be fabricated reproducibly with high yield using low-cost, vacuum-evaporation-based processes that are common in the packaging industry. However, improving circuit performance by minimising gate overlap capacitances must be a key target for future R2R processes.

Acknowledgements

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