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Fabrication and simulation of organic transistors and functional circuits

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ABSTRACT

We report the development of a vacuum-evaporation route for the roll-to-roll fabrication of functioning organic circuits. A number of key findings and observations are highlighted which influenced the eventual fabrication protocol adopted. Initially, the role of interface roughness in determining carrier mobility in thin film transistors (TFTs) is investigated. Then it is shown that TFT yield is higher for devices fabricated on a flash-evaporated-plasma-polymerised tri(propyleneglycol) diacrylate (TPGDA) gate dielectric than for TFTs based on a spin-coated polystyrene (PS) dielectric. However, a degradation in mobility is observed which is attributed to the highly polar TPGDA surface. It is shown that high mobility, low gate-leakage currents and excellent stability are restored when the surface of TPGDA was buffered with a thin, spin-coated PS film. The resulting baseline process allowed arrays of functional circuits such as ring oscillators, NOR/NAND logic gates and S–R latches to be fabricated with high yield and their performance to be simulated.

1. Introduction

The most widely adopted approaches for the roll-to-roll (R2R) fabrication of organic electronic devices and circuits are generally based on solution processing e.g. inkjet [1–3] and gravure [4–7] printing which have also been used in combination with other methods including screen and flexo printing [8,9]. However, devices fabricated using only solution processing can suffer from poor yield arising mainly from a defective gate insulating layer and layer interdiffusion. Open- or short-circuited electrodes and tracks can also become issues as device sizes are reduced and production speeds increase. The best performing organic circuits to date, however, have been achieved by combining solution processing with a photolithographic step [10–13]. The latter allows much higher resolution features to be formed which is especially important for defining the source–drain gap (channel length, L) in thin film transistors (TFTs). However, incorporating a photolithographic step into a roll-to-roll process is not trivial.

Given these problems and limitations, it is surprising perhaps that only limited interest has been shown in developing a fabrication method based on the vacuum-evaporation of all the device layers – metal, insulator and semiconductor. Such an approach overcomes many of the problems associated with solution processing. It is usually argued that the capital cost is prohibitive, yet commercial equipment is already available for (a) producing high resolution metal patterns on plastic sheets in a R2R process [14,15] and (b) depositing organic and inorganic barrier layers onto moving plastic webs [15–17] – in both cases by evaporation under vacuum.

We reported on the feasibility of a vacuum-evaporation route for organic thin film transistor (OTFT) fabrication some years ago [17]. The key step in the process was the production of the gate insulator in a vacuum R2R environment by deposition and subsequent electron-beam polymerisation of the deposited monomer tri(propyleneglycol) diacrylate (TPGDA). In this early work, the hole mobility in bottom-gate top-contact (BGTC) pentacene OTFTs was only ~0.09 cm^2/V s and the characteristics tended to be unstable. Also, pentacene is prone to long-term oxidative degradation so that identification of a high mobility, air-stable replacement semiconductor was essential. Although not reported earlier, top-gate bottom-contact (TGBC) OTFTs were also fabricated but showed much poorer performance. At the time, this was thought likely to be due to degradation of the pentacene by the high energy electron-beam used to polymerise the TPGDA.

In the following, previously unpublished results and data are used to trace, from this modest beginning, the development of a high-yield, baseline vacuum-evaporation process for the

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production of OTFTs with reproducibly good performance [18,19] which in turn has allowed the demonstration of functioning circuits [20].

2. Materials and methods

Dinaphtho[2,3-b:2′,3′-f] thieno[3,2-b]thiophene (DNTT) was chosen for this work since it has a similar mobility to pentacene but with better environmental stability [21] due to a reduced tendency to oxidise. It was synthesised following a previously published route [22] from 2-naphthaldehyde with 35% overall yield. By repetition of 300 mg scale iodine-catalysed ring closure followed by two recrystallisations from *o*-dichlorobenzene, high purity DNTT was obtained as bright yellow microcrystals in 1 g batches. TPGDA monomer and polystyrene (M_W = 350,000) were purchased from Sigma Aldrich and used without further purification.

Arrays of TFTs and circuits were fabricated on precleaned, 5 cm × 5 cm, 125 μm thick polyethylene naphthalate (PEN) substrates (Dupont-Teijin). Full details of our vacuum-fabrication procedures have been given in previous publications [17–19,23]. Briefly, aluminium gate electrodes and associated tracks were vacuum evaporated onto the substrates through shadow masks. Subsequently, the substrates were attached to a cooled web-coater drum (Aerre Machines). With the drum rotating at a linear speed of 25 m/min under vacuum, flash-evaporated TPGDA monomer vapour which condensed onto the substrates was cross-linked by exposure, in situ, to a plasma. The resulting smooth, pinhole-free films were typically 500 nm to 1 μm thick with a measured dielectric constant varying in the range 4–5. For circuit fabrication, the insulator was patterned using shadow masks to define rectangular areas separated by 1 mm gaps to act as vias for inter-layer metallic connections. The substrates were then transferred into an evaporator (Minispectros, Kurt Lesker) integrated into a nitrogen glovebox for the vacuum-deposition (2.4 nm/min) of DNTT onto the insulator. Without exposing the substrates to ambient air, the gold source/drain metallisation layer was deposited through a shadow mask in the same evaporator.

The OTFT masks defined an 18 × 5 array of 90 transistors with 5 capacitors arranged diagonally across the substrate. These capacitors were used to extract values for the capacitance per unit area of the gate dielectric for later use in parameter extraction. The variation in values over the substrate was typically less than 5%. The channel length L of the OTFTs in each row increased in steps from 50 to 200 μm. Each row comprised of two blocks of 9 OTFTs. In the left hand blocks the channel width, W, was 2 mm, yielding W/L ratios ranging from 40 in the first row down to 10 in the fifth row. In the right hand blocks of 9 OTFTs, a constant W/L ratio of 20 was maintained so that W ranged from 1 mm in the first row to 4 mm in the fifth row. Arrays of logic gates and ring oscillators were prepared on other PEN substrates using the fabrication protocols developed for the OTFTs [18,20]. Our OTFT designs were not optimised in the sense that allowances were made both for the resolution and registration ability (±100 μm) likely in a high-speed R2R process. The former limits channel length to ~40 μm, while the latter leads to the possibility of parasitic currents and capacitances in our devices and circuits as discussed later.

To counter the deleterious effects that the high-polarity TPGDA dielectric had on OTFT characteristics, it was found beneficial to passivate the insulator surface with thin (30–300 nm) polystyrene films (dielectric constant, 2.6) prior to depositing the semiconductor [24]. This was achieved by spin-coating from a toluene solution in a nitrogen glovebox and heating on a hot plate at 100 °C for 10 min. Also, for comparing the performances of top-gate versus bottom-gate OTFTs and process yield, some OTFT arrays were fabricated using thicker (~1 μm) spin-coated layers of polystyrene as the gate insulator.

Topographic images of the various film layers were obtained in tapping mode using a Veeco Dimension 3100 Atomic Force Microscope (AFM). OTFT characteristics were measured in air using a Keithley model 4200 Semiconductor Characterisation System in ambient dark conditions. Inverter transfer characteristics were obtained using the same system. The time responses of logic gates and ring oscillators were recorded by connecting the output of each circuit to a digital oscilloscope (Agilent DSO-X 2014A) via a buffer amplifier to minimise oscilloscope loading effects on the circuits. Device parameter extraction and circuit simulations were undertaken using Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model (Level = 37) and Smartspice Circuit Simulator.

3. Results and discussion

3.1. Bottom-gate versus top-gate OTFTs

Our initial investigations into the use of vacuum-deposited TPGDA as a gate insulator had established that bottom-gate, top-contact (BGTC) pentacene TFTs, Fig. 1(a), were superior to top-gate, bottom-contact (TGBC) devices, Fig. 1(b). Since, the BGTC structure is simply the inverted form of the TGBC structure, significant differences in injection area at the source contact may be ruled out as the cause. It was thought initially that the difference arose from the detrimental effect of electron-beam or plasma processing of the insulator when overlying the semiconductor in the top-gate structures. To rule out such radiation-related effects, initial measurements on DNTT devices were made using spin-coated polystyrene (PS) as the gate insulator in BGTC and TGBC TFTs.

In Fig. 2 is shown the output (I_D vs V_D) and transfer (log I_D vs V_G) characteristics of a typical PS-based TGBC DNTT OTFT. The inset in Fig. 2(b) shows the gate-voltage dependence of the device mobility, μ, extracted in the linear regime using the equation

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{WC_i V_D} \tag{1}$$

and in saturation using

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2 \cdot \frac{2L}{WC_i} \tag{2}$$

where C_i is the capacitance per unit area of the gate dielectric layer.

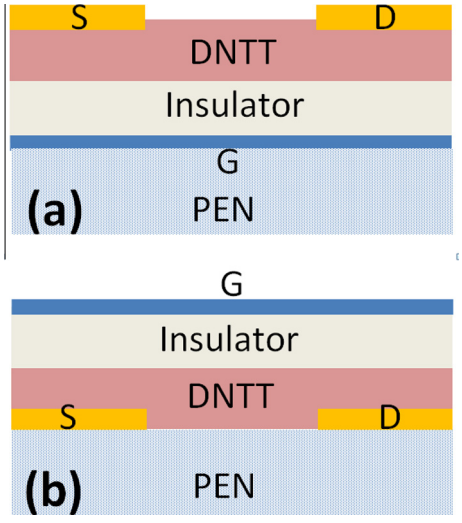

Fig. 1. Cross-sectional diagram of (a) bottom-gate top-contact (BGTC) and (b) top-gate bottom-contact (TGBC) on a PEN substrate.

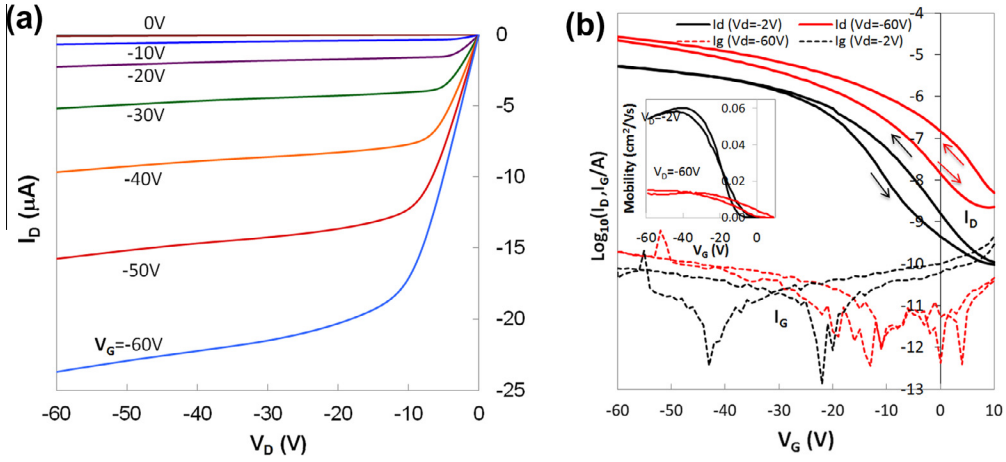

Fig. 2. (a) Output (I_D vs V_D) and (b) transfer (log I_D vs V_G) characteristics for a top-gate, DNTT transistor (W = 15.0 mm, L = 30 μm) with a 1.2 μm thick polystyrene gate insulator. The transfer characteristics were obtained in both the linear (V_D = −2 V) and the saturation (V_D = −60 V) regimes. Shown dotted is the corresponding gate leakage current, I_G. The inset in (b) shows the gate-voltage dependence of the mobility.

Although the gate leakage current, I_G, is low for these relatively large devices, all other performance criteria are poor. The output characteristics do not show good saturation, despite a reasonable linear regime. The on–off current ratio is only ~10^4. While mobility in the linear regime is significantly higher than in saturation, nevertheless, it is still low, rising to a maximum of ~0.06 cm^2/V s, almost two orders of magnitude lower than expected for DNTT [21]. The transfer characteristics are also unstable, displaying anticlockwise hysteresis.

This may be contrasted with the behaviour of BGTC devices (Fig. 3). Now the output characteristics show good linear and saturation regions. The transfer characteristics are stable with little hysteresis. The mobility in both the linear and saturation regimes is ~1 cm^2/V s, which is higher than a previously reported value for vacuum-deposited films of DNTT [21], but with μ_{lin} here slightly greater than μ_{sat}. The combination of higher mobility and lower off-currents leads to an on–off ratio between 10^6 and 10^7. Gate leakage currents are also low at ~10 pA.

This difference in behaviour is readily understood from the AFM images in Fig. 4. Here is shown the surface topography of a DNTT film evaporated directly onto (a) PEN film, (b) the gold electrode and (c) PS. On PEN and PS the DNTT grain size is similar. On the PEN substrate, the RMS surface roughness of the DNTT surface is 6.4 nm with differences of up to ~12 nm between the peak height of the DNTT grains and the inter-grain troughs. For DNTT on PS it is 9.5 nm with up to ~20 nm between peaks and troughs. On the gold electrode (Fig. 4(b)) DNTT has a finer grain structure with an RMS surface roughness of 3.4 nm. On the other hand, the RMS roughness of the PS film itself (Fig. 4(d)) was only 0.69 nm – an order of magnitude lower. Evidence has already been presented [25] on the importance of interface topography in determining the mobility in pentacene OTFTs. Here, both the interface topography and the low polarity of the PS surface are important, as will be discussed later.

The clear outcome of this study is that the surface of evaporated DNTT is too rough and of insufficiently good quality for top-gate OTFTs, and that the lower mobility in the top-gate case observed in our earlier study of pentacene OTFTs could not be ascribed solely to the effect of electron-beam irradiation. Accordingly, all further work concentrated on bottom-gate top-contact devices, where channel formation occurs adjacent to the much smoother dielectric interface.

Table 1 summarises the average maximum values extracted from plots such as the inset in Fig. 2(b) for μ_{lin} and μ_{sat}. The data were obtained from a 90-OTFT array of bottom-gate OTFTs formed on spin-coated PS. Each value should represent the average and

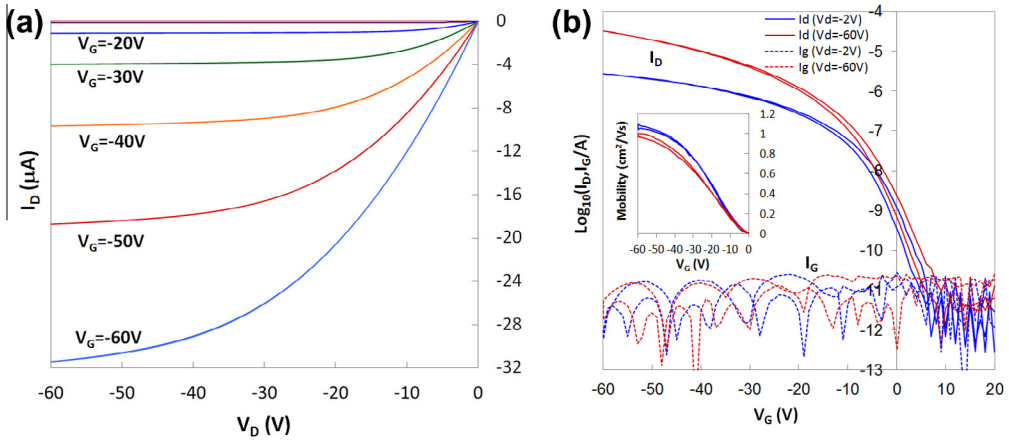

Fig. 3. (a) Output (I_D vs V_D) and (b) transfer (log I_D vs V_G) characteristics for a bottom-gate, DNTT transistor (W = 2.0 mm, L = 100 μm) with a 1.0 μm thick polystyrene gate insulator. The transfer characteristics were obtained in both the linear (V_D = −2 V) and the saturation (V_D = −60 V) regimes. Shown dotted is the corresponding gate leakage current, I_G. The inset in (b) shows the gate-voltage dependence of the mobility.

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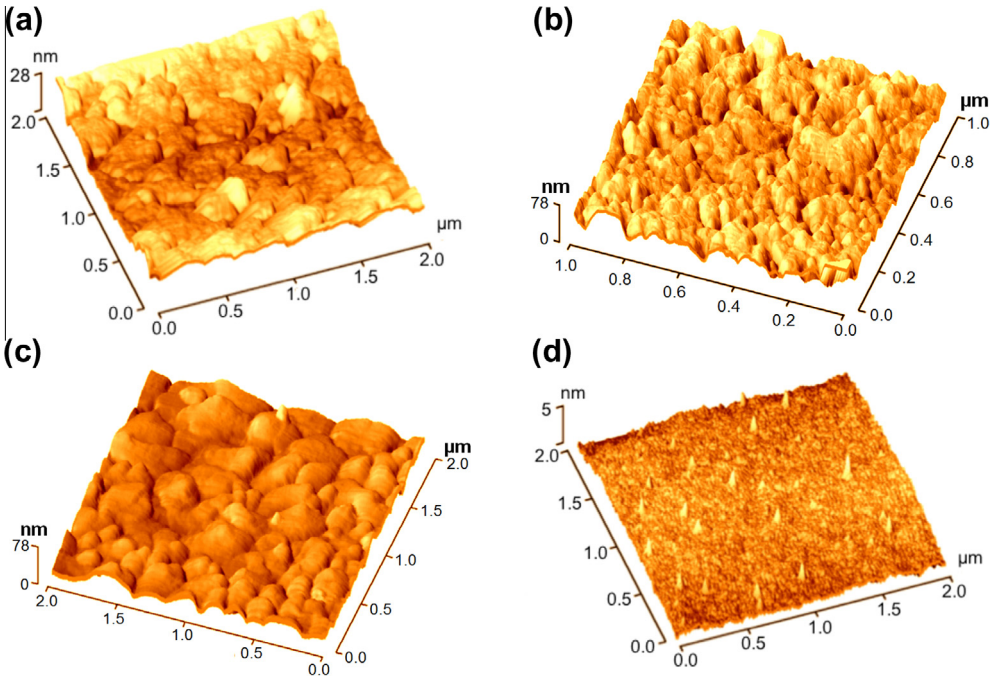

Fig. 4. AFM topographical images of the surfaces of evaporated DNTT on (a) PEN (b) gold and (c) polystyrene. (d) Spin-coated polystyrene on PEN. Over the image areas shown, RMS roughnesses are 6.4, 3.4, 9.5 and 0.69 nm respectively.

Table 1
Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs with a spin-coated polystyrene gate dielectric. Values were extracted from blocks of 9 devices (01–09 or 10–18) arranged in an 18 × 5 array with the device dimensions shown.

		Average maximum mobility (cm^2/V s)				
Row		A	B	C	D	E
L (µm)		50	75	100	150	200
W = 2 mm	01–09 Linear	0.93 ± 0.03	1.12 ± 0.02	1.10 ± 0.04	1.07 ± 0.13	1.06 ± 0.04
	01–09 Saturation	0.94 ± 0.06	1.05 ± 0.05	1.02 ± 0.03	0.98 ± 0.13	0.96 ± 0.05
W/L = 20	10–18 Linear	0.98 ± 0.04	1.12 ± 0.09	1.02 ± 0.19	1.14 ± 0.07	0.92 ± 0.03
	10–18 Saturation	0.96 ± 0.04	1.02 ± 0.07	0.95 ± 0.15	1.02 ± 0.10	0.67 ± 0.20

standard deviation for the 9 OTFTs with the indicated channel dimensions. In practice, however, the number of working devices was only 61, representing a yield of ~68%. Nevertheless, that mobility is independent of channel dimensions confirms the linear dependence of I_D on device dimensions – an important finding for subsequent circuit simulation for which the ability to scale device dimensions is important. Furthermore, the low standard deviation reflects the good reproducibility between devices – again an important consideration for circuit design and simulation.

3.2. TPGDA bottom-gate dielectric

Having established that bottom-gate devices were superior to top-gate, in this section we proceed to investigate the use of vacuum-deposited and plasma polymerised TPGDA as the bottom-gate dielectric with the DNTT evaporated directly onto the TPGDA surface. AFM images show that the RMS roughness of the TPGDA layer was 0.44 nm over an area 3 × 3 µm and even flatter, therefore, than the spin-coated PS surface. Of immediate interest is the improved OTFT yield on the TPGDA dielectric. Every device in the 90-OTFT array operated except for 1 block of 9 common-gate devices, resulting in a yield of 90% indicative of a high-integrity dielectric layer. Typical output and transfer characteristics are shown in Fig. 5.

In both cases, there is significant hysteresis with the output characteristics also showing poor saturation. Interestingly, in the transfer plots, hysteresis is anticlockwise arising from a negative shift of the flatband voltage, a common observation in organic OTFTs owing to interface hole trapping. In saturation, the hysteresis is clockwise and arises from the appearance of a plateau-like feature at $V_G = -25$ V during the negative voltage sweep. The origin of this feature is unclear, but may also be related to the presence of interface states [26].

As above, Eqs. (1) and (2) were used to extract values for the gate voltage dependence of μ_{lin} and μ_{sat}. The average maximum values together with the standard deviations are given in Table 2. These again are relatively low, confirming good reproducibility between devices of the same geometry. Now however, μ_{lin} is less than μ_{sat} in all but one case. Of greater significance is the increase in mobility with decreasing channel geometries. This is particularly marked for the devices in which $W/L = 20$ while L decreases from 200 to 50 µm. For these devices, the extracted μ_{lin} and μ_{sat} are a factor 3–4 higher in the small devices compared to the larger devices. After using a scribe to carefully remove the DNTT from the channel region of one device, a significant source–drain current

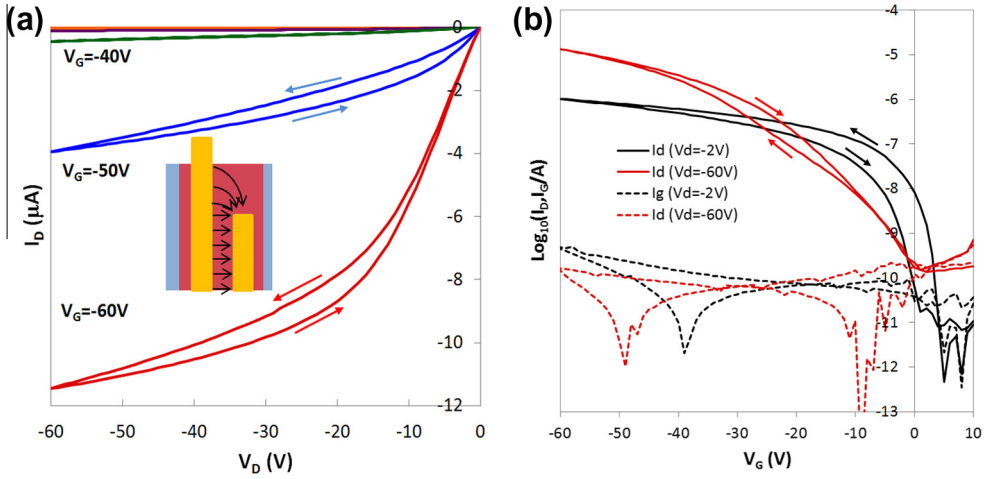

Fig. 5. (a) Output (I_D vs V_D) and (b) transfer (log I_D vs V_G) characteristics for a bottom-gate, DNTT transistor (W = 2 mm, L = 200 μm) with a TPGDA gate insulator (850 nm thick). The transfer characteristics were obtained in both the linear (V_D = −2 V) and the saturation (V_D = −60 V) regimes. Shown dotted is the corresponding gate leakage current, I_G. The inset in (a) shows current flow lines for both the true channel current and the parasitic fringe current outside the main channel area.

Table 2
Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs fabricated on the TPGDA gate dielectric. Values were extracted from blocks of 9 devices (01–09 or 10–18) arranged in an 18 × 5 array with the device dimensions shown.

		Average mobility (cm^2/V s)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
W = 2 mm	01–09 Linear	–	0.40 ± 0.03	0.38 ± 0.03	0.36 ± 0.05	0.22 ± 0.01
	01–09 Saturation	–	0.56 ± 0.03	0.42 ± 0.01	0.33 ± 0.04	0.33 ± 0.04
W/L = 20	10–18 Linear	0.66 ± 0.09	0.41 ± 0.08	0.34 ± 0.06	0.20 ± 0.02	0.15 ± 0.03
	10–18 Saturation	0.79 ± 0.08	0.65 ± 0.13	0.38 ± 0.05	0.27 ± 0.03	0.25 ± 0.01

still flowed. In an identical device excess DNTT was removed from outside the channel region resulting in a corresponding reduction in measured source–drain current. This demonstrates conclusively that the increase in mobility arose from the presence of a parasitic source–drain current flowing outside the channel area (see inset Fig. 5(a)) as discussed for oxide TFTs by Okamura et al. [27]. We conclude, therefore, that in bottom-gate devices fabricated on TPGDA the true mobility is significantly lower than for the equivalent PS-based devices.

Since the surface of TPGDA is extremely flat we may eliminate surface topography as a contributory factor to the low mobility. The most likely origin of the poor performance lies in the highly polar nature of the TPGDA surface. It is well-known [28] that a high-k dielectric surface degrades carrier mobility, with dipolar dispersion of the semiconductor density of states being given as a possible reason [29]. Such effects may be overcome by applying a low polarity passivating layer to the dielectric surface. We have shown [24] that a thin, spin-coated film of polystyrene is particularly effective in passivating TPGDA. X-ray diffraction studies [19] confirmed that the resulting increase in mobility is linked to a significant improvement in the crystal structure of DNTT on the passivated surface. In the following two sections, therefore, we focus on OTFTs and circuit elements fabricated on PS-buffered TPGDA.

3.3. Bottom-gate DNTT OTFTs on PS-buffered TPGDA

The fabrication of 90-OTFT arrays based on PS-buffered TPGDA was achieved at high yield (~90%) but again with 1 block of 9 common-gate TFTs failing [18]. Fig. 6 shows typical output and transfer characteristics of an OTFT from this earlier work. The output characteristics show good linear and saturation regions with no hysteresis discernible in the transfer plots, confirming that the devices are highly stable. The on–off ratio was between 10^6 and 10^7 and gate leakage current, I_G, ~10 pA over most of the voltage ranges. As before, Eqs. (1) and (2) were used to extract the average maximum values and standard deviation of μ_{lin} and μ_{sat} listed in Table 3. This time, μ_{sat} was only slightly greater than μ_{lin} but a tendency for mobility to increase with decreasing device dimensions was again observed, albeit not to the same extent as with the unbuffered TPGDA devices.

As reported earlier [18], in devices in which the parasitic current contribution to the total device current was small, the true mobility estimated from these devices was ~1 cm^2/V s. This is similar to that extracted from transistors formed on the spin-coated PS dielectric (Section 3.1). Since the three sets of mobility data presented in Tables 1–3 were obtained from identical array designs, it appears that the magnitude of the parasitic source–drain currents was dependent on the nature of the underlying dielectric. For all OTFT sizes in the array formed on the spin-coated PS-only dielectric, the parasitic current is negligible. For unbuffered TPGDA, parasitic currents make an increasingly large contribution to the total device current as device size decreases leading to a serious over-estimate of the mobility. This effect is partially mitigated upon passivating the TPGDA with a PS buffer layer. This unexpected observation, which has implications beyond the present work, may be associated with possible polarisation effects occurring in the TPGDA underlying the DNTT outside the channel region. However, further investigations are required to arrive at a definitive explanation.

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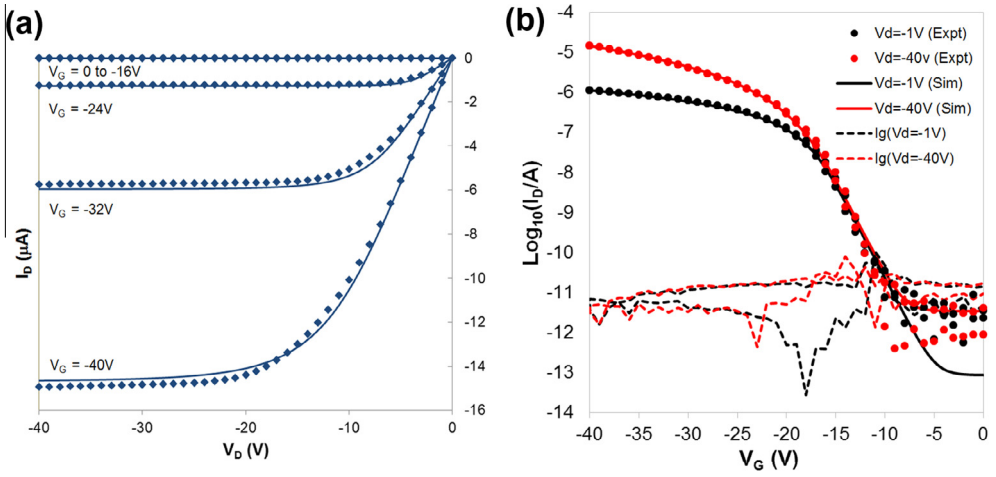

Fig. 6. (a) Output (I_D vs V_D) and (b) transfer (log I_D vs V_G) characteristics for a bottom-gate, DNTT transistor (W = 2 mm, L = 200 μm) formed on a PS-buffered TPGDA surface. The transfer characteristics were obtained in both the linear (V_D = −1 V) and the saturation (V_D = −40 V) regimes. Experimental results are shown by the data points while the solid curves are simulations used for parameter extraction. Shown dotted in (b) is the corresponding gate leakage current, I_G.

Table 3
Average maximum mobility and standard deviation for bottom-gate DNTT OTFTs fabricated on the PS-buffered TPGDA gate dielectric. Values were extracted from blocks of 9 devices (01–09 or 10–18) arranged in an 18 × 5 array with the device dimensions shown.

		Average mobility (cm^2/V s)				
Row		A	B	C	D	E
L (μm)		50	75	100	150	200
W = 2 mm	01–09 Linear	1.24 ± 0.05	1.12 ± 0.13	1.13 ± 0.25	1.16 ± 0.11	–
	01–09 Saturation	1.59 ± 0.09	1.50 ± 0.07	1.39 ± 0.21	1.46 ± 0.07	–
W/L = 20	10–18 Linear	1.36 ± 0.12	1.23 ± 0.08	1.20 ± 0.07	1.08 ± 0.09	0.92 ± 0.01
	10–18 Saturation	1.77 ± 0.20	1.62 ± 0.08	1.50 ± 0.10	1.43 ± 0.06	1.34 ± 0.04

In contrast to the TPGDA-only devices, the characteristics of the PS-buffered TFTs were highly stable. This allowed excellent fits (solid curves in Fig. 6) to be obtained *simultaneously* to both the output and transfer characteristics using Silvaco's UOTFT parameter extraction software. The Silvaco model [30] is an extension of that developed for amorphous and polycrystalline silicon TFTs. Within the framework of a channel conductivity based on variable range hopping and percolation concepts [31,32], the dependence of the effective mobility, μ_{FET}, on gate voltage is given by the equation

$$\mu_{FET} = \mu_{ACC}\left[\frac{V_G - V_T}{V_{ACC}}\right]^{\gamma} \quad (3)$$

Here μ_{ACC} defines the mobility at the onset of strong channel accumulation and V_{ACC} a fitting parameter assumed to be unity in all our simulations. Carrier mobility in the OTFT channel is often dependent on V_G and described by a power-law, with the value of the exponent, γ, reflecting the degree of departure from the ideal (γ = 0) as a result of carrier trapping in the channel. Other parameters required to achieve a good fit are listed in Table 4. The characteristic voltage, V_O, reflects the characteristic energy in the exponential density of trap states in the channel region, including the effects of interface states and influences the subthreshold region of the transfer plots. Not surprisingly then, values extracted for V_O depend on whether measurements are made in air or under vacuum [33]. The parameter λ is a measure of the output conductance in saturation. M_{SAT} and A_{SAT} are fitting parameters which adjust the shape of the output characteristics in the transition region from the linear to saturation regimes, σ_0 the minimum semiconductor bulk conductance and $R_{S/D}$ the zero-bias source/drain series resistances. The parameter values providing the best fit to the OTFT characteristics in Fig. 6 (measured in air) are listed in Table 4 and were used subsequently in a model card for the circuit simulations discussed in the next section.

Table 4
OTFT parameters giving the best fit to the experimental data in Fig. 6.

Parameter	Value	Parameter	Value
W (μm)	2000	γ	0.031
L (μm)	200	λ (S)	0
C_i (F/cm^2)	4.83×10^{-9}	M_{SAT}	3.90
V_T (V)	−17.86	A_{SAT}	1.19
V_O (V)	0.948	σ_0 (S)	8.66×10^{-15}
V_{ACC}	1	R_S (Ω)	0
μ_{ACC} (cm^2/V s)	1.07	R_D (Ω)	0

The simulations confirmed that in strong accumulation, carrier mobility is ~1 cm^2/V s and that the dependence on V_G is weak (γ = 0.031). Furthermore, the source and drain series resistances R_S and R_D respectively are both zero, or at least insignificant compared to the lowest channel resistance, ~3 MΩ measured in devices in which W = 2 mm. Non-zero values of contact resistances, $R_{S,D}$, inserted into the OTFT model resulted in poorer fits to data obtained in air. This contrasts with characteristics obtained under vacuum [33] where W-normalised values giving the best fit were ~19 kΩ cm for R_S and R_D which would correspond to R_S and R_D ~ 200 kΩ for the TFT in Table 4. That both R_S and R_D in Table 4 are significantly lower, presumably reflects in this case the reduced oxygen doping of the bulk DNTT between the contacts and the ends of the accumulation channel. (Molecular oxygen and ozone are known to act as reversible electron acceptors that withdraw electrons from some organic semiconductors creating free holes).

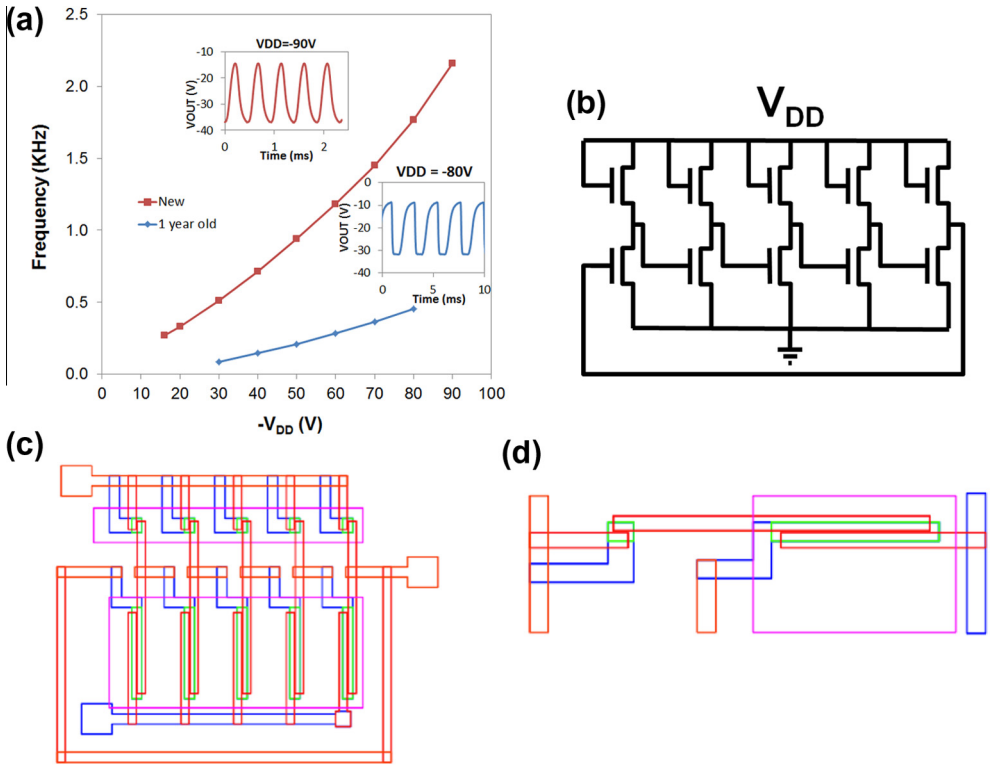

Fig. 7. (a) Output frequency of the 5-stage ring oscillator circuit in (b), plotted as a function of the supply voltage, V_{DD}, soon after fabrication and 1-year later. Also shown as insets are examples of the output signals for $V_{DD} = -90$ and -80 V the highest voltage applied in the two cases. The CAD layout diagram for the oscillator is shown in (c) and one inverter stage in (d). The gate metallisation is blue, the dielectric pink, DNTT is green and exactly overlays the gate electrode, source–drain electrodes are in red. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Interestingly, parameter extraction from a top-gate bottom-contact OTFT using a polystyrene gate dielectric, i.e. similar to that in Fig. 2, yielded much higher values, ~640 kΩ cm, for the contact series resistances [33] presumably reflecting more disorder arising in the finer grain structure in the DNTT above the gold electrode, Fig. 4(b). Such high values of $R_{S,D}$ result in additional degradation of TFT performance to that arising from the rougher DNTT/insulator interface which gave rise to the low value of μ_{ACC} (0.0147 cm^2/V s) and the high value of γ (0.633).

3.4. Logic circuits

Using the same protocols as for the OTFTs fabricated on the PS-buffered TPGDA we have fabricated arrays of basic circuits, all with 100% yield. For example, in Fig. 7(a) is shown the performance of a 5-stage ring oscillator (RO). The RO circuit is given in Fig. 7(b) and the CAD layout diagram in Fig. 7(c). The fabricated circuit began to oscillate with a supply voltage, V_{DD} as low as −16 V. On increasing V_{DD} to −90 V the output frequency exceeded 2 kHz which is significantly higher than achieved with *all-printed* ring oscillators where output frequencies are typically in the range of a few Hz to ~300 Hz [4,8,9,34]. A 7-stage RO ran continuously at $V_{DD} = -60$ V for 8 h with little change in output frequency although a reduction occurred in the output amplitude [18]. Unencapsulated ROs stored in a transparent plastic box under normal laboratory conditions for a month operated as new, showing no signs of environmental degradation. Even after 12 months, the ROs still showed good voltage amplitude albeit operating at reduced frequency (Fig. 7(a)).

Simulations using Silvaco Smartspice and utilising an OTFT model card incorporating the extracted parameters from Table 4, suggested that the ROs should have oscillated at significantly higher frequencies than those observed. For example, at $V_{DD} = -40$ and −60 V, a 5-stage RO should be capable of oscillating at 7 and 20 kHz respectively [18] i.e. more than an order of magnitude higher than observed in practice. It was argued [18] that the discrepancy arose from the parasitic capacitances $C_{gd} \sim C_{gs} \sim 40$ pF originating from the overlap of the source and drain electrodes with the gate electrode as seen in the layout diagram of one of the inverter stages in Fig. 7(d). Here the gate metallisation layer is shown in blue and the dielectric areas in pink. The DNTT areas (green) exactly overlap the gate electrodes. Finally, the source–drain metallisation layer is shown in red.

A range of logic circuits have also been fabricated including inverters, NOR/NAND gates and Set–Reset latches [20] which show switching times in the sub-millisecond range. When parasitic capacitances were included, circuit simulations reproduced closely the observed experimental performance [20]. Even in the presence of high parasitic capacitances, the switching times of our enhancement-load inverters ($t_{rise} \sim 150$ μs and $t_{fall} \sim 25$ μs) are significantly shorter than for the *all-printed* inverters reported by Hambsch et al. [35], the fastest being the complementary inverter in which $t_{rise} \sim t_{fall} \sim 7$ ms. Similarly, the digital circuits reported by Noh et al. [5–7] operated at low frequencies with delays >10 ms. Even inkjet-printed NAND gates formed by printing onto pre-deposited high-resolution electrodes had switching times ~7 ms [36]. While other technologies can produce faster circuits, see for example the recent review by Baeg et al. [37], as indicated earlier, these are not easy to transfer to a roll-to-roll process.

4. Conclusions

In the foregoing we have described the development of a vacuum-evaporation-based approach for the roll-to-roll fabrication of organic electronic circuits. The technology is based on the

vacuum-evaporation and subsequent polymerisation of TPGDA to form the gate insulator. This solventless process led to a high-integrity dielectric layer that significantly improved yield (>90%) compared with a spin-coated polystyrene dielectric (~68%).

The carrier mobility extracted from the characteristics of OTFTs incorporating evaporated films of the organic semiconductor DNTT was seen to be dependent on several factors. BGTC devices employing spin-coated polystyrene as the gate insulator were superior to TGBC devices owing to channel formation at the much smoother semiconductor/insulator interface in the former case. However, a smoother interface on its own was insufficient for achieving high mobility in BGTC DNTT devices formed on the bare TPGDA insulator. The lower mobility and unstable threshold voltage in this case was probably associated with the poorer crystalline structure of DNNT on TPGDA and the highly polar nature of the TPGDA surface.

Buffering the surface of TPGDA with a thin, spin-coated film of polystyrene gave highly stable OTFTs with reproducibly high mobility. In turn this allowed relevant device parameters to be extracted from device characteristics, and a realistic model card obtained for simulating a range of fabricated circuits including ring oscillators and logic gates.

On-going work is now concentrating on developing (a) a vacuum-compatible process for buffering TPGDA and (b) methods for additive patterning of the gate insulator and semiconductor using techniques such as organic vapour jet printing [19]. On successful completion of these next stages, a roll-to-roll process for fabricating organic electronic circuits will have been established, based entirely on vacuum-evaporation.

Conflict of interest

There is no conflict of interest.

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